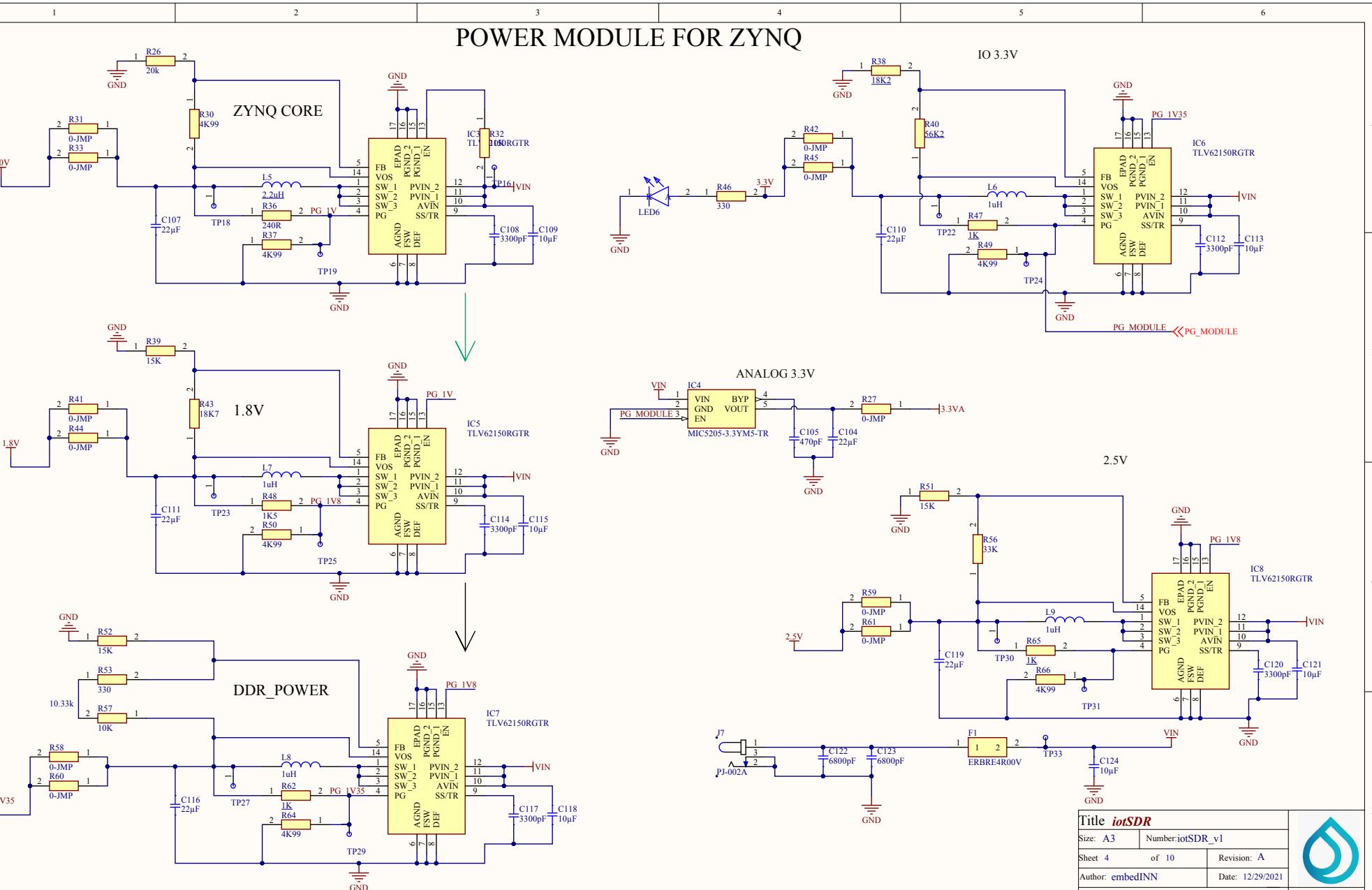
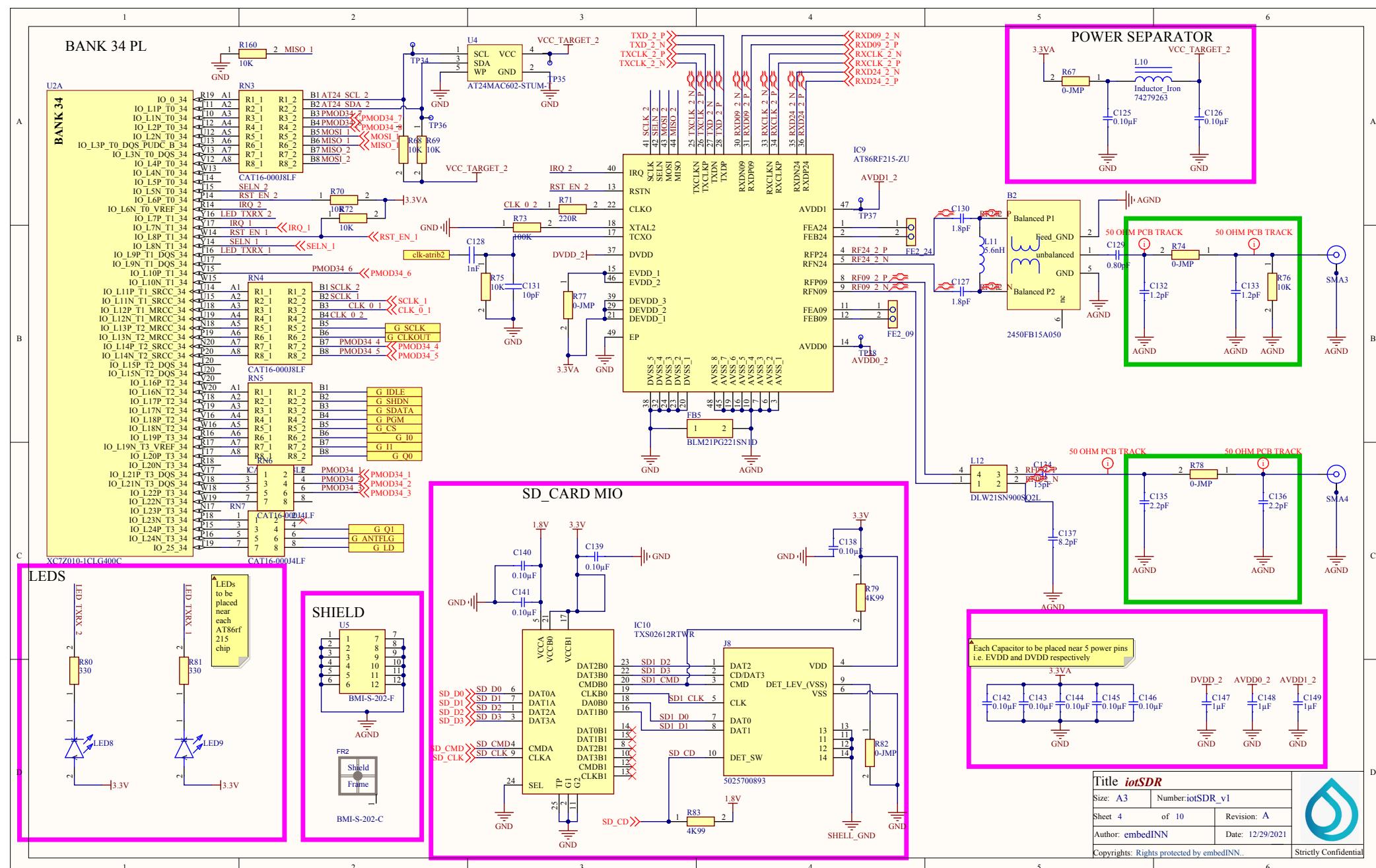


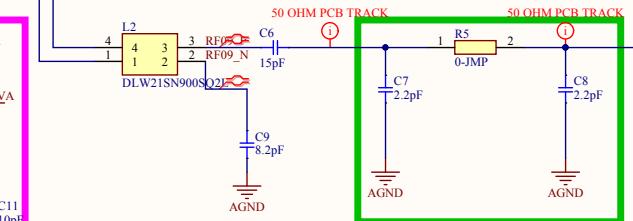
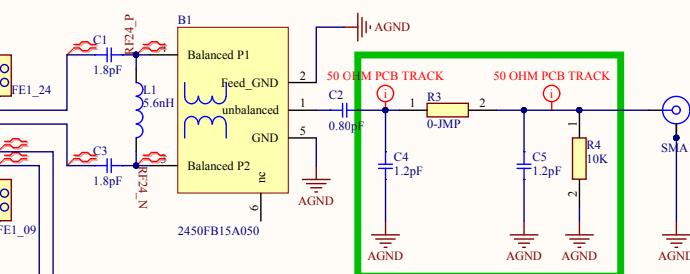
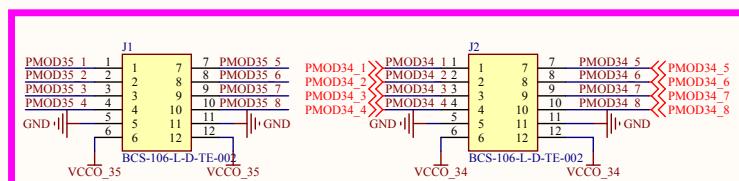
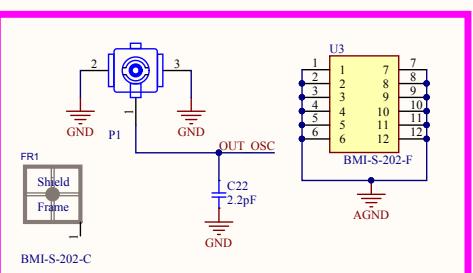
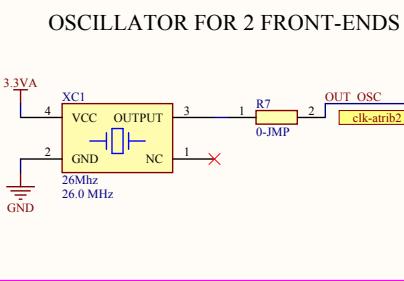
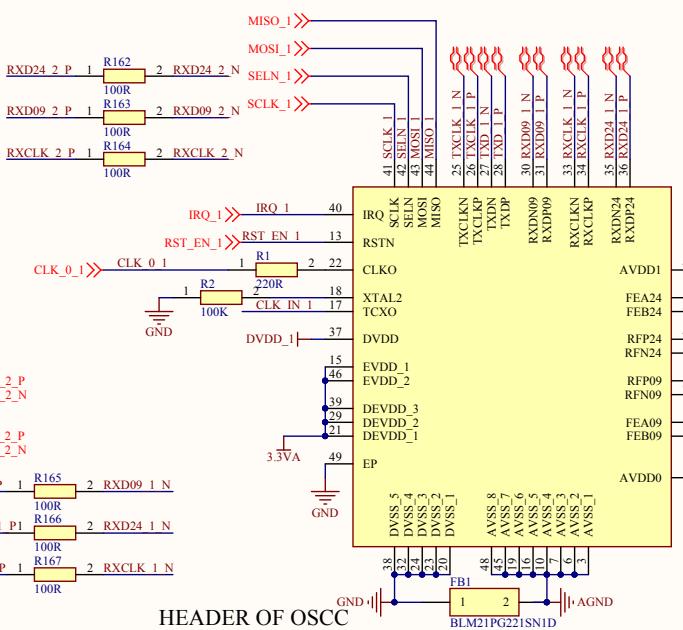
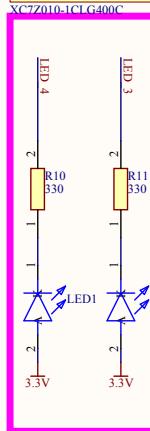
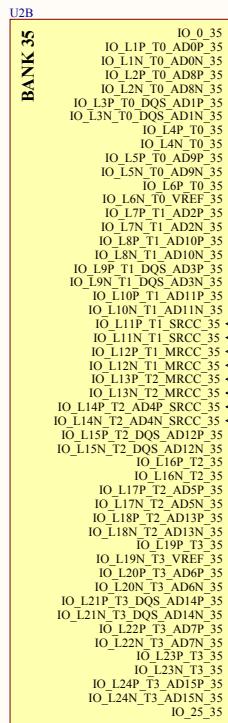
POWER MODULE FOR ZYNQ



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Sheet	4	of 10 Revision: A
Author:	embedINN	Date: <u>12/29/2021</u>
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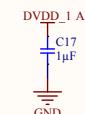
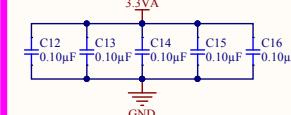


BANK 35 OF PL



DECOUPLING CAPACITORS

Each Capacitor to be placed near 5 power pins
i.e. EVDD and DVDD respectively



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Size: A3 Number: **iotSDR_v1**

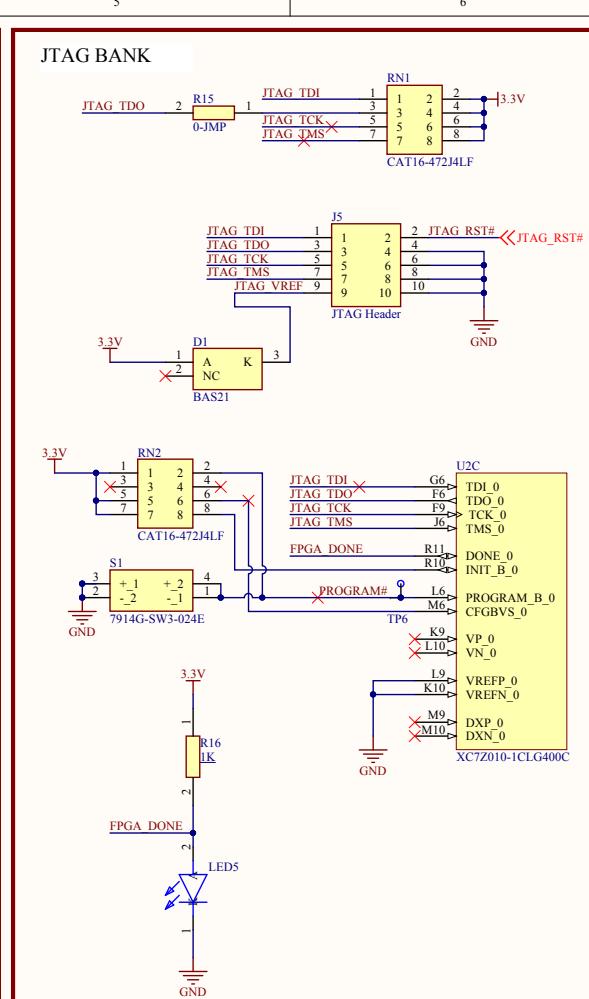
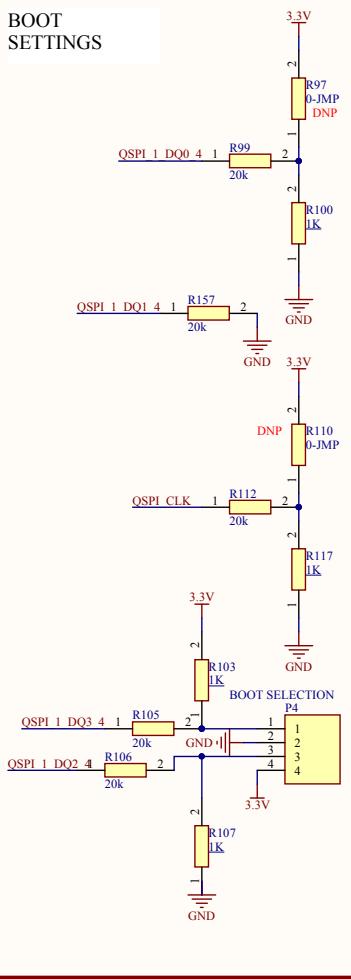
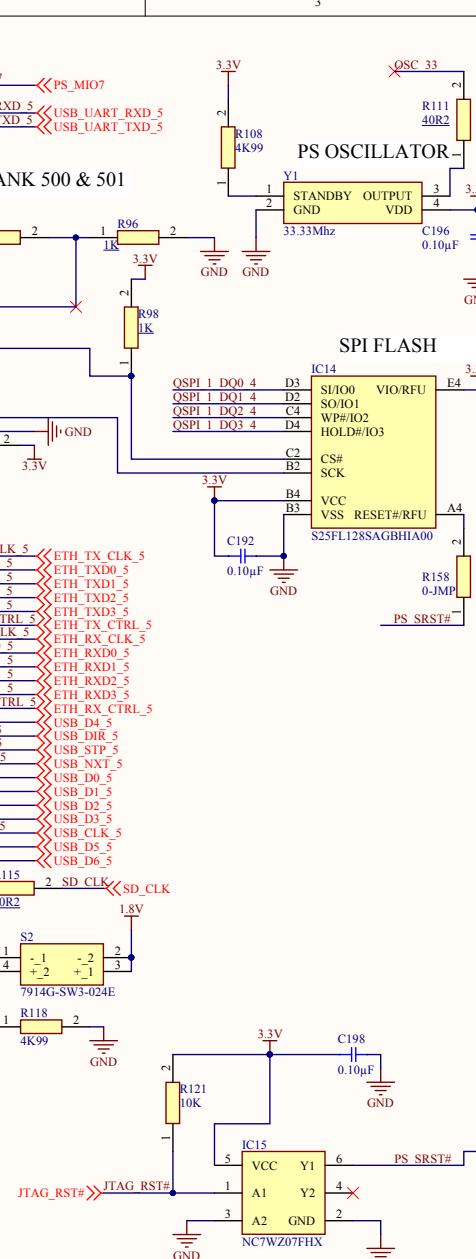
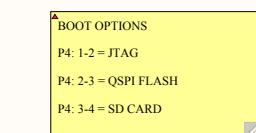
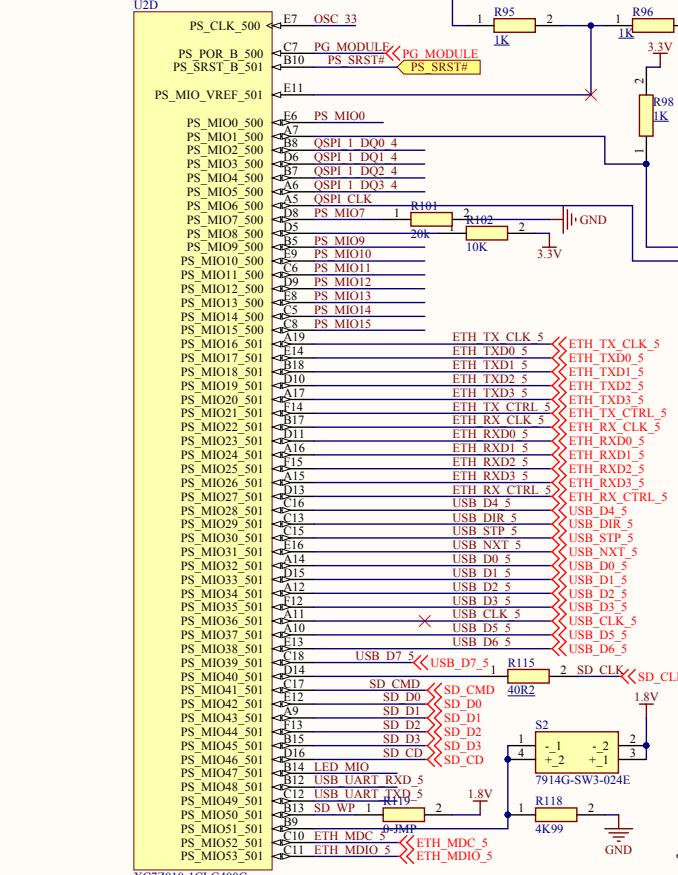
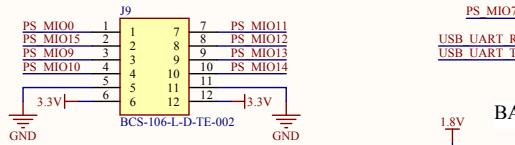
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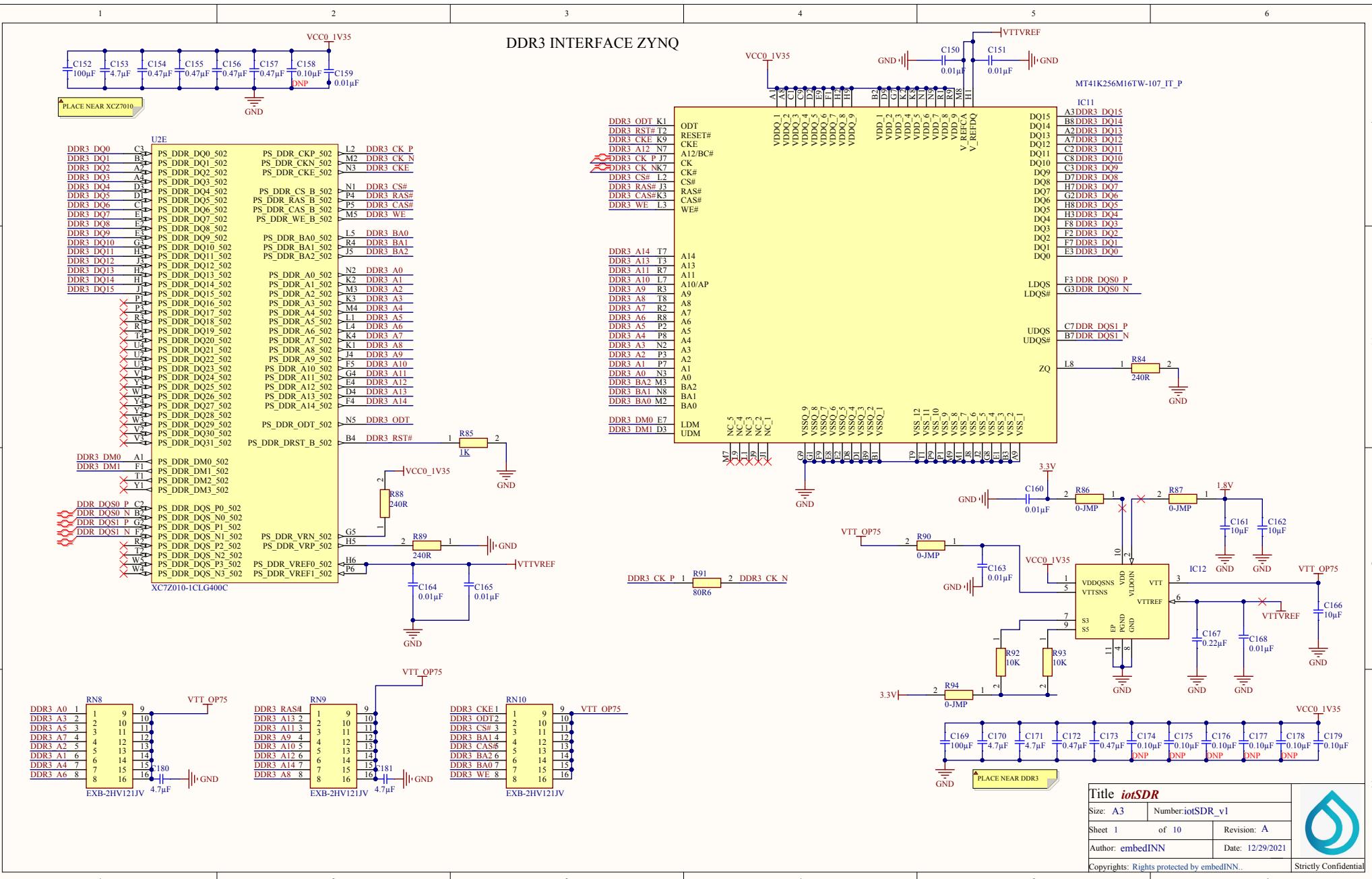
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PS_500_501_0_BANKS



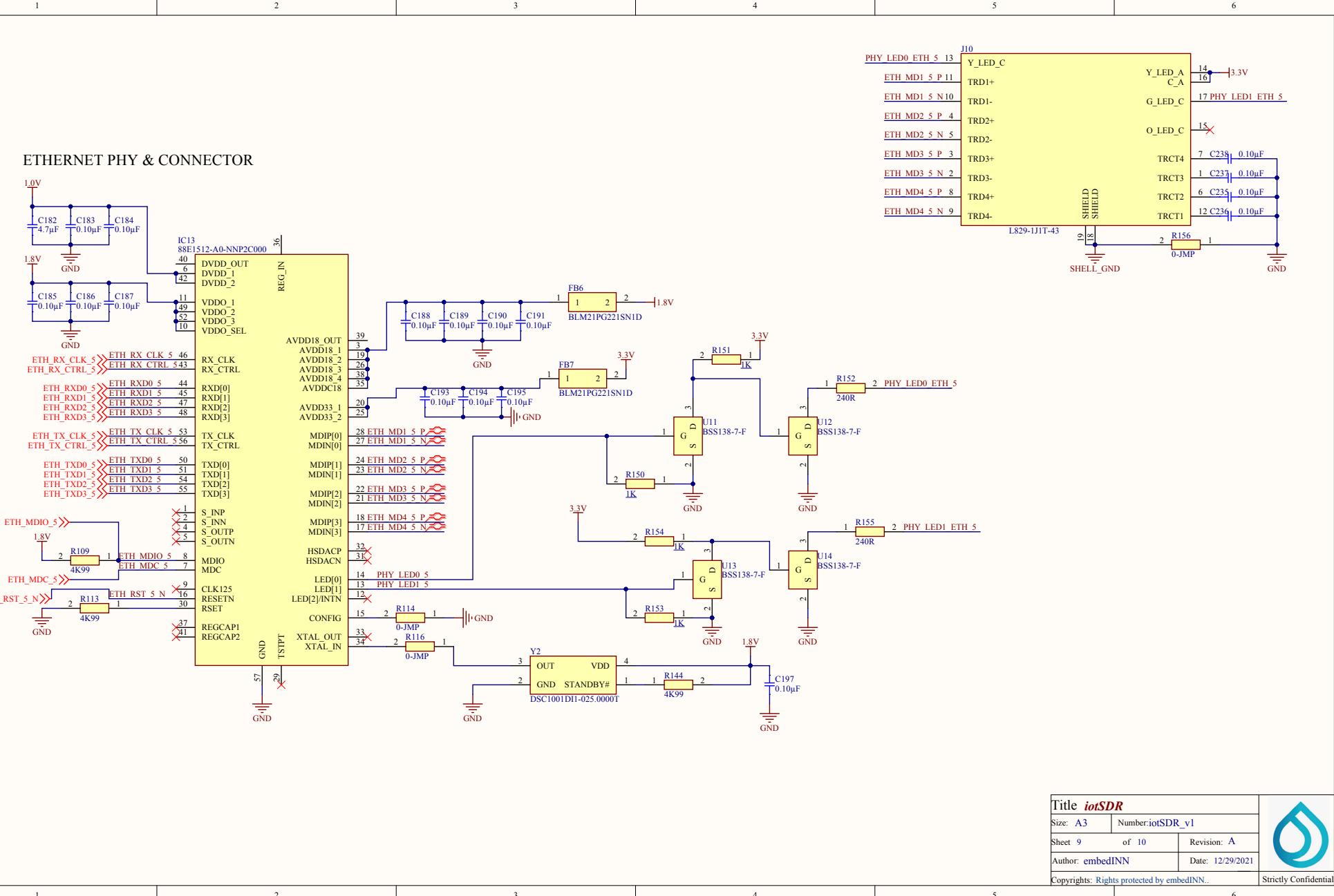
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DDR3 INTERFACE ZYNQ



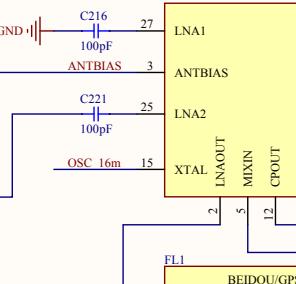
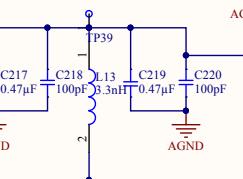
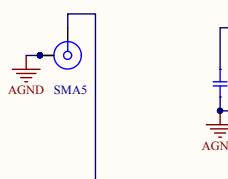
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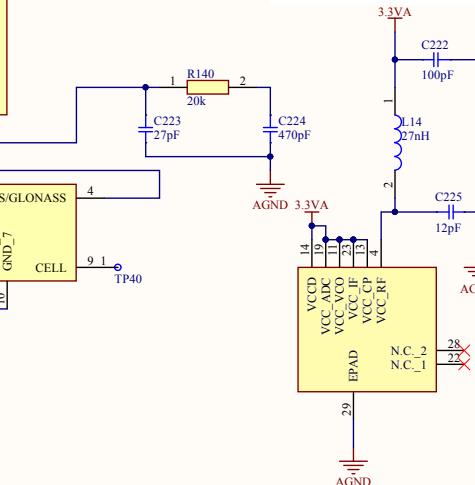




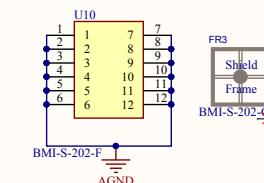
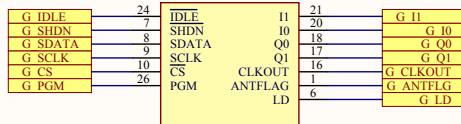
Analog Section Max 2769



Power Section Max 2769

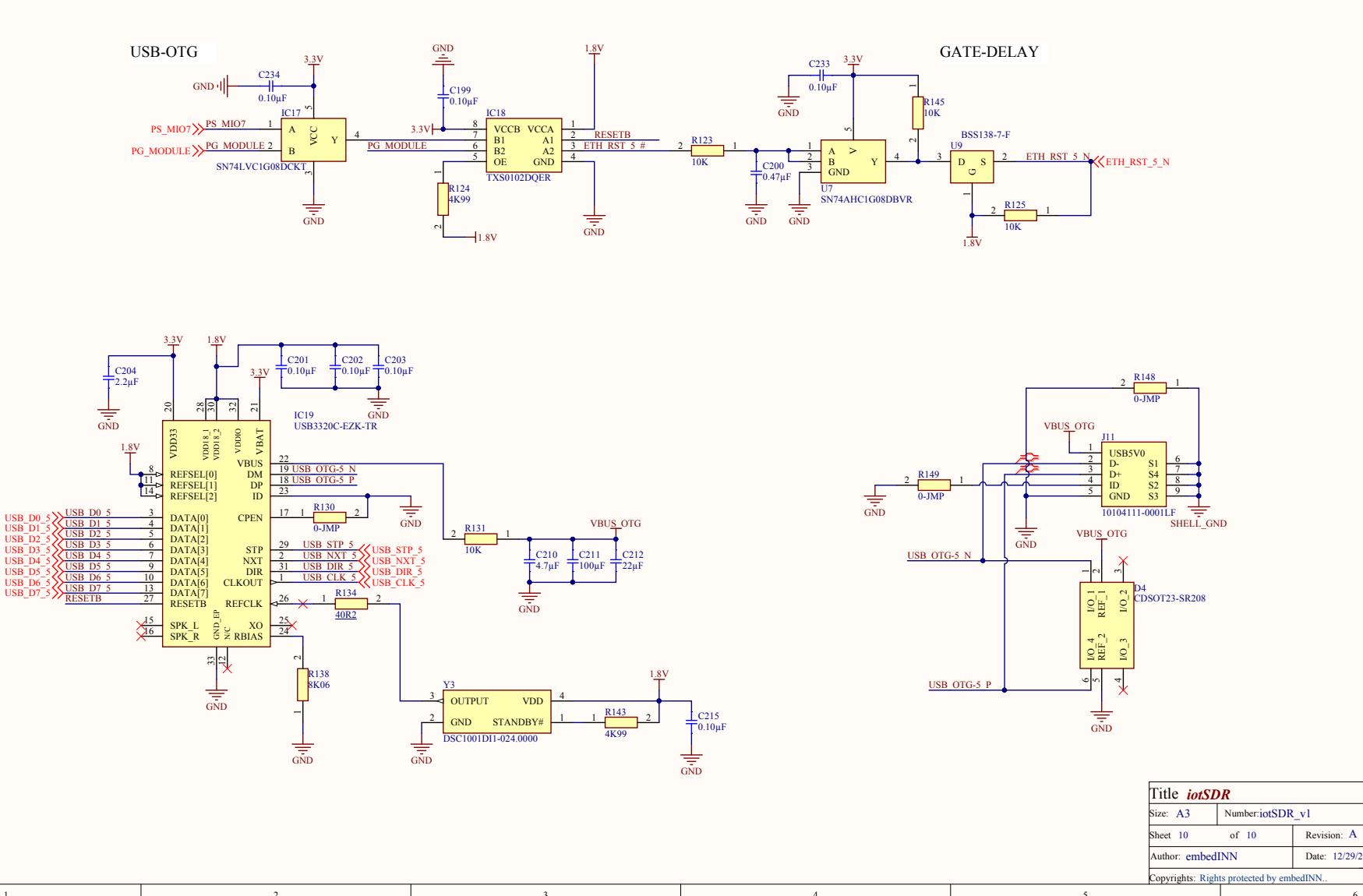


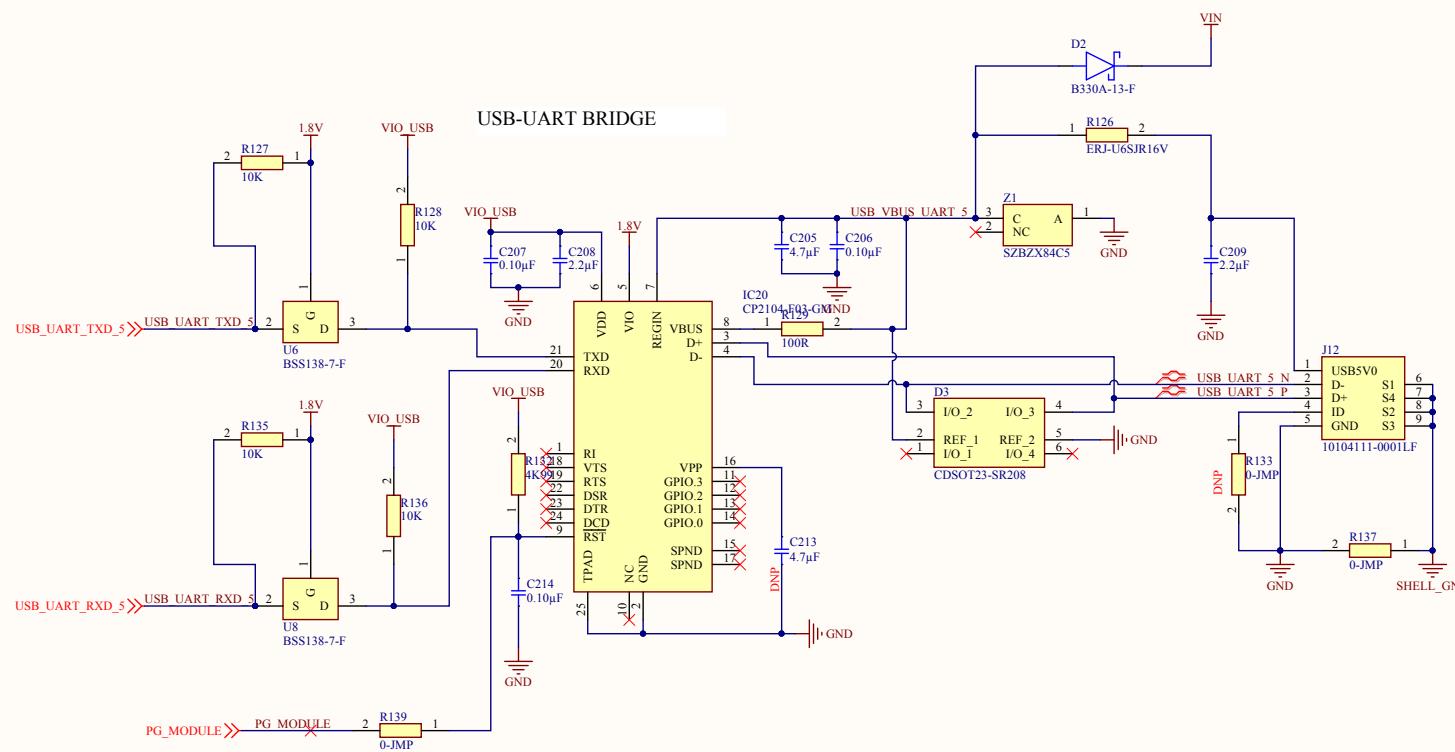
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USB_HS

USB_FS

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