Cortex®-M3 DesignStart™ Eval (AT421)

r0p0-00rel0

Release Note

Cortex-M3 DesignStart Eval Release Note

Confidential Proprietary Notice

Confidentiality Status

This document is Confidential. This document may only be used and distributed in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product status

The information in this document is for a product at Full Release status.

Web address

http://www.arm.com

Feedback

ARM limited welcomes feedback on both the product, and the documentation.

Support for Cortex-M3 DesignStart Eval

Support is not provided with Cortex-M3 DesignStart Eval. However, if you have a question you can post it on the ARM DesignStart community at https://community.arm.com/processors/designstart/.

Feedback on this document

If you have any comments about this document, please send email to errata@arm.com giving:

- The document title
- The document's number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

ARM Internal Document Reference

ARM-EPM-131513 1.0

Contents

1 PRODUCT DELIVERABLES

1.1 Product Release Status

This is a full release of ARM Cortex-M3 DesignStart Eval at revision r0p0. These deliverables are released under the terms of the agreement between ARM and each licensee (the "Agreement"). Use by recipient of the deliverables is subject to the terms and conditions of the Agreement.

1.2 About Cortex-M3 DesignStart Eval

Cortex-M3 DesignStart Eval is intended for system Verilog design and simulation of a prototype SoC based on the Cortex-M3 processor.

Cortex-M3 DesignStart Eval includes:

- An ARM Cortex-M3 processor (as obfuscated RTL)
- An ARM cycle model of the Cortex-M3 processor.
- An example system-level design for the ARM Cortex-M3 processor, based around the ARM Cortex-M prototyping system FPGA platform.
- Reusable AMBA components for system-level development.

Cortex-M3 DesignStart Eval uses a fixed configuration of the Cortex-M3 processor, enabling low cost easy access to Cortex-M3 processor technology by offering a subset of the full product.

The processor in Cortex-M3 DesignStart Eval is delivered as a preconfigured and obfuscated, but synthesizable, Verilog version of the full Cortex-M3 processor and is intended for integration and simulation purposes. It includes debug and the Cortex-M3 ETM within the obfuscated integration level and is not intended for production silicon. The other system level components and peripherals are provided in standard Verilog.

An FPGA bitstream is provided which you can load on the ARM® Versatile™ Express Cortex®-M Prototyping System (MPS2+). This FPGA platform must be purchased separately.

The RTL system integration can be modified, allowing the user to customize logic surrounding the Cortex-M3 processor. Subject to the constraints of the FPGA, a modified system can be synthesized to an MPS2+ bitstream using the Quartus Prime FPGA design tool (using the free or paid versions of this tool).

1.3 ARM Part Numbers for Cortex-M3 DesignStart Eval

The Cortex-M3 DesignStart Eval product is delivered as a single zipped tar file through ARM's IP delivery server.

The following table lists the ARM part number for the Cortex-M3 DesignStart Eval product.

Table *1.3-1*: ARM part number Cortex-M3 DesignStart Eval

Product code	Description	Version
AT421-MN-80001	Cortex-M3 DesignStart Eval Package	r0p0-00rel0

2 INSTALLATION

2.1 Introduction

These installation instructions only cover the UNIX platform/operating system.

2.2 Installation procedure

After download, you will have a single zipped tar file:

```
AT421-MN-80001-r0p0-00rel0.tgz
```

The installation procedure is summarized below:

2.2.1 Unpacking the shipment

The following steps describe how to unpack the Cortex-M3 DesignStart Eval product deliverable.

1. **Relocate the shipment file**

Copy the tgz file to the directory where it is to be installed.

2. **Extract tar files**

Extract the tar file contents using the UNIX GNU tar utility:

```
gtar -zxvf AT421-MN-80001-r0p0-00rel0.tgz
```

NOTE: A version of GNU tar later than 1.13 should be used to untar the deliverables as some versions of tar have problems dealing with very long path names. To find the version of gtar being used type `gtar --version`.

This will extract the deliverables into a directory named the same as the deliverable number: `AT421-MN-80001-r0p0-00rel0`.

2.3 Documentation

The Cortex-M3 DesignStart Eval product includes the following documents which you should refer to for specific tasks:

- ARM® Cortex®-M3 DesignStart™ Eval RTL and FPGA Quick Start Guide, ARM 100895.
  - Run basic tests using an RTL simulator or MPS2+ FPGA platform.

- ARM® Cortex®-M3 DesignStart™ Eval RTL and Testbench User Guide, ARM 100894.
  - Understand the deliverables which integrate a model of Cortex-M3, the CoreLink SSE-050 subsystem, and some basic peripherals. This includes a description of the integration tests.

- ARM® Cortex®-M3 DesignStart™ Eval FPGA User Guide, ARM 100896.
  - Understand how to use the MPS2+ FPGA platform to evaluate software running on the Cortex-M3 DesignStart platform. This includes how to build an updated FPGA image.

- ARM® Cortex®-M3 DesignStart™ Eval Customization Guide, ARM 100897.
  - Understand how to integrate your own peripherals, and make other modifications to the Cortex-M3 DesignStart system.

2.4 License for Keil MDK

A limited term license (with no code size restrictions) for ARM Keil Microcontroller Development Kit (MDK) is available when you register to download Cortex-M3 DesignStart Eval.

2.5 License for ARM Cycle Model

The Cycle model which can be used in simulation requires a license, and uses flexlm as a license manager. Full details of installing the license are provided in the *ARM® Cortex®-M3 DesignStart™ Eval RTL and Testbench User Guide*. This model can only be used on a Linux or UNIX platform.

3 TOOLS

3.1 Tools

This release of Cortex-M3 DesignStart Eval has been developed with the following tools:

- Mentor Questasim 10.4e_1
- Cadence Incisive 15.20.008
- Synopsys VCS 2016.06-SP2
- ARM DS5 5.06.409
- ARM Keil MDK 5.22
- GNU GCC GNU Tools for ARM Embedded Processors (ARM GCC) version 5-2016q2.
- Intel Quartus 16.1

3.2 Operating Systems

This release has been developed with the following operating system:

- Linux RHE6 64-bit
- Microsoft Windows 10

3.3 ARM Keil MDK

If you use ARM Keil MDK for software development, you can install the design kit in a location that is accessible from Linux, UNIX, and Windows. Do this using one of the following procedures:

- Install the design kit on a network drive that:
  - A Linux or UNIX terminal can access.
  - Is mapped to a network drive on a Windows machine.
- Use a personal computer to do the following:
  - Install virtualization software and install a guest Operating System (OS).
  - Set up a shared folder to access the design kit through the host OS.
  - Install the design kit in the shared folder.

Then compile the software with ARM Keil MDK in the Windows environment, and run the simulations in the Linux or UNIX environment.

3.4 Simulation

This release of Cortex-M3 DesignStart Eval supports Linux and UNIX operating systems for the simulation process.

3.5 FPGA Synthesis

FPGA synthesis can be run on Linux, UNIX or Windows operating systems without modification. When working on Windows, you should keep your working area close to the root directory of your drive since the length of paths in the design database can cause problems. This example indicates a typical location which has been confirmed to work:

```
C:\designs\AT421-MN-80001-r0p0-00rel0\m3designstart\fpga
```

4 KNOWN ISSUES AND LIMITATIONS

Please refer to section 1.3 of the ARM® Cortex®-M3 DesignStart™ Eval RTL and Testbench User Guide.

5 DIFFERENCES FROM PREVIOUS RELEASE

This is the first release of this product.

6 SUPPORT

Support is not provided with Cortex-M3 DesignStart Eval. However, if you have a question you can post it on the ARM DesignStart community at https://community.arm.com/processors/designstart/.