Test & Validation Requirements

IP Name: a_ip_wbias_sram_ln28fdsoi

Version – 1.0

Document Versions

VERSION	AUTHOR	DESCRIPTION	DATE
1.1	Nxf44777	Import from a_ip_wbias_sram_ln28fdsoi	05/23/2018

1 Table of Contents

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2 Purpose

This document is intended to outline the IP module level validation and test requirements for **a_ip_wbias_lpcnext_ln28fdsoi**, covering DC parametric, AC, and functional testing. It serves as a vehicle to communicate the validation requirements from Design Engineering entities to the Validation and Test Champions.

This document does identify unique equipment needs and/or high performance and precision measurement requirements for specific validation. This is done to identify critical equipment needs early in the NPI Planning phase. It also includes recommendations for specific board level test fixtures and external components needed to support validation activities.

Finally, this document serves to communicate which critical process parameters, voltage, and temperature ranges that the IP may have sensitivities to, based on circuit topology and the physical implementation of the module.

3 Supporting Documentation

Complimentary information to this document can be found in the IP block guide. The latest versions of this document, the BG and other documentation can be found in the design sync repository bellow. Please observe that this Block Guide is not included as part of the Reference Manual as most part of it was not considered interesting for the customer.

sync://sync-15088:15088/Projects/analogIP_blocks/a_ip_wbias_sram_ln28fdsoi/user_cell/ln28fdsoi/a_ip_wbias_sram_ln28fdsoi/doc

4 IP Overview

a_ip_wbias_sram_ln28fdsoi (BIAS_REG) is a regulator able to supply core logic RVT wells with levels not bounded by supply rails. Reverse Back Biasing (RBB) is available to provide negative back bias for nmos of SRAM, leading to SRAM consumption reduction.

Figure 1 depicts a simplified block diagram of the PMC bias module. In the diagram the several functional sub-modules can be seen with their most important connections, external component connections are also depicted.

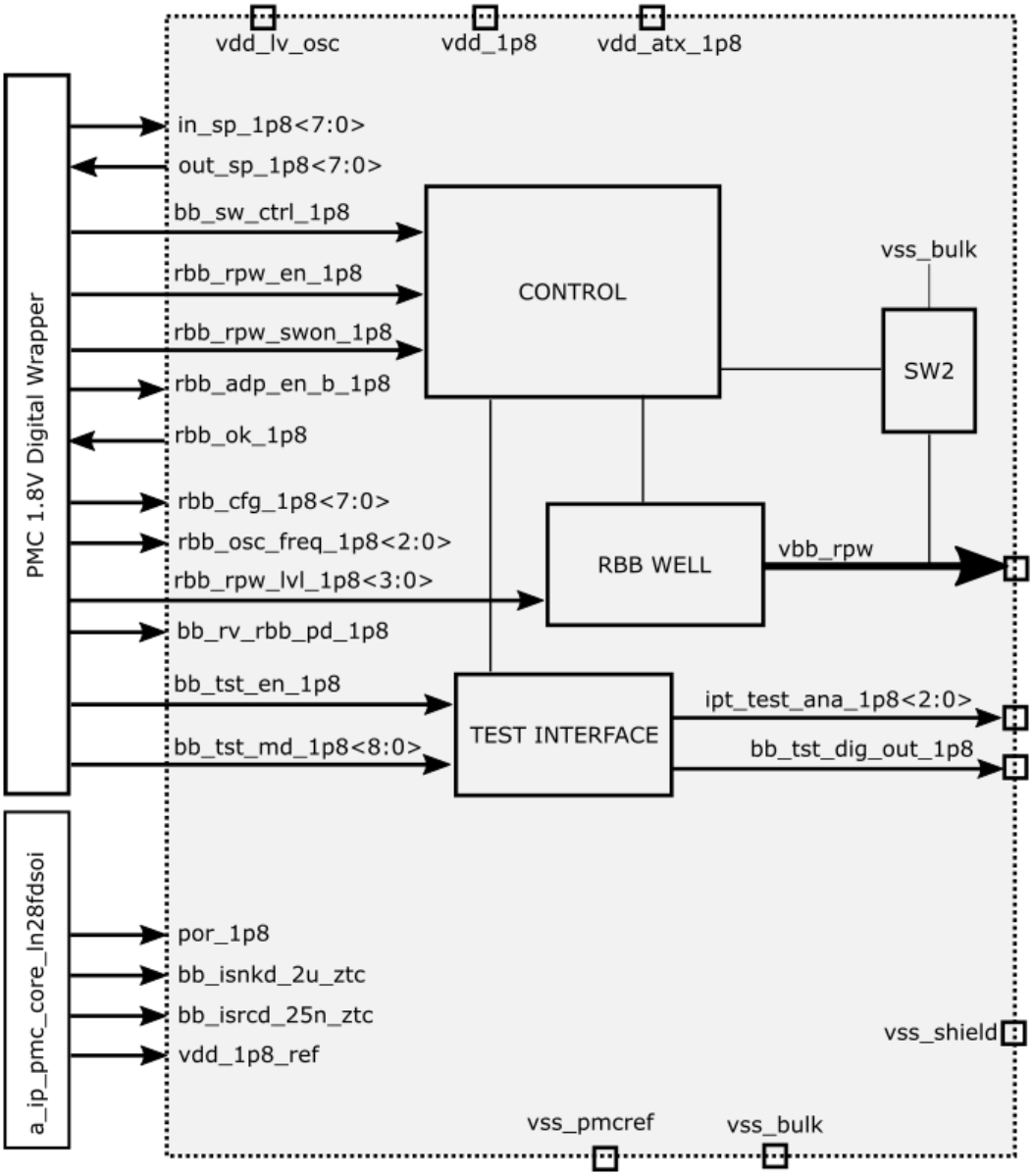

Figure 1 Block diagram for a_ip_wbias_sram_ln28fdsoi

4.1 *RBB Regulation System*

The RBB regulation system is based on controlling the charge injected on output capacitor to keep voltage on this device stable and inside specified range.

Every clock cycle, the reference voltages are generated and compared to the sampled output voltages producing digital control signals that can hold the charge pump clock signals.

In PW regulator, the sampled voltage is obtained by charging a capacitor referred to ground. By changing which terminal is connecting to ground, a sample positive voltage is produced that can be compared to module reference signal. PW RBB output voltage range is from -0.5V to -1.3V.

An additional circuit monitors the comparator output signal. If comparator output stays in the same state for a long time compared to clock cycle, it reduces the clock frequency to save current consumption.

The oscillator frequency can be adjusted in steps of 2 times (i.e., following a geometric progression) from 40 kHz to 5MHz. The circuit topology is supposed to minimize the impact on the frequency due to process variations on core transistors or to supply variation. When the core supply is reduced, the oscillator consumption will decrease but its frequency will remain constant. In adaptive mode (i.e., adp_en_b_1p8 = L), the oscillator frequency is loop controlled by an internal state machine.

5 IP Signal Definitions

The following table summarizes all IP signals that are connected to SoC pins and will be accessible for test and validation. See Integration Guide Tables on section 2.1 and 2.2 for an extensive description of all IP pins. Many supply pins on the table have more than one connection to the IP (supply, sense point, cold sense point, hot sense point, etc.), as those connections are made at SoC level, the respective signals are just listed once in Table .

NAME	TYPE	DOMAIN	DESCRIPTION		
			OFF	RBB	
vdd_1p8*	PWR	-	1.8V	1.8V	1.8-V supply
vdd_lv_osc	PWR	-	0.8V	0.7V	Core supply for oscillator
vss	GND	-	0V	0V	General ground. RBB PW voltage is regulated with respect to the voltage on this pin
ipt_test_ana_1p8<2:0>	A-IO	1.8V	High Z	High-Z	Analog test inout
bb_tst_dig_out_1p8	D-O	1.8V	L	L	Test digital output
bb_tst_en_1p8	D-I	1.8V	L	L	Enable the module Test mode
bb_tst_md_1p8<8:0>	D-I	1.8V	L	L	Test selection bits
bb_sw_ctrl_1p8	D-I	1.8V	L	L	Enables independent control of switches that defines the well voltage. When set to L, the switches will be controlled from D_IP.by the signals: fbb_rnw_swon_1p8, fbb_rpw_swon_1p8, rbb_rnw_swon_1p8, rbb_rpw_swon_1p8.
rbb_rpw_swon_1p8	D-I	1.8V	-	-	RBB PW connection switch control signal
rbb_rpw_en_1p8	D-I	1.8V	L	H	RBB PW regulator enable
rbb_rpw_lvl_1p8<3:0>	D-I	1.8V	L	0x4	RBB PW regulator voltage level selection bits
bb_rv_rbb_pd_1p8	D-I	1.8V	L	H	RBB pull down circuit enable bit
rbb_osc_freq_1p8<2:0>	D-I	1.8V	L	LLL	If adp_en_b_1p8 = L, set the minimum oscillator frequency. If these bits are set to L, the minimal value is selected.
rbb_cfg_1p8<11:0>	D-I	1.8V	LLL	0x000	Miscellaneous control bits, accessible from register
in_sp_1p8<2:1>	D-I	1.8V	LL	L	External FBB enable bits

rbb_adp_en_b_1p8	D-I	1.8V	L	L	Enables the ADP function

Table 1 Signals connected to SoC pins, accessible for test and validation.

5.1 Test Multiplexer

The bb_tst_md_1p8<8:0> bits configure test modes inside the module. It can be shared to all well biasing modules. An 8-bit register must be provided by SoC team to let these bits be configured. It should contain the following fields:

Bits	8	7	6	5	4	3	2	1	0
Description	FLIP_BUFF	MODSEL [3:0] - Module selection				TMOD[3:0] -Test modes inside the module			

Table 2 Test mode selection

MODSEL [3:0] - these 4 bits select which of the internal sub modules is going to be tested.
TMOD [3:0] - these 4 bits indicate which test inside the sub module is chosen. Up to 16 different tests are possible for each module.
FLIP_BUFF - This bit exchange voltage nets the Operational Amplifier (OA) that composes the RBB level test Buffer. This features allows cancelling random OA offset during test procedure with no external adjusting. Parametric Test

6 Test Mode Configuration

bb_tst_md<7:0>		Module selected	ipt_test_ana_1p8			bb_tst_dig_out_1p8
			<2>	<1>	<0>	
1.1 – 1.4	0x00	RBB_CLK	HighZ	HighZ	HighZ	osc_1p8
3.1	0x20	CTRLN	HighZ	anaref (continuous)	ref (continuous)	cmp_ps_b_1p8
3.2	0x21		HighZ	anaref (sampled)	ref (sampled)	cmp_ps_b_1p8
3.3	0x22		HighZ	anaref (sampled)	HighZ	cmp_ps_b_1p8
3.4	0x23		HighZ	pw_sense_out	ref_sampled	ncp_skip_b_1p8
3.5	0x24		HighZ	anaref (continuous)	ref (continuous)	cmp_ps_b_1p8
3.6	0x25		HighZ	anaref (sampled)	ref (sampled)	cmp_ps_b_1p8
3.7	0x26		vss_ref	anaref (sampled)	vdd_1p8_ref	cmp_ps_b_1p8
3.8	0x27		Not used	pw_sense_out	ref_sampled	Not used
3.9	0x28		HighZ	anaref (continuous)	ref (continuous)	cmp_ps_b_1p8
3.10	0x29		HighZ	anaref (sampled)	ref (sampled)	cmp_ps_b_1p8
3.11	0x2A		HighZ	anaref (sampled)	HighZ	cmp_ps_b_1p8
3.12	0X2B		Not used	pw_sense_out	ref_sampled	Not used
3.13	0x2C		HighZ	anaref (continuous)	ref (continuous)	cmp_ps_b_1p8
3.14	0x2D		HighZ	anaref (sampled)	ref (sampled)	cmp_ps_b_1p8
3.15	0x2E		vss_ref	anaref (sampled)	vdd_1p8_ref	cmp_ps_b_1p8
3.16	0x2F		Not used	pw_sense_out	ref_sampled	Not used
4.1	0x30	SENSE VRBB	Not used	pw_sense_out	vdd_1p8	rbb_ok_and_en
4.2	0x31		HighZ	pw_sense_out	vdd_1p8	ncp_skip_b_1p8
4.3	0x32		Not used	pw_sense_out	vdd_lv	rbb_ok_and_en
4.4	0x33		vdd_1p8	pw_sense_out	HiZ	ncp_skip_b_1p8
4.5	0x34		HighZ	pw_sense_out	vdd_1p8	skip_1p8
4.6	0x35		HighZ	pw_sense_out	vdd_1p8	~rbb_ok & rbb_en

4.7	0x36		HighZ	pw_sense_out	vdd_1p8	rbb_ok_1p8
4.8	0x37		HighZ	pw_sense_out	vdd_1p8	sw_ok_1p8
4.9	0x38		HighZ	vss_bulk	vdd_1p8	Not used
4.10	0x39		HighZ	vss_bulk	vdd_1p8	Not used
4.11	0x3A		HighZ	pw_sense_out	vdd_1p8	ok_pw_1p8
4.12	0x3B		HighZ	pw_sense_out	vdd_1p8	s2pw_1p8
4.13	0x3C		HighZ	vdd_1p8_ref	Vss_ref	osc_1p8

Color code:

external voltage	Apply an external voltage to this pin
Test output	Measure the voltage on this pin

Table 3 Test mode outputs

7 Parametric Test Descriptions

Table 4 lists most common operating/test conditions that apply to ULP1 PMC. Throughout this document those conditions will often be referenced by ID. When not specified the supplies must be held to their nominal values.

ID	NAME	MIN	NOM	MAX	UNIT	COMMENT
1	Junction temperature	-20	25	85	°C	
2	1.8-V supply	1.71	1.80	1.89	V	
5		1.62	1.80	1.98	V	Extended range
3	Core supply	0.60		1.00	V	RBB function enabled
6		0.60		1.15	V	Extended range

Table 4 Test conditions

Throughout this document the operating/test conditions will often be referenced by ID. When not specified the supplies must be held to their nominal values. When voltage ranges are specified the test must be performed at the extremes of the range and at nominal.

Table 5 Describes the full test requirement to be performed on Validation bench and Automatic Test Environment (ATE). Please refers to *type* field to categorize production or validation tests. The following type field label detailing is provided as following:

P - Production tests: To be included into test program and tested part-by-part;

C - Characterization test: Not production tests, but desirable to have statistical data to estimate mean and sigma parameters, requiring ATE tester to be performed.

V - Validation tests: Measurements on few parts are required, considering the conditions described on the test.

D – Debug tests: Test to be performed for debug purposes only.

Please also consider:

TST[0]: Analog test bus channel [0];

TST[1]: Analog test bus channel [1];

TST[2]: Analog test bus channel [2] (no available on all SoC's, please check integration);

TDO: Digital test output;

ID	NAME	TYPE	PARAMETER	COND	DIGITAL INPUTS			MIN	MAX	UNIT
1.10	**RBB_OSC_FREQ**	PCV	**OSCILLATOR FREQUENCY** $M = FREQ(TDO)$	P- TYP 1, 2, 3	TM=0x00 rbb_adp_en_b_1p8=1	rbb_osc_freq_1p8<2:0>	000	25	80	kHz
		PCV					001	50	160	kHz
		PCV					010	105	315	kHz
		PCV					011	215	625	kHz
		PCV					100	0.4	1.3	MHz
		PCV					101	0.8	2.5	MHz
		PCV					110	1.7	5.0	MHz
		PCV					111	3.5	10.0	MHz
1.5	**OSC_TRIM**	PCV	**OSCILLATOR TRIMMING @ FMAX** $GOAL: FREQ(TDO) \sim 5\ MHz$	TYP	TM=0x00 rbb_adp_en_b_1p8=1 rbb_osc_freq_1p8<2:0>=7 rbb_cfg_1p8<3:2>=0-4			3.5	10	MHz
2.1	**RPW_CMP_OS_CONT**	D	Comparator offset with test inputs continuously connected. $M = TST[0] - TST[1]$ @transition(TDO)	1, 2	TM=0x20 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0	force_ps=1		-30	30	mV
2.2	**RPW_CMP_OS_SWT**	CV	Comparator offset with sampled test inputs $M22 = TST[0] - TST[1]$ @transition(TDO)	1, 2	TM=0x21 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0			-30	30	mV
2.3	**RPW_INTVREF_ERR**	CV	Internal Reference error $M = TST[1]$ @transition(TDO)	1, 2	TM=0x22 rpw_lvl_1p8<3:0> = 0, 5, 8 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0	force_ps=1	0000	0.59	0.41	V
							0101	1.10	0.90	
							1000	1.41	1.18	
2.4	**RPW_SPL_ERR**	D	Sampler error, with test reference $M = \left(\left(\left(\frac{VDD_{1P8} - TST[1]}{0.4}\right) - 1\right) \times (0.5 + 0.1 \times lvl[0] + 0.2 \times lvl[1] + 0.4 \times lvl[2] + 0.8 \times lvl[3]) - M22\right)$	1, 2	TM=0x23 rpw_lvl_1p8<3:0> = 0, 5, 8 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0					

2.5	**RPW_CMP_OS_CONT**	D	Comparator offset with test inputs continuously connected $M = TST[0] - TST[1]$ @transition(TDO)	1, 2	TM=0x24	force_ps=0		-30	30	mV
2.6	**RPW_CMP_OS_SWT**	D	Comparator offset with sampled test inputs $M = TST[0] - TST[1]$ @transition(TDO)	1, 2	TM=0x25	force_ps=0		-30	30	mV
2.7	**RPW_INTVREF_ERR**	D	Internal Reference error $M = TST[1]$ @transition(TDO)	1, 2	TM=0x26 rpw_lvl_1p8<3:0> = 0, 5, 8	force_ps=0				
2.8	**RPW_SPL_ERR**	CV	Sampler error, with test reference $M = \left(\left(\left(\frac{VDD_{1P8} - TST[1]}{0.4}\right) - 1\right) \times (0.5 + 0.1 \times lvl[0] + 0.2 \times lvl[1] + 0.4 \times lvl[2] + 0.8 \times lvl[3]) - M22\right)$	1, 2	TM=0x27 rpw_lvl_1p8<3:0> = 0, 5, 8	force_ps=0	0000 0101 1000	0.59 1.10 1.41	0.41 0.90 1.18	V
2.9	**RPW_CMP_OS_CONT**	D	Comparator offset with test inputs continuously connected $M = TST[0] - TST[1]$ **@transit(TDO)**	1, 2	TM=0x28 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0	force_ps=1 pre-amp always on		-30	30	mV
2.10	**RPW_CMP_OS_SWT**	D	Comparator offset with sampled test inputs $M = TST[0] - TST[1]$ **@transit(TDO)**	1, 2	TM=0x29 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0	force_ps=1 pre-amp always on		-30	30	mV
2.11	**RPW_INTVREF_ERR**	D	Internal Reference error $M = TST[1]$**@transit(TDO)**	1, 2	TM=0x2A rpw_lvl_1p8<3:0> = 0, 5, 8 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0	force_ps=1, pre-amp always on	0000 0101 1000	0.59 1.10 1.41	0.41 0.90 1.18	V
2.12	**RPW_SPL_ERR**	D	Sampler error, with test reference $M = \left(\left(\left(\frac{VDD_{1P8} - TST[1]}{0.4}\right) - 1\right) \times (0.5 + 0.1 \times lvl[0] + 0.2 \times lvl[1] + 0.4 \times lvl[2] +$	1, 2	TM=0x2B rpw_lvl_1p8<3:0> = 0, 5, 8 bb_sw_ctrl_1p8=1 rbb_rnw_swon_1p8=1 rbb_rpw_swon_1p8=0	force_ps=1, pre-amp always on				

			$0.8 \times lvl[3]) - M22\Big)$							
2.13	**RPW_CMP_OS_CONT**	D	Comparator offset with test inputs continuously connected $M = TST[0] - TST[1]$ **@transit(TDO)**	1, 2	TM=0x2C	force_ps=0, pre-amp always on		-30	30	mV
2.14	**RPW_CMP_OS_SWT**	D	Comparator offset with sampled test inputs $M = TST[0] - TST[1]$ **@transit(TDO)**	1, 2	TM=0x2D			-30	30	mV
2.15	**RPW_INTVREF_ERR**	D	Internal Reference error $M = TST[1]$@transit(TDO)	1, 2	TM=0x2E rpw_lvl_1p8<3:0> = 0, 5, 8	force_ps=0, pre-amp always on				
2.16	**RPW_SPL_ERR**	D	Sampler error, with test reference $M = \Big(\Big(\big(\frac{VDD_{1P8} - TST[1]}{0.4}\big) - 1\Big) \times (0.5 + 0.1 \times lvl[0] + 0.2 \times lvl[1] + 0.4 \times lvl[2] + 0.8 \times lvl[3]) - M22\Big)$	1, 2	TM=0x2F rpw_lvl_1p8<3:0> = 0, 5, 8		0000	0.59	0.41	V
							0101	1.10	0.90	
							1000	1.41	1.18	
1.6	**RPW_AVG**	PCV	**PW AVERAGE VOLTAGE** $M = (TST[0] - TST[1])/0.4) * (0.5 + 0.1 * lvl[0] + 0.2 * lvl[1] + 0.4 * lvl[2] + 0.8 * lvl[3])$	1,2,3	TM=0x31 Use FLIP_BUFF bit	rbb_rpw_lvl_1p8<3:0>	0000	-0.59	-0.41	V
							0001	-0.69	-0.51	V
							0010	-0.79	-0.61	V
							0011	-0.90	-0.70	V
							0100	-1.00	-0.80	V
							0101	-1.10	-0.90	V
							0110	-1.20	-1.00	V
							0111	-1.30	-1.09	V
							1000	-1.41	-1.18	V
1.8	**RBB_OK**	PCV	**RBB TURN-ON TIME** $M = LVL(TDO)$ (ATE) $M = PW(TDO)$ (Validation)	1,2,3	TM=0x36 (ATE)	rbb_rnw_lvl_1p8<3:0> = rbb_rpw_lvl_1p8<3:0>	0000		150	µS
							0001		150	µS
							0010		150	µS
							0011		150	µS
							0100		150	µS
							0101		150	µS
							0110		150	µS

							0111		150	µS
							1000		150	µS
1.1	**VPW_ERR_OFF**	PCV	**PW VOLTAGE ERROR @ OFF** $M = (TST[0] - TST[1]) * 0.5/0.4$	1,5,6	TM=0x31 rbb_rpw_lvl_1p8<3:0>=0000 Use FLIP_BUFF bit			-	100	mV
1.3	**VSS_ ERR**	V	**REFERENCE GROUND ERROR** $M = TST[0]$	1,2,3	TM=0x3C Use FLIP_BUFF bit			-10	10	mV
1.4	**VDD1P8_ERR**	V	**REFERENCE SUPPLY ERROR** $M = TST[1] - VDD\_1P8$	1,2,3	TM=0x3C Use FLIP_BUFF bit			-10	10	mV
4.8	**RBB_TON**	V	PW_ON time	1,2,3	TM=0x35 TDO connected to PAD	rbb_rpw_lvl_1p8<3:0>	0000		150	µS
							0001		150	µS
							0010		150	µS
							0011		150	µS
							0100		150	µS
							0101		150	µS
							0110		150	µS
							0111		150	µS
							1000		150	µS
							1000		150	µS
4.7	**RPW_SW_S2**	D	PW discharge time (s2pw pulse width)	1,2,3	TM=0x3B TDO connected to PAD	rbb_rpw_lvl_1p8<3:0>	0000		10	µS
							0001		10	µS
							0010		10	µS
							0011		10	µS
							0100		10	µS
							0101		10	µS
							0110		10	µS
							0111		10	µS
							1000		10	µS

Table 5 Parametric tests

7.1 *Test Conditions*

Default test conditions are specified for each test and this IP is not verified beyond this range. If SoC specification is a subset of the IP specification, IP can be verified on the extremes of the SoC spec. range only.

7.2 Measured Data Format

When presenting results, identify individual results by its symbol or ID, specifying also measurements conditions for that specific result, i.e. Temperature, Voltages, Register Setting (when looping trough settings, etc.).

Results acquired for different temperatures and supply voltages should be presented separately. For example, for a test performed at -40C, 27C and 125C, with PMC supply voltage of 1.71V and 1.89V, 6 different tables or histograms are expected to be presented.

Most test procedures described in this document involve the measurement of continuous variables (Voltage, current, resistance, time…). For all such cases the expected format for the result depends on the number of samples measured. For small number of samples (<10 samples), results can be presented as a table including all measured values, average, sigma, spec limits. Whenever possible highlight maximum and minimum values found and highlight values outside spec limits using a different color or background.

For tests including larger number of samples results should be presented as a histogram. The histogram must include vertical lines for average, and 6 sigma limits, also for spec limits preferably in different colors. Whenever possible the histogram resolution must be such that all measurements are not collapsed to a few (1, 2, 3 …) bins only. The raw measurements must be stored for later reference and if possible some sort of serialization must be used so results from different tests can be compared for a given sample.

When presenting the histogram for tests with many samples, also present a table including: average, sigma, max, min, spec limits, cp, and cpk. Highlight instances of low cp/cpk values with different background color.

7.3 Test Procedures

For all the testes, provide block supply means:

Supply voltages at vdd_1p8, vdd_lv_osc, vdd_atx_1p8,
Currents bb_iscrd_25n_ztc, bb_isink_2u_ztc.
reference vdd_1p8_ref

7.3.1 OSC – MODSEL= 0x0h

7.3.1.1 RBB_OSC_FREQ

Measure the frequency used by ADP

1) Provide block supply
2) Configure test mode bb_tst_md_1p8<7:0> = 0x00h
3) Set rbb_adp_en_b_1p8=1;
4) Enable test mode, bb_tst_en_1p8=1;
5) Enable RBB, rbb_rnw_en_1p8= 1;
6) Change rbb_osc_freq_1p8<2:0> and measure the resulting frequency on TDO pin.

7.3.1.2 OSCILLATOR TRIMMING @ FMAX (OSC_TRIM)

Find the code that makes the maximum oscillator frequency close to 5MHz. This code must be used for the other measurements unless stated otherwise.

For each condition:

1) Provide block supply
2) Select the maximum oscillator frequency by setting rbb_osc_freq_1p8<2:0>=7;
3) Set rbb_cfg_1p8<3:2>=0;
4) Set rbb_adp_en_b_1p8=1;
5) Enable test mode, bb_tst_en_1p8=1;
6) Enable RBB → rbb_rnw_en_1p8=1;
7) Measure the clock frequency on TDO pin;
8) Repeat step 4 for rbb_cfg_1p8<3:2>=1, 2 and 3
9) Select rbb_cfg_1p8 code for which the clock frequency is closest to 5 MHz → OSC_TRIM

7.3.2 CONTROL – MODSEL= 0x2h

Control sub-module has 4 basic tests to evaluate: switched comparator in 2 specific conditions (offset and total offset including switching parasitic losses), the internal switched reference accuracy and the switched sampler accuracy. This basic group of tests includes the possibilities of testing the regulator under open/close loop conditions (identified by *force_ps* label). And the other condition considers the internal pre-amplifier circuit always on to check pre-amplifier turn time influence.

Both of conditions are setup by the appropriate and different TM. No additional setup needed beside what is indicated in these procedures.

force_ps=0 indicates close loop conditions and *force_ps*=1 indicates open loop conditions.

When open loop test condition is necessary, the SoG wells should be forced the default power net (PWELL to vss_bulk) to avoid biasing issue (floating wells). WELL forcing connection is done by configuring *bb_sw_ctrl_1p8* and *rbb_rpw_swon_1p8* bits according.

7.3.2.1 Comparator offset

The test purpose is to prove the integrity of the comparators used in the RBB control modules. The procedure is the same for PWELL generator, but with dedicated the test mode.

Procedure for each Supply and temperature condition:

1) Provide block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x20 (continuous);
3) Configure the switch control bits:
    - bb_sw_ctrl_1p8=1;
    - rbb_rpw_swon_1p8=0;
4) Enable test mode, bb_tst_en_1p8=1;
5) Enable RBB → rbb_rpw_en_1p8= 1;
6) Source V(ipt_tst_ana_1p8<0>)= *TST[0]*= V1. Tested values are 0.5V, 0.9V and 1.3V.
7) Apply voltage on ipt_tst_ana_1p8<1> = *TST[1]* = V1- 50mV;
8) Monitor TDO signal. Logic state should be HIGH;
9) Increment *TST[1]* in steps of xx mV;
10) If TD0 signal toggles to LOW, measure *TST[1]* => V2 and calculate offset:

    $$M22 = V_2 - TST[0]$$ (log this offset voltage).

    If signal remains in previous state, repeat step 7.
11) Repeat the test with test mode bb_tst_md_1p8<7:0> = 0x21 (sampled)

7.3.2.2 Internal reference error

The test purpose is to measure internal reference error relative to externally applied test voltage reference.

Procedure for each Supply and temperature condition:

1) Provide block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x22;
    - bb_sw_ctrl_1p8=1;
    - rbb_rpw_swon_1p8=0;
3) Select the internal reference level rpw_lvl_1p8<3:0> = rnw_lvl_1p8<3:0> = 0, 5, 8 (test under all these levels);
4) Enable test mode, bb_tst_en_1p8=1;
5) Enable RBB → = rbb_rpw_en_1p8 = 1;
6) Set *TST[1]* = V1 to xx mV under desired voltage V_{ref} value. Tested values are 0.5V, 0.9V and 1.3V (this voltage should match level selected by rpw_lvl_1p8<3:0> = rnw_lvl_1p8<3:0> bits);
7) Monitor TDO signal. Logic state should be HIGH;
8) Increment V1 in steps of xx mV;
9) If TDO signal toggles to LOW, measure *TST[1]*

    $$M = TST[1]$$

    If signal remains in previous state, repeat step 6.

Optionally, the comparator offset can be considered to improve accuracy (M22 to NWELL and M32 to PWELL) is the offset previously tested.

7.3.2.3 Sampler error with test reference

The objective of these tests is to measure error of Pwell sampler, as they enter the comparator inputs. The procedure is the same for PWELL voltage reference, but with dedicated the test mode.

Procedure for each Supply and temperature condition:

1) Provide block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x23;
3) Select the internal reference level rpw_lvl_1p8<3:0> = 0, 5, 8 (test under all these levels);
4) Enable test mode, bb_tst_en_1p8=1;
5) Enable RBB → rbb_rpw_en_1p8 = 1;
6) Set *TST[1]* = V1.Tested values are 0.5V, 0.9V and 1.3V (this voltage should match level selected by rpw_lvl_1p8<3:0>);
7) Measure PW scaled voltage *TST[1]* during 0.1 ms → $TST[1]$
8) Calculate $M = ((VDD1P8 - TST[1])/0.4) * (0.5 + 0.1 * lvl[0] + 0.2 * lvl[1] + 0.4 * lvl[2] + 0.8 * lvl[3])$ → VPW_AVG;

7.3.3 SENSE – MODSEL= 0x3h

7.3.3.1 PW AVERAGE VOLTAGE (VPW_AVG)

Measure the p-well back bias.

For each condition:

1) Provide the block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x3Ah;
3) Enable test mode, bb_tst_en_1p8=1;
4) Enable RBB, rbb_rpw_en_1p8= 1;
5) Wait bb_tst_dig_out_1p8 to assert;
6) Measure PW scaled voltage during 0.1 ms → $TST[1]$
7) Measure vdd_1p8 during 0.1ms → $TST[0]$ (concurrently with $TST[1]$ to save test time)
8) Calculate $M = ((TST[0] - TST[1])/0.4) * (0.5 + 0.1 * lvl[0] + 0.2 * lvl[1] + 0.4 * lvl[2] + 0.8 * lvl[3])$ → VPW_AVG
9) Repeat 4 to 6 with a 1-ms sampling window (validation only - ATE should choose the most appropriate time);

7.3.3.2 RBB_OK

Measure the turn-on time.

For each condition:

1) Provide the block supply

Separated procedures for ATE and Validation purposes:

ATE:

1) Configure the test mode bb_tst_md_1p8<7:0> = 0x36;
2) Enable test mode, bb_tst_en_1p8=1;
3) Enable RBB, rbb_rpw_en_1p8= 1;

4) Measure bb_tst_dig_out_1p8 after maximum spec value → PASS-FAIL test

VALIDATION:

2a) Configure the test mode bb_tst_md_1p8<7:0> = 0x36;
3a) Enable test mode, bb_tst_en_1p8=1;
4a) Enable RBB, rbb_rpw_en_1p8=1;
5a) Measure bb_tst_dig_out_1p8 pulse width → RBB_TON

7.3.3.3 PW peak to peak ripple

Same procedure of test described by VPW_AVG test. May need to filter high frequency noise.

7.3.3.4 PW VOLTAGE ERROR @ OFF (VPW_ERR_OFF)

With the module disabled, measure the p-well voltage error. In this condition, an internal switch shorts the p-well back gate to ground.

For each condition:

1) Provide the block supply
2) Configure rbb_rpw_lvl_1p8<3:0> = 0000
3) Configure the test mode bb_tst_md_1p8<7:0> = 0x3A
4) Enable test mode, bb_tst_en_1p8=1;
5) Measure the PW scaled voltage on ipt_test_ana_1p8[<1> → $TST[1]$
6) Measure the voltage on vdd_1p8 → $TST[0]$
7) Calculate $M = TST[0] - (TST[1] * 0.5/0.4)$ → VPW_ERR_OFF

7.3.3.5 REFERENCE GROUND ERROR (VSS_ERR)

With RBB enabled, measure the reference ground.

For each condition:

1) Provide the block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x3C;
3) Enable test mode, bb_tst_en_1p8=1;
4) Enable RBB → rbb_rpw_en_1p8
5) Measure the voltage on ipt_test_ana_1p8<0> → VSS_ERR

7.3.3.6 REFERENCE SUPPLY ERROR (VDD1P8_ERR)

With RBB enabled, measure the reference supply.

For each condition:

1) Provide the block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x3C;
3) Enable test mode, bb_tst_en_1p8=1;
4) Enable RBB → rbb_rpw_en_1p8
5) Measure the vdd_1p8_ref voltage on ipt_test_ana_1p8[<1>] → $TST[1]$;
6) Measure the voltage on vdd_1p8 → VDD_1P8;
7) Calculate $TST[1] - VDD\_1P8$ → VDD1P8_ERR;

7.3.3.7 RBB_TON

1) Provide the block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x35;
3) Enable test mode, bb_tst_en_1p8=1;
4) Enable RBB → rbb_rpw_en_1p8
5) Measure the time on TDO
6)

7.3.3.8 RPW_SW_S2

1) Provide the block supply
2) Configure the test mode bb_tst_md_1p8<7:0> = 0x3B;
3) Enable test mode, bb_tst_en_1p8=1;
4) Enable RBB → rbb_rpw_en_1p8
5) Measure the time on TDO

8 Special Equipment Considerations

8.1 Instruments

Where not specified measurement, accuracies are expected to be:

- 0.1% for voltages
- 0.1% for timing
- 0.5% for currents

8.2 On-Board Hardware

Please refer to for information regarding specific board level test fixtures and external components needed to support validation activities.