

QuestaSim Simulator Summary

QuestaSim is the new name for the *ModelSim* simulator. *QuestaSim* may be invoked on a verilog file as, `vsim VerilogFile.v`; or, on a text file containing a design-file list as,

```
vsim -f ListFilename.vcs
```

The file may have any extension, but we use `.vcs` here for consistency with *VCS*.

To run the Intro (Lab01) simulation, be sure you are in the `Lab01` directory.

1. Invoke `vsim -f IntroTop.vcs`; this will load all source files but will not itself compile anything.

A new **project** optionally also may be created for version tracking, but we ignore that here. All that is necessary to do a lab here is (a) to compile the design, (b) to decide what to add to the display in a waveform window, and then (c) to run the simulation.

2. Use the *QuestaSim* top menu bar

```
[Compile]/[Compile...]
```

form to highlight the design files which were read, and pick the lower-right "Compile" button. Errors (there should be none) will be displayed in the main text window. Then, pick "Done" to finish the compilation. You will see a new Workspace library named `work`. *QuestaSim* always creates a working library named `work` in the current directory; this is where the compiled design will be stored.

3. To choose what to simulate, first display the compiled design hierarchy by picking

```
[Simulate]/[Start Simulation...]
```

on the top menu bar. The form will list a lot of irrelevant libraries, but all we care about is the top one, named `work`. Open that `[+]` line and pick `TestBench`, which is our testbench module name. The name `work.TestBench` automatically will appear on the Design Unit(s) line. Pick "OK" to dismiss the Start Simulation form and elaborate the design.

4. Soon after you pick "OK", a new Objects window will appear with the simulation hierarchy displayed. Your design now is ready to be simulated, but you must choose what to see.
5. Select all signals in Objects; then, on the top menu bar, pick

```
[Add]/[Wave -->]/[Selected Signals].
```

If you want to see everything, pick `[Add]/[Wave -->]/[Signals in Design]` instead. A wave window will appear; pick the little square in its upper right corner to decouple it from the main *QuestaSim* window.

6. To run the simulation, on the top menu bar, pick

```
[Simulate]/[Run...]/[Run - All]; but,
```

DO NOT pick `[Yes]` when prompted "Are you sure you want to finish?". Instead, `[No]` this message box. `[Yes]` terminates *QuestaSim*.

7. Use the filled magnifying-glass icon to zoom full. When you have seen the waveforms, use the `vsim` window's top menu bar to pick `File/[Quit]`.

In current software, the main advantage of *QuestaSim* over *VCS* is that *QuestaSim* can display the contents of a verilog memory, all addresses at once. *VCS* can not do this, although *VCS* correctly will simulate address and data operations on a memory.