VCS Simulator Summary

Your startup environment includes this alias:

```
alias vcs='vcs -RI +charge_decay +memcbk +pathpulse +v2k'
```

To remove this alias (you usually would not want to), invoke `\vcs` instead of `vcs`.

You must provide a valid verilog file name when you invoke VCS; if the file has a serious syntax error, VCS will exit immediately with an informative error message.

For one verilog file, invoke `vcs` *filename*

To invoke VCS on a design of several files, the names (with path if necessary) must be listed top-down in a file. Then, invoke VCS on the file (using `-f`):

```
vcs -f file_with_design_files_listed
```

Graphical UI hints (for Introductory Lab 1):

Immediately after invoking `vcs -f Intro_Top.vcs`

notice in the GUI that the current simulation time of 0 appears at the bottom of the `Interactive Window`; it is in 100-ps units, as specified in `TestBench.v`. VCS always pauses at time `0`. Also notice that the scope is `TestBench`, which contains the top of the design as a verilog module instance.

To run the Intro simulation,

1. Open a `Hierarchy Browser` window, using the menu bar along the top. On the left of the new window, pick [+] to display the design hierarchy. If no [+] appears, pick [*Sim*] on the menu bar and [*Rebuild & re-exec*] to reestablish communication.

   Note: We shall not be concerned with the `Register Window` or `Logic Browser`.

2. Use the top menu bar to open a `Wave Window`. Then, holding down the middle mouse button, drag the text "`TestBench`" from the `Hierarchy Browser` window into the `Wave Window`. The dragged image should turn color in the area where it is allowed to drop the text.

3. Pick [*continue*] or [=>] with the mouse. This runs the simulation. Notice that the time now is 5,540 x 100 ps = 554 ns.

4. View the simulation results. To zoom on the entire simulation waveform, in the `Wave Window`, pick the small [z%] button and choose "100%" on the popup menu. You should see the initially unknown '`x`' and '`z`' states on the left, and the various top-level input and output wave shapes as the simulation proceeded.

5. Reminder: If you change anything in a design, always run `Rebuild & re-exec` from the `Sim` menu to compile and view your changes. Try this now.

6. After seeing that the simulation has run again, use the `File`/[`Exit`] menu choice to close all VCS windows at once. Don't bother saving configuration when prompted.

***Special hints (for labs after Lab 1)*:**

When simulating a netlist using a verilog library file of numerous component models, it is useful to add "`-v` " before the library line in the `.vcs` file: VCS compiles only those models actually in the design. Use `vcs -help` to see all available VCS options.

On exitting the VCS GUI, if you save configuration to a *some_name*`.cfg` configuration file, you can program the VCS GUI to start with the saved window setup and waveform signals by adding "`+cfgfile+`*some_name*`.cfg`" to your VCS command alias. "`+cfgfile+default.cfg`" works well.