Signal Chain Benchmarking – ACI Motor Control Application

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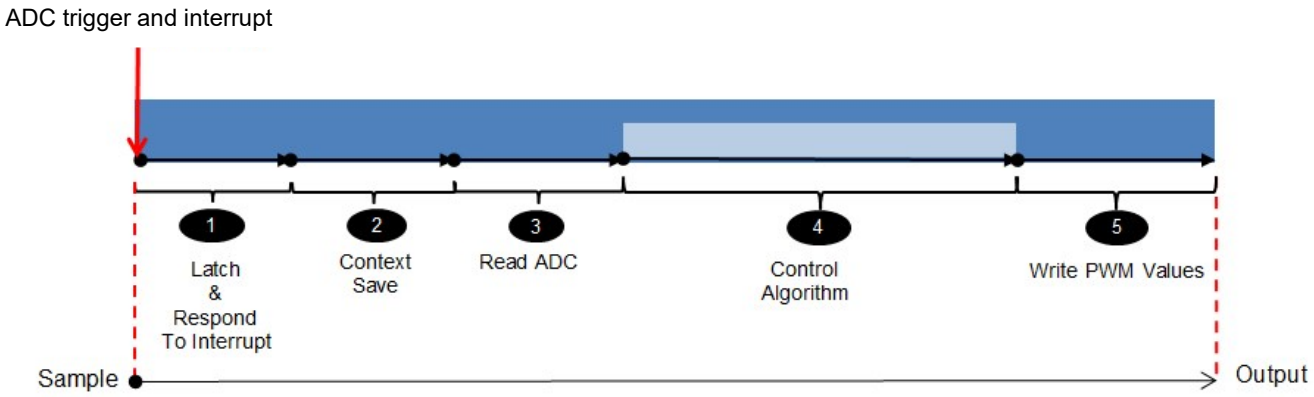
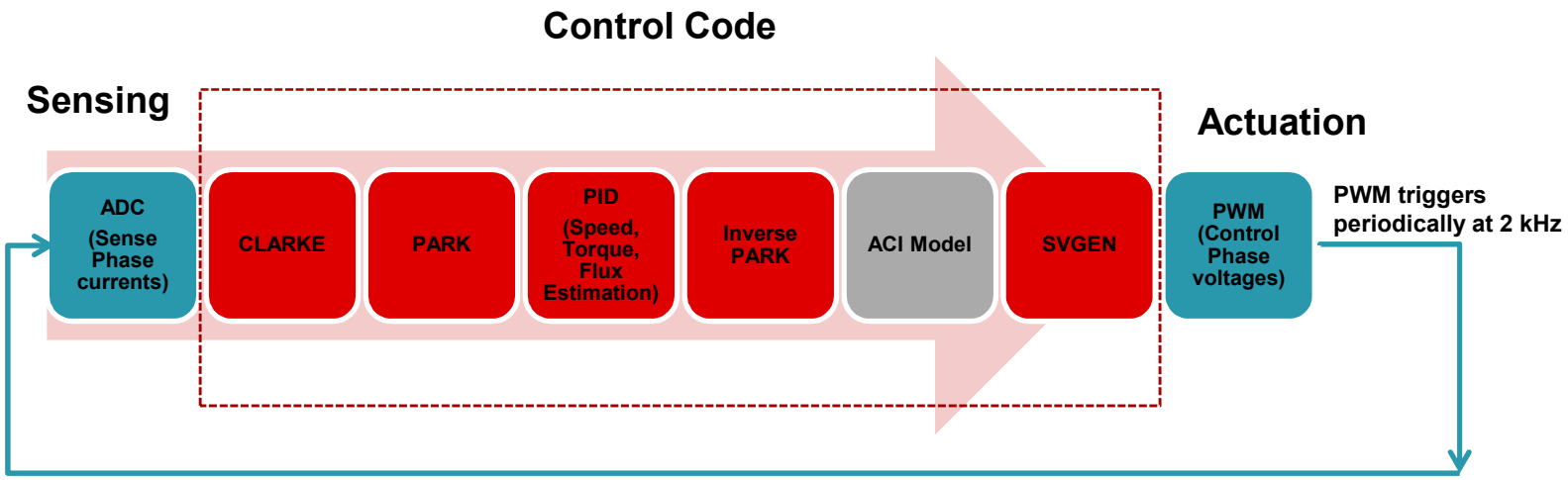
Signal Chain is the sample to output response



Benchmark application representative of real sensorless AC Induction Motor Control application

No special HW needed, SW based solution (C Code)



Application executes 1024 iterations of the real-time loop (sensing + control code + actuation) and outputs min, max and average execution cycles.

Cache based systems introduce large variance

- Flash execution with **No cache** (with wide prefetch, lookahead prefetch)

Device	CPU Clock (MHz)	Cache	Benchmark – Min (usec)	Benchmark – Max (usec)	Variance (usec)
C28	200	No	2.84	3.03	**0.19**

- Flash execution with L1 Instruction and Data Cache - **Cold cache vs Hot cache**

Device	CPU Clock (MHz)	Cache	Benchmark – Min Warm cache (usec)	Benchmark – Max Cold cache (usec)	Variance (usec)
M7	480	Yes	3.98	6.63	**2.65**

ADC architecture impacts real-time response

- Sequential scan – Application has 2 ADC channels in a sequence
  - C28: Multiple ADC results registers: Results can be read directly from register bank
  - M7 : Single ADC results registers: Needs DMA to prevent overrun
- Interrupt response
  - C28: ADC early interrupt: after 1st channel sampling completes
  - M7 : DMA interrupt: DMA buffer half-full or full

Device	CPU Clock (MHz)	ADC Clock (MHz)	CPU HW INT (cycles)	ADC with DMA	Benchmark ADC INT Response [ADC sampling + CPU HW INT + Compiler context save] (cycles)
C28	200	50	14	No (INT – 1st chan sampling complete)	**57** (10.6% of total cycles 537)
M7	480	50	12	Yes (INT – DMA half full)	**198** (17.3% of total cycles 1143)

Jitter fairly small for both devices

- Variance in ISR execution of 1024 iterations

Device	Benchmark – Jitter (cycles)
M7	**20** (Flash with cache) **10** (Tightly Coupled RAM)
C28	**12** (Flash) **12** (RAM)

Thank You.