SystemVerilog Tools in Python

Michał Czyż PG ETI UE CHIP The Other Dude His Company / University

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Abstract

Documentation for SystemVerilog Tools project available at: https:www.github.com/emcezet/sv-tools

1 Introduction

The goal of project is to develop parsing engine for a subsystem of SystemVerilog (SV) Hardware Description Language (HDL) and provide following utility:

- module generation from user-defined templates,
- module instantiation from user file,
- top level file generation from user files,
- simple testbench file generation.

Both named port and interface style are accepted.

2 Acceptable constructs in SystemVerilog.

2.1 Formal syntax.

Formal syntax descriptions use Backus-Naur Form (BNF). This notation was also used in Annex A of [1]. Revised and limit list of supported constructs is provided in this section. Please note, that a specific coding style is expected from users. Curly brackets '{' and '}' denote one or more occurrence and square '[' ']' denote optional.

```
⟨source_text⟩ ::= [timeunits_declaration] {description}
⟨description⟩ ::= ⟨module_declaration⟩
| ⟨interface_declaration⟩
⟨module_declaration⟩ ::= ⟨module_nonansi_header⟩ [ timeunits_declaration ] module_item ⟨endmodule⟩
[ : ⟨module_identifier⟩ ]
| ⟨module_ansi_header⟩ [ timeunits_declaration ] non_port_module_item ⟨endmodule⟩ [ : module_identifier ]
⟨module_nonansi_header⟩ ::= attribute_instance ⟨module_keyword⟩ [ lifetime ] ⟨module_identifier⟩ package_import_declaration [ parameter_port_list ] ⟨list_of_ports⟩ ';'
⟨module_ansi_header⟩ ::= attribute_instance ⟨module_keyword⟩ [ lifetime ] ⟨module_identifier⟩ package_import_declaration [ parameter_port_list ] [ list_of_port_declarations ] ;
⟨interface_declaration⟩ ::= ⟨⟩
```

3 Usage.

All scripts support -h and -help parameters for usage help.

References

- [1] 8299595,IEEE Std 1800-2017 (Revision of IEEE Std 1800-2012),IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language, 2018,Feb
- [2] placeholder