OLLSCOIL NA hÉIREANN, CORCAIGH
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Summer Examination 2013

Second Science

CS2502: Logic Design

Professor Ian Gent
Professor Barry O'Sullivan
Dr Frank Böhme

Answer all questions.

90 minutes

1. Recall the two canonical forms for switching functions, i.e. the *canonical sum of products* (CSOP) and the *canonical product of sums* (CPOS). These questions deal with general properties of these two forms and their components.

   a) Consider some switching function f about which only the following is known: Its notation in CPOS form is a product of 50 maxterms. What is the minimum possible number of input variables (function arguments) of f? Justify your answer. (*5 marks*)

   b) Consider some switching function g about which only the following is known: Its notation in CPOS form is longer than its notation in CSOP form (i.e. the CPOS contains more literals). Which general conclusion about g can be made from the assertion above?
   Hint: Consider the truth table of g. (*5 marks*)

   c) Recall that *maxterms* as well as *simplified sums* are both *OR-combinations* of direct or inverted input variables.
   Explain the general difference between these two expressions. (*5 marks*)

2. The questions deal with the *Associative Law*. Recall that the AND as well as the OR operations observe the Associative Law. For instance, in case of OR that law states that
   $(A + B) + C = A + (B + C)$.

   a) Does the XOR (exclusive OR) operation also observe the Associative Law?
   Justify your answer. (*6 marks*)

   b) Does the NAND (NOT AND) operation also observe the Associative Law?
   Justify your answer. (*6 marks*)

   c) Does the NOR (NOT OR) operation also observe the Associative Law?
   Justify your answer. (*6 marks*)

3. Consider a combinational circuit with 4 inputs A, B, C, D and one output Y. Its switching function expressed as the *canonical sum of products* (CSOP) is given by

$$Y = f(A, B, C, D) = m_1 + m_2 + m_3 + m_{10} + m_{11} + m_{12} + m_{14}$$

For clarification, the minterm m_2 is a short notation for the product $\overline{A} \cdot \overline{B} \cdot C \cdot \overline{D}$.

a) Use a Karnaugh-map to to find the *simplified sum of products* (SSOP) of f. (*6 marks*)

b) Rewrite your result from a) into an expression that contains only OR and NOT operations and draw the corresponding circuit diagram. This circuit diagram should only contain NOR gates. (*5 marks*)

c) Rewrite your result from a) into an expression that contains only AND and NOT operations and draw the corresponding circuit diagram. This circuit diagram should only contain NAND gates. (*5 marks*)

d) Use a Karnaugh-map to to find a *simplified product of sums* (SSOP) of f. There are multiple possible answers. (*7 marks*)

4. The following questions deal with the properties of a *sequential circuit* which is given by the following specification:

The circuit is a *Moore machine* with one binary input X and one binary output Y. The output Y depends on the two values of X sampled at the two most recent clock pulses. Y should always be the result of the NAND combination of these two input values.

For example, lets assume we have $X = 1$ when a clock pulse occurs. Lets assume that X has not changed when the next clock pulse occurs. Since the last two sampled values of X are 1 the output now assumes $Y = \overline{1 \cdot 1} = 0$. Now consider the next clock pulse and lets assume that X has meanwhile changed to $X = 0$. This means the last two sampled input values are 1 and 0 and therefore the output now changes to $Y = \overline{0 \cdot 1} = 1$.

a) Draw the state diagram for this circuit. Make sure that all arcs and all states are correctly labelled.
Hint: Your diagram should contain 4 states. However, a *Mealy machine* with similar behaviour could be realized with two states only. (*6 marks*)

b) Develop the *transition table* of this sequential circuit. Make sure the rows and columns carry the correct labels. (*6 marks*)

c) Is it possible to find an input sequence for X that causes the output Y to alternate with every clock pulse, i.e. $Y = 0, 1, 0, 1, 0, 1, 0, 1 \ldots$? If your answer is yes, then give such an input sequence. (*6 marks*)

d) Is it possible to find an input sequence for X that causes the output Y to alternate with *every second* clock pulse, i.e. $Y = 0, 0, 1, 1, 0, 0, 1, 1 \ldots$? If your answer is yes, then give such an input sequence. (*6 marks*)