PN544/C1

Near field communication (NFC) controller

Rev. 3.0 — 16 November 2009 Product data sheet

155230 CONFIDENTIAL

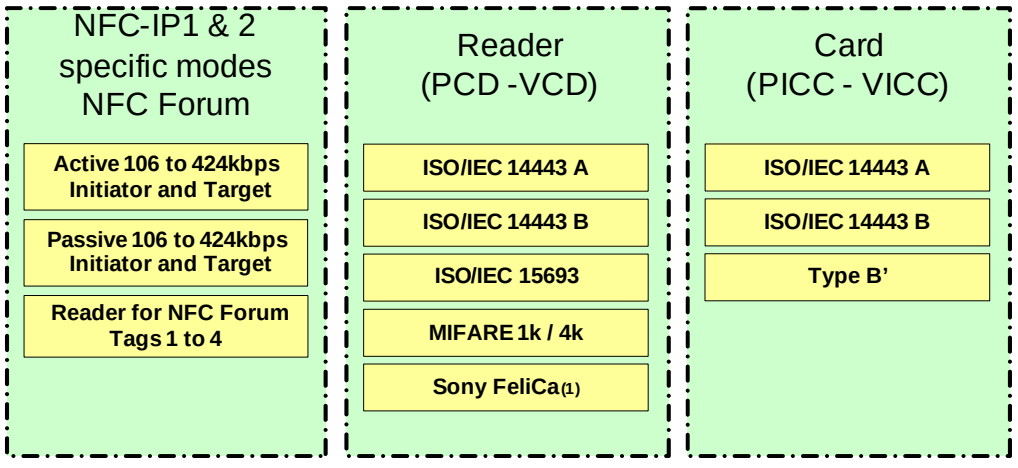
1. Introduction

This Product data sheet describes PN544, NXP's second generation NFC controller. This data sheet requires additional documents for functional chip description and design in. Please refer to the references listed in this document for full list of documentation provided by NXP.

2. General description

PN544 is full featured NFC controller designed for integration in mobile phones. It is optimized for low power consumption with fully host controllable power states and for low footprint for mobile phone applications.

PN544 builds a contactless frontend for phone platforms towards contactless applications available on existing infrastructure. Integrated CPU is decoupling the host controller from the timing constraints of RF communication and allowing autonomous operation. With support for both UICC based and separate, phone integrated, Secure Element it enables the flexibility for application design for different markets.



(1) According to ISO/IEC 18092 (ECMA 340) standard

Fig 1. PN544 transmission modes

Supported transmission modes are listed in Figure 1 "PN544 transmission modes" on page 1. For NFCIP-1 and PCD communication modes, host control is required, whereas for the contactless card functionality PN544 can act autonomously if previously configured by host in such a manner. PICC functionality in passive communication mode can be supported without phone being turned on or even with phone battery removed.

3. Features

- HT80C51MX low power microcontroller core
  - Code memory: 128 kB ROM, 44 kB EEPROM
  - Data memory: 5kB SRAM, 8 kB EEPROM
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated configurable Polling Loop for automatic device discovery
- RF protocols supported
  - ISO/IEC 14443A, ISO/IEC 14443B PCD 106kbit/s to 848kbit/s
  - ISO/IEC 14443A, ISO/IEC 14443B PICC 106kbit/s to 424kbit/s
  - MIFARE reader encryption mechanism (MIFARE 1K/4K)
  - Reading NFC Forum tags (MIFARE Ultralight, Jewel, FeliCa open tag, ISO/IEC 14443-4)
  - Reading Desfire card
  - ISO/IEC 15693 / ICODE VCD mode
  - NFC-IP1 & NFC-IP2 protocols (ISO/IEC 18092 / ECMA 340 and ISO/IEC 21481 / ECMA 352) 106kbit/s to 424kbit/s
  - B' card emulation
- Supported host interfaces
  - High Speed UART (HSU)
  - SPI
  - I^2C
  - Automatic wake up from STANDBY via host control interface
- Supported Secure Element interfaces
  - SWP/HCI (Single Wire Protocol) according ETSI/SCP standardization
  - ISO/IEC 28361 (ECMA 373) NFC-WI interface to connect an external Secure Element restricted to 106kbit/s. Signal In activation is not implemented.
- Flexible clock supply concept to facilitate PN544 integration
  - Integrated FracNPLL unit to make use of cellular reference clock
  - Internal oscillator for 27.12 MHz crystal connection
- Integrated power management unit
  - Direct connection to a mobile battery (2.3 V to 5.5 V voltage supply range)
  - Power switch for secure companion chips connected over SWP or NFC-WI
  - Support different power-down/standby mode by firmware
  - Powered-by-Field and Powered by the battery modes when mobile is off supported[1]
  - LDO generates transmitter supply, programmable to 2.7V, 3V and 3.3V, which includes a current limiter to 150mA typical (see $I_{TVDDlim}$ parameter)
- Dedicated IO ports for external device control
- Interrupt IRQ pin to ease host interface communication

1. This functionality is strongly dependent on implementation and mechanical constraints (e.g. antenna size)

- Integrated non-volatile memory to store data and executable code
- Integrated antenna detector for production tests

4. Applications

- Mobile phones
- Portable equipment (Personal Digital Assistants, notebooks)
- Consumer devices

5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	VBAT Battery Supply Voltage	Battery monitor enabled		2.85	-	5.5	V
V_{BAT}	VBAT Battery Supply Voltage	No RF field generation Battery monitor disabled		2.3	-	5.5	V
V_{BAT}	VBAT Battery Supply Voltage	RF field generation Battery monitor disabled		2.7	-	5.5	V
PV_{DD}	Pad power supply (supply voltage for host interface)			1.65	1.8	1.95	V
SV_{DD}	SVDD Supply voltage for Secure Element interface			1.65	1.8	1.95	V
TV_{DD}	TVDD Transmitter supply voltage	Configured to 2.7V, Offset enabled V_{BAT}>3.2V typical		2.5	2.7	2.9	V
TV_{DD}	TVDD Transmitter supply voltage	Configured to 3V, Offset enabled V_{BAT}>3.5V typical		2.8	3.0	3.2	V
TV_{DD}	TVDD Transmitter supply voltage	Configured to 3.3V, Offset enabled V_{BAT}>3.9V typical		3.1	3.3	3.5	V
$TV_{DDOFFSET}$	TVDD Transmitter supply offset voltage	Offset enabled	[8]		300		mV
AV_{DD}, DV_{DD}	AVDD Internal Analog, DVDD digital supply voltages			1.65	1.8	1.95	V
$SIMV_{CC}$	UICC supply output voltage	PMUVCC to ground I_{SIMVCC}= 5 mA		1.62	1.8	1.98	V
I_{HPD}	Hard Power Down current consumption	V_{BAT}=3V, V_{EN}=0V			3	6	µA
I_{MON}	Monitor Mode current consumption	V_{BAT} <$V_{BATcritical}$			7	10	µA
I_{STBY}	Standby Mode current consumption	V_{BAT}=3V V_{VEN_MON} is grounded SWIO is pulled-down	[1] [2] [3] [4]		44	55	µA
I_{STBY}	Standby Mode current consumption	V_{BAT}=5.5 V V_{VEN_MON} is grounded SWIO is pulled-down	[1] [2] [3] [4]		60	70	µA

Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{VBAT}	Continuous total current consumption	PCD mode at typical T_{VDD}=3 V, including secure elements supplies	[5]			150	mA
I_{SVDD}	Maximum current sourced to Secure Element on SVDD supply	VBAT>2.3V		20			mA
I_{SVDD}	Maximum current sourced to Secure Element on SVDD supply	Powered-by-Field, field strength allows VDHF>2.5V		5			mA
I_{PVDD}	Total current which can be pulled on PVDD referenced outputs					15	mA
$I_{TVDDlim}$	Transmitter LDO current limiter	V_{BAT} >TV_{DD}+300mV		130		210	mA
$I_{TVDDlim}$	Transmitter LDO current limiter	V_{BAT} <TV_{DD}+300mV		130		240	mA
I_{PMUVCC}	PMUVCC supply current	Class B, no SWP activity			35	45	µA
I_{PMUVCC}	PMUVCC supply current	Class C, no SWP activity			15	20	µA
P_{max}	Maximum power dissipation	Reader mode V_{BAT}=5.5V TX1 and TX2 to ground	[6]			1.5	W
P_{max}	Maximum power dissipation	Reader mode I_{TVDD} = 100mA V_{BAT}=5.5V	[7]			0.5	W
T_{amb}	Operating ambient temperature	JEDEC PCB-0.5		-30		+85	°C

[1] The values are given for junction temperature of less than 90°C as when in STANDBY in 85°C ambient the junction will stay below that value.

[2] If V_{VEN_MON} >1.1V, then the current is increased by 6µA maximum

[3] If SWIO is configured in High Impedance, then the current is increased by 5µA maximum.

[4] Standby current is current driven by V_{BAT} pin. When PMU_VCC is present, its current consumption shall be added to have PN544 overall current consumption in standby mode.

[5] This is considering an antenna tuning done as proposed by NXP in reference Ref. 9 “PN544 Antenna Design Guide”, so that current in TV_{DD} does not exceed 100mA even when antenna is loaded by target/card/tag.

[6] This value is given considering TX1 and TX2 shorted to ground. The current is then limited by the TXLDO limiter. It is the sum of the power within the TXLDO, power in the Secure element on SVDD and power in PN544 other circuitries on AVDD and DVDD. This power will be transient as the firmware will cut the TXLDO.

$$PWR = 0.21 \times 5.5 + 0.02 \times (5.5 - 1.65) + 5.5 \times 0.01$$

[7] This value is given considering a TVDD max current of 100mA according NXP recommendation. It is the sum of the power within the TXLDO, power within the transmitter impedances, power in the Secure element on SVDD and power in PN544 other circuitries on AVDD and DVDD.

$$PWR = 0.1 \times (5.5 - 2.7) + 0.1^2 \times (4 + 5) + 0.02 \times (5.5 - 1.65) + 5.5 \times 0.01$$

[8] To know how the offset is working, refer to Section 10.6.4 “TXLDO” on page 40.

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5441A2ET/C1xxyy [1][2]	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls; body 4.5 × 4.5 × 0.8 mm	SOT962-1

[1] Refer to chapter “Licenses”

[2] xx refers to the ROM code version

yy refers to the EEPROM code version.

The ROM and EEPROM codes functionalities are described in the User-Manual document (document number 1450zz where zz is the version).

7. Marking

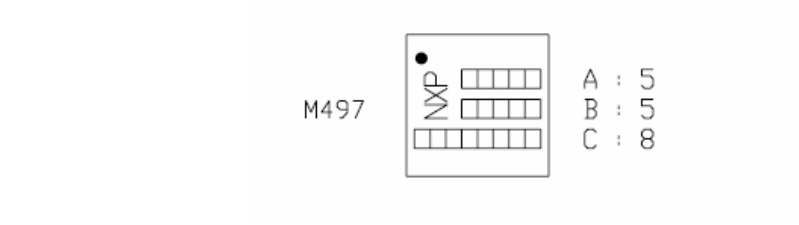


Fig 2. PN544 package marking

Table 3. Marking codes

Type number	Marking code
A	Product version identification: • 2 first digits: 44 from PN544 • 3rd digit: ROM code version • 4th and 5th digits: EEPROM code version
B	Diffusion batch sequence number
C	Manufacturing code including: • Diffusion center code: Z for SSMC • Assembly center code: S for APK • ROHS compliancy indicator: D for fully compliant RoHS, and no halogen and antimony • Manufacturing year and week: 3 digits YWW • Mask layout version • Product life cycle status code: x means not qualified product y means pre-Released product nothing means Released product

8. Block diagram

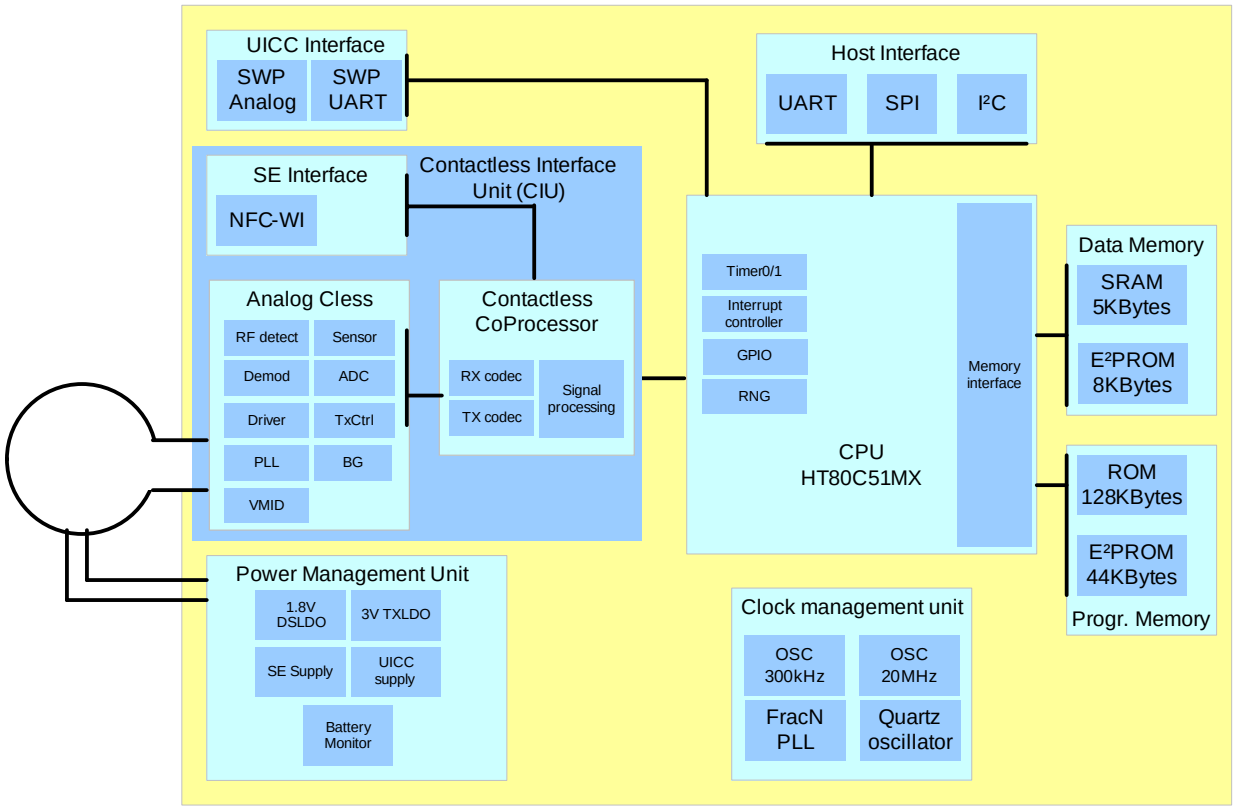


Fig 3. PN544 block diagram

9. Pinning information

9.1 Pinning

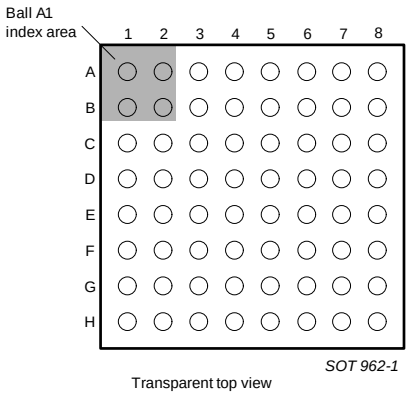


Fig 4. Pinning of PN544 in TFBGA64 (SOT962-1)

Table 4. PN544 Pin description

Symbol	Pin	Type	Refer	Description
GPIO7	A1	IO	PV_{DD}	General purpose IO / Debug interface
IFSEL0	A2	I	PV_{DD}	Host interface select input 0
IRQ	A3	O	PV_{DD}	IRQ output
PVDD	A4	Power	n/a	Pad supply voltage input (VI/O)
DVDD	A5	Power	n/a	Digital supply voltage output for decoupling
TEST1	A6	I	PV_{DD}	NXP production test - Shall be connected to PVDD
RFU1	A7	n/a	n/a	Reserved for future use
PMUVCC	A8	Power	n/a	UICC Power in from external PMU
GPIO4	B1	IO	PV_{DD}	General purpose IO / Download mode control / Debug interface
GPIO5	B2	IO	PV_{DD}	General purpose IO / Debug interface This pin must be kept low until PN544 has ended its boot, otherwise PN544 enters a test mode.
GPIO6	B3	IO	PV_{DD}	General purpose IO / Debug interface
IF1	B4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
PVSS	B5	Ground	n/a	Pad VSS
TEST2	B6	I	PV_{DD}	NXP production test - Shall be connected to PV_{DD}
VEN	B7	I	V_{BAT}	Enable/disable LDO regulator / Reset
SIMVCC	B8	Power	n/a	Power output to supply the UICC
VDHF	C1	Power	n/a	Powered-by-Field rectifier output voltage
GPIO3	C2	IO	PV_{DD}	PWR_REQ: power request / General purpose IO / Debug interface
GPIO2	C3	IO	PV_{DD}	CLK_REQ: clock request / General purpose IO / Debug interface

Table 4. PN544 Pin description *…continued*

Symbol	Pin	Type	Refer	Description
IF2	C4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
TEST3	C5	I	PV_{DD}	NXP production test - Shall be connected to PV_{DD}
TEST10	C6	I	PV_{DD}	NXP production test - Shall not be connected or connected to PV_{DD}
SWIO	C7	IO	DV_{DD} or $SIMV_{CC}$	SWP data connection
SVDD	C8	Power	n/a	SE power
VCO_VDD	D1	Power	n/a	FracNPLL supply voltage output for decoupling
DVSS	D2	Ground	n/a	Digital VSS
GPIO1	D3	IO	PV_{DD}	CLK_ACK: clock acknowledge / General purpose IO /Debug interface
IF3	D4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
TEST4	D5	I	PV_{DD}	NXP production test - Shall be connected to PV_{DD}
EXT_SW_CTRL	D6	O	$SIMV_{CC}$	Control output signal for external UICC power switch
SIGOUT	D7	O	SV_{DD}	NFC-WI data output
VBAT	D8	Power	n/a	Battery voltage
XTAL1	E1	I	AV_{DD}	Oscillator or FracNPLL input
AVSS1	E2	Ground	n/a	Analog VSS
GPIO0	E3	IO	PV_{DD}	General purpose IO / Debug interface
IF0	E4	IO	PV_{DD}	Host interface pin - functionality depends on selected interface
TEST5	E5	O	PV_{DD}	NXP production test - Shall not be connected
RFU2	E6	n/a	n/a	Reserved for future use
SIGIN	E7	I	SV_{DD}	NFC-WI data input
VEN_MON	E8	I	V_{BAT}	Enable of the battery voltage monitor
XTAL2	F1	O	AV_{DD}	Oscillator output
AVDD_out	F2	Power		Analog supply voltage output for decoupling
TEST7	F3	O	AV_{DD}	NXP production test - Shall not be connected
IFSEL1	F4	I	PV_{DD}	Host interface select input 1
IFSEL2	F5	I	PV_{DD}	Host interface select input 2
VSS	F6	Ground	n/a	VSS
TVDD_OUT	F7	Power	n/a	Contactless transmitter supply voltage output for decoupling
VBAT2	F8	Power	n/a	Power pin reserved for future use. Shall be connected to V_{BAT} pin
AVDD_in	G1	Power	n/a	Analog supply voltage input after decoupling
TEST8	G2	O	AV_{DD}	NXP production test - Shall not be connected
TEST9	G3	O	AV_{DD}	NXP production test - Shall not be connected
VMID	G4	Power	AV_{DD}	Contactless receiver Voltage reference
ANT1	G5	Power	n/a	Antenna connection for card emulation
ANT2	G6	Power	n/a	Antenna connection for card emulation

Table 4. PN544 Pin description *…continued*

Symbol	Pin	Type	Refer	Description
PMU_GND	G7	Ground	n/a	PMU VSS
TVDD	G8	Power	n/a	Contactless transmitter supply voltage input after decoupling
RFU3	H1	n/a	n/a	Reserved for future use
TEST6	H2	O	AV_{DD}	NXP production test - Shall not be connected
AVSS2	H3	Ground	n/a	Analog VSS
RX	H4	I	AV_{DD}	Contactless Receiver input
TVSS1	H5	Ground	n/a	Contactless Transmitter ground1
TX1	H6	O	TV_{DD}	Contactless Transmitter output1
TX2	H7	O	TV_{DD}	Contactless Transmitter output2
TVSS2	H8	Ground	n/a	Contactless Transmitter ground2

9.2 Pin description

In addition to the general pinning list, the pins of PN544 can be divided in groups according to the device they are connected to. Here provided list uses the same structure as functional groups used in Figure 41 “Application schematic 1” on page 62 and Figure 42 “Application schematic 2” on page 63.

Table 5. Host connection pins

Symbol	Pin	Description
VEN	B7	Enable/disable LDO regulator
PVDD	A4	Pad supply voltage Input (VI/O)
PMUVCC	A8	UICC power in from mobile PMU
IRQ	A3	IRQ output
XTAL1	E1	Oscillator input
IF0	E4	Host interface pin - functionality depends on selected interface
IF1	B4	Host interface pin - functionality depends on selected interface
IF2	C4	Host interface pin - functionality depends on selected interface
IF3	D4	Host interface pin - functionality depends on selected interface

Table 6. UICC connection pins

Symbol	Pin	Description
SIMVCC	B8	Power output to supply the UICC
SWIO	C7	SWP data connection
EXT_SW_CTRL	D6	Control output signal for external UICC power switch

Table 7. SE connection pins via NFC-WI

Symbol	Pin	Description
SVDD	C8	SE power; fixed to SV_{DD}=1.8V
SIGOUT	D7	NFC-WI data output
SIGIN	E7	NFC-WI data input

Table 8. Antenna connection pins

Symbol	Pin	Description
TX1	H6	Contactless Transmitter output1
TX2	H7	Contactless Transmitter output2
RX	H4	Contactless Receiver input
VMID	G4	Contactless Receiver Voltage reference
ANT1	G5	Antenna connection for card emulation
ANT2	G6	Antenna connection for card emulation

Table 9. GPIO pins

Symbol	Pin	Description
GPIO0	E3	General purpose IO
GPIO1	D3	General purpose IO / Clock acknowledge
GPIO2	C3	General purpose IO / Clock - power request
GPIO3	C2	General purpose IO / Power request
GPIO4	B1	General purpose IO / Download mode control
GPIO5	B2	General purpose IO
GPIO6	B3	General purpose IO
GPIO7	A1	General purpose IO

Table 10. Configuration pins

Symbol	Pin	Description
IFSEL0	A2	Host interface select input
IFSEL1	F4	Host interface select input
IFSEL2	F5	Host interface select input

10. Functional description

PN544 is an NFC transceiver IC designed for mobile phone integration.

PN544 can be connected on one side on a host controller through a selectable physical interfaces (I²C, SPI, UART) and on a second side to a UICC through a SWP interface. The 2 physical interface are controlled by a logical interface based on ETSI HCI.

PN544 is compliant with ETSI/SCP SWP and HCI, see Ref. 1 “ETSI SWP” and Ref. 2 “ETSI HCI”.

The logical interface towards the host baseband is ETSI/SCP HCI compliant with additional command set for NXP specific product features. This IC is fully user controllable by the firmware interface described in Ref. 7 “PN544 User Manual”.

Additionally, it provides NFC-WI interface towards second Secure Element connected via this interface. Thus, PN544 can provide full Secure Element functionality also without UICC present in the system.

Moreover, PN544 provides flexible and integrated power management unit in order to preserve energy supporting Powered-by-Field and powered-down mode. It also allows various power schemes for the UICC.

10.1 Functional / Power states of PN544

Two cases have to be considered for PN544's functional states:

Battery monitor is used: VEN_MON is high. These states are depicted in Figure 5 "Functional diagram when battery monitor is used" on page 12

Battery monitor is not used: VEN_MON is low. These states are depicted in Figure 6 "Functional diagram when no battery monitor" on page 13

In both cases, the functional / power states depend on two factors:

- Energy available from the system
- Configuration by host system, both in HW and SW

The power states of the following diagrams are described starting Section 10.1.1 "Standby mode" on page 14.

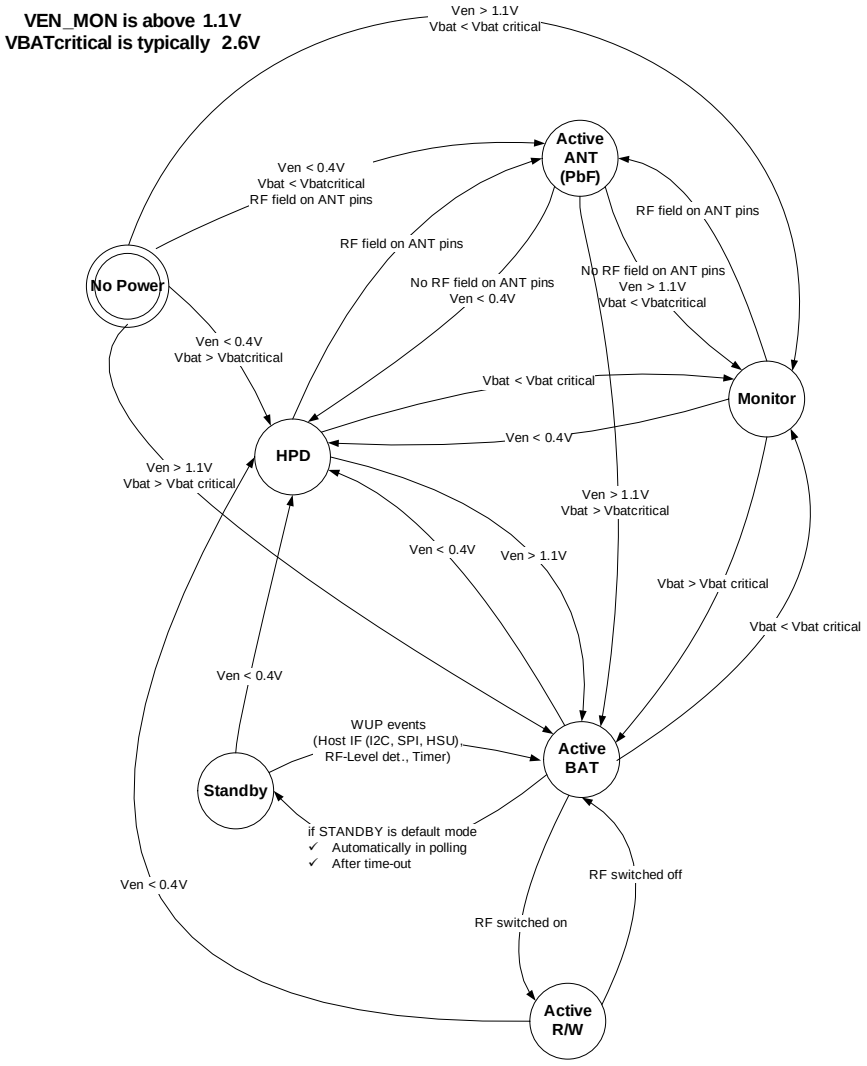


Fig 5. Functional diagram when battery monitor is used

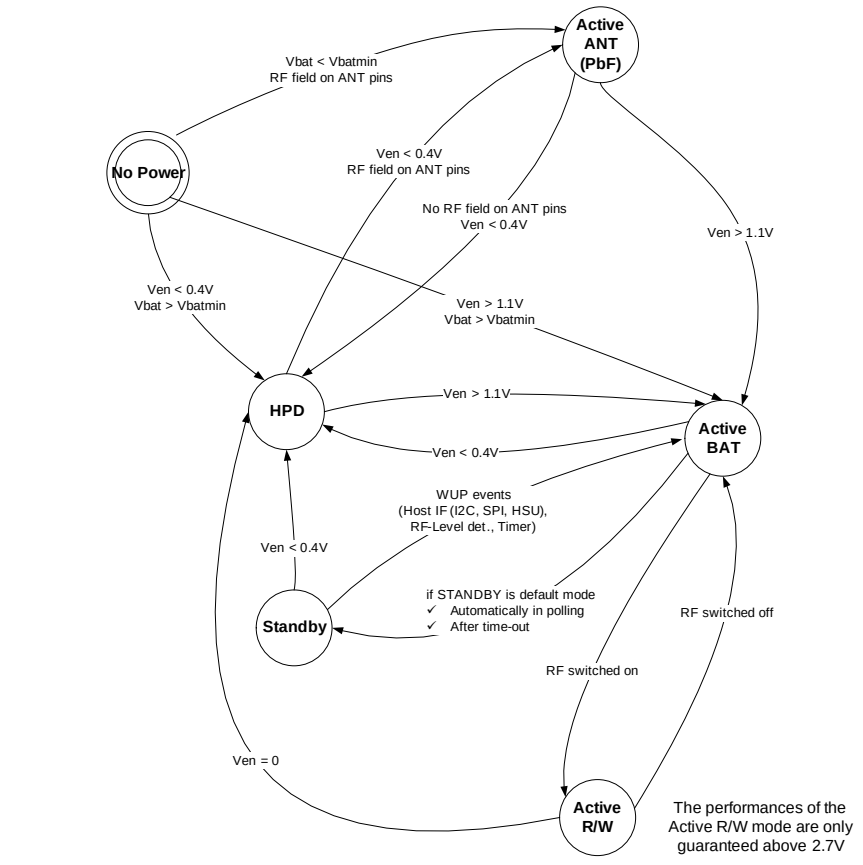


Fig 6. Functional diagram when no battery monitor

On application level, PN544 will continuously switch between different states to optimize the current consumption. Please refer to Table 1 “Quick reference data” on page 3 for targeted current consumption in here described states.

PN544 is designed to allow the host controller to have full control over its functional states, thus of the power consumption of PN544 based NFC solution and possibility to restrict parts of PN544 functionality.

10.1.1 Standby mode

ActiveBAT is PN544's default state after boot sequence in order to allow a quick configuration of PN544. It is recommended to change the default state to STANDBY after first boot in order to save power (see Ref. 7 "PN544 User Manual").

PN544 can switch to Standby mode autonomously (if configured by host). This state is independent of the PVDD value (meaning whatever the state of the mobile phone baseband; on or off).

In this mode PN544 is not functional as RF frontend and most blocks including CPU are physically detached from power supply. Number of wake-up sources[2] exist to put PN544 into active battery mode:

- Host interface wake-up event (I^2C, SPI, HSU)
- Antenna RF level detector
- Internal timer event when using polling loop

If wake-up event occurs, PN544 will switch to active battery mode. Any further operation depends on software configuration and/or wake-up source.

Standby mode is available for $V_{BAT} > V_{BATcritical}$ and V_{EN}>1.1V.

Table 11. Default host pin state in standby mode [1][2]

Pin name	PV_{DD}>1.65 V [3][4]		
	I^2C host interface	HSU host interface	SPI host interface
GPIO0	Pull-up		
GPIO1	Pull-up (CLK acknowledge)		
GPIO2	CLK request [5]		
GPIO3	High Impedance (PWR request)		
GPIO4	High Impedance (Enter download mode)		
GPIO5	High Impedance		
GPIO6	High Impedance		
GPIO7	High Impedance		
IF0	Input	Input	Input
IF1	Input	Input	Input
IF2	Open-Drain	Input	Input
IF3	Open-Drain	Output	Output
IRQ	Output		

[1] See Section 10.3.4 "IOs configuration" on page 27 for description of the different states.

[2] This table describes the default state. GPIOs states can be changed by HCI commands, see Ref. 7 "PN544 User Manual".

[3] To avoid extra current consumption, the voltage pin shall always stay within its specification: 0V to PV_{DD}.

[4] When PV_{DD} is not within its operational range, the pin functionality cannot be guaranteed. To avoid any overconsumption PVDD shall then be forced to 0V or left in high impedance.

[5] GPIO2 is per default configured for clock request mechanism. When clock is requested GPIO2 is configured in Push-pull with high level. When no clock is requested GPIO2 is in High Impedance state.

2. All host related wake-up events imply that PV_{DD} is available

10.1.2 Active R/W mode

In this mode, PN544 is acting as reader/writer, searching for or communicating with passive tags or NFC target. Once RF communication has ended, PN544 will switch to active battery mode (i.e. switch RF transmitter off) to save energy.

Active R/W mode shall be used with $2.7V<V_{BAT}<5.5V$, $1.65V<PV_{DD}<1.95V$ and $V_{EN}>1.1V$. Active R/W shall not be used with $V_{BAT}<2.7V$.

Table 12. Default host pin state in Active R/W mode [1][2]

Pin name	$2.7V<V_{BAT}<5.5V$ $1.65V<PV_{DD}<1.95V$ [3] $V_{EN}>1.1V$.		
	I^2C host interface	HSU host interface	SPI host interface
GPIO0	Pull-up		
GPIO1	Pull-up (CLK acknowledge)		
GPIO2	CLK request [4]		
GPIO3	High Impedance (PWR request)		
GPIO4	High Impedance (Enter download mode)		
GPIO5	High Impedance		
GPIO6	High Impedance		
GPIO7	High Impedance		
IF0	Input	Input	Input
IF1	Input	Input	Input
IF2	Open-Drain	Input	Input
IF3	Open-Drain	Output	Output
IRQ	Output		

[1] See Section 10.3.4 “IOs configuration” on page 27 for description of the different states.

[2] This table describes the default state. GPIOs states can be changed by HCI commands, see Ref. 7 “PN544 User Manual”.

[3] To avoid extra current consumption, the voltage pin shall always stays within its specification: 0V to PV_{DD}.

[4] GPIO2 is per default configured for clock request mechanism. When clock is requested GPIO2 is configured in Push-pull with high level. When no clock is requested GPIO2 is in High Impedance.

10.1.3 Active battery mode

In active battery mode PN544 is fully powered, but the RF transmitter stage is turned off.

Active battery mode shall be used with $V_{BATcritical}<V_{BAT}$ <5.5V, 1.65V<PV_{DD}<1.95V and V_{EN}>1.1V. If the V_{BAT} monitor is disabled then the mode is guaranteed for 2.3V<V_{BAT}<5.5V.

Table 13. Default host pin state in Active battery mode [1][2]

Pin name	$V_{BAT\ critical}<V_{BAT}<5.5V$ or $2.3V<V_{BAT}<5.5V$ if V_{BAT} monitor is disable [3] $1.65V<PV_{DD}<1.95V$ [4] $V_{EN}>1.1V$		
	I^2C host interface	HSU host interface	SPI host interface
GPIO0	Pull-up		
GPIO1	Pull-up (CLK acknowledge)		
GPIO2	CLK request [5]		
GPIO3	High Impedance (PWR request)		
GPIO4	Input (Enter download mode)		
GPIO5	High Impedance		
GPIO6	High Impedance		
GPIO7	High Impedance		
IF0	Input	Input	Input
IF1	Input	Input	Input
IF2	Open-Drain	Input	Input
IF3	Open-Drain	Output	Output
IRQ	Output		

[1] See Section 10.3.4 “IOs configuration” on page 27 for description of the different states.

[2] This table describes the default state. GPIOs states can be changed by HCI commands, see Ref. 7 “PN544 User Manual”.

[3] When the V_{BAT} monitor is disable, the pins states cannot be guaranteed when V_{BAT} is below 2.3V

[4] To avoid extra current consumption, the voltage pin shall always stays within its specification: 0V to PV_{DD}.

[5] GPIO2 is per default configured for clock request mechanism. When clock is requested GPIO2 is configured in Push-pull with high level. When no clock is requested GPIO2 is in High Impedance.

10.1.4 Polling loop

The polling loop will sequentially set PN544 in different functional states (Reader/Writer mode, Card emulation mode,...).
In order to optimize the power consumption, each functional mode is implemented using different power modes (Active battery, standby etc....).
Detailed description of polling loop configuration option is given in Ref. 7 “PN544 User Manual”.

10.1.5 Hard power down (HPD) mode

Hard power down mode is entered only by setting V_{EN} to low. As this signal is under host control, PN544 has no influence on entering or exiting this state. By putting V_{EN} < 1.1V, PN544's PMU is physically detached from the battery supply (please refer to Figure 28 "Battery voltage monitor principle" on page 46 for principle schematic).

Table 14. Host pin state in hard power-down mode [1]

Pin name	V_{EN}<1.1V
	All host interfaces [2]
GPIO0	High Impedance
GPIO1	High Impedance
GPIO2	Extra pull-down
GPIO3	High Impedance
GPIO4	Extra pull-down
GPIO5	High Impedance
GPIO6	High Impedance
GPIO7	High Impedance
IF0	High Impedance
IF1	High Impedance
IF2	High Impedance
IF3	High Impedance
IRQ	Extra pull-down

[1] See Section 10.3.4 "IOs configuration" on page 27 for description of the different states.

[2] The pin voltage shall still be within 0V to PV_{DD} voltage to avoid any extra current consumption

10.1.6 Monitor mode

By V_{EN} > 1.1V and battery supply reaching the monitor threshold (see also Section 10.6.7 “Battery voltage monitor” on page 46) PN544 will autonomously detach internal PMU from battery supply to protect the battery from deep discharge. In monitor mode, PN544 will exit it only if it can be powered from the field or the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 40 “Battery voltage monitor characteristics” on page 66.

Table 15. Host pin state in monitor mode [1]

Pin name	$V_{BAT}<V_{BATcritical}$ $V_{EN}>1.1V$ $V_{EN\_MON}>1.1V$
	All host interfaces [2]
GPIO0	High Impedance
GPIO1	High Impedance
GPIO2	Extra pull-down
GPIO3	High Impedance
GPIO4	Extra pull-down
GPIO5	High Impedance
GPIO6	High Impedance
GPIO7	High Impedance
IF0	High Impedance
IF1	High Impedance
IF2	High Impedance
IF3	High Impedance
IRQ	Extra pull-down

[1] See Section 10.3.4 “IOs configuration” on page 27 for description of the different states.

[2] The pin voltage shall still be within 0V to PV_{DD} voltage to avoid any extra current consumption

10.1.7 Active antenna mode (Powered-by-Field)

Active antenna mode describes the state of PN544 in which the battery supply is not available (either because host has detached PN544 via VEN pin or the battery voltage level has reached the critical level) and RF field provides sufficient energy to power-up PN544.

To have a proper functionality this mode requires VEN to be in low state. It means that when VBAT < VBATcritical, VEN > 1.1V and RF field is present, PN544 will go in that power state but the card emulation functionality will not work properly.

PN544 implements a programmable RF guard time set to 16ms per default. It covers the time required to establish, then to stabilize the supplies generated from the field power and finally answer first RF command. Lowering this value might jeopardize the functionality.

In that power mode only the type B', ISO/IEC 14443 A and B PICC at 106kbit/s are available.

The field strength range for which this mode will work will be strongly dependant of the antenna design, UICC power consumption, mobile environment...

Table 16. Host pin state in active antenna mode [1]

Pin name	All host interfaces [2]
	$V_{BAT}<V_{BAT\ critical}$ or $V_{EN}<1.1V$ RF field present
GPIO0	High Impedance
GPIO1	High Impedance
GPIO2	Extra pull-down
GPIO3	High Impedance
GPIO4	Extra pull-down
GPIO5	High Impedance
GPIO6	High Impedance
GPIO7	High Impedance
IF0	High Impedance
IF1	High Impedance
IF2	High Impedance
IF3	High Impedance
IRQ	Extra pull-down

[1] See Section 10.3.4 "IOs configuration" on page 27 for description of the different states.

[2] The pin voltage shall still be within 0V to PV_{DD} voltage to avoid any extra current consumption

10.2 Microcontroller HT80C51MX

PN544 is controlled via an embedded HT80C51MX microcontroller core.

PN544 microcontroller core is an improved version of the low-power 80C51.
This microcontroller is an asynchronous core offering following advantages:

- Extremely low power: Zero stand-by power while in sleep mode, both for CPU core and CPU peripherals, but immediately available for full-speed fully-functional operation
- Very low electromagnetic emission (EMI)

Its main features are:

- Clock-less, low-power design
- MMU/MPU interface to interface with Data and Code memory
- Power control module to manage the CPU power consumption
- Interface to configure I/O pads
- Interrupt controller
- Timer 0/1

10.2.1 PN544 memory management

The memory organization of PN544 is based on the standard 80C51MX memory model that offers a unified address space for code and data memory.
The integrated Memory Management Unit (MMU) offers improved addressing capabilities in order to address up to 16 MB of physical code/data memory. All types of memories, except the Special Functions Registers (SFRs, which are quick access registers) of the HT80C51MX, are accessed via the Memory Management Unit (MMU).

The standard 80C51 memory areas (CODE, DATA, IDATA, etc.) are mapped into 16 MB memory space, therefore PN544 can operate with the following memory model:

- ROM (128 kB) are used for storing code for execution and fixed data
- RAM (5 kB)
- EEPROM
  - 8 kB EEPROM module are used for data storage (HCI registries, configuration ...)
  - 44 kB EEPROM are used for code execution only

10.2.2 Timer0/1 description

Timer0/1 comprises two 16-bit timer/counters: Timer0 and Timer1. Both can be configured as either a timer or an event counter.Timer0/1 are general purpose timer/counters.

Timer0/1 have the following functionality:

- Configurable edge or level detection interrupts
- Timer or counter operation
- 4 timer/counter modes

In the Timer function, the register's timer is incremented every timer clock cycle.
In the Counter function, the register is incremented in response to a 1 to 0 transition at its corresponding external input pin.
It is configured to work with following clock frequencies 1kHz/13.56 MHz/27.12 MHz.

This feature is used and reserved for embedded PN544 firmware and can not be used for external application purposes.

10.2.3 Interrupts management

The interrupts are grouped in 3 priority levels shown in Table 17. The interrupts of lower level can be interrupted by the higher levels interrupts.

Table 17. Interrupt sources

Interrupt priority	Interrupt sources
3 (highest)	Internal event like: • Thermal sensor • TXLDO overcurrent • Memory address violation • PV_{DD} presence • PMU_VCC presence
2	RF event and SIGIN activity
1	Host interface and SWP link

For example, if an over current occurs during the treatment of an interrupt due to a host interface, PN544 will jump to the treatment of the over current.

The management of the interrupts is done by the embedded PN544 firmware and can not be controlled by host.

10.2.4 FW architecture

PN544 features integrated in firmware are referenced in Ref. 7 "PN544 User Manual"

10.3 Host interfaces

PN544 supports the following host interfaces:

- HSU Slave Interface, up to 460 800 Baud
- SPI Slave Interface, up to 9 MBaud
- I^2C Slave Interface, up to 3.4 MBaud

Only one host interface can be active at same time as pins are shared for all interfaces. The host interfaces are waken-up in the following way:

- HSU: Wake-up after multiple pulses on RX line
- SPI: Transition of NSS Serial
- I^2C: Wake-up on I^2C address

To enable and ensure data flow control between PN544 and host controller additionally a dedicated interrupt line IRQ is provided.

10.3.1 High Speed UART (HSU) Interface

The HSU interface can only be used when running on the quartz oscillator.

The High Speed UART is a buffered, full or half duplex asynchronous serial interface with multi master support. It provides configurable clock rates.
The different data rates are derived from the quartz oscillator frequency (27.12 MHz).

In order to select HSU for host communication, interface selection pins have to be configured as described in Table 18. This information is also provided in the application schematic for quick reference.

Table 18. Pin configuration for HSU interface selection

Pin name	Connection
IFSEL0	Connect to Ground
IFSEL1	Connect to Ground
IFSEL2	Connect to Ground

The HSU interface shares four (4) pins with other host interfaces supported by PN544. When interface selection pins IFSEL0-2 are configured as described in Table 18, functionality of interface pins IF0-3 changes to one described in Table 19.

Table 19. IF0-3 functionality for HSU interface

Pin name	Functionality
IF0	Not used
IF1	RX
IF2	Not used
IF3	TX

Herebelow is the table describing the clock accuracy required from the host for the HSU baud rates

Table 20. HSU interface baud rates

Baud rates	Minimum clock frequency	Maximum clock frequency
9 600	9 312	9 888
28 800	27 936	29 664
115 200	111 744	118 656
230 400	223 488	237 312
460 800	446 976	474 624

10.3.2 I²C interface

The I²C interface implements a Slave I²C bus interface with integrated shift register, shift timing generation and Slave address recognition. I²C Standard mode (100 kHz SCLK), Fast mode (400 kHz SCLK) and High speed mode (3.4 MHz SCLK) are supported.

The mains hardware characteristics of the I²C module are:

- Support Slave I²C bus
- Standard, Fast and High speed modes supported [3]
- Wake-up of PN544 on its address only
- Serial clock synchronization can be used by PN544 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C interface module is optimized for low power, with power consumption of almost zero in sleep mode. It features address decoder for PN544 wake-up functionality.The on-chip I²C logic provides a serial interface that meets the I²C bus specification (refer to Ref. 5 “I²C Specification”), with some timings restriction (see [3]) and below specificities.

When the host send PN544 address for a read, and PN544 has no data to send back, PN544 sends back its address shifted by 1 bit + 01h. For example, if PN544 address is 2Bh, PN544 will send back 57h.

PN544 does not handle START and STOP conditions which appears within an on-going frame exchange.

When PN544 is in STANDBY mode, the host can wake it up by sending its address. PN544 will not acknowledge this address but will be woken-up. The host shall then send a new command for PN544 address before PN544 goes back to STANDBY. The waiting time before PN544 goes back to STANDBY is programmable (refer to Ref. 7 “PN544 User Manual” for more information).

PN544 has some timing deviations from standard, see for timings details.

3. High Speed mode has some timing restrictions on t_{LOW} and $T_{HD;SDA}$. Fast Mode has some timing restriction on $T_{SU;SDA}$. 2.7Mbit/s can be reached using SCL duty-cycle of the I²C specification, 3.4Mbit/s is achieved with dedicated SCL duty cycles.

10.3.2.1 I²C configuration options

In order to select I²C interface for host communication, interface selection pins have to be configured as described in Table 21. This information is also provided in the application schematic for quick reference.

Table 21. Pin configuration for I²C interface selection

Pin name	Connection
IFSEL0	Connect to Ground
IFSEL1	Connect to PVDD
IFSEL2	Connect to Ground

The I²C interface shares four (4) pins with other host interfaces supported by PN544. When interface selection pins IFSEL0-2 are configured as described in Table 21, functionality of interface pins IF0-3 changes to one described in Table 22.

Table 22. IF0-3 functionality for I²C interface

Pin name	Functionality
IF0	ADR0: I²C address bit 0 (LSB)
IF1	ADR1: I²C address bit 1
IF2	SDA
IF3	SCL

The 5 MSB values are 28h. The addresses range is then from 28h to 2Bh.

10.3.2.2 I²C functional description

In PN544, the I²C interface is restricted by firmware as a slave only.

The I²C interface may operate in any of the following two modes:

- Slave Receiver
- Slave Transmitter

Two types of data transfers are possible on the I²C bus (see the Ref. 5 “I²C Specification” for more details):

- Data transfer from a Master transmitter to a Slave receiver. The first byte transmitted by the Master is the Slave address. Next follows a number of data bytes. The Slave returns an acknowledge bit after each received byte.
- Data transfer from a Slave transmitter to a Master receiver. The first byte (the Slave address) is transmitted by the Master. The Slave then returns an acknowledge bit. Next follows the data bytes transmitted by the Slave to the Master. The Master returns an acknowledge bit after each received byte except the last byte. At the end of the last received byte, a “not acknowledge” is returned.

In the Slave mode, the I²C interface hardware looks for its own Slave address and the general call address. If one of these addresses is detected, an interrupt is requested.

10.3.3 Serial Peripheral Interface

10.3.3.1 Features

- Synchronous, Serial, Full-Duplex communication, 8 Mbit/s max
- Slave mode
- Programmable clock polarity and phase

10.3.3.2 SPI configuration options

In order to select SPI interface for host communication, interface selection pins have to be configured as described in Table 23.
This information is also provided in the application schematic for quick reference.

Table 23. Pin configuration for SPI interface selection

Pin name	Connection
IFSEL0	CPHA switch: Clock PHAse: defines the sampling edge of MOSI data • CPHA = 1: Data are sampled on MOSI on the odd clock edges of SCK after NSS goes low • CPHA = 0: Data are sampled on MOSI on the even clock edges of SCK after NSS goes low
IFSEL1	CPOL switch: Clock POLarity • IFSEL1 = 0: the clock is idle low, and the first valid edge of SCK will be a rising one. • IFSEL1 = 1: the clock is idle high, and the first valid edge of SCK will be a falling one.
IFSEL2	Connect to PVDD

The SPI interface shares four (4) pins with other host interfaces supported by PN544. When interface selection pins IFSEL0-2 are configured as described in Table 23, functionality of interface pins IF0-3 changes to one described in Table 24.

Table 24. IF0-3 functionality for SPI interface

Pin name	Functionality
IF0	NSS (Not Slave Select)
IF1	MOSI (Master Out Slave In)
IF2	SCK (Serial Clock)
IF3	MISO (Master In Slave Out)

10.3.3.3 SPI functional description

When a master device transmits data to PN544 (slave device) via the MOSI line, PN544 responds by sending data to the master device via the masters MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal.

PN544 starts logic when receiving a logic low at pin NSS and the clock at input pin SCK. Thus, PN544 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loads the 8 bit shift register. After the 8 bit shift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then PN544 waits for a clock train from the master to shift the data out on the slaves MISO line.

- Master In Slave Out (MISO)

  The MISO line is configured as an input in a master device and as an output in a slave device. It is used to transfer data from the slave to the master, with the most significant bit sent first. The MISO line of a slave device should be placed in the high impedance state if the slave is not selected.

- Master Out Slave In (MOSI)

  The MOSI line is configured as an output in a master device and as an input in a slave device. It is used to transfer data from the master to a slave, with the Most significant bit sent first.

- Serial Clock (SCK)

  The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines. The master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since the master device generates SCK, this line becomes an input on a slave device and an output at the master device.

- Not Slave Select (NSS)

  The slave select input line is used to select a slave device. It has to be low prior to data transactions and must stay low of the duration of the transaction. The NSS line on master side must be tied high.

The timing relationships may be chosen by using IFSEL0 (CPHA) and IFSEL1 (CPOL) pins. Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, in order for the slave device to latch the data.

For more information about the SPI functionality see Ref. 6 “SPI”.

10.3.4 IOs configuration

This chapter describes the different configurations for the IO pads:

Table 25. IO pins

Symbol	Pin	Description
GPIO0	E3	General purpose IO
GPIO1	D3	General purpose IO / Clock acknowledge
GPIO2	C3	General purpose IO / Clock -power request
GPIO3	C2	General purpose IO / Power request
GPIO4	B1	General purpose IO / Download mode control
GPIO5	B2	General purpose IO / Digital testbus signal
GPIO6	B3	General purpose IO / Digital testbus signal
GPIO7	A1	General purpose IO / Digital testbus signal
IF0	E4	Host interface pin - functionality depends on selected interface
IF1	B4	Host interface pin - functionality depends on selected interface
IF2	C4	Host interface pin - functionality depends on selected interface
IF3	D4	Host interface pin - functionality depends on selected interface

10.3.4.1 Pad configuration description

Several pad configurations are used within PN544. The configurations used per the delivered embedded code are described in the following chapter.

More configurations can be defined using host interfaces commands, see Ref. 7 “PN544 User Manual”.

For all the following pad structure schematics, the pad structure of GPIO2, GPIO4 and IRQ is somewhat different, there is an extra pull-down resistor directly connected to the pad. See Section “Extra pull-down” on page 30.

Open-Drain

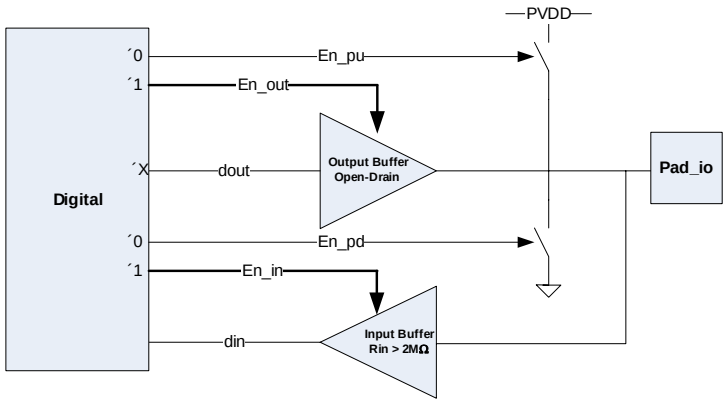


Fig 7. Open-drain

Input

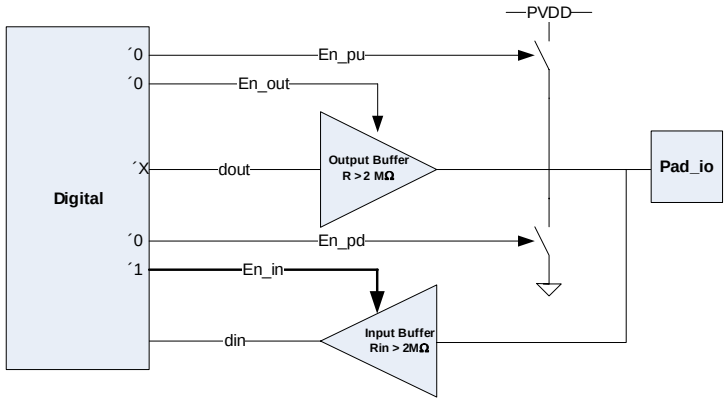


Fig 8. Input

Output

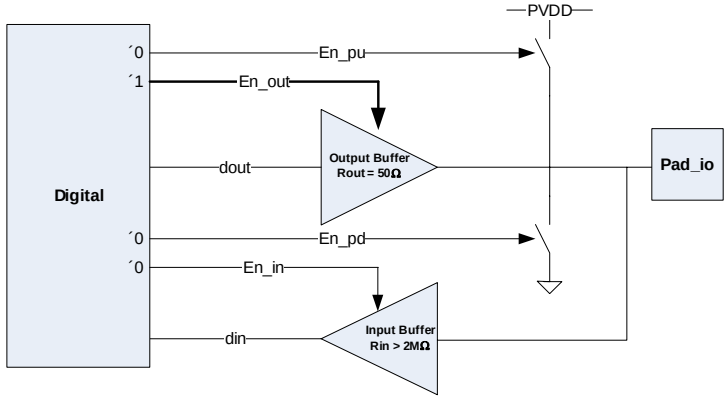


Fig 9. Output

Pull-up

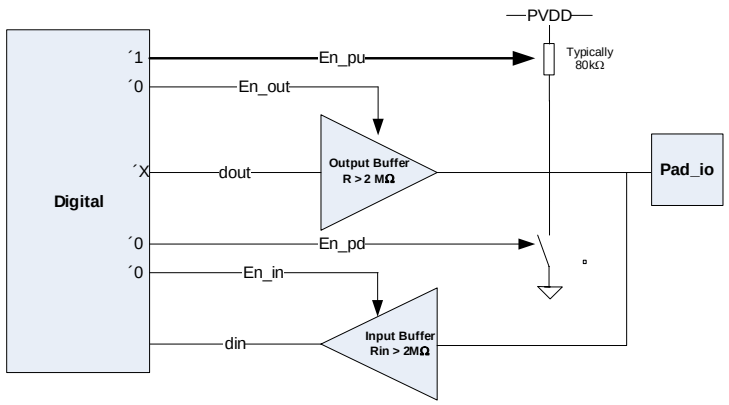


Fig 10. Pull-up

When configured in pull-up, the value of the pull-up resistor is typically 80kΩ.+/–30%. The typical I_{IL} is increased by 25μA.

Pull-down

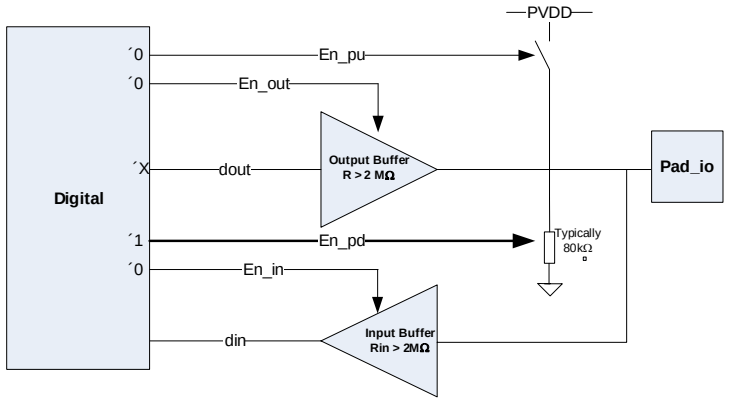


Fig 11. Pull-down

When configured in pull-down, the value of the pull-down resistor is typically 80kΩ+/–30%. The typical I_{IH} is increased by 25μA

Extra pull-down: This configuration is only available for GPIO2, GPIO4 and IRQ.

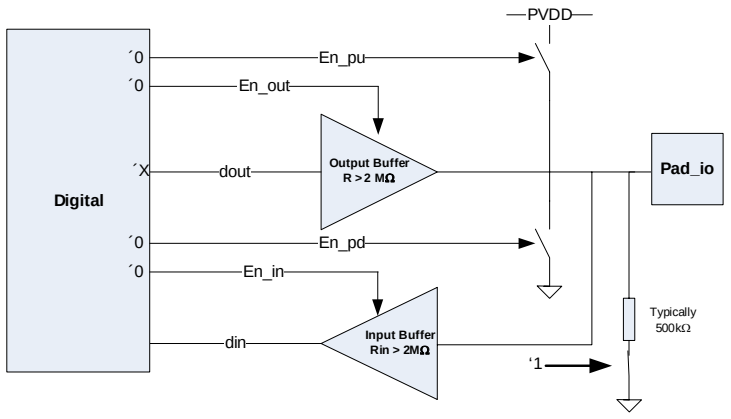


Fig 12. Extra pull-down

When configured in extra pull-down, the value of the pull-down resistor is typically 500kΩ+/–30%.
The typical I_{IH} is increased by 3μA.

This extra pull-down is purely controlled by PN544 HW and is only activated for Monitor, HPD and Powered-by-Field modes.

High Impedance

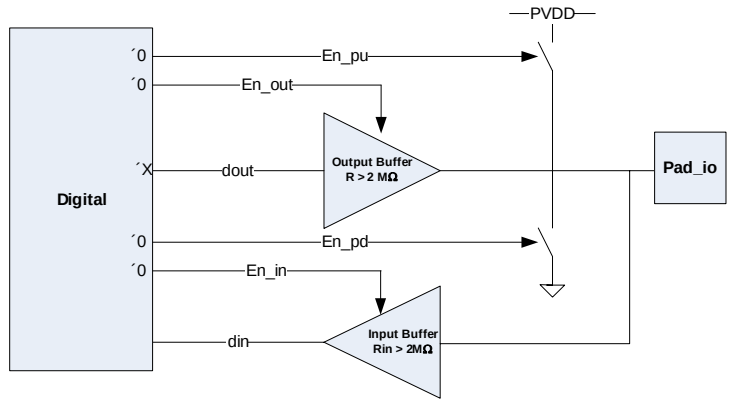


Fig 13. High Impedance (HiZ)

10.4 Secure Element interfaces

PN544 supports 2 interfaces to be connected to Secure Element:

- Single Wire Protocol (SWP)
- NFC-WI

10.4.1 SWP interface

PN544 features ETSI compliant SWP interface towards UICC (see Ref. 1 “ETSI SWP”).

The SWP interface is a bit oriented, point-to-point communication protocol between a UICC and the contactless front end, like PN544. PN544 is the master and the UICC is the slave. This interface is based on the transmission of digital information in full duplex mode. The master sends information on the wire in the voltage domain, while the slave sends information back in the current domain.

PN544 supports the ETSI optional CLT mode for MIFARE (see Ref. 1 “ETSI SWP”).

PN544 offers also the possibility to configure SWIO in High Impedance when VEN>1.1V. This could be done via a host command. See Ref. 7 “PN544 User Manual”

PN544 following state machine is implemented in PN544 design:

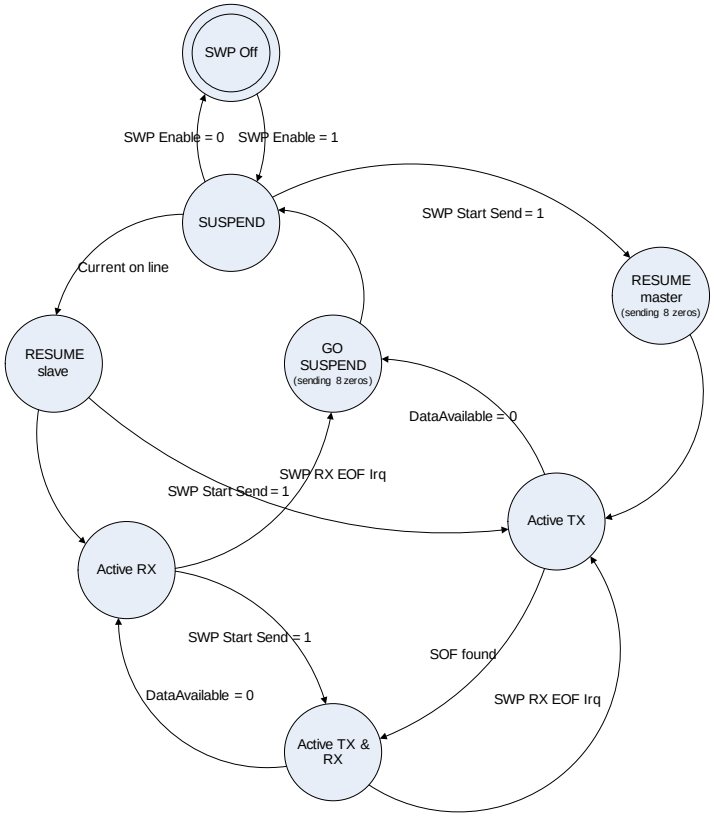


Fig 14. SWP state diagram

10.4.1.1 SWP parameters

PN544 SWP interface implementation features 4 different baud rates:

- 238.1 kbit/s
- 454.5 kbit/s
- 833 kbit/s
- 1.25 Mbit/s (activated by embedded FW if the UICC supports it, otherwise stays at 833 kbit/s)

Except during RESUME sequence, where S2 current detection threshold is 260uA, the detection threshold on S2 current is configurable, four values are supported:

- 240 μA
- 270 μA
- 300 μA (default)
- 330 μA

PN544 also allows configuration of SWIO pin in high Impedance state. The application can choose to have PN544 configuring this high impedance automatically when UICC class B is detected, or on demand via host. For the configuration, refer to Ref. 7 “PN544 User Manual”.

10.4.1.2 SWP test signals

To ease the monitoring of the SWP data transfer during development, PN544 implements test signal S2 (data from UICC to CLF).

This signals represents the data on SWIO.
It can be made available on pin GPIO7 (S2), see Ref. 10 “PN544 RF setting Guide”

10.4.2 NFC-WI interface support

The NFC-WI provides the possibility to directly connect a Secure Element to PN544 in order to act as a contactless smart card IC via PN544 at 106kbit/s. The interfacing signals are routed to the pins SIGIN and SIGOUT. SIGIN can receive a digital ISO/IEC 14443A signal sent by the Secure Element. The SIGOUT pin can provide a digital signal and a clock to communicate to the Secure Element. A Secure Element can be provided by NXP Semiconductors, e.g. the SmartMX P5CN080.

The following figure outlines the supported communication flows via PN544 to the Secure Element core.

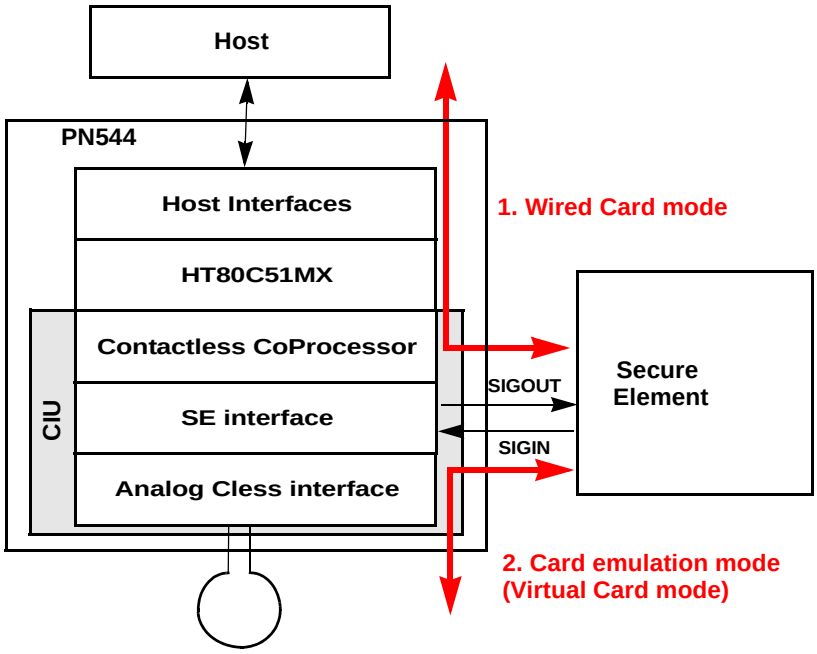


Fig 15. Communication flows supported by the NFC-WI interface

PN544 generates SV_{DD} to supply the Secure Element. The pins SIGIN and SIGOUT are referenced to this supply.

Configured in the Wired Card mode the host controller can directly communicate to the Secure Element via SIGIN/SIGOUT. In this mode PN544 generates the RF clock and performs the communication on the SIGOUT line. To enable the Wired Card mode the clock has to be derived by the internal oscillator or by the FracNPll of the system clock provided by the system.

Configured in Card emulation mode the Secure Element can act as contactless smart card IC via PN544. In this mode the signal on the SIGOUT line is provided by the RF field of the external Reader/Writer. To enable the Virtual Card mode the clock derived by the external RF field has to be used.

The signal shape for ISO/IEC 14443-A and MIFARE NFC-WI support at SIGOUT is a digital signal at a bit rate of 106 kbit/s between PV_{SS} and SV_{DD}. SIGOUT signal carries the AND combination of the Modified Miller bit coded and the 13.56 MHz carrier. It is either derived from the external RF field signal when in Virtual Card Mode or internally generated when in Wired Card mode.

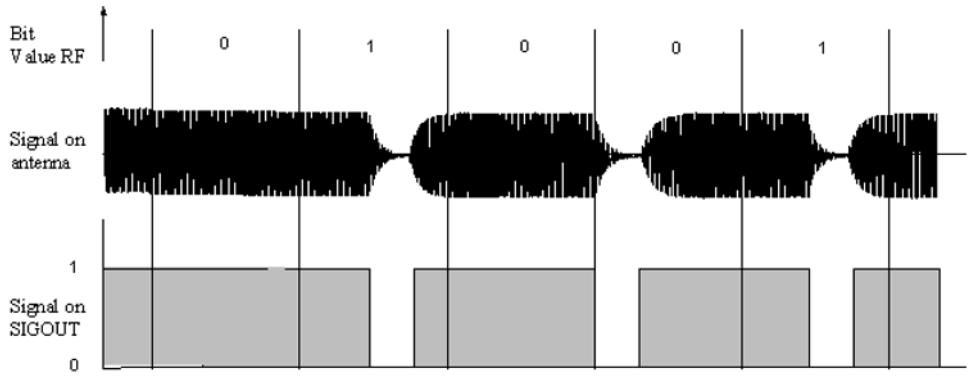


Fig 16. Signal shape for SIGOUT in NFC-WI mode

The signal at SIGIN is a digital Manchester coded signal compliant with ISO/IEC 14443A with a subcarrier frequency of 847.5 kHz generated by the Secure Element.

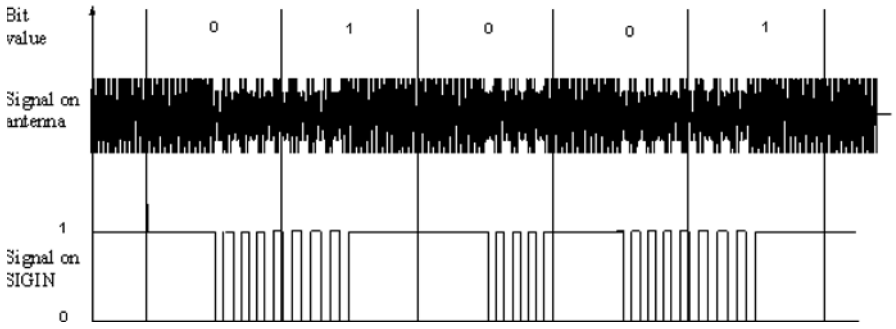


Fig 17. Signal shape for SIGIN in NFC-WI mode

10.5 PN544 clock concept

There are 4 different clock sources in PN544:

- 27.12 MHz clock coming either/or from:
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated FracNPLL unit
- 13.56 RF clock recovered from RF field
- Low power oscillator 20MHz
- Low power oscillator 333kHz

The Figure 18 describes reference clocks used in PN544.

These sources can be used to clock some blocks depending on functional state of PN544 (Active BAT, Standby, Monitor, Powered-by-Field...).

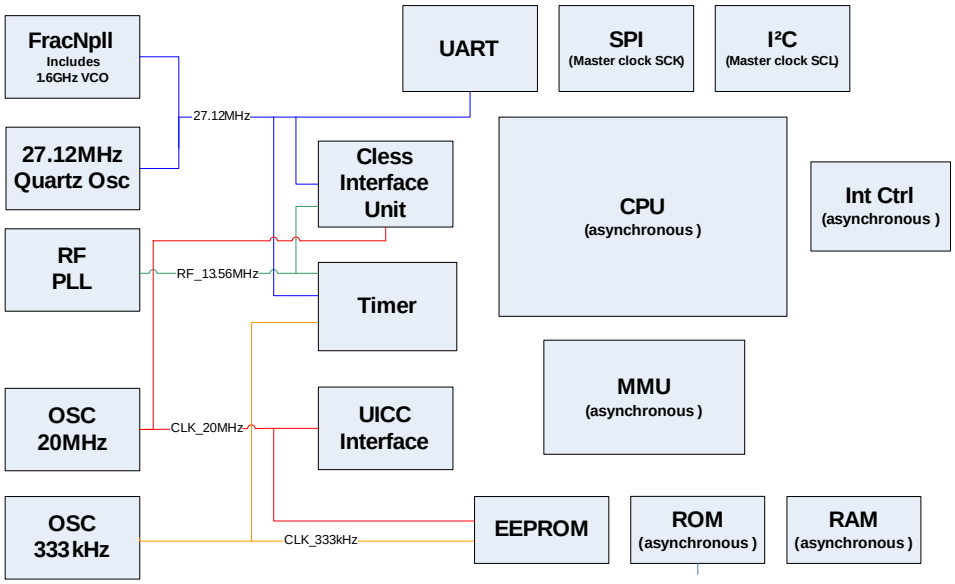


Fig 18. System clock tree

10.5.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN544 is the time reference for the RF front-end when PN544 is behaving in reader mode or ISO/IEC 18092 initiator as well as in target when configured in active communication mode.

Its usage is mandatory when using HSU as host interface.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 19.

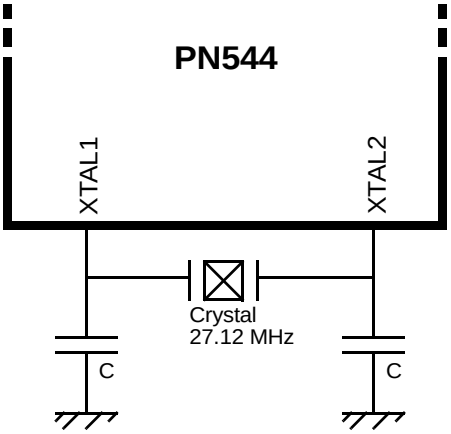


Fig 19. 27.12 MHz crystal oscillator connection

The below table describes the levels of accuracy and stability required on the crystal

Table 26. Crystal requirements

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{XTAL}	XTAL frequency	ISO/IEC and FCC compliancy	[1]	27.107	27.12	27.133	MHz
ESR	Equivalent series resistance				50	100	Ω
C_{LOAD}	Load capacitance				10		pF
P_{XTAL}	Drive level					100	μW

[1] This requirement is to meet the ISO/IEC 14443 and ISO/IEC18092 specifications.

10.5.2 Integrated FracNpll to make use of external clock

When enabled, the FracNpll is designed to generate a low noise 27.12 MHz for an input clock between 10 and 40 MHz.

The FracNPLL cannot be used when using HSU as host interface.

The 27.12 MHz output of the FracNpll is used as the time reference for the RF front-end when PN544 is behaving in reader mode or ISO/IEC 18092 initiator as well as in target when configured in active communication mode.

The input clock on XTAL1 shall comply with the following phase noise requirements across the input frequency which can be from 10Mhz to 40Mhz:

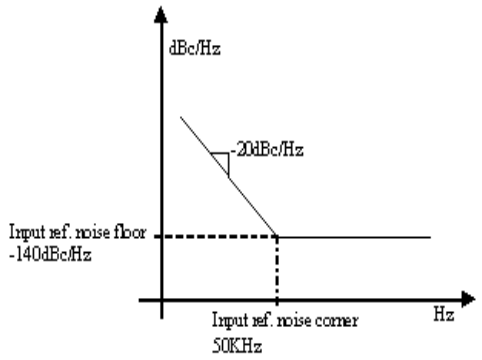


Fig 20. Input reference phase noise characteristics

This phase noise is equivalent to a RMS jitter of 6.23ps from 10Hz to 1MHz.

For configuration of input frequency, please refer to Ref. 7 “PN544 User Manual”. There are 4 pre programmed and validated frequency for the FracNPLL: 13MHz, 19.2MHz, 26MHz and 38.4MHz.

Others frequencies are possible, but NXP has not validated them. In case of a wrong programming of the FracNPLL versus the input clock frequency, the consequence is that the PCD and initiator modes might not be functional.

Please refer to Ref. 7 “PN544 User Manual” and Ref. 8 “PN544 Hardware Design Guide” for detailed description of clock request mechanisms.

10.5.3 Low power 20MHz oscillator

Low power 20MHz oscillator is used for 3 main purposes:
- Clock SWP block
- Clock Contactless interface sub-block to filter RF spam
- Clock EEPROM memory in READ access

10.5.4 Low power 333kHz oscillator

A low frequency oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN544 from standby mode.
This allows implementation of low power reader polling loop at application level.
Moreover, this 333Khz is used as the reference clock for WRITE access to EEPROM memory.

10.6 Power concept

10.6.1 PN544 core supply sources

PN544 can be supplied from two independent voltage sources: external battery (or similar voltage source) and by the RF field. The functionality used for RF power extraction is named “Powered-by-Field” (PbF) in this document. The PbF is an optional feature of PN544 and needs to be enabled via software. If both supply sources are available in the system, PN544 will use both of them concurrently, drawing more current from the stronger one. Simplified working principle is pictured in Figure 21. Both supply sources are connected to PN544’s power management unit (PMU), which decides autonomously which one is used to which extent.

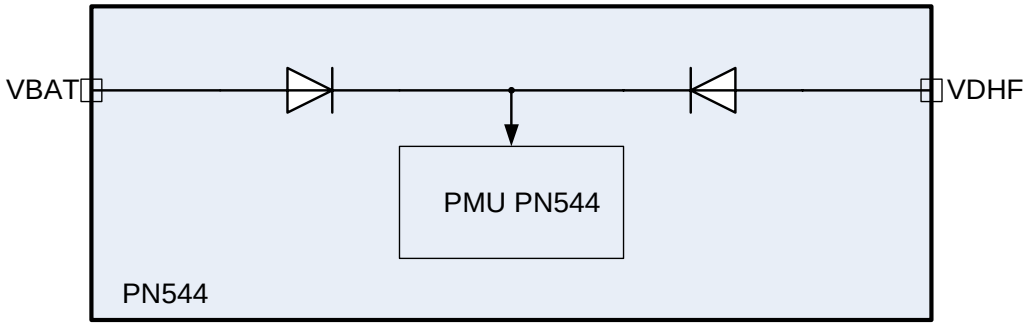


Fig 21. Power sourcing (simplified)

10.6.2 PMU functional description

The Power Management Unit of PN544 generates internal supplies required by PN544 out of V_{bat}, VDHF voltage or V_{PMU_VCC} inputs supplies:

- AV_{DD}: Analog supply
- DV_{DD}: Digital supply
- VCO_V_{DD}: Analog supply to supply FracNpll
- TV_{DD}: Supply for RF transmitter
- SV_{DD}: Supply of the Secure Element connected over NFC_WI
- $SIMV_{CC}$: Supply of the UICC when not directly connected to the mobile PMU

The following functional diagram is describing the main blocks available in PMU:

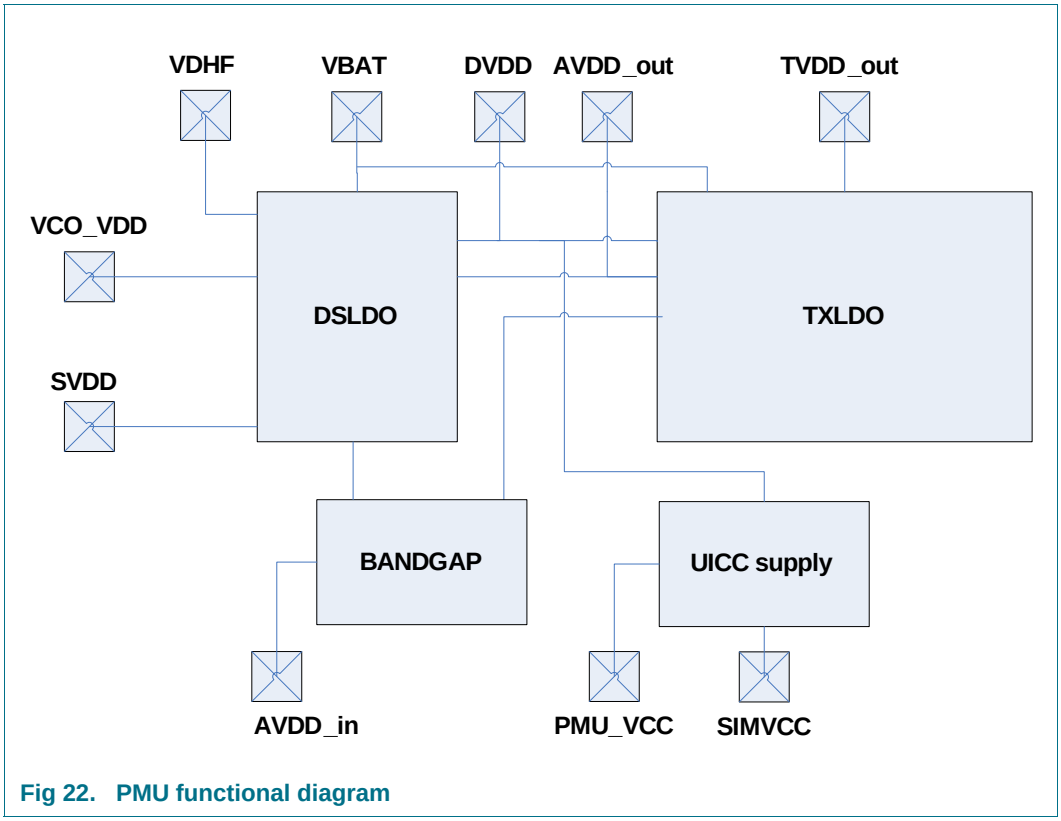


Fig 22. PMU functional diagram

10.6.3 DSLDO: Dual Supply LDO

The input pins of the DSLDO are VBAT and VDHF

The Low drop-out regulator provides different supplies required in PN544.

- AV_{DD}: Analog supply
- DV_{DD}: Digital supply
- VCO_V_{DD}: Analog supply dedicated to the VCO of the FracNpll
- SV_{DD}: Supply of the Secure Element

10.6.4 TXLDO

This is the LDO which generates the transmitter voltage.

The value of TV_{DD} can be configured by a host command to 2.7V, 3V or 3.3V.
TVDD is set by default to 3V.

TV_{DD} value shall be chosen according the minimum targeted V_{BAT} value for which reader mode shall work.

$$V_{BATmin} \geq 3.3V \Rightarrow TV_{DD} = 3.3V$$

$$3.3V \geq V_{BATmin} \geq 3.0V \Rightarrow TV_{DD} = 3V$$

$$3.0V \geq V_{BATmin} \geq 2.7V \Rightarrow TV_{DD} = 2.7V$$

TV_{DD} value can be configured with an offset compared to V_{BAT}. With offset enabled the TXLDO is able to filter V_{BAT} bursts for V_{BAT} near the programmed TV_{DD} value. When V_{BAT}-0.5V < TV_{DD} the offset is enabled. 0.5V is a typical value, its spread is +/-150mV. When at threshold where offset gets enabled TV_{DD} goes down to typical V_{BAT}-0.8V. This offset can be enabled or disabled by a host command (refer to Ref. 7 “PN544 User Manual”). By default the offset is enabled.

The supervisor implemented in the TXLDO is monitoring VBAT once the block is activated.

Three levels of V_{BAT} are thresholds of detection for the offset mode according to pre-configured TV_{DD} level:

- If pre-configured TV_{DD} is 3.3V, then when V_{BAT} < 3.8V typical, TV_{DD} is set to 3.0V
- If pre-configured TV_{DD} is 3.0V, then when V_{BAT} < 3.5V typical, TV_{DD} is set to 2.7V
- If pre-configured TV_{DD} is 2.7V, then when V_{BAT} < 3.2V typical, TV_{DD} is set to 2.4V

Once V_{BAT} reaches the same voltage as T_{VDD} (with or without offset configuration), T_{VDD} will follow V_{BAT} voltage with a drop-out of 100mV typical.

Figure 23 shows the case where TV_{DD} is configured to 3V and offset is enabled.

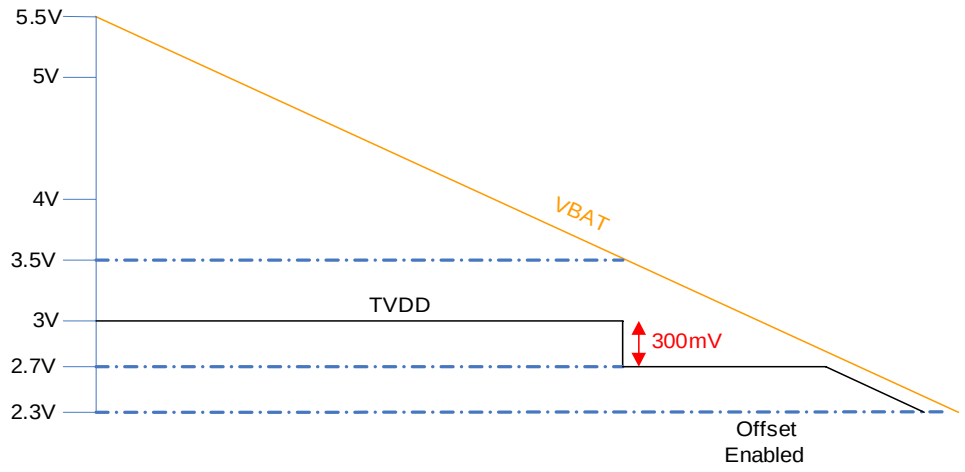


Fig 23. TV_{DD} offset enabled behavior

Figure 24 shows the case where TV_{DD} is configured to 3V and offset is disabled.

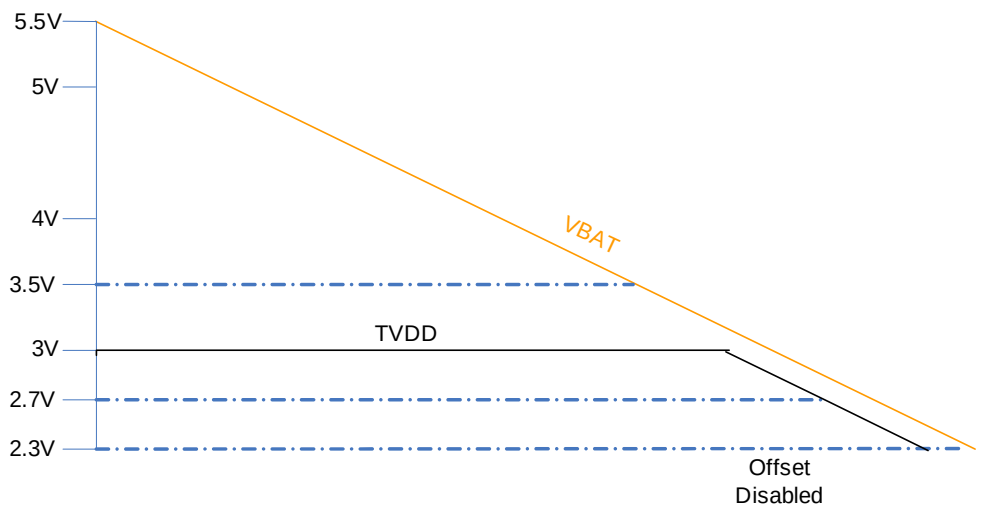


Fig 24. TV_{DD} offset disabled behavior

10.6.4.1 TXLDO limiter

The TXLDO includes a current limiter to avoid too high current within TX1, TX2 when in reader or initiator modes.

The current limiter block compare an image of the TXLDO output current to a reference. Once the reference is reached, which is equivalent to a typical output current of 165mA, the output current gets limited to that value.

Before reaching that value the limiter sends a flag to the embedded FW. It occurs when the output current is typically 130mA. If the overcurrent interrupt is enabled, which is strongly recommended, the embedded FW disables the TXLDO and the overcurrent consumption disappears. It allows a self protection of PN544 and avoid high power dissipation.

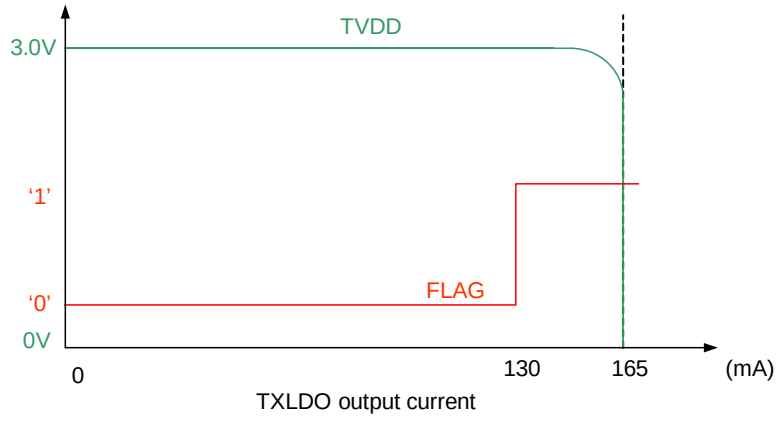


Fig 25. TXLDO limiter without overcurrent interrupt enabled

10.6.5 Secure Element supply

The DSLDO described above is generating SV_{DD}.
This supply is used to supply Secure Element connected over NFC-WI.
References of SV_{DD} supply are in Table 1 “Quick reference data” on page 3.

10.6.6 UICC supply

The UICC supply block is in charge to deliver the proper supply for the external UICC and also to provide SWIO data signal.

At the phone level, the UICC supply (UICC C1 pin = VCC as described in the ETSI/SCP 102.221) might be connected to either PN544 SIMVCC pin, or directly from a PMU/LDO of the phone.

When using SIMVCC to supply the UICC, to allow the phone to communicate with the UICC when PN544 is in Hard-Power-Down, PMUVCC pin has been added and shall be connected to the PMU/LDO output which is used as reference for the ETSI/SCP 102.221 interface of the UICC. SIMVCC voltage is present as soon as the PMU/LDO voltage is present and it is of the same class. PN544 withstands 1.8 V (class C) or 3 V (class B).

When using PMU/LDO to directly supply the UICC, PMUVCC shall also be connected to the same supply in order to guarantee the compatibility of the SWIO S1 signal with the Ref. 1 “ETSI SWP” specification for both 1.8 V (class C) or 3 V (class B). When in class C, the SWIO signal is directly generated from $PMUV_{CC}$ voltage, whereas in class B it is derived from DV_{DD} , internal 1.8V reference.

As seen 2 paragraphs above, when using SIMVCC to supply the UICC, then PMUVCC is connected to the PMU/LDO which gives the power supply used by the ETSI/SCP 102.221 interface. If the PMU/LDO is disabled, then a switch has been added to derive from DVDD, 1.8 V supply for SIMVCC, so that PN544 can still supply the UICC. As for DVDD, SIMVCC is either generated from the remaining battery voltage or from the RF field power if the Powered-by-Field mode is enabled. When PMUVCC is off, SIMVCC is only high when activity is required on SWIO.

Whatever the mode in which PN544 is, including Hard Power Down (V_{EN} < 1.1V), when $PMUV_{CC}$ rises, $SIMV_{CC}$ will follow $PMUV_{CC}$.

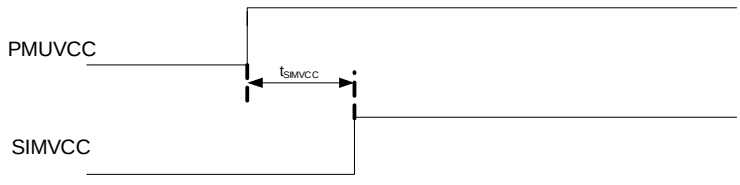


Fig 26. $SIMV_{CC}$ versus $PMUV_{CC}$

PN544 UICC circuitry is able to detect if $PMUV_{CC}$ is ON or OFF and from which class it is.

To meet the above functionality, the UICC block has been designed as follows:

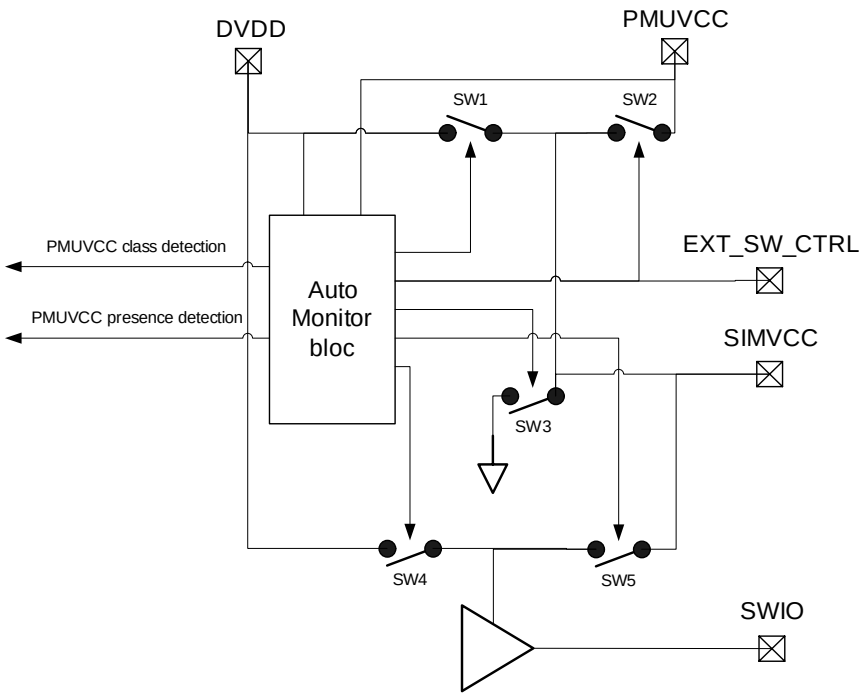


Fig 27. UICC supply functional diagram

The On resistance of the internal switch between PMUVCC and SIMVCC is designed to be below 1.5Ω. If this is too high for a given application, meaning that the voltage drop introduced by the switch is too high to keep the SIMVCC above the ETSI limits, (i.e. 2.7 V in class B and 1.62 V in class C), an external switch can be used to reduce the overall resistance of both switches in parallel. A signal is available on pin EXT_SW_CNTRL to drive the gate of the external switch which has to be made of 2 transistors connected in series in order to cancel the parasitic diodes.

Remark: A possible reference is FDMA1027P from Fairchild. The switch made with both transistors in series would have then the following max RdsOn: 240 mΩ × 2 = 480 mΩ at VGS = 1.8 V. assuming that the internal switch On resistance is 1500 mΩ, the overall On resistance would be: 363 mΩ.

In order to fulfill the ISO/IEC requirements, an internal switch will also connect SIMVCC to ground when the UICC is not supplied anymore (both internal switches are OFF).

If SWP only is used as an interface to the UICC, it is mandated that the unused pins have a voltage limited to ± 0.4 V with respect to ground. This can be guaranteed by the design of the ISO/IEC 7816 interface on the phone, but only when the battery is charged enough to bias the driver. If not, it is necessary to apply pull-downs on the 3 ISO/IEC 7816 signals (CLK, RST and IO). PN544 is not capable to permanently apply a pull-down on IO, otherwise the ISO/IEC 7816 interface may be disturbed. A workaround is to drive an external NMOS using the EXT_SW_CTRL pin from PN544.

In term of power scenarios it gives the following table:

Table 27. SWP reference supplies

IRQ of PMUVCC class detection enabled [1]				
Powering of UICC enable (bit 2 SECONF) [1]	**PMUVCC**	**SWP Activation required (RF, Host...)**	**$SIMV_{CC}$ reference supply**	**SWIO reference supply**
0	0V	No	0V	Not supplied
0	0V	Yes	0V	Not supplied
0	1.8V or 3.3V	No	PMUVCC	Not supplied
0	1.8V	Yes	PMUVCC	PMUVCC
0	3V	Yes	PMUVCC	Internal 1.8V reference[2]
1	0V	No	0V	Not supplied
1	0V	Yes	Internal 1.8V reference	Internal 1.8V reference
1	1.8V or 3.3V	No	PMUVCC	Not supplied
1	1.8V	Yes	PMUVCC	PMUVCC
1	3V	Yes	PMUVCC	Internal 1.8V reference

[1] See Ref. 7 “PN544 User Manual” for more information about how to set this feature

[2] If the IRQ of PMUVCC class detection is disabled then when PMUVCC voltage is pulled low, as the supply of UICC is done via the internal reference and the information of PMUVCC not given to embedded FW, the internal reference is not cut.

10.6.7 Battery voltage monitor

PN544 features low power V_{BAT} voltage monitor which protects phone battery from being discharged below critical levels. Refer to Figure 28 for principle schematic.

The battery voltage monitor is enabled via the pin VEN_MON.

The battery voltage monitor consists of ultra low power voltage reference (not depicted), supply switching logic and voltage threshold configuration logic (not depicted). If PN544 is activated by host via VEN pin and VEN_MON is high, the battery voltage monitor is powered and active. When PN544 monitors battery voltage continuously as long as VEN pin is active and detaches battery supply once the critical level is reached.

If PN544 has been disabled by the host (V_{EN} is low), than the battery voltage monitor is also detached from the battery in order not to consume any power.

In both cases PN544 can be powered by the energy from the field only.

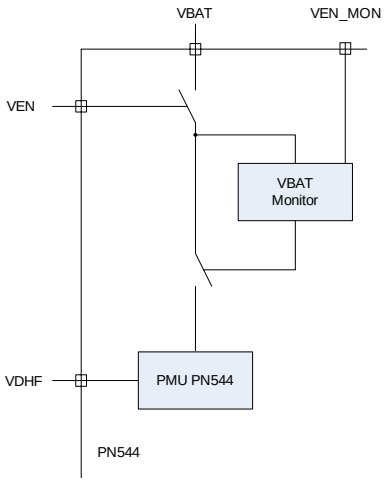


Fig 28. Battery voltage monitor principle

The battery voltage monitor threshold value is fixed to 2.6V with a typical hysteresis of around 100mV.

10.6.8 Powered-by-Field mode (PbF)

When in a RF field at 13.56MHz, PN544 can be fully or partially powered from it, see Section 10.6.1 “PN544 core supply sources” on page 39. To get benefit of this feature the antenna shall be connected to ANT1 and ANT2 pins as described in Ref. 9 “PN544 Antenna Design Guide”.

The RF field strength at which power can be extracted from the field is strongly dependant of the antenna tuning and of the system environment.

PbF will only be possible if the field is strong enough to have AV_{DD} and DV_{DD} above APOR and DPOR thresholds, whatever the battery monitor circuitry is enabled or not. It corresponds to VDHF is around 2.5V.

The voltages on ANT1 and ANT2 is limited via an internal limiter at 3.3V typical, which corresponds to 2.7V on VDHF pin.

10.6.9 Thermal protection

In case of failure (short of TX1, TX2 or TVDD) the current consumption can increase up to the limiters value. In case the overcurrent detection interrupt is disabled (which is not the recommended configuration) the TXLDO can sink continuously up to nearly 200mA. PN544 will be heating, therefore a thermal protection is included.

The thermal protection is triggered at 125°C typical. When it happens the embedded FW do the following sequence:

- shuts down the TXLDO
- informs host
- waits 50ms to get host answer
- enters the STANDBY mode, then no wake-up possible until over temperature disappears

When over temperature disappears:

- wakes-up and goes to Active battery mode (ActiveBAT)
- informs host

10.7 Reset and download concept

10.7.1 Resetting PN544

To enter reset there are 3 ways:

- Pulling V_{EN} low (Hard Power-Down mode)
- if VBAT monitor is enabled: lowering V_{BAT} below the monitor threshold (Monitor mode, if V_{EN} is kept above 1.1V)
- if VBAT monitor is disabled, when V_{BAT} goes below 2.1V typical (from 1.9V to 2.3V).

This reset mode can be left if PbF is enabled when the field is high enough (RF field detected, AV_{DD} and DV_{DD} are above 1.55V) to enter PbF mode.

Reset means resetting the embedded FW execution and the registers values to their default values. Part of these default values are defined from EEPROM data loaded values, others are hardware defined. See Ref. 7 “PN544 User Manual” to know which ones are accessible to tune PN544 to the application environment.

To get out of reset there are 3 ways:

- Pulling V_{EN} high with
  - VBAT above VBAT monitor threshold if enabled
  - VBAT above 2.1V typical if VBAT monitor is disabled
- Entering a field strong enough to have AV_{DD} and DV_{DD} above 1.55V

Herebelow the figure showing reset done via VEN pin

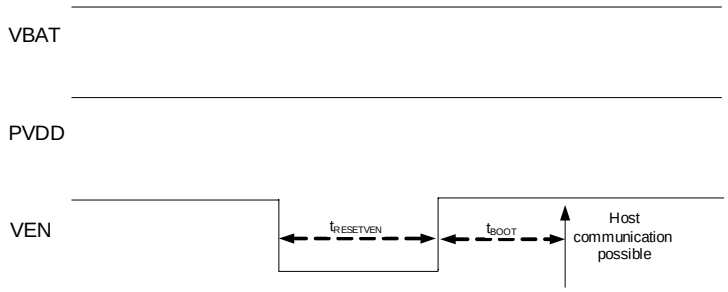


Fig 29. Resetting PN544 via VEN pin

See Section 15.2.4 for the timings values.

10.7.2 Power-up sequences

There are 2 different supplies for PN544. PN544 allows these supplies to be set-up independently, therefore different power-up sequences have to be considered.

10.7.2.1 V_{BAT} is set-up before PV_{DD}

This is at least the case when VBAT pin is directly connected to the battery and when PN544 V_{BAT} is always supplied as soon the system is supplied.

As VEN pin is referred to VBAT pin, VEN shall go high after VBAT has been set.

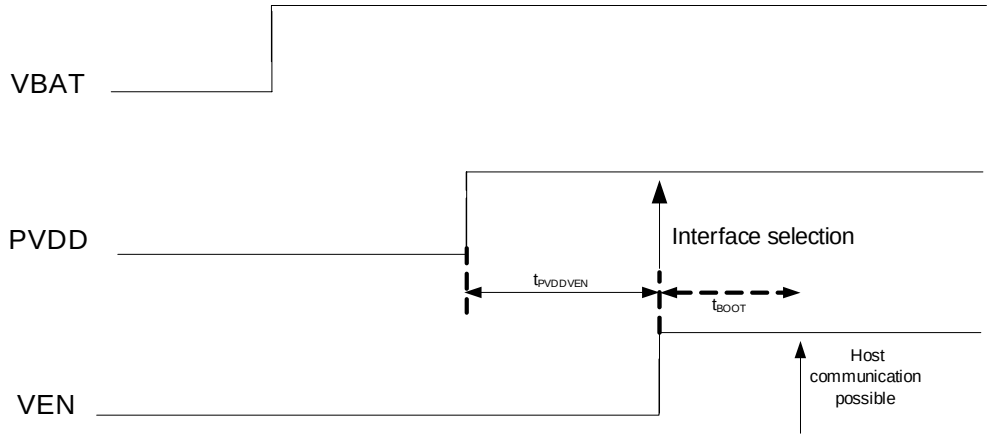


Fig 30. V_{BAT} is set-up before PV_{DD}

See Section 15.2.5 for the timings values.

10.7.2.2 PV_{DD} is set-up before V_{BAT}

It is at least the case when VBAT is connected to a PMU/regulator and PV_{DD} is used for other purposes than NFC device. Then for power optimization the system might set-up PV_{DD} without setting up V_{BAT}.

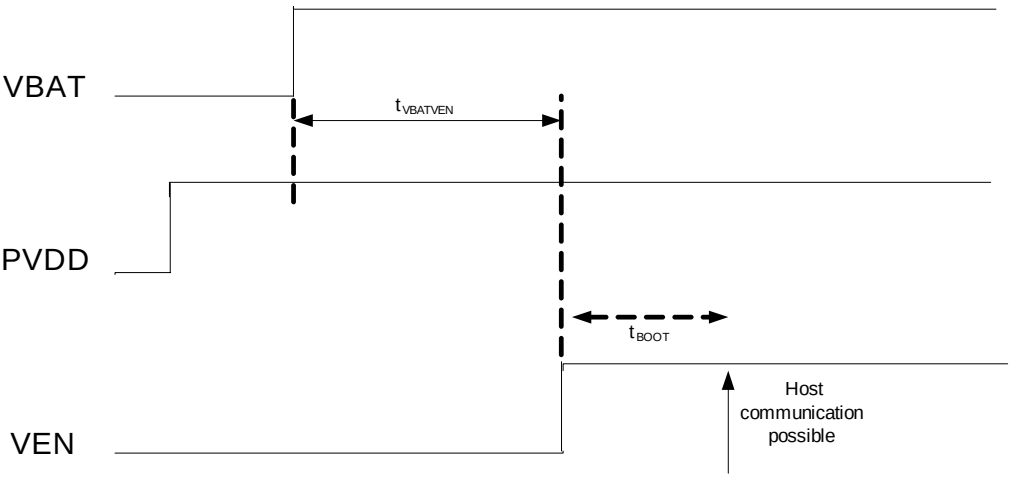


Fig 31. PV_{DD} is set-up before V_{BAT}

See Section 15.2.5 for the timings values.

10.7.2.3 PN544 has been enabled before PV_{DD} is set or before PV_{DD} has been cut

This can be the case when VBAT is directly connected to the battery and when PV_{DD} is generated from a PMU. When the battery voltage is too low, then the PMU might no more be able to generate PV_{DD}. When the device gets charged again then PV_{DD} is set-up again.

As the pins to select the interface are biased from PV_{DD}, when PV_{DD} disappears the pins might not be correctly biased internally and the information might be lost. Therefore it is required to make the IC boot after PV_{DD} is set-up again.

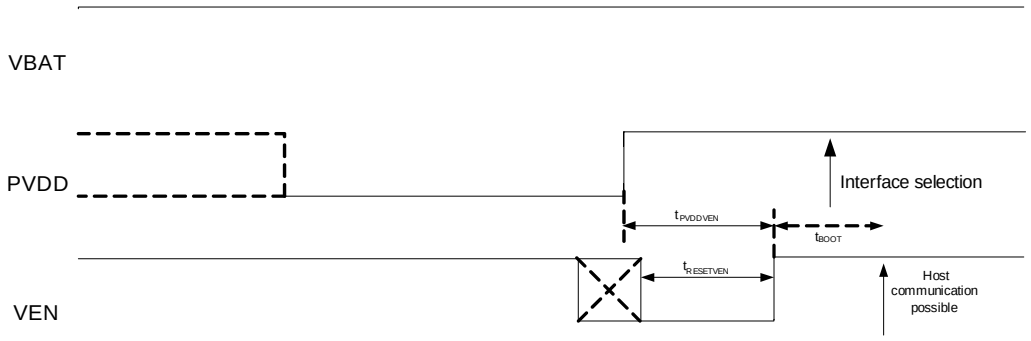


Fig 32. PV_{DD} is set-up or cut after PN544 has been enabled

See Section 15.2.5 for the timings values.

10.7.3 Download mode

PN544 offers the possibility to download EEPROM with upgrades using the host interface commands, see Ref. 7 “PN544 User Manual” for more details.

To enters this mode the pin GPIO4 shall be pull to PV_{DD} before Reset via VEN pin is done.

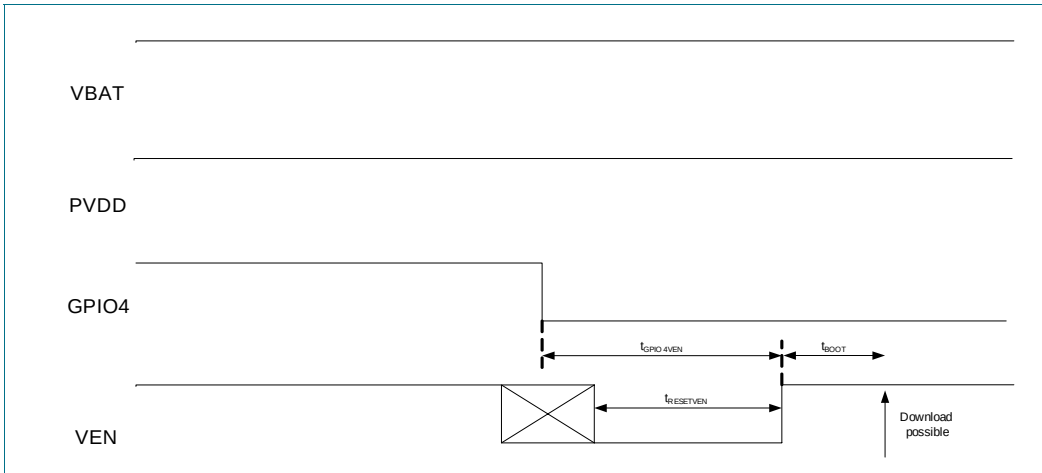


Fig 33. PN544 download mode sequence

See Section 15.2.6 for the timings values.

10.8 Contactless interface Unit

PN544 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Note: All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

10.8.1 Reader/Writer modes

Generally 5 Reader/Writer modes are supported:

- PCD reader/writer for ISO/IEC 14443A/MIFARE
- PCD reader/writer for JEWEL/TOPAZ tags
- PCD reader/writer for FeliCa cards
- PCD reader/writer for ISO/IEC 14443B
- VCD reader/writer for ISO/IEC 15693/ICODE.

10.8.1.1 ISO/IEC 14443-A/MIFARE and JEWEL/TOPAZ PCD mode

The ISO/IEC 14443-A/MIFARE PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-A specification. This modulation scheme is as well used for communications with JEWEL/TOPAZ cards.

The following diagram describes the communication on a physical level, the communication table describes the physical parameters (the numbers take the antenna effect on modulation depth for higher datarates).

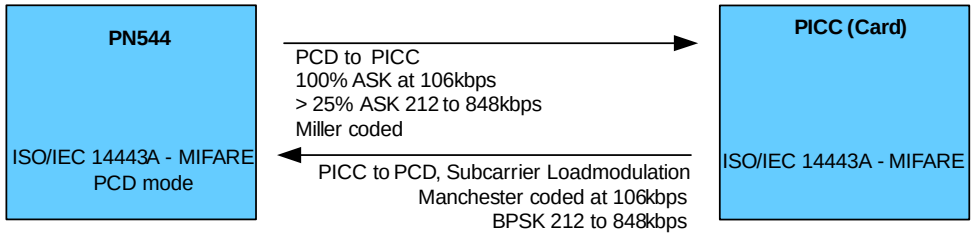


Fig 34. ISO/IEC 14443A/MIFARE Reader/Writer mode communication diagram

Table 28. Communication overview for ISO/IEC 14443A/MIFARE reader/writer

Communication direction		**ISO/IEC 14443A MIFARE JEWEL TOPAZ**	**ISO/IEC 14443A higher transfer speeds**		
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
Bit length		(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN544 → PICC (Data sent by PN544 to a card)	Modulation on PN544 side	100% ASK	>25% ASK	>25% ASK	>25% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC → PN544 (Data received by PN544 from a card)	Modulation on PICC side	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	Manchester coding	BPSK	BPSK	BPSK

The contactless CoProcessor and the on-chip CPU of PN544 handle the complete ISO/IEC 14443-A/MIFARE RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.8.1.2 FeliCa PCD mode

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication overview describes the physical parameters.

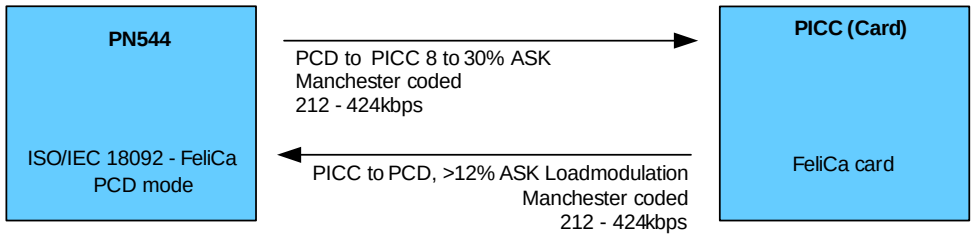


Fig 35. FeliCa reader/writer Communication Diagram

Table 29. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
Bit length		(64/13.56) µs	(32/13.56) µs
PN544 → PICC (Data sent by PN544 to a card)	Modulation on PN544 side	8 - 30% ASK	8 - 30% ASK
	Bit coding	Manchester Coding	Manchester Coding
PICC → PN544 (Data received by PN544 from a card)	Modulation on PICC side	Load modulation	Load modulation
	Subcarrier frequency	No subcarrier	No subcarrier
	Bit coding	Manchester coding	Manchester coding

The contactless CoProcessor of PN544 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

10.8.1.3 ISO/IEC 14443B PCD mode

The ISO/IEC 14443-B PCD mode is the general reader to card communication scheme according to the ISO/IEC 14443-B specification.The following diagram describes the communication on a physical level, the communication table describes the physical parameters.

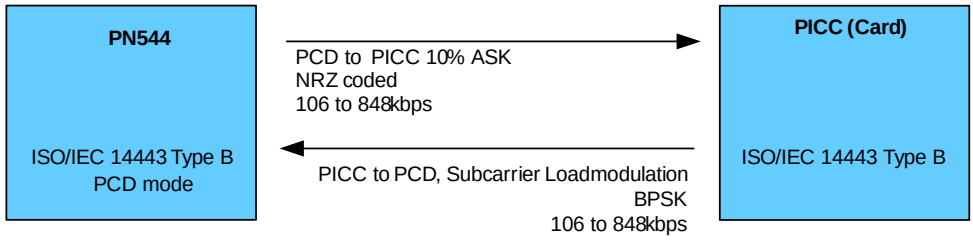


Fig 36. ISO/IEC 14443B reader/writer communication diagram

Table 30. Communication overview for ISO/IEC 14443B reader/writer

Communication direction		**ISO/IEC 14443B**	**ISO/IEC 14443B higher transfer speeds**		
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
Bit length		(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN544 → PICC (Data sent by PN544 to a card)	Modulation on PN544 side	8-14% ASK	8-14% ASK	8-14% ASK	8-14% ASK
	Bit coding	NRZ	NRZ	NRZ	NRZ
PICC → PN544 (Data received by PN544 from a card)	Modulation on PICC side	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	BPSK	BPSK	BPSK	BPSK

The contactless CoProcessor and the on-chip CPU of PN544 handles the complete ISO/IEC 14443-B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.8.1.4 ISO/IEC 15693 VCD mode

The ISO/IEC 15693 VCD reader/writer mode is the general reader to card communication scheme according to the ISO/IEC 15693 specification. PN544 will communicate with VICC using only the higher datarates of the VICC (26.48kbit/s with single subcarrier and 26.69kbit/s with dual subcarrier).

PN544 supports the commands as defined by the ETSI HCI (see Ref. 2 “ETSI HCI”), and on top offers the inventory of the tags (anticollision sequence) on its own.

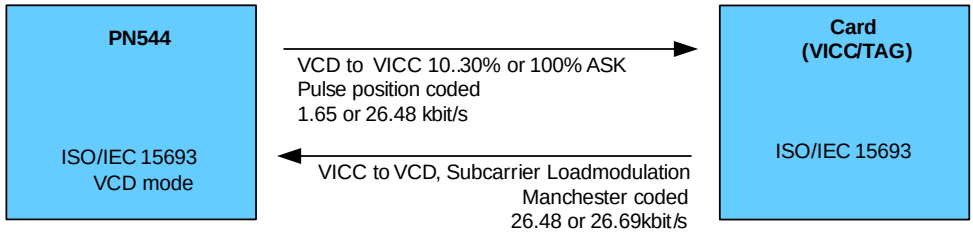


Fig 37. ISO/IEC 15693 VCD mode communication diagram

The following figures shows the communication schemes used.
2 communication schemes can be used from card to PN544 and 2 communication schemes can be used from PN544 to card.
Thus, 4 communication schemes are possible.

Table 31. Communication overview for ISO/IEC 15693 VCD

Communication direction			
PN544 → VICC	**Transfer speed**	**1.65 kbit/s**	**26.48 kbit/s**
(Data sent by PN544 to a tag)	Bit length	(8192/13.56) µs	(512/13.56) µs
	Modulation on PN544 side	10-30% or 100% ASK	10-30% or 100% ASK
	Bit coding	Pulse Position Modulation 1 out of 256 mode	Pulse Position Modulation 1 out of 4 mode
VICC → PN544	**Transfer speed**	**26.48 kbit/s**	**26.69 kbit/s**
(Data received by PN544 from a tag)	Bit length	(512/13.56) µs	(508/13.56) µs
	Modulation on VICC side	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	Single Subcarrier	Dual Subcarrier
	Bit coding	Manchester coding	Manchester coding

10.8.2 ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode

A NFCIP-1 communication takes place between 2 devices:

- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data
- Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme. The Initiator is active in terms of generating the RF field.

In order to fully support the NFCIP-1 standard PN544 supports the Active and Passive Communications mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

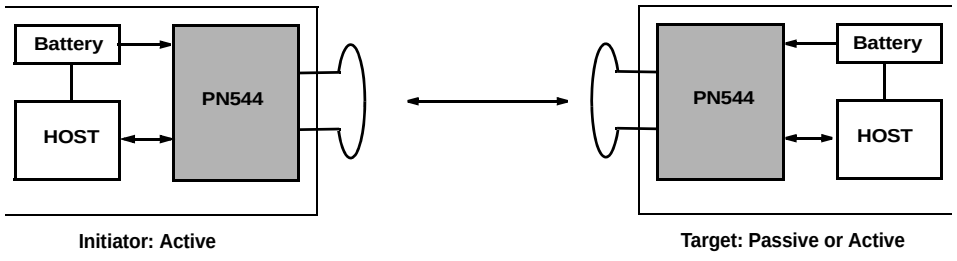


Fig 38. NFCIP-1 mode

The contactless CoProcessor of PN544 and the on-chip CPU handle NFCIP-1 protocol, for all communication modes and data rates, for both Initiator and Target. Nevertheless a dedicated external host has to handle the application layer communication.

10.8.2.1 ACTIVE Communication mode

Active Communication Mode means both the Initiator and the Target are using their own RF field to transmit data.

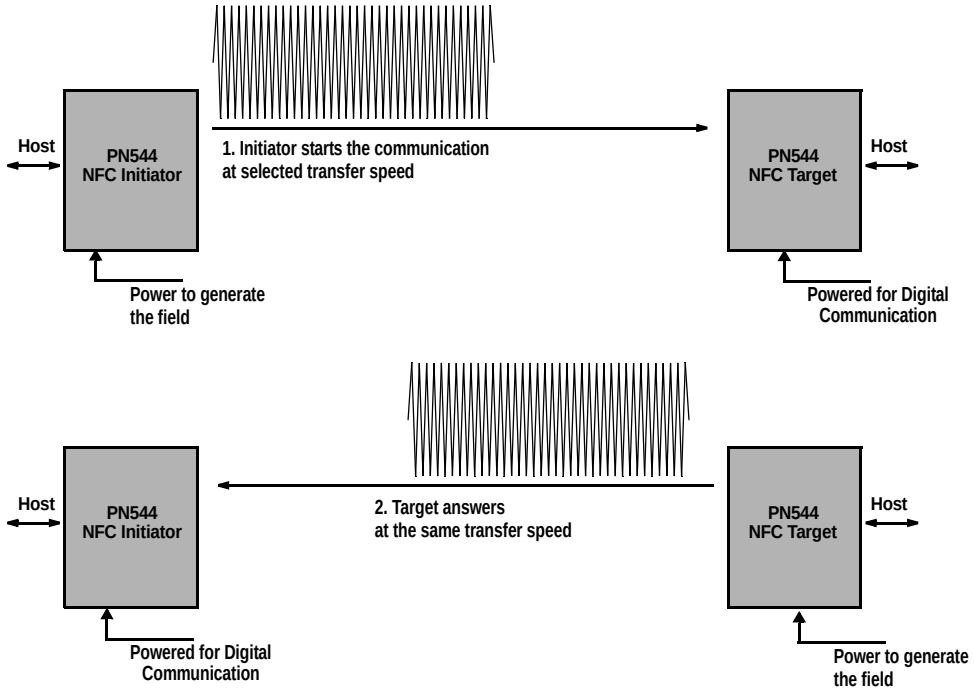


Fig 39. Active NFC mode

The following table gives an overview of the active communication modes:

Table 32. Communication overview for NFC Active Communication mode

Communication scheme		**ISO/IEC 18092, ECMA 340, NFCIP-1**		
Baud rate		**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		(128/13.56) μs	(64/13.56) μs	(32/13.56) μs
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Modified Miller Coded	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded

10.8.2.2 PASSIVE Communication mode

Passive Communication Mode means that the target answers to an Initiator command in a load modulation scheme.

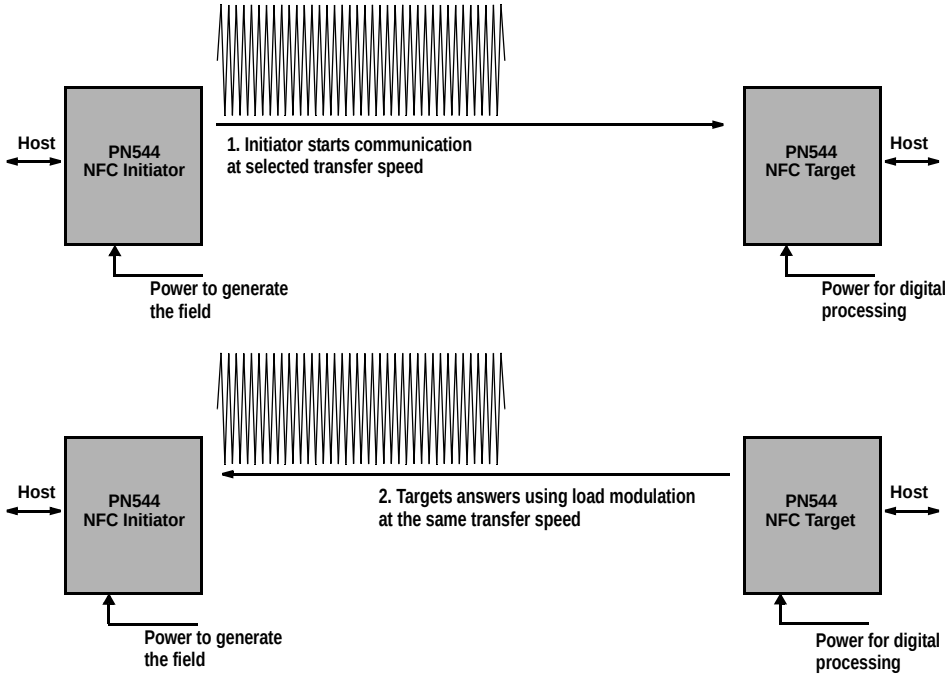


Fig 40. Passive NFC mode

The following table gives an overview of the active communication modes:

Table 33. Communication overview for NFC Passive Communication mode

Communication scheme		**ISO/IEC 18092, ECMA 340, NFCIP-1**		
Baud rate		**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		(128/13.56) μs	(64/13.56) μs	(32/13.56) μs
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Modified Miller coding	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	Subcarrier load modulation	Load modulation	Load modulation
	Subcarrier frequency	13.56 MHz/16	No subcarrier	No subcarrier
	Bit coding	Manchester coding	Manchester coding	Manchester coding

10.8.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or ECMA 340.

10.8.2.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the ISO/IEC 18092 or ECMA340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction.
- PSL shall be used to change the speed between the target selection and the data transfer, but the speed should not be changed during a data transfer.

10.8.3 Card Operation mode

PN544 can be addressed as a ISO/IEC 14443 A, MIFARE, ISO/IEC 14443 B or B' cards. This means that PN544 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A, ISO/IEC 14443B interface description.

MIFARE is supported via NFC-WI or via SWP CLT.

Note: PN544 does not support a complete card protocol. This has to be handled either by a connected companion Secure Element or the host controller.

The following tables describe the physical parameters.

10.8.3.1 ISO/IEC 14443-A / MIFARE Card Operation mode

Table 34. ISO/IEC 14443-A / MIFARE Card Operation mode

Communication direction		**ISO/IEC 14443A/ MIFARE**	**ISO/IEC 14443A higher transfer speeds**	
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN544 (Data received by PN544 from a reader)	Modulation on PCD side	100% ASK	> 25% ASK	>25% ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
PN544 → PCD (Data sent by PN544 to a card)	Modulation on PN544 side	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	Manchester coding	BPSK	BPSK

10.8.3.2 ISO/IEC 14443 B and B' Card Operation mode

Table 35. ISO/IEC 14443 B Card Operation mode

Communication direction		**ISO/IEC 14443B**	**ISO/IEC 14443B higher transfer speeds**	
	transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN544 (Data received by PN544 from a reader)	Modulation on PCD side	8-14% ASK	8-14% ASK	8-14% ASK
	Bit coding	NRZ	NRZ	NRZ
PN544 → PCD (Data sent by PN544 to a card)	Modulation on PN544 side	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	BPSK	BPSK	BPSK

10.8.4 Frequency inter operability

When in communication, PN544 is generating some RF frequencies. PN544 is also sensitive to some RF signals as it is looking from data in the field.

In order to avoid interference with others RF communication it is required to tune the antenna and design the board according to Ref. 9 “PN544 Antenna Design Guide”.

Whenever ISO/IEC 14443 and ISO/IEC 18092 / ECMA 340 allows an RF frequency of 13.56MHz +/-7kHz, FCC regulation does not allow this wide spread and limits the dispersion to +/-50ppm, which is in line with PN544 capability.

10.9 Support for production test and implementation

PN544 supports several tests functions which ease test in final application production environment.

- Antenna self test:
  If the antenna tuning is done according recommendations given in Ref. 9 “PN544 Antenna Design Guide”, this test can detect that all tuning components are present with the right value.
  Refer to Ref. 7 “PN544 User Manual” to know how to use the associated commands.
- SWP self test
  This function checks the connection of SWIO and PMUVCC lines.
  Refer to Ref. 7 “PN544 User Manual” to know how to use the associated commands

To allow easy integration of PN544 within the application environment some internal signals can be displayed. Refer to Ref. 10 “PN544 RF setting Guide”

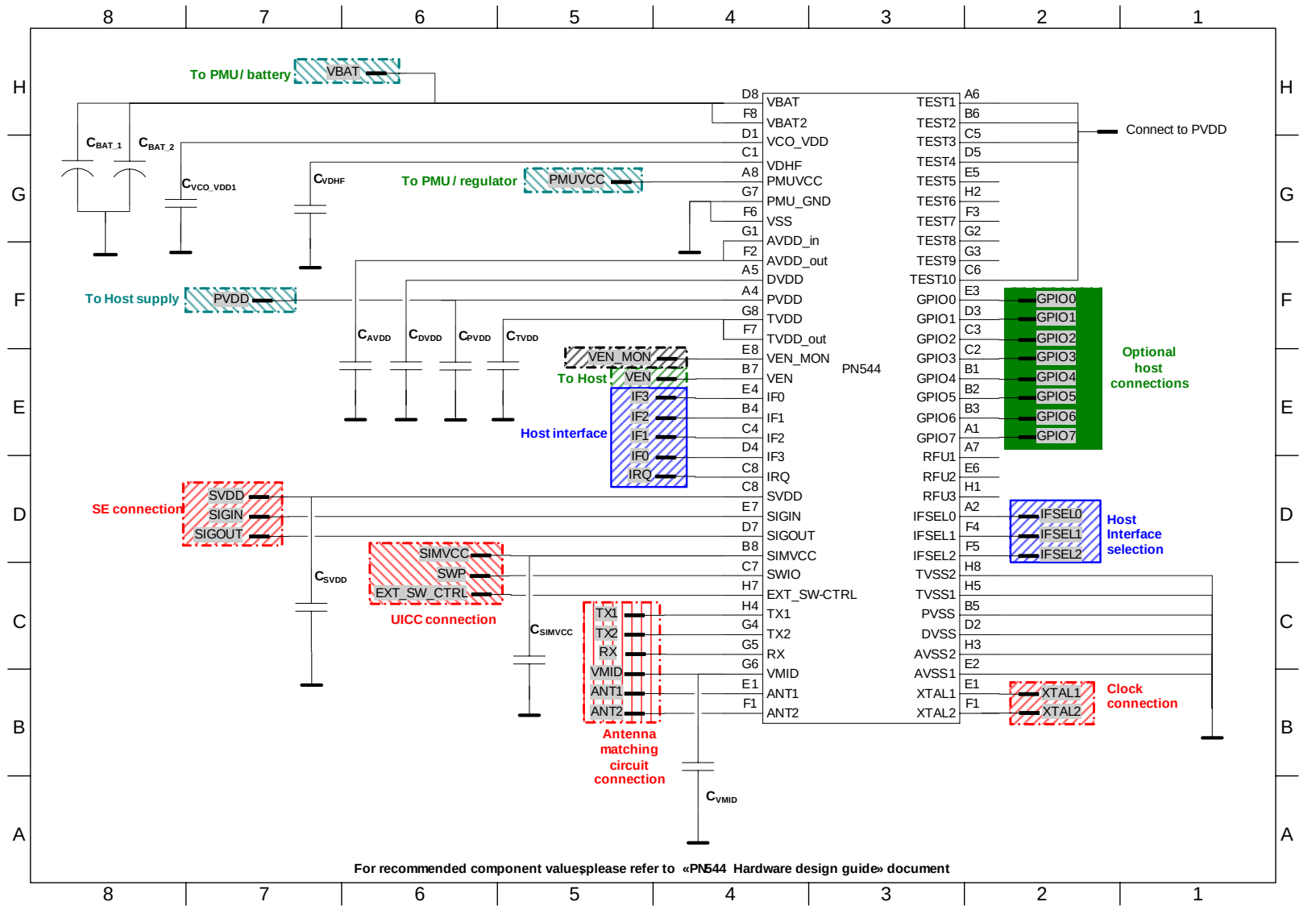


Fig 41. Application schematic 1

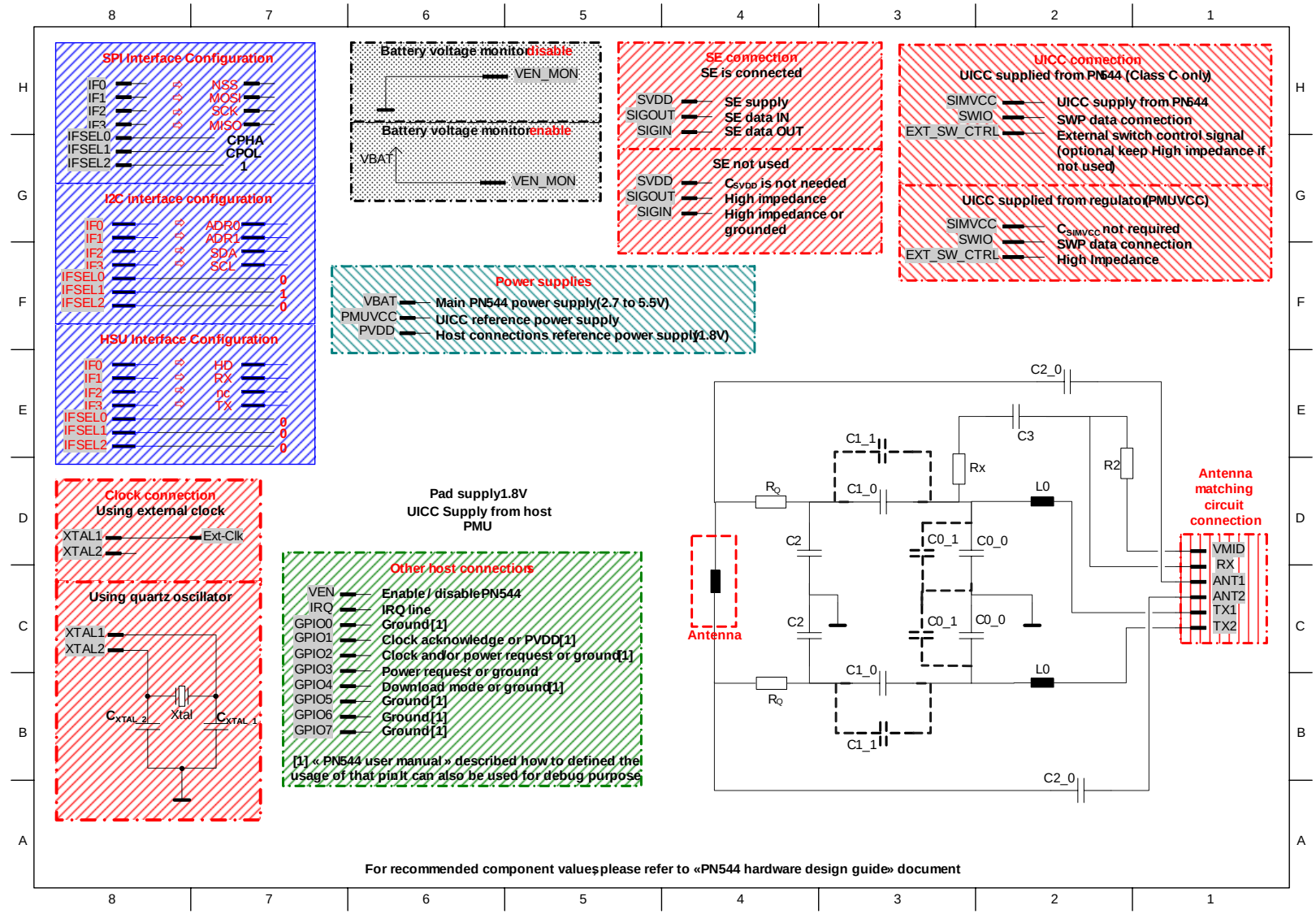


Fig 42. Application schematic 2

12. Limiting values

Table 36. Limiting values (in accordance with the Absolute Maximum Rating System (IEC 60134))

Symbol	Parameter	Conditions		Min	Max	Unit
PV_{DD}	Pad Supply Voltage				2.5	V
V_{BAT}	Power Supply Voltage				6	V
V_{ESDH}	ESD Susceptibility (Human Body model)	1500 Ω, 100pF; EIA/JESD22-A114-D			1	kV
V_{ESDC}	ESD Susceptibility (Charge Device model)	Field induced model; EIA/JESC22-C101-C			750	V
T_{stg}	Storage temperature			-55	150	°C
P_{tot}	Total power dissipation	all modes	[1]		0.5	W

[1] The design of the solution shall be done so that for the different use cases targeted the power to be dissipated from the field or generated by PN544 does not exceed this value.

13. Recommended operating conditions

Table 37. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	Ambient Temperature			-30	+25	+85	°C
V_{BAT}	Battery Supply Voltage	Battery monitor enabled V_{SS} = 0 V		2.85	-	5.5	V
V_{BAT}	Power Supply Voltage Card emulation mode	Battery monitor disabled V_{SS} = 0 V	[1] [2]	2.3		5.5	V
V_{BAT}	Power Supply Voltage Reader mode	Battery monitor disabled V_{SS} = 0 V	[1] [2]	2.7		5.5	V
PV_{DD}	Supply Voltage for host interface	V_{SS} = 0 V	[1]	1.65	1.8	1.95	V
t_{VBAT}	V_{BAT} slew rate	$V_{VEN\_MON} = V_{BAT}$ V_{BAT} drop is above 1V	[3]			0.1	V/µs
t_{VBAT}	V_{BAT} slew rate	$V_{VEN\_MON} = V_{BAT}$ V_{BAT} drop is below 1V	[3]			1	V/µs
P_{tot}	Total power dissipation	Reader mode I_{TVDD}=100mA V_{BAT}=5.5V				0.5	W
I_{TVDD_OUT}	Maximum current in TVDD		[4]	100			mA
I_{SVDD}	Maximum current in SVDD switch	V_{BAT}>2.3V		20			mA
I_{SVDD}	Maximum current in SVDD switch	Powered-by-Field, VDHF>2.5V	[2]	5			mA

[1] V_{SS} represents PV_{SS}, DV_{SS}, AV_{SS1}, AV_{SS2}, TV_{SS1}, TV_{SS2}.

[2] Supply voltage of V_{BAT} below 3.6 V can reduce the performance in reader/writer mode (e.g. the achievable operating distance).

[3] If VEN_MON pin is grounded, the limiting value on V_{BAT} slew rate is not applicable

[4] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

14. Thermal characteristics

Table 38. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{thj-a}	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer Jedec PCB-0.5		80	85	K/W

15. Characteristics

15.1 Current consumption characteristics

Table 39. Current consumption characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HPD}	Hard-Power-down current	V_{BAT}=3V, V_{EN}=0V			3	6	µA
I_{STBY}	Standby mode current	V_{BAT}=3V V_{VEN_MON} is grounded SWIO is pulled-down	[4] [5] [6]		44	55	µA
I_{STBY}	Standby mode current	V_{BAT}=5.5 V V_{VEN_MON} is grounded SWIO is pulled-down	[4] [5] [6]		60	70	µA
I_{MON}	Monitor mode current	V_{BAT} = 3 V			7	10	µA
I_{PVDD}	Total current which can be pulled on PVDD referenced outputs	PV_{DD} = 1.95 V				15	mA
I_{TVDD}	Transmitter supply current	Continuous wave, TV_{DD} = 3 V	[1] [3]		30	100	mA
I_{PMU_VCC}	PMU_VCC supply current	Class B, no SWP activity			35	45	µA
I_{PMU_VCC}	PMU_VCC supply current	Class C, no SWP activity			15	20	µA

[1] I_{TVDD} depends on TV_{DD} and on the external circuitry connected to Tx1 and Tx2.

[2] I_{SVDD} depends on the overall load on S_{VDD} pad, the minimum value given here shall not be exceeded by the connected secure element to guarantee proper functionality in all operating range.

[3] During operation with a typical circuitry as recommended by NXP in Ref. 9 “PN544 Antenna Design Guide”, the overall current is below 100 mA even when loaded by target/card/tag

[4] If V_{VEN_MON} >1.1V, then the current is increased by 6µA maximum

[5] If SWIO is configured in High Impedance, then the current is increased by 5µA maximum.

[6] Standby current is current driven V_{BAT} pin. To have PN544 overall current consumption in standby mode, current on PMU_VCC shall be added.

15.2 Functional block electrical characteristics

15.2.1 Battery voltage monitor characteristics

Table 40. Battery voltage monitor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{THRES}	Threshold voltage		2.5	2.61	2.72	V
V_{HYST}	Hysteresis voltage		85		115	mV

15.2.2 AV_{DD} and DV_{DD} reset thresholds

Table 41. AV_{DD} and DV_{DD} Power on reset thresholds characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
APOR	Power On Reset threshold voltage on AV_{DD}			1.55		V
DPOR	Power On Reset threshold voltage on DV_{DD}			1.55		V

15.2.3 UICC supply characteristics

The Ron resistors induced by switches are also specified as it has to be taken into account in design application environment.Refer to Figure 27 “UICC supply functional diagram” on page 44 for the meaning of the parameters.

Table 42. Electrical characteristics of UICC supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SIMVCC}	Time from $PMUV_{CC}$ present to $SIMV_{CC}$ present	$T_{rPMUVCC}$=10µs/V			20	µs
$PMUV_{CC}$_Thresh	Threshold for $PMUV_{CC}$ at which $SIMV_{CC}$ is supplied from $PMUV_{CC}$		0.2	0.5	0.85	V
ClassB_thresh	Class B detection threshold for $PMUV_{CC}$		2.2	2.4	2.6	V
$SIMV_{CC}$	SIMVCC voltage	PMUVCC to ground I_{SIMVCC}= 5 mA	1.62		1.98	V
Ron_SW2_B	Power switch SW2 RdsOn	$PMUV_{CC}$=2.75V, I_$SIMV_{CC}$=50mA		1	1.5	Ω
Ron_SW2_C	Power switch SW2 RdsOn	$PMUV_{CC}$=1.67V I_$SIMV_{CC}$=30mA		1.4	2	Ω
Ron_SW3	Power switch SW3 RdsOn	DV_{DD}=1.65V V_{BAT}=0V		600	1000	Ω
I_{SIMVCC}	Charging current on SIMVCC	$SIMV_{CC}$=1.0V $PMUV_{CC}$=1.8V	15	25	35	mA

15.2.4 Reset via VEN

Table 43. Reset timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{RESETVEN}$	VEN pulse width to reset	C_{AVDD}= 1µF C_{DVDD}= 100nF	[1]	7			ms
t_{BOOT}	Boot time					3	ms

[1] For larger capacitance value the time shall be increased. The time shall be long enough to have both AV_{DD} and DV_{DD} below 0.5V.

15.2.5 Power-up timings

Table 44. Power-up timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VBATVEN}$	Minimum time from V_{BAT} high to V_{EN} high	C_{AVDD}= 1µF C_{DVDD}= 100nF	0			ms
$t_{PVDDVEN}$	Minimum time from PV_{DD} high to V_{EN} high		0			ms

15.2.6 Download mode timings

Table 45. Download mode timings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{GPIO4VEN}$	Minimum time from GPIO4 voltage high to V_{EN} high		0			ms

15.2.7 Thermal protection

Table 46. Thermal threshold

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{overcurrent}$	Temperature at which the thermal protection is triggered		120	125	130	°C

15.2.8 I²C timings

Here below are timings and frequency specifications.

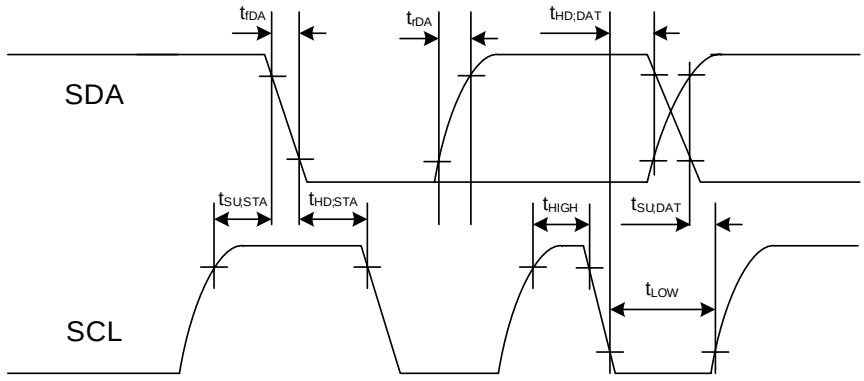


Fig 43. I²C timings

Table 47. High speed I²C timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLH}	SCLH clock frequency	Using t_{LOW} range	0	3.4	MHz
$t_{SU;STA}$	set-up time for a (repeated) START condition		160		ns
$t_{HD;STA}$	hold time (repeated) START condition		160		ns
t_{LOW}	LOW period of the SCL clock	C_b<100pF	215		ns
t_{HIGH}	HIGH period of the SCL clock	C_b<100pF	60		ns
$t_{SU;DAT}$	data set-up time		10		ns
$t_{HD;DAT}$	data hold time	C_b<100pF	6		ns
t_{rDA}	rise time of SDA	C_b<100pF	10	80	ns
t_{fDA}	fall time of SDA	C_b<100pF	10	80	ns
V_{hys}	hysteresis of Schmitt trigger inputs		$0.1xPV_{DD}$		V

Table 48. Fast mode I²C timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLH}	SCLH clock frequency		0	400	kHz
$t_{SU;STA}$	set-up time for a (repeated) START condition		600		ns
$t_{HD;STA}$	hold time (repeated) START condition		600		ns
t_{LOW}	LOW period of the SCL clock		1.3		µs
t_{HIGH}	HIGH period of the SCL clock		600		ns
$t_{SU;DAT}$	data set-up time		100		ns
$t_{HD;DAT}$	data hold time		30	900	ns
V_{hys}	hysteresis of Schmitt trigger inputs		$0.1xPV_{DD}$		V

15.2.9 SPI timings

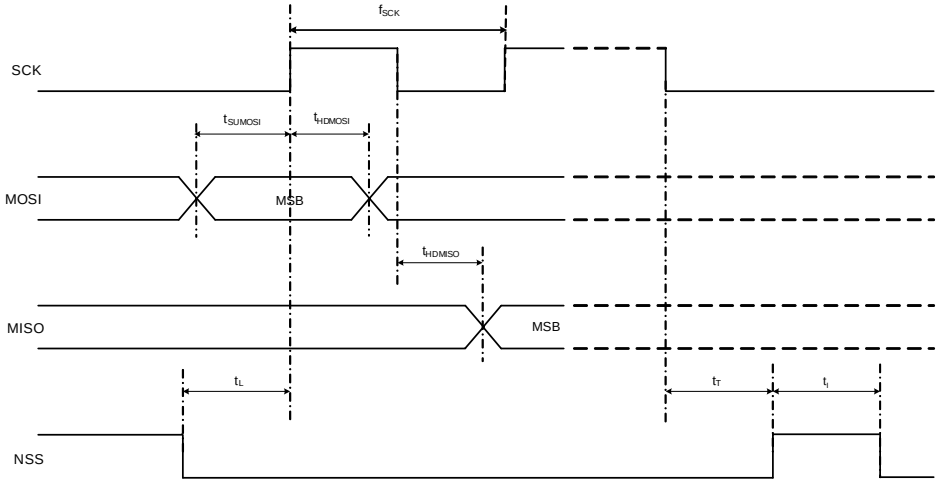


Fig 44. SPI timing diagram

Table 49. SPI timings specification

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK}	Frequency of SCK		0	9	MHz
t_{SUMOSI}	Set-up time for MOSI		25		ns
t_{HDMOSI}	Hold time for MOSI		25		ns
t_{HDMISO}	Hold time for MISO		25		ns
t_T	SCK low to NSS high		50		ns
t_L	NSS low to SCK high		100		ns
t_I	Idle time between two frames		50		ns

15.3 Pin characteristics

15.3.1 XTAL pin characteristics (XTAL1, XTAL2)

Table 50. Input clock characteristics on XTAL1 when using FracNpll

Parameter	Conditions		Min	Typ	Max	Unit
Input frequency			10		40	MHz
Input frequency accuracy	Using an optimally set FracNPLL	[1]	-400		400	ppm
Noise floor corner frequency				50		kHz
Noise floor	Offset frequency > 50 kHz				-140	dBc/Hz
Peak-peak input voltage			0.2		1.65	V
Duty Cycle			35		65	%

[1] The +/-400ppm are to meet +/-7kHz for generated 13.56MHz for ISO/IEC 14443 / 18092 and FCC.

Table 51. Pin characteristics for XTAL1 when FracNPLL input

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IH}	High level Input current	V_I=AV_{DD}				1	µA
I_{IL}	Low level input current	V_I=0V		-1			µA
V_{IH}	High level input voltage					AV_{DD}	V
V_{IL}	Low level input voltage			0			V
C_{IN}	Input Capacitance	All power modes			2		pF
F_{acc}	Output frequency accuracy	FracNPLL settings are optimally done	[1]	-10		10	ppm

[1] For preset frequency (13MHz, 19.2MHz, 26MHz and 38.4MHz) embedded FW set the FracNPLL to meet this requirement

Table 52. Pin characteristics for 27.12 MHz XTAL Oscillator

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{inXTAL1}$	XTAL1 Input Capacitance	AV_{DD}=1.8V, V_{DC}=0.65V, V_{AC}=0.9Vpp	[1]		2		pF
$V_{OHXTAL2}$	High level output voltage				1.1		V
$V_{OLXTAL2}$	Low level output voltage				0.2		V
$C_{INXTAL2}$	XTAL2 Input Capacitance				2		pF

[1] See the Figure 41 “Application schematic 1” on page 62 for example of appropriate connected components. The layout should ensure minimum distance between the pins and the components

15.3.2 VEN and VEN_MON input pin characteristics

Table 53. VEN and VEN_MON input pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.1		V_{BAT}	V
V_{IL}	Low level input voltage		0		0.4	V
I_{IH}	High level input current	$V_I=V_{BAT}$			1	µA
I_{IL}	Low level input current	V_I=0V	-1			µA
t_R	Input rise time				10	ms
t_F	Input fall time				10	ms
C_{IN}	Input capacitance			5		pF

15.3.3 Output pin characteristics for IRQ

Table 54. Output pin characteristics for IRQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	High level output voltage	I_{OH}= -100µA		PV_{DD}-0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}=100µA		0		0.2	V
V_{OH}	High level output voltage	I_{OH}= -2mA		0.85xPV_{DD}		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}=2mA		0		0.15xPV_{DD}	V
I_{IH}	High level input current	$V_I=PV_{DD}$ Extra Pull-down	[1]		4	10	µA
I_{IL}	Low level input current	V_I=0V Extra Pull-down	[1]	-1			µA
C_L	Load Capacitance					30	pF
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate enable		1.5		5	ns
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate disable		0.8		2.5	ns

[1] Extra Pull-down is activated in HPD, monitor and Powered-by-Field modes

15.3.4 Pin characteristics for GPIO2 and GPIO4

Table 55. Pin characteristics for GPIO2 and GPIO4

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.65 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.35 × PV_{DD}	V
V_{OH}	High level output voltage	I_{OH} = -100µA	PV_{DD} -0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL} = 100µA	0		0.2	V
V_{OH}	High level output voltage	I_{OH}= -2mA	0.85xPV_{DD}		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}= 2mA	0		0.15xPV_{DD}	V
I_{IH}	High level input current	V_I=PV_{DD} Extra Pull-down [1]		4	10	µA
I_{IL}	Low level input current	V_I=0V Extra Pull-down	-1			µA
I_{IH}	High level input current	V_I=PV_{DD} Pull-down		25	40	µA
I_{IL}	Low level input current	V_I=0V Pull-up	-40	-25		µA
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate enable	1.5		5	ns
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate disable	0.8		2.5	ns
C_{IN}	Input capacitance			5		pF
C_L	Load capacitance				30	pF

[1] Extra Pull-down is activated in HPD, monitor and Powered-by-Field modes

15.3.5 Pin characteristics for IFSELs

Table 56. Pin characteristics for IFSEL0, IFSEL1, IFSEL2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.65 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.35 × PV_{DD}	V
I_{IH}	High level input current	V_I=PV_{DD}			1	µA
I_{IL}	Low level input current	V_I=0V	-1			µA

15.3.6 Pin characteristics for TEST1, TEST2, TEST3, TEST4 and TEST10

Table 57. Pin characteristics for TEST1, TEST2, TEST3, TEST4 and TEST10

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	High level input current	V_I=PV_{DD}			1	µA
V_{IH}	High level Input voltage		0.65 × PV_{DD}		PV_{DD}	V

15.3.7 Pin characteristics for GPIOs, IF0 and IF1

Table 58. Pin characteristics for GPIO0, GPIO1, GPIO3, GPIO5, GPIO6, GPIO7, IF0, IF1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.65 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.35 × PV_{DD}	V
V_{OH}	High level output voltage	I_{OH}= -100µA	PV_{DD} -0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}=100µA	0		0.2	V
V_{OH}	High level output voltage	I_{OH}=-2mA	0.85xPV_{DD}		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}= 2mA	0		0.15xPV_{DD}	V
I_{IH}	High level input current	V_I=PV_{DD} High Impedance			1	µA
I_{IL}	Low level input current	V_I=0V High Impedance	-1			µA
I_{IH}	High level input current	V_I=PV_{DD} Pull-down		25	40	µA
I_{IL}	Low level input current	V_I=0V Pull-up	-40	-25		µA
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate enable	1.5		5	ns
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate disable	0.8		2.5	ns
C_{IN}	Input capacitance			5		pF
C_L	Load capacitance				30	pF

15.3.8 Pin characteristics for IF2, IF3

Table 59. Pin characteristics for IF2 and IF3 configured as I^2C pads

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.7 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.3 × PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}=3mA	0		0.2 x PV_{DD}	V
I_{IH}	High level input current	V_I=PV_{DD} High Impedance			1	µA
I_{IL}	Low level input current	V_I=0 V High Impedance	-1			µA
C_{IN}	Input capacitance			5		pF
C_L	Load capacitance		10		400	pF

Table 60. Pin characteristics for IF2 and IF3 not used as I²C pads

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage		0.65 × PV_{DD}		PV_{DD}	V
V_{IL}	Low level Input voltage		0		0.35 × PV_{DD}	V
V_{OH}	High level output voltage	I_{OH}= -100µA	PV_{DD} -0.2		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}=100µA	0		0.2	V
V_{OH}	High level output voltage	I_{OH}= -2mA	0.85xPV_{DD}		PV_{DD}	V
V_{OL}	Low level output voltage	I_{OL}= 2mA	0		0.15xPV_{DD}	V
I_{IH}	High level input current	V_I=PV_{DD} High Impedance			1	µA
I_{IL}	Low level input current	V_I=0V High Impedance	-1			µA
I_{IH}	High level input current	V_I=PV_{DD} Pull-down		25	40	µA
I_{IL}	Low level input current	V_I=0V Pull-up	-40	-25		µA
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate enable	1.5		5	ns
$t_{rise,fall}$	Rise and fall times	C_L=5pF max slew rate disable	0.8		2.5	ns
C_{IN}	Input capacitance			5		pF
C_L	Load capacitance				30	pF

15.3.9 SWIO pin characteristics

Table 61. Electrical characteristics of SWIO

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SWIO_VOH_B	Output High Voltage $PMUV_{CC}$ in class B	I_SWIO=1mA I_$SIMV_{CC}$=50 mA $PMUV_{CC}$=2.75V	[1]	1.4			V
SWIO_VOH_C_ext	Output High Voltage $PMUV_{CC}$ in class C	I_SWIO=1mA I_$SIMV_{CC}$=30mA $PMUV_{CC}$=1.67V	[1]	0.85 × $SIMV_{CC}$			V
SWIO_VOH_C_int	Output High Voltage $SIMV_{CC}$ = DV_{DD}	I_SWIO=1mA I_$SIMV_{CC}$=5mA $PMUV_{CC}$=0V	[1]	0.85 × $SIMV_{CC}$			V
SWIO_VOL	Output low voltage	0µA<I_SWIO<20µA	[1]			0.3	V
SWIO_IIH_240	Current threshold			145	240	335	µA
SWIO_IIH_270	Current threshold			165	270	375	µA
SWIO_IIH_300	Current threshold			180	300	420	µA
SWIO_IIH_330	Current threshold			200	330	460	µA
SWIO_IIH_susp	Current threshold	Suspend state		155	260	360	µA
I_{leak}	Leakage current	High Impedance		-1		1	µA

[1] To allow for overshoot the voltage on SWIO shall remain between -0,3 V and $V_{OH\ max}$ + 0,3 V during dynamic operation

Table 62. S1 waveform timings

Symbol	Parameter	Conditions		Min	Nom	Max	Unit
t_F	Fall time	C_{LOAD}<50 pF T<5000ns	[2]	5	-	0.05 × T	ns
		C_{LOAD}<50pF T>5000ns	[2]	5	-	250	ns
t_R	Rise time	C_{LOAD}<50pF T<5000ns	[1] [2]	5	-	0.05 × T	ns
		C_{LOAD}<50pF T>5000 ns	[1] [2]	5	-	250	ns
T_{H1}	Duration of the state H for coding a logical 1 of S1			0.70 × T	0.75 × T	0.80 × T	
T_{H0}	Duration of the state H for coding a logical 0 of S1			0.20 × T	0.25 × T	0.30 × T	
BR_{238k}	SWP Baud Rate	@238.1kbit/s	[3]	209		262	kb/s
BR_{454k}	SWP Baud Rate	@454.5kbit/s	[3]	400		500	kb/s
BR_{833k}	SWP Baud Rate	@833kbit/s	[3]	730		916	kb/s
BR_{1250k}	SWP Baud Rate	@1.25Mbit/s	[3]	1100		1375	kb/s

[1] Valid for the leading edge and the trailing edge of each bit

[2] Load capacitance is different than specified in ETSI to include capacitance of the connector and routing towards UICC

[3] This is compatible with Extended bit durations as defined in ETSI TS 102 613

15.3.10 ANT1 and ANT2 pin characteristics

Table 63. Electrical characteristics of ANT1 and ANT2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	Impedance between ANT1 and ANT2	Low impedance		10	17	Ω
I_{IH}	High input current	High Impedance			1	µA
I_{IL}	Low input current	High Impedance	-1			µA
V_{LIM}	Limiter threshold on ANT1 and ANT2	I = 10mA		3.3		V

15.3.11 Output pin characteristics for EXT_SW_CTRL

Table 64. Output pin characteristics for EXT_SW_CTRL

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	I_{OH}= -100µA	$SIMV_{CC}$-0.1		$SIMV_{CC}$	V
V_{OL}	Low level output voltage	I_{OL}=100µA	0		0.1	V
$t_{rise,fall}$	Rise and fall times	C_L=1nF		10		µs
C_{out}	Load Capacitance				2	nF

15.3.12 Input pin characteristics for SIGIN

Table 65. Input pin characteristics for SIGIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input voltage	1.65<SV_{DD}<1.95	1.1		SV_{DD}	V
V_{IL}	Low level Input voltage		0		0.7	V
I_{IH}	High level input current	V_I=SV_{DD} High Impedance			1	µA
I_{IL}	Low level input current	V_I=0V High Impedance	-1			µA
$t_{rise,fall}$	Input rise and fall times		4		20	ns
C_{in}	Input Capacitance				10	pF

15.3.13 Output pin characteristics for SIGOUT

Table 66. Output pin characteristics for SIGOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	DV_{DD}-0.1<SV_{DD}<DV_{DD} I_{OH}=-1 mA	1.32		SV_{DD}	V
V_{OL}	Low level output voltage	DV_{DD}-0.1<SV_{DD}<DV_{DD} I_{OL}=1 mA	0		0.3	V
C_{out}	Load Capacitance		10		30	pF
$t_{rise,fall}$	Rise and fall times	Between 10% to 90% SV_{DD} level C_{out} = 10 to 30 pF	4	12	20	ns

15.3.14 Input pin characteristics for RX

Table 67. Input pin characteristics for RX

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IH}	High level input current	V_I=AV_{DD}, Receiver OFF				1	µA
I_{IL}	Low level input current	V_I=0V Receiver OFF		-1			µA
V_{INRX}	Dynamic Input voltage Range		[1]	0		AV_{DD}	V
C_{inrx}	RX Input Capacitance				5		pF
R_{RXVMID}	Impedance from RX to VMID	Reader and Active modes			11.2		kΩ
R_{RXVMID}	Impedance from RX to VMID	Card emulation and passive modes			360		Ω
$V_{RX,MinIV,Mill}$	Minimum Dynamic Input voltage, Miller coded	106kbit/s			100	150	mVpp
$V_{RX,MinIV,Mill}$	Minimum Dynamic Input voltage, Miller coded	212 to 424kbit/s			150	200	mVpp
$V_{RX,MinIV,Man}$	Minimum Dynamic Input voltage, Manchester, NRZ or BPSK coded	106 to 848kbit/s			150	200	mVpp
$V_{RX,MaxIV,Mill}$	Maximum Dynamic Input voltage, All data coding	106kbit/s to 848kbit/s	[1]	AV_{DD}			Vpp

[1] It is therefore recommended to design the application so that RX voltage never exceeds AV_{DDmin} = 1.65V.

15.3.15 Output pin characteristics for TX1/TX2

Table 68. Output pin characteristics for TX1/TX2

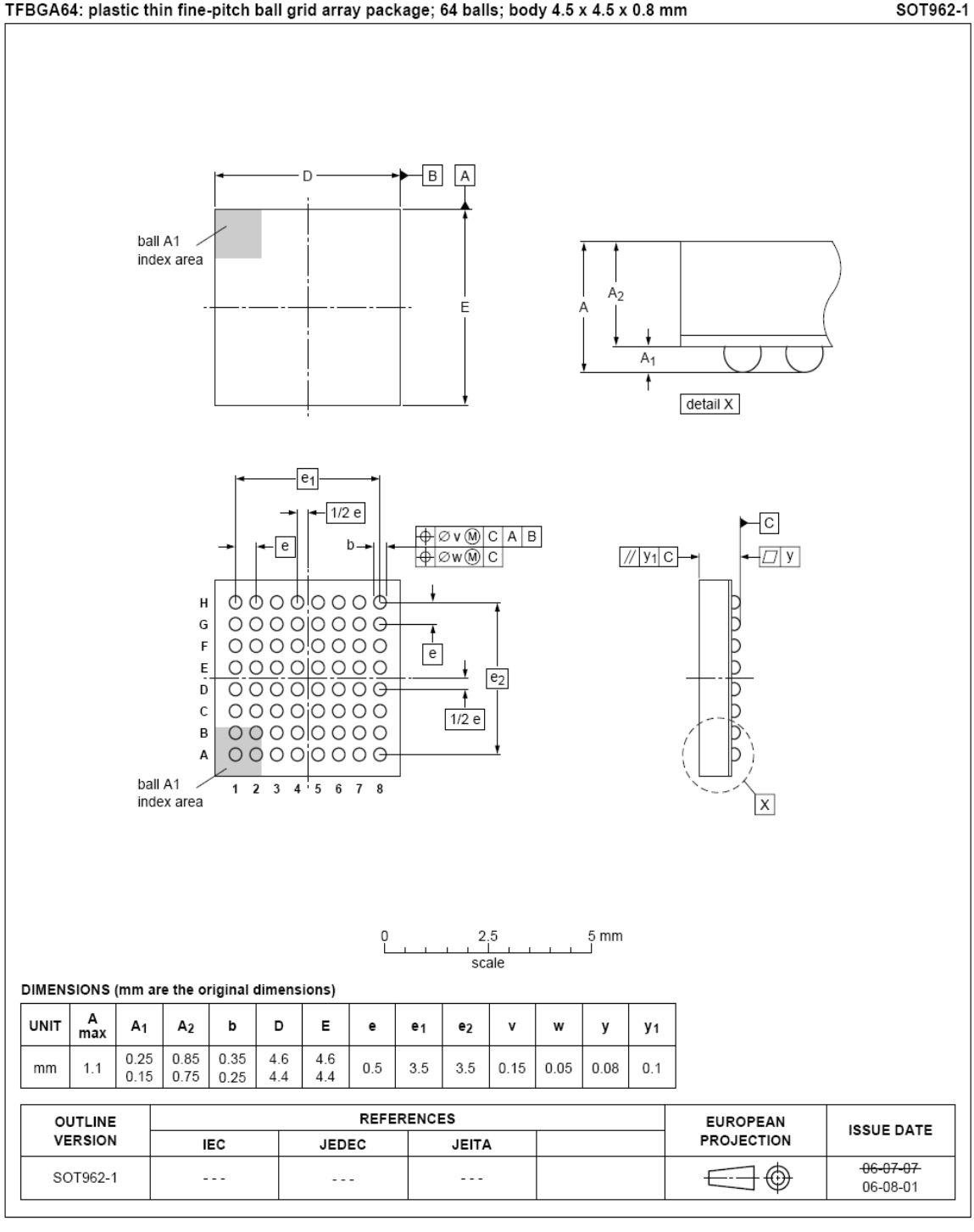
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	High level input current	V_I=TV_{DD} High Impedance			1	µA
I_{IL}	Low level input current	V_I=0V High Impedance	-1			µA
$V_{OH, C32, 3 V}$	High level output voltage	TV_{DD}=3V and I_{TX}=30mA, PMOS fully on	TV_{DD} - 150			mV
$V_{OL, C32, 3 V}$	Low level output voltage	TV_{DD}=3V and I_{TX}=30 mA, NMOS fully on			200	mV

Table 69. Output resistance for TX1/TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ON,10H}$	Low level output resistance	TV_{DD}=2.3V, V_{TX}=TV_{DD}-100mV, CWGsN=10h	45	54	70	Ω
$R_{ON,F0H}$	Low level output resistance	TV_{DD}=2.3V, V_{PX}=TV_{DD}-100mV, CWGsN=F0h	3.5	4.6	6	Ω
$R_{OP,01H}$	High level output resistance	TV_{DD}=2.3V, V_{TX}=TV_{DD}-100mV, CWGsP=01h	600	770	950	Ω
$R_{OP,FFH}$	High level output resistance	TV_{DD}=2.3V, V_{PX}=TV_{DD}-100mV, CWGsP=FFh	2.9	3.7	4.7	Ω
$R_{ON,10H}$	Low level output resistance	TV_{DD}=3V, V_{TX}=TV_{DD}-100mV, CWGsN=10h	40	47	60	Ω
$R_{ON,F0H}$	Low level output resistance	TV_{DD}=3 V, V_{TX}=TV_{DD}-100mV, CWGsN=F0h	3.2	4.2	5.5	Ω
$R_{OP,01H}$	High level output resistance	TV_{DD}=3V, V_{TX}=TV_{DD}-100mV, CWGsP=01h	480	600	740	Ω
$R_{OP,FFH}$	High level output resistance	TV_{DD}=3 V, V_{TX}=TV_{DD}-100mV, CWGsP=FFh	2.3	3	4	Ω
$R_{ON,10H}$	Low level output resistance	TV_{DD}=3.5 V, V_{TX}=TV_{DD}-100mV, CWGsN=10h	36	45	57	Ω
$R_{ON,F0H}$	Low level output resistance	TV_{DD}=3.5 V, V_{TX}=TV_{DD}-100 mV, CWGsN=F0h	3	4	5.2	Ω
$R_{OP,01H}$	High level output resistance	TV_{DD}=3.5 V, V_{TX}=TV_{DD}-100mV, CWGsP=01h	430	530	680	Ω
$R_{OP,FFH}$	High level output resistance	TV_{DD}=3.5 V, V_{TX}=TV_{DD}-100mV, CWGsP=FFh	2	2.8	3.6	Ω

16. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls; body 4.5 x 4.5 x 0.8 mm SOT962-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	4.6 4.4	4.6 4.4	0.5	3.5	3.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT962-1	---	---	---			~~06-07-07~~ 06-08-01

Fig 45. Package outline SOT962-1

17. Abbreviations

Table 70. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
Automatic anticollision	Detect and recognize requests from any NFC initiator or reader/writer device, like NFC-Target, ISO/IEC 14443, Type A PICC (identical to NFC -Target) or ISO/IEC 14443, Type B PICC
Automatic device discovery	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and UltraLight PICC, ISO/IEC 15693 VICC
Autonomous tag communication	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and UltraLight PICC, ISO/IEC 15693 VICC
Card emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller.
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
Loadmodulation Index	The load modulation index is defined as the card's voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) measured at the card's coil.
MISO	Master In Slave Out (for SPI interface)
Modulation Index	The modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin).
MOSI	Master Out Slave In (for SPI interface)
NFC-WI	Near Field Communication - Wired Interface
NSS	Not Slave Select (for SPI interface)
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE.
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE.
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification or MIFARE.
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE.
Powered-by-Field mode	A contactless device supports Powered-by-Field mode if it is capable of performing PICC emulation mode transactions while extracting the required power from the electromagnetic RF-field generated by a coupled PCD. Example: contactless plastic smart cards.
SCK	Serial Clock (for SPI interface)
SPI	Serial Peripheral Interface
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator).
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO/IEC 15693 specification.

18. References

[1] **ETSI SWP —** TS 102 613 V7.6.0

[2] **ETSI HCI —** TS 102622 V7.5.0

[3] **ISO/IEC 14443 —** parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: 2nd edition 2008 (15/07/2008)

[4] **ISO/IEC 28361 (NFC-WI) —** 1st edition, 01/10/2007

[5] **I²C Specification —** I²C Specification, Version 2.1, January 2000, http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

[6] **SPI —** Motorola de-facto standard described in Motorola 68HC11 datasheet

[7] **PN544 User Manual —** UM1450xx PN544

[8] **PN544 Hardware Design Guide —** AN1067xx PN544 Hardware Design Guide

[9] **PN544 Antenna Design Guide —** AN1457xx

[10] **PN544 RF setting Guide —** AN1659xx PN544 RF settings.pdf

[11] **ISO/IEC 18092 (NFC-IP1) —** 1st edition, 01/04/2004

[12] **ISO/IEC15693 —** part 2: 2nd edition (15/12/2006), part 3: 1st edition (01/04/2001)

19. Revision history

Table 71. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
155210	14 May 2008	Objective data sheet		
		Modifications:	• Initial version	
155220	21 October 2008	Objective data sheet		155210
		Modifications:		
155221	2 December 2008	Objective data sheet		155220
		Modifications:	• Rename of DCDC_VSS by VSS • Rename PWR_RFU by VBAT2. • ESD HBM update	
155222	3 March 2009	Objective data sheet		155221
		Modifications:	Update for A-gate	
155223	13 March 2009	Objective data sheet		155222
		Modifications:	Update for A-gate	
155224	17 July 2009	Objective data sheet		155223
		Modifications:	All pages	
155230	16 November 2009	Product data sheet		155224
		Modifications:	All pages	

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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22. Tables

Table 1. Quick reference data 3
Table 2. Ordering information 5
Table 3. Marking codes 5
Table 4. PN544 Pin description 7
Table 5. Host connection pins 9
Table 6. UICC connection pins 9
Table 7. SE connection pins via NFC-WI 9
Table 8. Antenna connection pins 10
Table 9. GPIO pins 10
Table 10. Configuration pins 10
Table 11. Default host pin state in standby mode. 14
Table 12. Default host pin state in Active R/W mode . . . 15
Table 13. Default host pin state in Active battery mode . . 16
Table 14. Host pin state in hard power-down mode 17
Table 15. Host pin state in monitor mode 18
Table 16. Host pin state in active antenna mode 19
Table 17. Interrupt sources. 21
Table 18. Pin configuration for HSU interface selection . . 22
Table 19. IF0-3 functionality for HSU interface. 22
Table 20. HSU interface baud rates 23
Table 21. Pin configuration for I^2C interface selection . . . 24
Table 22. IF0-3 functionality for I^2C interface 24
Table 23. Pin configuration for SPI interface selection . . . 25
Table 24. IF0-3 functionality for SPI interface 26
Table 25. IO pins 27
Table 26. Crystal requirements. 36
Table 27. SWP reference supplies 45
Table 28. Communication overview for ISO/IEC 14443A/MIFARE reader/writer 52
Table 29. Communication overview for FeliCa reader/writer 53
Table 30. Communication overview for ISO/IEC 14443B reader/writer 54
Table 31. Communication overview for ISO/IEC 15693 VCD 55
Table 32. Communication overview for NFC Active Communication mode. 57
Table 33. Communication overview for NFC Passive Communication mode. 58
Table 34. ISO/IEC 14443-A / MIFARE Card Operation mode 60
Table 35. ISO/IEC 14443 B Card Operation mode 60
Table 36. Limiting values (in accordance with the Absolute Maximum Rating System (IEC 60134)) 64
Table 37. Operating conditions. 64
Table 38. Thermal characteristics 65
Table 39. Current consumption characteristics 66
Table 40. Battery voltage monitor characteristics. 66
Table 41. AVDD and DVDD Power on reset thresholds characteristics. 66
Table 42. Electrical characteristics of UICC supply 67
Table 43. Reset timing 67
Table 44. Power-up timings 67
Table 45. Download mode timings 68
Table 46. Thermal threshold. 68
Table 47. I2C timings specification. 68
Table 48. SPI timings specification 69
Table 49. Input clock characteristics on XTAL1 when using FracNpll 70
Table 50. Pin characteristics for XTAL1 when FracNPLL input 70
Table 51. Pin characteristics for 27.12 MHz XTAL Oscillator 70
Table 52. VEN and VEN_MON input pin characteristics . 71
Table 53. Output pin characteristics for IRQ 71
Table 54. Pin characteristics for GPIO2 and GPIO4 72
Table 55. Pin characteristics for IFSEL0, IFSEL1, IFSEL2 . 72
Table 56. Pin characteristics for TEST1, TEST2, TEST3, TEST4 and TEST10. 72
Table 57. Pin characteristics for GPIO0, GPIO1, GPIO3, GPIO5, GPIO6, GPIO7, IF0, IF1 73
Table 58. Pin characteristics for IF2 and IF3 configured as I^2C pads 73
Table 59. Pin characteristics for IF2 and IF3 not used as I^2C pads 74
Table 60. Electrical characteristics of SWIO 74
Table 61. S1 waveform timings 75
Table 62. Electrical characteristics of ANT1 and ANT2 . . 76
Table 63. Output pin characteristics for EXT_SW_CTRL 76
Table 64. Input pin characteristics for SIGIN 76
Table 65. Output pin characteristics for SIGOUT 76
Table 66. Input pin characteristics for RX 77
Table 67. Output pin characteristics for TX1/TX2 77
Table 68. Output resistance for TX1/TX2 78
Table 69. Abbreviations 80
Table 70. Revision history 82

23. Figures

Fig 1. PN544 transmission modes 1
Fig 2. PN544 package marking 5
Fig 3. PN544 block diagram 6
Fig 4. Pinning of PN544 in TFBGA64 (SOT962-1) 7
Fig 5. Functional diagram when battery monitor is used 12
Fig 6. Functional diagram when no battery monitor. . . . 13
Fig 7. Open-drain 27
Fig 8. Input 28
Fig 9. Output 28
Fig 10. Pull-up 29
Fig 11. Pull-down 29
Fig 12. Extra pull-down 30
Fig 13. High Impedance (HiZ) 30
Fig 14. SWP state diagram 31
Fig 15. Communication flows supported by the NFC-WI interface 33
Fig 16. Signal shape for SIGOUT in NFC-WI mode 34
Fig 17. Signal shape for SIGIN in NFC-WI mode 34
Fig 18. System clock tree 35
Fig 19. 27.12 MHz crystal oscillator connection. 36
Fig 20. Input reference phase noise characteristics 37
Fig 21. Power sourcing (simplified) 39
Fig 22. PMU functional diagram 40
Fig 23. TV_{DD} offset enabled behavior 41
Fig 24. TV_{DD} offset disabled behavior 42
Fig 25. TXLDO limiter without overcurrent interrupt enabled 42
Fig 26. SIMVCC versus PMUVCC. 43
Fig 27. UICC supply functional diagram 44
Fig 28. Battery voltage monitor principle 46
Fig 29. Resetting PN544 via VEN pin 48
Fig 30. VBAT is set-up before PVDD. 49
Fig 31. PVDD is set-up before VBAT. 49
Fig 32. PVDD is set-up or cut after PN544 has been enabled 50
Fig 33. PN544 download mode sequence. 50
Fig 34. ISO/IEC 14443A/MIFARE Reader/Writer mode communication diagram. 52
Fig 35. FeliCa reader/writer Communication Diagram. . . 53
Fig 36. ISO/IEC 14443B reader/writer communication diagram 54
Fig 37. ISO/IEC 15693 VCD mode communication diagram 55
Fig 38. NFCIP-1 mode. 56
Fig 39. Active NFC mode. 57
Fig 40. Passive NFC mode 58
Fig 41. Application schematic 1 62
Fig 42. Application schematic 2 63
Fig 43. I2C timings. 68
Fig 44. SPI timing diagram 69
Fig 45. Package outline SOT962-1 79

24. Contents

1 Introduction 1
2 General description 1
3 Features 2
4 Applications 3
5 Quick reference data 3
6 Ordering information 5
7 Marking 5
8 Block diagram 6
9 Pinning information 7
9.1 Pinning 7
9.2 Pin description 9
10 Functional description 11
10.1 Functional / Power states of PN544 12
10.1.1 Standby mode 14
10.1.2 Active R/W mode 15
10.1.3 Active battery mode 16
10.1.4 Polling loop 16
10.1.5 Hard power down (HPD) mode 17
10.1.6 Monitor mode 18
10.1.7 Active antenna mode (Powered-by-Field) . . . 19
10.2 Microcontroller HT80C51MX 20
10.2.1 PN544 memory management 20
10.2.2 Timer0/1 description 21
10.2.3 Interrupts management 21
10.2.4 FW architecture 21
10.3 Host interfaces 22
10.3.1 High Speed UART (HSU) Interface 22
10.3.2 I²C interface 23
10.3.2.1 I²C configuration options 23
10.3.2.2 I²C functional description 25
10.3.3 Serial Peripheral Interface 25
10.3.3.1 Features 25
10.3.3.2 SPI configuration options 25
10.3.3.3 SPI functional description 26
10.3.4 IOs configuration 27
10.3.4.1 Pad configuration description 27
10.4 Secure Element interfaces 31
10.4.1 SWP interface 31
10.4.1.1 SWP parameters 32
10.4.1.2 SWP test signals 32
10.4.2 NFC-WI interface support 33
10.5 PN544 clock concept 35
10.5.1 27.12 MHz quartz oscillator 36
10.5.2 Integrated FracNpll to make use of external clock 37
10.5.3 Low power 20MHz oscillator 37
10.5.4 Low power 333kHz oscillator 38
10.6 Power concept 39
10.6.1 PN544 core supply sources 39
10.6.2 PMU functional description 39
10.6.3 DSLDO: Dual Supply LDO 40
10.6.4 TXLDO 40
10.6.4.1 TXLDO limiter 42
10.6.5 Secure Element supply 43
10.6.6 UICC supply 43
10.6.7 Battery voltage monitor 46
10.6.8 Powered-by-Field mode (PbF) 47
10.6.9 Thermal protection 47
10.7 Reset and download concept 48
10.7.1 Resetting PN544 48
10.7.2 Power-up sequences 49
10.7.2.1 VBAT is set-up before PVDD 49
10.7.2.2 PVDD is set-up before VBAT 49
10.7.2.3 PN544 has been enabled before PVDD is set or before PVDD has been cut 50
10.7.3 Download mode 50
10.8 Contactless interface Unit 51
10.8.1 Reader/Writer modes 51
10.8.1.1 ISO/IEC 14443-A/MIFARE and JEWEL/TOPAZ PCD mode 52
10.8.1.2 FeliCa PCD mode 53
10.8.1.3 ISO/IEC 14443B PCD mode 54
10.8.1.4 ISO/IEC 15693 VCD mode 55
10.8.2 ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode 56
10.8.2.1 ACTIVE Communication mode 57
10.8.2.2 PASSIVE Communication mode 58
10.8.2.3 NFCIP-1 framing and coding 59
10.8.2.4 NFCIP-1 protocol support 59
10.8.3 Card Operation mode 60
10.8.3.1 ISO/IEC 14443-A / MIFARE Card Operation mode 60
10.8.3.2 ISO/IEC 14443 B and B' Card Operation mode . . 60
10.8.4 Frequency inter operability 61
10.9 Support for production test and implementation . 61
11 Application design-in information 62
12 Limiting values 64
13 Recommended operating conditions 64
14 Thermal characteristics 65
15 Characteristics 66
15.1 Current consumption characteristics 66

continued >>

15.2 Functional block electrical characteristics. . . . 66
15.2.1 Battery voltage monitor characteristics. 66
15.2.2 AVDD and DVDD reset thresholds 66
15.2.3 UICC supply characteristics 67
15.2.4 Reset via VEN 67
15.2.5 Power-up timings 67
15.2.6 Download mode timings 68
15.2.7 Thermal protection 68
15.2.8 I2C timings 68
15.2.9 SPI timings 69
15.3 Pin characteristics 70
15.3.1 XTAL pin characteristics (XTAL1, XTAL2) . . . 70
15.3.2 VEN and VEN_MON input pin characteristics 71
15.3.3 Output pin characteristics for IRQ. 71
15.3.4 Pin characteristics for GPIO2 and GPIO4 . . . 72
15.3.5 Pin characteristics for IFSELs. 72
15.3.6 Pin characteristics for TEST1, TEST2, TEST3, TEST4 and TEST10 72
15.3.7 Pin characteristics for GPIOs, IF0 and IF1 . . . 73
15.3.8 Pin characteristics for IF2, IF3 73
15.3.9 SWIO pin characteristics 74
15.3.10 ANT1 and ANT2 pin characteristics 76
15.3.11 Output pin characteristics for EXT_SW_CTRL 76
15.3.12 Input pin characteristics for SIGIN 76
15.3.13 Output pin characteristics for SIGOUT 76
15.3.14 Input pin characteristics for RX. 77
15.3.15 Output pin characteristics for TX1/TX2. 77
16 Package outline 79
17 Abbreviations. 80
18 References 81
19 Revision history. 82
20 Legal information. 83
20.1 Data sheet status 83
20.2 Definitions. 83
20.3 Disclaimers 83
20.4 Licenses 84
20.5 Patents 84
20.6 Trademarks. 84
21 Contact information. 84
22 Tables 85
23 Figures 86
24 Contents 87

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