TLE4209G

Automotive Power



TLE4209G



Table of Contents

Table of Contents

1	Overview 3
2	Block Diagram
3 3.1 3.2	Pin Configuration5Pin Assignment5Pin Definitions and Functions5
4.1 4.2 4.3 4.4	General Product Characteristics6Absolute Maximum Ratings6Operating Range6Thermal Resistance7Electrical Characteristics7
5	Application Information
6	Package Outlines
7	Revision History



0.8A DC Motor Driver for Servo Driver Applications

TLE4209G





1 Overview

Features

- · Optimized for manual headlight beam control applications
- Delivers up to 0.7 A continuous
- Low saturation voltage; typ.1.6 V total @ 25 °C; 0.7 A
- · Output protected against short circuit
- Over temperature protection with hysteresis
- · Over- and under voltage lockout
- Internal clamp diodes
- Enhanced SMD power package
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-14-22

Description

The TLE4209G is a protected H-Bridge Driver designed specifically for automotive manual headlight beam control and industrial servo control applications with DC-brush motor loads.

The part is built using the bipolar high voltage power technology DOPL.

The standard enhanced power PG-DSO-14-22 package meets the application requirements and saves PCB-board space and costs. The package is lead- and halogen-free.

The servo-loop-parameter pos.- and neg. Hysteresis, pos.- and neg. deadband and angle-amplification are programmable with external resistors.

An internal window-comparator controls the input line. In the case of a fault condition, like short circuit to GND, short circuit to supply-voltage, and broken wire, the TLE4209G stops the motor immediately (brake condition).

Furthermore the built in features like over- and under voltage-lockout, short-circuit-protection and over-temperature-protection will open a wide range of automotive- and industrial applications.

Туре	Package	Marking
TLE4209G	PG-DSO-14-22	TLE4209G

Data Sheet 3 Rev. 1.3, 2008-02-04



Block Diagram

2 Block Diagram

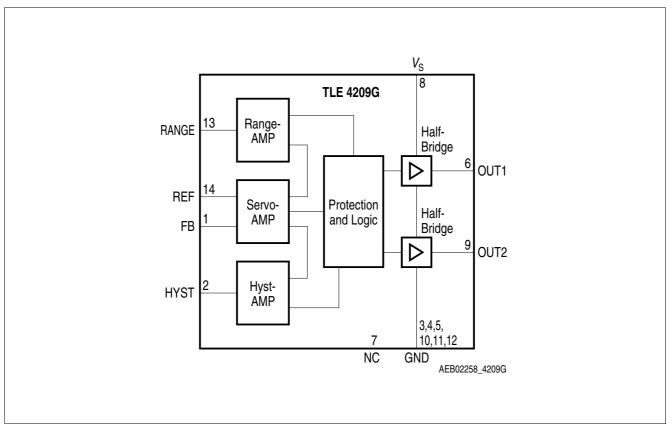


Figure 1 Block Diagram



Pin Configuration

3 Pin Configuration

3.1 Pin Assignment

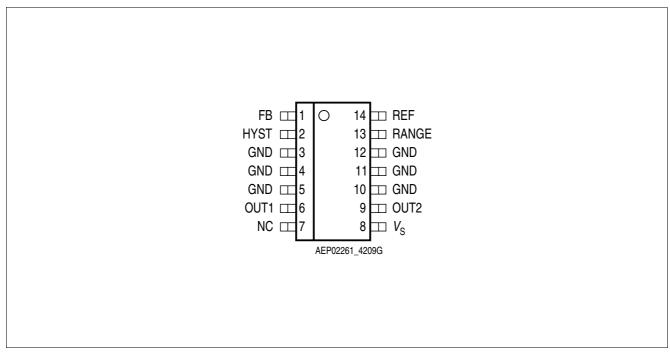


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	FB	Feedback Input
2	HYST	Hysteresis I/O
3, 4, 5,	GND	Ground
10, 11,		
12		
6	OUT1	Power Output 1
7	NC	Not Connected
8	V_{S}	Power Supply Voltage
9	OUT2	Power Output 2
13	RANGE	Range Input
14	REF	Reference Input



4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings 1)

 $T_{\rm j}$ = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Lin	nit Values	Unit	Conditions	
			Min.	Max.			
Voltage	es	+		<u> </u>	l .	+	
4.1.1	Supply voltage	V_{S}	-0.3	45	V	_	
4.1.2	Supply voltage	V_{S}	-1	-	V	t < 0.5 s; $I_{\text{S}} > -2 \text{ A}$	
4.1.3	Logic input voltages (FB, REF, RANGE, HYST)	V_1	-0.3	20	V	_	
Curren	ts	1				1	
4.1.4	Output current (OUT1, OUT2)	I_{OUT}	_	_	Α	internally limited	
4.1.5	Output current (Diode)	I_{OUT}	-0.9	0.9	Α	_	
4.1.6	Input current (FB, REF, RANGE, HYST)	I_{IN}	-2 -6	2 6	mA mA	t < 2 ms; t/T < 0.	
Tempe	ratures	1	*	<u> </u>			
4.1.7	Junction temperature	T_{j}	-40	150	°C	_	
4.1.8	Storage temperature	T_{stg}	-50	150	°C	_	

¹⁾ Not subject to production test, specified by design.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Operating Range

Pos.	Parameter	Symbol	Liı	nit Values	Unit	Conditions	
			Min.	Max.			
4.2.1	Supply voltage	V_{S}	8	18	V	After $V_{\rm S}$ rising above $V_{\rm UVON}$	
4.2.2	Supply voltage increasing	V_{S}	-0.3	V_{UVON}	V	Outputs in tristate	
4.2.3	Supply voltage decreasing	V_{S}	-0.3	V_{UVOFF}	V	Outputs in tristate	
4.2.4	Output current	I_{OUT1-2}	-0.7	0.7	Α	_	
4.2.5	Input current (FB, REF)	I_{IN}	-50	500	μΑ	_	
4.2.6	Junction temperature	T_{j}	-40	150	°C	_	

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.



4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Pos.	Parameter	Symbol		Limit Val	ues	Unit	Conditions	
			Min.	Тур.	Max.			
4.3.1	Junction to Soldeering Point ¹⁾	R_{thJSP}	_	_	25	K/W	measured to pin 5	
4.3.2	Junction to Ambient ¹⁾ minimal-footprint	R_{thJA}	-	130	-	K/W	2)	
4.3.3	Junction to Ambient ¹⁾ additional 600 mm ² CU area	R_{thJA}	_	65	-	K/W	3)	

¹⁾ Not subject to production test, specified by design.

4.4 Electrical Characteristics

Electrical Characteristics

 $V_{\rm S}$ = 8 V to 18 V, $T_{\rm j}$ = -40 °C to +150 °C, $I_{\rm OUT1-2}$ = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions	
			Min.	Тур.	Max.			
Curren	t Consumption			-	-			
4.4.1	Supply current	I_{S}	_	12	20	mA	_	
4.4.2	Supply current	I_{S}	_	20	30	mA	$I_{\rm OUT1}$ = 0.3 A $I_{\rm OUT2}$ = -0.3 A	
4.4.3	Supply current	I_{S}	_	30	50	mA	$I_{\text{OUT1}} = 0.7 \text{ A}$ $I_{\text{OUT2}} = -0.7 \text{ A}$	
Over- a	and Under Voltage Lockout		•					
4.4.4	UV Switch ON voltage	V_{UVON}	_	7.4	8	V	$V_{\rm S}$ increasing	
4.4.5	UV Switch OFF voltage	V_{UVOFF}	6.3	6.9	_	V	$V_{\rm S}$ decreasing	
4.4.6	UV ON/OFF Hysteresis	V_{UVHY}	_	0.5	_	V	V _{UV ON} - V _{UV OFF}	
4.4.7	OV Switch OFF voltage	V_{OVOFF}	_	20.5	23	V	$V_{\rm S}$ increasing	
4.4.8	OV Switch ON voltage	V_{OVON}	17.5	20	_	V	$V_{\rm S}$ decreasing	
4.4.9	OV ON/OFF Hysteresis	V_{OVHY}	_	0.5	_	V	$V_{ m OVOFF}$ - $V_{ m OVON}$	
Output	s OUT1-2, Saturation Voltaç							
4.4.10	Source (upper) I_{OUT} = -0.3 A	V_{SATU}	_	0.90	1.20	V	T _j = 25 °C	
4.4.11	Sink (upper) I_{OUT} = -0.7 A	V _{SAT U}	_	1.10	1.50	V	<i>T</i> _j = 25 °C	
4.4.12	Sink (lower) $I_{\text{OUT}} = 0.3 \text{ A}$	V _{SAT L}	_	0.25	0.40	V	<i>T</i> _j = 25 °C	
4.4.13	Sink (lower) $I_{\text{OUT}} = 0.7 \text{ A}$	V _{SAT L}	_	0.45	0.75	V	<i>T</i> _j = 25 °C	

²⁾ JESD 51-2, 51-3, FR4 76.2 mm \times 114.3 mm \times 1.5 mm, 70 μ m Cu, minimal footprint

³⁾ JESD 51-2, 51-3, FR4 76.2 mm \times 114.3 mm \times 1.5 mm, 70 μm Cu, 600 mm 2 CU cooling area connected to Pins: 3, 4, 5, 10, 11, 12



Electrical Characteristics (cont'd)

 $V_{\rm S}$ = 8 V to 18 V, $T_{\rm j}$ = -40 °C to +150 °C, $I_{\rm OUT1-2}$ = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions	
			Min.	Тур.	Max.			
4.4.14	Total drop $I_{\text{OUT}} = 0.3 \text{ A}$	V_{SAT}	_	1.2	1.7	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$	
4.4.15	Total drop I_{OUT} = 0.7 A	V_{SAT}	-	1.6	2.5	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$	
Output	s OUT1-2, Clamp Diodes			"	II.	"		
4.4.16	Forward voltage; upper	V_{FU}	_	1	1.5	V	$I_{\rm F}$ = 0.3 A	
4.4.17	Upper leakage current	I_{LKU}	-	_	5	mA	$I_{\rm F}$ = 0.3 A	
4.4.18	Forward voltage; lower	V_{FL}	_	0.9	1.4	V	$I_{\rm F}$ = 0.3 A	
Input-Ir	nterface, Input REF				"		<u>'</u>	
4.4.19	Quiescent voltage	V_{REFq}	_	200	_	mV	I_{REF} = 0 μA	
4.4.20	Input resistance	R_{REF}	_	6	_	kΩ	0 V < V _{REF} < 0.5 V	
Input-Ir	nterface, Input FB				"		"	
4.4.21	Quiescent voltage	V_{FBq}	_	200	_	mV	I_{FB} = 0 μ A	
4.4.22	Input resistance	R_{FB}	_	6	_	kΩ	$0 \text{ V} < V_{\text{FB}} < 0.5 \text{ V}$	
Input-Ir	nterface, Input/Output HYST				"			
4.4.23	Current Amplification $A_{\rm HYST}$ = $I_{\rm HYST}$ / ($I_{\rm REF}$ - $I_{\rm FB}$)	A_{HYST}	0.8	0.95	1.1	-	-20 μA < $I_{\rm HYST}$ < -10 μA; 10 μA < $I_{\rm HYST}$ < 20 μA; $I_{\rm REF}$ = 250 μA; $V_{\rm HYST}$ = $V_{\rm S}$ / 2	
4.4.24	Current Offset	I_{HYSTIO}	-2	0.35	3	μΑ	I_{REF} = I_{FB} = 250 μA ; V_{HYST} = V_{S} / 2	
4.4.25	Threshold voltage High	V_{HYH} / V_{S}	-	52	_	%	_	
4.4.26	Deadband voltage High	$V_{ m DBH}$ / $V_{ m S}$	_	50.4	_	%	_	
4.4.27	Deadband voltage Low	V_{DBL} / V_{S}	_	49.6	_	%	_	
4.4.28	Threshold voltage Low	V_{HYL} / V_{S}	_	48	_	%	_	
4.4.29	Hysteresis Window	V _{HYW} / V _S	3	4	5	%	$(V_{ m HYH}$ - $V_{ m HYL})$ / $V_{ m S}$	
4.4.30	Deadband Window	V_{DBW} / V_{S}	0.4	0.8	1.2	%	$(V_{\mathrm{DBH}}$ - $V_{\mathrm{DBL}})$ / V_{S}	
Input-Ir	nterface, Input RANGE	·		·	·			
4.4.31	Input current	I_{RANGE}	-1	_	1	μΑ	$0 \text{ V} < V_{\text{RANGE}} < V_{\text{S}}$	
4.4.32	Switch-OFF voltage High	V_{OFFH}	-25	0	100	mV	refer to $V_{\rm S}$	
4.4.33	Switch-OFF voltage Low	V_{OFFL}	300	400	500	mV	refer to GND	



Electrical Characteristics (cont'd)

 $V_{\rm S}$ = 8 V to 18 V, $T_{\rm j}$ = -40 °C to +150 °C, $I_{\rm OUT1-2}$ = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol		Limit Val	ues	Unit	Conditions
			Min.	Тур.	Max.		
Therma	al Shutdown			1		1	
4.4.34	Thermal shutdown junction temperature ¹⁾	T_{jSD}	150	175	200	°C	_
4.4.35	Thermal switch-on junction temperature ¹⁾	T_{jSO}	120	_	170	°C	_
4.4.36	Temperature hysteresis	ΔT	_	30	_	K	_

¹⁾ Not subject to production test, specified by design.

Data Sheet 9 Rev. 1.3, 2008-02-04



Application Information

5 Application Information

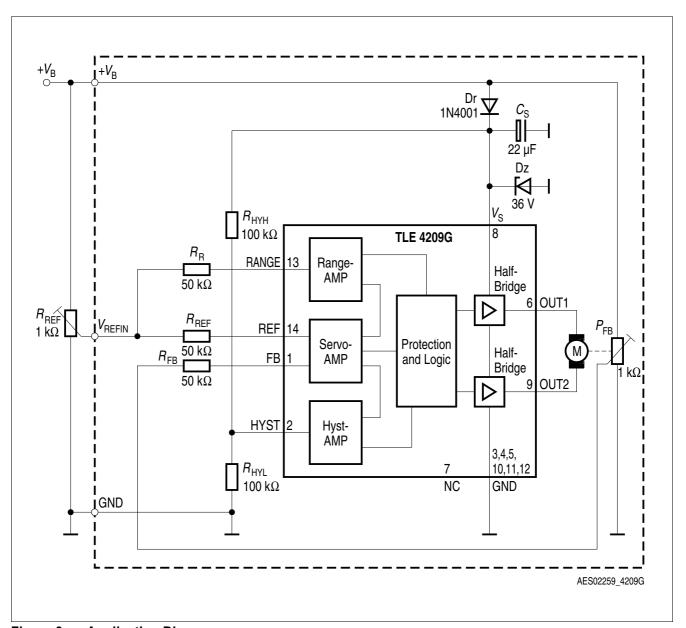


Figure 3 Application Diagram

Note: In the application the PIN 7 can remain not connected.



Application Information

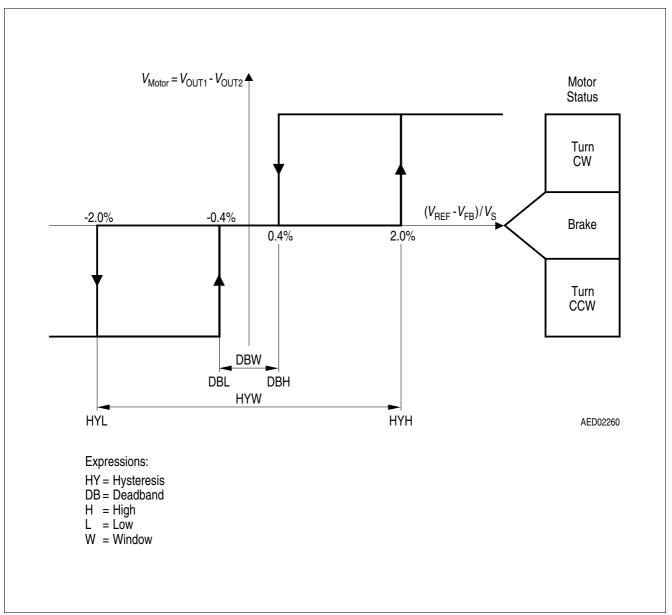


Figure 4 Hysteresis, Phaselag and Deadband-Definitions



Application Information

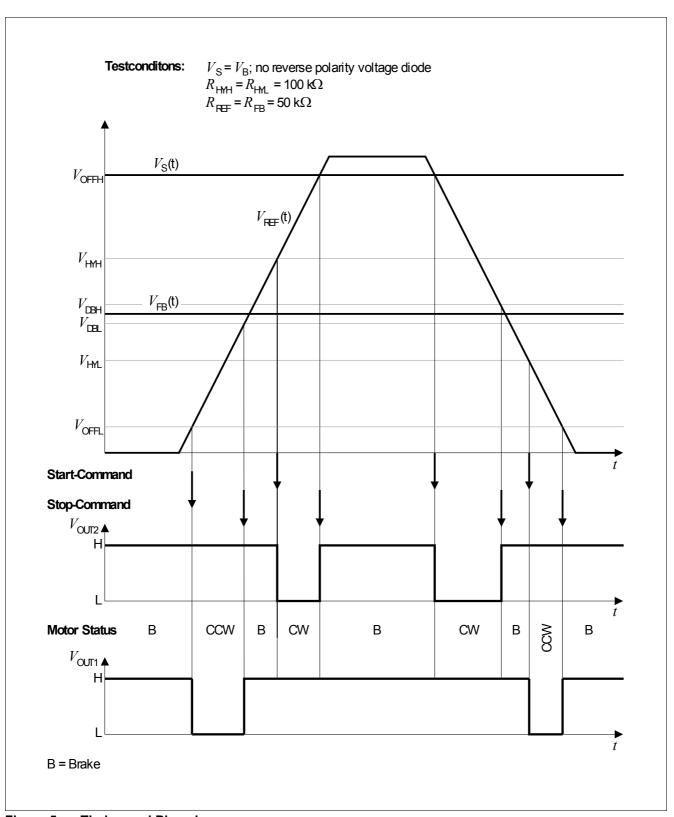


Figure 5 Timing and Phaselag



Package Outlines

6 Package Outlines

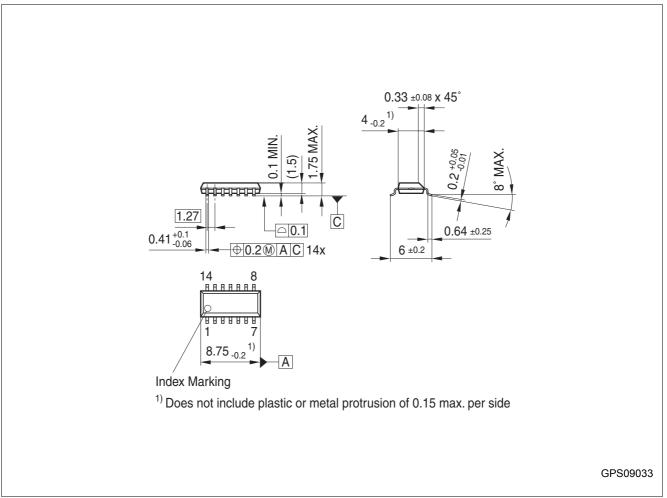


Figure 6 PG-DSO-14-22 (Plastic Green - Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).



Revision History

7 Revision History

Revision	Date	Changes
1.1	2007-04-11	RoHS-compliant DSO package version of the TLE 4209
		All pages: Infineon logo updated
		Page 1:
		"AEC qualified" and "RoHS" logo added, "Green Product (RoHS compliant)" and
		"AEC qualified" statement added to feature list, package names changed to
		RoHS compliant versions, package pictures updated
		Page 13:
		Package names changed to RoHS compliant versions, "Green Product"
		description added
		Revision History added
		Legal Disclaimer added
1.2	2007-08-10	Package name changed to PG-DSO-14-22
1.3	2008-02-04	Page 1: Editorial change: deleted "fully" (The term "fully protected" often leads to misunderstandings as it is unclear with respect to which parameters).

Edition 2008-02-04

Published by Infineon Technologies AG 81726 Munich, Germany © 2008 Infineon Technologies AG All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.