Optional Homework 1

Design of a sequential circuit

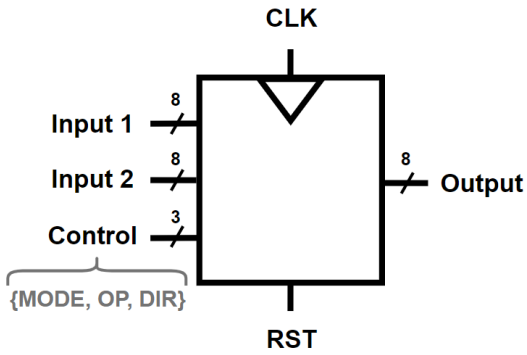
The aim of this homework is to understand the basics of SystemVerilog and to simulate the operation of a sequential circuit using ModelSim. The code is verified using the Inginious platform. The grading system (3 free attempts, then a 10% penalty) is similar to what you will have in the midterm evaluation.

Here is the **functional description** of the circuit to be implemented. An illustration of the circuit with its inputs and outputs is given in Figure 1.

- **Inputs:** Input 1 [7:0], Input 2 [7:0], CLK, RST, Control [2:0].
- **Output:** Output [7:0].
- **Function:** The circuit's Output [7:0] is re-evaluated on each rising edge of the CLK clock signal. The circuit has two modes: (1) a calculation mode and (2) a rotation mode. The circuit mode is determined by the most significant bit (MSB) of the Control signal `MODE`: a logic 1 corresponds to the calculation mode, a 0 corresponds to the rotation mode. If the second bit of the Control signal `OP` is a logic 1, the operation performed between the two inputs is an addition; otherwise, it is a subtraction. The least significant bit (LSB) of the Control signal `DIR` determines the direction in the rotation mode: a logic 1 shifts the bits of the Output signal to the left, while a logic 0 shifts them to the right. An example of rotation to the left on an 8-bit binary word is shown in Figure 2. Whenever the `RST` reset signal is activated, the output is reset to zero on the rising edge of the RST signal. This means that this reset is asynchronous.

Before submitting to Inginious :

1. Test your implementation as you learned it in the lab, using a testbench.
2. Check that the name of your module in your .sv file matches the module description on Inginious. Your module must be called module `Homework_1 (CLK, RST, Input_1, Input_2, Control, Output);`.



(a) Your circuit at the functional block level.

0	0	0	**1**	**1**	**1**	0	0
0	0	**1**	**1**	**1**	0	0	0
0	**1**	**1**	**1**	0	0	0	0
1	**1**	**1**	0	0	0	0	0
1	**1**	0	0	0	0	0	**1**
1	0	0	0	0	0	**1**	**1**

(b) Illustration of the rotation function to the left