

Generalized Predictive dc-Link Voltage Control for Grid-Connected Converter

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Abstract—The main function of the grid-connected converter in many applications is to control the dc-link voltage with high performance, i.e., strong disturbance rejection capability and good dynamic response. Take the grid-connected pulsedwidth modulation (PWM) rectifier of a motor drive system as an example, good disturbance rejection capability is essential for the dc-link voltage control to address the varying loads on the motor side, and the dynamic process of the dc-link voltage control is preferred to be fast and overshoot-free, so as to adaptively adjust the dc-link voltage according to the motor speed and reduce the switching losses. However, the performance of the conventional proportional-integral (PI)-based dc-link voltage control is not always satisfying and can be further improved. In this article, the generalized predictive control (GPC) method is applied to the dc-link voltage control of a grid-connected converter for the first time, which can provide both good disturbance rejection capability and satisfying dynamic performance. Moreover, stability analysis of the proposed GPC-based dc-link voltage control strategy is theoretically studied, and a parameter tuning guideline is provided. The effectiveness and advantages of the proposed method are validated with experimental results.

Index Terms—dc-link voltage, generalized predictive control (GPC), Grid-connected converter.

I. INTRODUCTION

DC-LINK voltage control is essential for many power electronic devices, such as pulsedwidth modulation (PWM) rectifiers [1], renewable power generation systems [2], high voltage direct current (HVDC) transmission systems [3], [4], etc. In most conditions, the dc-link voltage is controlled by the grid-connected converter, which is usually a three-phase voltage source converter (VSC).

For most applications, the common targets for the dc-link voltage control are strong disturbance rejection capability and good dynamic performance. On the one hand, disturbances in both the grid and the load should be well rejected, otherwise overvoltage or over-modulation problems may occur

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when the dc-link voltage fluctuates too much. On the other hand, the dc-link voltage needs to be frequently adjusted in many applications. Thus, the high-performance dc-link voltage control should have the following three features: the fast step response, the slight/no overshoot, the mild and short transient processes when facing disturbances. For example, in single-stage PV systems, the dc-link voltage is adjusted by the grid-connected converter to achieve the maximal power point tracking (MPPT) [5]. In wind power generation systems based on permanent magnet synchronous generator (PMSG), the dc-link voltage is adjusted by the grid-connected converter to ensure a high dc-link voltage utilization ratio at different rotor speeds, so as to reduce the inverter loss [6]. Similar concepts are applied to two-stage PV systems [7] and permanent magnet motor drive systems [8]. In multiterminal VSC-HVDC transmission systems with droop control, the local dc-link voltage of each VSC is adjusted according to its output power [9]. In addition, a novel virtual synchronous generator (VSG) concept proposed in [10] also requires fast dc-link voltage control. All the applications in [5]–[10] share the same control structure for the dc-link voltage control, only with different power flow directions. The disturbance rejection capability and the dynamic response should be mainly considered when designing the dc-link voltage controller.

The conventional dc-link voltage control for grid-connected converter is based on the cascaded proportional-integral (PI) controllers [3], [4], [11]. The outer PI controller takes the dc-link voltage as the input, and produces the current reference, which is then tracked by the inner PI controllers. However, the integral process of PI controller inherently limits the disturbance rejection capability and dynamic response speed. To achieve better dc-link voltage control performance, some novel control methods can be applied. In [12], a fuzzy logic controller is used in the outer loop to improve the disturbance rejection capability of the dc-link voltage control, but only the wind speed disturbance is considered, and the dynamic performance and experimental results are absent. In [13], a deadbeat predictive dc-link voltage control method is proposed for the dynamic performance and disturbance rejection capability improvements, but the dc load current sensor is required. To avoid the dc load sensor, reference [1] proposes an improved deadbeat predictive dc-link voltage control method by using a dc load power estimator, but this extra estimator is still undesired in practical systems due to its limited accuracy in dynamic processes. Meanwhile, the fixed-step gradually approaching manner used in [1] makes the dc-link voltage control rigid, since all the different transient processes are forced to last the same duration.

In recent years, model predictive control (MPC), as a novel high-performance control method, has been widely applied to power electronic devices, which shows significant advantages in both disturbance rejection capability and dynamic performance [14]–[27]. In [19] and [20], the finite-control-set MPC (FCS-MPC) is applied to the grid-connected converter, which yields good results. However, they both focus on the power control, rather than the dc-link voltage control. In [21] and [22], the FCS-MPC method is applied to the grid-connected converter, to control both the dc-link voltage and the active and reactive powers with a noncascaded control loop. However, the FCS-MPC used in [21] and [22] have unfixed switching frequency (note that FCS-MPC with fixed switching frequency can be achieved [25], [27], but that for dc-link voltage control is not reported yet) and the high-frequency ripple, and an extra integrator is required to correct the steady-state bias caused by the inevitable parameter mismatch, which can potentially weaken the disturbance rejection capability and dynamic performance. Meanwhile, the prediction horizon of FCS-MPC is only one single step, and can hardly be extended, for the exponentially increasing computation burden when searching for the globally optimized solution. Considering that the dc-link voltage loop has relatively larger time constant compared with the inner ac current loops, especially for applications with large dc capacitors, long prediction horizon is beneficial or even necessary for the dc-link voltage control. This claim will be theoretically validated in this article. Moreover, the fixed-step gradually approaching manner similar as [1] is utilized in [21] and [22], which is undesired.

Generalized predictive control (GPC) is another MPC type, which inherits the good disturbance rejection capability and dynamic performance of the MPC family, as well as other good features including fixed switching frequency, small high-frequency ripple, and no static error even with parameter mismatch [28]–[30]. More importantly, GPC is quite suitable for long-horizon prediction. Thus, GPC is more effective for the control of relatively slow dynamics. In this article, GPC is applied to the dc-link voltage control of a grid-connected converter for the first time, which utilizes a cascaded structure, and both the outer dc-link voltage control loop and the inner current control loop are based on GPC. It should be noted that conventional PI control can still be utilized for the inner current control loop (GPC+PI cascaded structure), but the GPC-based inner current control loop is likely to provide better rejection capability to the grid voltage harmonics [14]–[18], since the wider control bandwidth is more likely to be achieved by GPC for the absence of the stability-related compromises in the tuning stage [31], as well as the mature delay compensation methods [32]. The proposed method can be applied to many applications that require high-performance dc-link voltage control.

Meanwhile, the transfer functions of the GPC controlled system are derived, based on which the stability analysis, disturbance rejection capability, and parameter tuning are studied in detail. These works are significant considering that the performance valuation and parameter tuning of GPC have long been tricky problems without systematic solutions available in published papers.

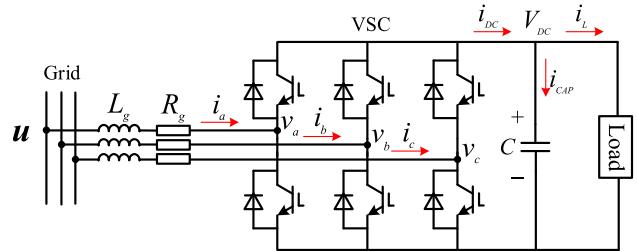


Fig. 1. Topology of grid-connected converter.

The novelties and contributions of this article are as follows.

- 1) The first time to apply GPC to the dc-link voltage control of a three-phase converter, which achieves satisfying performance.
- 2) The first time to systematically analyze the stability and disturbance rejection capability of a GPC controlled system based on transfer functions.
- 3) The impacts of parameter mismatch on both the system stability and disturbance rejection capability are theoretically analyzed and experimentally tested.
- 4) A tuning guideline of GPC is proposed, which can benefit not only the application of this article, but also any other GPC applications.

It should be noted that the plant focused in this article is a grid-connected PWM rectifier with dc load, whose control structure can be easily applied to other applications in [5]–[10]. This article is organized as follows: first, the mathematical model of the grid-connected converter is presented, based on which the prediction model of both the dc-link voltage and the ac current are derived. Then, the proposed control structure and the GPC controller design are introduced in detail. Afterward, the stability analysis, disturbance rejection capability analysis, and a guideline for parameter tuning are presented. Finally, the effectiveness and advantages of the proposed method are validated by experimental results.

II. MATHEMATICAL MODEL

The grid-connected converter studied in this article is shown in Fig. 1. When applying the motor configuration, the dc-link voltage dynamic can be expressed as

$$\frac{dV_{DC}}{dt} = \frac{i_{DC} - i_L}{C} \quad (1)$$

where V and i represent the voltage and the current, respectively. The subscripts dc and L represent the variables of the dc bus and the load, respectively. C is the capacitance of the dc capacitor.

For the convenience of GPC design, the discrete prediction equation in increment form can be derived from (1)

$$\Delta V_{DC}(k+1) = \Delta V_{DC}(k) + \Delta i_{DC}(k)T_s/C - \Delta i_L(k)T_s/C \quad (2)$$

where Δ represents the incremental variables. T_s is the sampling period of the controller. k represents the current instant in a discrete-time sequence. Here, the incremental dc load current can be ignored since the dc load can be considered as a disturbance when designing the GPC controller.

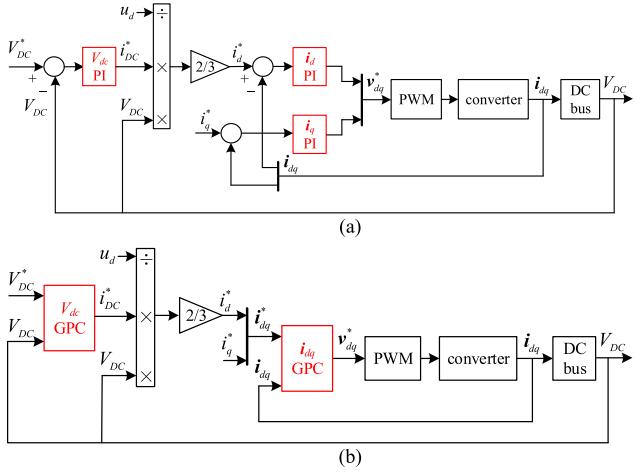


Fig. 2. General structure of dc-link voltage control. (a) Conventional PI-based dc-link voltage control. (b) Proposed GPC-based dc-link voltage control.

On the ac side, the current dynamics can be expressed as

$$\frac{d}{dt} \mathbf{i}_{dq} = \frac{\mathbf{u}_{dq}}{L_g} - \frac{\mathbf{v}_{dq}}{L_g} - \frac{R_g}{L_g} \mathbf{i}_{dq} - j\omega_1 \mathbf{i}_{dq} \quad (3)$$

where \mathbf{u} represents the grid voltage and \mathbf{v} is the voltage modulated by the VSC. The subscript dq represents the d - q synchronous rotating frame. ω_1 is the angular velocity of the grid voltage.

Considering that L_g and R_g are usually not large, in steady states, the power balance between the dc side and the ac side can be expressed as

$$V_{DC} i_{DC} = \frac{3}{2} (v_d i_d + v_q i_q) \approx \frac{3}{2} (u_d i_d + u_q i_q). \quad (4)$$

The equations above are the basis of the implementation of the GPC-based dc-link voltage control to be proposed.

III. PROPOSED GPC-BASED DC-LINK VOLTAGE CONTROL AND IMPLEMENTATION

In this section, the proposed GPC-based dc-link voltage control strategy, including both the dc-link voltage control loop and the three-phase current control loop, is introduced in detail.

A. General Structure Introduction

The general structures of the conventional PI-based and the proposed GPC-based dc-link voltage control strategies are shown in Fig. 2. It can be observed that the two structures are quite similar, but the proposed strategy uses two GPC controllers to replace the three PI controllers of the conventional strategy. To use the grid voltage as feedforward and improve the disturbance rejection capability, the d -axis current reference is calculated based on the power balance in (4) while assuming the q -axis grid voltage as 0 due to the grid voltage orientation.

B. GPC for dc-Link Voltage Control

For GPC implementation, the controlled plant in (2) is preferred to be rewritten as the following extended form [33], [34]:

$$\left\{ \begin{array}{l} \underbrace{\begin{bmatrix} \Delta V_{DC}(k+1) \\ V_{DC}(k+1) \end{bmatrix}}_{\mathbf{x}_m(k+1)} = \underbrace{\begin{bmatrix} 10 \\ 11 \end{bmatrix}}_{A_m} \underbrace{\begin{bmatrix} \Delta V_{DC}(k) \\ V_{DC}(k) \end{bmatrix}}_{\mathbf{x}_m(k)} \\ + \underbrace{\begin{bmatrix} T_s/C \\ T_s/C \end{bmatrix}}_{B_m} \underbrace{\Delta h(k)}_{\Delta h(k)} \\ V_{DC}(k) = \underbrace{\begin{bmatrix} 0 & 1 \end{bmatrix}}_{C_m} \underbrace{\begin{bmatrix} \Delta V_{DC}(k) \\ V_{DC}(k) \end{bmatrix}}_{y(k)} \end{array} \right. \quad (5)$$

where \mathbf{x}_m is the extended state variable, y and h are the output and input variables, respectively. A_m , B_m , and C_m are the coefficient matrices.

The prediction equation of the whole prediction horizon (N steps) can be expressed in a compact form

$$\mathbf{Y} = \Omega \mathbf{x}_m(k) + \mathbf{F} \Delta \mathbf{H} \quad (6)$$

$$\begin{aligned} \mathbf{Y} &= \begin{bmatrix} y(k+1) \\ y(k+2) \\ \vdots \\ y(k+N) \end{bmatrix}; \Delta \mathbf{H} = \begin{bmatrix} \Delta h(k) \\ \Delta h(k+1) \\ \vdots \\ \Delta h(k+N-1) \end{bmatrix}; \\ \Omega &= \begin{bmatrix} C_m A_m \\ C_m A_m^2 \\ \vdots \\ C_m A_m^N \end{bmatrix}; \mathbf{F} = \begin{bmatrix} C_m B_m & 0 & \cdots & 0 \\ C_m A_m B_m & C_m B_m & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots \\ C_m A_m^{N-1} B_m C_m & A_m^{N-2} B_m & \cdots & C_m B_m \end{bmatrix}. \end{aligned}$$

The cost function of GPC is usually designed as a quadratic form. Thus, the optimization problem to be solved can be expressed as [33], [34]

$$\min_{\Delta H} J = (\mathbf{Y}^* - \mathbf{Y})^T \mathbf{Q} (\mathbf{Y}^* - \mathbf{Y}) + \Delta \mathbf{H}^T \mathbf{R} \Delta \mathbf{H} \quad (7)$$

where $\mathbf{Y}^* = [V_{DC}^* \ V_{DC}^* \ \cdots \ V_{DC}^*]^T$ is the reference vector, in which the reference at the current instant is applied to the whole horizon; $\mathbf{Q} = \text{diag}[Q_1 \ Q_2 \ \cdots \ Q_N]^T$ and $\mathbf{R} = \text{diag}[R_1 \ R_2 \ \cdots \ R_N]^T$ are the weighting matrices of the output variables and input variables, which are related to the control performance of the GPC and should both be positive semi-definite. The elements of \mathbf{Q} are set as the same for all steps, i.e., $Q_k = q$, while the elements of \mathbf{R} are various in different steps, i.e., $R_k = r/R_{\text{step}}^{k-1}$, here R_{step} is the coefficient of the variation among steps.

According to the quadratic programming theory, the optimal solution of (7) is [33], [34]

$$\Delta \mathbf{H} = (\mathbf{F}^T \mathbf{Q} \mathbf{F} + \mathbf{R})^{-1} \mathbf{F}^T \mathbf{Q} [\mathbf{Y}^* - \Omega \mathbf{x}_m(k)]. \quad (8)$$

Finally, the first element of the optimized solution is accumulated to obtain the dc current reference:

$$i_{DC}^* = \frac{1}{1 - z^{-1}} \mathbf{W} \Delta \mathbf{H} \quad (9)$$

where $\mathbf{W} = \underbrace{[10 \ \cdots \ 0]}_N$.

C. ac Current Reference Calculation

The dc current reference obtained in (9) should be converted into the ac current reference, and then be tracked by the inner current control loop. The ac current reference calculation is based on the instantaneous power balance between the ac side and the dc side of the converter.

When the d -axis being oriented on the grid voltage vector, the q -axis grid voltage is 0, and thus, (4) can be simplified as

$$V_{DC}i_{DC} \approx \frac{3}{2}u_d i_d. \quad (10)$$

Then, the dc current reference obtained in (9) can be converted as the d -axis current as follows:

$$i_d^* = \frac{2V_{DC}i_{DC}^*}{3u_d}. \quad (11)$$

It should be noted that the approximately equal sign in (10) will not introduce any static errors to the dc-link voltage control, due to the existence of the accumulator of the GPC shown in (9), which plays a similar role as the integrator of a PI controller, and provides infinite open-loop gain to the dc errors. This claim will be validated by experiments in Section V.

D. Current Constraint

In a practical system, the ac current should be limited. If simply adding a limiter to the d -axis current reference, the GPC may suffer from overshoots in transient processes. This is because the output of the accumulator in (9) will not stop increasing even when the d -axis current limiter is triggered. To solve this problem, the accumulator in (9) should be responsible for the ac current limitation, which works similarly as an integrator with antiwindup. To accurately limit the ac current, the threshold of the accumulator should be adaptively adjusted, due to the varying dc-link voltage and grid voltage. The adaptive threshold is also calculated based on the instantaneous power balance.

When the d -axis current constraint is defined as $i_{d_low} \leq i_d \leq i_{d_up}$, the threshold of the accumulator should be set as

$$\frac{3u_d i_{d_low}}{2V_{DC}} \leq i_d^* \leq \frac{3u_d i_{d_up}}{2V_{DC}}. \quad (12)$$

E. GPC for ac Current Control

Actually, conventional PI control can also be utilized in the inner current control loop (leads to a cascaded structure with outer GPC and inner PI), which can largely remain the advantages of dc-link voltage control provided by the outer GPC loop only if the inner PI is well tuned. However, the GPC-based inner current control loop is likely to provide better rejection capability to the grid voltage harmonics, since the wider control bandwidth is more likely to be achieved by GPC for the absence of the stability-related compromises in the tuning stage [31], as well as the mature delay compensation methods [32]. Meanwhile, the design, implementation, and analysis of the current GPC are almost the same as the dc-link voltage GPC, which means that little extra effort is required to

utilize GPC in the inner current control loop. Therefore, GPC is utilized in both the outer and inner loops in this article.

The design of the GPC for the ac current control is similar to the previous GPC design for the dc-link voltage control. The extended incremental model for the ac current control can be expressed as [33], [34]

$$\left\{ \begin{array}{l} \begin{bmatrix} \Delta i_d(k+1) \\ \Delta i_q(k+1) \\ i_d(k+1) \\ i_d(k+1) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 - \frac{R_s}{L_s}\omega_{100} \\ -\omega_1 - \frac{R_s}{L_s}00 \\ 1 - \frac{R_s}{L_s}\omega_{110} \\ -\omega_1 - \frac{R_s}{L_s}01 \end{bmatrix}}_{A_m} \begin{bmatrix} \Delta i_d(k) \\ \Delta i_q(k) \\ i_d(k) \\ i_d(k) \end{bmatrix} \\ + \underbrace{\begin{bmatrix} T_s/L_s \\ T_s/L_s \end{bmatrix}}_{B_m} \begin{bmatrix} \Delta v_d(k) \\ \Delta v_q(k) \end{bmatrix}_{\Delta h(k)} \\ \begin{bmatrix} i_d(k) \\ i_d(k) \end{bmatrix} = \underbrace{\begin{bmatrix} 0010 \\ 0001 \end{bmatrix}}_{C_m} \begin{bmatrix} \Delta i_d(k) \\ \Delta i_q(k) \\ i_d(k) \\ i_d(k) \end{bmatrix}. \end{array} \right. \quad (13)$$

The prediction equation and the cost function are the same as (6) and (7). The only difference is that the multistep reference is $\mathbf{Y}^* = [i_d^* i_q^* i_d^* \dots i_d^* i_q^*]^T$, and the elements of the weighting matrices are submatrices rather than numbers, i.e., $\mathbf{Q}_j = [Q_{jd} \ 0; \ 0 \ Q_{jq}]$ and $\mathbf{R}_j = [R_{jd} \ 0; \ 0 \ R_{jq}]$.

Then, the optimized solution is obtained in the same way as (8). Finally, the first two elements of the optimized solution are accumulated to obtain the d - q axis voltage commands to supply the PWM module [33], [34]:

$$\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = \frac{1}{1-z^{-1}} \mathbf{W} \Delta \mathbf{H} \quad (14)$$

$$\text{where } \mathbf{W} = \underbrace{\begin{bmatrix} 10 \dots 0 \\ 01 \dots 0 \end{bmatrix}}_N.$$

IV. STABILITY ANALYSIS AND DESIGN REMARKS

The stability analysis of GPC with constraints and online-optimizer is still an open problem, since none of the classical methods, e.g., Bode plot, Nyquist curve, or eigenvalue locus, is applicable. Fortunately, the GPC proposed in this article can be implemented in an off-line way (also called as explicit GPC), which means that the GPC controller can be finally expressed as some constant matrices. This is achieved based on two conditions: first, the controlled plant should be a time-invariant system; second, the constraints should be ignored in the GPC (but still achieved with extra methods outside the GPC in this article). Thus, the classical stability analysis methods can be applied. In this section, the transfer functions of the proposed GPC-based control strategy will be derived, based on which, the impacts of different parameters on the system stability and performance will be theoretically

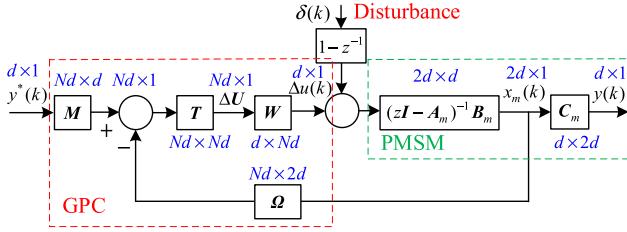


Fig. 3. Block diagram of GPC (same for both dc-link voltage control loop and ac current control loop).

discussed, and then, a guideline of parameter design of the proposed GPC-based control strategy will be given.

A. Transfer Functions

In order to simplify the analysis, the outer dc-link voltage control loop and the inner ac current control loop are separately studied by ignoring the coupling between them, since the control bandwidths of these two loops are usually very different and the interaction between them is quite slight. Based on (5) to (14), the proposed GPC-based control strategy for the dc-link voltage and the ac current can both be expressed as block diagrams shown in Fig. 3, where the dimensions of all the matrices are indicated. In Fig. 3, d represents the dimension of the output variable, which should be one for the outer dc-link voltage control loop, and should be two for the inner ac current control loop. In Fig. 3, $\delta(k)$ represents the disturbance, $M = [I(2 \times 2), \dots, I(2 \times 2)]^T$ is used

to exploit the current reference to the whole prediction horizon. $T = (F^T Q F + R)^{-1} F^T Q$ is obtained from (8), and all the other matrices are defined previously in Section II.

Based on Fig. 3, the open-loop and closed-loop transfer functions of the proposed GPC-based control strategy can be respectively expressed as

$$G_{\text{open}}(z) = (zI - A_m)^{-1} B_m W T \Omega \quad (15)$$

$$G_{\text{closed}}(z) = \frac{y(k)}{y^*(k)} = C_m \frac{(zI - A_m)^{-1} B_m W T}{I + (zI - A_m)^{-1} B_m W T \Omega} M. \quad (16)$$

The transfer functions in (15) and (16) will be used in the subsequent stability analysis and parameter design.

The closed-loop transfer function from the disturbance to the output can also be obtained from Fig. 3, as

$$G_{\delta,y}(z) = \frac{y(k)}{\delta(k)} = C_m \frac{(1 - z^{-1})(zI - A_m)^{-1} B_m}{I + (zI - A_m)^{-1} B_m W T \Omega} \quad (17)$$

which can be used to analyze the disturbance rejection capability in the subsequent part.

B. Stability Analysis

When discussing the stability, the outer dc-link voltage control loop and the inner ac current control loop are still separately considered. In this part, the impacts of the main GPC parameters on the system stability will be analyzed. Meanwhile, the estimation errors of the plant parameters are also discussed. The stability analysis in this part is based on

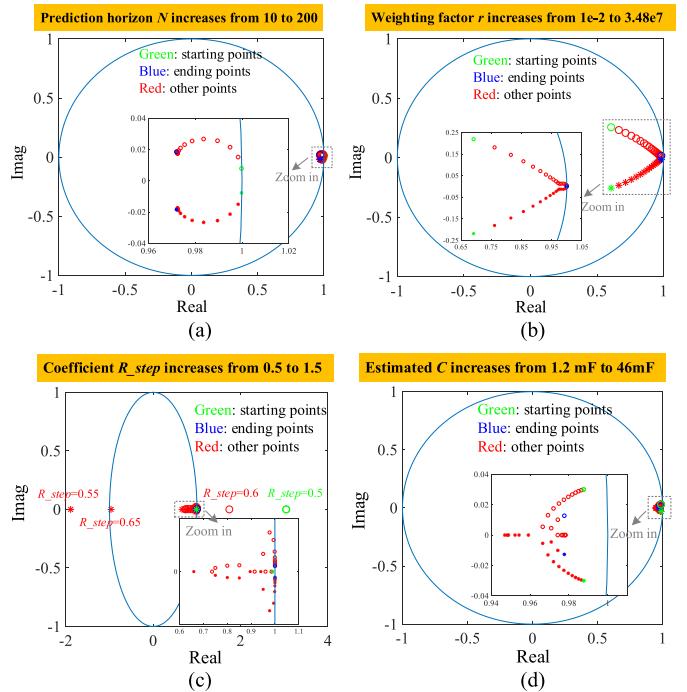


Fig. 4. Eigenvalue loci of outer GPC control loop for dc-link voltage control with varying parameters. (a) Prediction horizon N . (b) Weighting factor r . (c) Coefficient R_{step} . (d) dc-link capacitance mismatch.

the eigenvalue loci of the characteristic equation, which can be expressed as

$$\det[I + (zI - A_m)^{-1} B_m W T \Omega] = 0. \quad (18)$$

Considering the discrete system, the system is stable when all the eigenvalues are located inside the unit circle, otherwise the system is unstable [35].

The eigenvalue loci of the outer GPC control loop for the dc-link voltage control are shown in Fig. 4. The system parameters used in the analysis are the same as those of the test platform, as shown in Table II in Section V. As can be observed in Fig. 4(a), the outer loop is stable when the prediction horizon varies from 10 to 200 with a fixed increment of ten. However, when the prediction horizon is quite small, e.g., $N = 10$, the eigenvalues are located quite close to the boundary of the unit circle, which indicates that the outer GPC loop is almost critically stable and might suffer from some resonance problems. When the prediction horizon increases to 90 or larger values, the eigenvalues are almost fixed, which indicates that very little benefit can be obtained by further increasing the prediction horizon when it is larger than 90.

The weighting matrix Q is set as a unit diagonal matrix, and the other weighting matrix R is tuned and analyzed. As given previously, the weighting matrix R is defined as $R = \text{diag}[R_1 R_2 \dots R_N]^T$ and $R_k = r/R_{\text{step}}^{k-1}$. Thus, two coefficients, i.e., r and R_{step} , are discussed in Fig. 4(b) and (c), respectively. As can be observed in Fig. 4(b), the eigenvalues are always located inside the unit circle, but they move toward the boundary of the unit circle when the coefficient r increases from $1e-2$ to $3.48e7$ exponentially with a base of 2, which indicates that the system is always stable but it tends to be

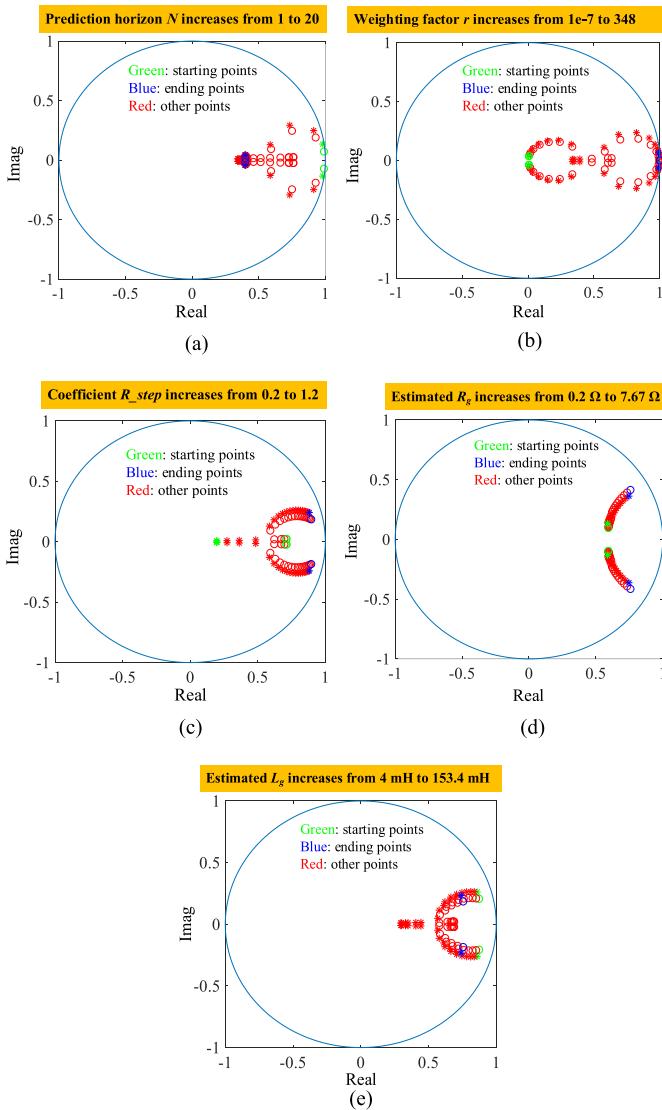


Fig. 5. Eigenvalue loci of inner GPC control loop for ac current control with varying parameters. (a) Prediction horizon N . (b) Weighting factor r . (c) Coefficient R_{step} . (d) Filter resistance mismatch. (e) Filter inductance mismatch.

critically stable when r is too large. In Fig. 4(c), the coefficient R_{step} changes from 0.5 to 1.5 with a fixed increment of 0.05, and it can be observed that the eigenvalues are located outside the unit circle when R_{step} is relatively small, which means that the system is unstable. On the contrary, when R_{step} is larger than 1.1, the outer GPC loop is almost critically stable, and thus, resonance might appear.

In addition to the control parameters discussed above, the parameter mismatch of the dc-link capacitance C is analyzed in Fig. 4(d), where the estimated C increases from 1.2 to 46 mF exponentially with a base of 1.2. It can be observed that the outer GPC loop keeps stable when the estimated C varies in the larger range, and the eigenvalues keep far enough from the boundary of the unit circle, which indicates that resonances are likely to be avoided even when a large parameter mismatch of the dc-link capacitance exists.

A similar analysis can be conducted to the inner GPC loop for the ac current control, whose eigenvalue loci are shown in Fig. 5. It can be observed that the parameters impact the

TABLE I
IMPACTS OF PARAMETERS ON STABILITY

Parameters		Impacts
Prediction horizon N	Large	Good stability
	Small	Tend to be critically stable (resonance)
Weighting factor r	Large	Tend to be critically stable (resonance)
	Small	Good stability
Coefficient R_{step}	Large	Outer loop: critically stable (resonance) Inner loop: little impact
	Small	Outer loop: unstable Inner loop: little impact
Plant parameter mismatch		Little impact

stability of the inner GPC loop in a similar way as the outer GPC loop is impacted. Thus, the inner GPC loop has good stability unless the system gets critically stable with a very small prediction horizon (1 or 2) or a very large weighting factor r (larger than 1). The coefficient R_{step} has less impact on the inner GPC loop than on the outer one, since the inner GPC loop keeps stable when R_{step} varies from 0.2 to 1.2. The plant parameters of the inner GPC loop, i.e., the estimated filter resistance R_g and the estimated filter inductance L_g , both have quite limited impacts on the stability of the inner GPC loop, since the system keeps stable when a large parameter mismatch exists, and all the eigenvalues stay far enough from the boundary of the unit circle.

Therefore, it can be concluded that the prediction horizon N and the weighting factor r have similar impacts on the outer and inner GPC loops, i.e., the system keeps stable when N and r vary in larger ranges, but potential resonances might appear when N is too small or r is too large. The coefficient R_{step} has significant impacts on the outer GPC loop, i.e., unstable when R_{step} is too small and critically stable when it is too large. However, R_{step} has little impact on the inner GPC loop. The mismatches of the plant parameters have little impact on both the outer and inner GPC loops, since the system keeps stable when large parameter mismatches exist. These findings are also presented in Table I.

C. Disturbance Rejection Analysis

The disturbance rejection capability of the GPC with different control parameters and system parameter mismatches can be analyzed based on the Bode diagrams of transfer function shown in (17). For the outer GPC loop, which is a single-input-single-output (SISO) one, the disturbance is the dc load. For the inner GPC loop, which is a multiple-input-multiple-output (MIMO) one, the disturbance is the grid voltage, and the Bode diagram of the d - d channel (from d -axis disturbance to d -axis output) is presented, which is actually the same for the q - q channel. It should be noted that a lower magnitude of the Bode diagram means better disturbance rejection capability, and the system parameters used in the analysis are the same as those of the test platform, as shown in Table II in Section V.

In Fig. 6, the disturbance rejection capability of the outer GPC loop is demonstrated. From Fig. 6(a), it can be observed that a longer prediction horizon can benefit the disturbance rejection, but little benefit can be obtained when N is

TABLE II
PARAMETERS OF PLATFORM

Parameters	Values
DC capacitance	6000 μF
Line inductance	0.02 H
Line resistance	0.5 Ω
Sampling frequency	5 kHz
Grid voltage (phase to phase, peak)	40 V
Fixed DC load resistance	100 Ω
Switchable DC load resistance	300 Ω

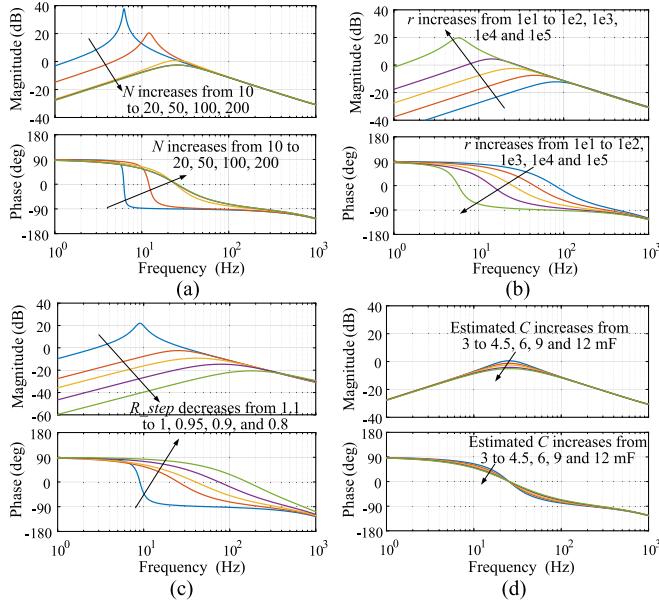


Fig. 6. Bode diagram of disturbance rejection of outer GPC control loop for dc-link voltage control with different parameters. (a) Prediction horizon N . (b) Weighting factor r . (c) Coefficient R_{step} . (d) dc-link capacitance mismatch.

greater than a particular value, since the Bode diagrams with $N = 100$ and 200 are almost the same. Meanwhile, the magnitudes are small in both the low-frequency range and the high-frequency range, and the dc components in the disturbance can be completely rejected by the GPC due to the $-\infty$ dB magnitude at 0 Hz point (cannot be shown in the figures), which is introduced by the internal integrator of the GPC. In Fig. 6(b), smaller r is observed to provide better disturbance rejection capability, since the GPC is more “free” due to the less penalty given to the input increments. In Fig. 6(c), the coefficient R_{step} seems to have similar influences on the disturbance rejection capability of GPC, i.e., smaller R_{step} can better reject the load disturbances. In Fig. 6(d), the estimation mismatch of the dc capacitance is evaluated, and it can be observed that the parameter mismatch only has slight impact on the disturbance rejection capability.

Similar results can be found in the Bode diagrams of the inner GPC loop, as shown in Fig. 7. Thus, the following conclusions can be drawn: 1) larger prediction horizon N benefits the disturbance rejection, but further improvement cannot be achieved when N is already large enough, 2) smaller weighting factor r and coefficient R_{step} can both improve

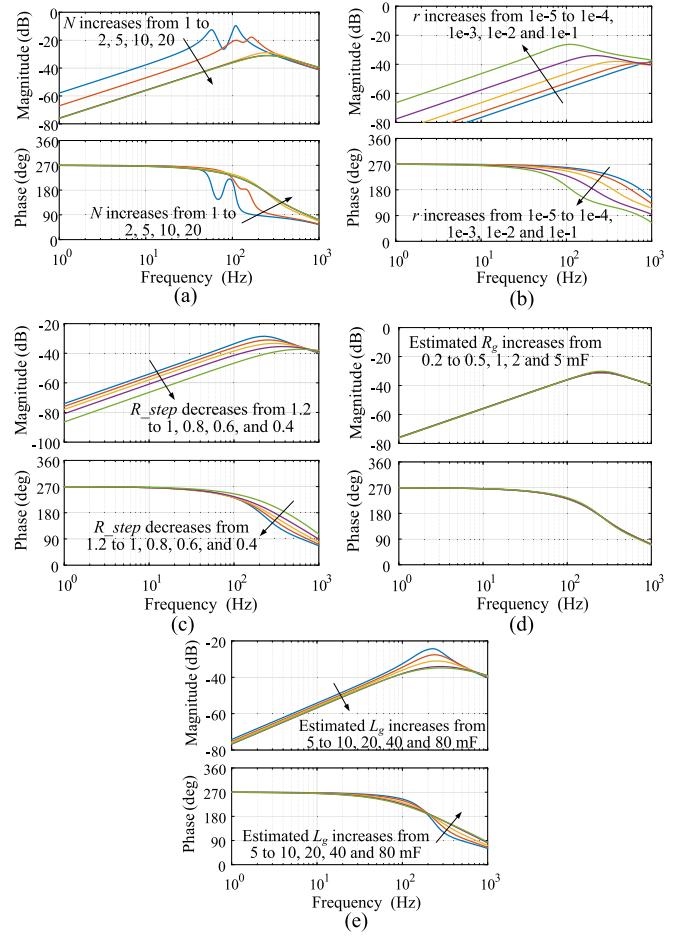


Fig. 7. Bode diagram of disturbance rejection of inner GPC control loop for ac current control with different parameters. (a) Prediction horizon N . (b) Weighting factor r . (c) Coefficient R_{step} . (d) Filter resistance mismatch. (e) Filter inductance mismatch.

the disturbance rejection capability, and 3) the estimation mismatches of the system parameters only have slight impact on the disturbance rejection capability.

D. Parameter Design Remarks

A brief discussion about the parameter design of the proposed GPC-based control strategy is given in this part. Three main parameters should be designed for both the outer and inner GPC loops, i.e., the prediction horizon N , the weighting factor r , and the coefficient R_{step} . The closed-loop transfer function $G_{closed}(z)$ derived in (16) can help the parameter design. The step responses of the GPC loops can be easily obtained by calling the MATLAB function $step[G_{closed}(z)]$, and that of the outer GPC loop with different parameters are shown in Fig. 8. With the help of the step response, the guideline of the parameter design can be described with the flowchart shown in Fig. 9.

More detailedly, among the three parameters, the prediction horizon N is the most fundamental one, since it directly determines the computation burden of the GPC control. Thus, N should be selected first. Considering that the dynamic of the inner current loop is much faster than that of the outer V_{dc}

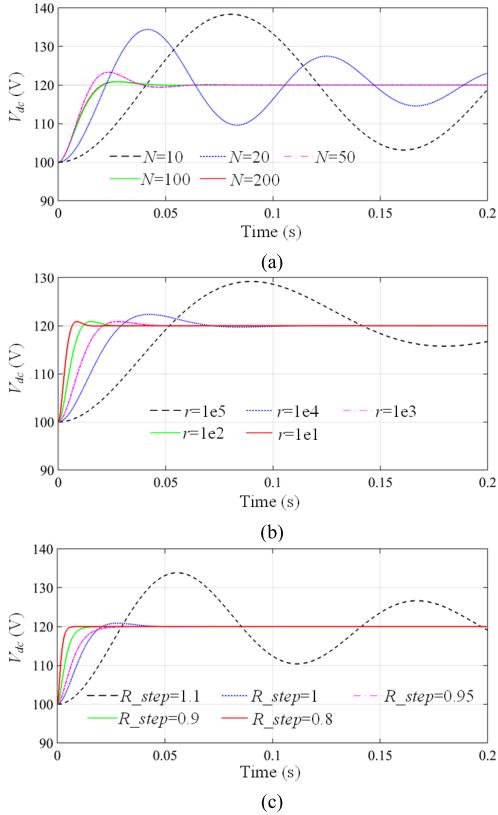


Fig. 8. Step responses of outer GPC loop with different parameters. (a) Different prediction horizon N ($r = 1e3$, $R_{step} = 1$). (b) Different weighting factor r ($N = 100$, $R_{step} = 1$). (c) Different coefficient R_{step} ($N = 100$, $r = 1e3$).

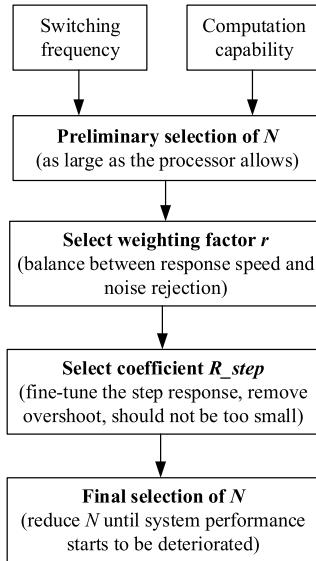


Fig. 9. Parameter design process of proposed GPC-based control strategy.

loop, N of the outer loop should be much larger than that of the inner loop. Thus, the matrix dimensions of the outer loop are much larger and the most computation effort is actually consumed by the outer loop. Therefore, the N selection of the outer loop is more important, which should be selected with the consideration of the switching frequency and the

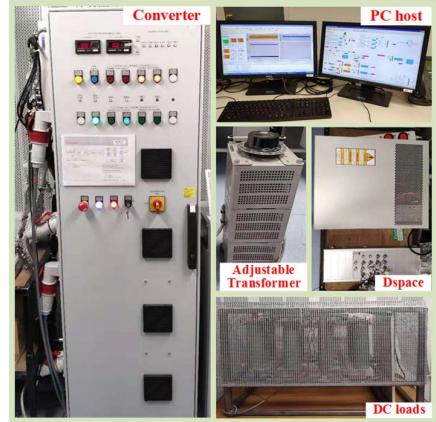


Fig. 10. Test platform used in experiments.

computation capability of the processor (memory and clock frequency). Considering that the control performance (stability and step response) will hardly change when N is higher than a value [see Figs. 4(a), 5(a), and 8(a)], a large N can be selected first, but it should be acceptable to the processor. For example, in this article, N can be set as 200 and 20 for the outer and inner GPC loops, respectively.

Then, the weighting factor r should be selected (here R_{step} is set as 1), which determines the step response speed. Large r leads to slow step response and good measurement noise rejection, but low-frequency resonance may appear. Small r leads to fast step response, but high-frequency distortions might be caused due to the sensitivity to the measurement noises. A middle r is recommended to balance the step response speed and the measurement noise rejection, e.g., $r = 1e3$ for the outer GPC loop and $r = 1e-2$ for the inner GPC loop are recommended in this article.

In most conditions, overshoots can hardly be completely removed by merely adjusting r , as shown in Fig. 8(b). Thus, the coefficient R_{step} can be adjusted to fine-tune the step response. R_{step} smaller than 1 can help eliminate the overshoots, but it should not be too small, due to the instability risk shown in Fig. 4(c). In this article, R_{step} for the outer GPC loop is set as 0.8, and that for the inner GPC loop is set as 0.4.

Finally, we can turn back to reduce the prediction horizon N , until the system performance starts to be deteriorated. The final parameters for the outer GPC loop are $N = 100$, $r = 1e3$, and $R_{step} = 0.8$, and those for the inner GPC loop are $N = 10$, $r = 1e-2$, and $R_{step} = 0.4$.

V. EXPERIMENTAL VALIDATION

In order to validate the proposed strategy, experimental results are provided in this section. The used test platform is shown in Fig. 10. The proposed GPC-based control strategy is implemented on a set of dSPACE DS1006. The system parameters are shown in Table II. All the results were captured using dSPACE software and then plotted using EXCEL. In the experiments, the d -axis current limitation is set as -3 A to 3 A. In the experiments, the following three indexes are mainly concerned: the step response speed, the overshoot,

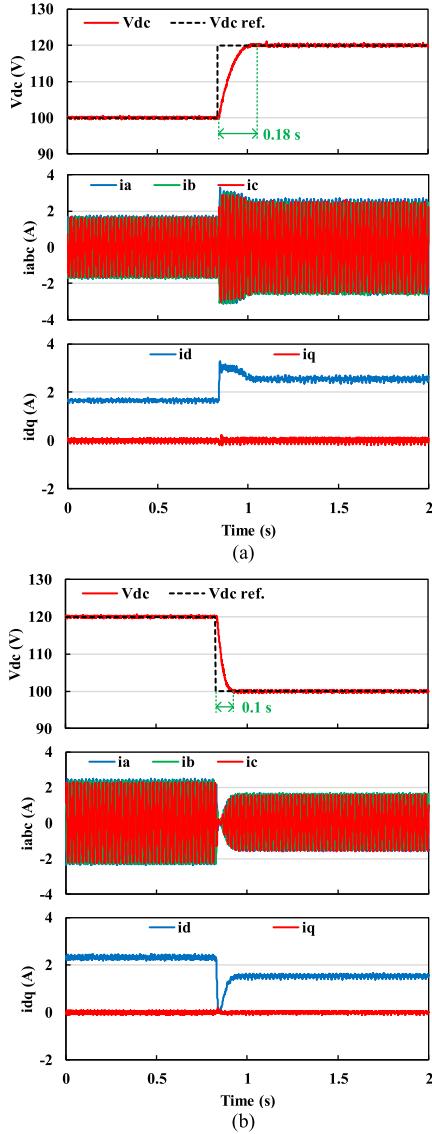


Fig. 11. Experimental results of proposed GPC-based control strategy for dynamic performance test. (a) dc-link voltage steps up. (b) dc-link voltage steps down.

the peak, and the duration of the transient processes caused by disturbances.

This section is presented in the following five parts.

- 1) Dynamic performance test.
- 2) Disturbance rejection test.
- 3) Comparison with cascaded PI.
- 4) Parameter mismatch test.
- 5) Roles of outer and inner loops (simulation results).

A. Dynamic Performance Test

One of the merits of the proposed GPC-based dc-link voltage control strategy is the good dynamic performance. In order to validate this, the experimental waveforms of dc-link voltage reference stepping up and down are presented in Fig. 11. It can be observed that the transient processes of the dc-link voltage stepping up and down are both overshoot-free. When the dc-link voltage reference steps from 100 to 120 V, the whole

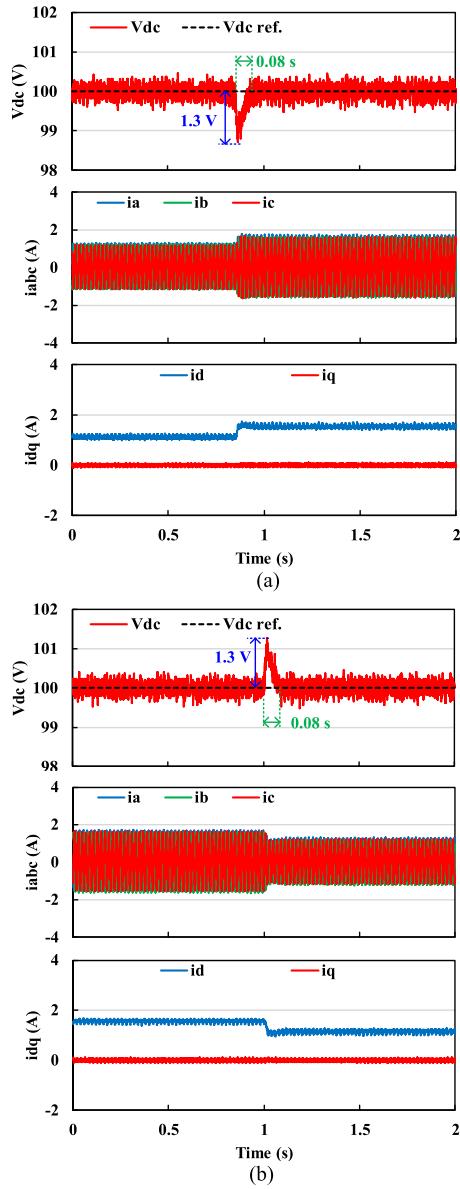


Fig. 12. Experimental results of proposed GPC-based control strategy for dc load disturbance test. (a) dc load steps up. (b) dc load steps down.

transient process lasts about 0.18 s, and the *d*-axis current is limited below 3 A as desired. When the dc-link voltage reference steps from 120 to 100 V, the whole transient process lasts about 0.1 s.

B. Disturbance Rejection Test

In addition to the good dynamic performance, the proposed GPC-based dc-link voltage control strategy also has advantages in disturbance rejection capability. In order to validate this, the experimental waveforms of dc load steps and grid voltage steps are presented in Figs. 12 and 13, respectively.

In Fig. 12, a switchable load resistor is used to increase or decrease the dc load, which makes the dc load resistance change between 100 and 75 Ω. It can be observed that the transient peaks caused by the dc load steps are about 1.3 V,

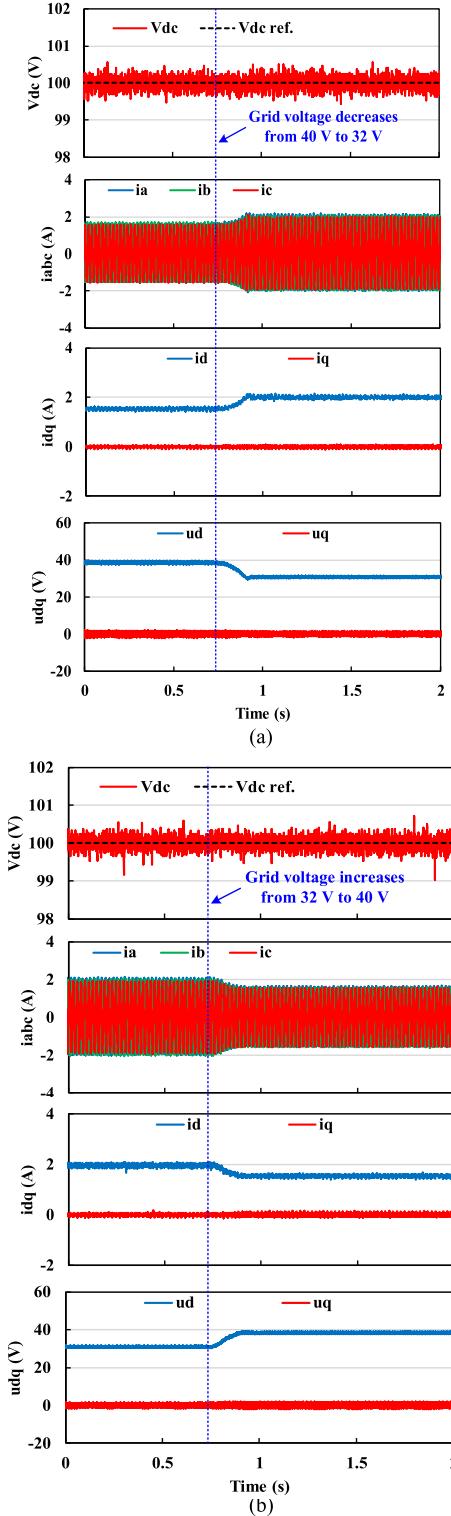


Fig. 13. Experimental results of proposed GPC-based control strategy for grid voltage disturbance test. (a) Grid voltage steps down. (b) Grid voltage steps up.

regardless of the dc load stepping up or down. The transient processes are fast, which last about 0.08 s.

In Fig. 13, the grid voltage disturbance is tested. In Fig. 13, when the grid voltage changes, the d -axis current responds rapidly, and little transient process can be observed in the

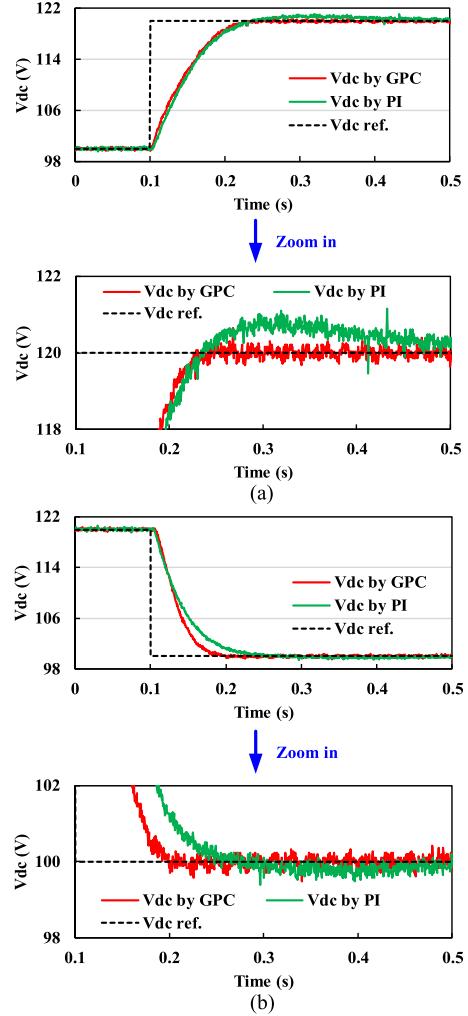


Fig. 14. Experimental results of proposed GPC-based control strategy and cascaded PI for dynamic performance test. (a) dc-link voltage steps up. (b) dc-link voltage steps down.

dc-link voltage waveforms. It should be noted that the grid voltage changes are not ideal fast steps, since they are achieved by manually operating the adjustable transformer. In order to better validate the good disturbance rejection capability against the grid voltage step, simulation results are provided in Appendix C, where the same parameters are applied, but the grid voltage changes abruptly. From the simulation results, it can be observed that the proposed GPC-based control strategy actually suffers a transient process when the grid voltage changes abruptly, but the peak and duration of the transient process are both very slight.

C. Comparison With Cascaded PI

In order to better validate the merits of the proposed GPC-based dc-link voltage control strategy, the conventional cascaded PI control is also tested for comparison, as shown in Figs. 14 and 15. In these tests, the PI controller is carefully tuned in a trial and error way to balance the dynamic performance and the disturbance rejection capability: $K_p = 0.1$ and $K_i = 1$ for the outer loop, $K_p = 20$ and $K_i = 500$ for the inner

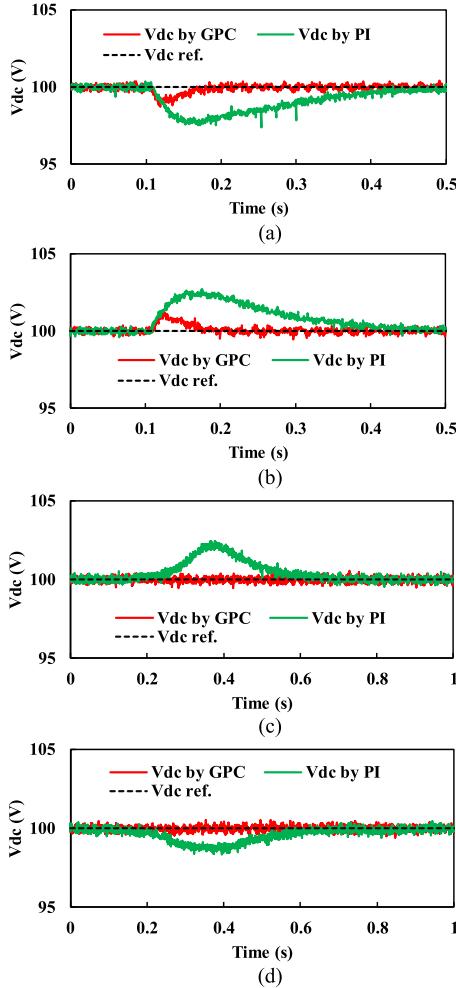


Fig. 15. Experimental results of proposed GPC-based control strategy and cascaded PI for disturbance rejection test. (a) dc load steps up. (b) dc load steps down. (c) Grid voltage steps up. (d) Grid voltage steps down.

loop. To better explain the tuning process of the PI controller, more experimental results with different PI parameters are shown in Appendix A, and the tuning results with the help of linear control toolbox are shown in Appendix B. In general, the finally selected PI parameters make a proper benchmark to be compared with the proposed GPC-based control strategy.

In Fig. 14, the dynamic performances of the proposed GPC-based control strategy and the cascaded PI are compared. As can be observed in Fig. 14(a), the proposed GPC-based control strategy completely avoids overshoots when the dc-link voltage steps from 100 to 120 V. However, the cascaded PI introduces an overshoot of about 1 V. As for the dynamic response speed, the proposed GPC-based control strategy and the cascaded PI have similar dc-link voltage rising speed, since the d -axis current is limited as 3 A in this process. However, the total settling time (the time required for the dc-link voltage to reach and remain within the error band of 0.2 V) is different, i.e., about 0.15 s for the proposed GPC-based control strategy, and over 0.4 s for the cascaded PI due to the aforementioned overshoot. In Fig. 14(b), the proposed GPC still has better dynamic performance than the cascaded PI when the

TABLE III
COMPARISON OF PERFORMANCE INDEXES

Performance indexes		GPC	PI
Overshoot	$V_{dc} \uparrow$	0 V	1 V
	$V_{dc} \downarrow$	0 V	0 V
Response speed	$V_{dc} \uparrow$	0.13 s	0.13 s
	$V_{dc} \downarrow$	0.1 s	0.15 s
Disturbance rejection	Transient peak	DC Load \uparrow	2.9 V
		DC Load \downarrow	2.9 V
	Transient duration	$V_{grid} \uparrow$	2.5 V
		$V_{grid} \downarrow$	1.5 V
	DC Load \uparrow	0.08 s	0.4 s
	DC Load \downarrow	0.08 s	0.4 s
	$V_{grid} \uparrow$	0 s	0.45 s
	$V_{grid} \downarrow$	0 s	0.4 s

dc-link voltage steps down. The proposed GPC-based control strategy completely avoids overshoots, while the cascaded PI introduces a slight overshoot of about 0.3 V. The dynamic response speeds of the two strategies differ significantly. The transient period of the proposed GPC-based control strategy is about 0.1 s, and that of the cascaded PI is about 0.27 s. By comparing Figs. 14(a) and (b), it can be observed that the dynamic response speed is more different when the dc-link voltage steps down, since the current constraint is not triggered in the dc-link voltage stepping down process, and thus, the merits of GPC are more significantly demonstrated.

In Fig. 15, the disturbance rejection capabilities of the proposed GPC-based control strategy and the cascaded PI are compared. In Fig. 15(a) and (b), the dc load disturbance is tested. It can be observed that the proposed GPC-based control strategy has smaller transient peak and shorter transient period than the cascaded PI, i.e., about 1.2 V and 0.08 s for the proposed GPC-based control strategy, and about 2.9 V and 0.4 s for the cascaded PI. In Fig. 15(c) and (d), the grid voltage disturbance is tested. It can be observed that the proposed GPC-based control strategy can well reject the grid voltage disturbances, but the cascaded PI suffers from significant transient processes, i.e., 2.5 V and 0.45 s when the grid voltage increases, and 1.5 V and 0.4 s when the grid voltage decreases. The grid voltage step disturbance rejection is also tested with simulation in Appendix C, from which the same conclusion can be drawn, i.e., the proposed GPC-based control strategy can significantly better reject the grid voltage disturbance.

The main performance indexes of the two controllers are shown in Table III, which clearly demonstrates the superiority of the proposed GPC-based control strategy. However, it should be noted that the PI controller can be tuned to be as good as GPC or even better in one or two performance indexes, e.g., completely avoiding the overshoot, at the expense of greater compromises in the rest indexes, as shown in the tuning results with the help of linear control toolbox in Appendix B.

D. Parameter Mismatch Test

Considering that the outer loop is more important than the inner loop for the dc-link voltage control, the key parameter

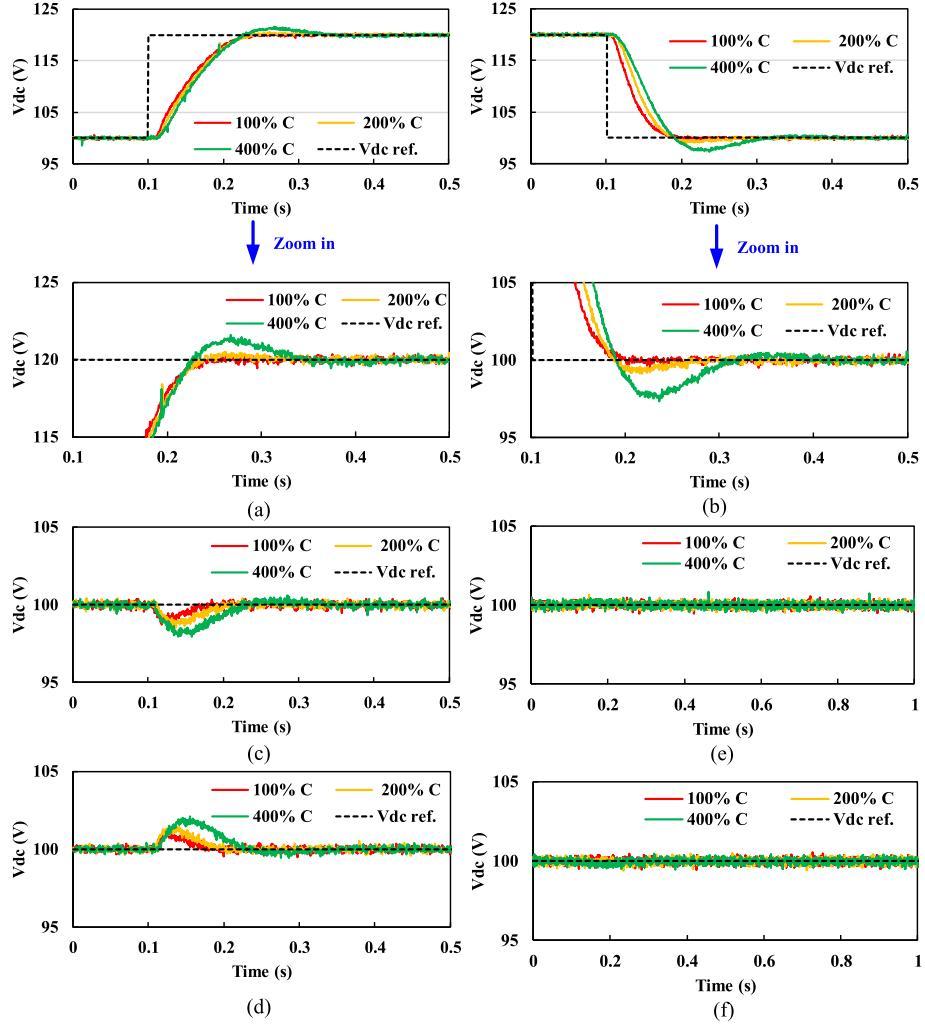


Fig. 16. Experimental results of proposed GPC with overestimated dc capacitance. (a) dc-link voltage steps up (b) dc-link voltage steps down. (c) dc load steps up. (d) dc load steps down. (e) Grid voltage steps up. (f) Grid voltage steps down.

of the GPC implementation for dc-link voltage control is the dc capacitance. When the estimation error of the dc capacitance exists, the control performance of the proposed GPC-based control strategy will be impacted. The experimental results of the proposed GPC-based control strategy with dc capacitance overestimated and underestimated are shown in Figs. 16 and 17, respectively.

Fig. 16(a) shows the dynamic responses of the dc-link voltage reference stepping up with different degrees of dc capacitance overestimation. It can be observed that the dynamic performance of the proposed GPC-based control strategy keeps as good as that with correct parameter even when the dc capacitance is overestimated as two times, but overshoot appears when the dc capacitance is overestimated as four times. Similar results can be observed in the dynamic responses of the dc-link voltage reference stepping down shown in Fig. 16(b). In Fig. 16(c) and (d), the disturbance rejection capability of the proposed GPC-based control strategy against load disturbances recedes with the increase of the dc capacitance estimation error. When the dc capacitance is overestimated as four times, the transient peak and period are about 2 V and 1.5 s

which is still significantly better than the well-tuned PI shown in Fig. 15. In Fig. 16(e) and (f), the proposed GPC-based control strategy can well reject the grid voltage disturbances even when the dc capacitance is significantly overestimated.

In general, the following conclusions can be drawn: 1) the dynamic performance and the rejection capability against load disturbances of the proposed GPC-based control strategy are both deteriorated when the dc capacitance is overestimated, but the rejection capability against grid voltage disturbances is not impacted and 2) when the dc capacitance is overestimated by no more than two times, the control performance of the proposed GPC-based control strategy is only slightly impacted.

Fig. 17(a) shows the dynamic response of the dc-link voltage reference stepping up with different degrees of dc capacitance underestimation. It can be observed that the dynamic performance of the proposed GPC-based control strategy is only slightly deteriorated even when the dc capacitance is underestimated as 25%. However, as can be seen in Fig. 17(b), the dynamic performance of the dc-link voltage reference stepping down is more seriously impacted by the dc capacitance underestimation, and the overshoot is about 2.3 V when the dc

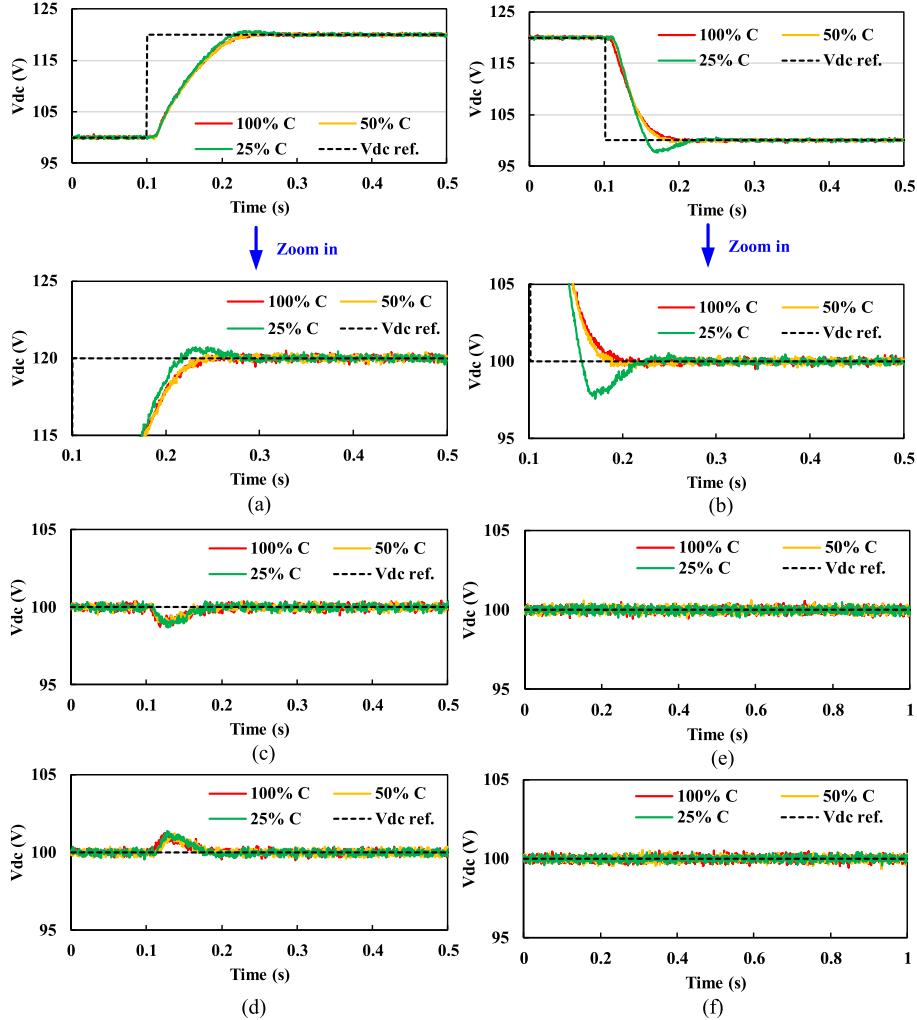


Fig. 17. Experimental results of proposed GPC-based control strategy with underestimated dc capacitance. (a) dc-link voltage steps up. (b) dc-link voltage steps down. (c) dc load steps up. (d) dc load steps down. (e) Grid voltage steps up. (f) Grid voltage steps down.

capacitance is underestimated by 25%. In Fig. 17(c) and (d), it can be observed that the disturbance rejection capability of the proposed GPC-based control strategy is rarely impacted by the dc capacitance underestimation. In Fig. 17(e) and (f), the proposed GPC-based control strategy can well reject the grid voltage disturbances even when the dc capacitance is significantly underestimated.

The grid voltage step disturbance rejection of the proposed GPC-based control strategy with different parameter mismatches is also tested with simulation in Appendix C. Different from the experimental results with slow grid voltage change, the abrupt grid voltage in the simulation can cause a transient process to the proposed GPC-based control strategy, and the transient process is greater when the dc-link capacitance is more misestimated.

Most importantly, when the dc capacitance is significantly misestimated, the static error can always be avoided.

Thus, the following conclusions can be drawn: 1) the dynamic performance of the proposed GPC-based control strategy is deteriorated by the underestimated dc capacitance, but the disturbance rejection capability is rarely impacted and

2) when the dc capacitance is underestimated by no less than 50%, the control performance of the proposed GPC-based control strategy is only slightly impacted, and 3) the static error can be fully avoided even when significant parameters exist.

E. Roles of Outer and Inner Loops (Simulation)

In the experimental tests, GPCs are applied to both the outer and inner control loops of a cascaded structure. For a fair and comprehensive comparison, different combinations of the outer and inner controllers are compared, i.e., PI+GPC (outer PI, inner GPC), PI+PI, GPC+GPC, and GPC+PI, as shown in Fig. 18. It should be noted that simulation results instead of experimental results are presented here, due to the lockdown of laboratory in the U.K. caused by the Covid-19 pandemic. It can be observed that the PI+PI (cascaded PI) and the PI+GPC almost have the same performance in both the step response and the disturbance rejection capability. Similarly, the GPC+GPC and the GPC+PI are also approximately the same. The comparison shows that the outer control loop plays

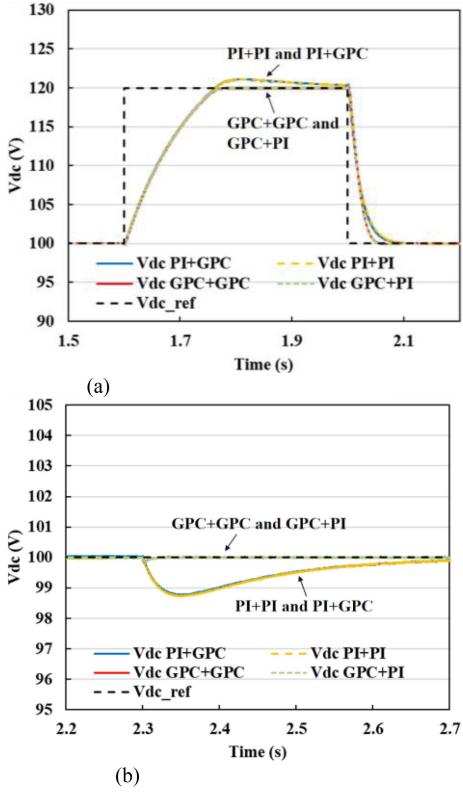


Fig. 18. Simulation results with different combinations of outer and inner controllers. (a) dc-link voltage step responses. (b) Grid voltage steps down.

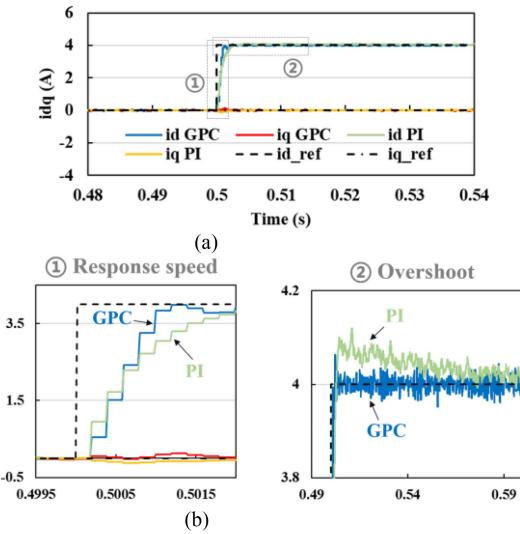


Fig. 19. Simulation results of current control with GPC and PI. (a) Overall view. (b) Zoom-in views.

the dominant role to improve the dc-link voltage control performance, while the inner current loop has little impact only if it is significantly faster than the outer loop. Meanwhile, considering the common inner current controller, the comparison between GPC+GPC and PI+GPC leads to the same conclusions as drawn in Part C of this section (experimental comparison between GPC+GPC and PI+PI), i.e., the GPC brings faster and overshoot-free step response, as well as better

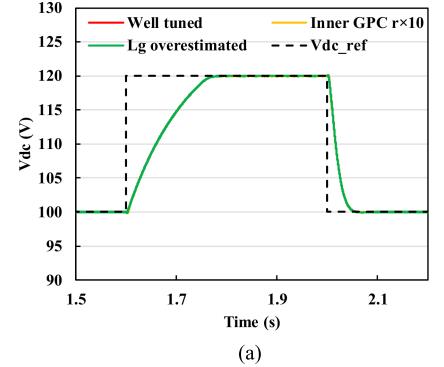
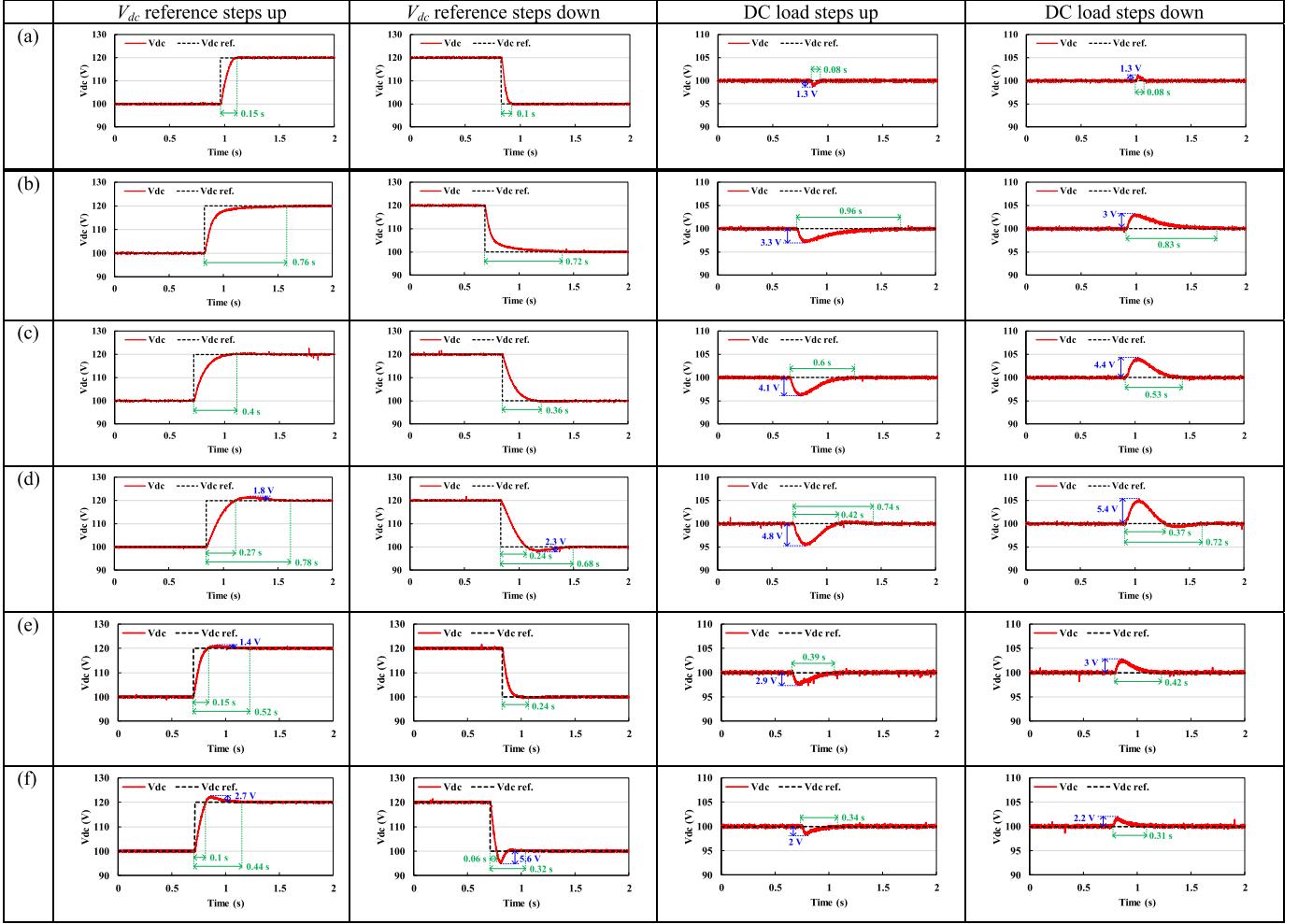


Fig. 20. Simulation results with different inner and outer GPC tunings. (a) dc-link voltage step responses with different inner GPC tunings. (b) Grid voltage steps down with different inner GPC tunings. (c) dc-link voltage step responses with different outer GPC tunings. (d) Grid voltage steps down with different outer GPC tunings.

disturbance rejection capability. The same conclusions can be drawn by comparing the waveforms of GPC + PI and PI+PI. It should be noted that the comparison study above can only illustrate the superiority of the outer GPC.

TABLE IV

EXPERIMENTAL RESULTS OF CASCADED PI STRATEGY WITH DIFFERENT OUTER LOOP PI PARAMETERS. (a) PROPOSED GPC. (b) PI WITH $K_p = 0.05$, $K_i = 0.25$. (c) PI WITH $K_p = 0.05$, $K_i = 0.5$. (d) PI WITH $K_p = 0.05$, $K_i = 1$. (e) PI WITH $K_p = 0.1$, $K_i = 1$. (f) PI WITH $K_p = 0.2$, $K_i = 2$



To better show the performance of the proposed GPC-based controller, the inner GPC for the current control is also compared with PI in Fig. 19, where the outer loop is removed and the dc-link voltage is fixed. From Fig. 19, it can be observed that the GPC also behaves better than PI in both the response speed and the overshoot of current control. More specifically, in the zoomed-in view on the left, it can be seen that the PI responds faster than the GPC at the first two steps due to the large PI parameters, but the rising rate of the PI decreases as the current approaching its reference value (an inherent feature of PI), and the GPC come up from behind. In the zoomed-in view on the right, it can be seen that the GPC almost avoids overshoot, but an overshoot of 0.1 A can be found in the PI waveform, which lasts about 0.1 s. In conclusion, the GPC also has some merits over conventional PI when applied to the inner current control.

In order to better show the separate impacts of the outer and inner GPCs of a cascaded GPC control structure, comparisons based on simulation are demonstrated in Fig. 20. It can be observed from Fig. 20(a) and (b) that the dc-link voltage waveforms with different inner GPC parameters or parameter

mismatches (L_g overestimated as two times) are almost coincident, which means that the inner current controller has little impact on the dc-link voltage control performance, only if it is significantly faster than the outer voltage controller. It should be noted that a slight resonance can be observed in Fig. 20(b) when the inner GPC is with an increased weighting factor r (leads to a slower inner loop), which indicates that the inner current controller should not be further slowed down. On the contrary, in Fig. 20(c) and (d), it can be observed that the dc-link voltage control performance is significantly impacted by the outer GPC tuning and parameter mismatch (C overestimated as two times), on both the step response and the disturbance rejection capability. Therefore, it is reasonable to pay more attention to the tuning and testing of the outer GPC.

VI. CONCLUSION

This article has presented a GPC-based control strategy for the dc-link voltage control of a grid-connected converter. The proposed strategy utilizes a cascaded structure with an outer dc-link voltage control loop and an ac current control loop, which are both based on GPC-based control strategy.

The design and implementation of the proposed strategy has been introduced in detail, and the system stability has been theoretically analyzed with eigenvalue loci. With the experimental validation, it can be concluded that the proposed GPC-based control strategy can better control the dc-link voltage than the conventional cascaded PI strategy, including faster and nonovershoot dynamic response and better rejection capability to grid or load disturbances. Meanwhile, the proposed GPC-based control strategy shows good robustness to parameter mismatches. The main drawback of the proposed strategy is the higher computation burden compared with PI, but it has been greatly reduced since the proposed GPC-based control strategy is implemented in an explicit way.

APPENDIX

A. Extra Experimental Results With Different PI Parameters

For a fair comparison, the PI controller used as a benchmark should be well tuned, which is achieved in a trial and error way. Thus, more experimental results of PI controllers with different parameters are presented and compared with the proposed strategy in Table IV. It should be noted that only the PI controller of the outer loop is considered here, since the dc-link voltage control performance mainly depends on the outer loop. Group (a) is the proposed GPC-based control strategy. By comparing groups (b), (c), and (d), it can be observed that larger K_i leads to faster step response and shorter disturbance transient duration, but may cause overshoot, and increases the transient peak amplitude caused by disturbances. By comparing groups (d) and (e), it can be observed that larger K_p can help damping the overshoot, as well as accelerate the step response speed and improve the disturbance rejection capability, but the high-frequency burrs are more significant due to the poor noise rejection capability, and the system can be unstable when K_p is too large. The waveforms in group (e), i.e., the PI controller used as the benchmark in the experiments ($K_p = 0.1$, $K_i = 1$), are significantly improved compared with groups (b) to (d). If the PI parameters are further increased to ($K_p = 0.2$, $K_i = 2$), the significant overshoot will appear, as shown in group (f), although the step response is faster and the disturbance rejection capability is improved. In general, among all the different PI parameter sets in Table IV, the group (e) with ($K_p = 0.1$, $K_i = 1$) has the best general performance to compromise the step response speed, overshoot, and disturbance rejection. Thus, it is fair to select this PI parameter set in the comparison study.

B. PI Tuning With Linear Control Toolbox (MATLAB)

In order to better prove that the PI controller compared with the proposed strategy is well tuned, the linear control toolbox provided by MATLAB is utilized for the PI tuning. It should be noted that only the PI controller of the outer loop is tuned here, since the dc-link voltage control performance mainly depends on the outer loop. In Fig. 21, the left waveform of each subfigure is the step response, and the right waveform is the disturbance response. First, the PI controller used in the experiments, i.e., $K_p = 0.1$ and $K_i = 1$, is used as a benchmark, whose responses are shown with dashed lines,

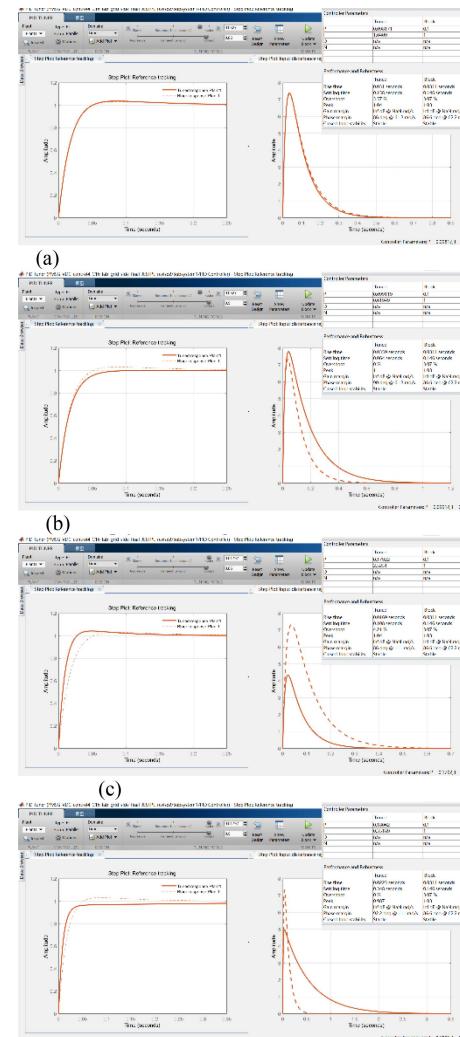


Fig. 21. PI tuning with linear control toolbox provided by MATLAB. (a) Benchmark compared with GPC in Section V. (b) Simply increasing transient behavior factor. (c) Simply reducing response time. (d) Simultaneously increasing transient behavior factor and reducing response time.

while the solid line shows the responses of the PI controller tuned by the toolbox. There are two adjustable parameters in the toolbox, i.e., the response time and the transient behavior. In Fig. 21(a), the PI controller is tuned to be similar as the benchmark, which shows that the response time is 0.0327 s, and the transient behavior factor is 0.86. In Fig. 21(b), only the transient behavior factor is increased to 0.9, and then the overshoot of the tuned PI controller (solid line) is completely avoided, which leads to an improved step response. However, in the right waveform of Fig. 21(b), it can be observed that the disturbance rejection capability is reduced, since the peak amplitude and the transient duration are both increased compared with the benchmark. In Fig. 21(c), only the response time is reduced to 0.01797 s, it can be observed that the tuned PI controller has a faster step response (larger rising slope), and the disturbance rejection capability is also improved. However, the overshoot is more serious than the benchmark (increases from 3.07% to 4.21%). In Fig. 21(d), the response time is reduced to 0.01797 s, and meanwhile, the transient behavior factor is increased to 0.9. It can be observed that

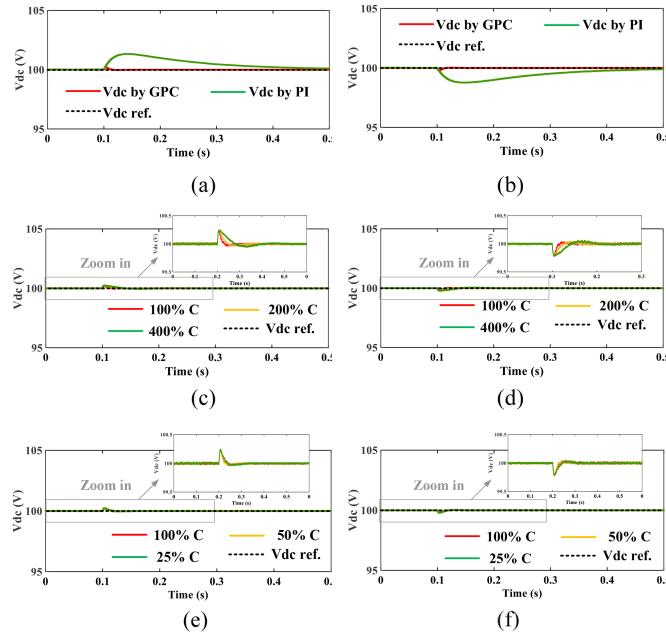


Fig. 22. Rejection of disturbances caused by abrupt grid voltage change. (a) Grid voltage increase (PI compared with GPC). (b) Grid voltage decrease (PI compared with GPC). (c) Grid voltage increase (dc-link capacitance overestimated). (d) Grid voltage decrease (dc-link capacitance overestimated). (e) Grid voltage increase (dc-link capacitance underestimated). (f) Grid voltage decrease (dc-link capacitance underestimated).

the overshoot is completely avoided and the step response is faster, but the disturbance rejection capability is poor, since the transient process caused by the disturbance is significantly longer.

Therefore, it can be seen that the main performance indexes, i.e., the step response speed, the overshoot, and the disturbance rejection capability, can hardly be comprehensively improved, and compromises must be made in the PI tuning process even with the help of the linear control toolbox provided by MATLAB. Considering that the proposed GPC-based strategy behaves better than the PI benchmark in all the three main performance indexes, it is reasonable to conclude that the proposed strategy has a better performance than PI.

C. Simulation Results of Disturbance Rejection With Grid Voltage Step

In Section V, the disturbance rejection capability tests with grid voltage step are conducted by manually operating the adjustable transformer, which is not convincing enough. Therefore, the simulation results with abrupt grid voltage steps are provided here for supplementary validation, as shown in Fig. 22. It can be observed that the proposed GPC-based strategy also suffers transient processes when the grid voltage abruptly changes (in the experiments, the transient process cannot be observed due to the relatively slow grid voltage change rate), but the peak and duration are both significantly smaller than those of the PI controller. Furthermore, as for the impacts of the capacitance mismatch, the simulation results lead to the same conclusions as the experimental results do.

In general, the proposed GPC-based strategy can better reject the disturbances of grid voltage step than conventional PI controllers.

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