ANALOG INTEGRATED CIRCUIT LAYOUT (EE 549)

DESIGN OF A LINEAR VOLTAGE REGULATOR

PROJECT

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Date: 05-12-2018

INTRODUCTION:

A linear voltage regulator circuit provides a constant voltage over a fixed load independent of the supply voltage.

SCHEMATIC OF LDO:

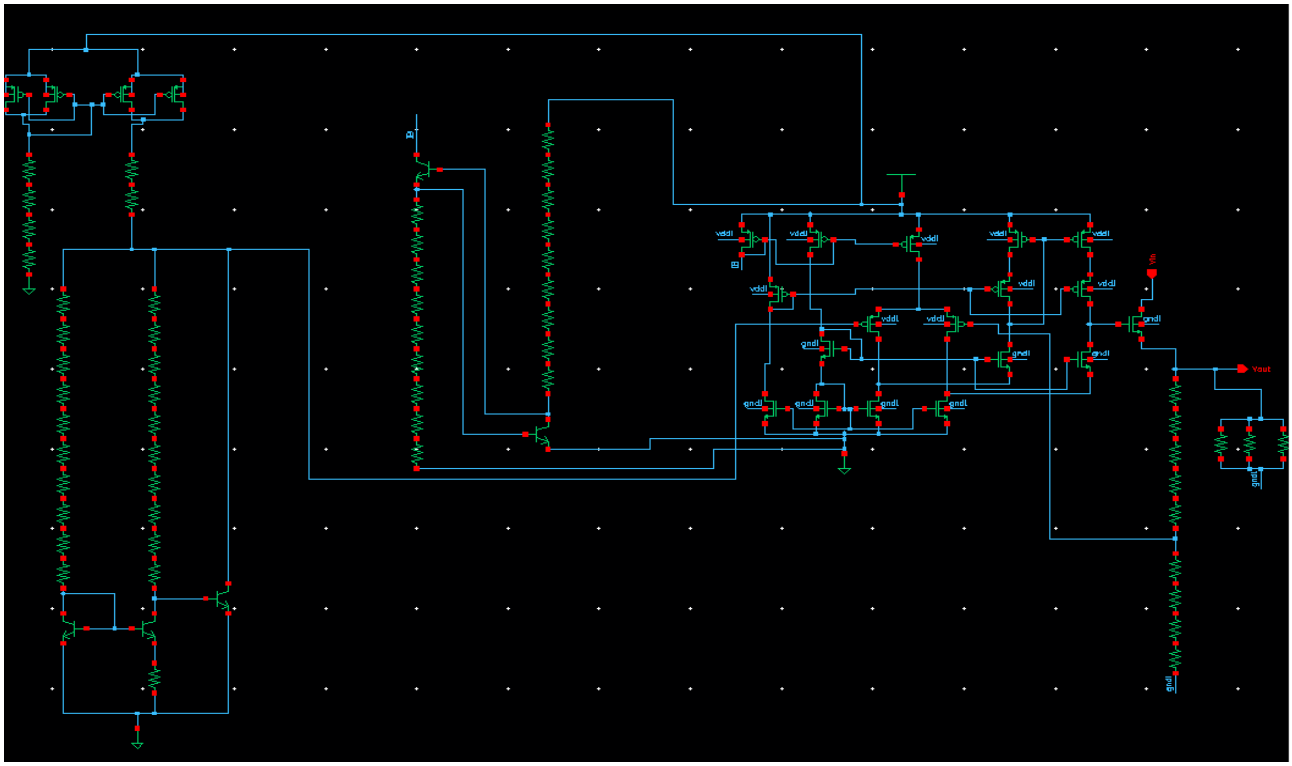

FIG 1

LAYOUT AND DESIGN RULE CHECK:

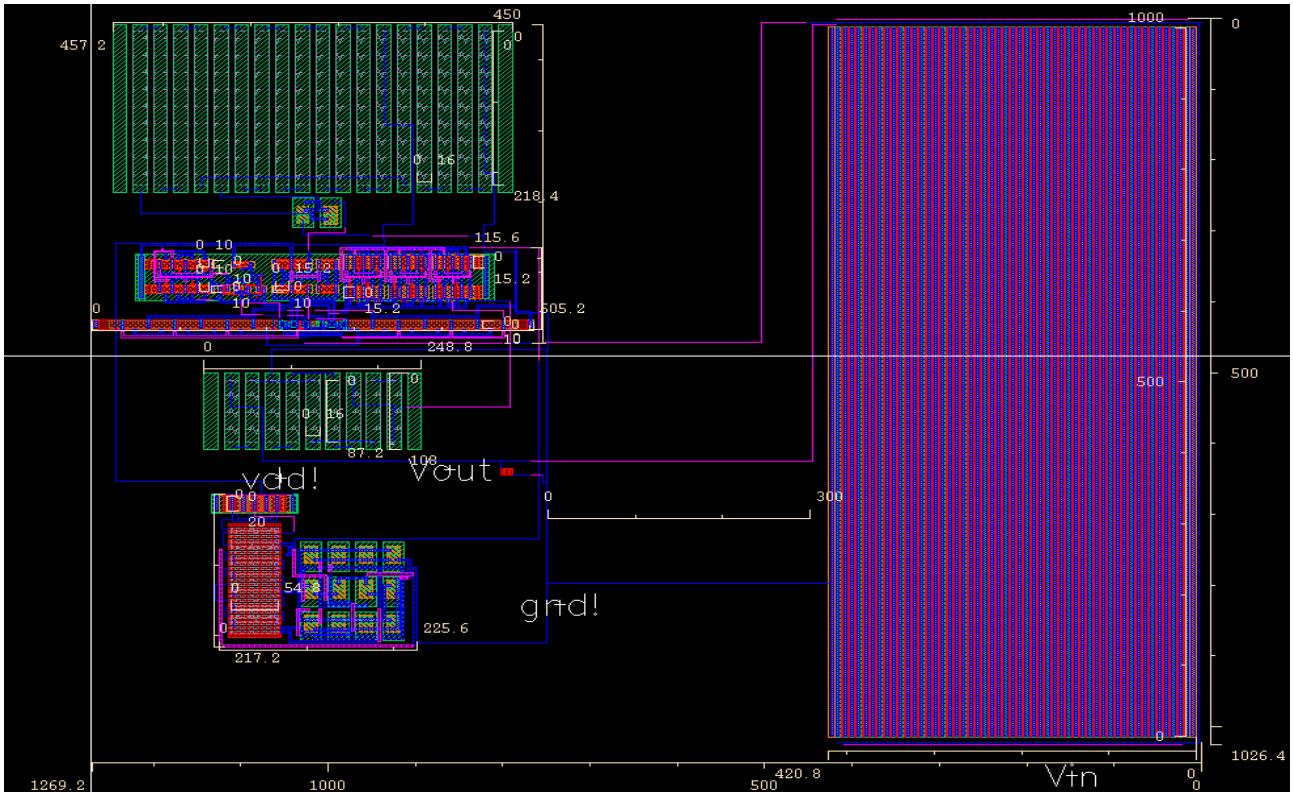

FIG 2

FIG 3

The total area covered by the layout is (1.2692 × 1.0264) mm = 1.302 mm^2

SCHEMATIC EXTRACTION:

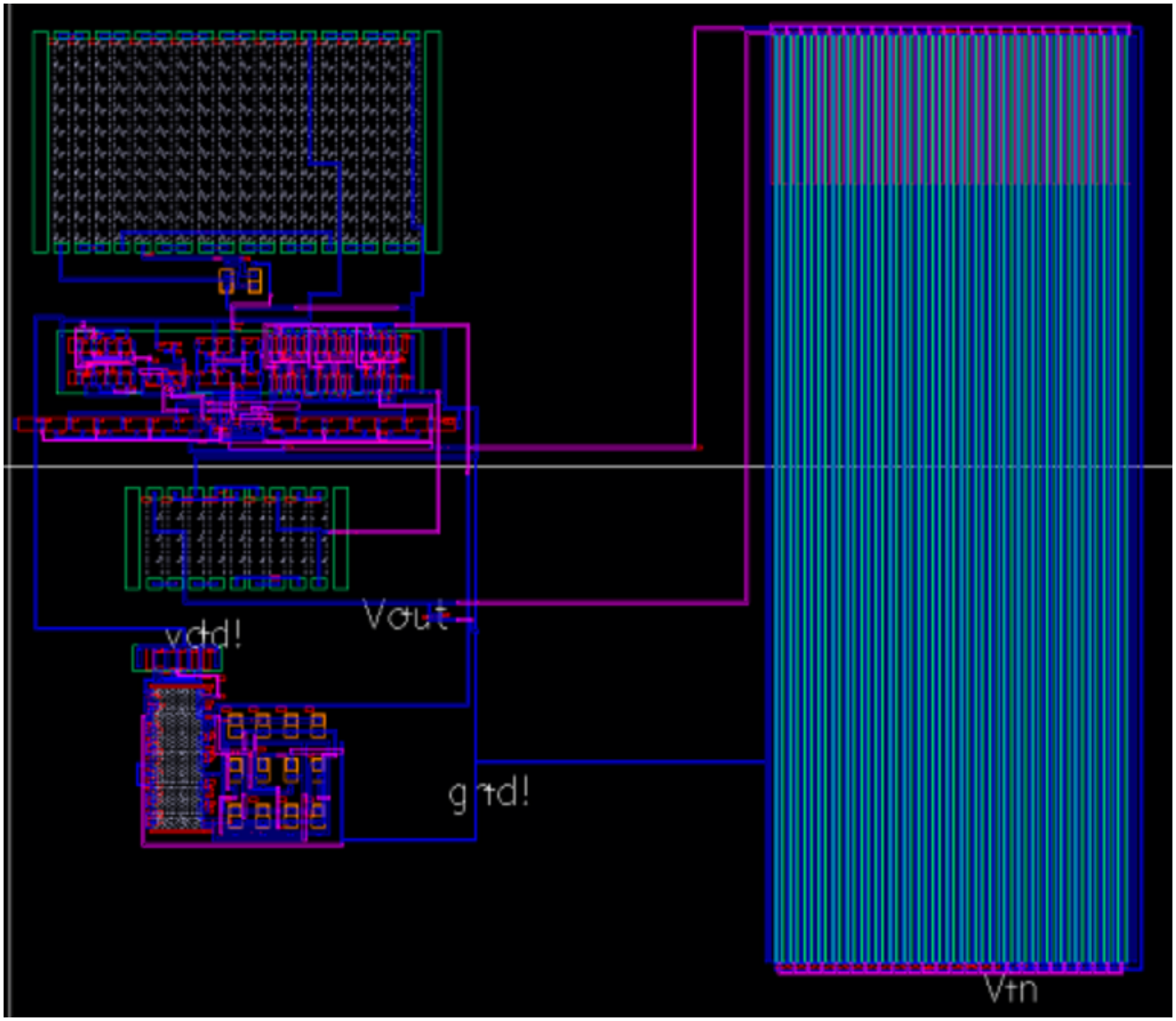

FIG 4

SCHEMATIC, LAYOUT DESIGN AND EXTRACTED OUTPUT OF EACH BLOCK:

Widlar Bandgap Reference

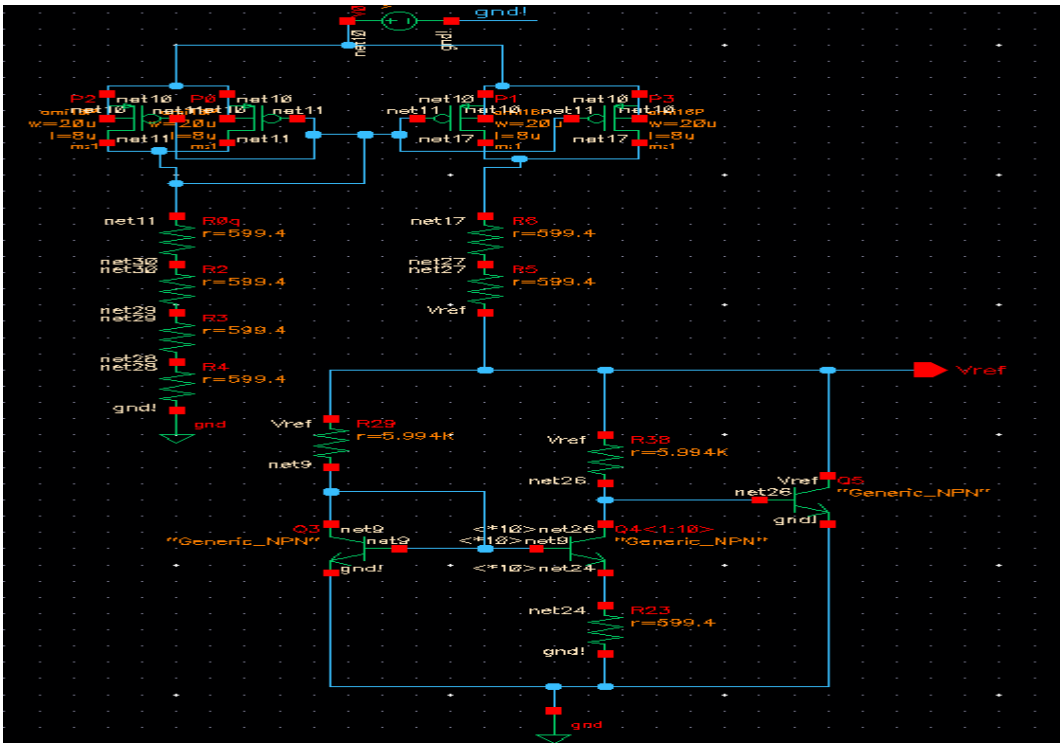

FIG 5

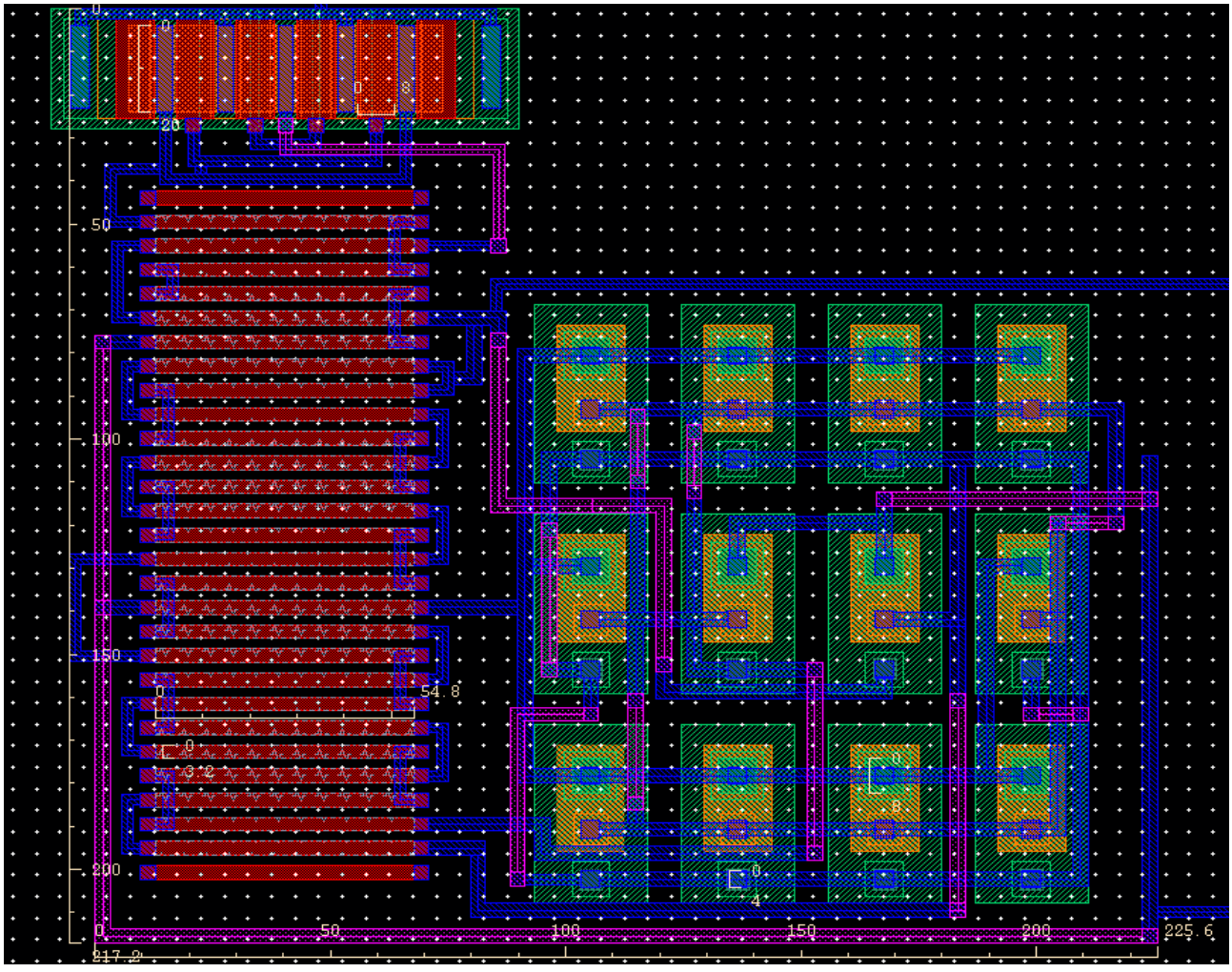

FIG 6

The total area covered by this block is (225.6 × 217.2) µm = 0.049 mm^2

PMOS current mirrors were used to generate the current of 300µA

Layout is drawn for moderate matching: BJT interdigitated pattern – ***T2 T2 T2 T2***
Resistors: **DBABABABABACABABABABABD** **T2 T1 T3 T2**
Resistors (PMOS current mirrors): **ABA|ABA** ***T2 T2 T2 T2***
PMOS interdigitated pattern: $_S\mathbf{A_D B_S B_D A_S}$

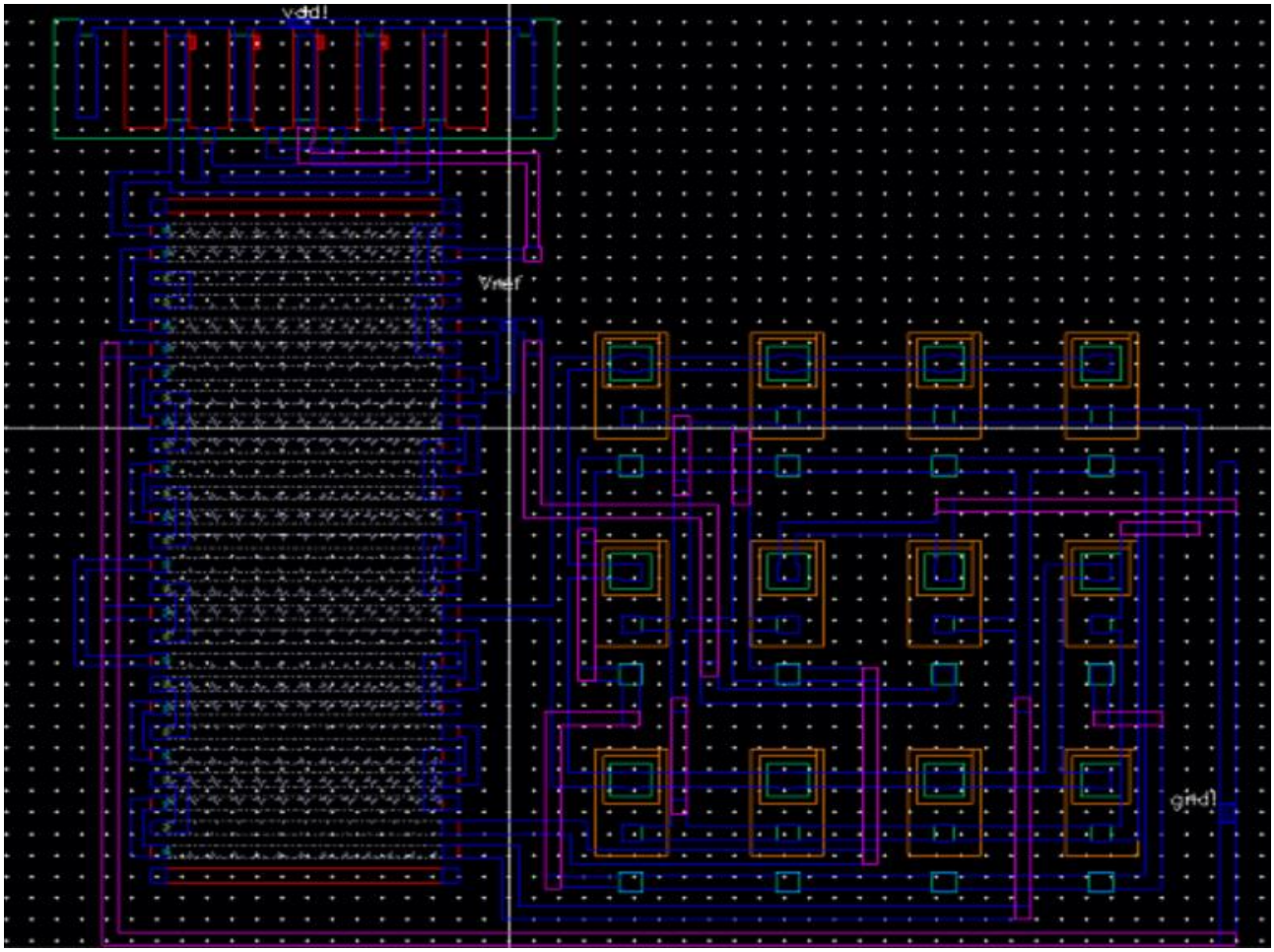

FIG 7

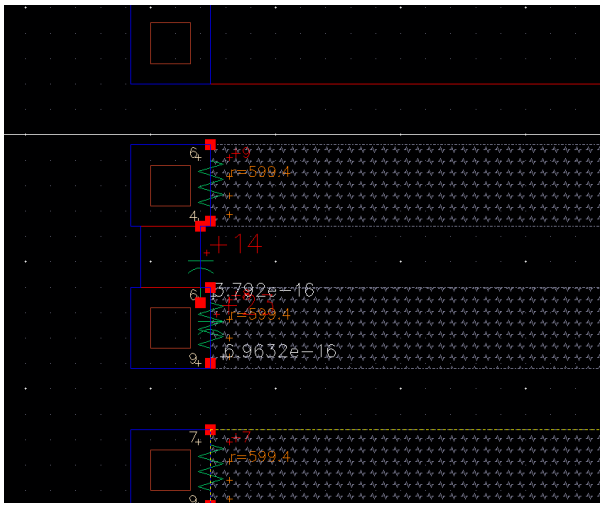

FIG 8

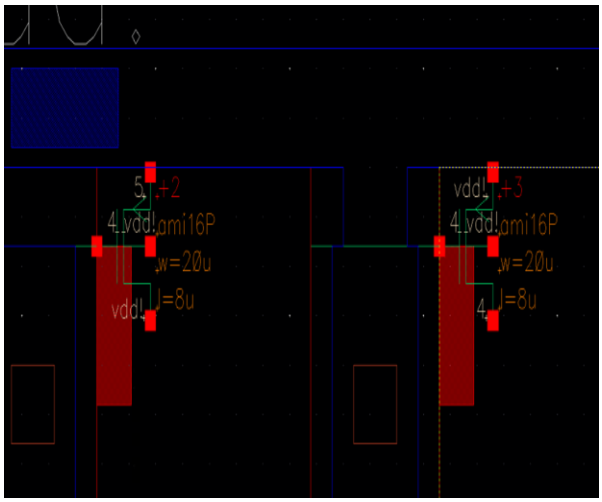

FIG 9

Error Amplifier

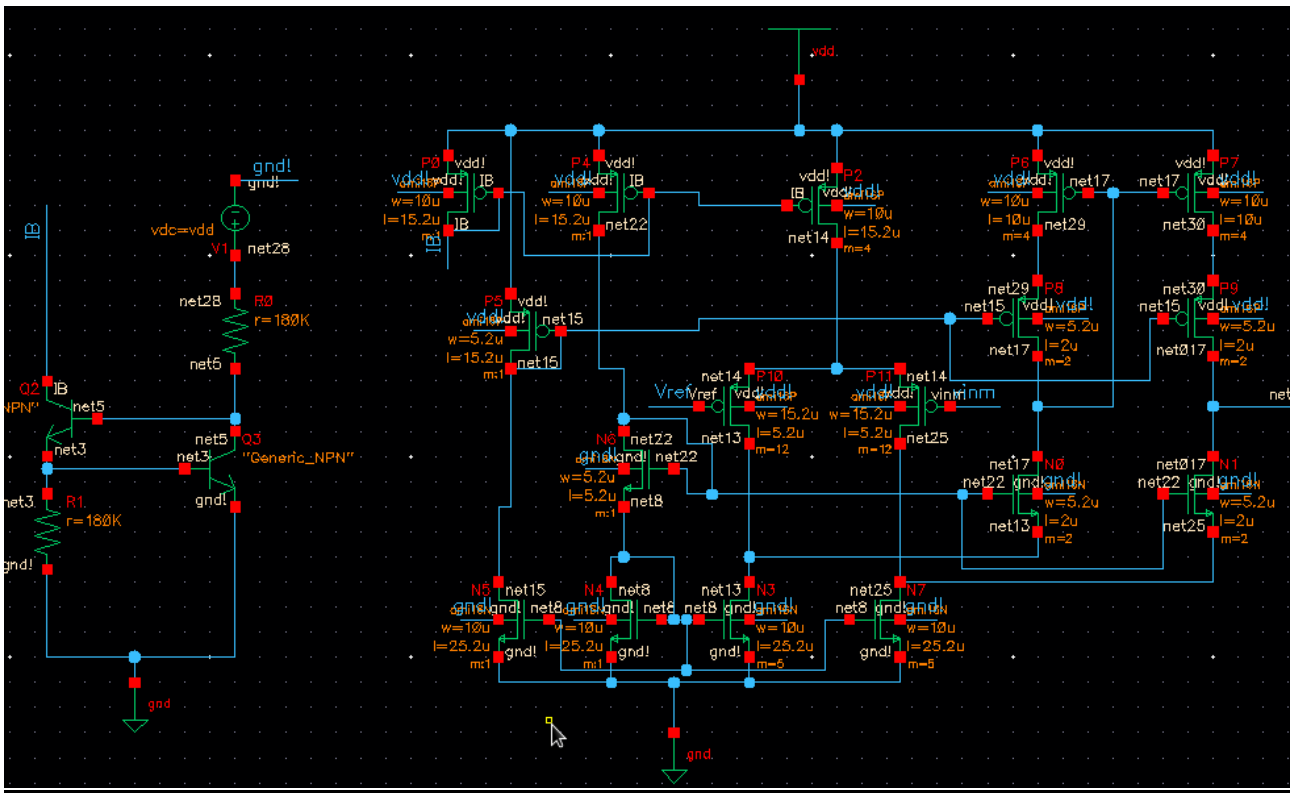
vdd!
gnd!
vdc=vdd
V1
net28
R0
r=180K
net5
Q2
"NPN"
IB
net3
Q3
"Generic_NPN"
R1
r=180K
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
N0
N1
N2
N3
N4
N5
N6
N7
w=10u
l=15.2u
m=1
m=4
w=5.2u
l=5.2u
m=12
w=10u
l=1u
m=4
w=5.2u
l=2u
m=2
w=10u
l=25.2u
m=5
net22
net8
net15
net14
net13
net25
net17
net29
net30
net017
net1
Vref
vinm
vinn

FIG 10

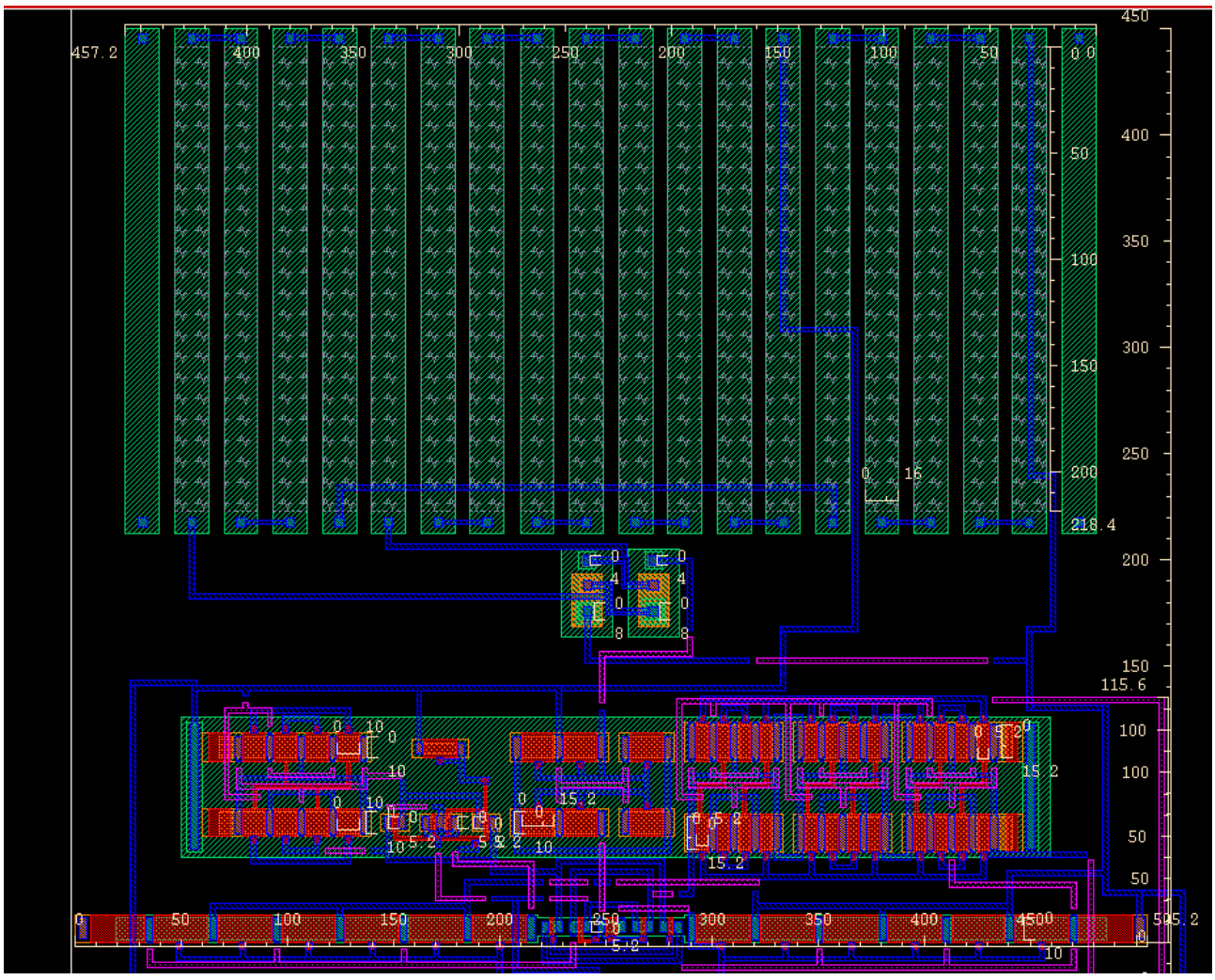
457.2
400
350
300
250
200
150
100
50
0
450
400
350
300
250
200
150
100
50
0
218.4
115.6
15.2
525.2

FIG 11

The total area covered by this block is (505.2 × 450) µm = 0.22734 mm^2

Common-centroid layout interdigitated pattern:

MP1(A), MP2(B), MP3(C):

$_DC_SA_D\ _SC_D$

$_DC_SB_D\ _SC_D$

MP4(A), MP5(B):

$_DA_SB_DB_SA_D$

$_DB_SA_DA_SB_D$

$_DA_SB_DB_SA_D$

$_DB_SA_DA_SB_D$

$_DA_SB_DB_SA_D$

$_DB_SA_DA_SB_D$

$_DA_S\ _DB_{SS}B_D\ _SA_D$

MP7(A), MP8(B):

$_DA_S\ _DB_{SS}B_D\ _SA_D$

MP7(A), MP8(B):

$_DA_S\ _DB_{SS}B_D\ _SA_D$

MP9(A), MP10(B):

$_DA_SB_DB_SA_D$

$_DB_SA_DA_SB_D$

MN2(A), MN3(B):

$_SA_D\ _SB_SB_S\ _DA_S$

MN4(A), MN5(B), MN6(C), MN7(D):

CDDC

DACD

CBB

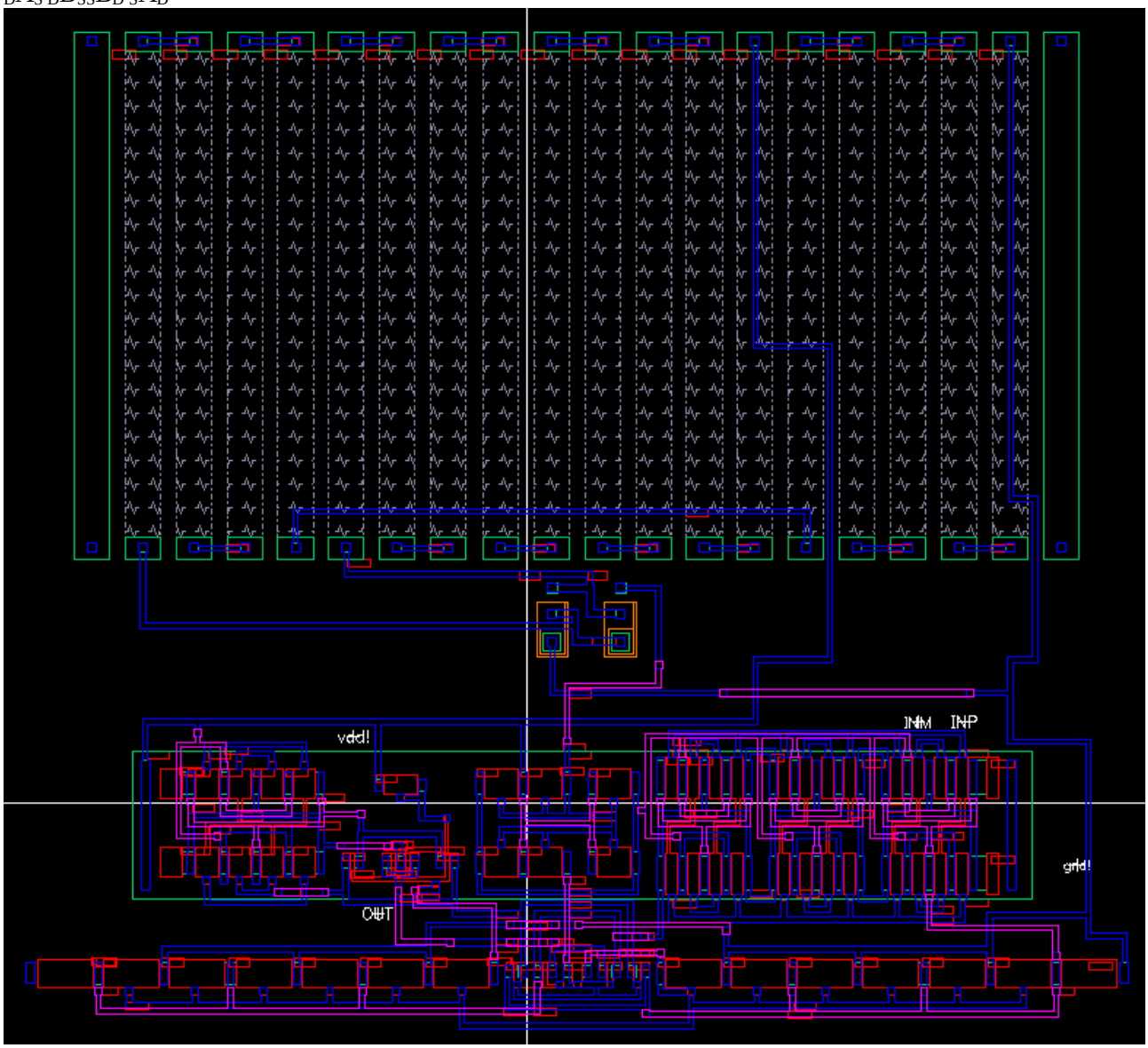

FIG 12

Feedback Resistors and the external load resistor

Common-centroid layout interdigitated pattern for the resistors:

Resistors(Feedback):R2(B)- 40k Ω, R1(A)- 32k Ω **BBAABAABB** (Each segment equivalent to 8k Ω; W-16µm, L- 87.2 µm)

Load Resistor: 10Ω = 3 segments **AAA** = 30Ω each (W=3.2 µm, L= 2.8 µm)

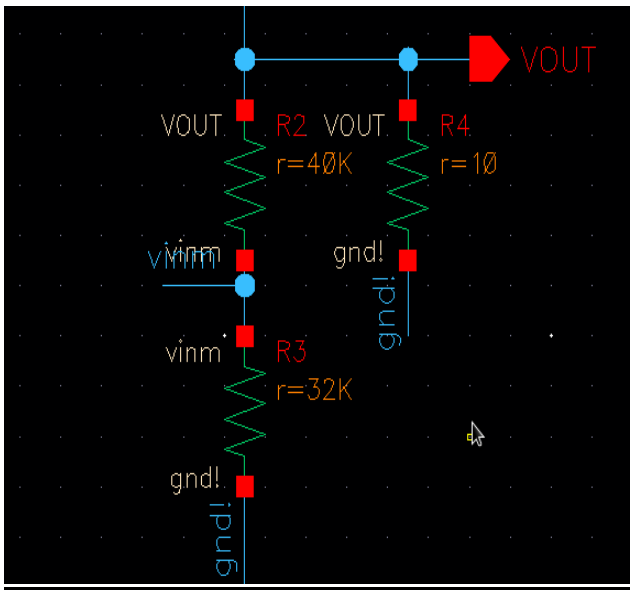

FIG 13

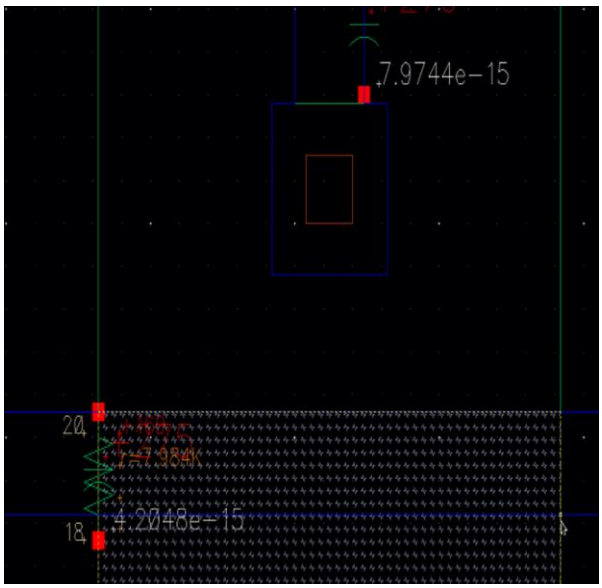

FIG 14

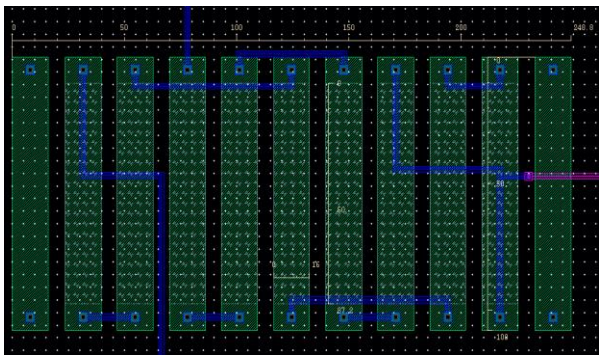

FIG 15

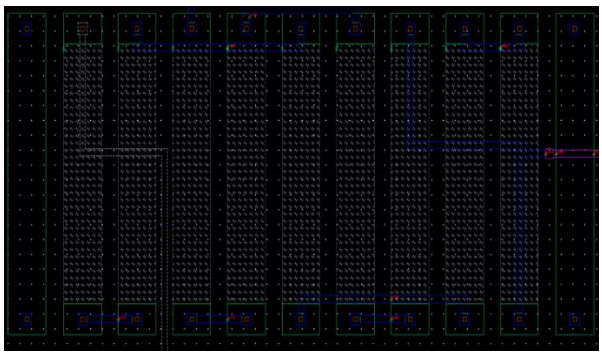

FIG 16

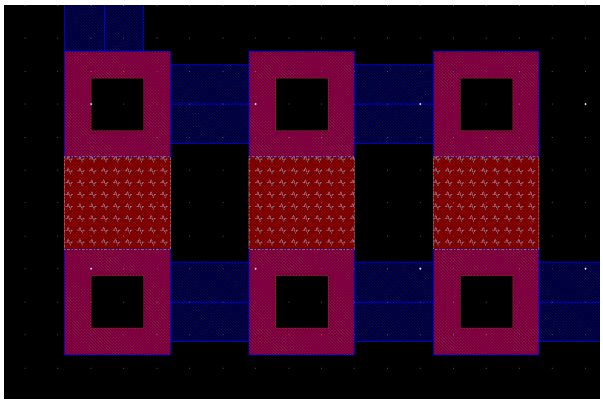

FIG 17

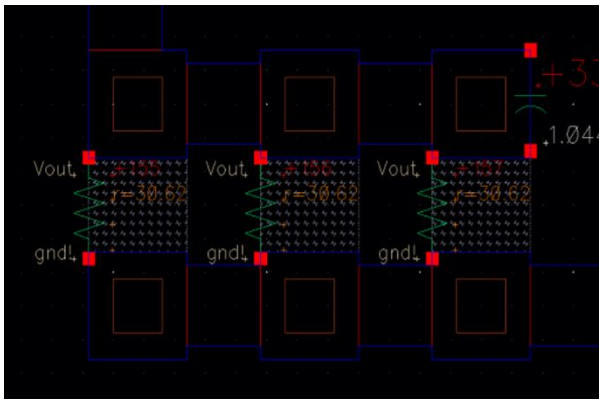

FIG 18

The total area covered by the feedback resistor block is (248.8 × 108) µm = 0.0268704 mm^2

R2 and R1 values are chosen to be big enough to kill the current which satisfies the following specification of standby current < 0.1mA and also to reduce load on the power transistor, so that a smaller (W/L) ratio can be used which saves area. The ratio is also maintained;

$$V_{out} = V_{ref}\,(R_1+R_2)/R_1;$$

$$2.6 = 1.2\,(32k\,\Omega + 40k\,\Omega)/32k\,\Omega$$

NMOS Power Pass Transistor

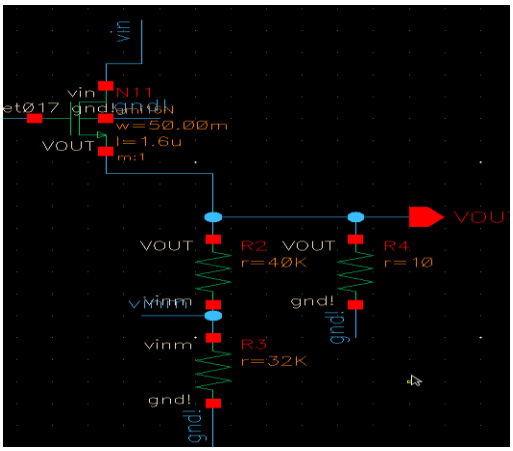

FIG 19

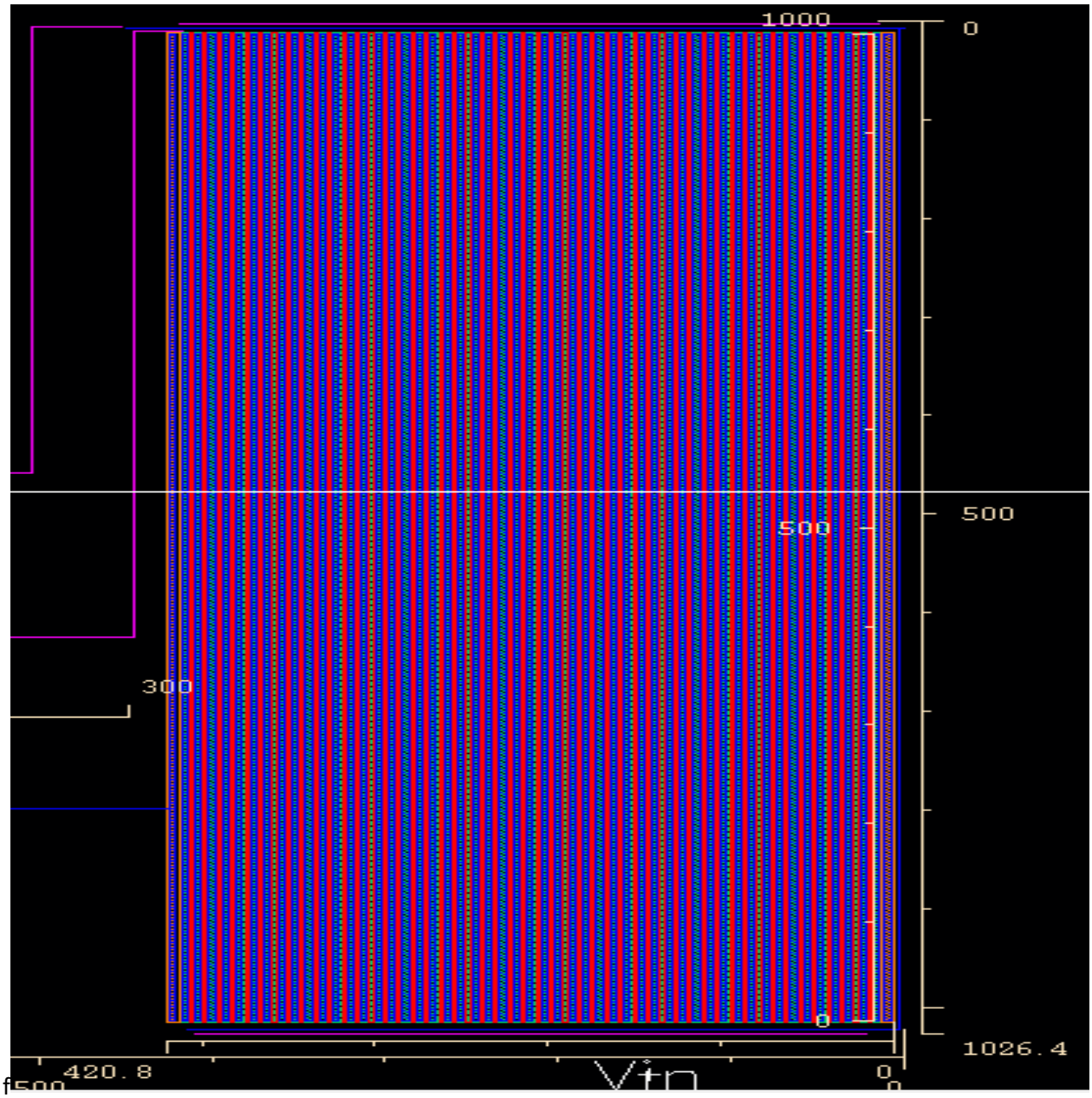

FIG 20

The total area covered by this block is (420.8 × 1026.4) µm = 0.431909 mm^2

Interdigitated pattern: (A: W/L= 1mm/1.6 µm) 50 fingers

$_S A_D A_S$
$A_D A_S A_D A_S A_D A_S A_D A_S A_D A_S A_D A_S$

FIG 21

LAYOUT, DESIGN RULE CHECK AND EXTRACTED IMAGE OF LDO IN THE PAD FRAME:

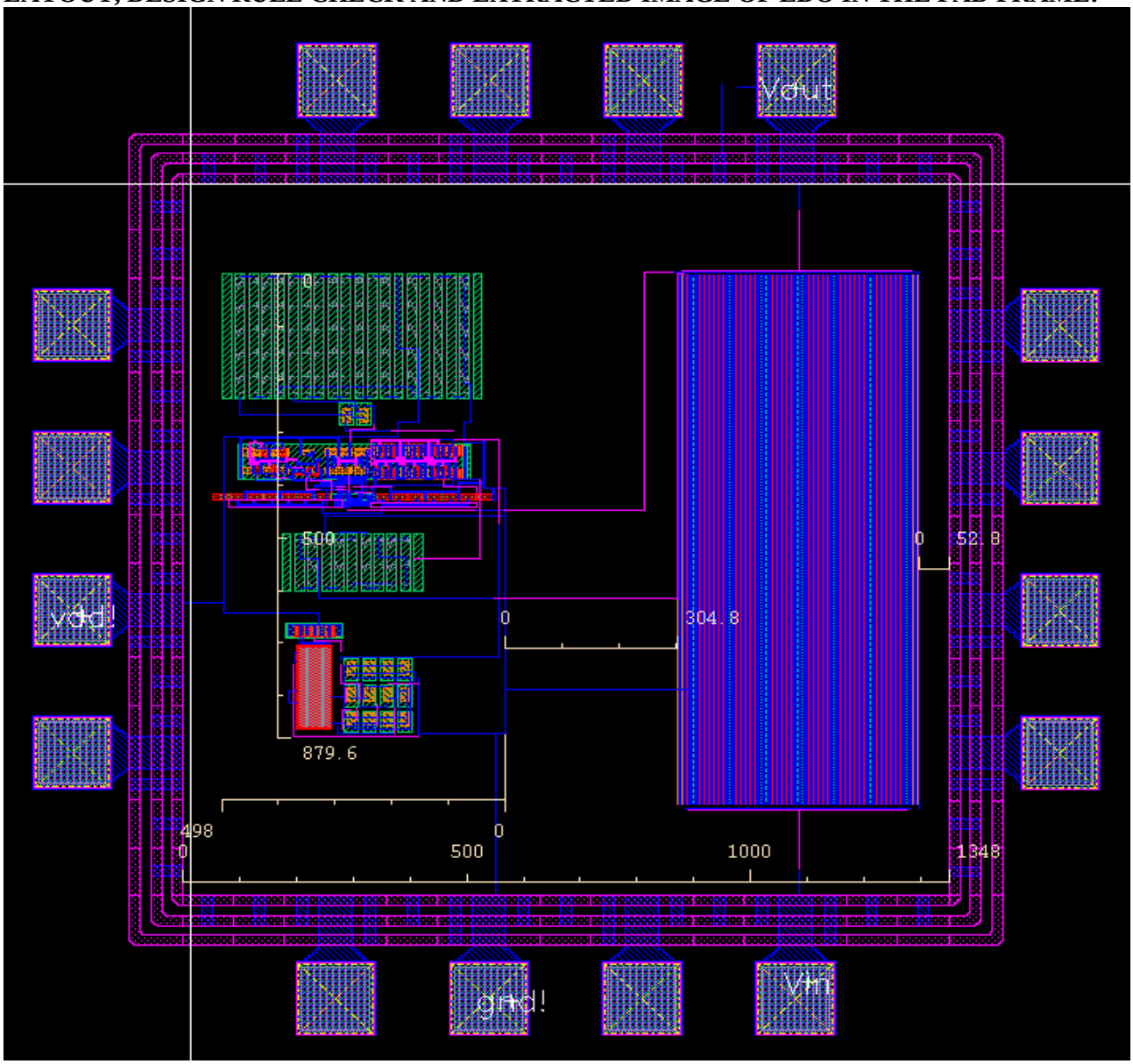

FIG 22

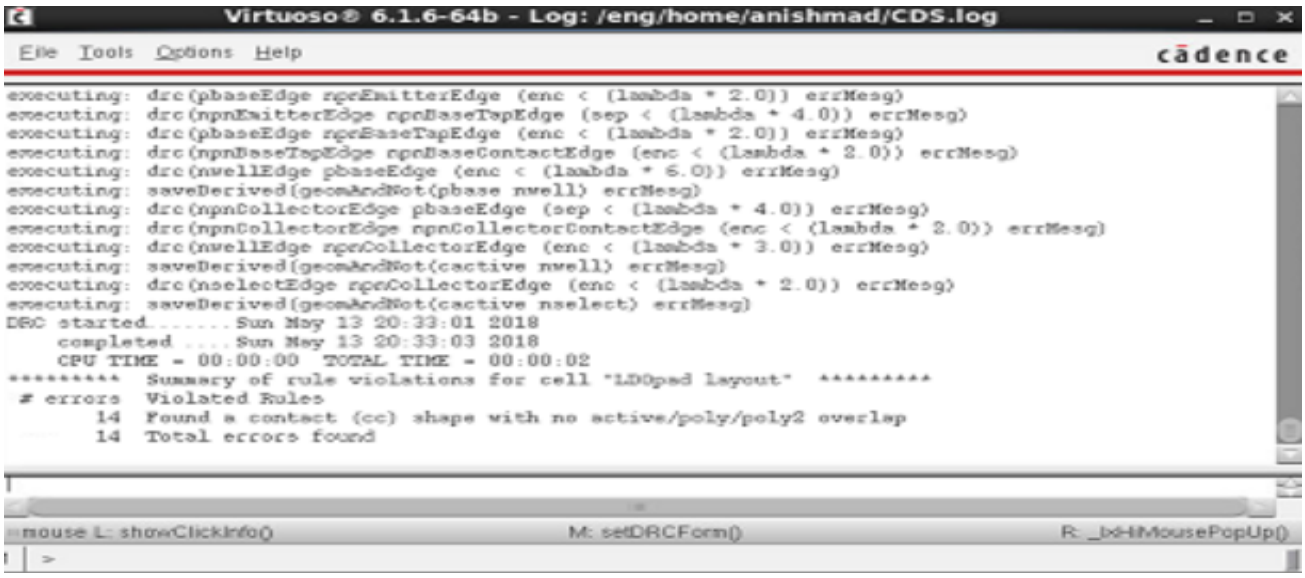

FIG 23

The power pass transistor is placed at least 300µm apart (304.8 µm) from the rest of the circuit and placed 52.8 µm from the pad frame to protect the circuit from thermal runaway/breakdown. **The area inside the pad frame is 1348µm × 1348 µm. The total area covered by the regulator inside the layout is (1.2692 × 1.0264) mm = 1.302 mm^2**

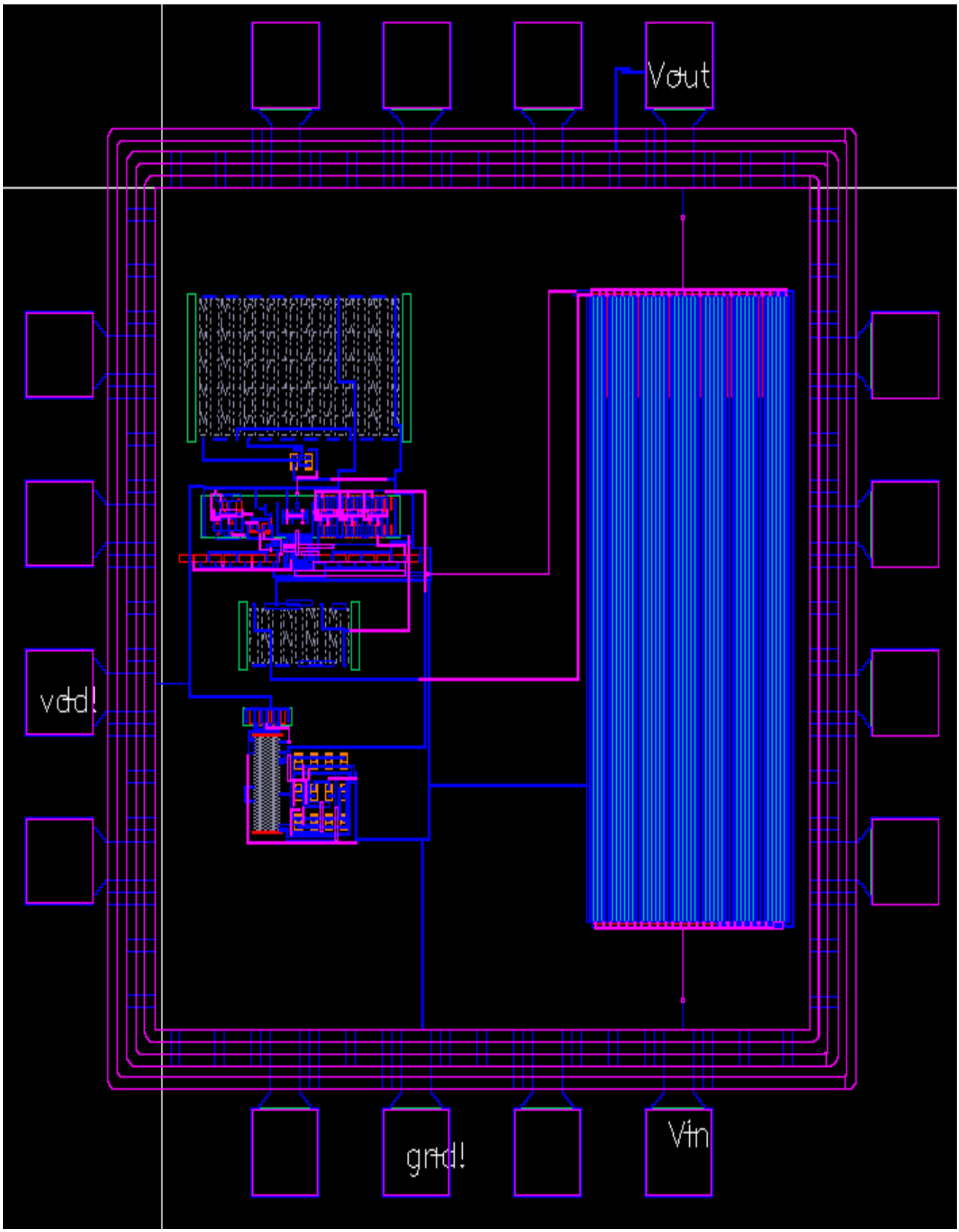

FIG 24

LAYOUT VS SCHEMATIC

/eng/home/anishmad/Desktop/LVS/si.log

File Edit View Help cadence

```
End netlist:     May 12 10:54:49 2018

Moving original netlist to extNetlist
Removing parasitic components from netlist
            presistors removed:  0
            pcapacitors removed: 261
            pinductors removed:  0
            pdiodes removed:     0
            trans lines removed: 0
            110 nodes merged into 110 nodes


Begin netlist:     May 12 10:54:49 2018
            view name list         = ("auLvs" "schematic")
            stop name list         = ("auLvs")
            library name           = "Project"
            cell name   = "LDO"
            view name   = "schematic"
            globals lib = "basic"
Running Artist Flat Netlisting ...
*WARNING* (icLic-3) Could not get license Virtuoso_Layout_Suite_L
*WARNING* (icLic-21) License Virtuoso_Layout_Suite_L ("Layout L") is not available to run Layout L.
Trying to check out the license Virtuoso_Layout_Suite_XL ("Layout XL") instead.
*WARNING* (icLic-3) Could not get license Virtuoso_Layout_Suite_XL
*WARNING* (icLic-21) License Virtuoso_Layout_Suite_XL ("Layout XL") is not available to run Layout L.
Trying to check out the license Virtuoso_Layout_Suite_GXL ("Layout GXL") instead.
*INFO* (icLic-25) License Virtuoso_Layout_Suite_GXL ("Layout GXL") was used to run Layout L.
End netlist:     May 12 10:54:50 2018

Moving original netlist to extNetlist
Removing parasitic components from netlist
            presistors removed:  0
            pcapacitors removed: 0
            pinductors removed:  0
            pdiodes removed:     0
            trans lines removed: 0
            71 nodes merged into 71 nodes

Running netlist comparison program:  LVS
Begin comparison:     May 12 10:54:50 2018
@(#)$CDS: LVS version 6.1.6-64b 10/30/2014 21:55 (sjfbm191) $

10 net-list ambiguities were resolved by random selection.

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   182     90
        total                    182     90

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   69      69
        total                    69      69

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    4       4
```

FIGURE: LVS

SIMULATION RESULT OF VOUT:

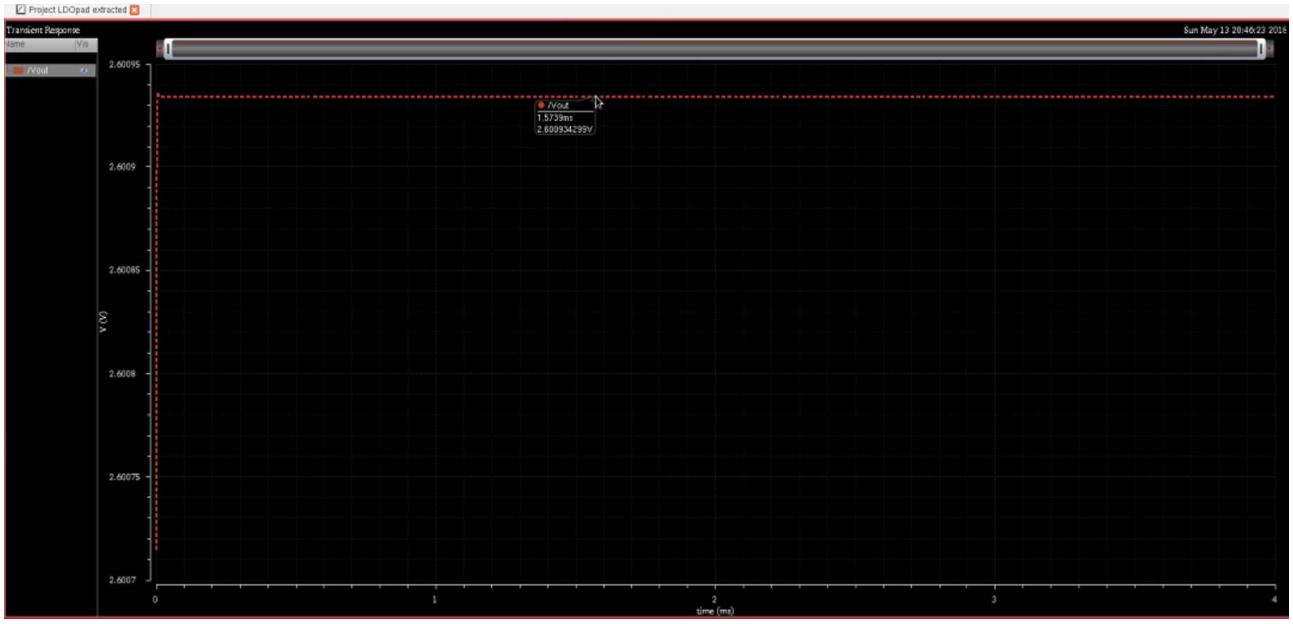

FIG 25

Fig 25: **Transient response of V_{out} of the regulator from the pad frame with load connected - V_{out} = 2.6 V**

Simulation results to find (W/L) = (50mm/1.6µm)

Considering current driving capability, output voltage with and without load and power handling capability. Fig 26: **Output voltage vs W (V = 2.5 to 2.6)**, Fig 27: **Current with load (10Ω) vs W = 254mA**, Fig 28: **Current without load (Standby Current) vs W = 37.4µA at 50mm**

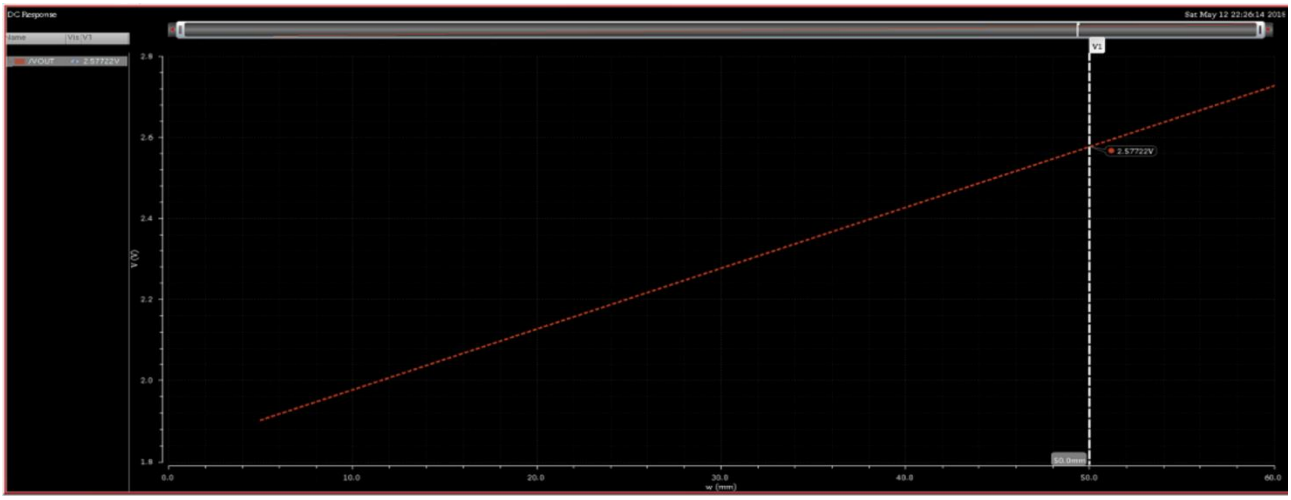

FIG 26

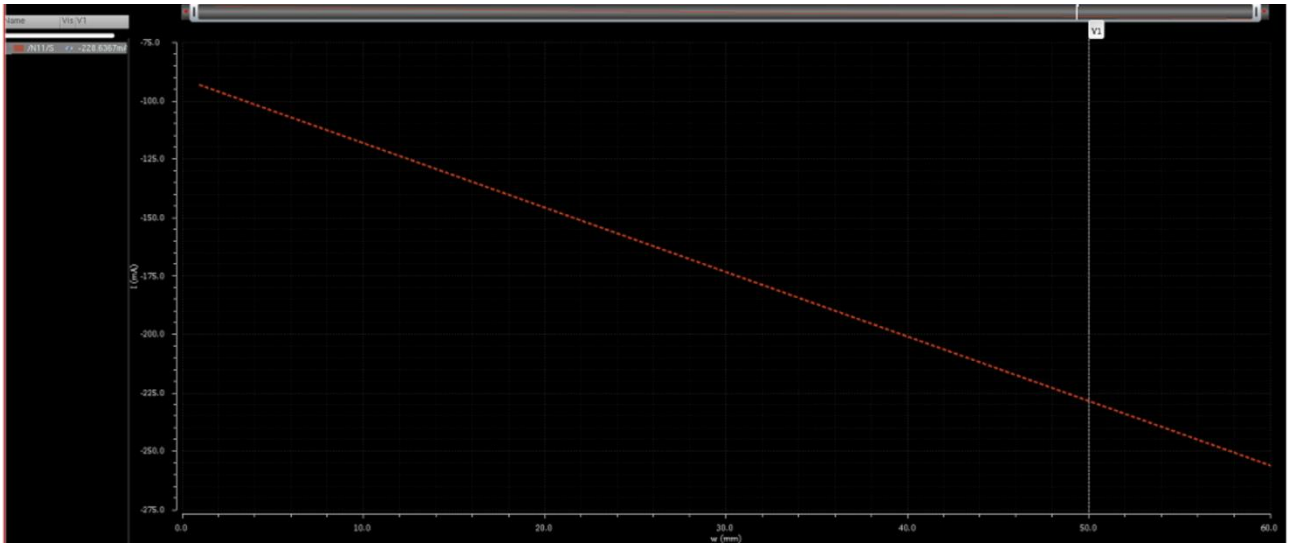

FIG 27

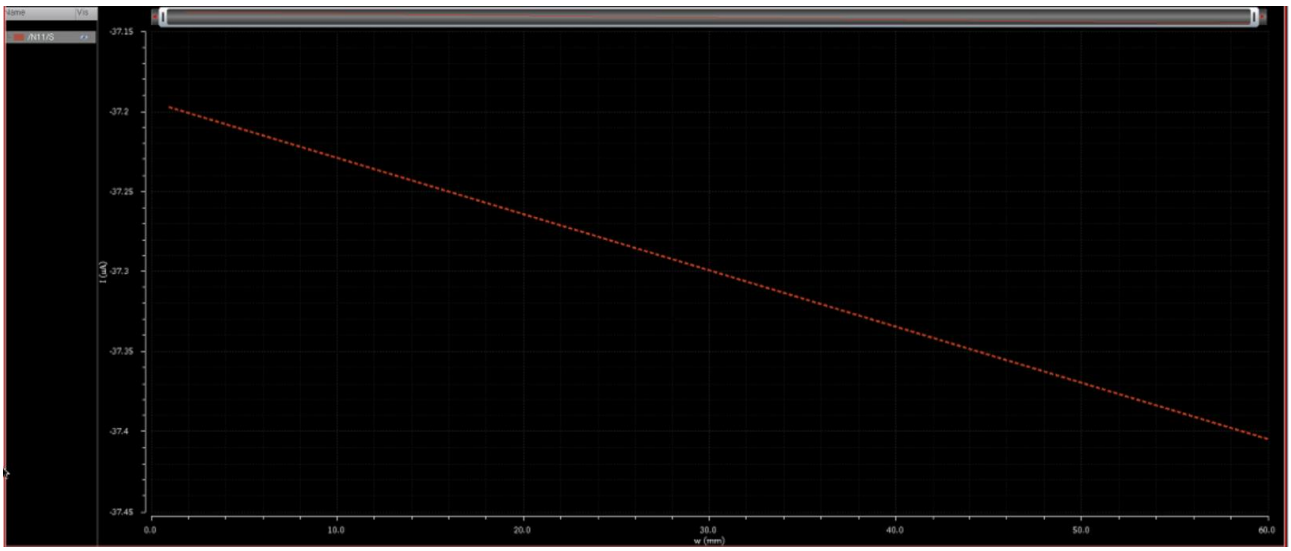

FIG 28

Simulation results of Widlar Bandgap reference used in the regulator:

Fig 29: **Transient response of V_{ref} in the regulator**, Fig 30: **V_{ref} with respect to temperature (-50ºC – 100 ºC) – Average V_{ref} = 1.201 V**

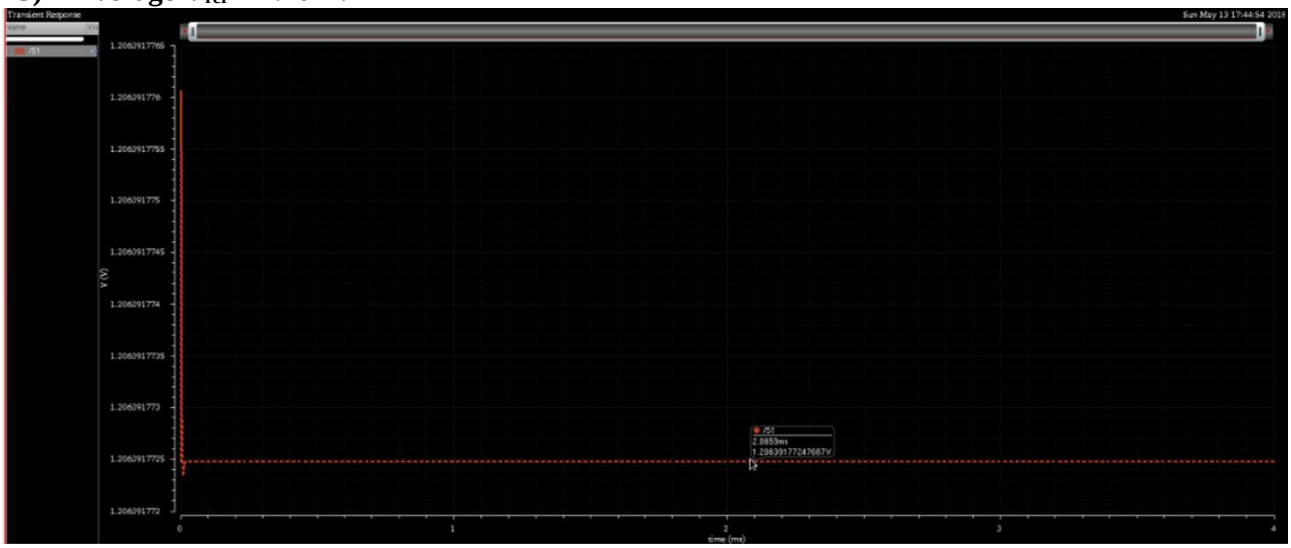

FIG 29

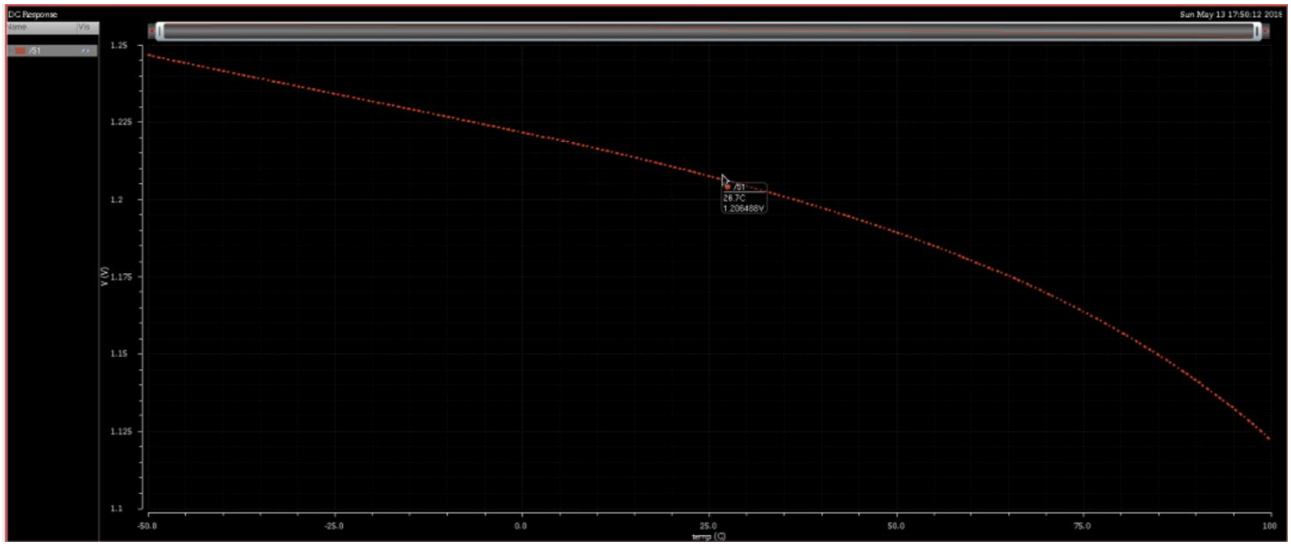

FIG 30

Simulation results with respect to the power pass transistor used in the regulator:

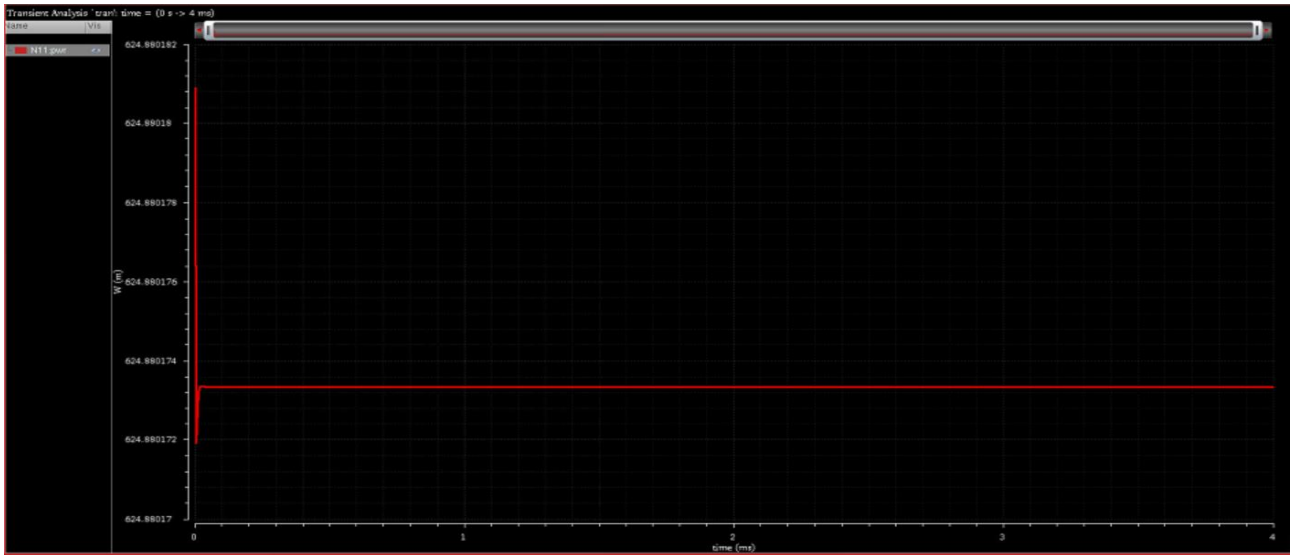

FIG 31

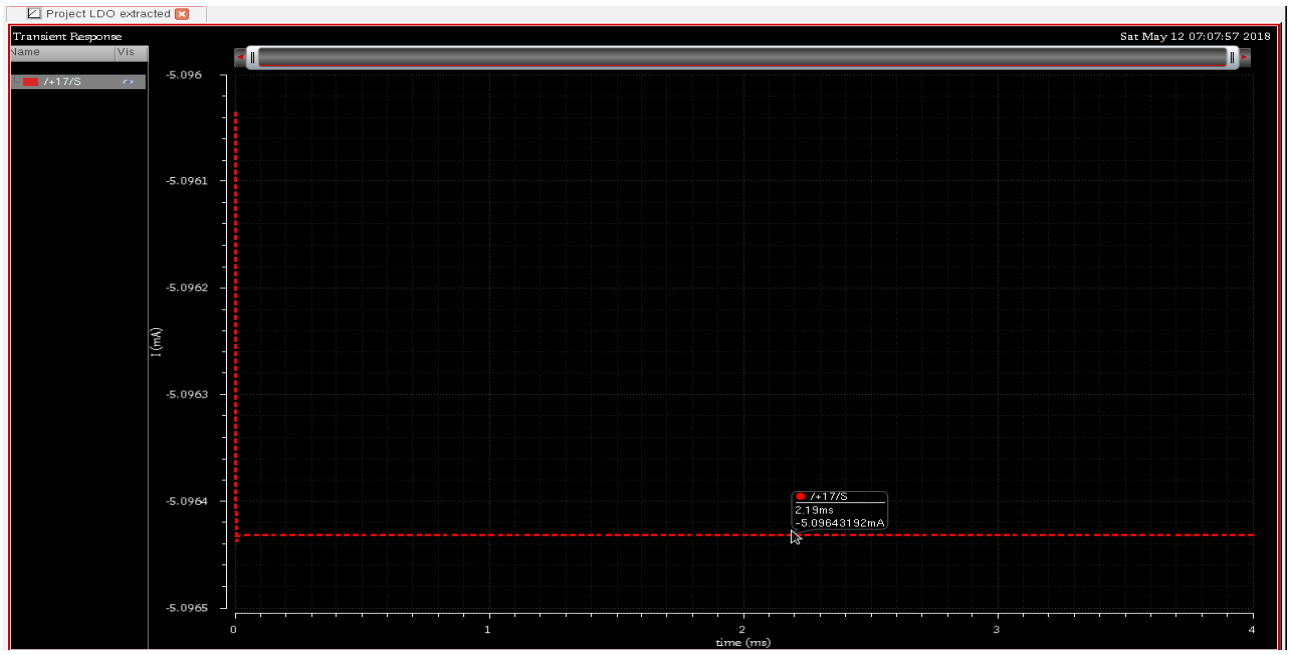

FIG 32

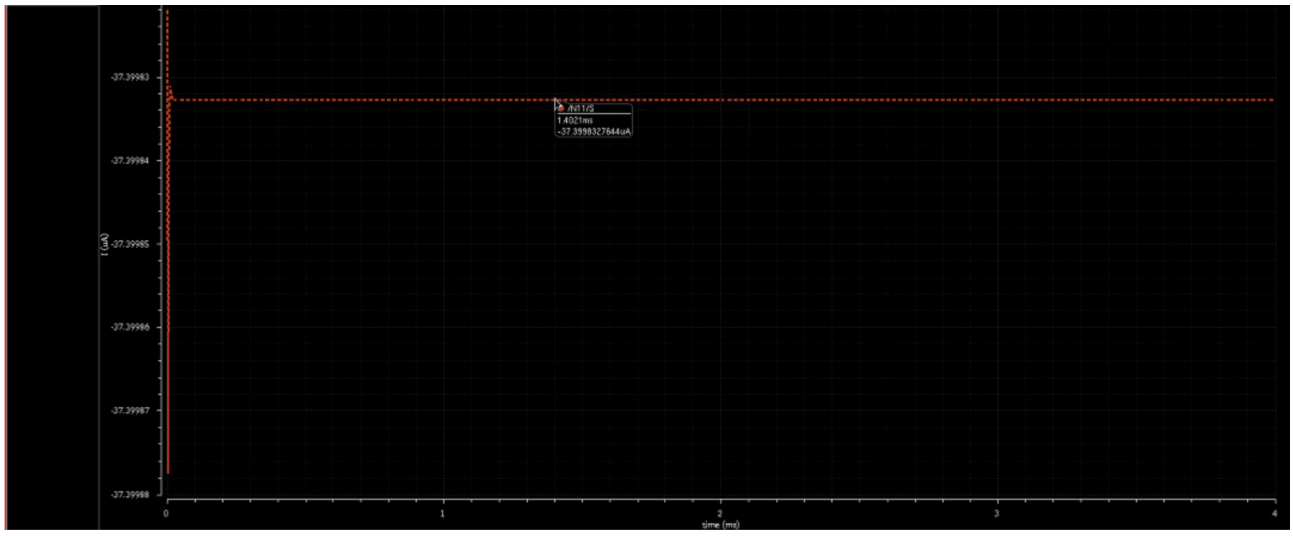

FIG 33

Fig 31: **Transient response with respect to handling power**
Fig 32: **Transient response with respect to handling load current from one node of the power pass transistor (1 mm) – 5.0964 mA, so for 50 nodes (50 mm) – 5.0964 mA × 50**
Fig 33: **Transient response of the power pass transistor's current without load (Standby Current)**

Table below shows the specifications met by the power pass transistor.

Power Handling	**624.8 mW**
Current Handling	**254.8215 mA**
Standby Current	**37.4µA**

Power dissipated by T1:

$$P_d = I\ (V_{in} - V_{out})$$
$$P_d = 254.8215\ (5 - 2.6)$$
$$\mathbf{P_d = 611\ mW}$$

LINE REGULATION (dV_{OUT}/dV_{IN})

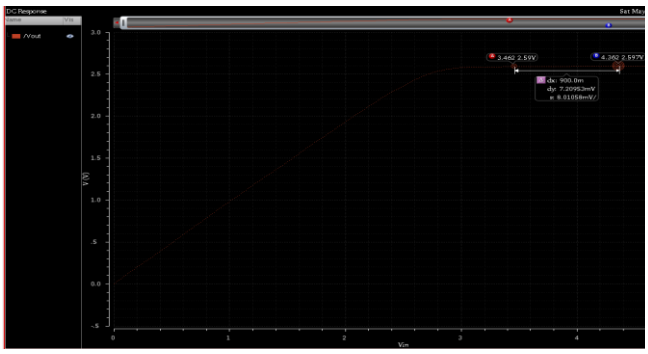

FIG 34

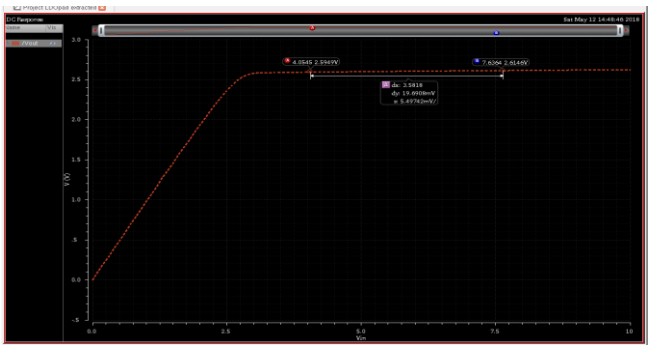

FIG 35

Fig 34 and Fig 35: **Shows the rate of change of Vout with respect to Vin,** it can be observed that a Vin of 2.8V is required for the circuit to be operated in the regulated region.
Fig 36: Shows $\mathbf{dV_{out}/dV_{in}}$ in the regulated region.

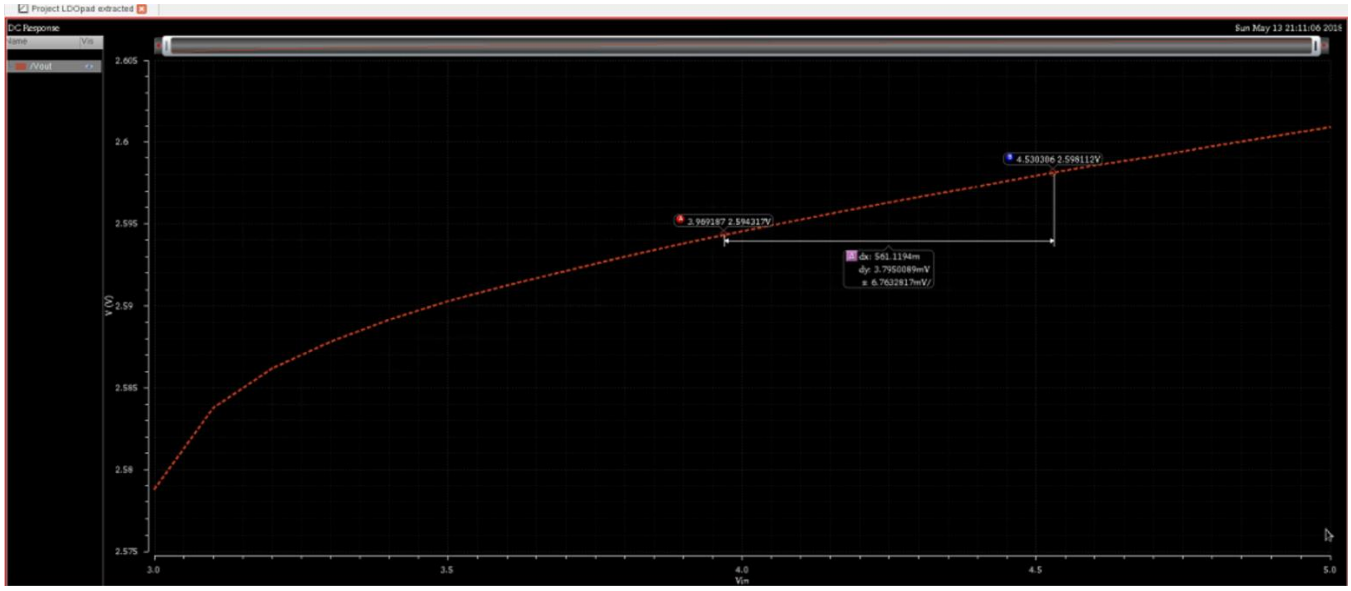

FIG 36

The rate of change of output with respect to the input is $\mathbf{dV_{out}/dV_{in}}$ = 6.76mV/V

LOAD REGULATION ($\mathbf{dV_{OUT}/dV_{IN}}$)

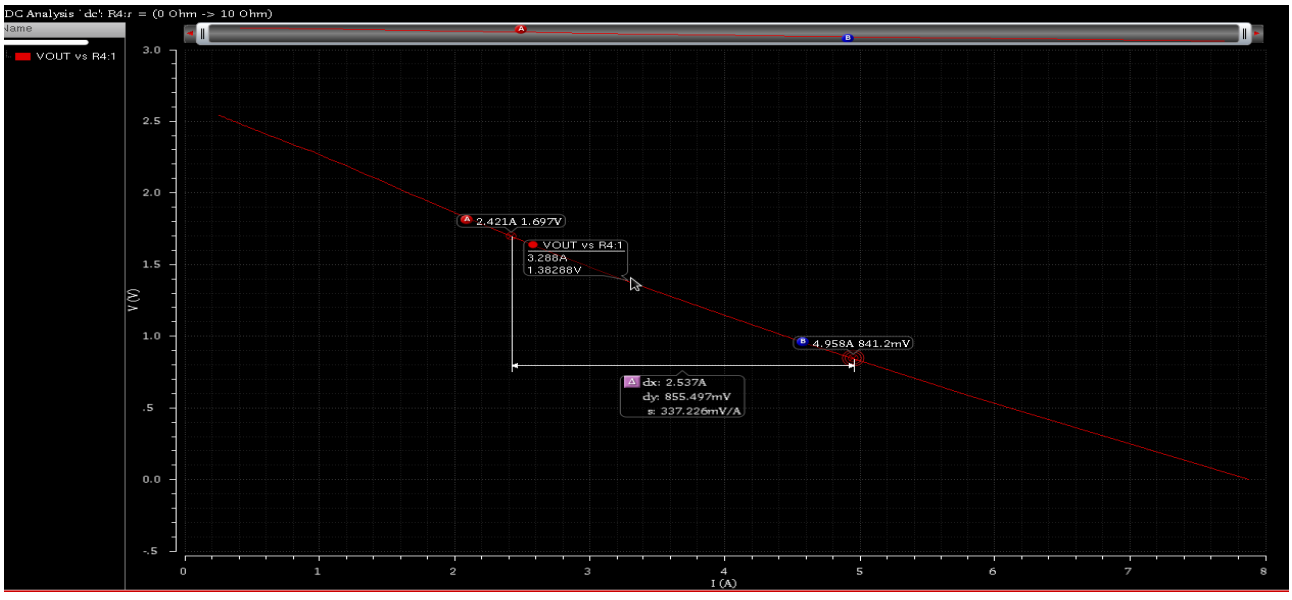

FIG 37

Fig 37: Shows $\mathbf{dV_{out}/dI_L}$ of the circuit varying beyond the load(0 – 10 Ω), from this plot the $\mathbf{dV_{out}/dI_L}$ is **337mV/A**, however we are interested in this circuit which is operated with a maximum of an assumed load of 10 Ω, the figure below shows the variation of the output with respect to this load.

Fig 38: Shows the actual load regulation of the circuit,

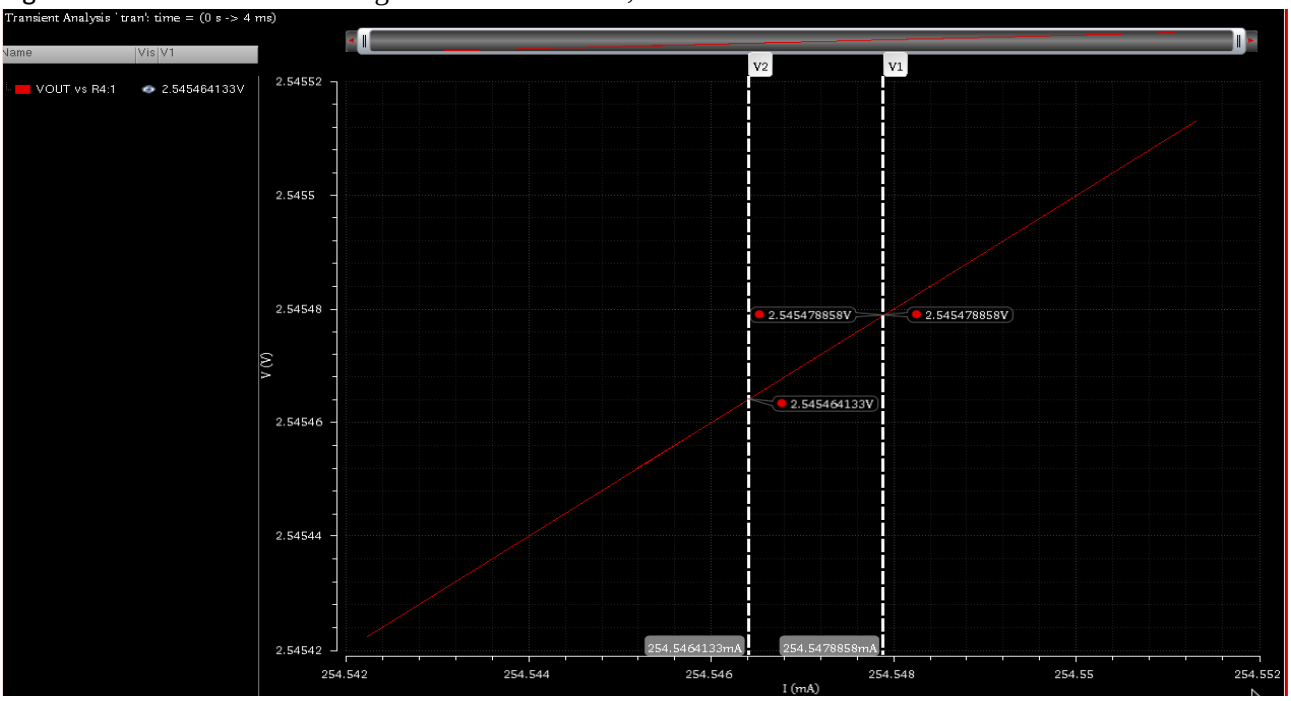

FIG 38

The rate of change of output with respect to the load is $\mathbf{dV_{out}/dI_L}$ = 10mV per milliamps

$\mathbf{V_{OUT}}$ vs TEMPERATURE (-30°C to 100°C)

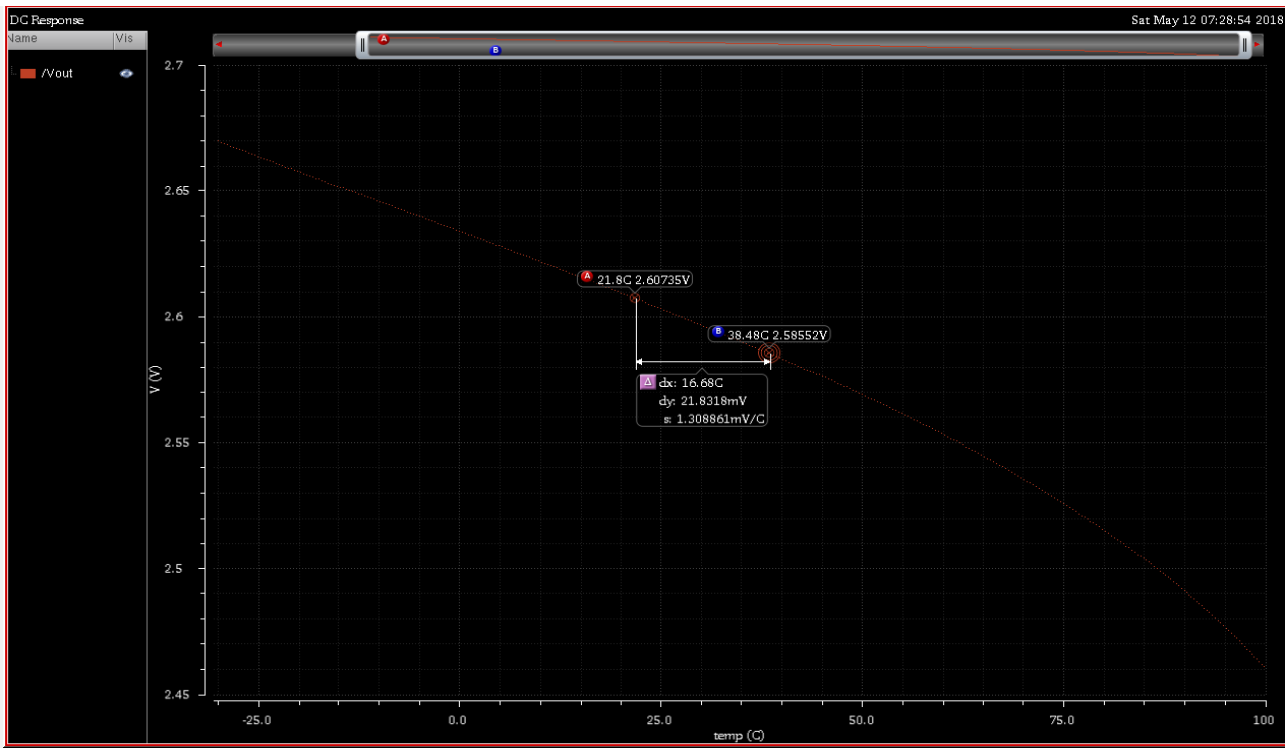

FIG 39

The rate of change of output with respect to the temperature is $\mathbf{dV_{out}/dTemp}$ = 1.3mV/°C

DROPOUT VOLTAGE (V_{IN} - V_{OUT})

Dropout voltage can be defined as the minimum difference between the input and output voltage where the circuit ceases to regulate.

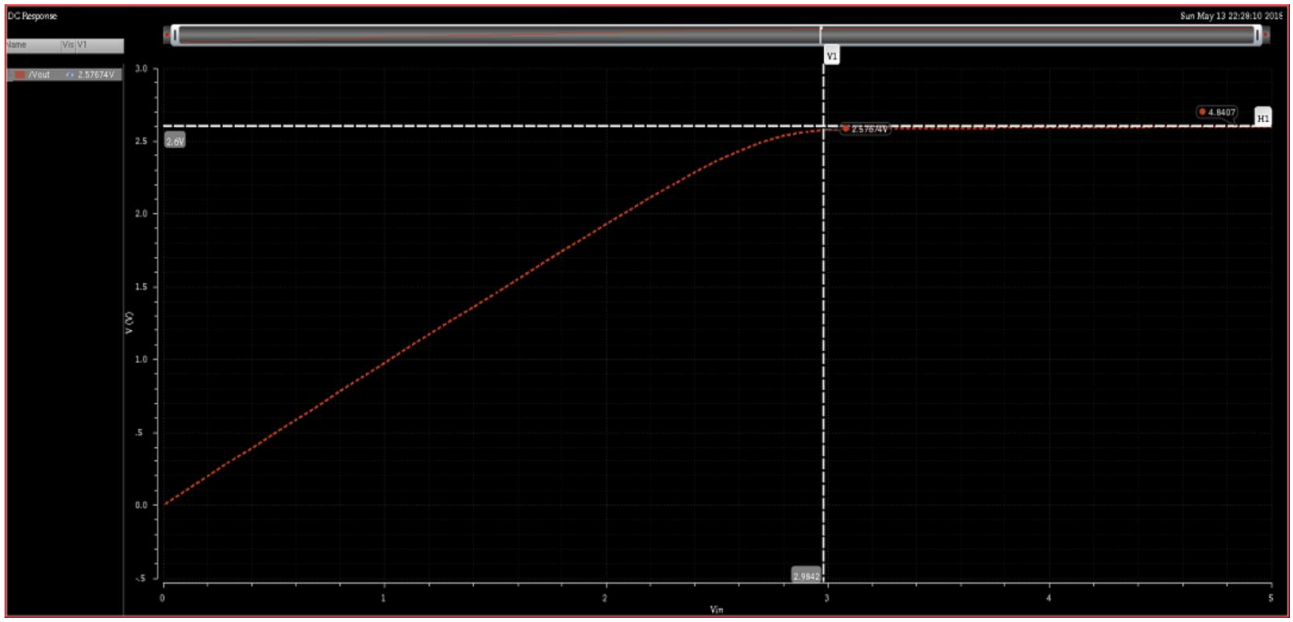

FIG 40

As per Fig 40, the dropout voltage **V_{IN} - V_{OUT} = 2.9842 – 2.6 = 384mV**

EFFICIENCY

$$P_{OUT}/P_{IN} = V_{OUT}/V_{IN} = \frac{5}{2.6} \times 100\% = \mathbf{52\ \%}$$

Table of specifications met by the voltage regulator vs the required specs

V_{ref}	1.201V (Average)
V_{out}	2.6V
Maximum load current handling capability	254.8215mA > 125mA
Maximum Power handling capability	624.8 mW > 320mW
Standby Current	37.4µA < 0.2mA
Line Regulation	6.76mV per volt
Load Regulation	10mV per milliamps
Temperature variation	1.3mV per ºC
Dropout Voltage	384mV
Efficiency	52%
Power dissipated by T1	611 mW

CONCLUSION

A linear voltage regulator is designed and the required specifications are met.