Digital & Mixed Signal Design (EE559)
Project

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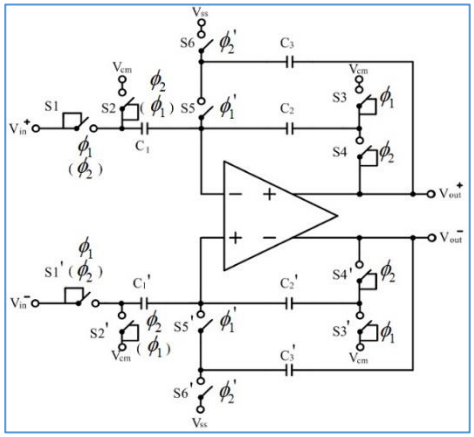
Objective

Our objective is to design a fast-settling, fully differential switched-capacitor amplifier with a gain of 2. The design aim is to be able to meet the specifications while minimizing power and maximizing settling speed.

Introduction

Analog signal amplification in discrete-time system can be performed by switched-capacitor amplifiers. Switched-capacitor amplifier has been used in the design of digital-to-analog converter. Below is the circuit diagram of a fully differential CMOS switched-capacitor amplifier based on transmission gates logic based switches.



For Miller compensation capacitor circuit

$\frac{g_{m2}}{C_L} > \frac{\sqrt{3}g_{m1}}{C_c}$; Value of C_c > 0.22*1 pf = 0.22 pf; we have chosen **C_c=500fF**; $\boldsymbol{g_{m2} = 7.25 * 10^{-3}\Omega^{-1}}$

Design methodology

Calculations

For single stage opamp

For DC voltage gain = 116.5 dB

$$GBW = g_m * \left(\frac{1}{2\pi C_L}\right)$$
$$= 200\ MHz\ (Assuming)$$

$$g_m = 1.256 * 10^{-3}\Omega^{-1}$$

Now, by using the (g_m/I_d) technique, the transistor sizes of single stage op-amp are (All transistors in saturation) :

Transistor	Length	Width
N7,N8	970nm	31.3µm
P5,P4	850nm	113µm

$$\frac{g_m}{I_d} = 13.3444\ V^{-1}$$

$\frac{g_m}{\frac{g_m}{I_d}} = \frac{1.256*10^{-3}}{13.3444}$; $\boldsymbol{I_d = 9.412 * 10^{-5}\ A}$

From the above equation $\boldsymbol{I_{d2} = 5.433 * 10^{-4} A}$

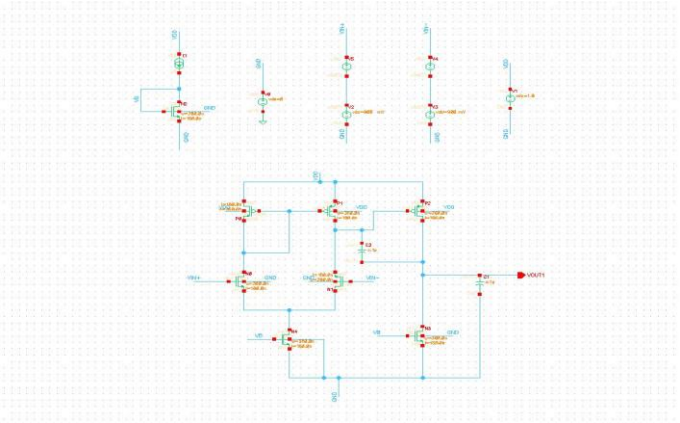
Transistor Sizing

Transistor	Length	Width
N16,N6	970nm	590µm
P9,P3	850nm	134µm

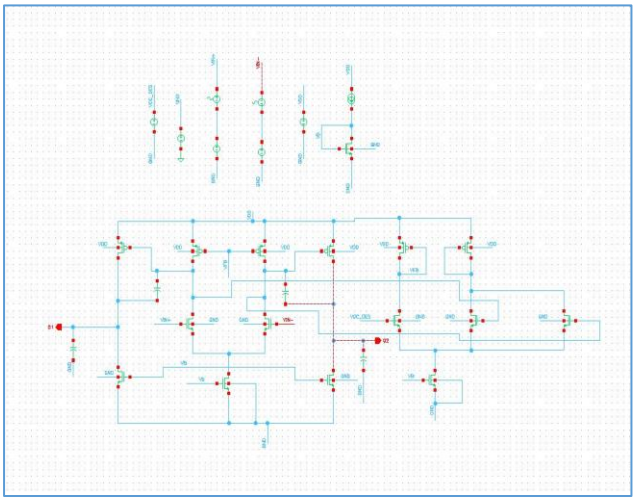
Sizing of the remaining transistors of the two stage opamp

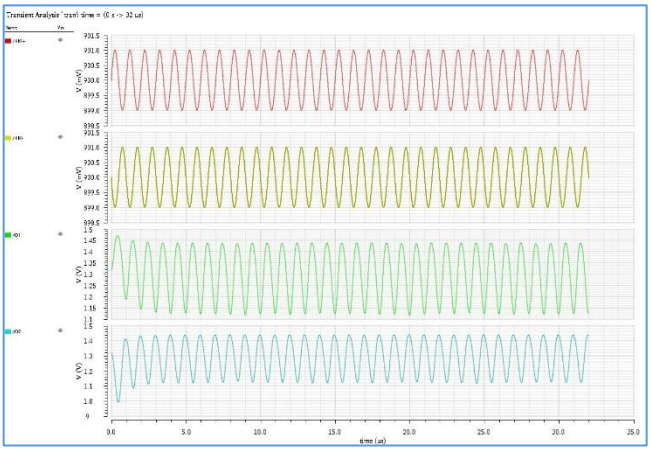
Transistor	Length	Width
N5	970nm	62.6µm
P8,P7	850nm	56.6µm
N9	850nm	31.3 µm
N11	970nm	15.65 µm
N12,N10	970nm	7.83 µm

Single stage op-amp



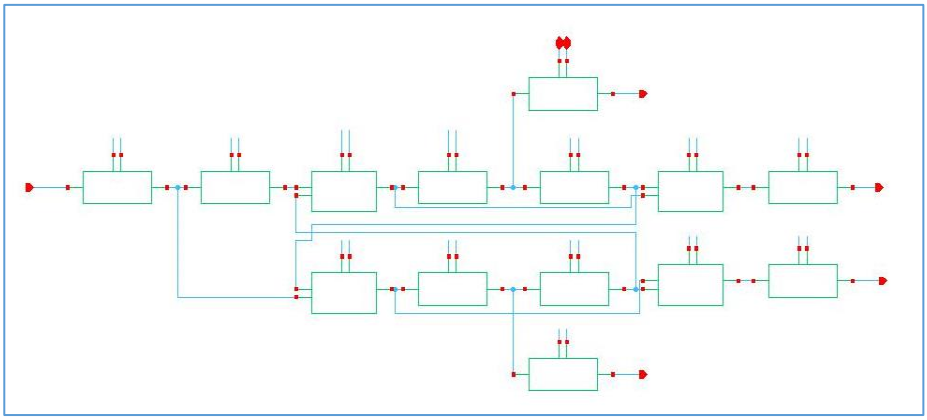
Two-stage fully differential OTA



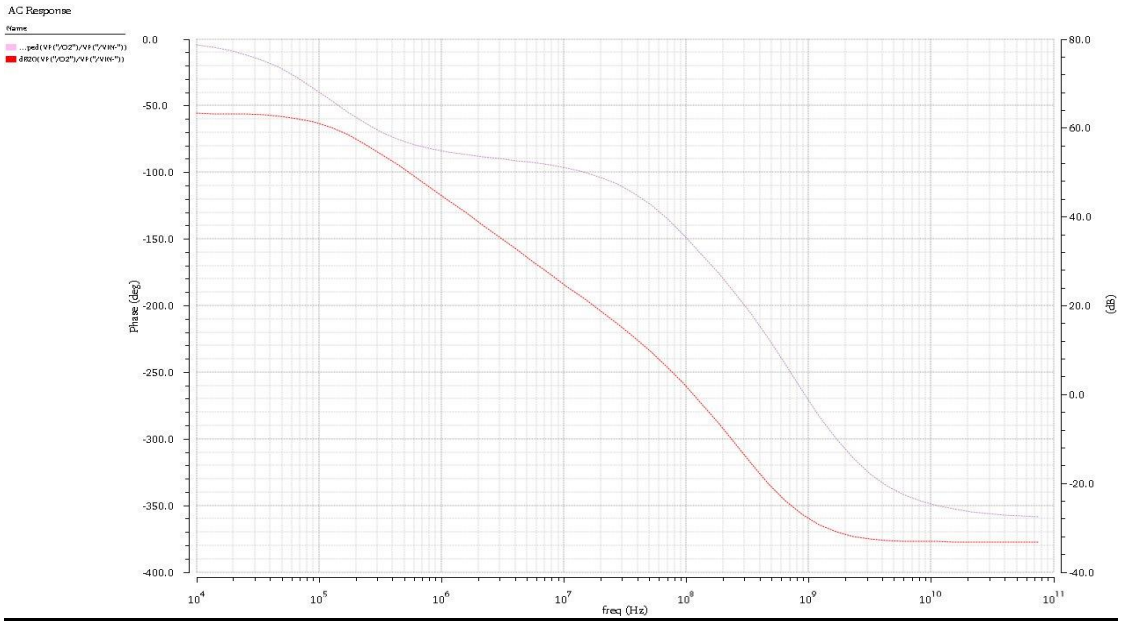


Amplified output 1

Non-overlapping clock generator



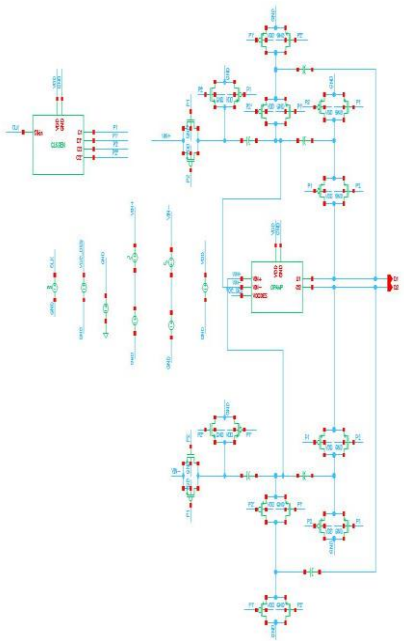
Gain and phase margin

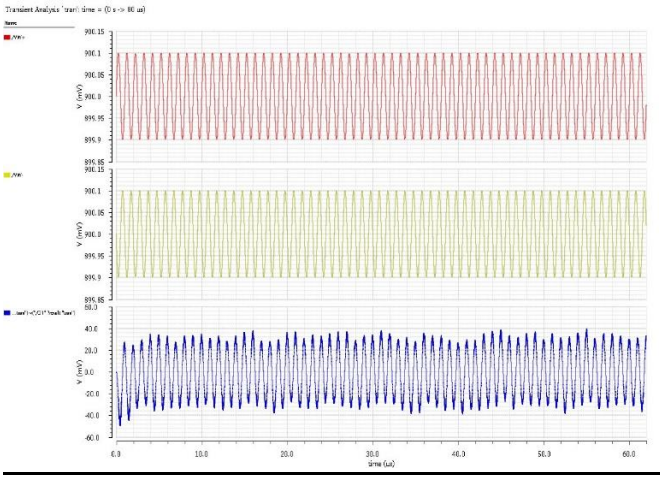


Gain: 63.2046 dB

Phase Margin: 63º

Differential switched capacitor amplifier





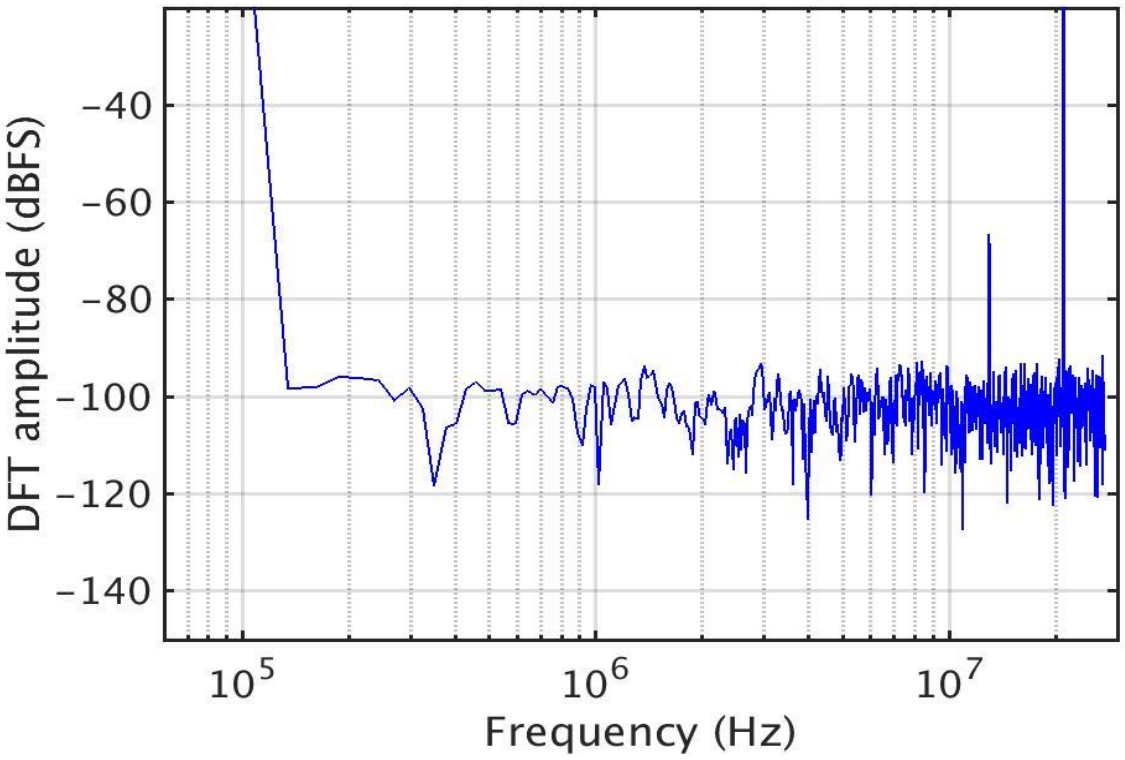
Amplified output 2

All sizes and passive values of the differential switched capacitor circuit

Transmission gates transistor sizes for the sampling switches	For Pmos(W/L): 20um/5um	For Nmos(W/L): 20um/5um
C_L		10pF
fs		33kHz
fin		2.5kHz
Ts		30µs
Pulse width		15µs
Vin		30µV

The **gain** of the switched capacitor amplifier was found to be above **2** on giving the above values.

DFT plot of the differential output of the differential switched capacitor circuit



Final calculations:

The SNDR was found out to be **57.043 dB** from the above DFT plot

Power consumption P=VI; 1.8V*80.55µA; P = 145 µW

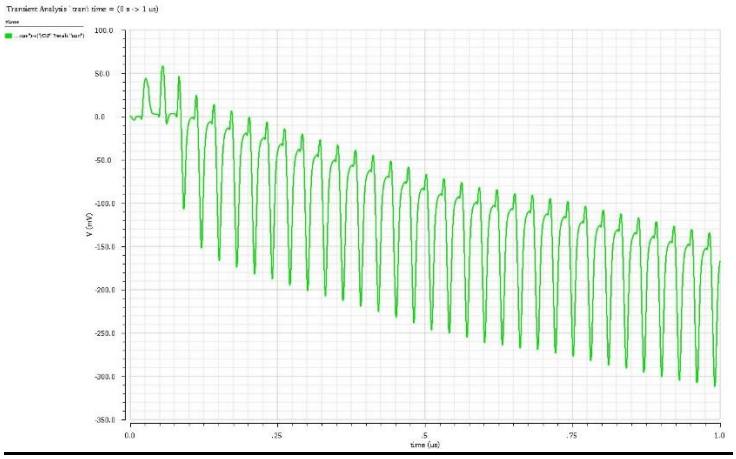
The Energy Efficiency number = 57.043 + 10log (33*10^3/145 µW)

Energy Efficiency number = 140.61

Static settling error = ϵs = -1/T (where T = Avβ) where 1336688 is Av(Voltage ratio) and β is ½; T = 1.49* 10^-6 (converting it to db and calculating for settling error)

ϵs = - 118 db

Transient Noise Analysis



References

1. A Differential Switched-Capacitor Amplifier KEN MARTIN, MEMBER,IEEE,LEVENT OZCOLAK, MEMBER, IEEE, Y, S, LEE, AND GABOR C. TEMES, FELLOW,IEEE (IEEEJOURNAL OF SOLID-STATECIRCUITS,VOL. SC-22,NO. 1, FEBRUARY1987)
2. FULLY DIFFERENTIAL SWITCHED CAPACITOR AMPLIFIER MODELLING AND PARAMETER EVALUATION Andrei DANCHIV* , Mircea BODEA# , Claudius DAN§
3. Digital CMOS design by Razavi