

Project 2

Microcoded Instruction Set Processor

Student Number: 18340180

I have built on the first project to implement a Microprogrammed Instruction Set Processor. I increased the number of registers in the register file from 32 to 33. The testbench shows that when TD, TA or TB are set to 1, the temp register is selected. I used two multiplexers for the TA and TB bits and I changed the decoder to include TD. The testbench for the decoder shows that it satisfies the requirements. All the components of the Datapath are 32 bits. I added all the components in the circuit diagram that we were given, and the testbench results show that they work as expected. The components include the Memory and the Control Memory. Mux M feeds 32 bit addresses from either Bus A or the PC into the Memory, the 9 least significant bits are then used to index into the array. The CAR feeds 17 bit addresses into the Control Memory but only the 8 least significant bits will be used to select a memory location in the Control Memory, the testbench for the control memory shows this. I implemented reset logic for the PC and CAR registers and then tested it using the testbenches for these components. I wrote microprogrammed instructions for the Control Memory that implement ADI, LD, SR, INC, NOT, ADD, unconditionally jump and conditional branch. I also wrote machine code for the Memory that demonstrates the use of those instructions. I included comments in my code to explain what the code is doing. The functional unit has the functionality defined in the table given for the assignment, I show this in the testbench for the datapath. I didn't have time to complete the carry look ahead adder, however this is something I'd be interested to do when I have more time.