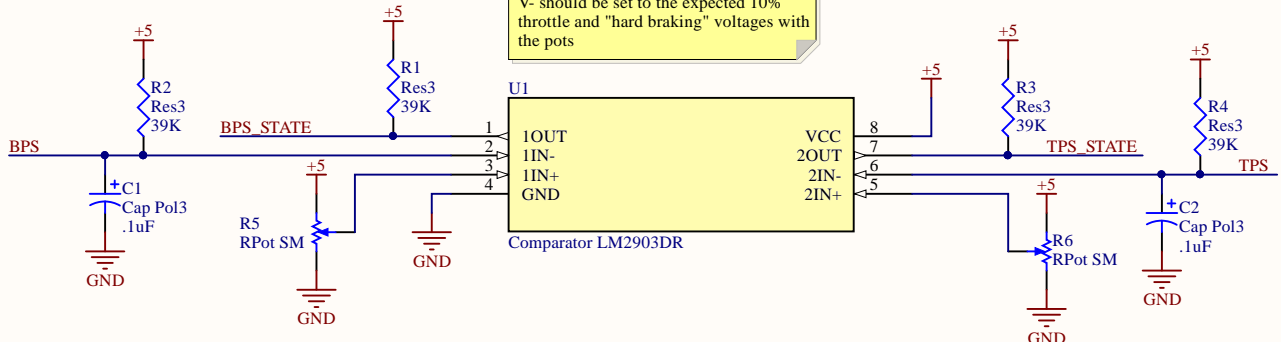
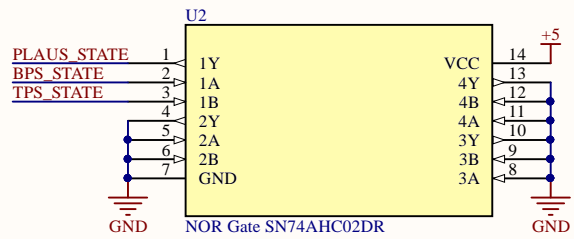


POWER JUMPERS
 Connected: Circuit Bypassed
 Disconnected: Circuit Active

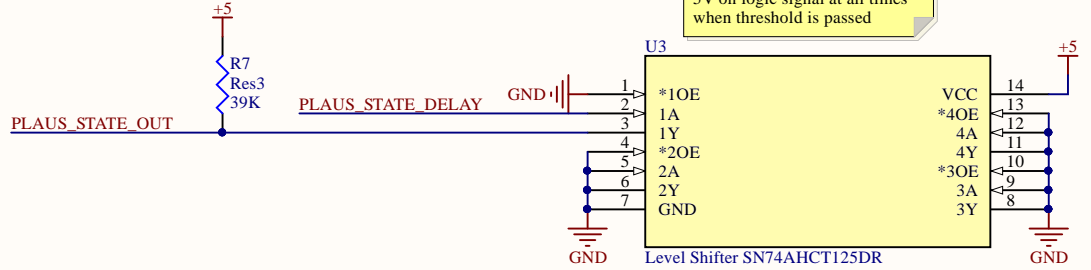
COMPARATORS
 When the input signal surpasses the V-set point the comparators will be pulled LOW
 V- should be set to the expected 10% throttle and "hard braking" voltages with the pots



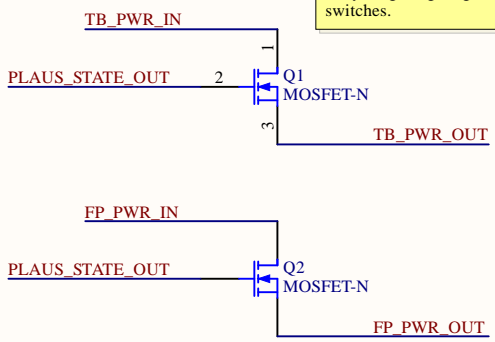
XOR GATE
 When both comparators output logic LOW the XOR will output a logic HIGH which will indicate the implausable state



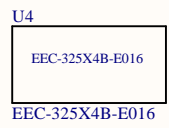
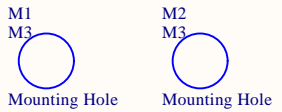
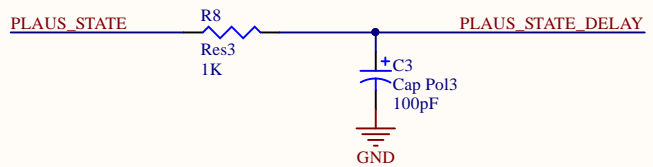
Level shifting buffer provides 5V on logic signal at all times when threshold is passed



POWER MOSFETS
 100V 60A Mosfets to control power to the fuel pump and throttle body. Logic signal gate controlled switches.



RC CIRCUIT FOR DELAY
 $\tau = RC = 5.1k * 100u = 500ms$
 Should be edited for 1sec per



Title		
Size	Number	Revision
A4		
Date:	2019-02-11	Sheet of
File:	C:\Users\...\BrakePlaus2019.SchDoc	Drawn By:

Comment	Description	Designator	Footprint	LibRef	Quantity
Cap Pol3	Polarized Capacitor (Surface Mount)	C1, C2, C3	C0805	Cap Pol3	3
DTM13-12PA-R008	DTM Series, 4.19mm Pitch 12 Way 2 Row Right Angle PCB Header, Solder Termination	J1	*TE_DTM13-12PA-R008	DTM13-12PA-R008	1
Mounting Hole		M1, M2	M3 Mounting Hole	M3 Mounting Hole	2
MOSFET-N	N-Channel MOSFET	Q1, Q2	DPAK	MOSFET-N	2
Res3	Resistor	R1, R2, R3, R4, R7, R8	J1-0603	Res3	6
RPot SM	Square Trimming Potentiometer	R5, R6	POT4MM-2	RPot SM	2
Comparator LM2903DR	Comparator	U1	D8	LM2903DR	1
NOR Gate SN74AHC02DR	Quad 2 Input NOR Gate	U2	D14	NOR Gate	1
Level Shifter SN74AHCT125DR	Buffer (Level Shifter)	U3	D14	SN74AHCT125DR	1
EEC-325X4B-E016		U4	*TE_EEC-325X4B-E016	EEC-325X4B-E016	1