AN-5075

Wafer-Level Chip-Scale Package (WLCSP) at Fairchild Semiconductor

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1. Purpose

The purpose of this application note is to provide basic guidelines to use Fairchild Semiconductor Wafer-Level Chip-Scale Package (WLCSP) to ensure consistent Printed Circuit Board (PCB) assembly yield and robust board-level reliability. The recommendations and references in this document are proven to work under the given conditions. However, users of this document must be aware that variances in manufacturing equipment, processes, and PCB design may require optimizations for specific applications for assembly yield and board-level performance. Fairchild WLCSP performance such as: MSL rating, board-level reliability, and thermal resistance data are included as reference. Unique requirements for handling a bare-die package, like WLCSP, are emphasized in this document.

2. Scope

This application note encompasses a broad range WLCSP technology. Device-specific information is not provided. This document should only be used as a guideline to help develop a user-specific solution. Actual experience and development efforts are often required to optimize the process per individual device requirements and practices.

3. Wafer-Level Chip-Scale Package

Wafer-Level Chip-Scale Package (WLCSP) is a bare-die packaging technology; the silicon and solder bumps on the active side constitute the final package form. The technology is a dramatic deviation from other types of semiconductor packages, which always feature additional packaging and interconnecting materials surrounding the semiconductor device(s). WLCSP shares the same roots with the long-standing flip-chip technology, but unlike typical flip chip, which is always assembled in a substrate package; WLCSP devices are directly mounted face down on PCB through solder interconnects. WLCSP is a true chip-scale packaging technology and offers smallest possible footprint among packaging technologies.

The WLCSP process is often referred as a “bumping” process. The whole operation is completed in the wafer form and finishes individual units after wafer saw. This process is considered an extension of the wafer FAB processes, where the device interconnects and protection are accomplished using the traditional semiconductor FAB processes and tools. In the final form, a WLCSP device is essentially a die with an array pattern of solder bumps at an I/O of the selection. The key advantages of WLCSP are the reduced package size, minimized die-to-PCB inductance, and enhanced thermal conduction characteristics.

3.1. WLCSP Bumping Technology

WLCSP bumping technologies can be categorized in two basic forms: Bump-On-Pad (BOP) technology and Redistribution-Layer (RDL) technology. Of the two WLCSP bumping technologies, BOP has the Under-Bump Metallization (UBM) directly bonded onto the chip’s top metallization. BOP is the most widely adopted WLCSP technology for analog/power devices, which often have limited numbers of I/Os and power/ground connections. One of the most distinctive advantages of BOP is the low bumping cost. Figure 1 highlights three basic BOP technologies: Electroless Nickel Immersion Gold (ENIG), Bump On Nitride (BON), and Bump On Re-passivation (BOR). Variances exist in polymer repassivation materials, UBM metal stack, re-passivation termination and thickness.

Unlike BOP with UBM/solder bumps directly anchored to the chip aluminum pad, RDL separates bump/UBM structure from the device surface with a polymer layer, typically polyimide (PI) or polybenzobisoxazole (PBO). The addition of this soft, stress-buffering polymer layer improves WLCSP board-level reliability, such as drop and temperature cycle (TMCL) life. Figure 1 highlights basic structures of three-mask RDL, four-mask RDL, and RDL plus encapsulated copper post technologies. The RDL plus encapsulated copper post approach provides superior board-level reliability performance due to the RDL structure. The copper posts effectively increase separation between silicon and PCB (stand-off height); front side encapsulating materials have a CTE that closely matches PCB CTE, and aggressive thinning of silicon all improve reliability.

As the industry moves towards higher device-level integrations with larger die size and more solder joints for signal, power, and ground connections; RDL technology becomes more popular due to solid board-level reliability at high pin count.

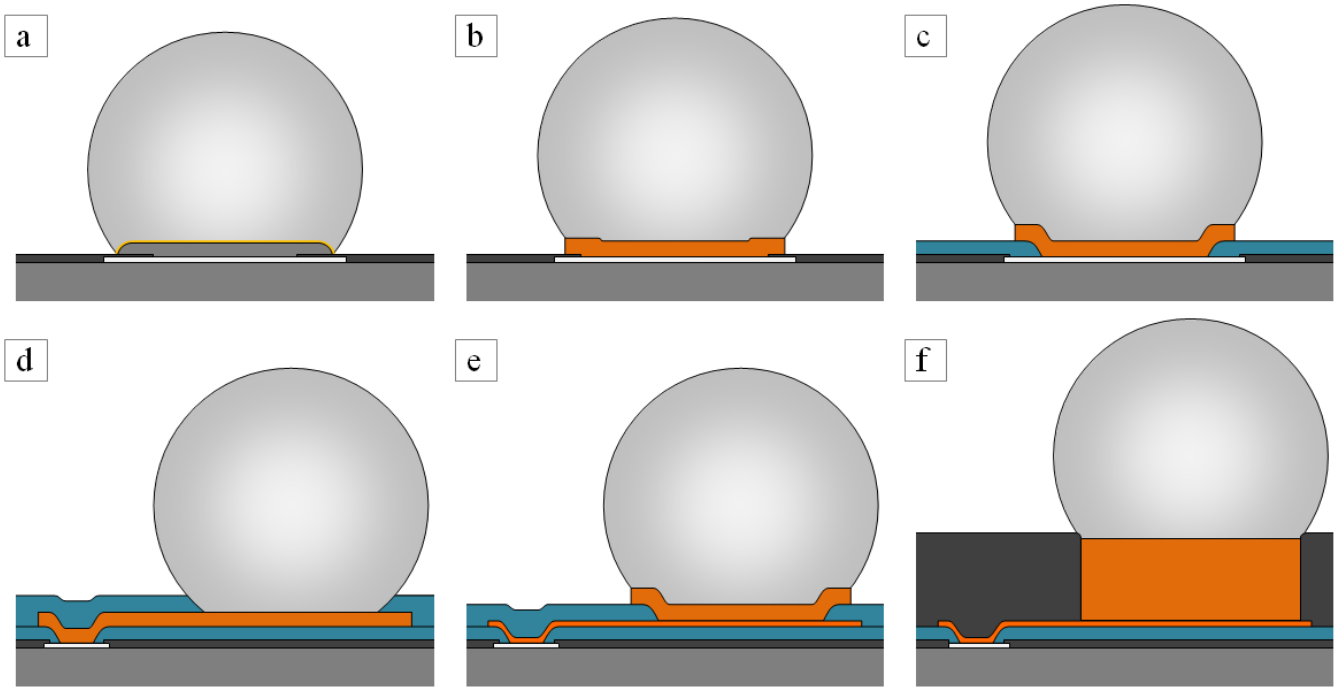


Figure 1. Cross-sections of Various WLCSP Bumping Technologies: a) Mask-Free Electroless Nickel Immersion Gold (ENIG) UBM Solder Bump; b) One-Mask Bump on Nitride (BON) UBM Solder Bump; c) Two-Mask Bump on Re-passivation (BON) UBM Solder Bump; d) 3 Mask RDL Solder Bump; e) 4 Mask RDL Solder Bump; f) Three-Mask RDL + Encapsulated Copper Post WLCSP Bump Structure

3.2. WLCSP Die Size, Thickness, and BSL

WLCSP packages from Fairchild Semiconductor range from 2 × 2 to 12 × 12 bump arrays, with bump pitch from 0.3 mm to 0.5 mm. WLCSP device size depends on the size of active die area, bump count, pitch, saw kerf width, and specific customer requirements. Minimum WLCSP package size, however, is determined by the within-die-bump pitch and the across-die-bump pitch. *Refer to Table 1 for minimum within-die and across-die pitch for standard solder bump arrays at selected bump pitch.*

Table 1. WLCSP Within-Die and Across-Die Pitch

Within-Die	0.5 mm	0.4 mm	0.35 mm	0.3 mm
Min. Across-Die	0.4 mm	0.4 mm	0.35 mm	0.35 mm

Given the bump count and minimum across-die pitch in a giving direction; i.e., x or y; the minimum die size in that direction can be calculated using the following equation:

$$\text{Minimum die size} = (n\text{-}1) \times \text{within-die pitch} + \text{minimum across-die pitch} \quad (1)$$

where n is the bump count.

WLCSP from Fairchild Semiconductor is most common in square form; however, it can also be in rectangular form. Fully populated WLCSP bump array is common. Depopulated bump array with selected solder bump(s) missing from a fully populated array is allowed, depending on the design and functional needs. A staggered arrangement of solder bumps is another option when it brings benefits like flexible chip / PCB designs. WLCSP comes in a variety of sizes, shapes, and bump arrays.

Besides the size of WLCSP; total package height, which is the sum of final silicon thickness plus solder bump height, is another important parameter when considering WLCSP. Fairchild Semiconductor offers selections of WLCSP package height from less than 300 µm to maximum 625 µm and could accommodate unique customer requirements.

Backside laminate (BSL) is not a default option for Fairchild WLCSP, but it can be added at customer request. Through the course of WLCSP development, Fairchild has demonstrated that BSL is neither a necessity for backside silicon chipping, nor a significant factor for board-level reliability. Light-sensitive circuit protection, as claimed in literatures, is not a reality concern since silicon is only transparent to long wavelength light, which is rarely encountered in broad applications of WLCSP. BSL is an addition to standard Fairchild WLCSP, but slightly higher cost should be expected due to additional material cost and manufacturing processing steps.

4. Printed Circuit Board (PCB) for WLCSP

PCB design requirements are based on IPC-2221, IPC-SM-7351, and IPC-7525 standards. General guidelines for PCB and stencil design are for optimum electrical performance and highly reliable solder joints. Board attributes and design guidelines are based on industry best practices and industry standards. These guidelines should be referenced in the design and assembly of PCB to ensure that they conform to acceptable industry standards.

4.1. PCB Design Guideline

IPC-SM-7351 is the often-referenced standard for designing PCB land patterns. It provides guidelines on how to design a land pattern for surface-mount components. The information provided includes the size, shape, and tolerance of the land pattern, with dimensions based on industry-registered component specifications, board manufacturing standards, and component-placement accuracy capabilities. The IPC-9701 standard provides information on board designs and reliability performance of the surface-mount device.

SMD and NSMD

There are two types of PCB pads for WLCSP mounting: Solder-Mask Defined (SMD) or Non-Solder-Mask Defined (NSMD), as shown in Figure 2. NSMD is recommended due to better overall land pattern registration accuracy and wider space for routing between adjacent pads. In combination with the right surface finish, NSMD also allows solder to wet the pad side walls that effectively increase the solder joint cross-section on the PCB side, As shown in Figure 3. In comparison, a SMD pad is defined by low-accuracy solder mask process. The design also creates the notch near the solder mask edge that can be a stress concentration point and, therefore, a potential reliability risk in the field. Typical clearance of 0.075 mm is set between the solder mask and the Cu pads for a NSMD pad and an overlap of 0.050 mm between the solder mask and the SMD Cu pads. Tighter space is often required for fine-pitch WLCSP and is acceptable as long as it satisfies PCB manufactures design rules and manufacturability targets.

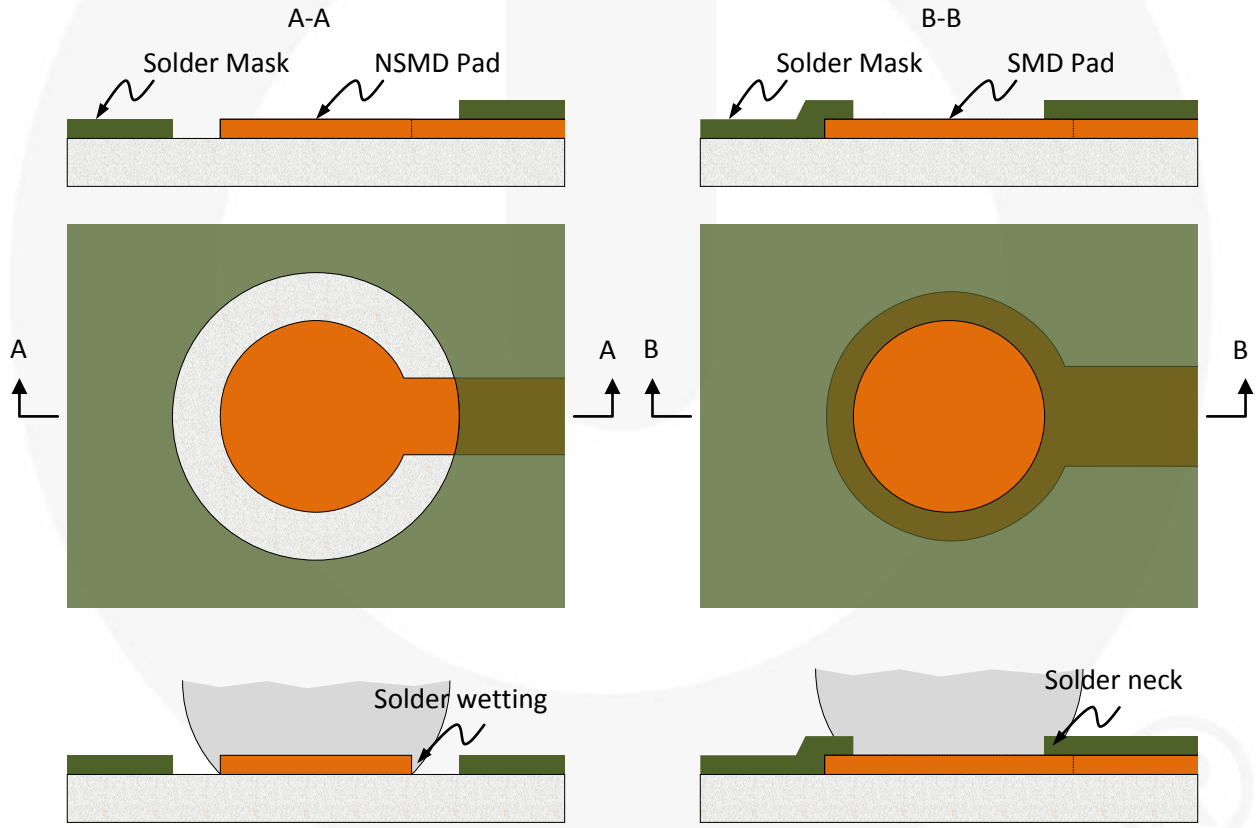


Figure 2. Top View and Cross-Sectional View of NSMD and SMD PCB Pad Designs, Solder Wetting on Side Walls of NSMD Pad, and Solder Neck on SMD Pad

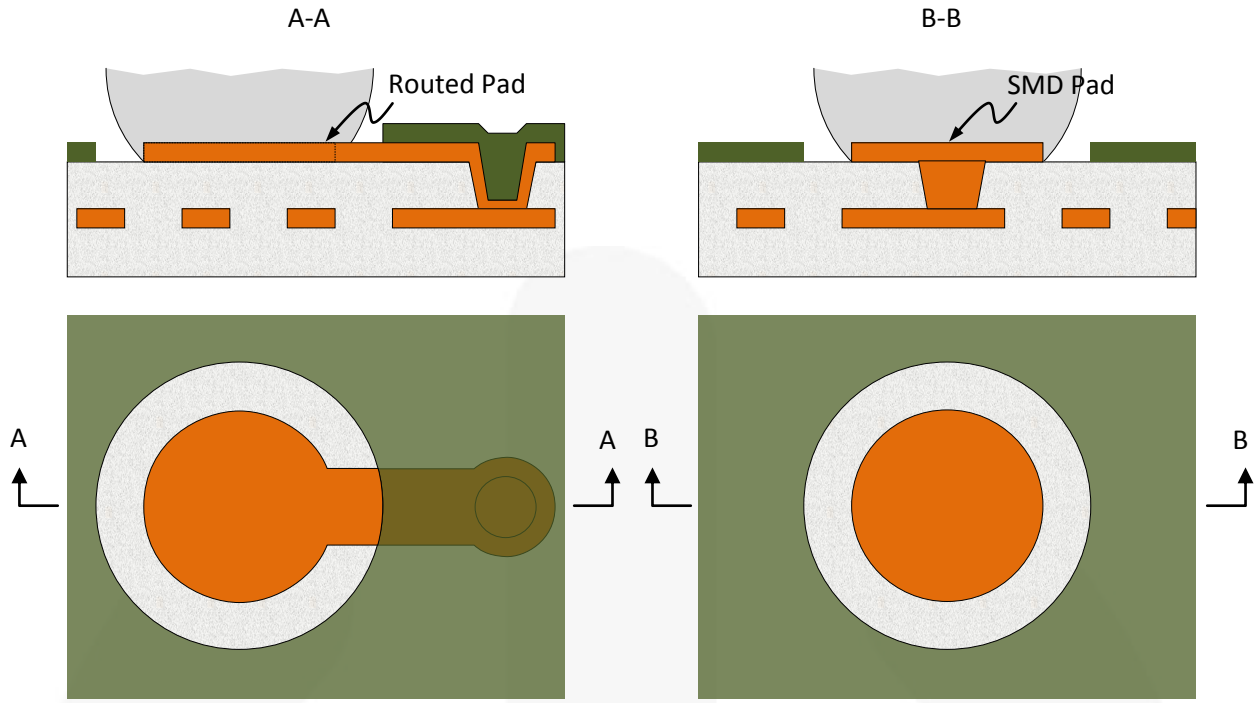


Figure 3. Cross-Sectional View and Top View of Routed PCB Copper Pad and via in Pad PCB Copper Pad. Filled Copper via is desired in the Via in Pad Design

Pad Size

PCB land pad size is typically matched to the UBM diameter of WLCSP component to ensure good board-level reliability. This applies to either SMD or NSMD design.

PCB Pad Surface Finish

ENIG, Organic Solderability Preservative (OSP), and Hot-Air Surface Leveling (HASL) are commonly used pad surface finishes. Immersion Ag (silver) is becoming popular as well. ENIG offers excellent surface solderability. Typical Ni thickness is 2.5 – 5.0 µm, while Au is 0.08 – 0.23 µm. Low-cost OSP has found wider adoptions for WLCSP. HASL is not preferred due to poor flatness. Immersion silver (Ag) is a lead-free alternative and has an excellent flatness; however, special handling may be required.

Vias Under WLCSP

Improperly designed and placed through-PCB vias within a WLCSP land pattern induce excessive stress in solder joints during solder reflow and reliability testing, and are not suggested for WLCSP[22]. Blind vias, either via-in-pad or routed, are recommended when addition routing is needed in a WLCSP footprint. A solder mask over the routed trace and via is mandated for routed vias (seen in Figure 3) to prevent undesired solder wetting beyond the pad area. For the via-in-pad design, bottom-up via fill plating is recommended to avoid difficulties in solder screen printing and prevent excessive voids or irregular solder joint shapes. Via-in-pad design is recommended for improved thermal dissipation.

Local Fiducials

Local fiducials are normally placed on the board to assist automatic placement equipment placing WLCSP accurately onto the board. Diagonally placed fiducials outside the component land pad are most common *(see Figure 4)*.

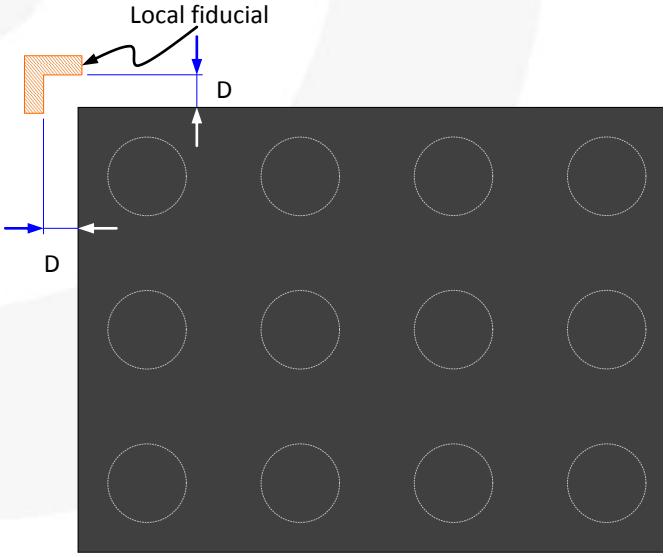


Figure 4. Local Fiducial for WLCSP Surface Mounting; Critical Gap D between Package and Fiducial Highlighted

PCB Materials

High-temperature FR4 or BT laminate (T_g=170°C to 185°C) is generally recommended for WLCSP assembly with lead-free solder bumps, which typically requires peak temperature of solder reflow profiles from 240°C to 260°C. Use the thinnest copper foil thickness that meets the electrical requirements of the circuit design.

PCB Trace

A balanced fan out of traces from land pads in the X and Y direction help avoid the impact of unintentional component movement as a result of unbalanced solder wetting forces during reflow. Use smaller trace routings from NSMD land pads to prevent solder migration that can result in lower standoff height of the bumps. Typically PCB trace width is less than 2/3 of the board pad diameter. Orientation of PCB trace needs special consideration for drop test PCB to avoid potential copper trace crack that often occurs before real component failures[21].

4.2. Stencil Design Guideline

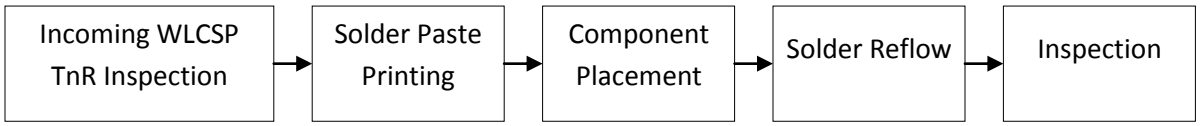
IPC-7525 provides guidelines on the design of stencils for surface mount. There are three major factors that affect the solder paste release performance of the stencil during the printing operation: 1) the area ratio and aspect ratio of the aperture; 2) the sidewall design, 3) the surface finish of the stencil walls.

Laser-cut stencil with complementary electro-polishing is recommended to improve solder paste release performance. Generally, the aspect ratio should be > 1.5 and the area ratio > 0.66. However, in certain cases, depending on termination size and termination pitch; the aspect and area ratio may change. Common stencil thicknesses for WLCSP are 0.100 and 0.125 (4 and 5 mils, respectively). Tapering on the stencil aperture is usually between 2 to 5°, which can be achieved by making the PCB contact side 0.025 mm larger than the squeegee side.

Additionally, curved corners for rectangular apertures promote better paste release and stencil cleaning. Reducing the stencil aperture to less than that of the board land pad is desirable to enhance the process of printing, reflow, and stencil cleaning. This minimizes the board pad and stencil opening misalignment.

5. WLCSP PBC Assembly

WLCSP PCB assembly typically follows the process flow depicted below.



5.1. WLCSP TnR Inspection

Incoming WLCSP tape and reel (TnR) inspection should be performed to confirm die orientation in the tape, device PIN 1 identification, laser marking, device thickness, and overall bumping quality.

5.2. Solder Paste

Common information needed for solder paste selection is: solder alloy recommendation, flux material and activity level, particle size, and metal content of the paste system. A commonly used solder paste in board assembly printing application is Type III solder particle and 89.5% metal content. Flux compositions are "no clean" or water-soluble. No-clean fluxes may be rosin based (RO), resin (RE), or free of rosins and resins, which are classified as organic (OR). Flux activity level may be low (L) or moderate (M). Water-soluble fluxes generally have organic (OR) composition and high (H) activity level, where cleaning is mandatory[2,6]. Halide-free fluxes are preferred and designated by a 0, while 1 indicates the presence of halides. A flux with ROL0 classification means rosin based, low activity, and halide free. Common solder alloys for board assembly are SnAgCu, the most common for lead-free soldering (~217- 220°C liquidus temperature).

After solder paste printing, optical inspection is recommended to ensure uniform solder paste coverage over the PCB pads.

5.3. Component Placement

Automated placement equipment with vision alignment systems is used for placing WLCSP onto PCB. The allowable package offset with respect to pad should be determined. Proper nozzle is critical for damage-free picking from tape and releasing on the PCB. Die placement pressure should be characterized. Generally, a 50% misalignment during placement of the component on the board is tolerable; as WLCSP tends to self-align during the reflow process. The placement machine nozzle z-height should have enough over-travel to allow the bumps to be submerged about 50 µm (2 mils) (or half of the solder paste height) to the printed paste to allow the self-centering of the package. This also prevents the package from moving during transit from the pick-and-place equipment to the reflow oven.

The two most popular methods of package alignment are the package silhouette ("look-down camera") and the ball-recognition system ("look-up camera"). In the package silhouette system, the vision system locates the package outline only. In the ball recognition system, the vision system locates the ball-array pattern and can also detect missing balls.

5.4. Assembly Reflow

Post component placement and before reflow, X-ray inspection is recommended to ensure acceptable placement accuracy of WLCSP components.

Solder Reflow

The SnAgCu solder alloy melts at ~ 217°C. Reflow peak temperature at joint level should be 15 to 20°C higher than the melting temperature. FSC WLCSP is qualified for 260°C reflow. A typical temperature/time profile for the lead-free (SnAgCu) solder and the corresponding critical reflow parameters based on JEDEC JTSD020D are shown below. The actual profile for the individual application depends on many factors; such as the size of the package, complexity of the PCB assembly, oven type, solder paste type, temperature variation across the board, oven tolerance, and thermal couple tolerance.

Reflow profile and critical parameters for lead-free (SnAgCu) solder:

- Ramp up 3°C/second maximum
- Preheat temperature (T_{smin} to T_{smax}): 150 to 200°C
- Time in pre-heat (t_s): 60 to 120 seconds
- Liquidus temperature (T_L): 217°C
- Time above T_L (t_L): 60 to 150 seconds
- Peak temperature T_P: ≤ 260°C
- Ramp-down rate: 6 °C/second maximum
- Time 25°C to peak temperature: 480 seconds maximum

Ramp-down rate should be below 6°C/s to prevent incurring stresses on the package and to create finer solder grain structure, which may affect reliability. On the other hand, slower than 2°C/s ramp-down rate is prone to produce large Ag3Sn aggregations in high silver solder, which is not desired. Convection-type or combined convection-IR reflow may be used. A Nitrogen-purge environment is preferable to improve solder wetting. Normally, the oxygen level should be less than 1000 ppm.

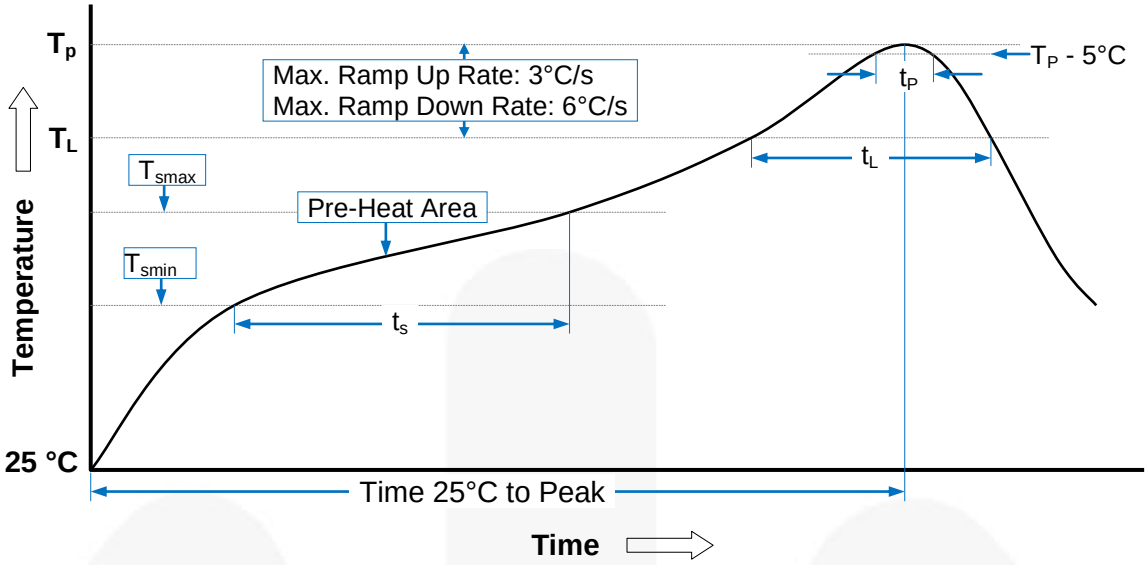


Figure 5. Reflow profile for Fairchild WLCSP, with definitions and reference rates for specific segments

5.5. Inspection

Visual and X-ray inspection is recommended after solder reflow for solder joint size and shape irregularities. Well-reflowed solder joints show evidence of good wetting of copper pads with uniform solder surface appearance. Dull or grainy solder surface is not uncommon for lead-free solder. These solder joints are acceptable.

5.6. Cleaning (Post-Soldering)

Depending on the application, soldering flux activity, board surface finish used, and whether under fill will be applied; cleaning after solder reflow may be required. There are three typical methods for cleaning the assembly: 1) boiling liquid bath with or without ultrasonic agitation; 2) liquid bath plus vapor; and 3) aqueous spray cleaning (most commonly used in the PCBA industry when cleaning is required using water-soluble fluxes).

Caution must be used when conducting ultrasonic cleaning because it may result in weakened solder joints, especially for the fine-pitch WLCSP. Typical liquid cleaning solutions are alcohol at 40°C or water-based cleaning solutions. An appropriate drying methodology must be used to ensure no water entrapment under the package.

IPC/EIA J-STD-001 provides acceptance criteria for post soldering cleaning, particularly on the rosin flux residues, ionic residues, and other surface organic contamination. IPC-TM-650 provides the test methodology for these.

5.7. Under Fill of WLCSP

Unless clearly stated, Fairchild WLCSP is tested without applying under fill materials. WLCSP reliability performances provided are all guaranteed without under fill. However, it is up to the end user to decide whether under fill is applied. It is generally accepted that under fill materials improves WLCSP reliability, as well as helping hold components when reflowed upside down.

5.8. Upside-Down Reflow

If WLCSP is reflowed on the bottom side, it is important to know if there is enough surface tension on the solder joints to hold the package. If analysis determines that the package would drop, the application and curing methodology of an appropriate adhesive should be provided.

The need for adhesive can be estimated using the following calculations:

Actual weight of the component ≤ Allowable weight

Allowable weight = Total solder contact surface area of WLCSP in $mm^2 \times 0.665$

5.9. Storage and Shelf Life

Floor life of the package is the allowable period after removal of the SMD components from the moisture barrier bag and before the solder reflow process in an environment not exceeding 30°C and 60% RH ambient conditions. Classifications of moisture sensitive packages per J-STD-020 and the floor life per J-STD-033 are tabulated in Table 2 below. WLCSP is rated as Level 1 moisture sensitive.

Table 2. Moisture-Sensitive Classifications

Level	Floor Life at 30°C / 60% RH Environment
1	Unlimited
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use, must be reflowed within the time limit specified

5.10. Rework

WLCSP components removed during PCB rework should not be reused for final assemblies. A WLCSP that has been attached to a PCB and then removed has seen 2 ~ 3 solder reflows, depending on whether the PCB is double sided. This is at or near the end of the tested and qualified three-solder-reflow survivability for Fairchild WLCSP. The removed WLCSP components should be properly disposed of so that they do not mix with fresh WLCSP components.

WLCSP component removal and replacement procedures should be established and qualified. A reference rework process follows this flow:

1. The floor life of moisture-sensitive components starts from the time the moisture barrier bag is opened and the mounted component(s) is exposed to ambient conditions. The floor life of the component should not have been exceeded before rework. Baking may be required in case this has been exceeded.
2. Pre-heating of the whole PCB assembly before localized heating of the component for rework. Pre-heating reduces the overall heating time and prevents potential substrate warping when localized heating is applied on the region for rework. Typical pre-heating temperature is around 100°C.
3. Localized heating on the region for rework is recommended to minimize heat exposure to the surrounding components. A hot air gun equipped with a thermocouple to monitor the temperature at the component site is preferred. Once the solder interconnect reaches the specified reflow temperature, a vacuum pick-up tool is used to remove the component from the board.
4. Cleaning of the board land pads: residue solder is removed using a soldering iron and a braided solder wicking material. A vacuum-desoldering tool can also be used to extract the solder by continuous vacuum aspiration of the solder. After removing the residue solder, leftover flux must also be removed.
5. Solder paste or flux printing: solder paste is usually deposited using a miniature stencil and squeegee. Where space is limited, flux is deposited on the solder pads.
6. Component placement on the board– replacing WLCSP components can be placed onto the board using automatic placement equipment.
7. Soldering or reflow– this can be selectively soldering the component using the same tools for removing the component or by passing the whole board to the original reflow profile.

5.11. Return WLCSP to Fairchild

When experiencing issues with Fairchild WLCSP devices in applications, please follow the guidelines listed below to return Fairchild WLCSP components for analysis.

1. If the Fairchild WLCSP is already mounted on PCB, return the whole assembly to Fairchild for the most complete assessment of issues experienced.
2. If full assembly return is not practical, cut out as large as possible piece of PCB with Fairchild WLCSP mounted for return to Fairchild. Close clearance from saw blade to the mounted WLCSP components is known to cause potential damages to solder joints and the bare silicon die, so exercise caution.
3. It is generally not recommended to remove the WLCSP components from the PCB assembly. Artificial damage, such as silicon crack, often occurs as the components are removed from the PCB. If a mounted WLCSP must be removed from the PCB assembly, procedures outlined in the 5.10 Rework section should be followed. Only a vacuum tool, not tweezers, can be used to remove WLCSP from PCB.
4. A WLCSP component or assembly must be well packaged and protected for shipping. For PCB assembly, place the assembly between two ESD hard foam materials and securely tape along all edges. For demounted WLCSP, a gel pack is recommended and the pack should be securely locked or taped. It is required to place packages in ESD bags before packaging and shipping. The Fastest shipping method should be used.

6. WLCSP Reliability

WLCSP is required to pass the same component reliability requirements originally set for the more traditional IC packages. Due to the unique package form – bare silicon with array of solder bumps – WLCSP is often mounted onto to test PCB to facilitate test and handling during reliability assessment; such as moisture sensitivity, optional life (OPL), temperature humidity bias test (THBT), high temperature storage life (HTSL), and TMCL. In addition, WLCSP must pass a separate set of board-level reliability tests, such as drop, TMCL, and bending tests designed specifically for devices bound for mobile applications.

6.1. Component-Level Reliability

Fairchild WLCSP undergoes the component-level reliability tests highlighted in Table 3, besides various device-specific functional tests. PCB via, pad, trace, and materials guidance is followed to ensure isolation of component failures from board-related failures.

Table 3. Typical Fairchild WLCSP Reliability Rests

Test	Test Condition	Read Points	Sample Size
DOPL	125°C, Biased	168, 500, 1000	77 × 3
HTSL	150°C	168, 500, 1000	77 × 3
THBT	85% RH, 85°C, Biased	168, 500, 1000	77 × 3
TMCL	-40 ~ +125°C	500, 850, 1000	77 × 3
HAST	85% RH, 110°C, Biased	264	45 × 3

6.2. Board-Level Reliability

Board-level reliability often refers to three tests: drop test, temperature cycle test (TMCL), and cyclic bend test. All board-level tests are performed on specially designed, daisy-chained, WLCSP test chips and test PCBs to allow continuous monitoring of the chain resistance throughout the stress cycles.

Fairchild daisy-chain test chips all feature multi-metal layer structure that mimics typical metal/dielectric and via stack common on real WLCSP chips. This allows a realistic assessment and expectation setting of WLCSP board-level reliability performance. Figure 5 shows two examples of daisy-chain test chip / PCB designs. The first is a single spiral daisy chain layout where resistance is monitored through all solder joints except the very center one in one electrical connection. The split daisy-chain design doubles the detection channels needed for real-time resistance monitoring and offers unique fault-isolation capability and low test net resistance for multi-layer test chips. Split daisy-chain design is generally preferred over a single design with a high pin count.

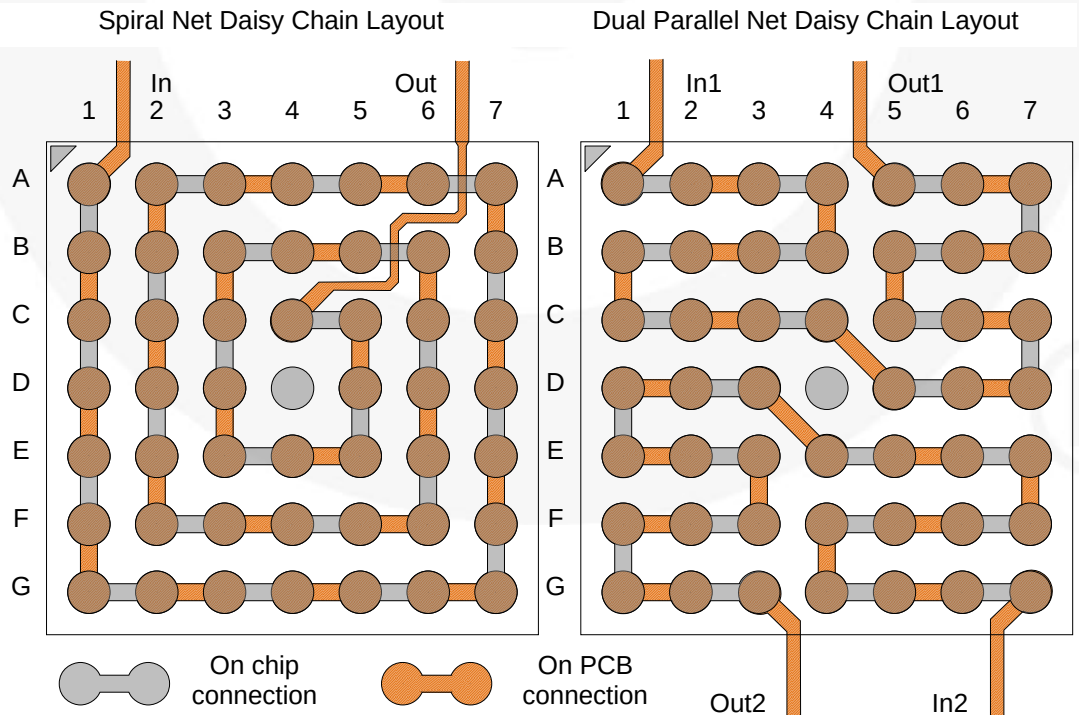


Figure 5. Spiral Net Single Daisy Chain Layout and Parallel Net Split Daisy Chain Layout

Test board design follows industrial standards or customer specifications for overall size, mounting hole size/locations, metal/dielectric stack up and metal layer coverage, etc., so as the test conditions.

Table 4 listed out typical test conditions and reference standards for Fairchild WLCSP board level reliability assessment.

The following board-level test, data collection, and probability plot referred to as a "Weibull plot" can be generated if a sufficient number of failures occur before the preset stop point. With upper confidence bond added, whether individual test meets specific requirements (failure probability at a fixed confidence level) can be determined. Figure 6 shows a Weibull plot of a daisy-chain drop test performed on JEDEC type PCB. The first failure occurred at 230 drops and the results satisfy minimum 150 drops at <10% unreliability with > 90% confidence.

Table 4. Typical Fairchild WLCSP Board-Level Reliability Tests

Test	Condition	Sample Size	Test Duration
Temperature Cycling	-40 ~125°C (IPC9701)	32	1000 Cycles / 6 Weeks
Drop	1500G, 0.5 ms JESD-22-B111	60 (4 PCBs)	1000 Drops / 2 Days
Cyclic Bend	2 mm, 1 Hz (JESD22-B113)	36 (4 PCBs)	200K Cycle / 12 Days

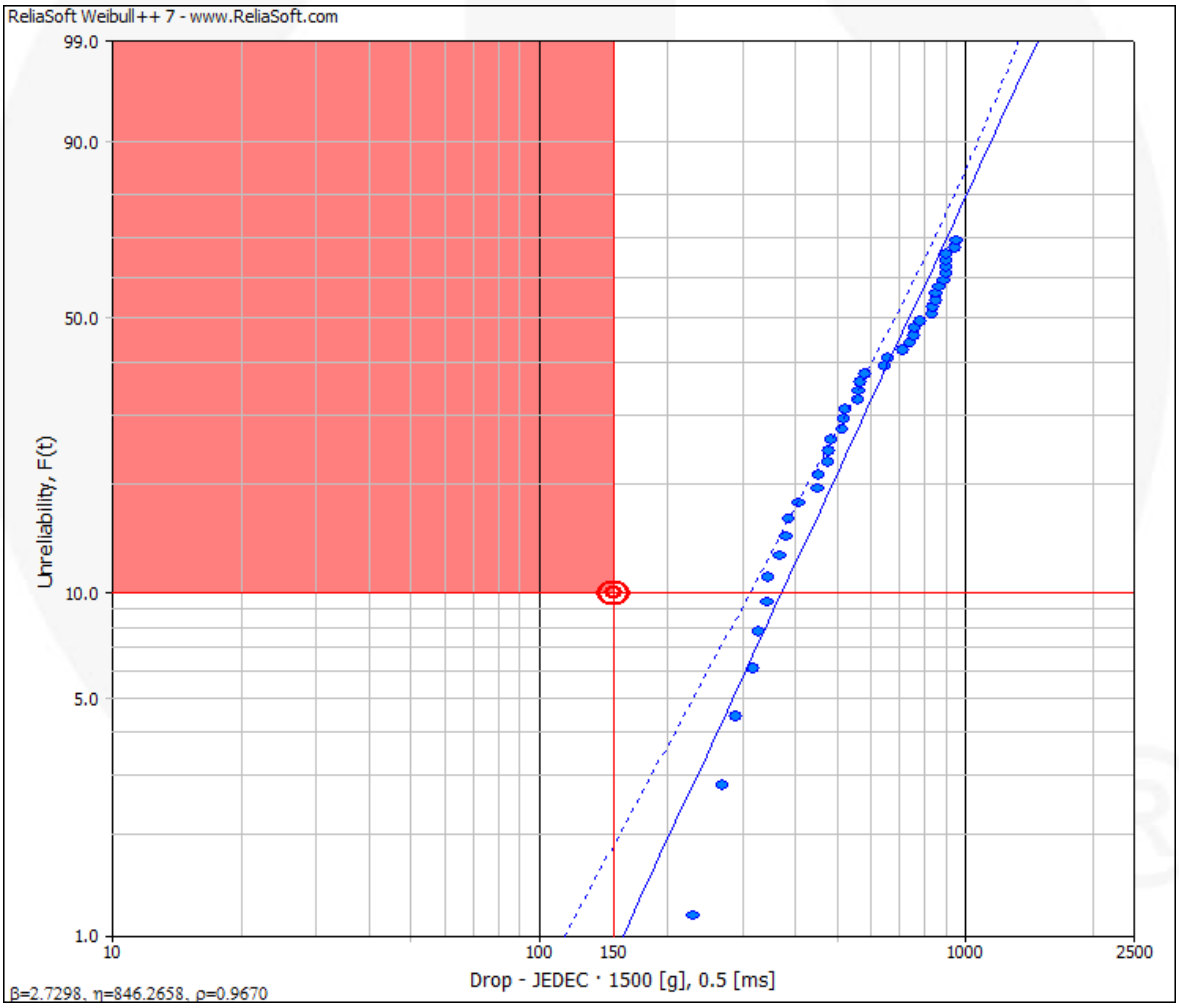


Figure 6. Weibull Plot of a Daisy-Chain WLCSP Drop Test Results

7. WLCSP Thermal Performance

WLCSP dissipates heat along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the PCB followed by convection and radiation off the exposed board surfaces. Of the two heat dissipating paths, the most significant is through solder joints to the PCB board. Because of this, WLCSP thermal performance is determined by the number of solder joints, joint size, pitch, PCB construction, and density of on-board copper traces, as well as presence of thermal vias connecting solder joints to the PCB ground plane.

Junction-to-ambient thermal resistance (Θ_{JA} JEDEC EIA / JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (hottest spot on die) to the environment near the package. Θ_{JA} is the most often reported thermal parameter for WLCSP.

Other than Θ_{JA}, junction-to-board thermal resistance (Θ_{JB}) is sometimes provided. Θ_{JB} measures the horizontal spreading of heat between the junction and the board.

The board temperature is taken 1 mm from the package on a board trace located on the top surface of the board. Another thermal resistance rarely reported for WLCSP is the junction-to-case thermal resistance (Θ_{JC}). WLCSP is typically not used with a metal housing or heat sink, so Θ_{JC}, used to estimate the thermal performance for package with cases, is the least often reported.

Θ_{JA}, junction-to-ambient thermal resistance is often simulated. The comparison simulations can be simplified by assuming that die is mounted on standard boards (JESD51-9 1s0p and JESD51-9 2s2p) with fully populated solder joint array. Figure 7 plots die size base Theta-J results based on two different simulation scenarios: the best case when all solder joints are connected to die size copper plan and with trace fan-out from there; the worst has only the edge joints connected to the fan-out copper traces. Neither case occurs in the real world, but it does represent two theoretical extremes. Actual device thermal performance should fall in the middle of these two extreme conditions.

JEDEC 2s2P, 1W

ball count	Die Size
4	0.85 × 0.85
4	1.0 × 1.5
6	0.85 × 1.25
6	1.0 × 1.75
9	1.25 × 1.25
9	1.5 × 1.5
16	1.65 × 1.65
16	2.0 × 2.0
20	1.65 × 2.05
20	2.0 × 2.4
25	2.05 × 2.05
25	2.4 × 2.4
49	2.85 × 2.85
49	3.0 × 3.0

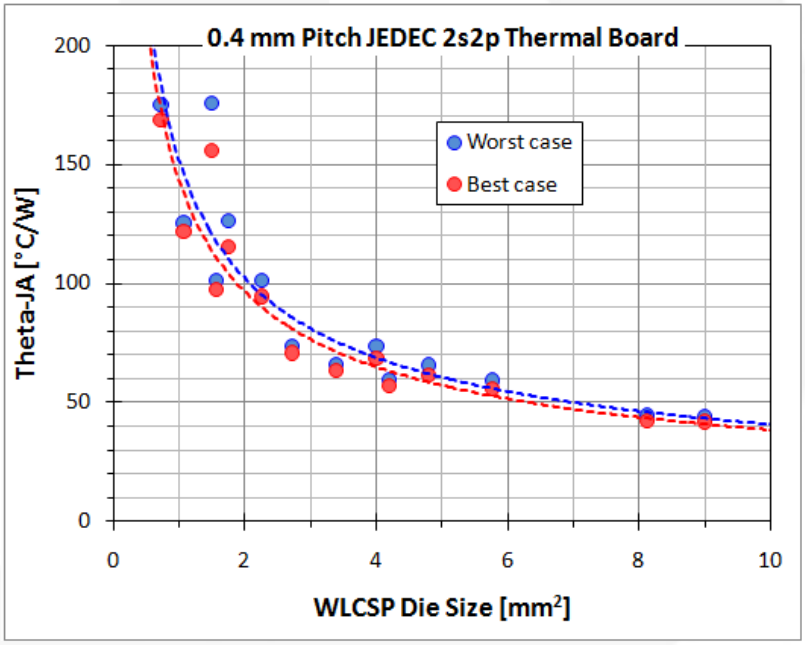


Figure 7. Theta-JA for Various Ball Count and Die Size, Under Two Simulation Extremes

8. Summary

Fairchild WLCSP technology, from wafer bumping to PCB design to surface mounting to reliability testing, is introduced in this application note. Following the guidelines in this document ensures consistent assembly yield and reliability performance. Though WLCSP is considered a maturing packaging technology and receives wide acceptance in the mobile computing market place, innovations continue and the application landscape is constantly changing. Users of Fairchild WLCSP are encouraged to contact Fairchild for the latest developments and knowledge for the advanced application needs.

9. References

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