Synthesis Report

Sat Apr 18 17:53:40 2015

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Release 14.4 - xst P.49d (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.25 secs

--> Reading design: hybrid.prj
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================================================================================
*                      Synthesis Options Summary                         *
================================================================================
---- Source Parameters
Input File Name                    : "hybrid.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "hybrid"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : hybrid
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
```

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Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                        HDL Parsing                                    *
=========================================================================
Analyzing Verilog file "D:\Changeproject\hi.v" into library work
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
=========================================================================
*                         HDL Elaboration                               *
=========================================================================
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
=========================================================================
*                         HDL Synthesis                                 *
=========================================================================
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
INFO:Xst:3210 - "D:\Changeproject\hi.v" line 130: Output port  of the instance  is unconnected or connected to loadless signal.
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\hi.v".
    Summary:
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Xors                                                : 141
 1-bit xor2                                          : 141
=========================================================================
=========================================================================
*                     Advanced HDL Synthesis                            *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Xors                                                : 141
 1-bit xor2                                          : 141
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block hybrid, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                         Partition Report                              *
=========================================================================
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Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=====================================================================
*                            Design Summary                         *
=====================================================================
Top Level Output File Name         : hybrid.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 96
#      LUT2                        : 1
#      LUT3                        : 7
#      LUT4                        : 8
#      LUT5                        : 51
#      LUT6                        : 29
# IO Buffers                       : 32
#      IBUF                        : 16
#      OBUF                        : 16
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice LUTs:                   96  out of  63400     0%
    Number used as Logic:                96  out of  63400     0%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     96
   Number with an unused Flip Flop:      96  out of     96   100%
   Number with an unused LUT:             0  out of     96     0%
   Number of fully used LUT-FF pairs:     0  out of     96     0%
   Number of unique control sets:         0
IO Utilization:
 Number of IOs:                          32
 Number of bonded IOBs:                  32  out of    210    15%
Specific Feature Utilization:
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=====================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
No clock signals found in this design
Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 7.045ns
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=====================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 11646 / 16
---------------------------------------------------------------------
Delay:               7.045ns (Levels of Logic = 11)
  Source:            y<1> (PAD)
  Destination:       p<14> (PAD)
  Data Path: y<1> to p<14>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            23   0.001   0.781  y_1_IBUF (y_1_IBUF)
     LUT5:I0->O            4   0.097   0.570  q4/k<2>1 (q4/k<2>)
     LUT4:I0->O            2   0.097   0.697  h4/x11 (h4/x1)
     LUT6:I0->O            2   0.097   0.688  h4/m2/o1 (c0<0>)
     LUT5:I0->O            2   0.097   0.688  h12/m1/o1 (ip1<5>)
     LUT5:I0->O            3   0.097   0.566  cla2/c<0>1 (cla2/c<0>)
     LUT6:I2->O            2   0.097   0.688  cla2/out71 (cla2/c<2>)
     LUT5:I0->O            3   0.097   0.521  cla2/out81 (c2<1>)
     LUT5:I2->O            3   0.097   0.693  cla3/out51 (cla3/c<1>)
     LUT6:I1->O            1   0.097   0.279  cla3/Mxor_n<3>_xo<0>1 (p_14_OBUF)
     OBUF:I->O                 0.000          p_14_OBUF (p<14>)
    ----------------------------------------
    Total                      7.045ns (0.874ns logic, 6.171ns route)
                               (12.4% logic, 87.6% route)
=====================================================================
Cross Clock Domains Report:
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=====================================================================
Total REAL time to Xst completion: 25.00 secs
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Total CPU time to Xst completion: 25.04 secs

-->
Total memory usage is 444228 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```