Synthesis Report

Sat Apr 18 17:33:46 2015

```
Release 14.4 - xst P.49d (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.23 secs

--> Reading design: booth.prj
TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report
================================================================================
*                      Synthesis Options Summary                               *
================================================================================
---- Source Parameters
Input File Name                    : "booth.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "booth"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : booth
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
================================================================================
```

```
=========================================================================
*                        HDL Parsing                                    *
=========================================================================
Analyzing Verilog file "D:\Changeproject\booth.v" into library work
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
=========================================================================
*                         HDL Elaboration                               *
=========================================================================
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
=========================================================================
*                         HDL Synthesis                                 *
=========================================================================
Synthesizing Unit .
    Related source file is "D:\Changeproject\booth.v".
INFO:Xst:3210 - "D:\Changeproject\booth.v" line 141: Output port  of the instance  is unconnected or connected to loadless signal.
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\booth.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\booth.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\booth.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "D:\Changeproject\booth.v".
    Summary:
        no macro.
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Xors                                                : 139
 1-bit xor2                                          : 139
=========================================================================
=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Xors                                                : 139
 1-bit xor2                                          : 139
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block booth, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                         Partition Report                              *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                          Design Summary                               *
=========================================================================
Top Level Output File Name         : booth.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 102
#      LUT2                        : 2
#      LUT3                        : 10
#      LUT4                        : 13
#      LUT5                        : 46
#      LUT6                        : 31
# IO Buffers                       : 32
#      IBUF                        : 16
#      OBUF                        : 16
Device utilization summary:
---------------------------
```

```
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice LUTs:                  102  out of  63400     0%
    Number used as Logic:               102  out of  63400     0%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    102
   Number with an unused Flip Flop:     102  out of    102   100%
   Number with an unused LUT:             0  out of    102     0%
   Number of fully used LUT-FF pairs:     0  out of    102     0%
   Number of unique control sets:         0
IO Utilization:
 Number of IOs:                          32
 Number of bonded IOBs:                  32  out of    210    15%
Specific Feature Utilization:
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
No clock signals found in this design
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 7.583ns
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 44168 / 16
-------------------------------------------------------------------------
Delay:               7.583ns (Levels of Logic = 13)
  Source:            x<0> (PAD)
  Destination:       p<13> (PAD)
  Data Path: x<0> to p<13>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            23   0.001   0.791  x_0_IBUF (x_0_IBUF)
     LUT6:I0->O            5   0.097   0.702  p3/ca1 (n<3>)
     LUT5:I0->O            2   0.097   0.697  p4/Mxor_p_xo<0>1 (fp<2>)
     LUT6:I0->O            3   0.097   0.305  fa3/cy1 (c1<2>)
     LUT5:I4->O            5   0.097   0.314  fa5/cy1 (c1<4>)
     LUT6:I5->O            4   0.097   0.393  fa8/cy1 (c1<7>)
     LUT5:I3->O            2   0.097   0.688  fa9/h2/Mxor_s_xo<0>1 (ip1<6>)
     LUT5:I0->O            2   0.097   0.697  sa7/cy1 (c2<6>)
     LUT6:I0->O            4   0.097   0.393  sa8/cy1 (c2<7>)
     LUT3:I1->O            2   0.097   0.561  sa9/h2/Mxor_s_xo<0>1 (ip2<6>)
     LUT5:I1->O            3   0.097   0.693  foa7/cy1 (c3<6>)
     LUT5:I0->O            1   0.097   0.279  foa8/h2/Mxor_s_xo<0>1 (p_13_OBUF)
     OBUF:I->O                 0.000          p_13_OBUF (p<13>)
    ----------------------------------------
    Total                      7.583ns (1.068ns logic, 6.515ns route)
                                       (14.1% logic, 85.9% route)
=========================================================================
Cross Clock Domains Report:
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=========================================================================
Total REAL time to Xst completion: 28.00 secs
Total CPU time to Xst completion: 28.67 secs

-->
Total memory usage is 419012 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```