Pipelined CPU implementation

- Forwarding: The value of rd at EX/MEM register and MEM/WB register are compared with the rs1 and rs2 values at the ID/EX register. If the instruction requires the rs1 and rs2 values, then the MUX(within pipeline_CPU module) selects the required value and forwards it to the CPU.

- Stalling: When an instruction intends to change the PC value, the pc_replace signal is set. Then the control signals of the instruction moving out of the ID/EX register are set to 0 and the idata corresponding to the instruction moving out of the IF/ID register is changed to the instruction ADDI R0,R0,0. In this way, both the previously loaded instructions are invalidated. The instruction at the new PC value is loaded in the next clock cycle.

- Hazard detection: If there is an ALU instruction immediately following a Load instruction which writes to the register read by the ALU instruction, the hazard is detected and the flag signal is set to 0 and the iaddr_upd value is set to 4. This decreases the PC value by 4 so that the same instruction is loaded again. The act signal is also set to 0, which sets all control signals of the ALU instruction to 0, so that the wrong register

values do not result in wrong outputs being written. The PC offset is given by the pc_new value. If the PC value is taken from a register(in case of JALR), the pc_JALR signal is set to 1.

Pipelined CPU architecture