

APP_1_huom2704_rene0901

Conception PCB 1

N/A

Revision 1.00

Date: 2024-01-12

Revision history	

Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

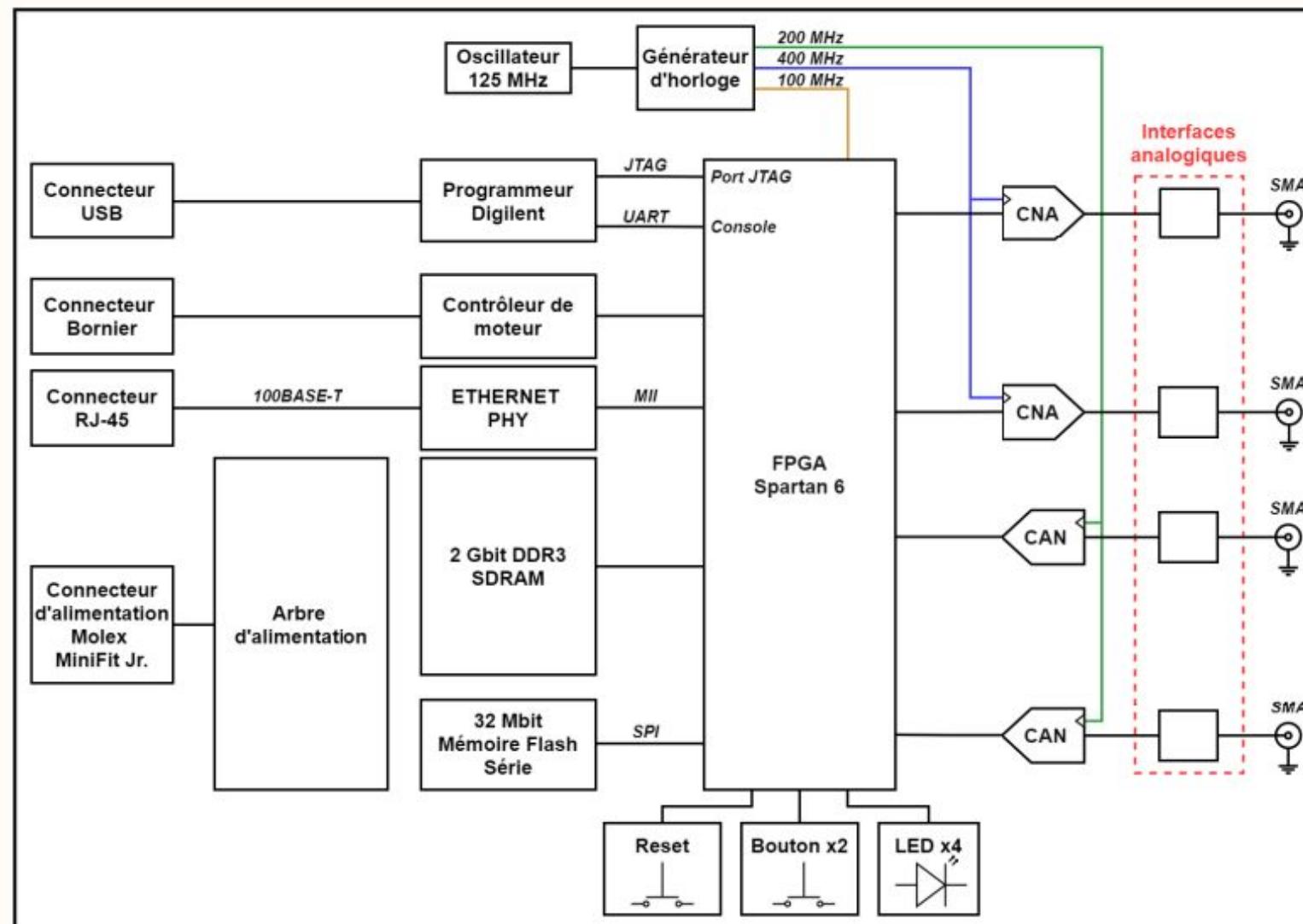
Project Title APP_1_huom2704_rene0901	Global Project <i>Conception PCB 1</i>
Size 11x17	Group N/A
Date 2024-01-12	Sheet 1 of 16
Filename APP_1_Title.SchDoc	Designers Mathieu Huot Emile Renaud

DDR3, FPGA, ALIM, Port Ethernet, Radiateur

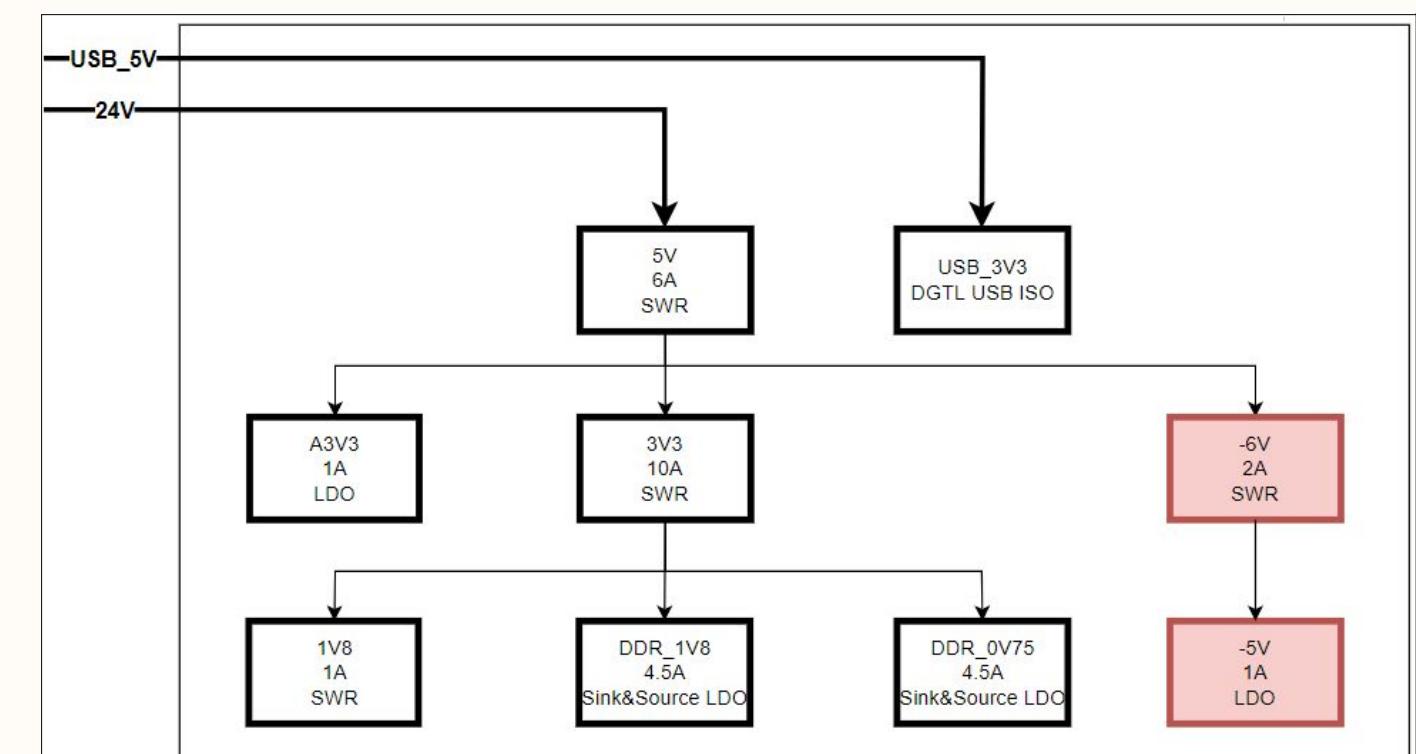
A

A

Note : Le placement de tous les composants est exigé. Toutefois, afin de circonscrire le travail, seul le routage de la DDR3, le port Ethernet, le radiateur du FPGA et les alimentations du FPGA, les plans de retour de courant, l'arbre d'alimentation comprenant son découplage doivent être réalisés à la revue de conception. Une contrainte



POWER



Sheet Name

Overview

Project Title

Conception PCB 1

Global Project

Size

11x17

Group

N/A

Revision

1.00

Date

2024-01-12

Sheet

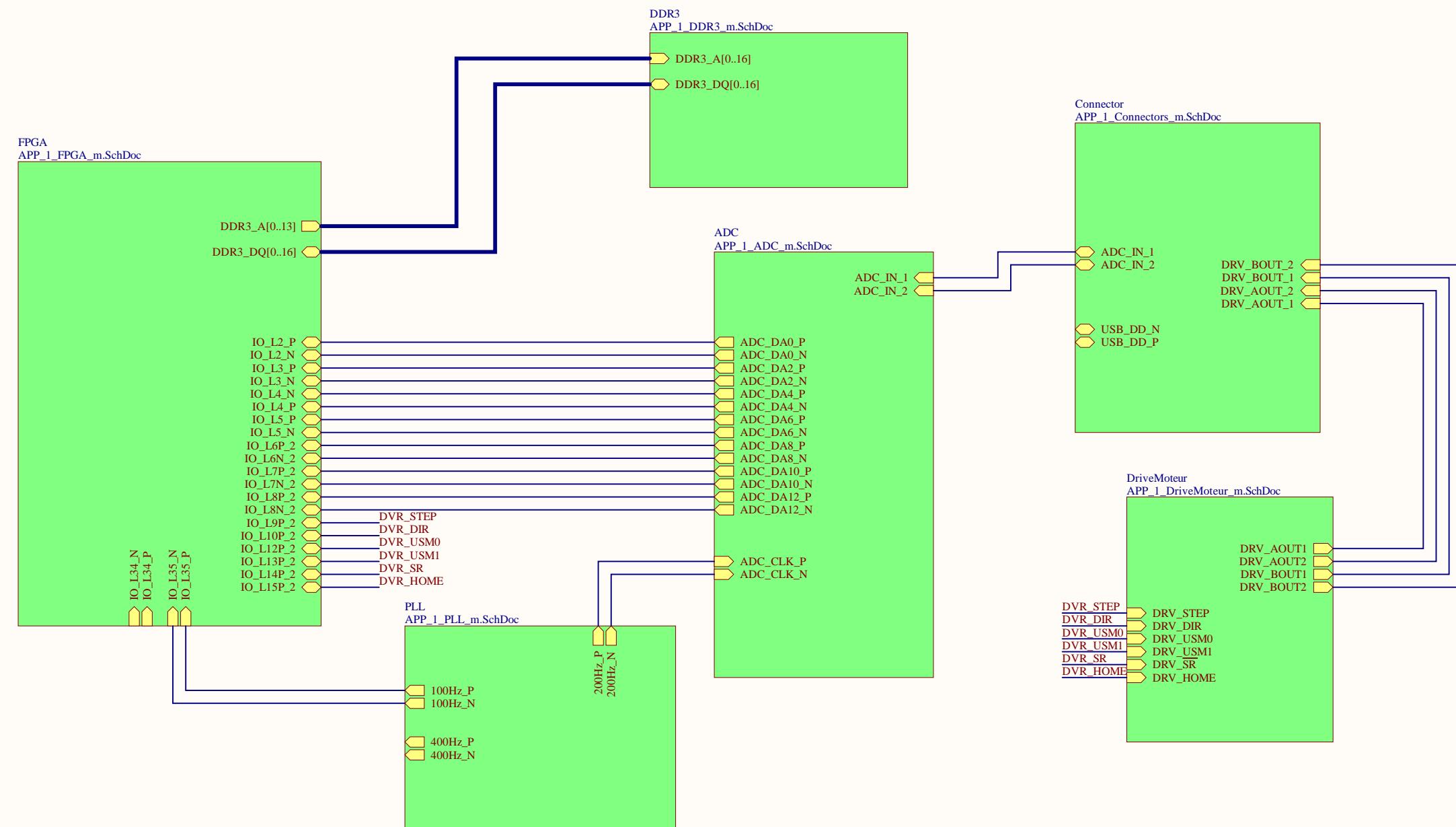
2 of 16

Filename

APP_1_Overview.SchDoc

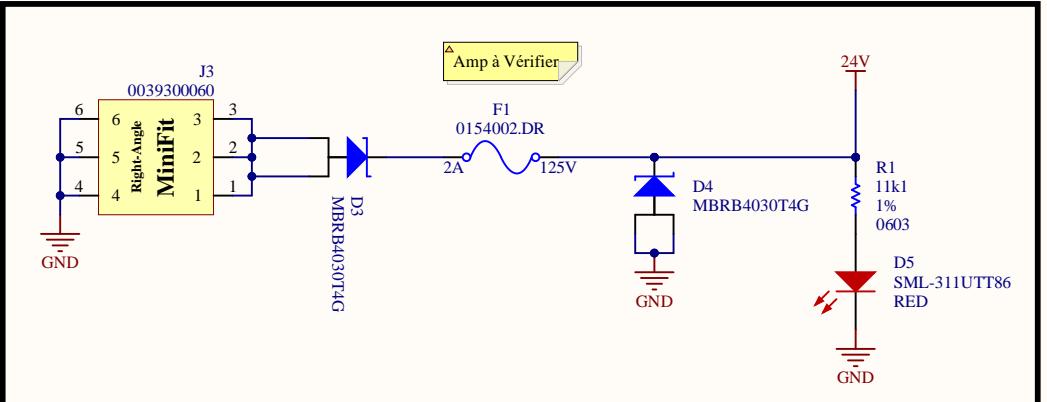
Designers

Mathieu Huot
Emile Renaud

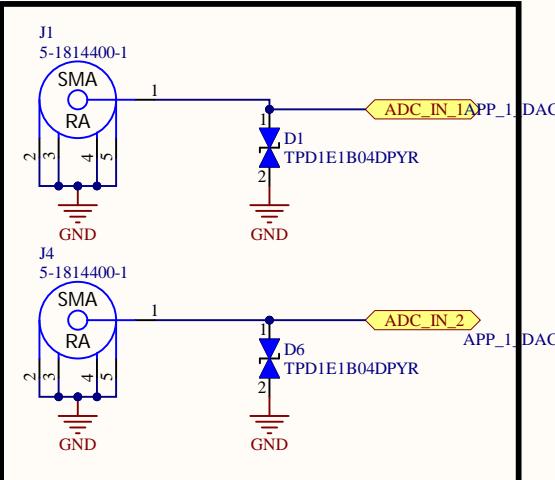


Sheet Name	Hierarchic		
Project Title	APP_1_huom2704_rene0901		
Global Project	<i>Conception PCB 1</i>		
Size	11x17	Group	N/A
Date	2024-01-12	Sheet	3 of 16
Filename	APP_1_Hierarchic.SchDoc		Designers Mathieu Huot Emile Renaud

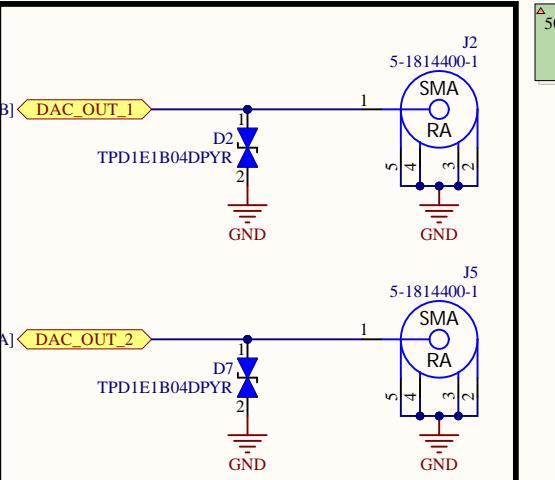
Main Power



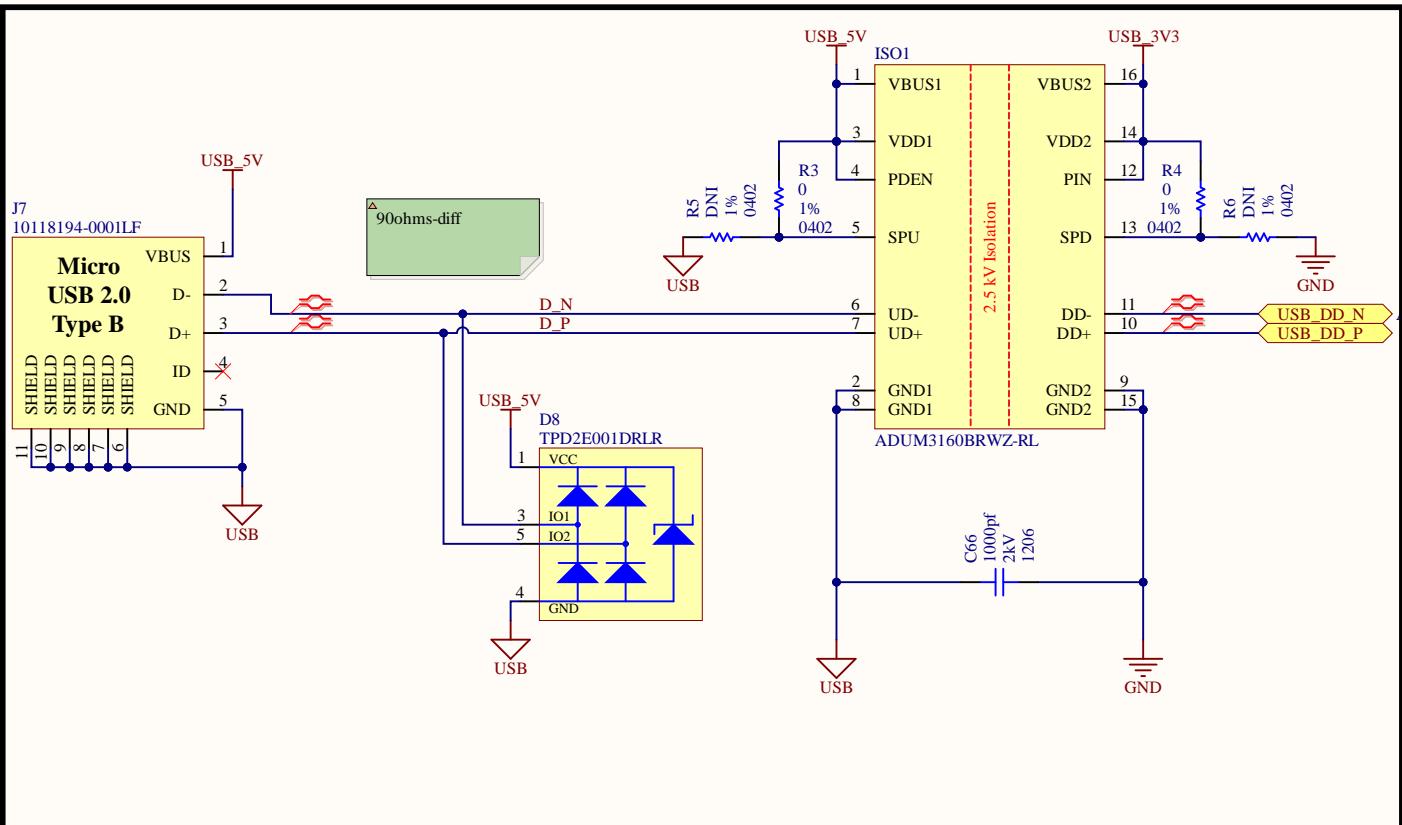
ADC SMA



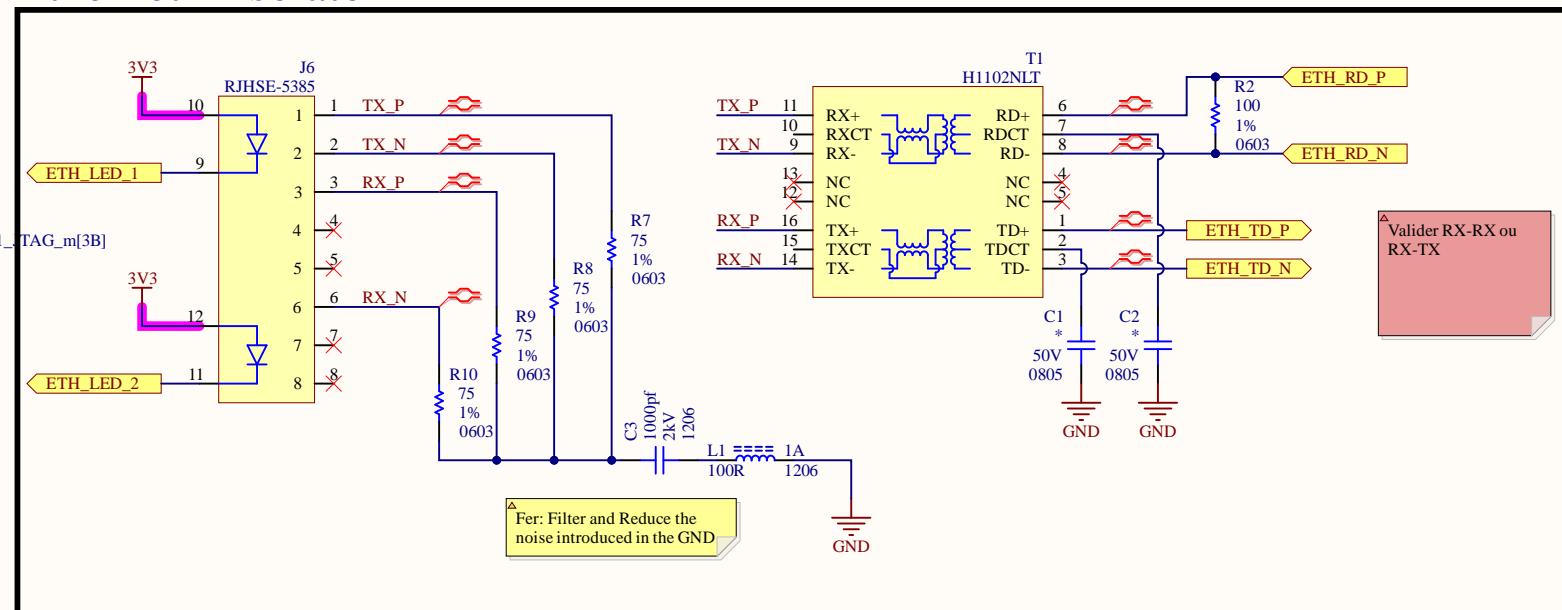
DAC SMA



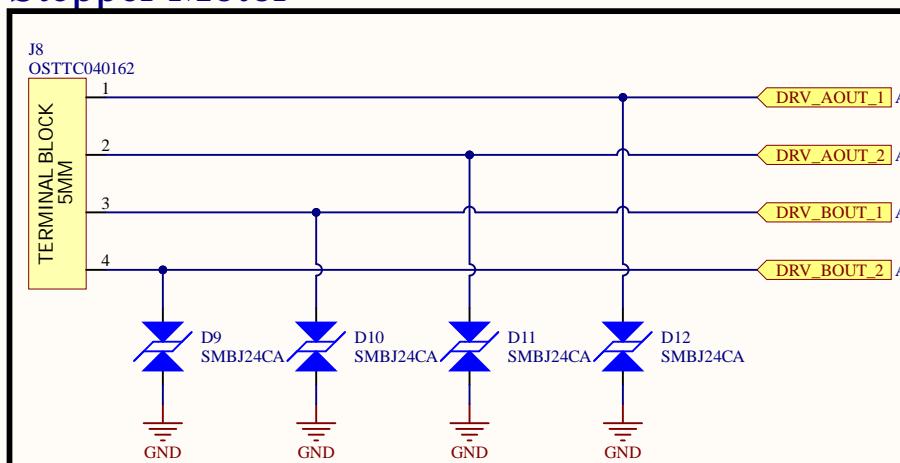
USB + Isolator



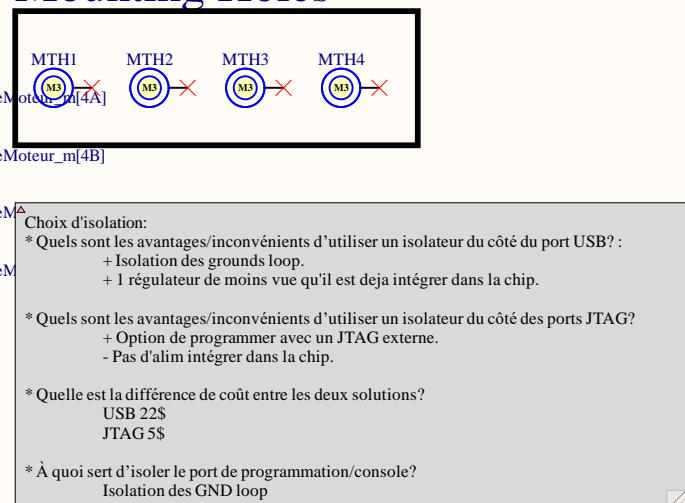
Ethernet + Isolator



Stepper Motor



Mounting Holes



Sheet Name

Connectors_m

Project Title
APP_1_huom2704_rene0901

Conception PCB 1

Global Project

N/A

Revision
1.00

Size

11x17

Group

N/A

Date

2024-01-12

Sheet

4

of

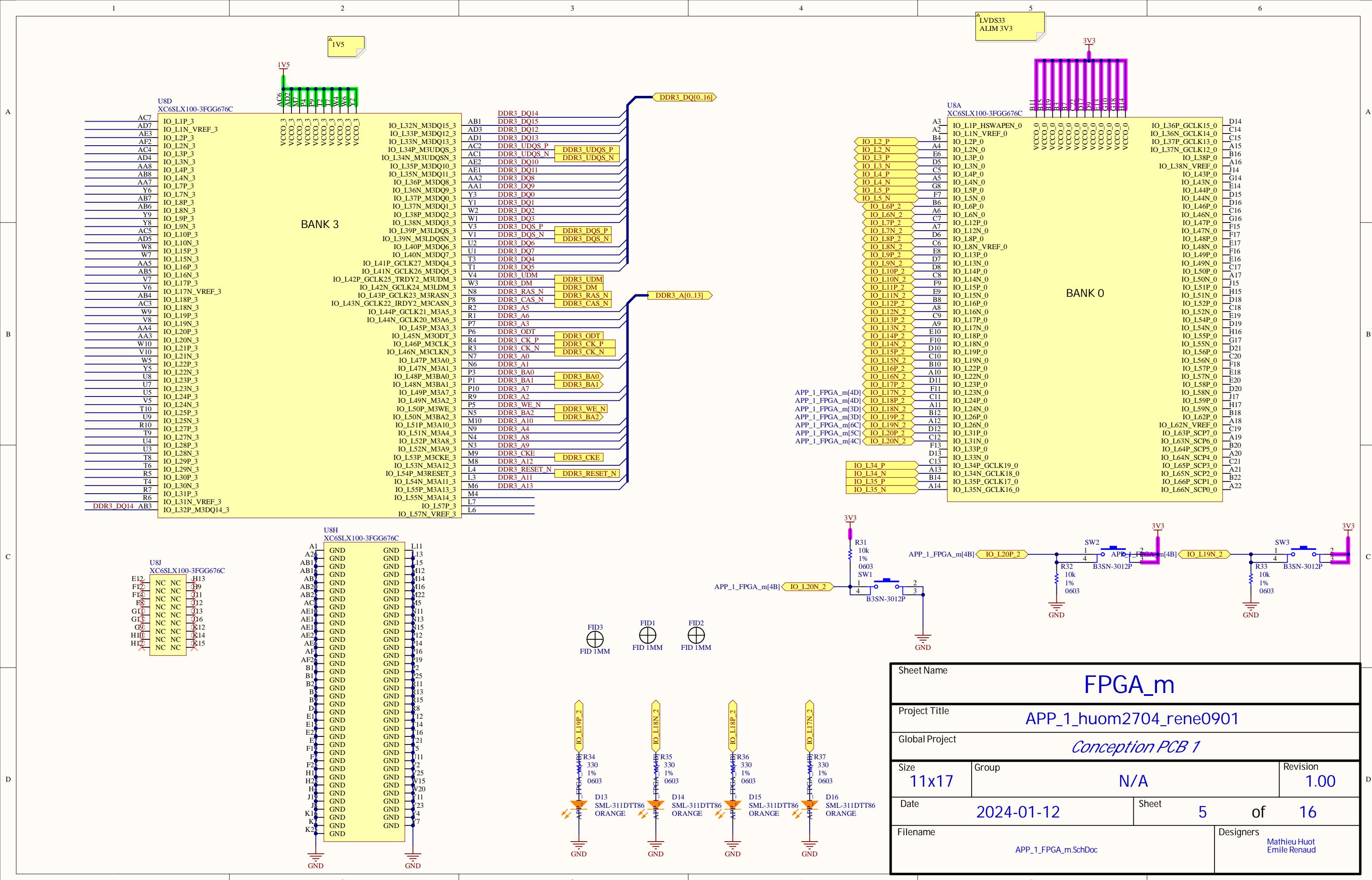
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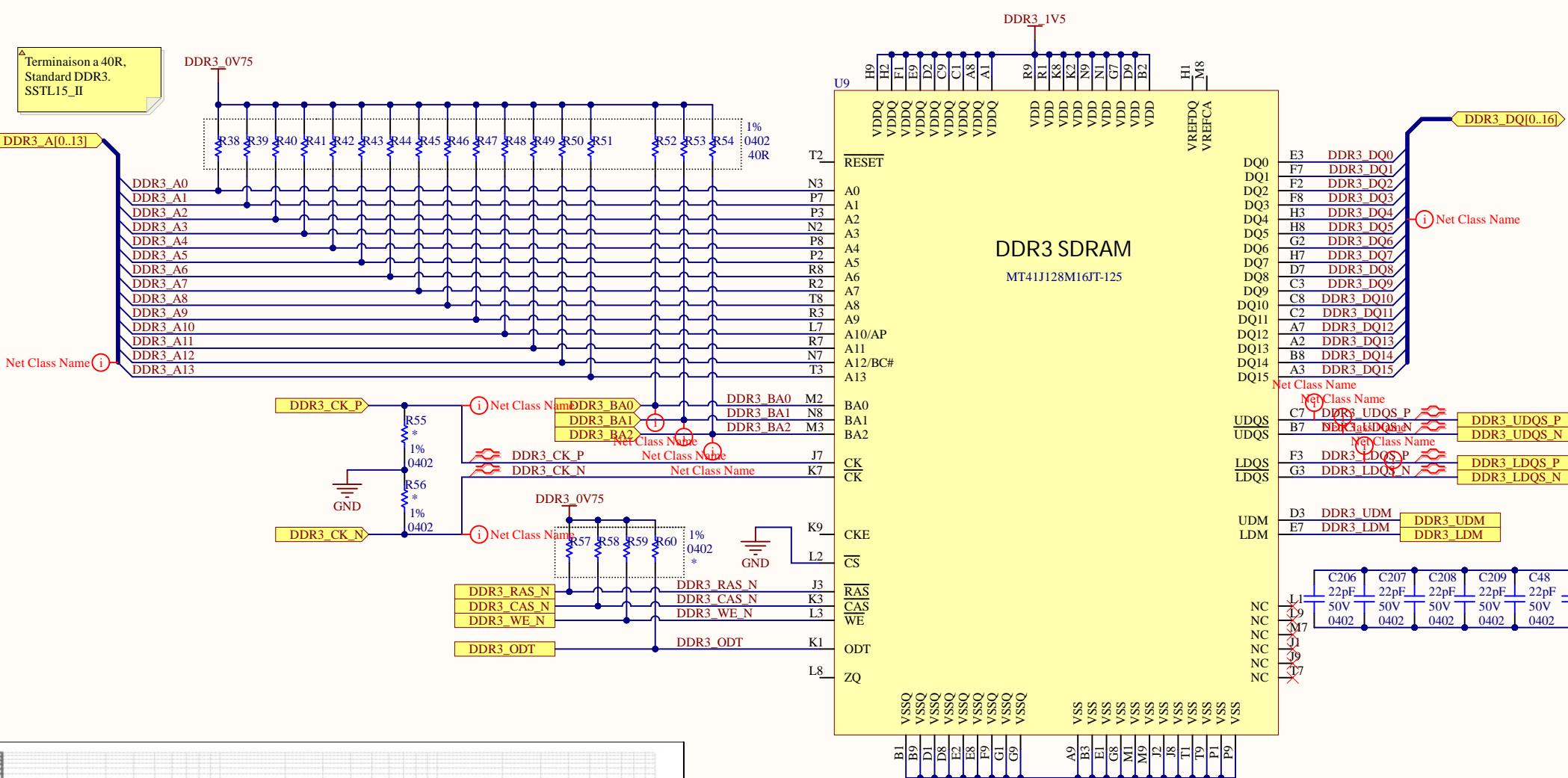
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APP_1_Connectors_m.SchDoc

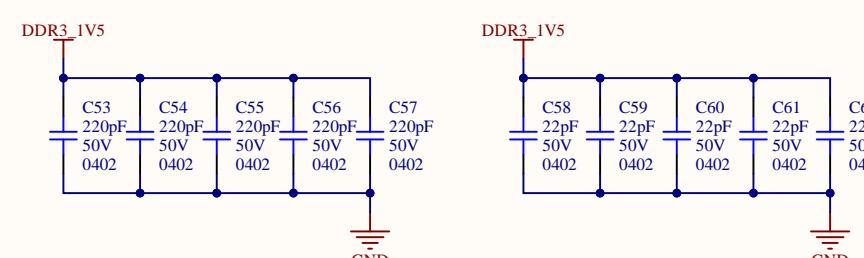
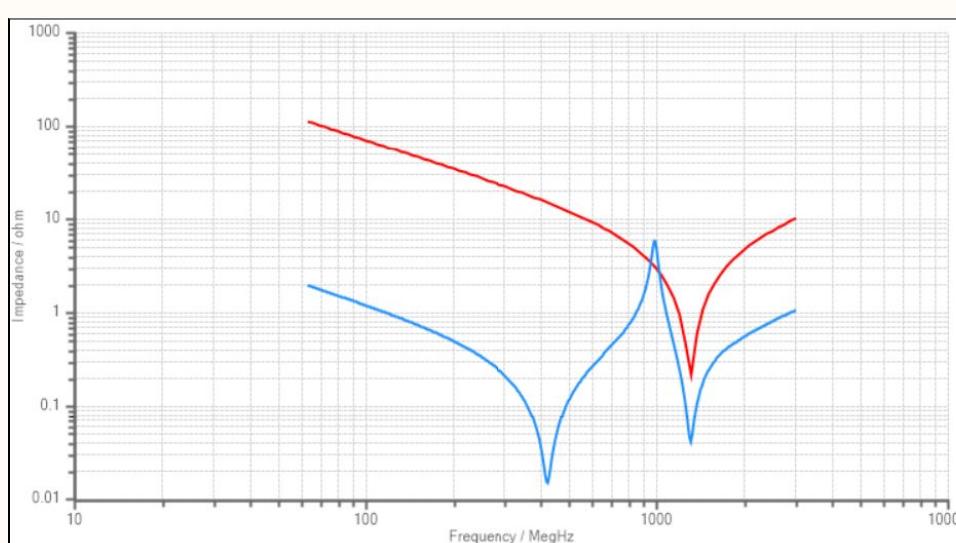
Designers

**Mathieu Huot
Emile Renaud**



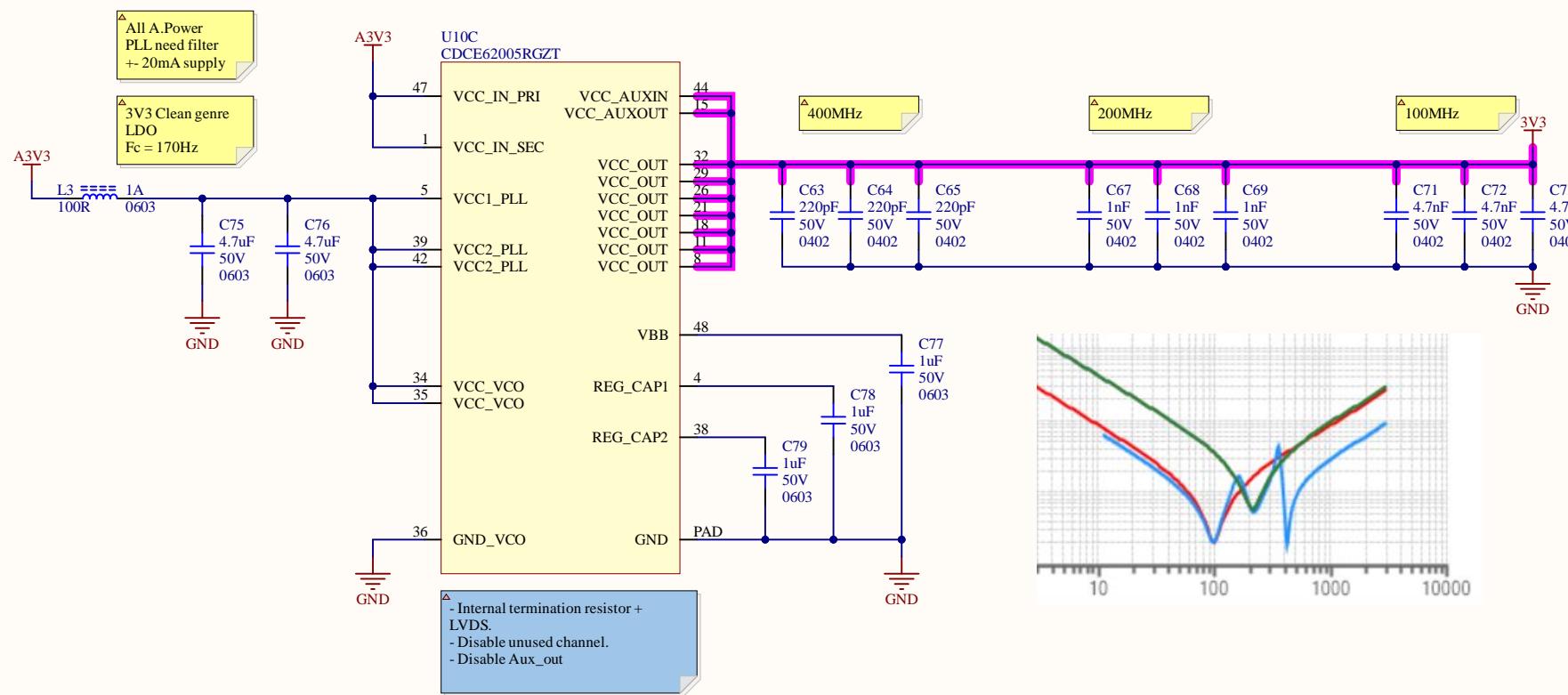


- GND
- VTT islands must be placed at the end of the memory channel, as close as possible to the last device.
 - VTT islands require at least two additional decoupling capacitors (4–7 μ F) and two bulk capacitors (100 μ F) at each end.
 - VTT island surface trace = 150 mil MIN; 250 mil preferred.
 - VTT power at initialization must be applied after VDDQ to avoid device latch-up; VTT power is nominally coincident with VREF power.

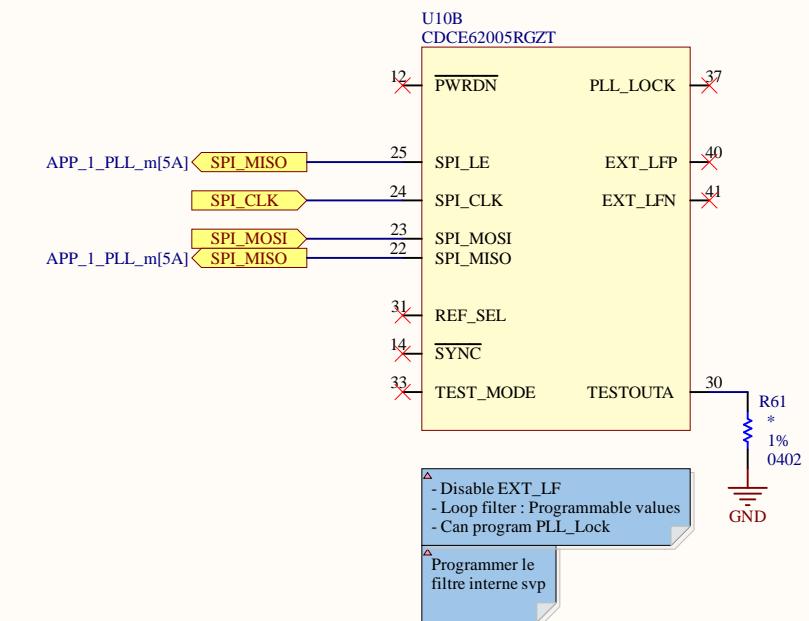


Sheet Name	DDR3_m		
Project Title	APP_1_huom2704_rene0901		
Global Project	<i>Conception PCB 1</i>		
Size	Group	N/A	Revision
11x17			1.00
Date	2024-01-12	Sheet 6	of 16
Filename	APP_1_DDR3_m.SchDoc	Designers	Mathieu Huot Emile Renaud

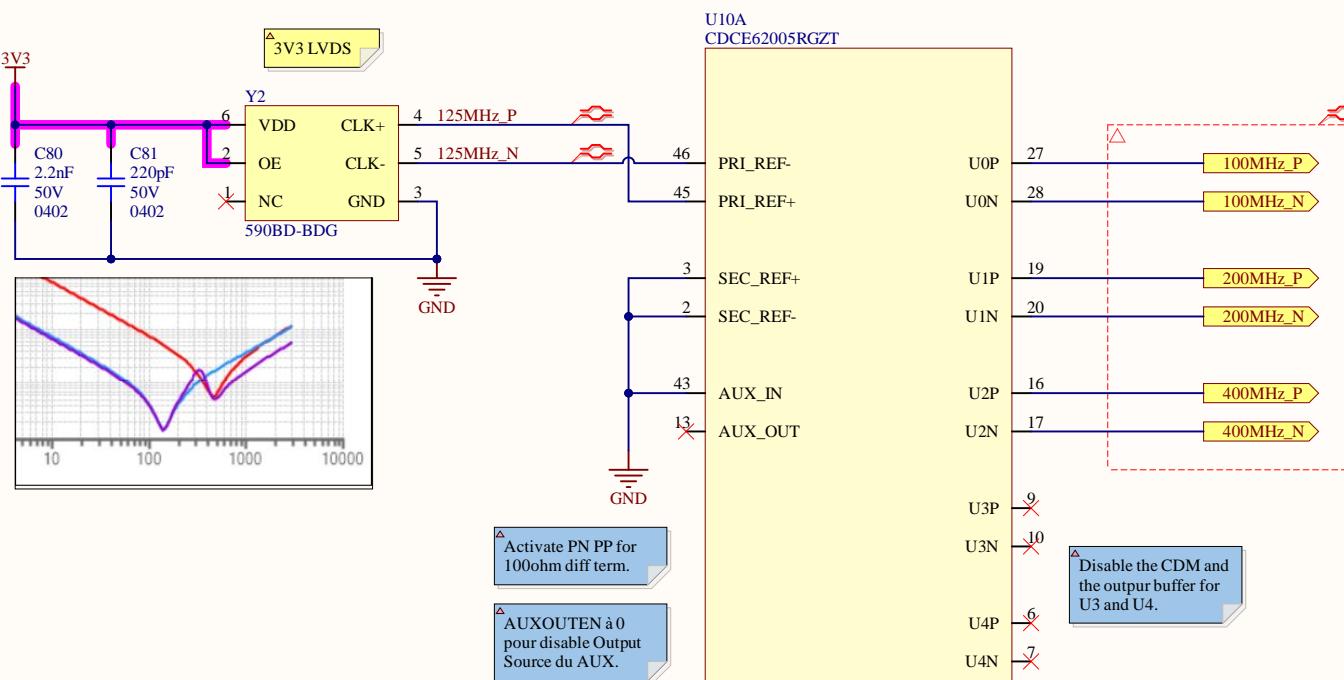
Power



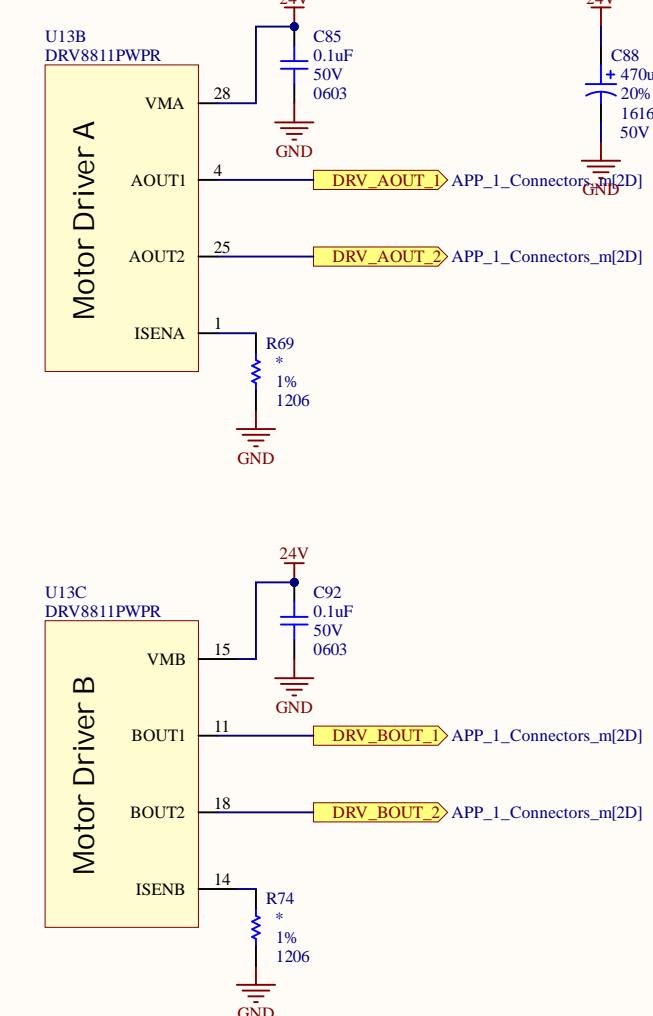
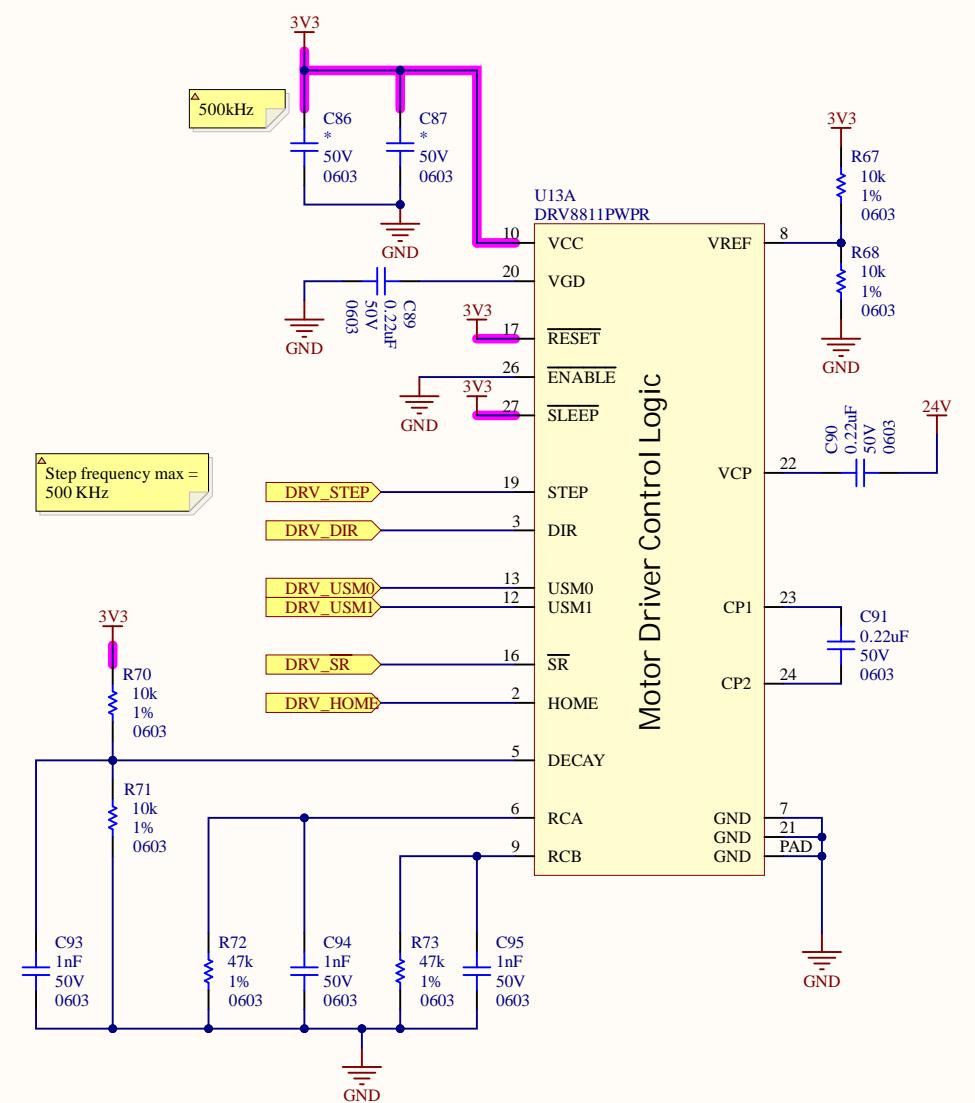
Control



PLL Clock



Sheet Name		PLL	
Project Title		APP_1_huom2704_rene0901	
Global Project		Conception PCB 1	
Size	11x17	Group	N/A
Date	2024-01-12	Sheet	7 of 16
Filename		Designers Mathieu Huot Emile Renaud	
APP_1_PLL_m.SchDoc			



10.2 Layout Example

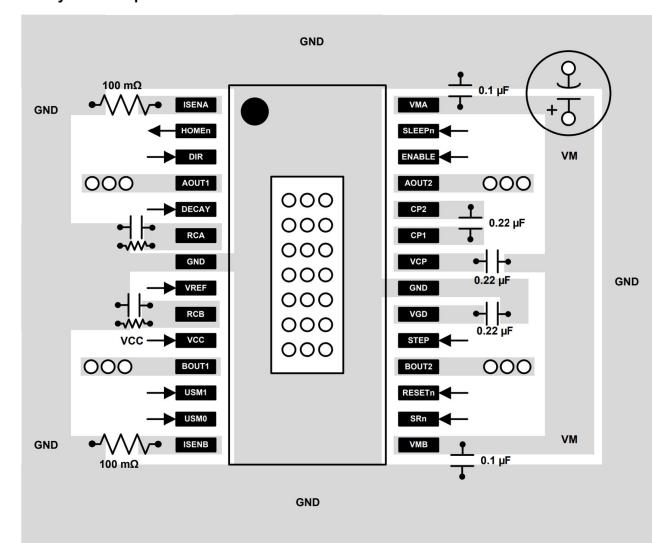
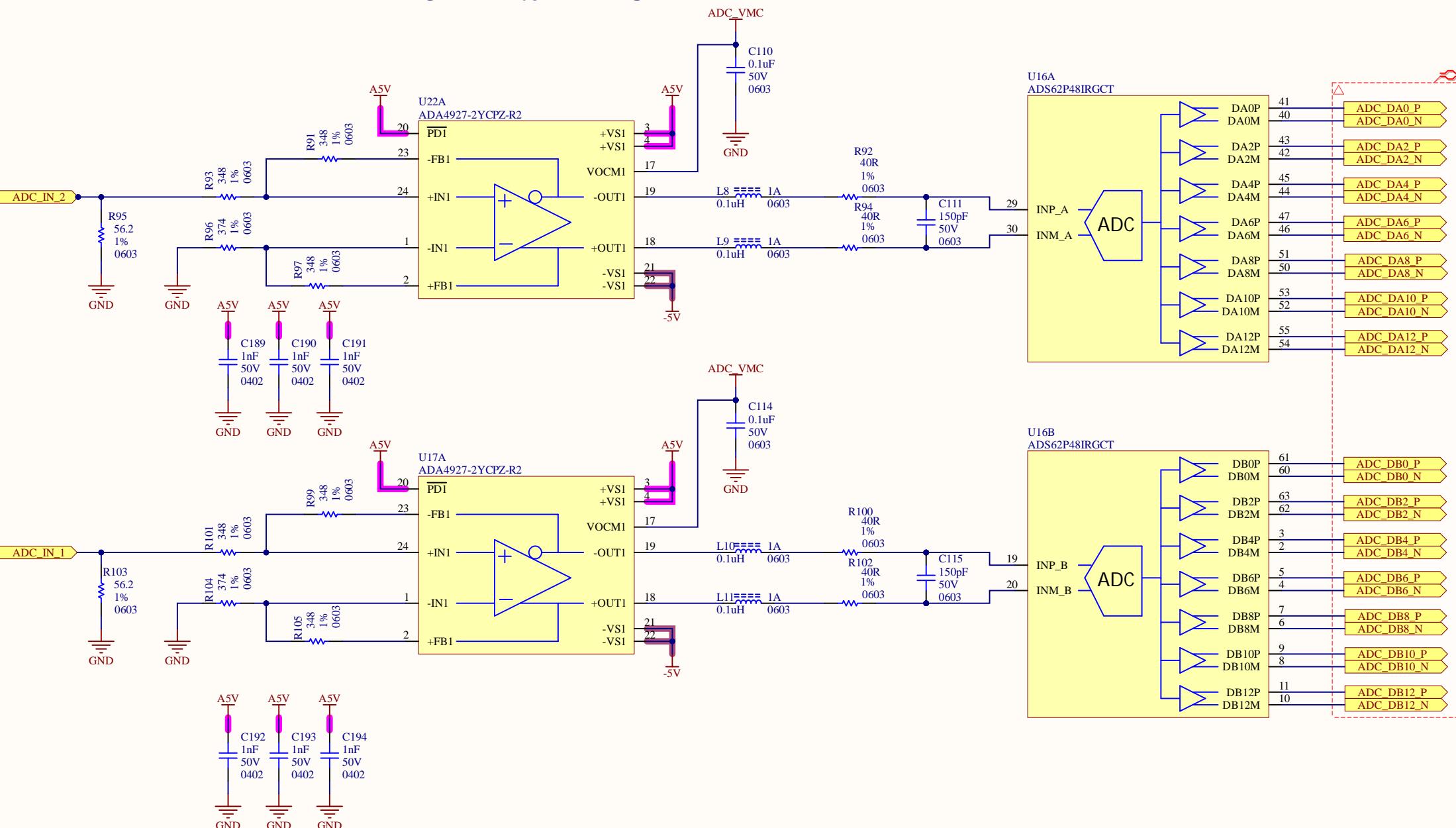


Figure 14. Layout Example Schematic

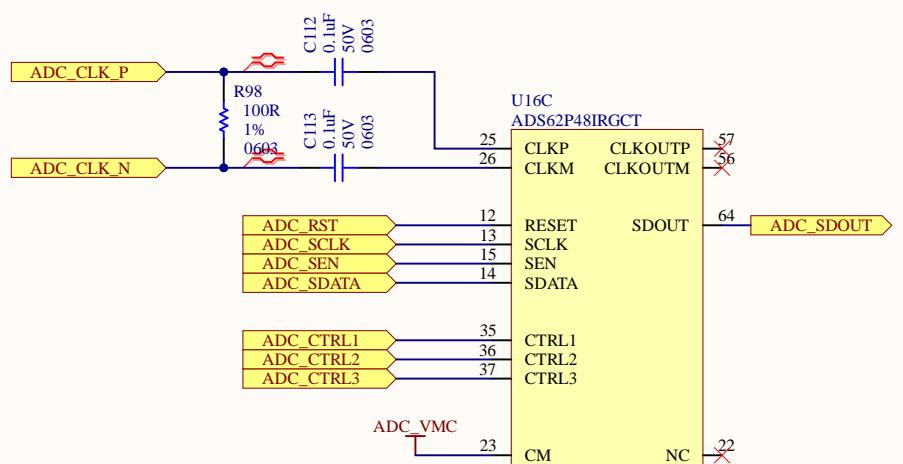
Sheet Name		DriveMoteur	
Project Title		APP_1_huom2704_rene0901	
Global Project		<i>Conception PCB 1</i>	
Size	11x17	Group	N/A
Date	2024-01-12	Sheet	8 of 16
Filename	APP_1_DriveMoteur_m.SchDoc	Designers	Mathieu Huot Emile Renaud

OP - Filter - ADC

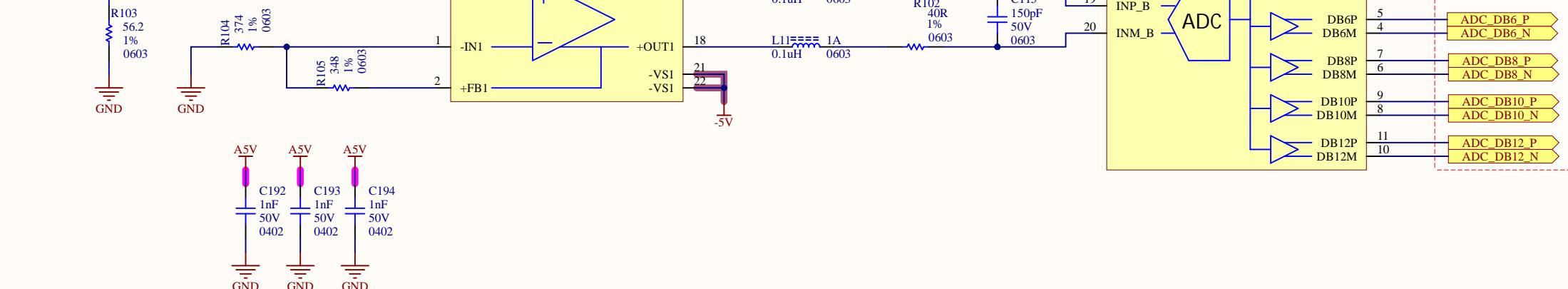
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Control

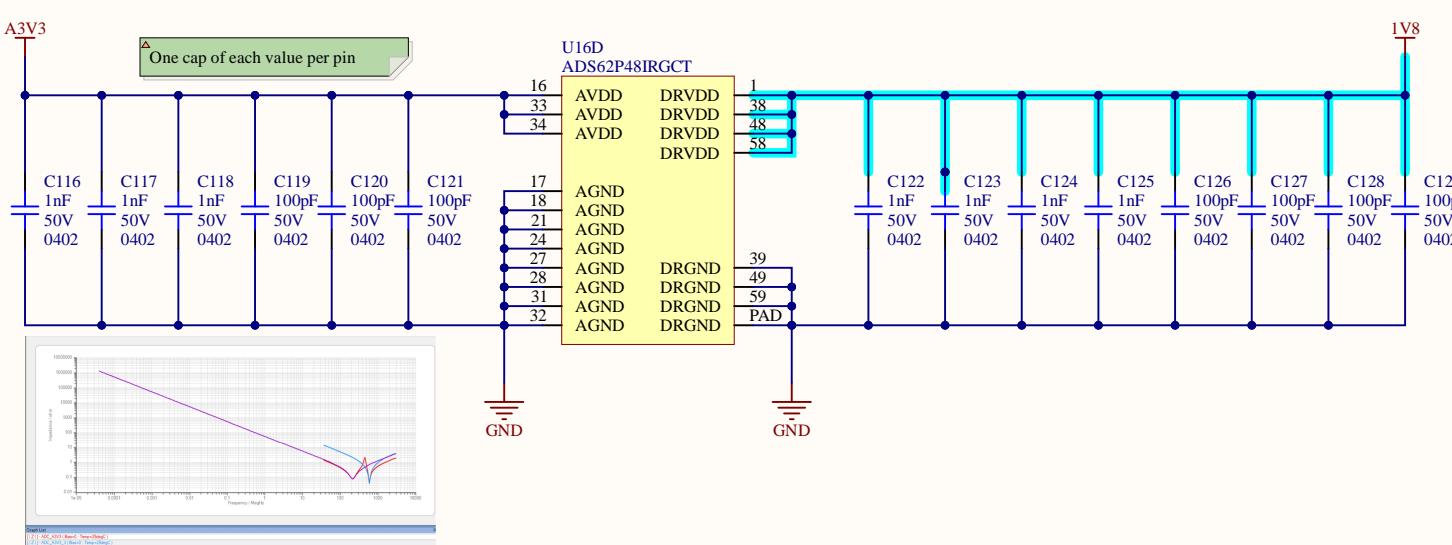


B



C

Power



Sheet Name	
ADC	
Project Title	
APP_1_huom2704_rene0901	Revision
Conception PCB 1	1.00
Size	11x17
Group	N/A
Date	2024-01-12
Sheet	9 of 16
Filename	APP_1_ADC.m.SchDoc
Designers	Mathieu Huot Emile Renaud

D

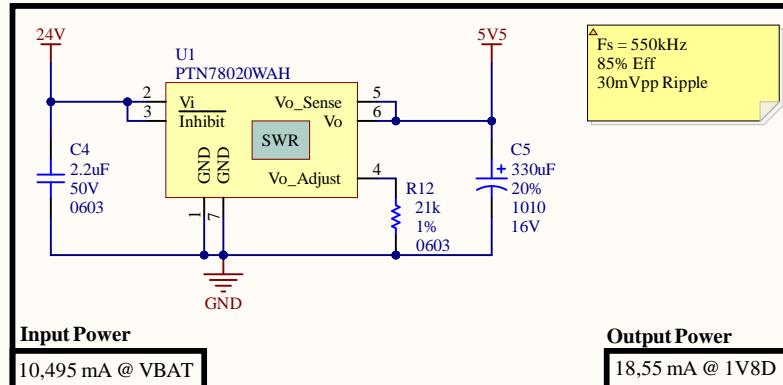
A

B

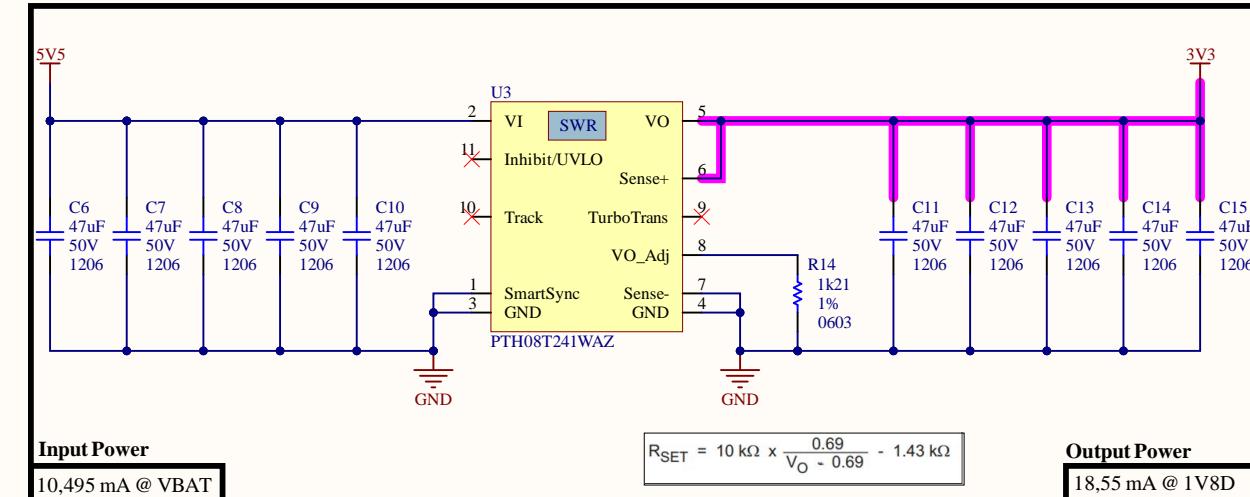
C

D

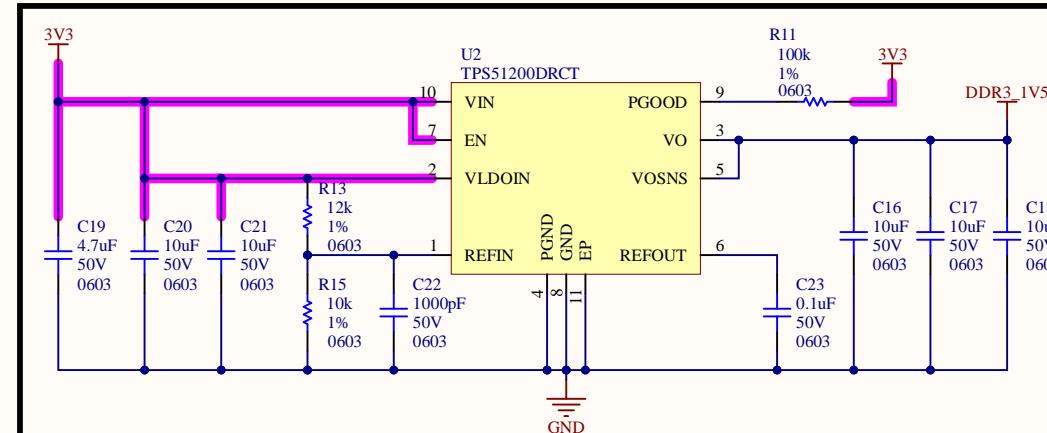
SWR 24V->5V



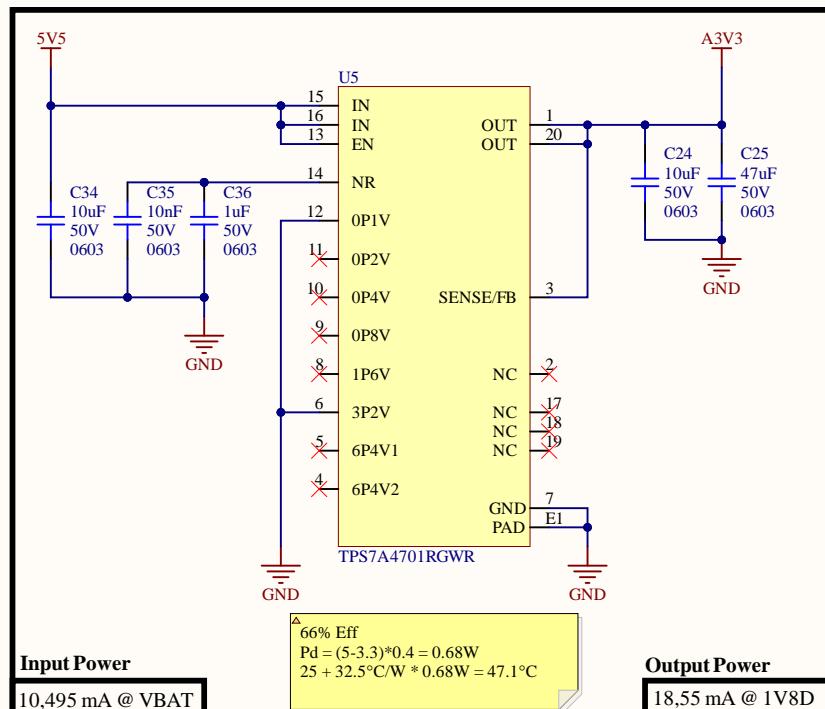
SWR 5V->3V3



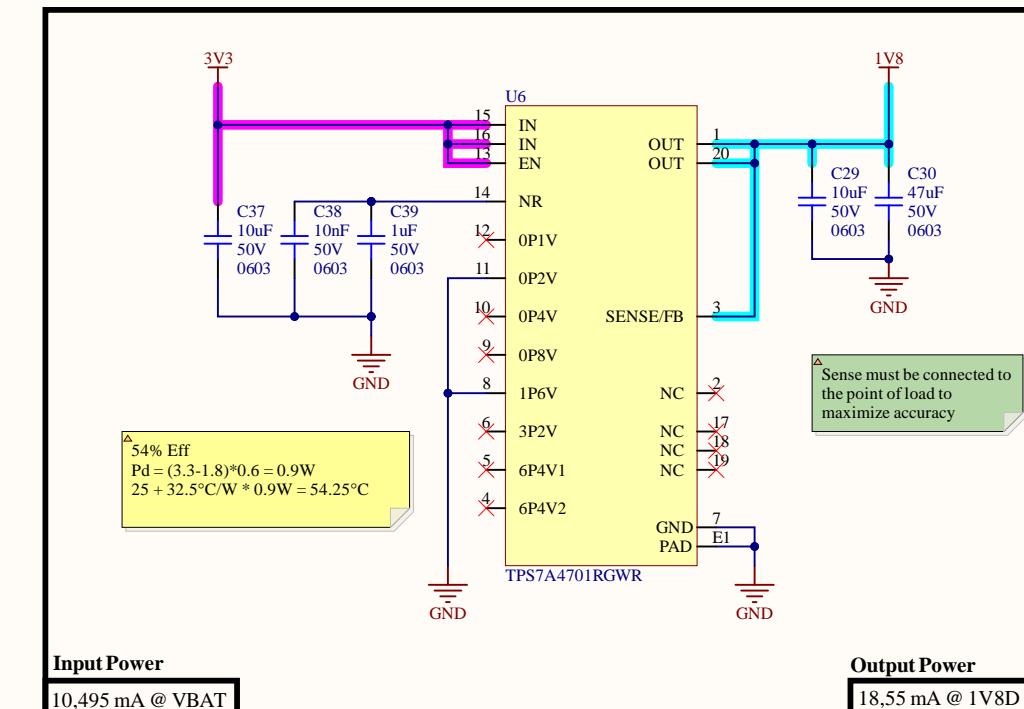
LDO DDR3 1V5 & 0V75



LDO 5V->A3V3



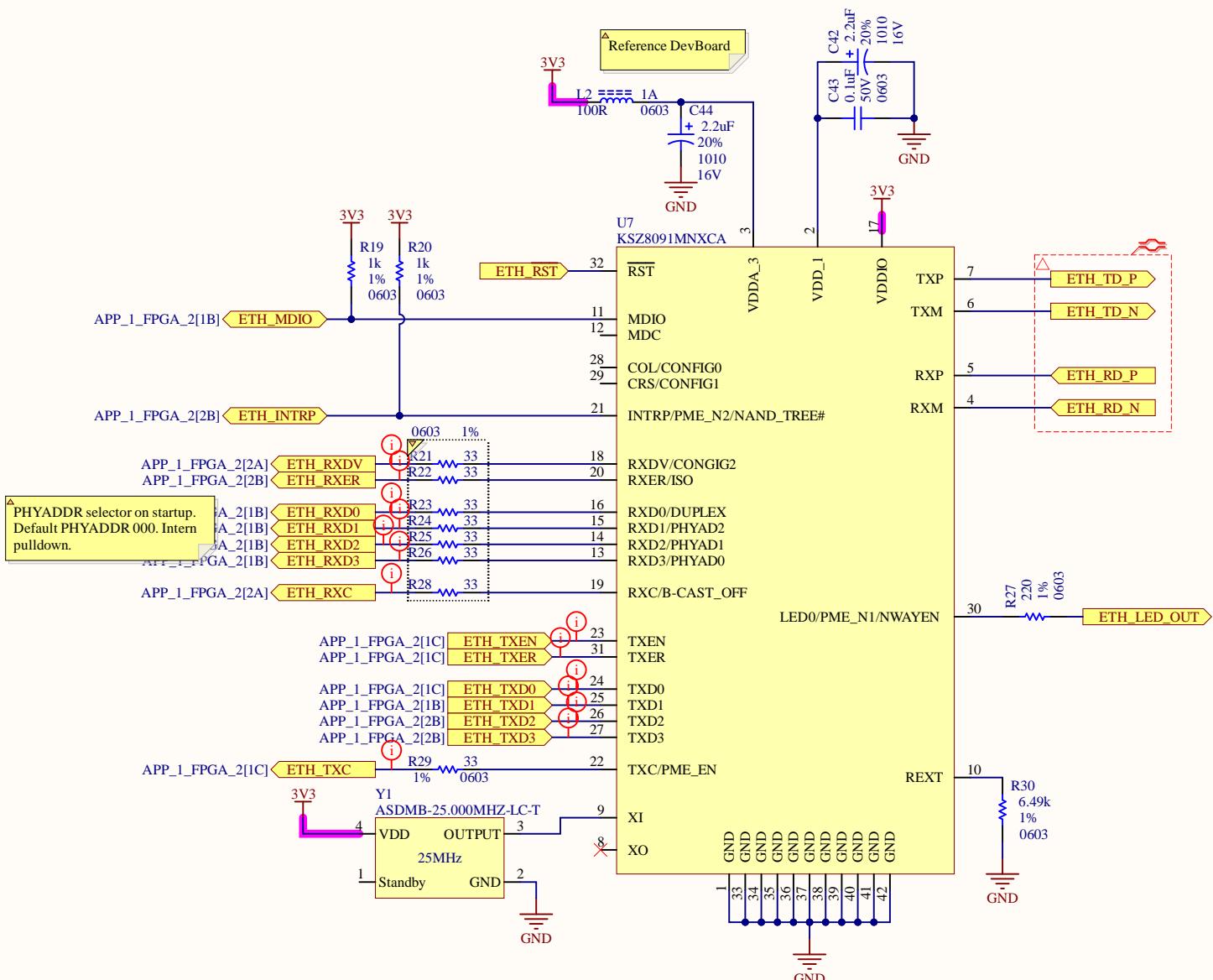
LDO 3V3->1V8



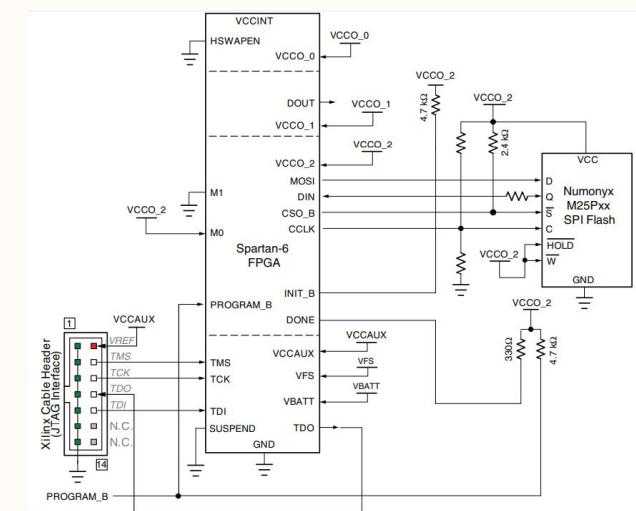
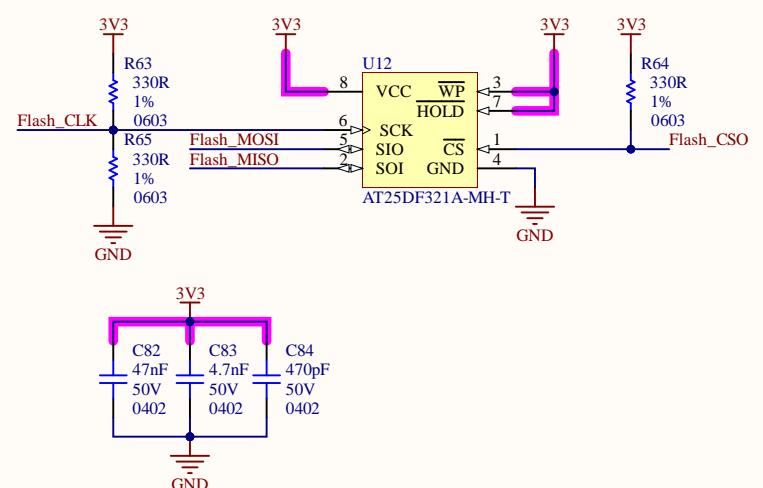
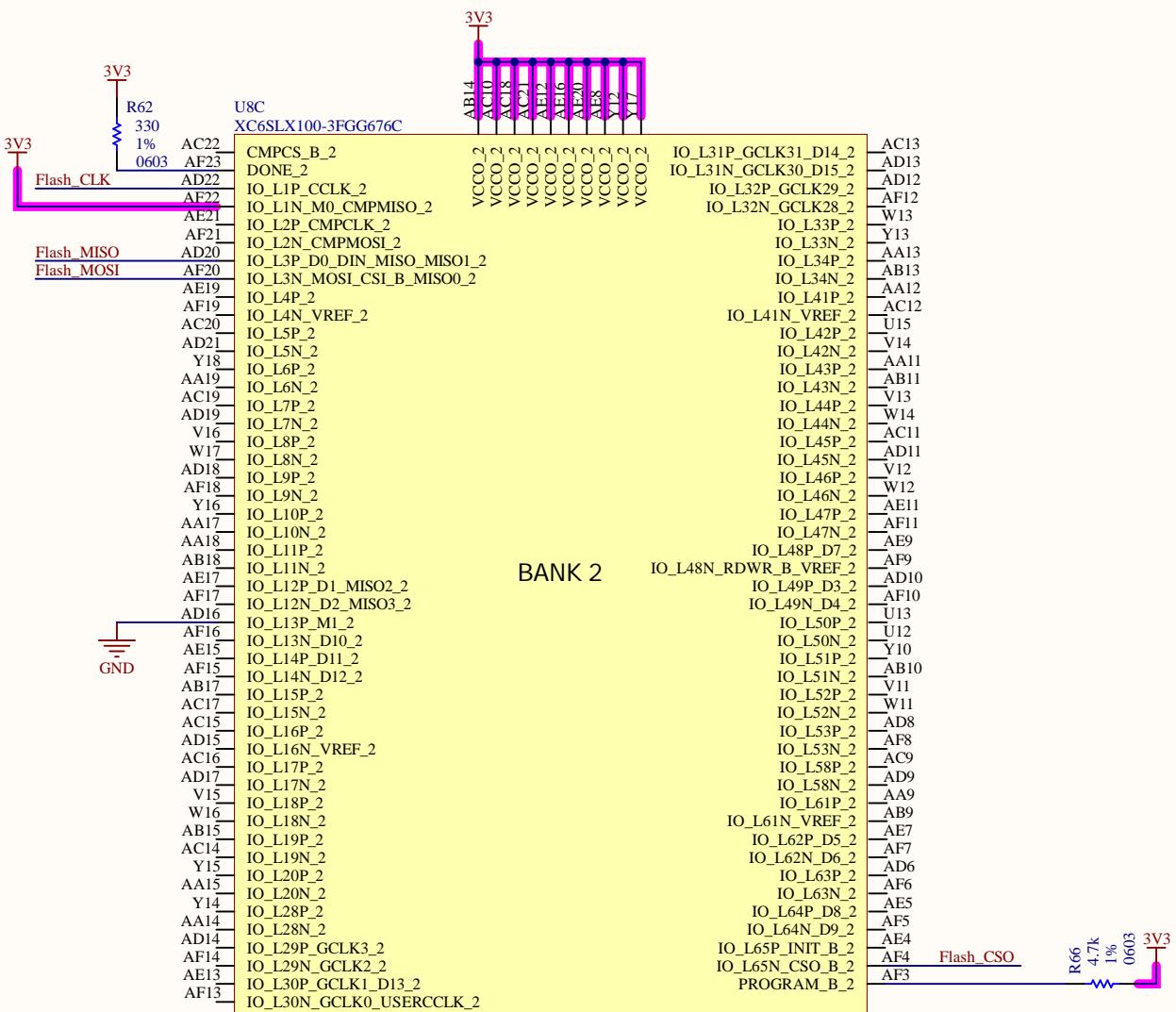
Input Power: 10,495 mA @ VBAT **Output Power:** 18.55 mA @ 1V8D

Sheet Name		Power	
Project Title		APP_1_huom2704_rene0901	
Global Project		Conception PCB 1	
Size	Group	N/A	Revision
11x17			1.00
Date	2024-01-12	Sheet	10 of 16
Filename	APP_1_Power_m.SchDoc	Designers	Mathieu Huot Emile Renaud

Ethernet



Sheet Name	Ethernet		
Project Title	APP_1_huom2704_rene0901		
Global Project	<i>Conception PCB 1</i>		
Size	11x17	Group	N/A
Revision			1.00
Date	2024-01-12	Sheet	11 of 16
Filename	APP_1_Ethernet_m.SchDoc		
Designers	Mathieu Huot Emile Renaud		

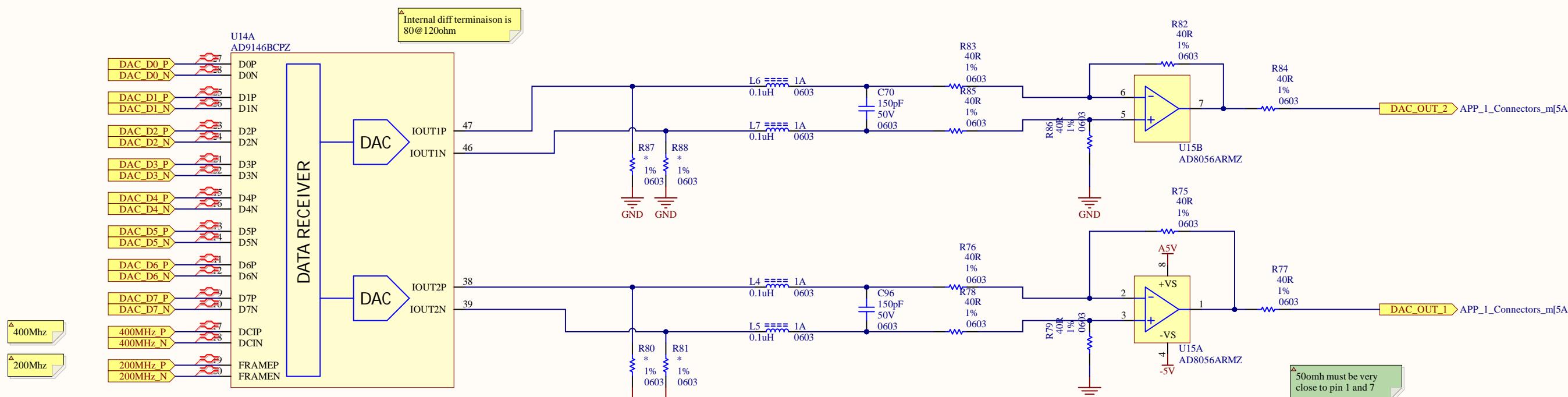


Refer to the Notes following this figure for related information.
UD0001_02_000010

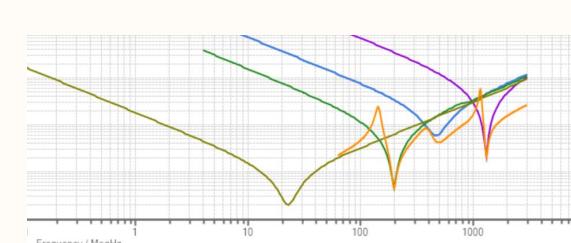
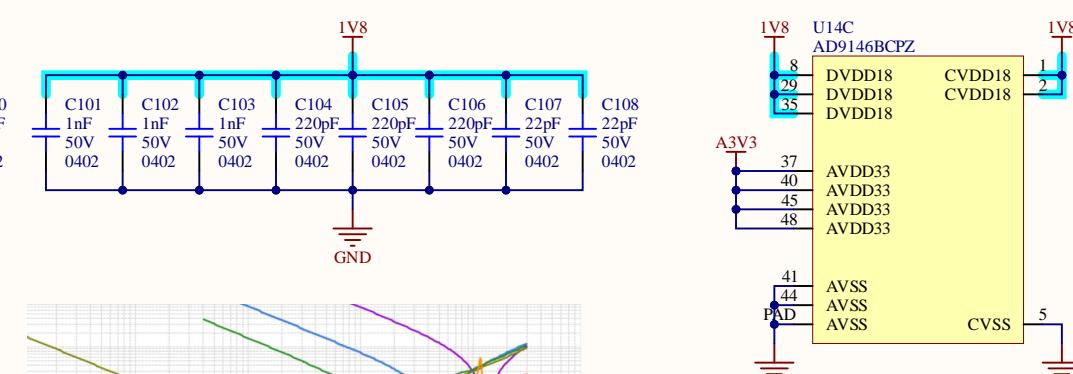
Figure 2-12: Spartan-6 FPGA SPI Configuration Interface

Sheet Name		FLASH	
Project Title		APP_1_huom2704_rene0901	
Global Project		Conception PCB 1	
Size	11x17	Group	N/A
Revision	1.00		
Date	2024-01-12	Sheet	12 of 16
Filename	APP_1_Flash_m.SchDoc	Designers	Mathieu Huot Emile Renaud

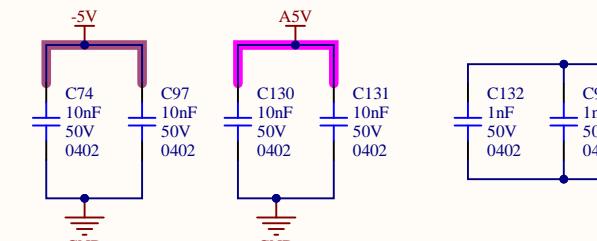
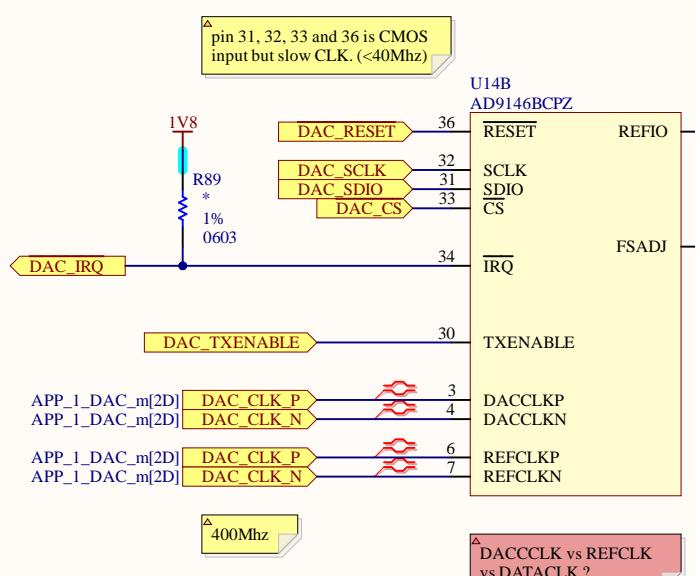
DATA - DAC - Filter



Power

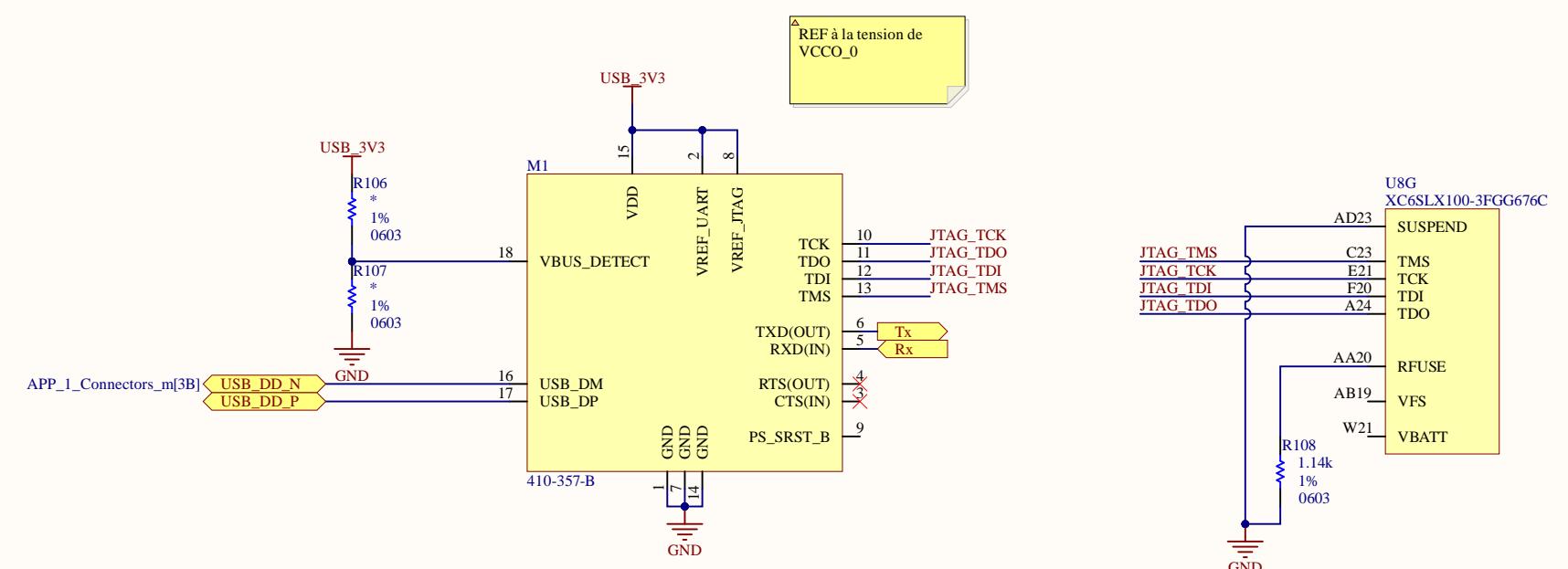


Control



Sheet Name	DAC	
Project Title	APP_1_huom2704_rene0901	
Global Project	Conception PCB 1	
Size	11x17	Group
Date	2024-01-12	Sheet
Filename	APP_1_DAC_m.SchDoc	Designers
		Mathieu Huot Emile Renaud

JTAG



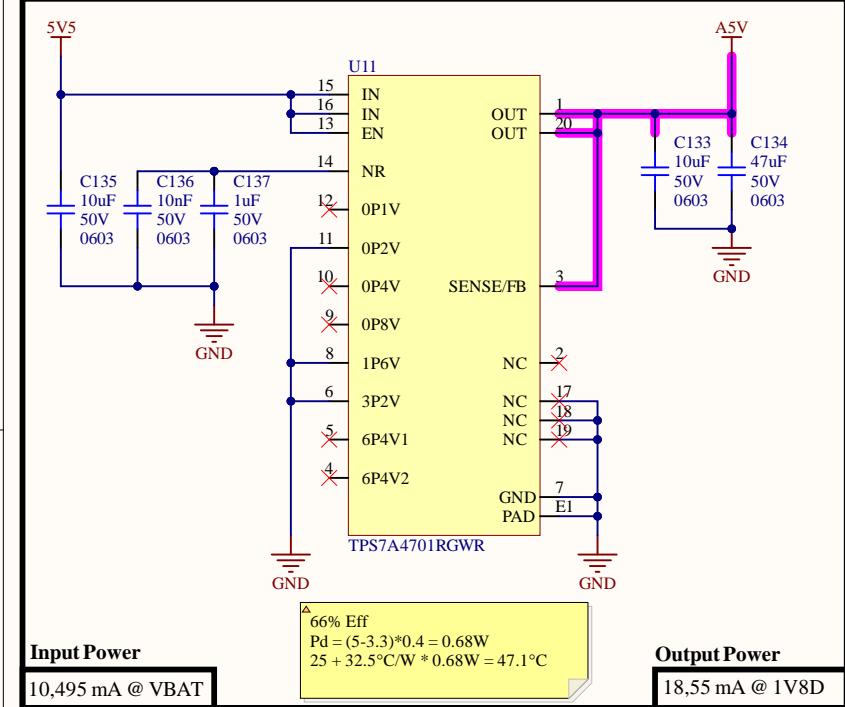
V_{BATT}	Key memory battery backup supply (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)	-0.5 to 4.05	V
V_{FS}	External voltage supply for eFUSE programming (LX75, LX75T, LX100, LX100T, LX150, and LX150T only) ⁽²⁾	-0.5 to 3.75	V

Table 3: eFUSE Programming Conditions⁽¹⁾

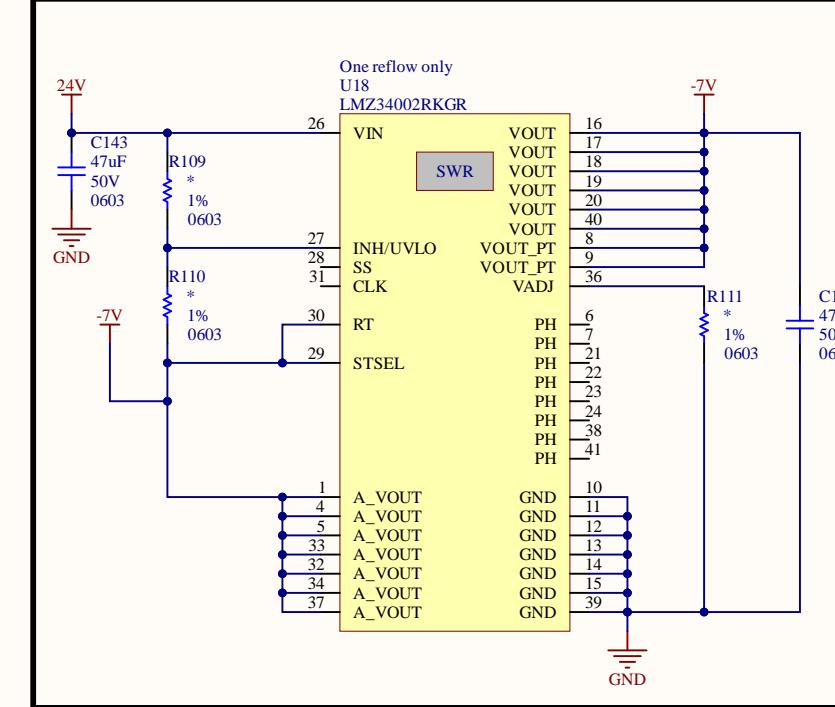
Symbol	Description	Min	Typ	Max	Units
$V_{FS}^{(2)}$	External voltage supply	3.2	3.3	3.4	V
I_{FS}	V_{FS} supply current	—	—	40	mA
V_{CCAUX}	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
$R_{FUSE}^{(3)}$	External resistor from R_{FUSE} pin to GND	1129	1140	1151	Ω
V_{CCINT}	Internal supply voltage relative to GND	1.14	1.2	1.26	V
t_j	Temperature range	15	—	85	°C
...					

Sheet Name			
JTAG			
Project Title			
APP_1_huom2704_rene0901			
Global Project			
<i>Conception PCB 1</i>			
Size	Group	Revision	
11x17		N/A	
Date	Sheet		Revision
2024-01-12	14		1.00
Filename			Designers
APP_1_JTAG_m.SchDoc			Mathieu Huot Emile Renaud

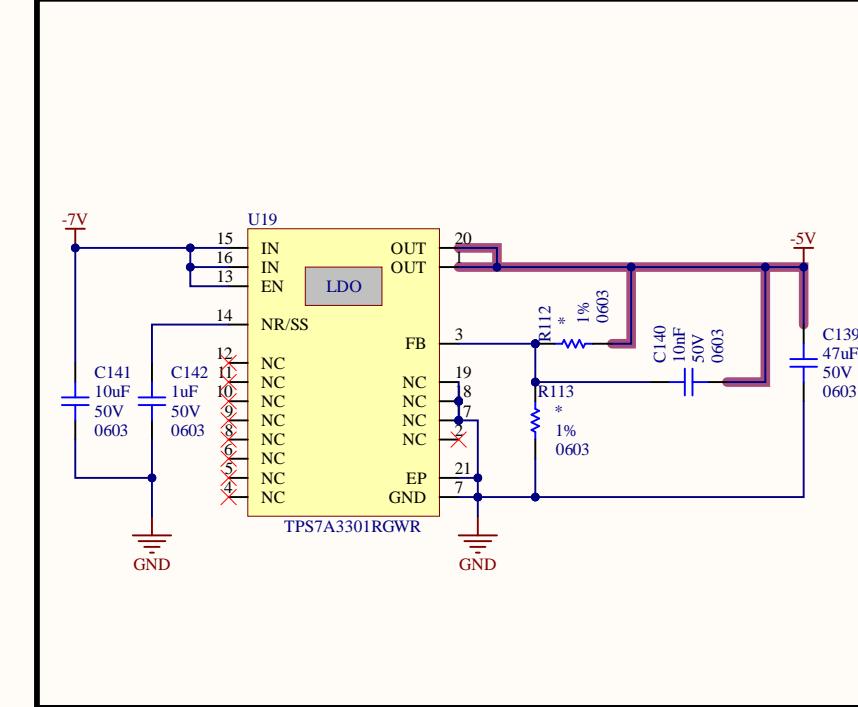
LDO 5V5 -> A5V



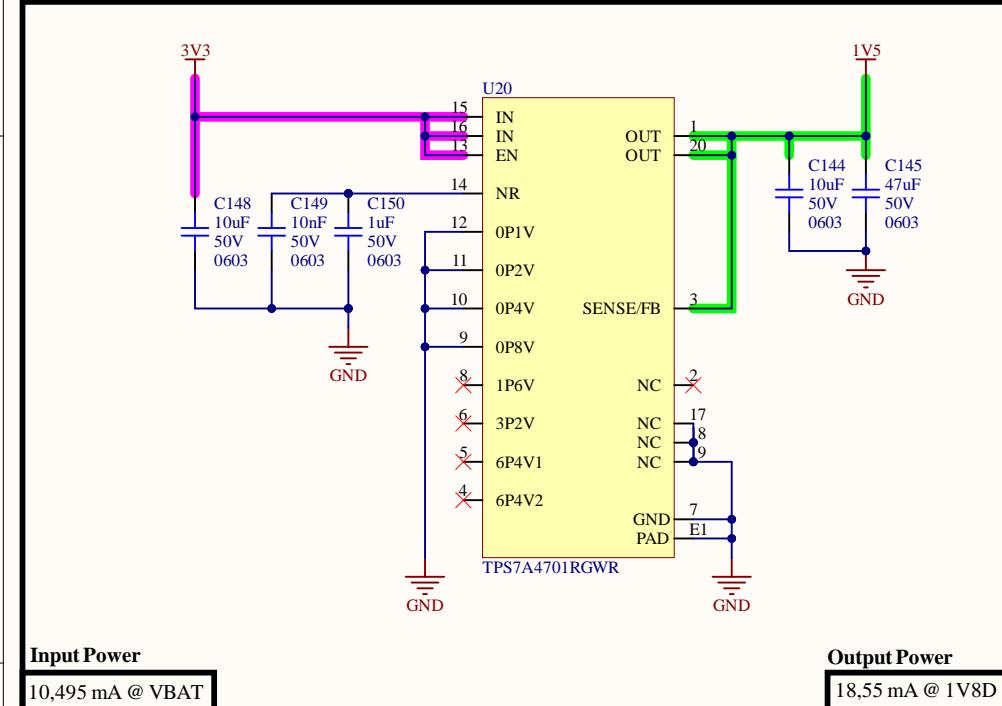
SWR 24->-7V



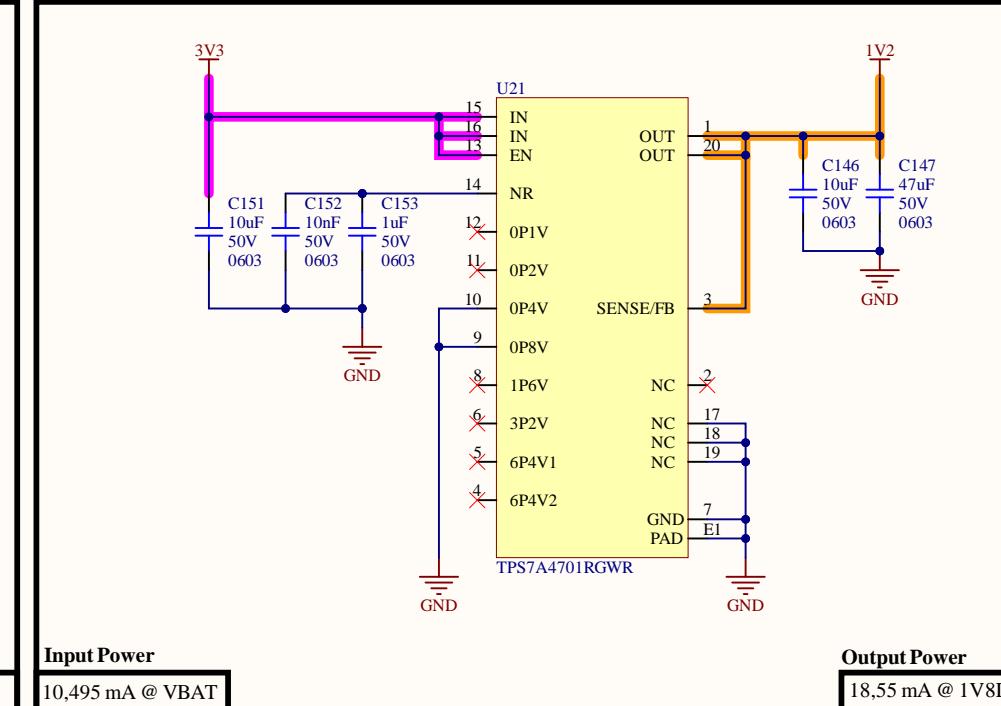
LDO -7V -> -5V



LDO 3V3->1V5



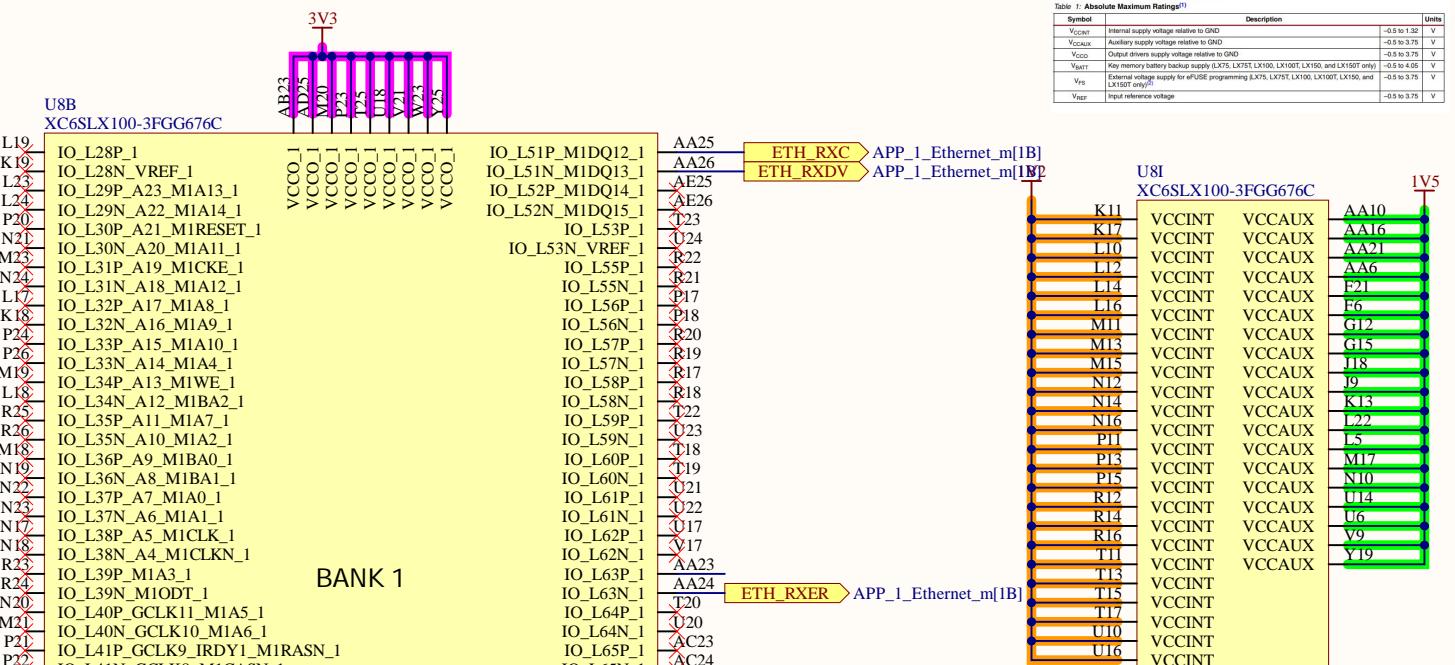
LDO 3V3->1V2



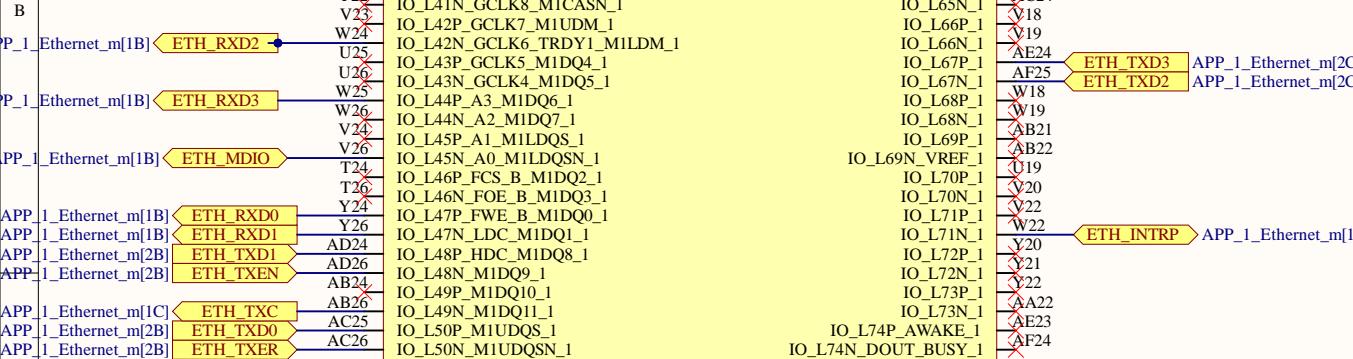
Input Power Output Power
10,495 mA @ VBAT 18,55 mA @ 1V8D

Sheet Name		Power	
Project Title		APP_1_huom2704_rene0901	
Global Project		Conception PCB 1	
Size	Group	N/A	Revision
11x17		1.00	
Date	2024-01-12	Sheet	15 of 16
Filename	APP_1_PowerAnalog.SchDoc		Designers
	Mathieu Huot Emile Renaud		

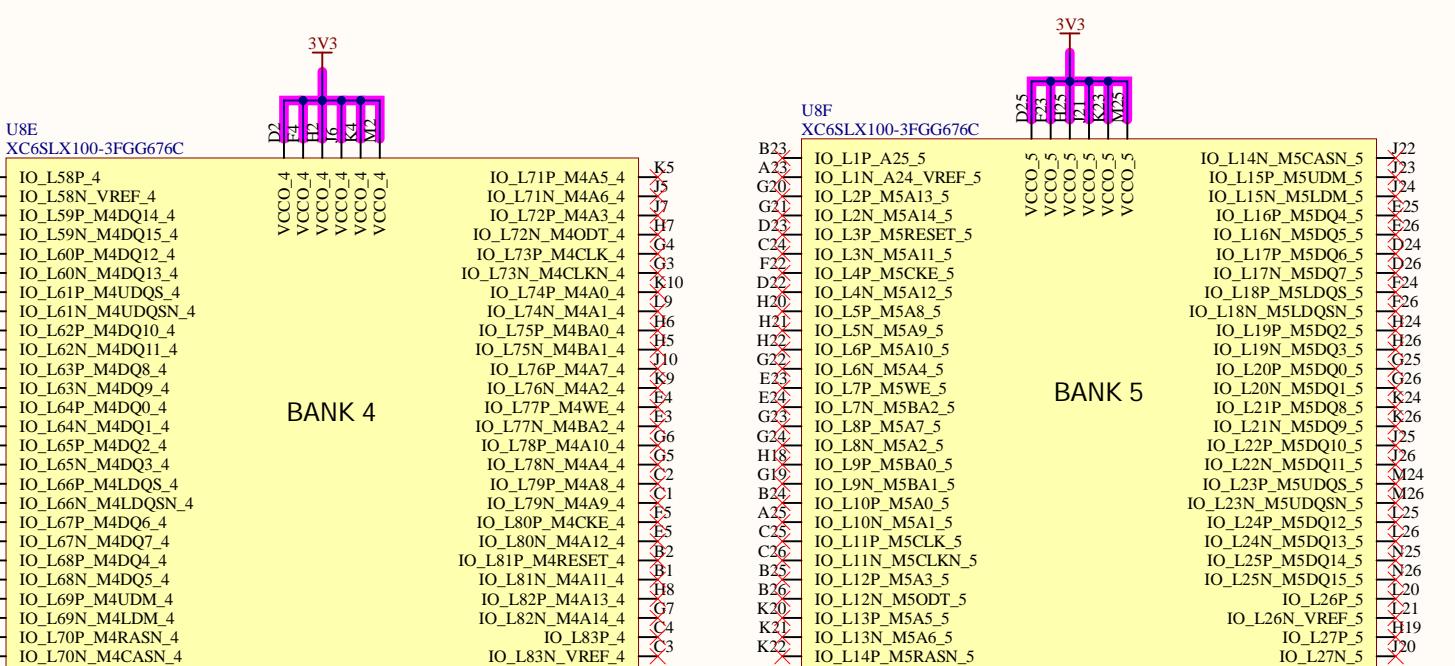
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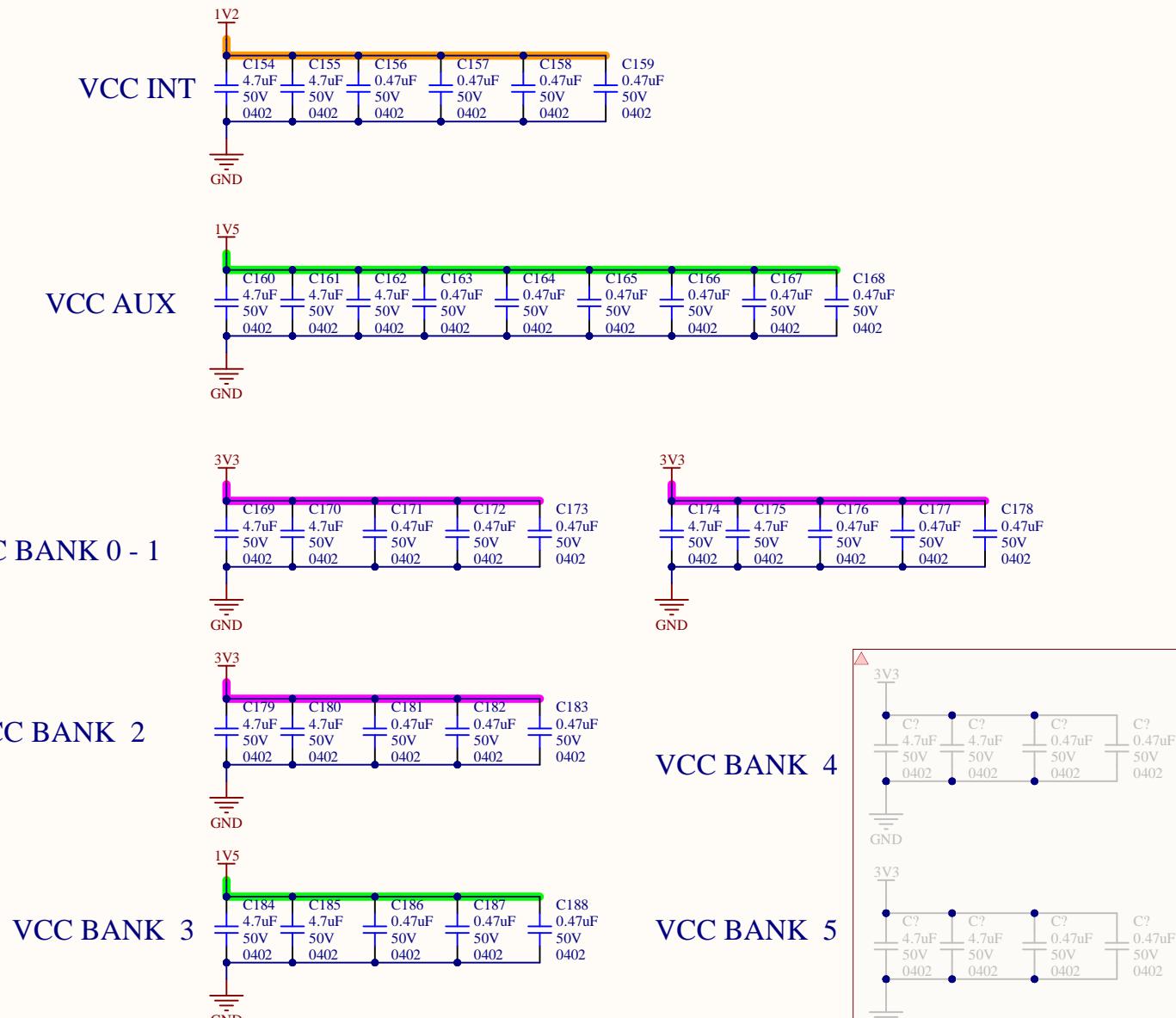
B



C



D



Sheet Name

FPGA_2

Project Title

Global Project

Size

11x17

Group

Revision

1.00

Date

2024-01-12

Sheet

16 of 16

Filename

Designers

Mathieu Huot
Emile Renaud