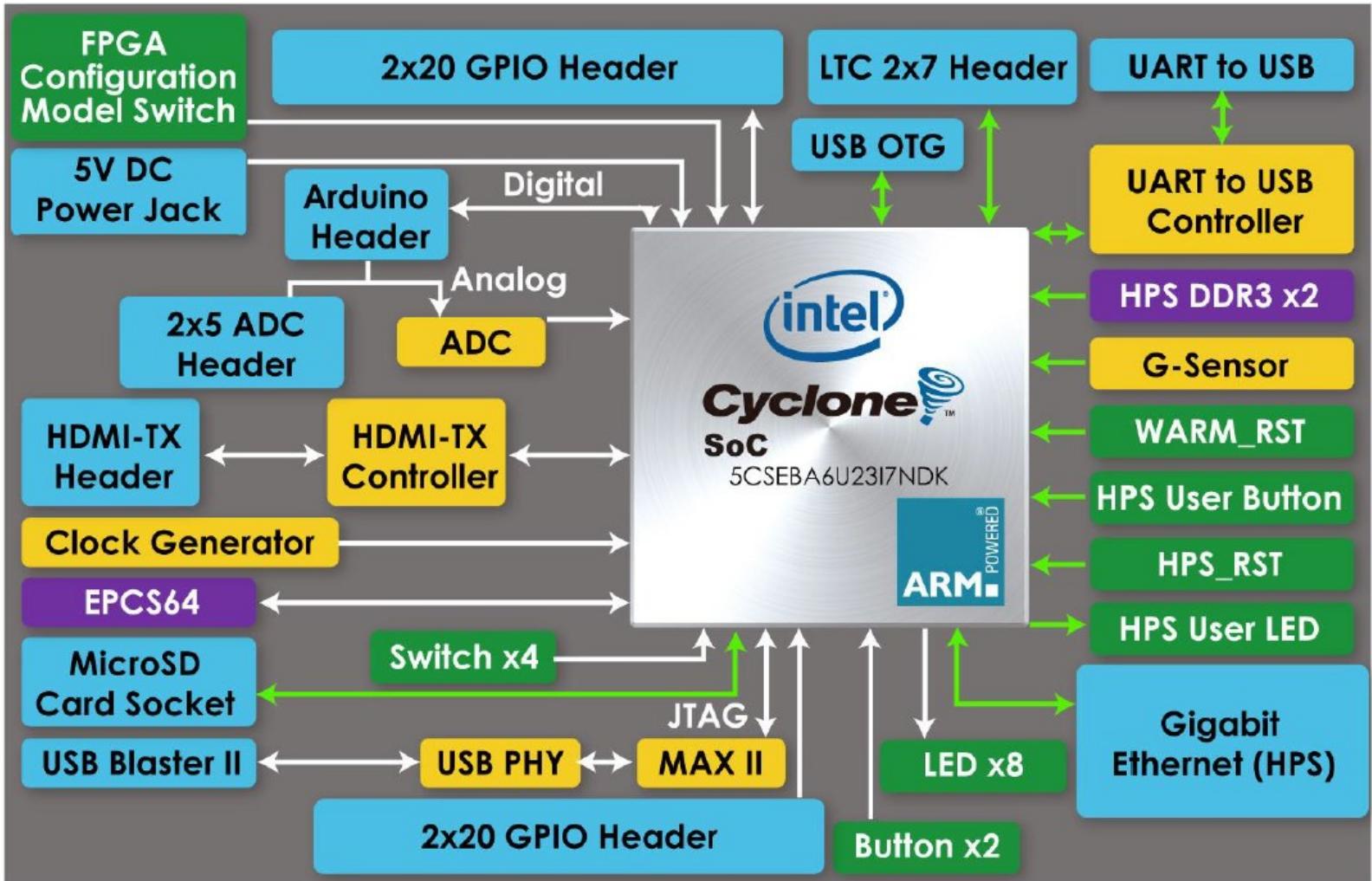


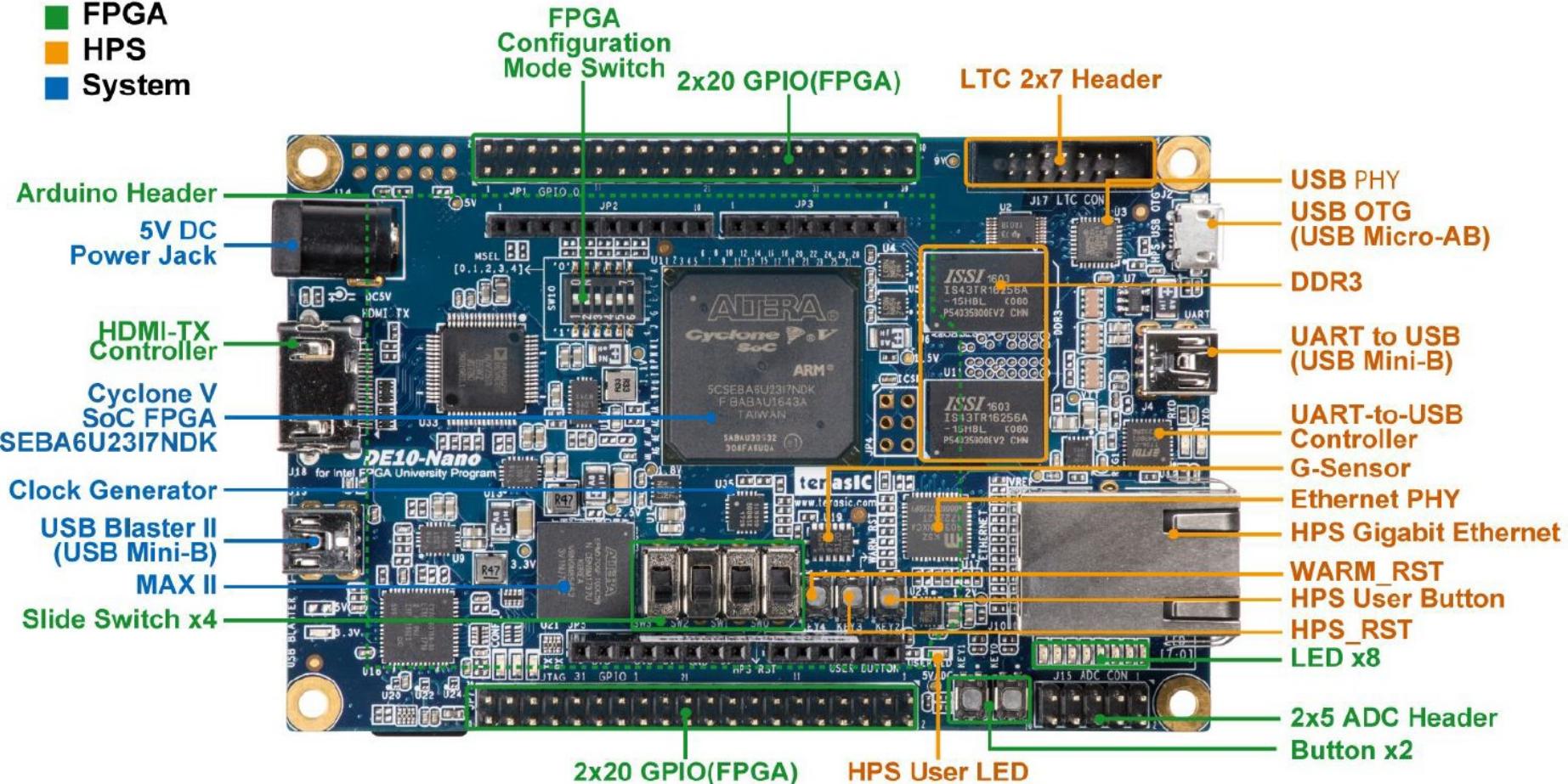
DE10-Nano development board

DE10-Nano



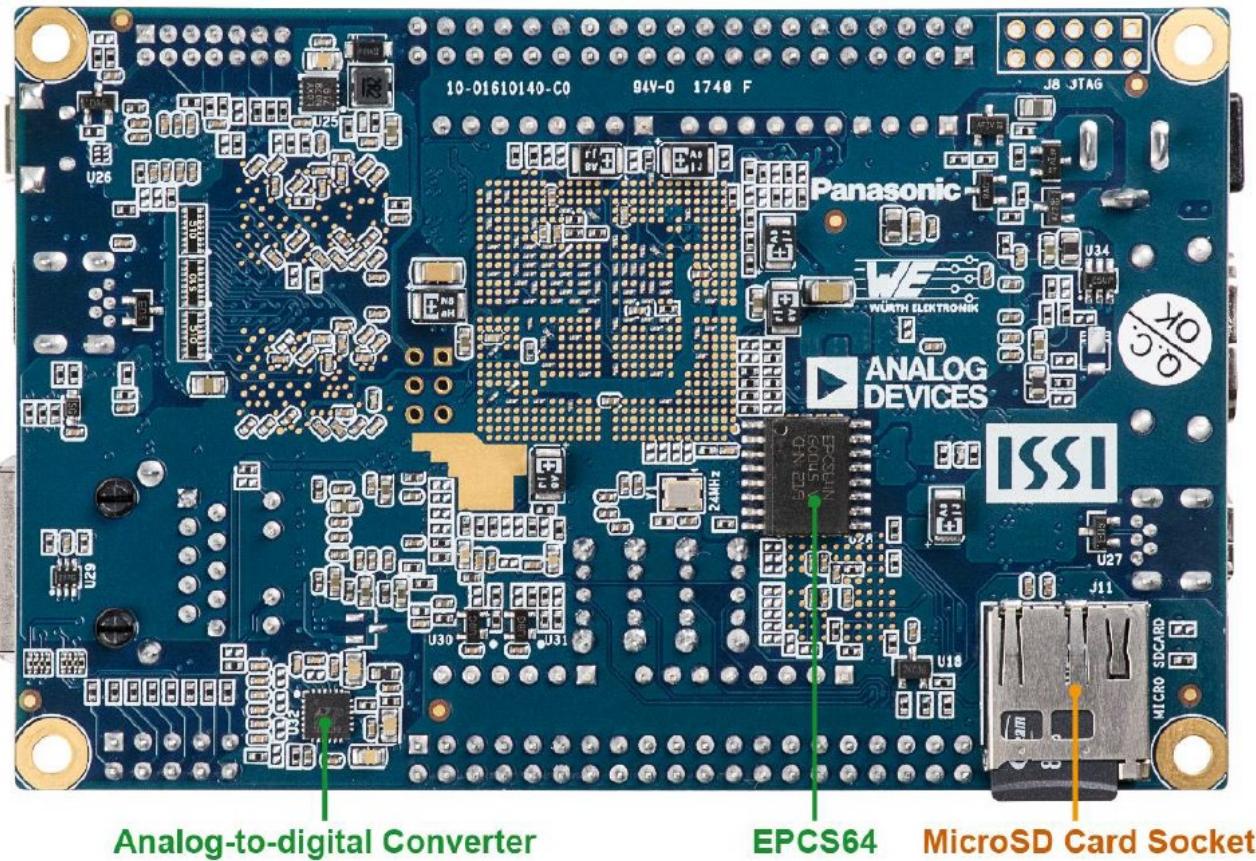
DE10-Nano

- FPGA
- HPS
- System



DE10-Nano

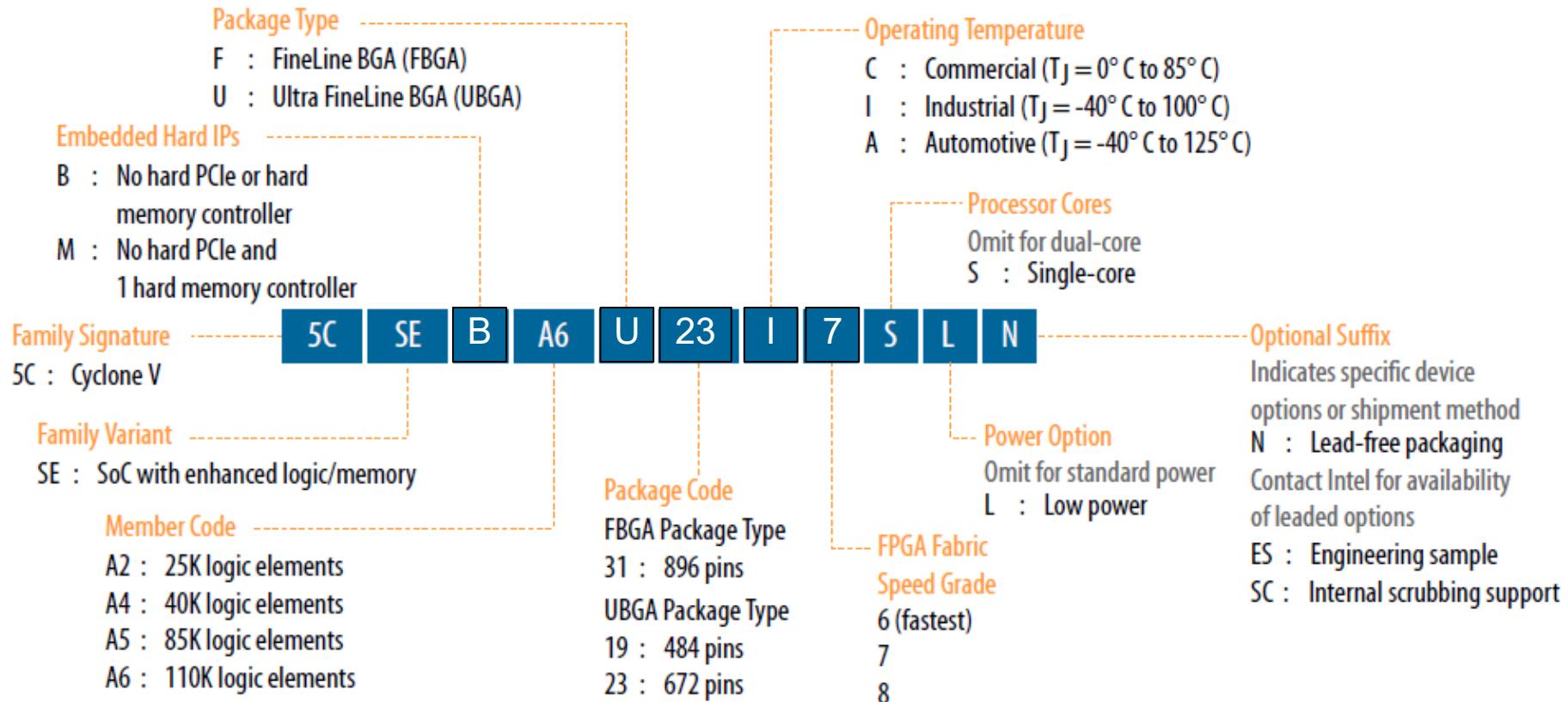
- FPGA
- HPS



ALTERA®

Cyclone® V SE 5CSEBA6U23I7

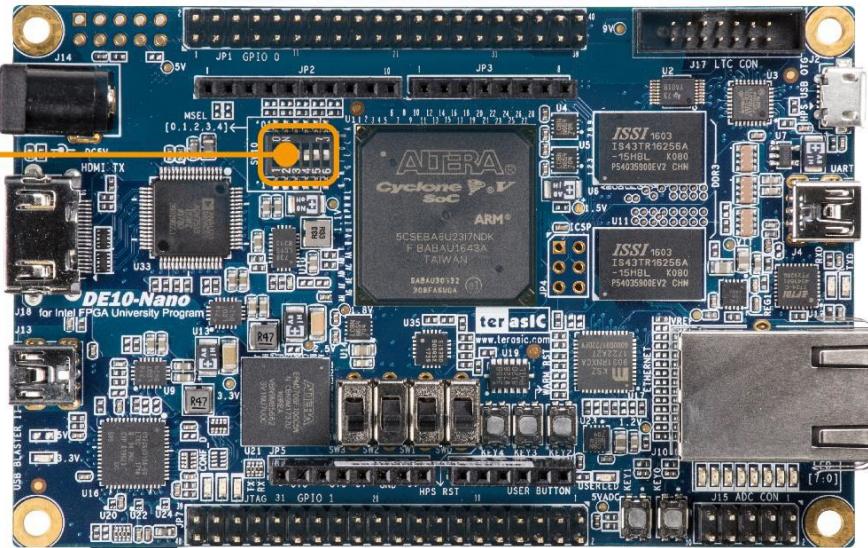
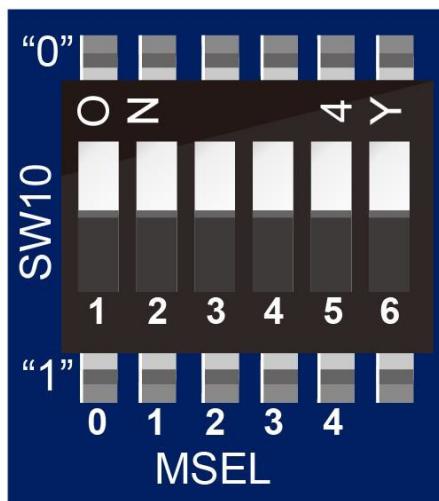
Available LEs: 110K (41910 ALMs)



DE10-Nano

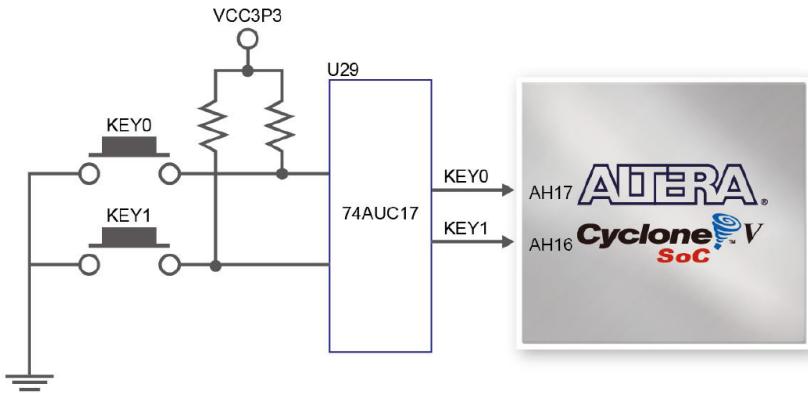
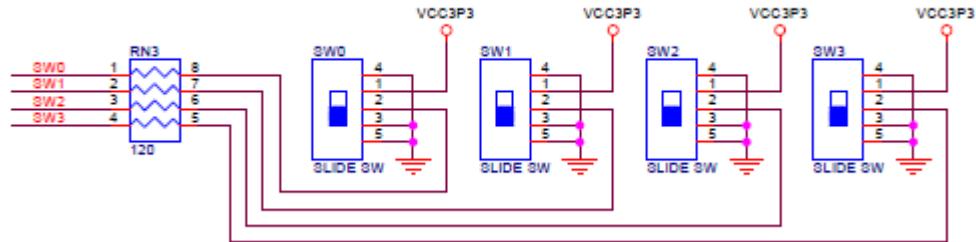
- When the DE10-Nano board is powered on, the FPGA can be configured from EPCS or HPS.
 - The MSEL[4:0] pins are used to select the configuration scheme.

FPPx16 / Compression Disabled / Fast POR	ON	ON	ON	ON	ON	N/A	FPGA configured from HPS software: U-Boot, with image stored on the SD card
---	----	----	----	----	----	-----	---

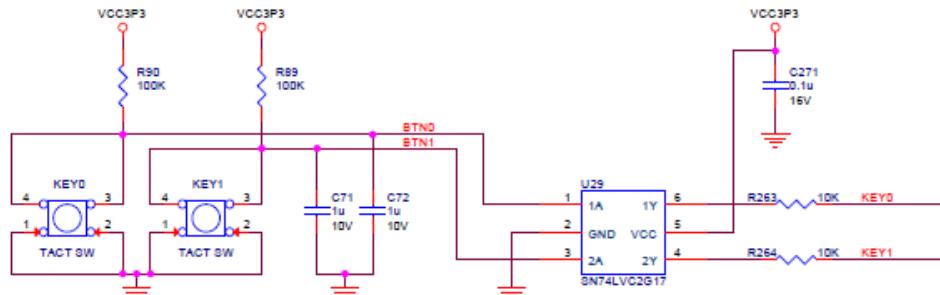


ALTERA®

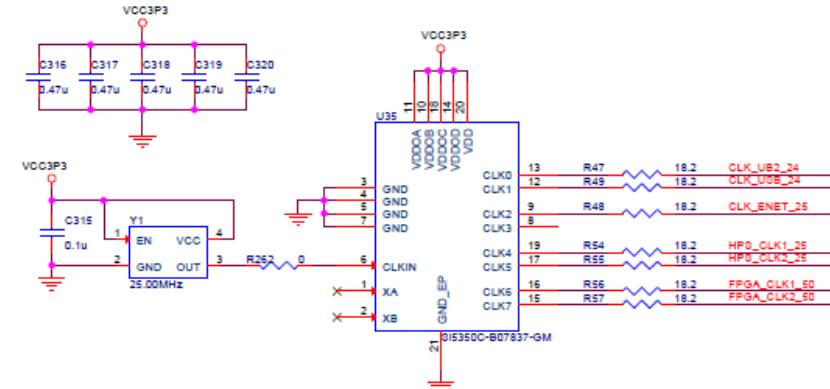
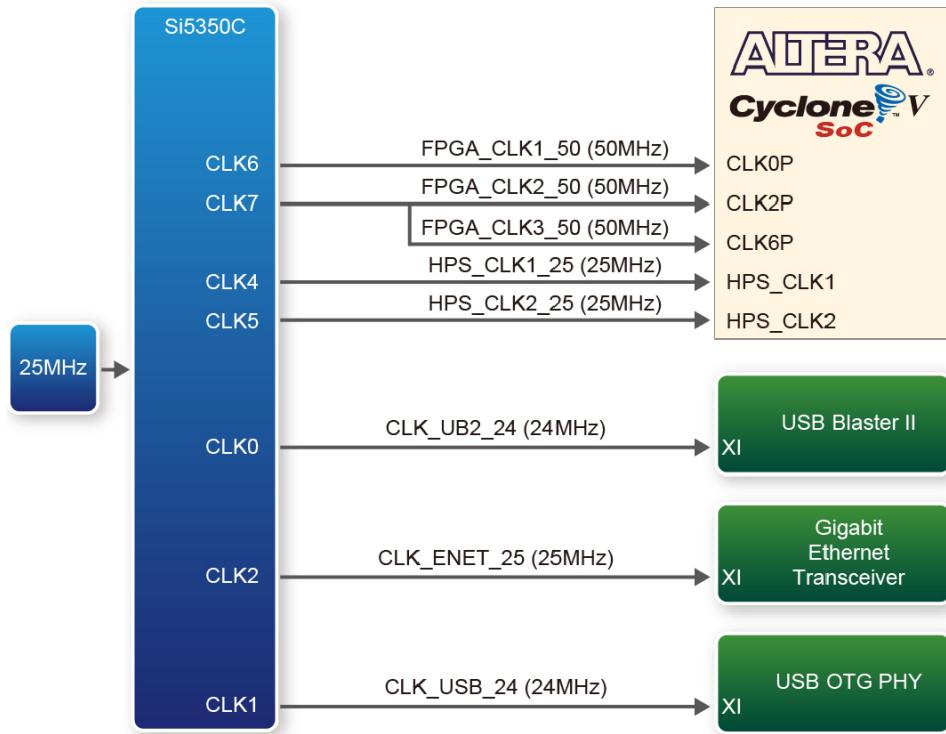
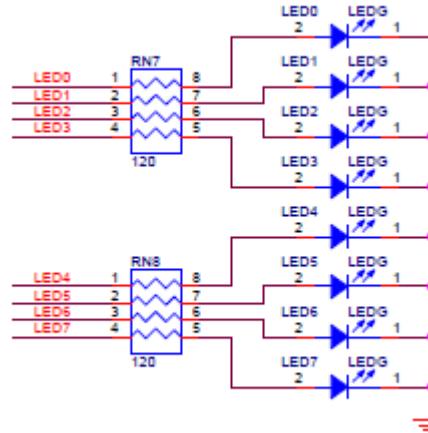
DE10-Nano – Switches and buttons



HEX SCHMITT-TRIGGER
BUFFER

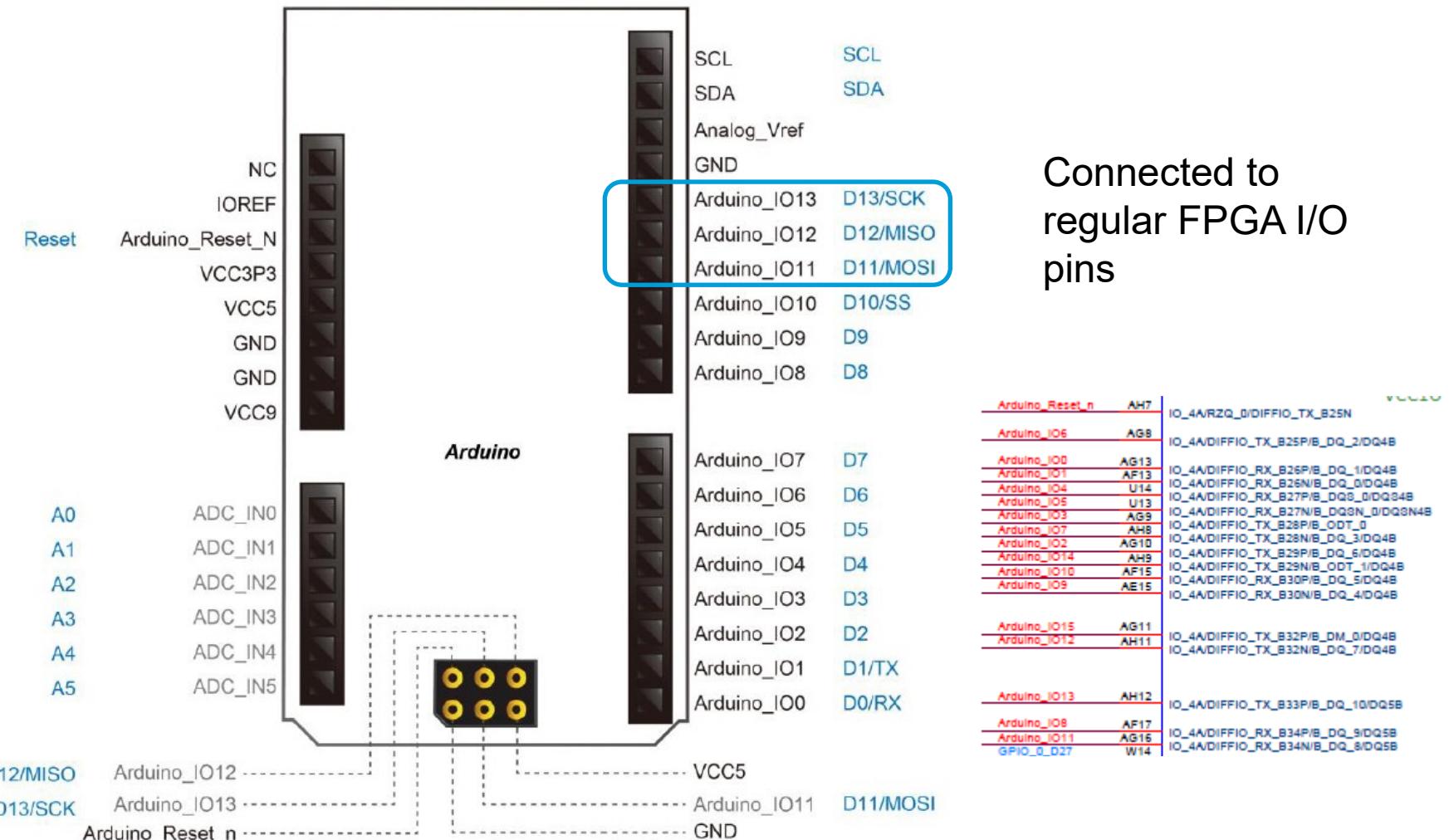


DE10-Nano – LEDs and clock tree



ALTERA

DE10-Nano – Arduino Uno Connector

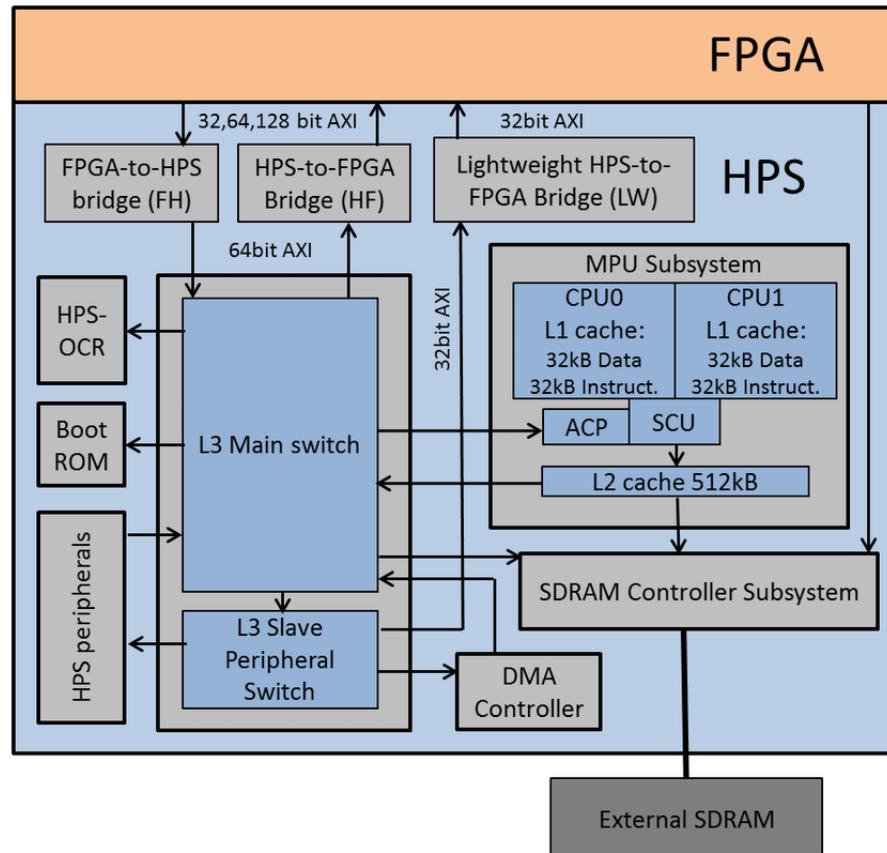


Altera Cyclone V - HPS

- Cyclone V FPGAs are manufactured on 300-mm wafers using Taiwan Semiconductor Manufacturing Company's (TSMC's) 28-nm (11 metal layers) low-power (LP) process technology, designed for low dynamic power and low leakage power

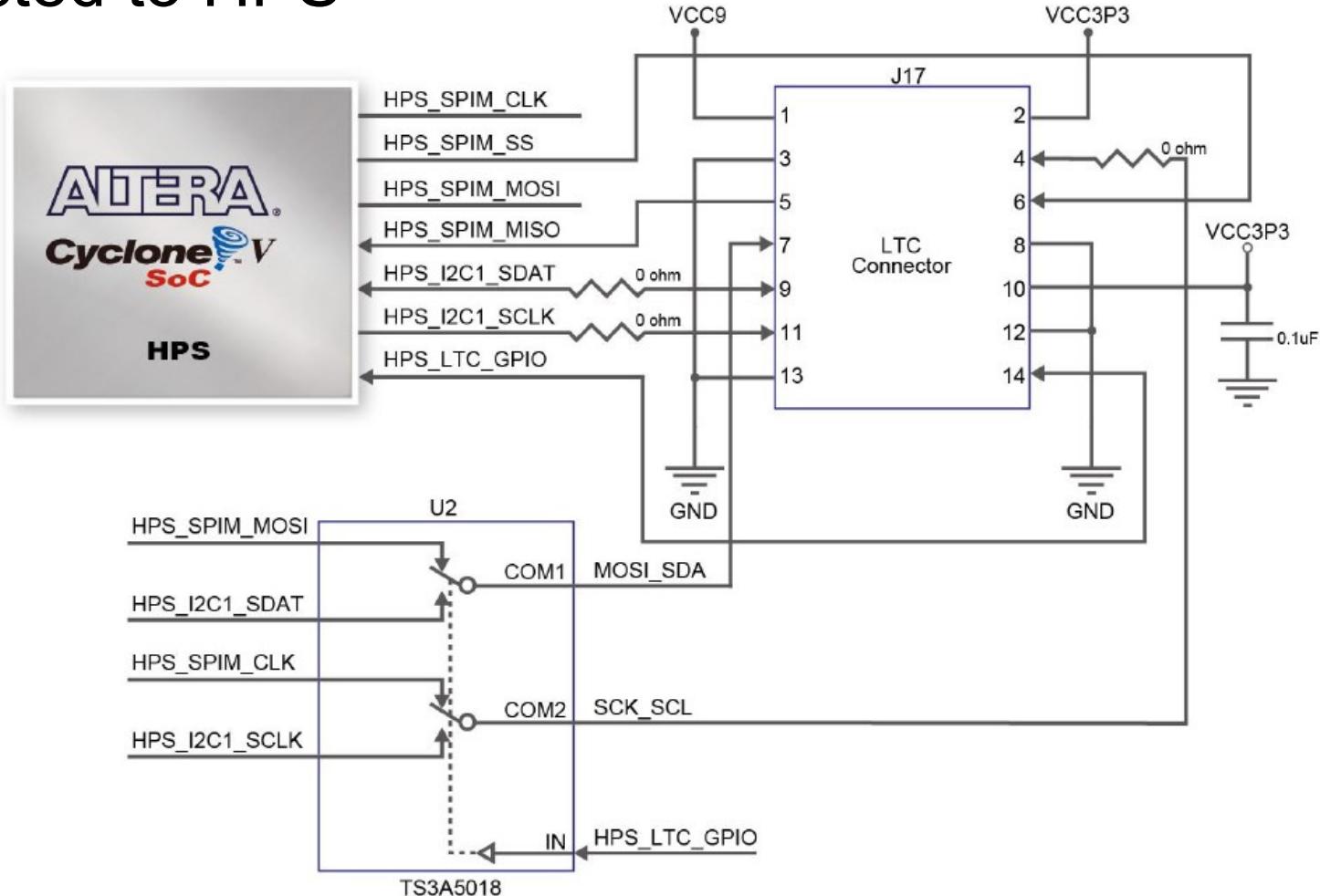
The HPS part contains a microprocessor unit (MPU) subsystem with:

- ✓ dual ARM Cortex-A9 MPCore processors,
- ✓ flash memory controllers,
- ✓ SDRAM L3 Interconnect,
- ✓ on-chip memories,
- ✓ support peripherals,
- ✓ interface peripherals,
- ✓ debug capabilities,
- ✓ PLLs.

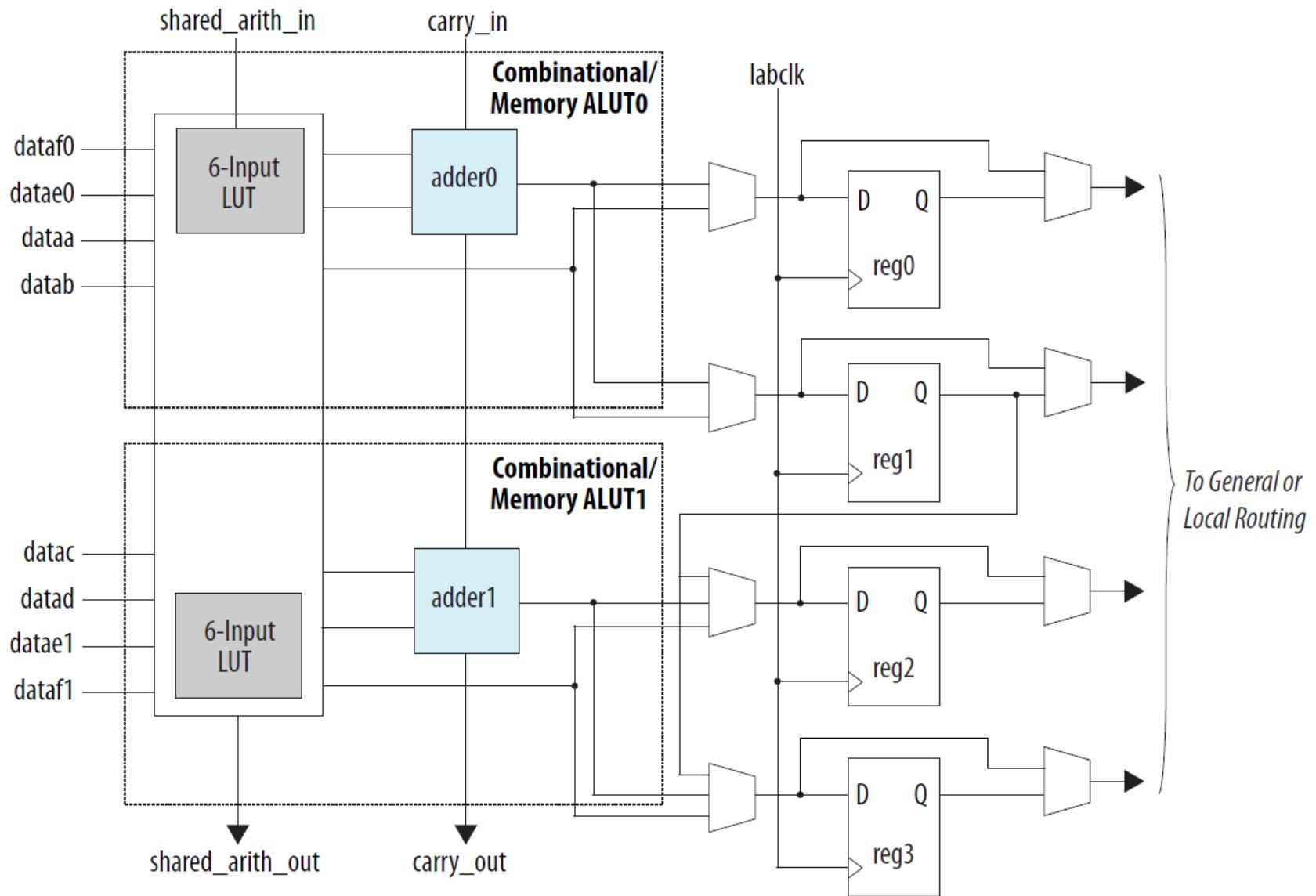


DE10-Nano – LTC Connector

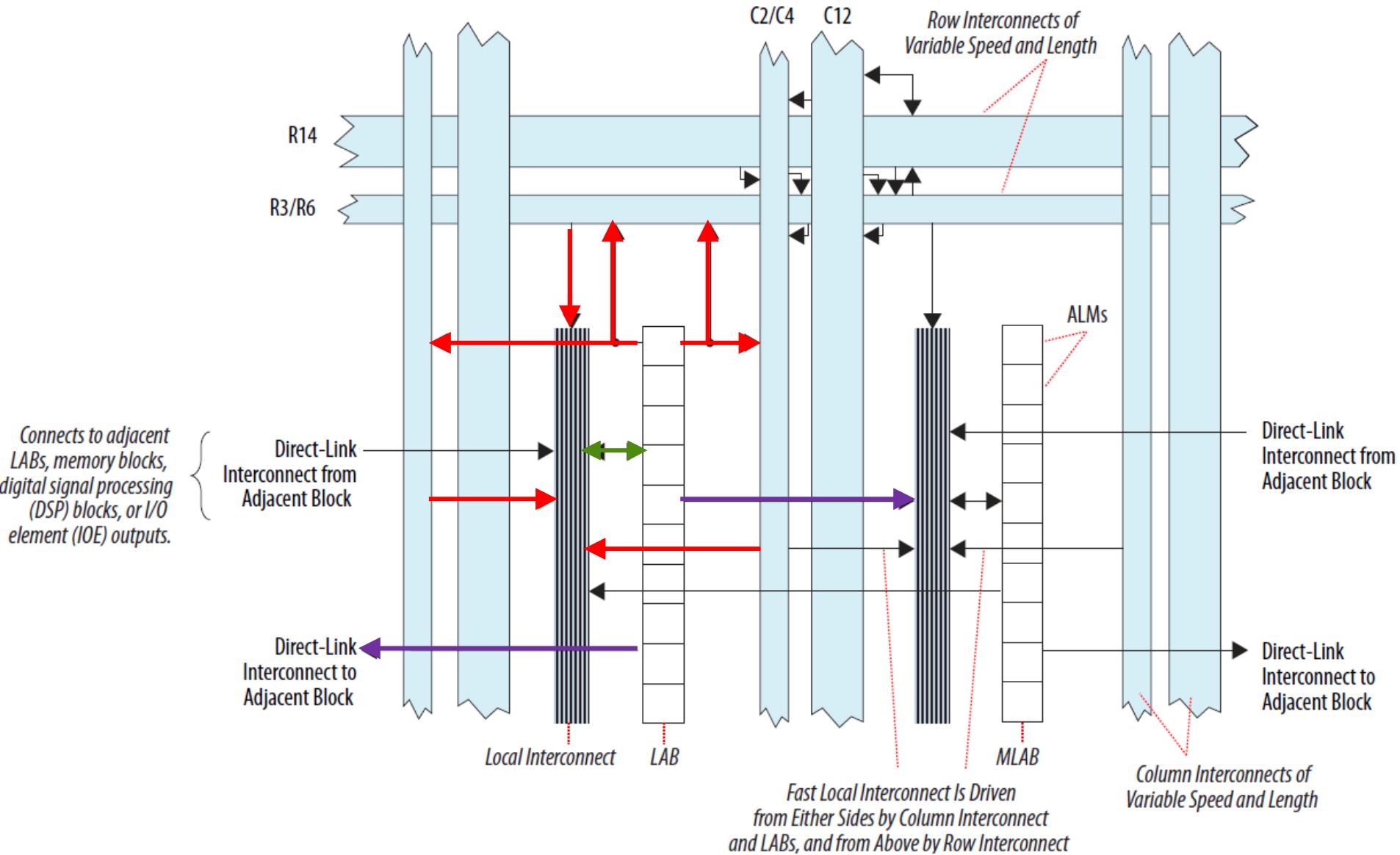
Connected to HPS



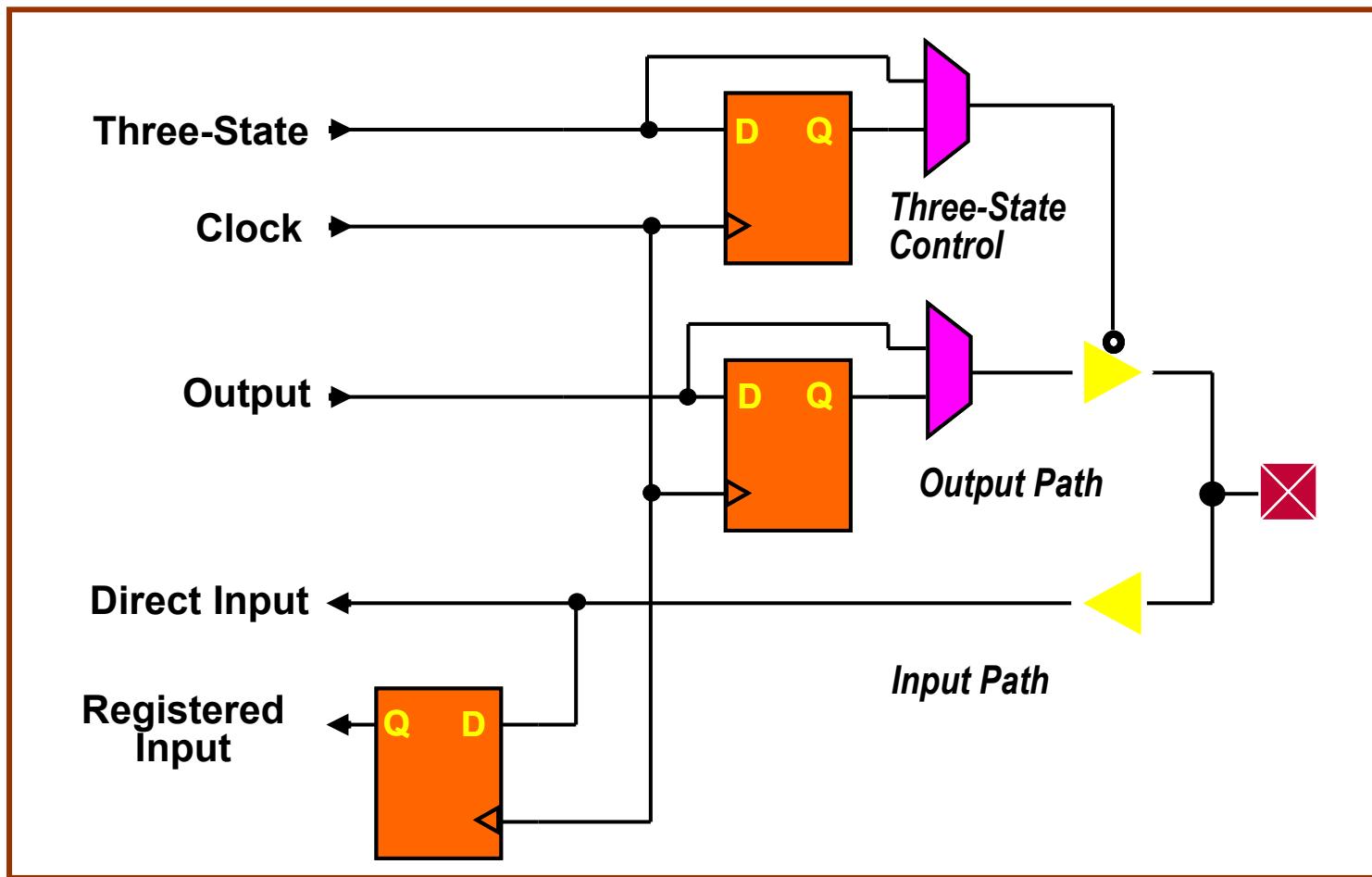
Altera Cyclone V – Adaptive Logic Module



Altera Cyclone V – Links

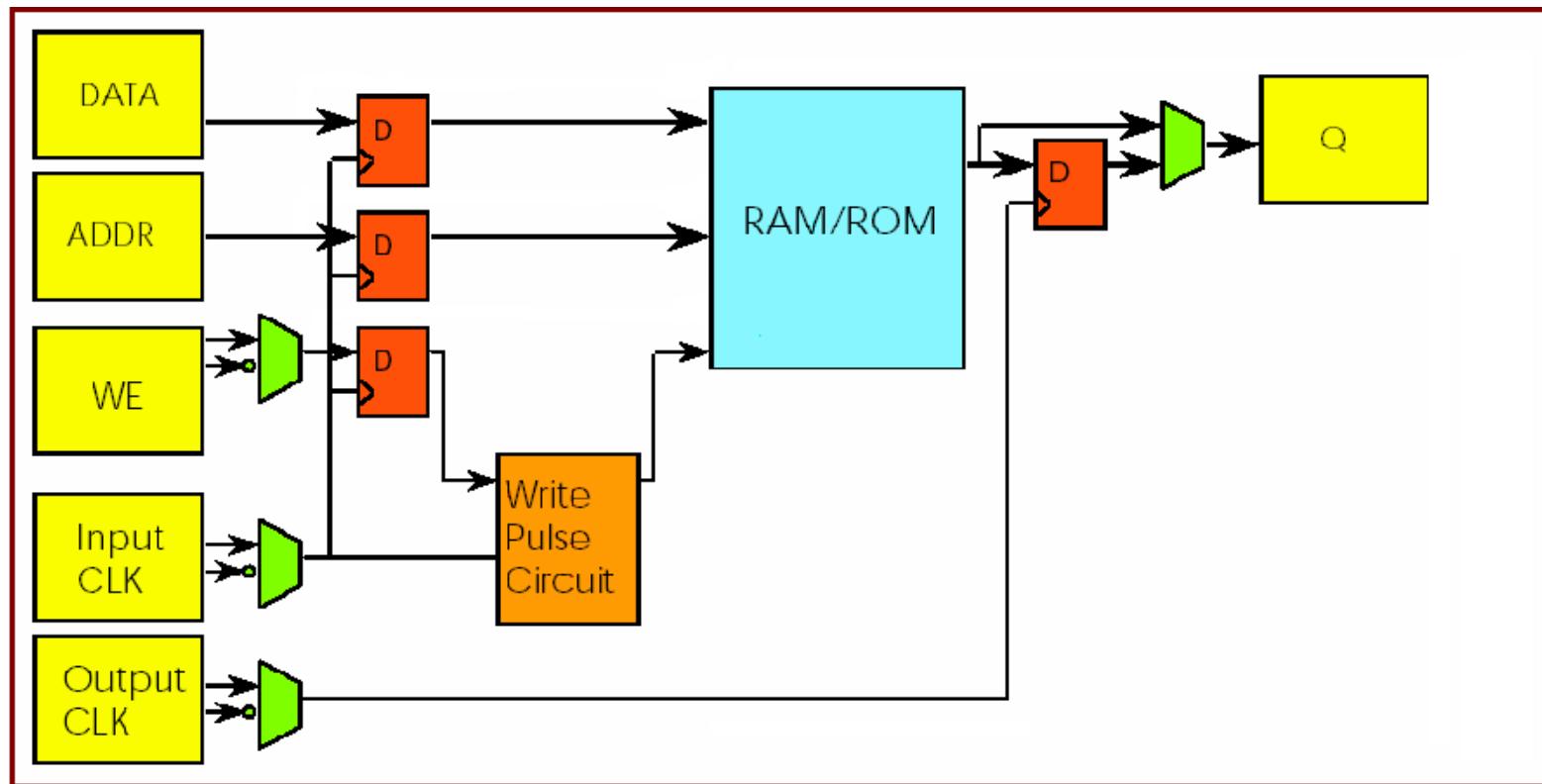


Altera Cyclone V – I/O



Altera Cyclone V – M10K blocks

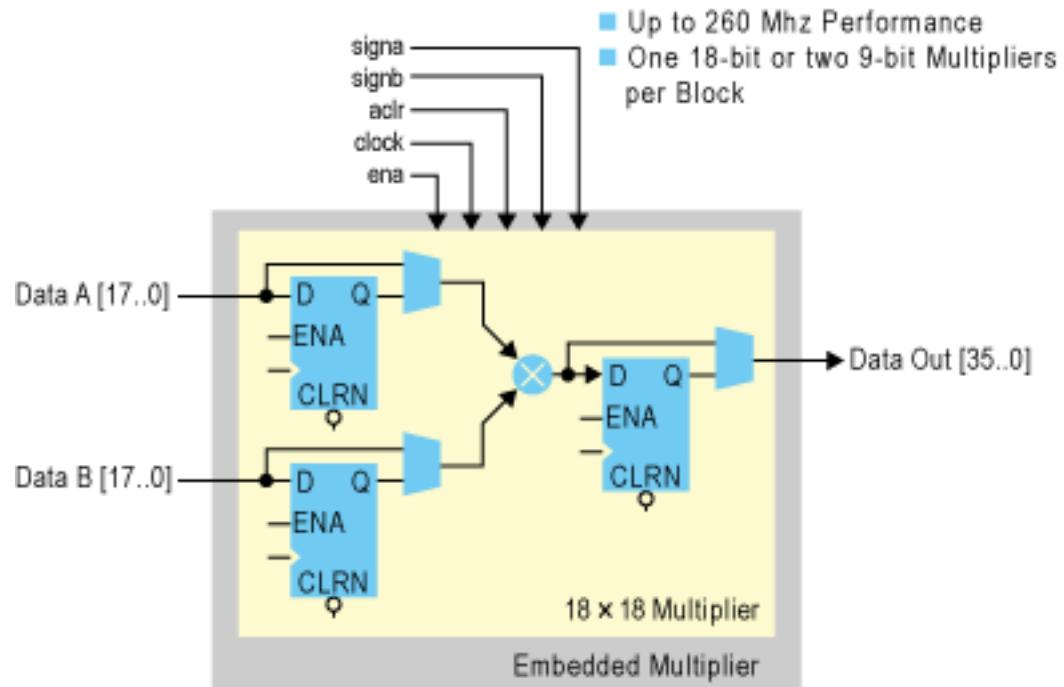
- M10K: 10240 bits (including those for parity)
- Single and dual ports arrangements
- Fully synchronous memory and variable word size



Altera Cyclone V – Embedded Multiplier

- Supports high- 27-bit (1x) or medium- 18-bit (2x) or low- precision (3x) modes

- can be cascaded to support wider bit widths
- supports both signed and unsigned multiplication
- offers optional input and output registers for increased performance
- supports accumulation



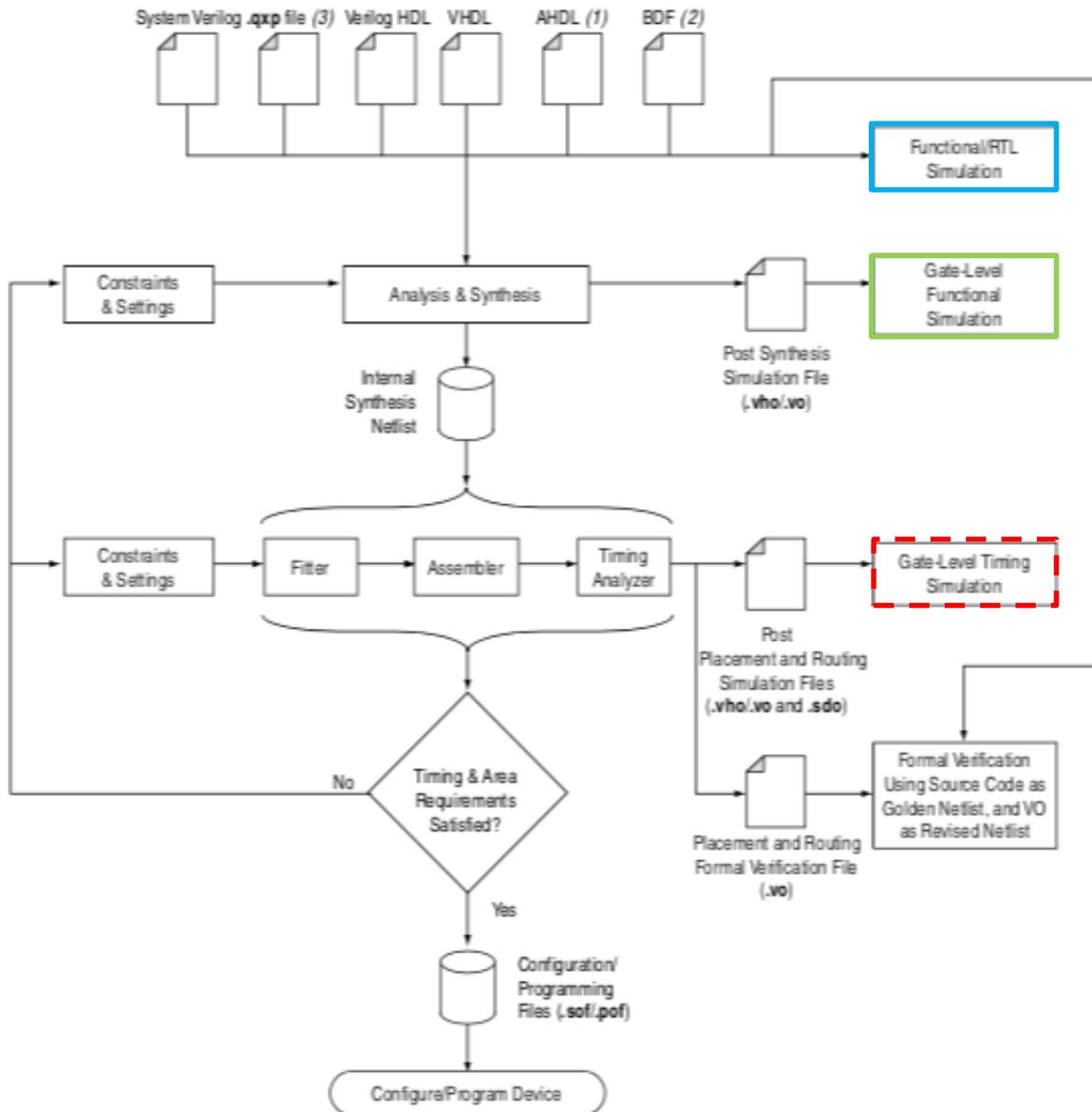
QUARTUS II

ALTERA®

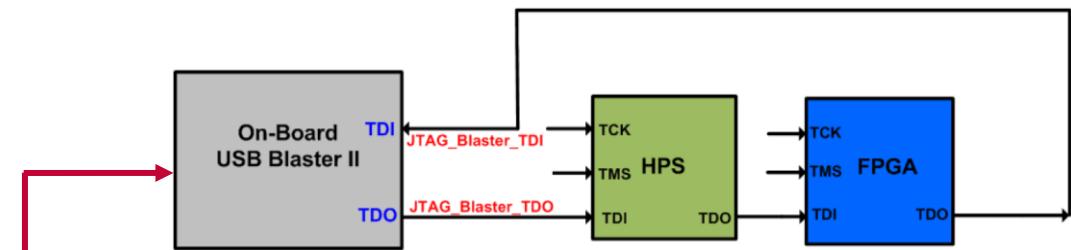
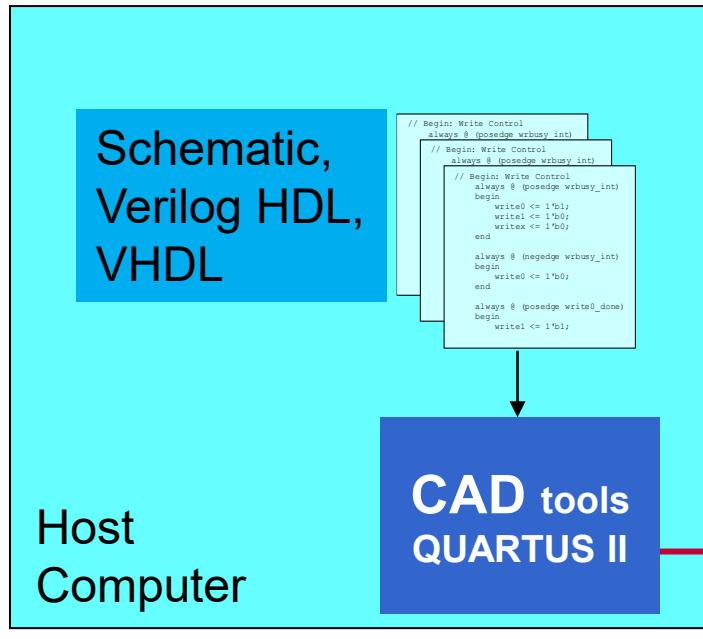
Quartus II Design Flow

■ VHO and SDO

- for gate-level simulation, a synthesized design netlist in the form of a VHDL Output File (.vho) is generated
- the .sdo file contains the delay information of each architecture primitive and routing element of the design: NOT AVAILABLE for Cyclone V

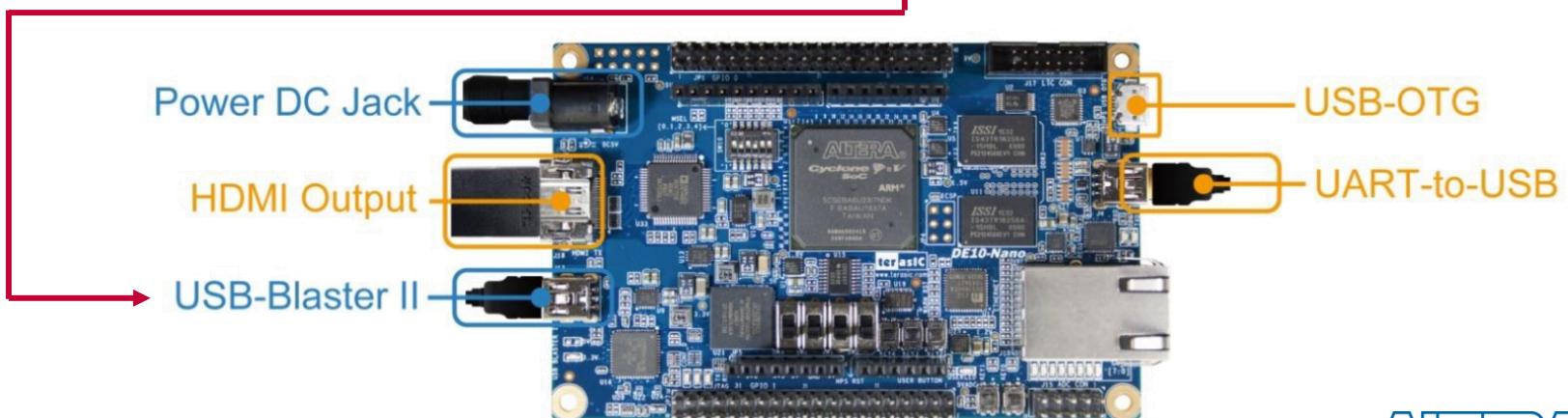


Altera Quartus II CAD Tools



JTAG consists of four logic signals: TDI, TCK, TMS (input) and TDO (output)

TMS controls the JTAG controller (16 states FSM)



ALTERA

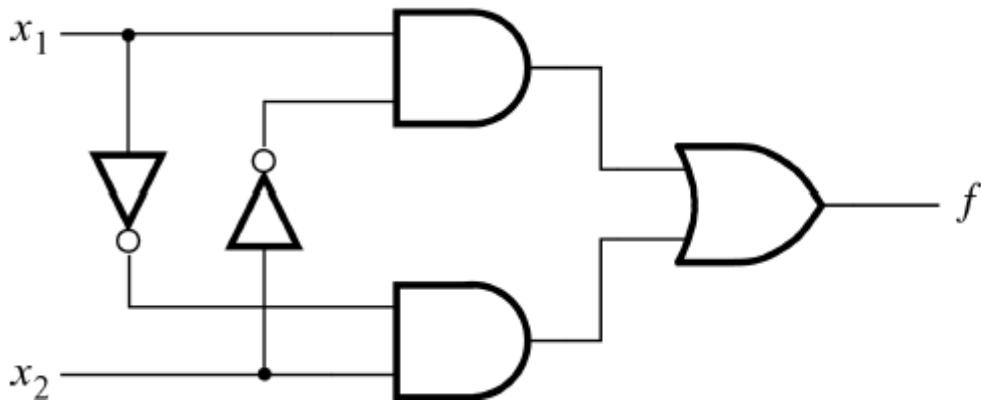
Developing Digital Logic with Altera Technology

Creating a Quartus II project

Outline

- Creating projects in Quartus II
- Targeting a project for a DE10 Board
- Downloading a circuit onto a DE10 board
- Compiling and debugging

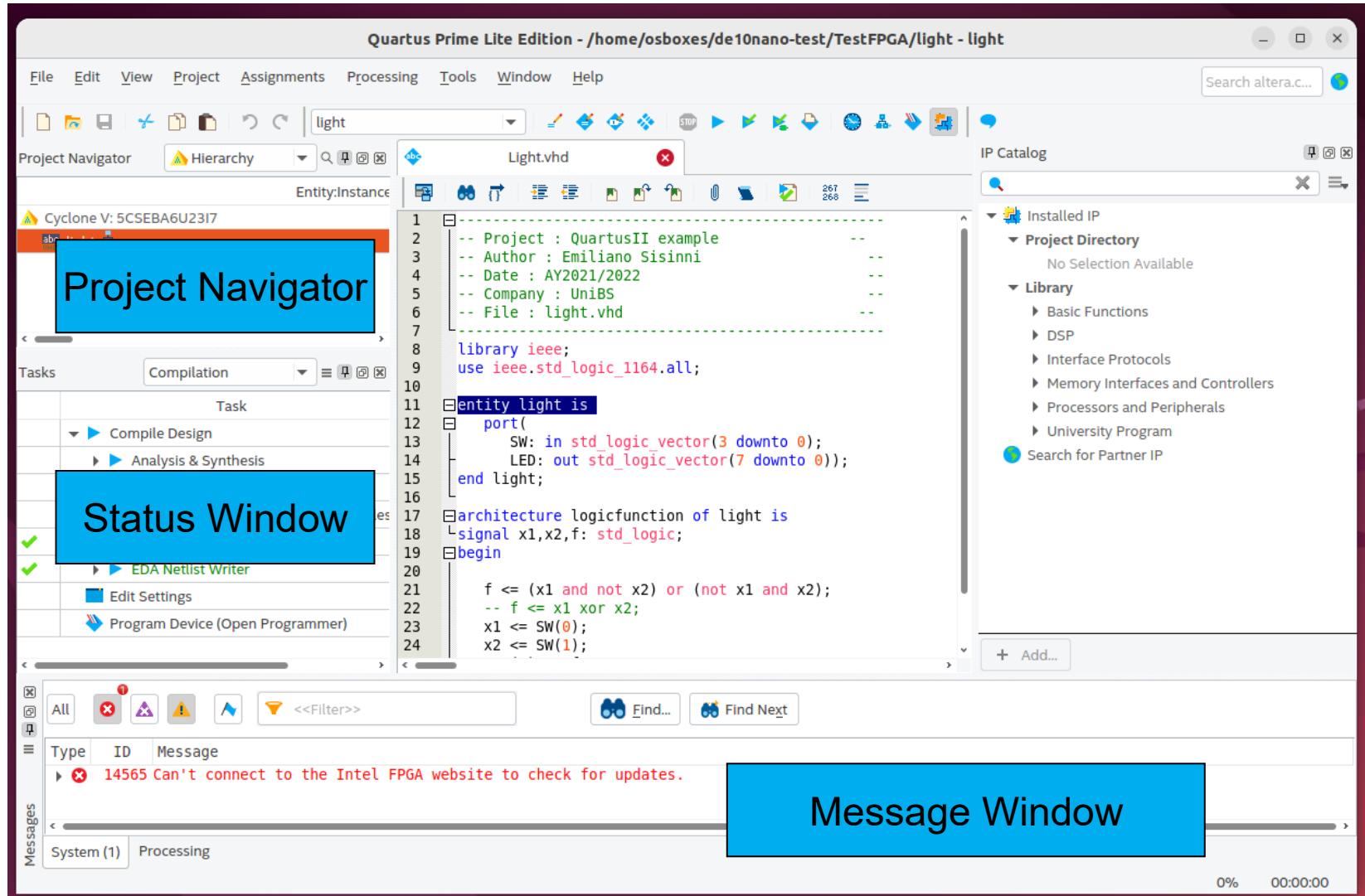
Simple Project (XOR)



x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

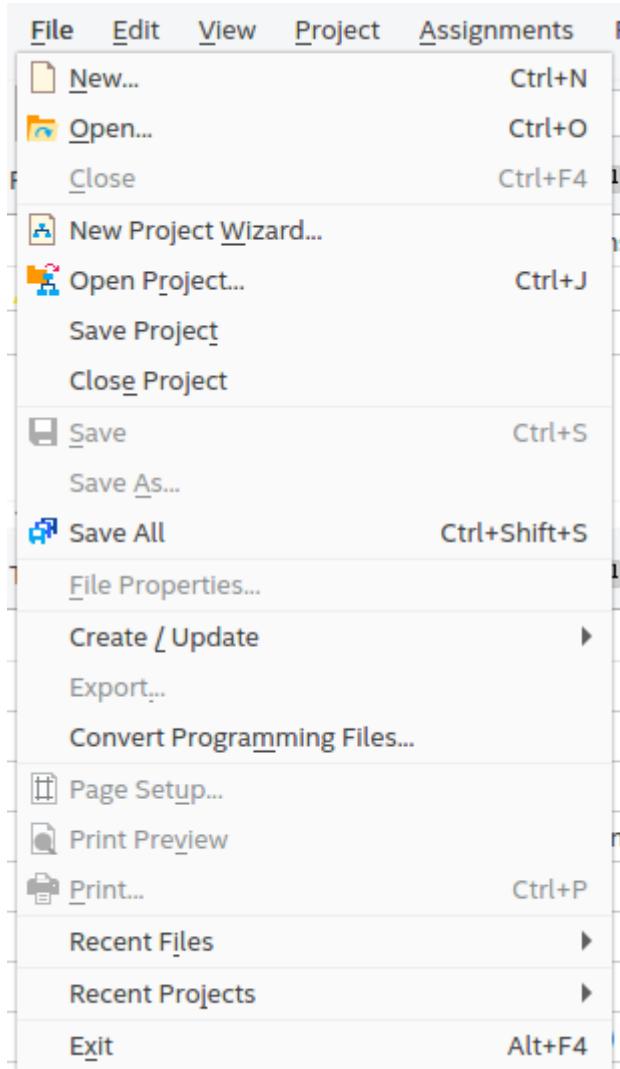
```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY light IS
    PORT ( x1, x2 : IN      STD_LOGIC ;
            f      : OUT      STD_LOGIC ) ;
END light ;
ARCHITECTURE LogicFunction OF light IS
BEGIN
    f <= (x1 AND NOT x2) OR (NOT x1 AND x2);
END LogicFunction ;
```

Step 1: Start Quartus II



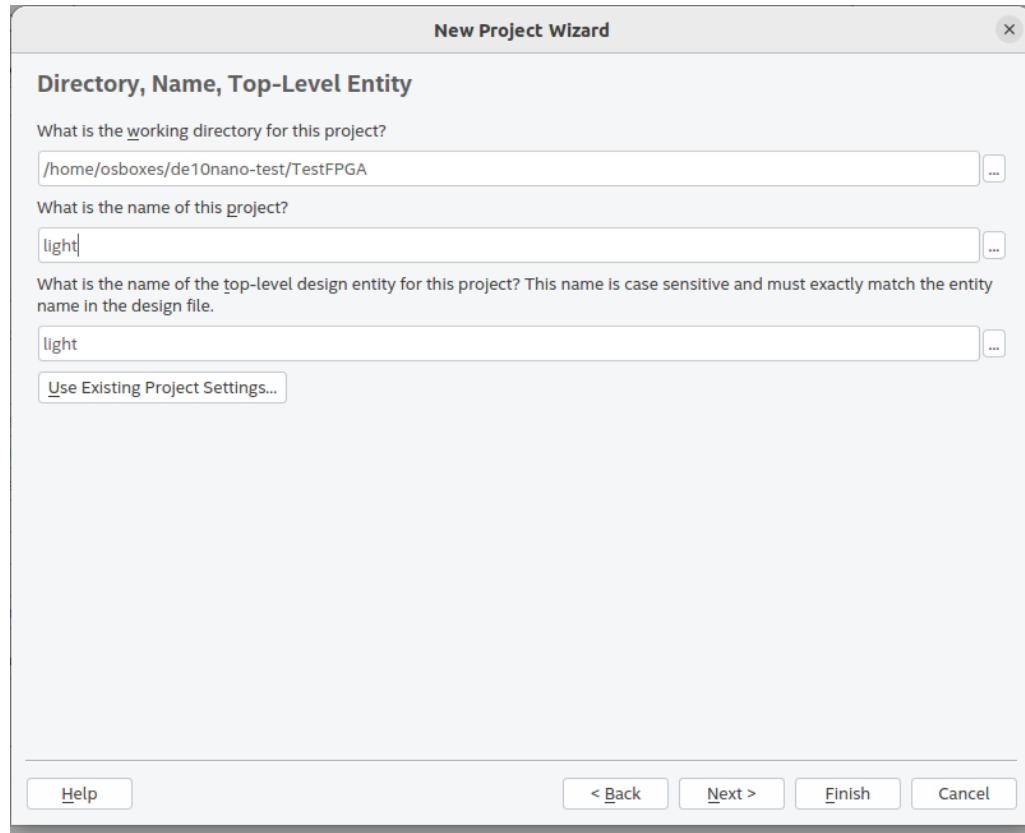
ALTERA®

Step 2: Create a New Project



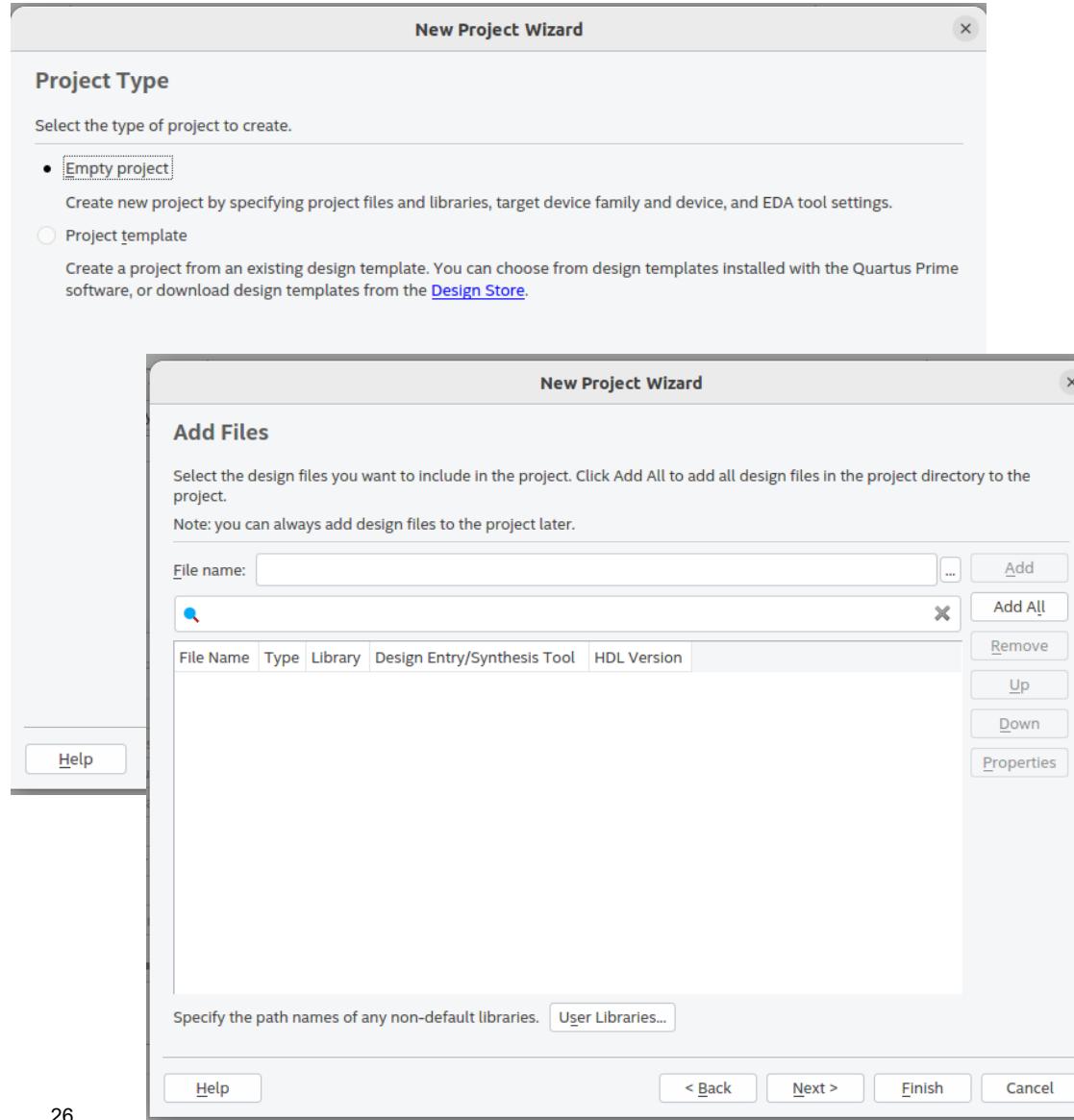
- Click **File** Menu
- Select **New Project Wizard**
- This will open a new window where project information can be specified

Project Name and Directory



The project must have a name, which is usually the same as the top-level design entity that will be included in the project.

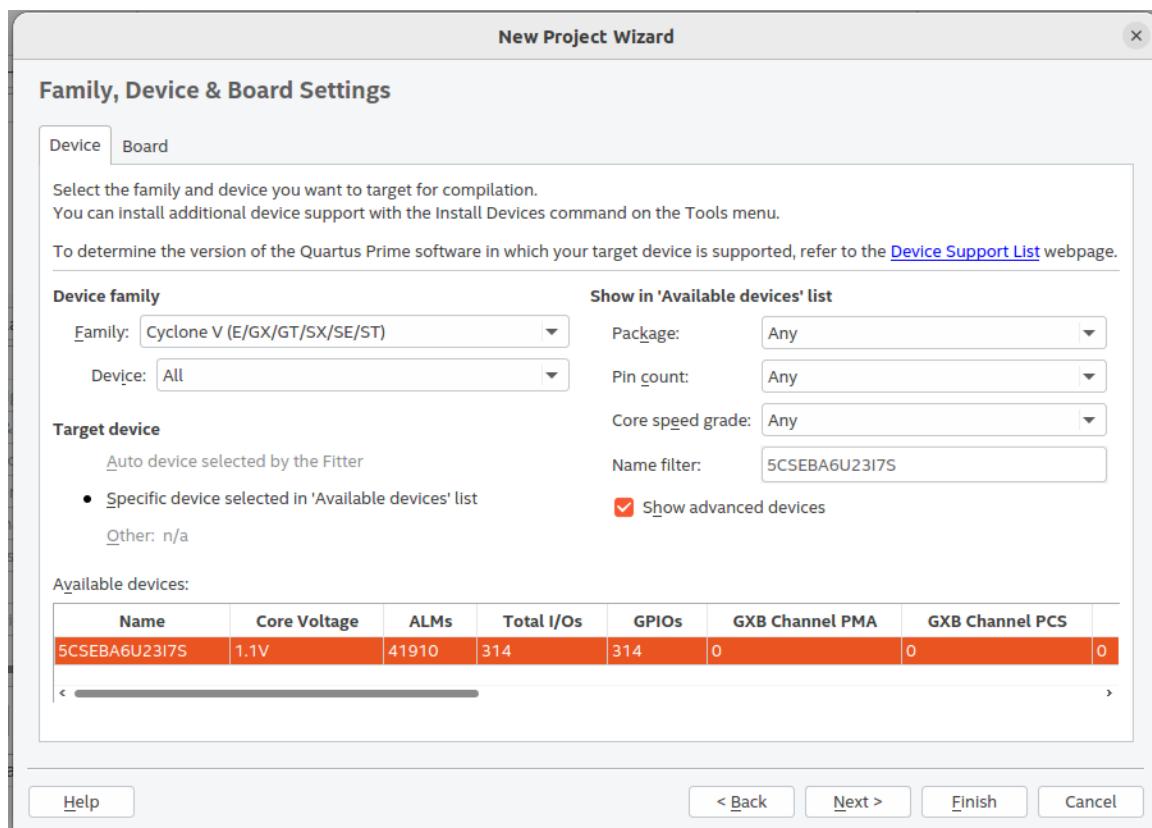
Add Source Files to Project



The wizard makes it easy to specify which existing files (if any) should be included in the project. Assuming that we do not have any existing files, click Next

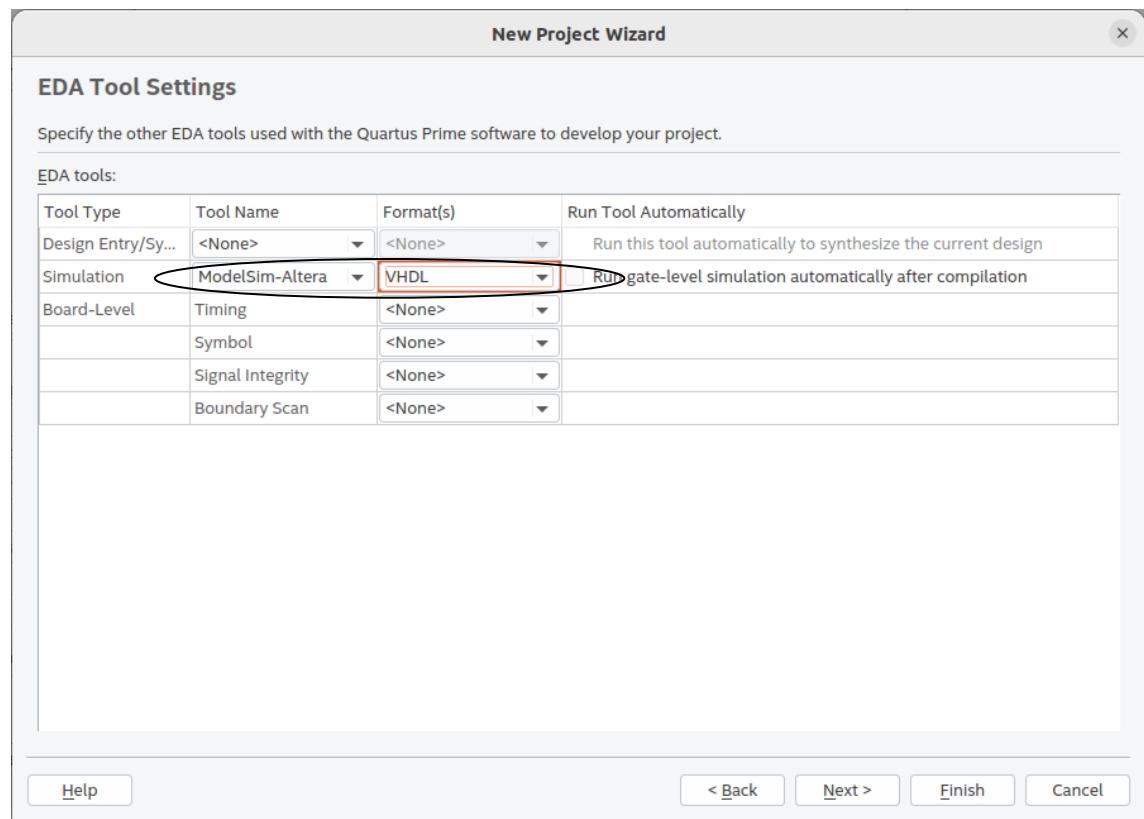
Specify FPGA Device

- Select the FPGA device on the board
 - Cyclone V Family
 - For DE10 Nano – 5CSEBA6U23I7S

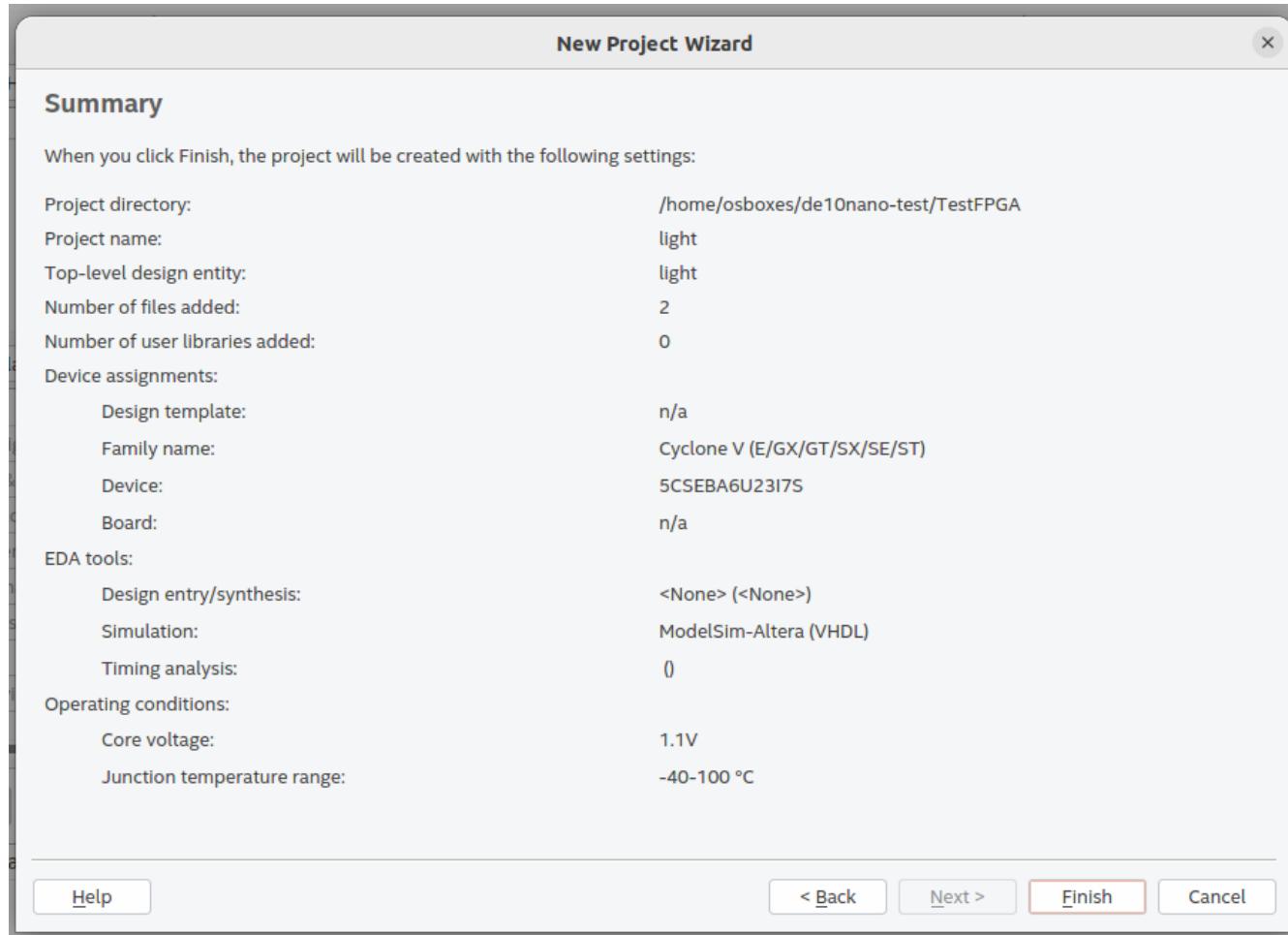


Additional EDA Tools

- Specify Tools, in addition to Quartus II, that you will use
- These are unnecessary for small student designs
 - Leave all entries as <None> (choose Simulation: ModelSim-Altera)
 - Press Next



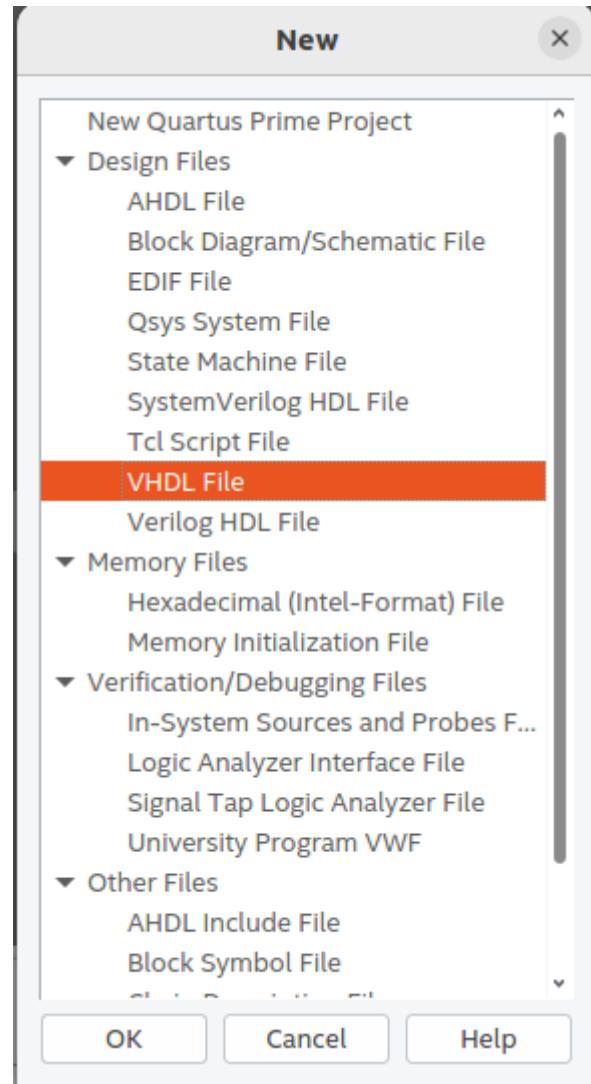
New Project Summary



- A summary of the chosen settings appears in the screen shown in Figure.
- Press **Finish**, which returns to the main Quartus II window, but with *light* specified as the new project, in the display title bar

Step 3a: Create Source File

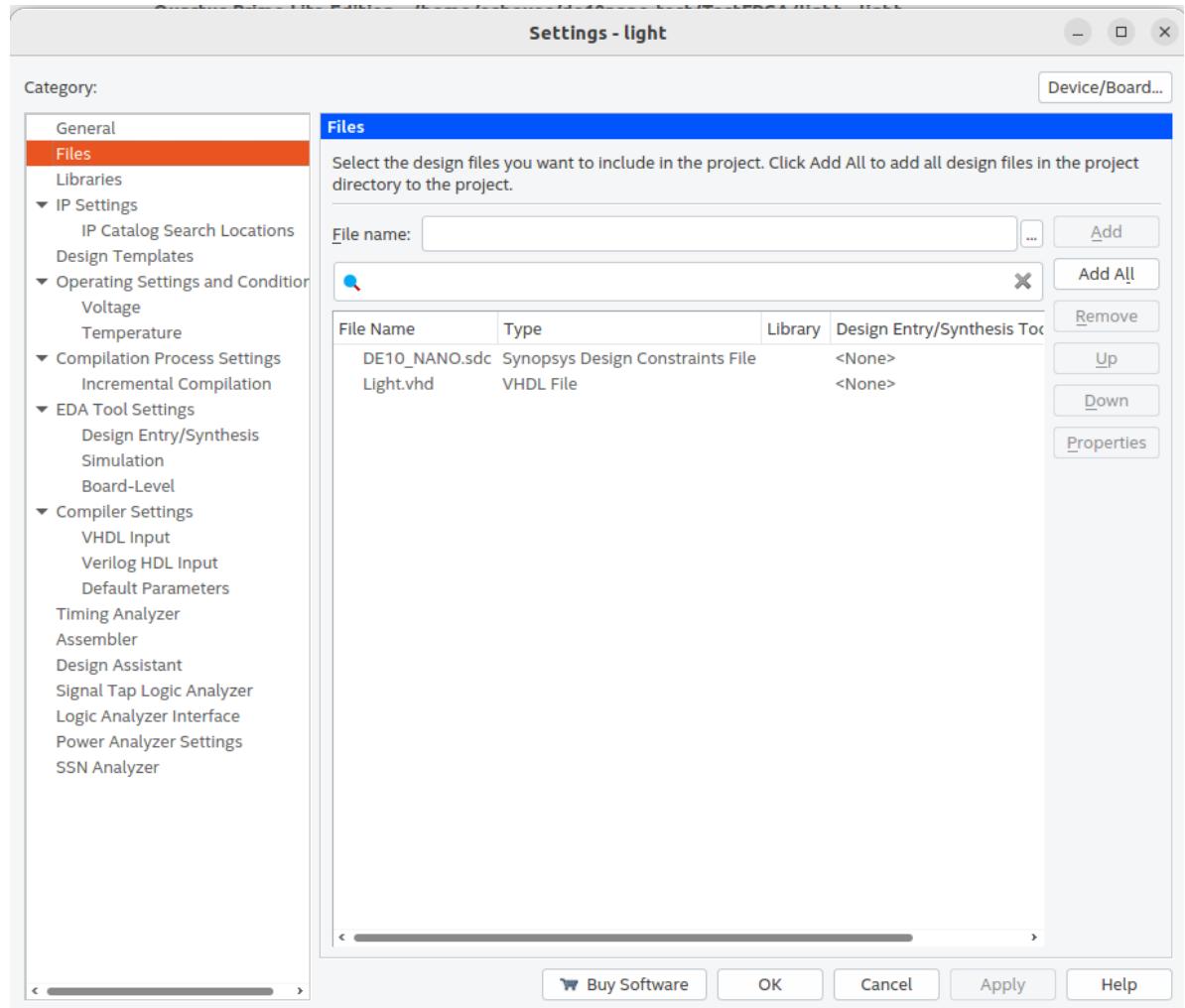
- Select File > New to get the window in Figure, choose VHDL File, and click OK. This opens the Text Editor window.
- Specify a name for the file that will be created and select File > Save to open a pop-up box and in the box labeled Save as type choose VHDL File



Step 3b: Add Source File

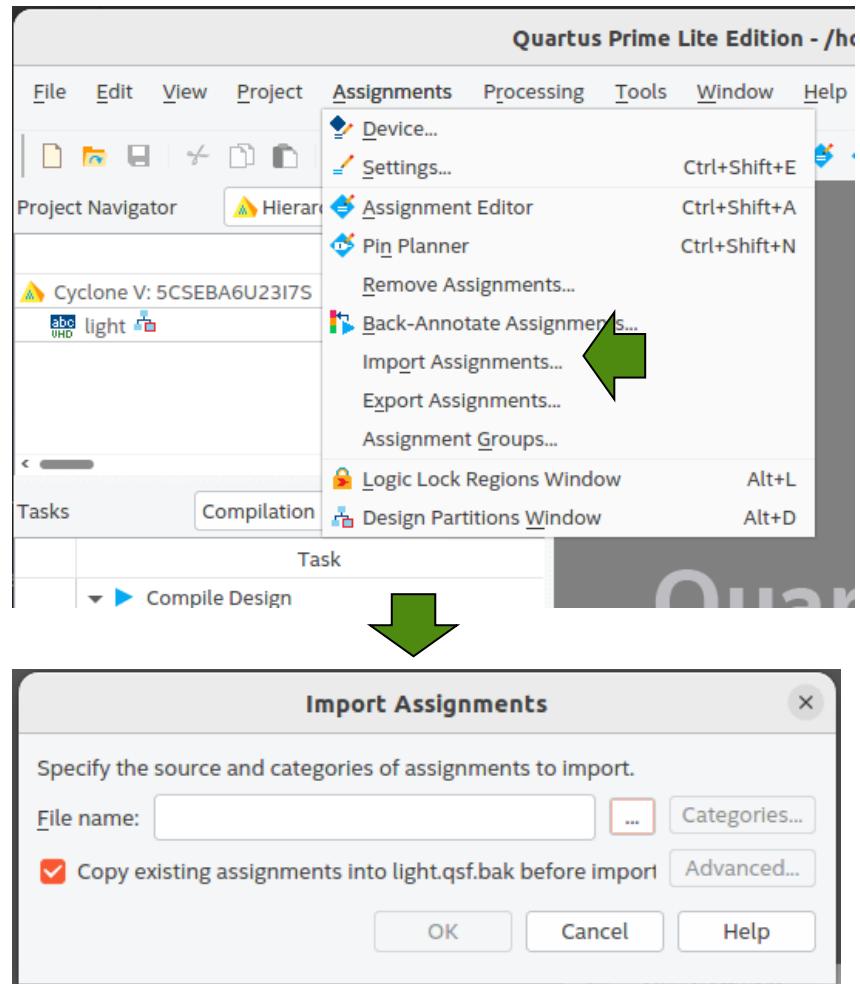
Select:

- Assignments > Settings and looks for File item, or
- Project > Add/Remove Files in Project



Step 4: Assign Pins to connect switches/lights to inputs and outputs of your circuit

- Click **Assignments**, then **Import Assignments...**
- Import file
 - DE10_NANO.qsf
- Imports locations for predefined port names, such as SW, LED, KEY, and others
 - Can be done manually for custom port names



Step 4: Assign Pins to connect switches/lights to inputs and outputs of your circuit

```
# Pin & Location Assignments
# =====
set_location_assignment PIN_AH17 -to KEY[0]
set_location_assignment PIN_AH16 -to KEY[1]

# =====
set_location_assignment PIN_W15 -to LED[0]
set_location_assignment PIN_AA24 -to LED[1]
set_location_assignment PIN_V16 -to LED[2]
set_location_assignment PIN_V15 -to LED[3]
set_location_assignment PIN_AF26 -to LED[4]
set_location_assignment PIN_AE26 -to LED[5]
set_location_assignment PIN_Y16 -to LED[6]
set_location_assignment PIN_AA23 -to LED[7]

# =====
set_location_assignment PIN_Y24 -to SW[0]
set_location_assignment PIN_W24 -to SW[1]
set_location_assignment PIN_W21 -to SW[2]
set_location_assignment PIN_W20 -to SW[3]

# =====
set_location_assignment PIN_V11 -to FPGA_CLK1_50
set_location_assignment PIN_Y13 -to FPGA_CLK2_50
set_location_assignment PIN_E11 -to FPGA_CLK3_50
```

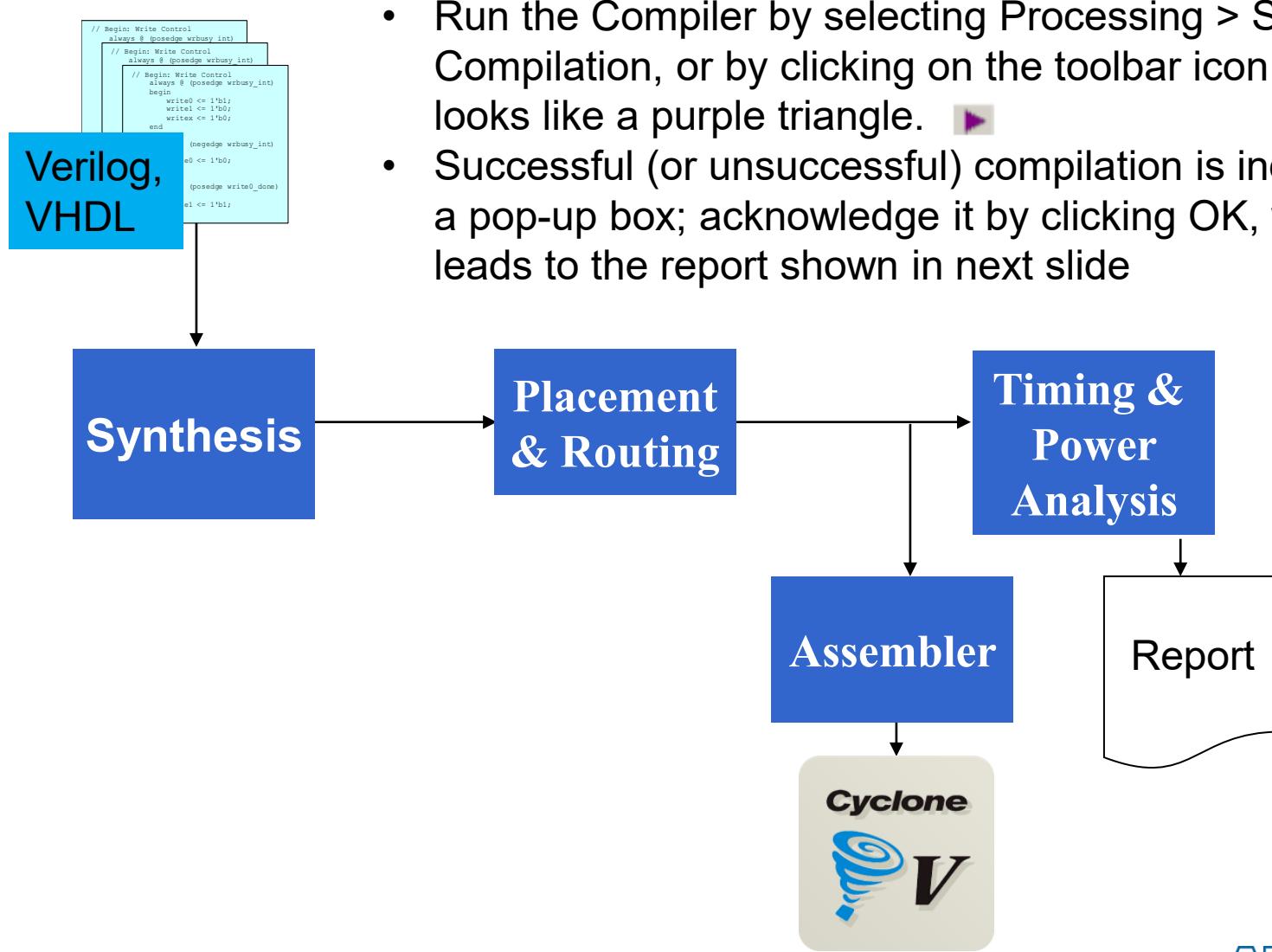
```
# Pin & Location Assignments
# =====
set_location_assignment PIN_AG13 -to ARDUINO_IO[0]
set_location_assignment PIN_AF13 -to ARDUINO_IO[1]
set_location_assignment PIN_AG10 -to ARDUINO_IO[2]
set_location_assignment PIN_AG9 -to ARDUINO_IO[3]
set_location_assignment PIN_U14 -to ARDUINO_IO[4]
set_location_assignment PIN_U13 -to ARDUINO_IO[5]
set_location_assignment PIN_AG8 -to ARDUINO_IO[6]
set_location_assignment PIN_AH8 -to ARDUINO_IO[7]
set_location_assignment PIN_AF17 -to ARDUINO_IO[8]
set_location_assignment PIN_AE15 -to ARDUINO_IO[9]
set_location_assignment PIN_AF15 -to ARDUINO_IO[10]
set_location_assignment PIN_AG16 -to ARDUINO_IO[11]
set_location_assignment PIN_AH11 -to ARDUINO_IO[12]
set_location_assignment PIN_AH12 -to ARDUINO_IO[13]
set_location_assignment PIN_AH9 -to ARDUINO_IO[14]
set_location_assignment PIN_AG11 -to ARDUINO_IO[15]
```

SW: IN STD_LOGIC_VECTOR(N DOWNTO 0);
LED: OUT STD_LOGIC_VECTOR(N DOWNTO 0);
KEY: IN STD_LOGIC_VECTOR(0 TO N)

x1, x2, f ??????



Step 5: Compile Design



Step 6: Examine Compilation Report

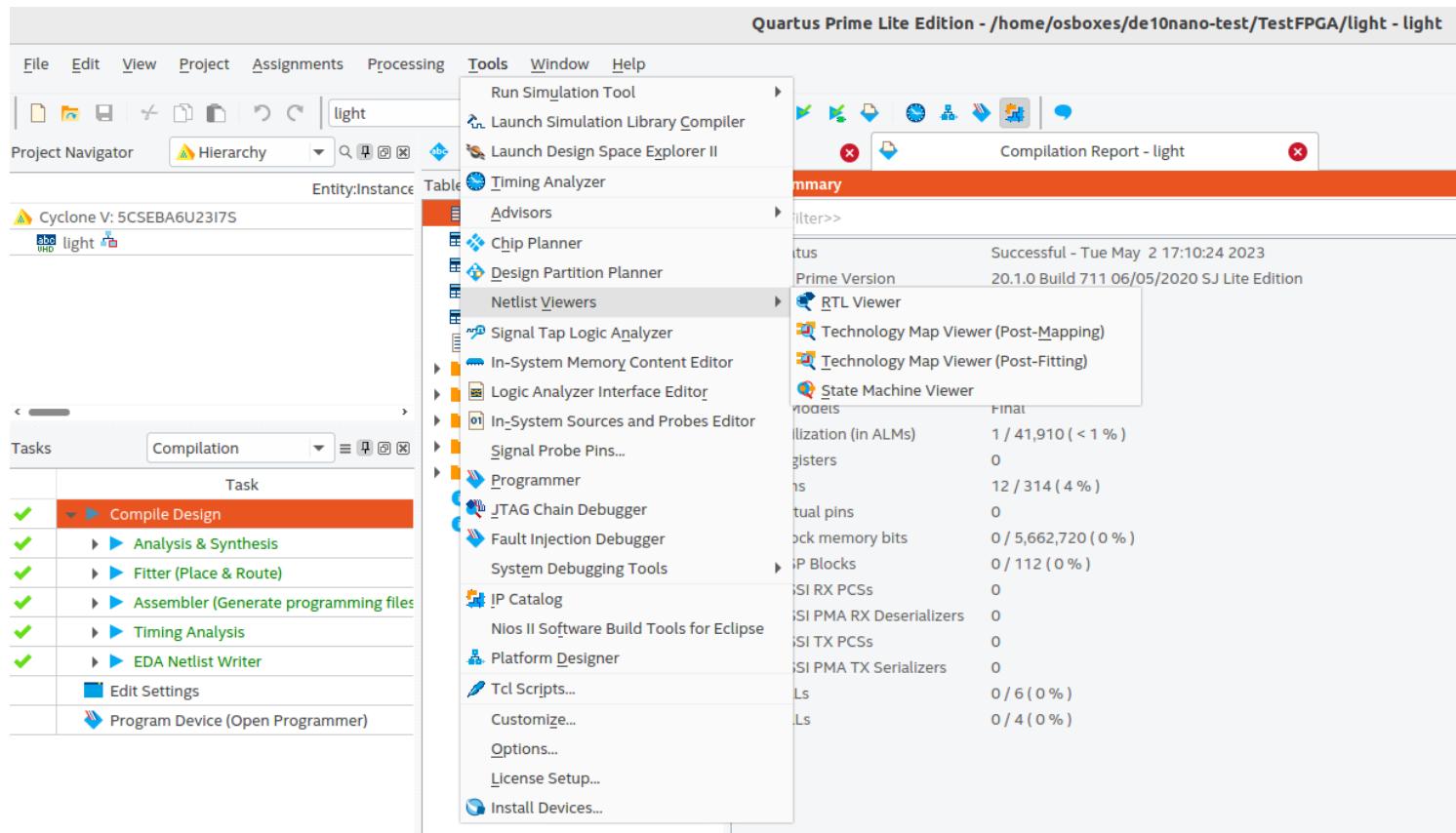
Table of Contents		Flow Summary
		<<Filter>>
Flow Summary		
Flow Settings		Flow Status Successful - Tue May 2 17:10:24 2023
Flow Non-Default Global Settings		Quartus Prime Version 20.1.0 Build 711 06/05/2020 SJ Lite Edition
Flow Elapsed Time		Revision Name light
Flow OS Summary		Top-level Entity Name light
Flow Log		Family Cyclone V
Analysis & Synthesis		Device 5CSEBA6U23I7S
Fitter		Timing Models Final
Assembler		Logic utilization (in ALMs) 1 / 41,910 (< 1 %)
Timing Analyzer		Total registers 0
EDA Netlist Writer		Total pins 12 / 314 (4 %)
Flow Messages		Total virtual pins 0
Flow Suppressed Messages		Total block memory bits 0 / 5,662,720 (0 %)
		Total DSP Blocks 0 / 112 (0 %)
		Total HSSI RX PCSs 0
		Total HSSI PMA RX Deserializers 0
		Total HSSI TX PCSs 0
		Total HSSI PMA TX Serializers 0
		Total PLLs 0 / 6 (0 %)
		Total DLLs 0 / 4 (0 %)



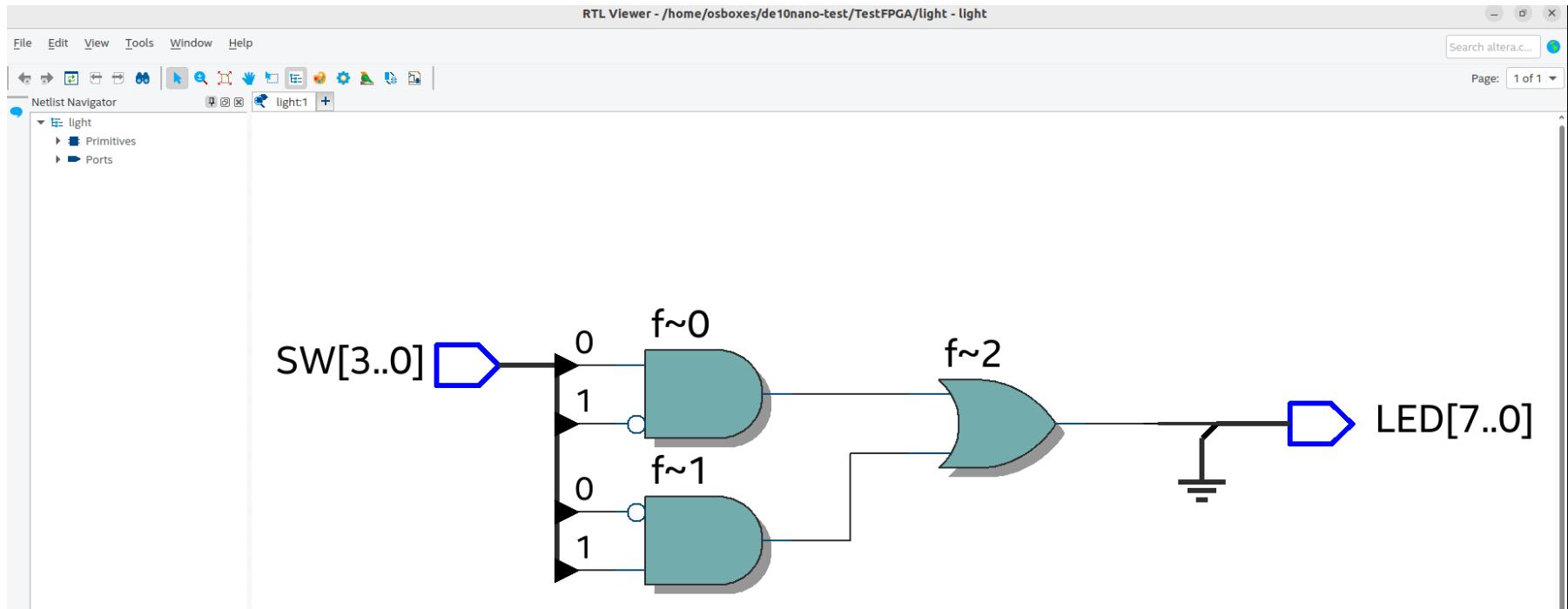
Step 6: See the Circuit in RTL Viewer

■ Start the RTL Viewer

- Click Tools
- Expand the Netlist Viewers list
- Click RTL Viewer



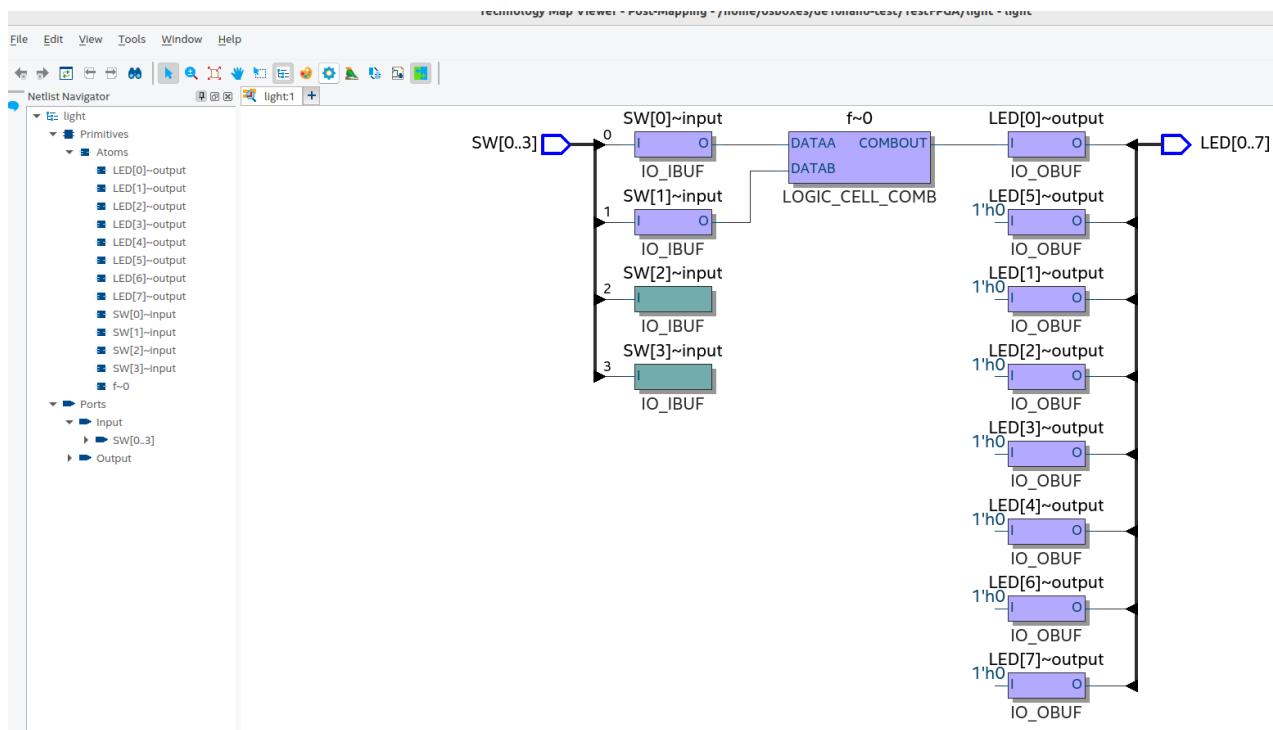
Step 6: Examine the Circuit – RTL Viewer



ALTERA®

Step 6: Examine the Circuit, Technology Map Viewer

- Start the Technology Map Viewer
 - Click Tools
 - Expand the Netlist Viewers list
 - Click Technology Map Viewer (Post Mapping –i.e. after synthesis-, or Post Fitting)
 - View of the internal structure

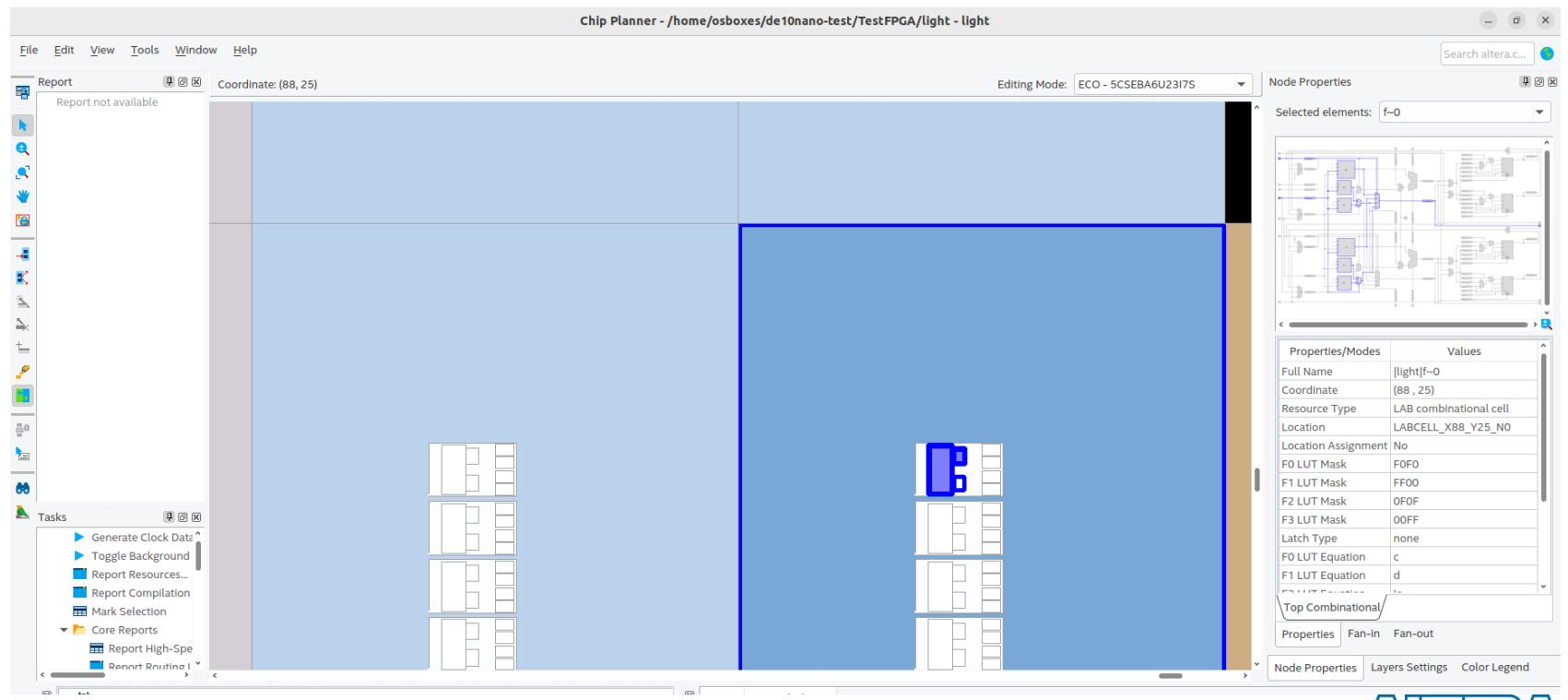


ALTERA®

Step 6: Examine the Circuit – Chip Planner

■ Start the Chip Planner

- Click Tools
- Click Chip Planner
- Provides a visual display of FPGA resources
- Some preset views are available

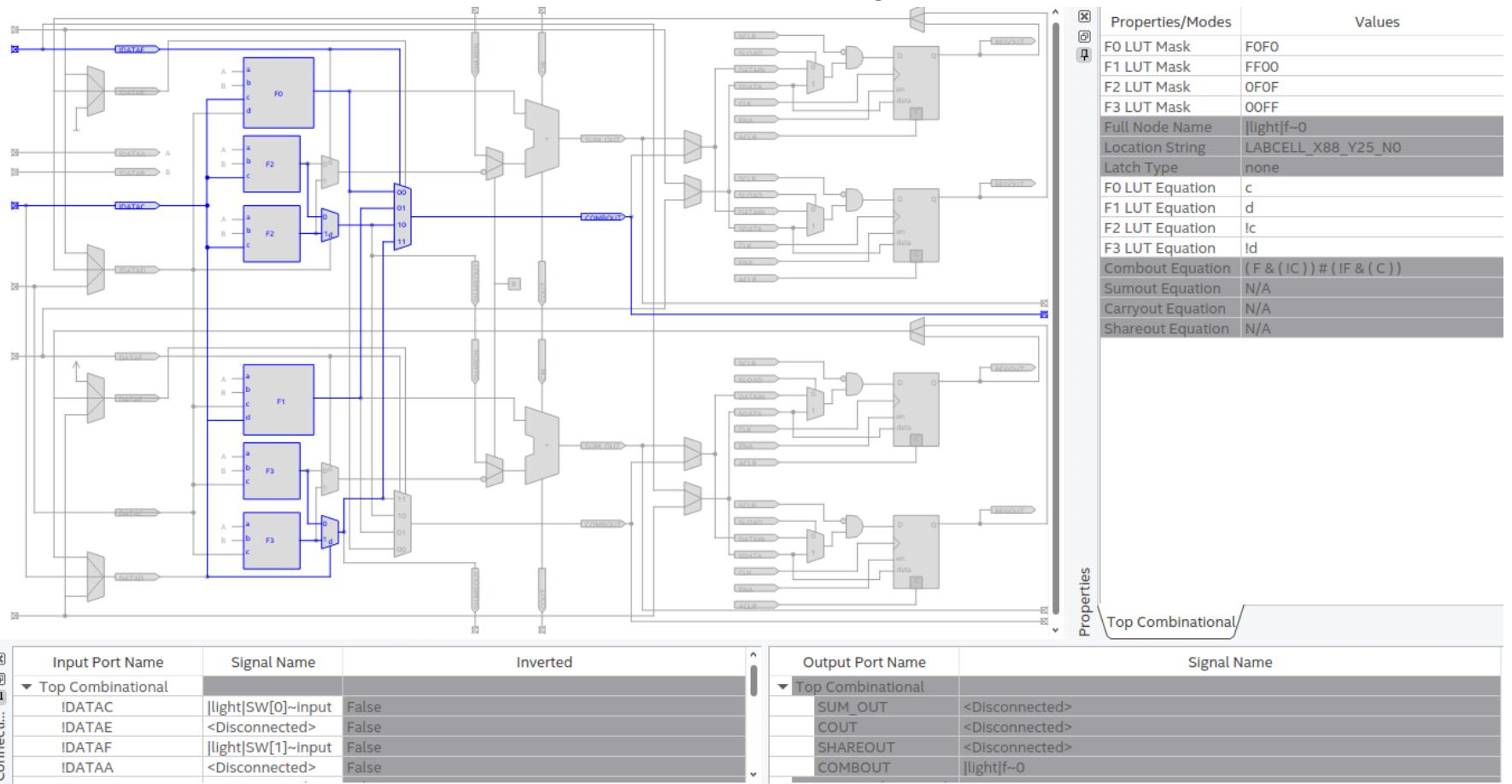


ALTERA®

Step 6: Examine the Circuit – Chip Planner

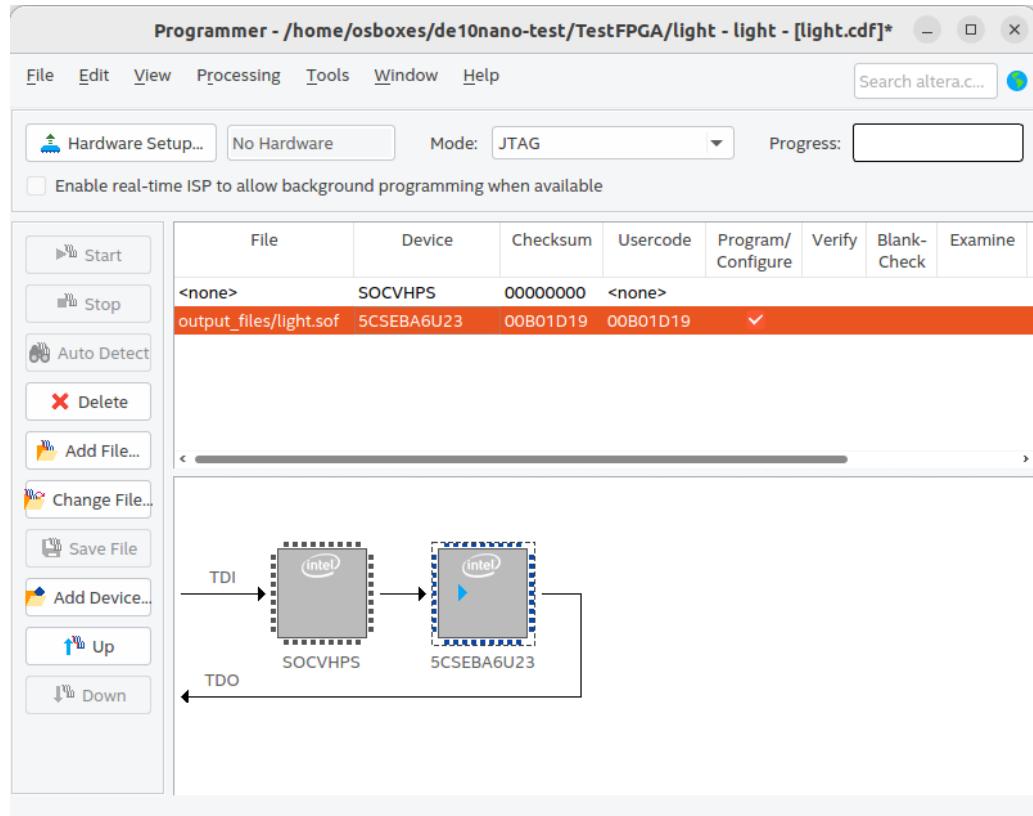
■ Double click on a used “resource”

- Detailed view in the "Resource Property Editor"
- it is possible to “edit” without recompiling



Step 7: Program the DE10 Board

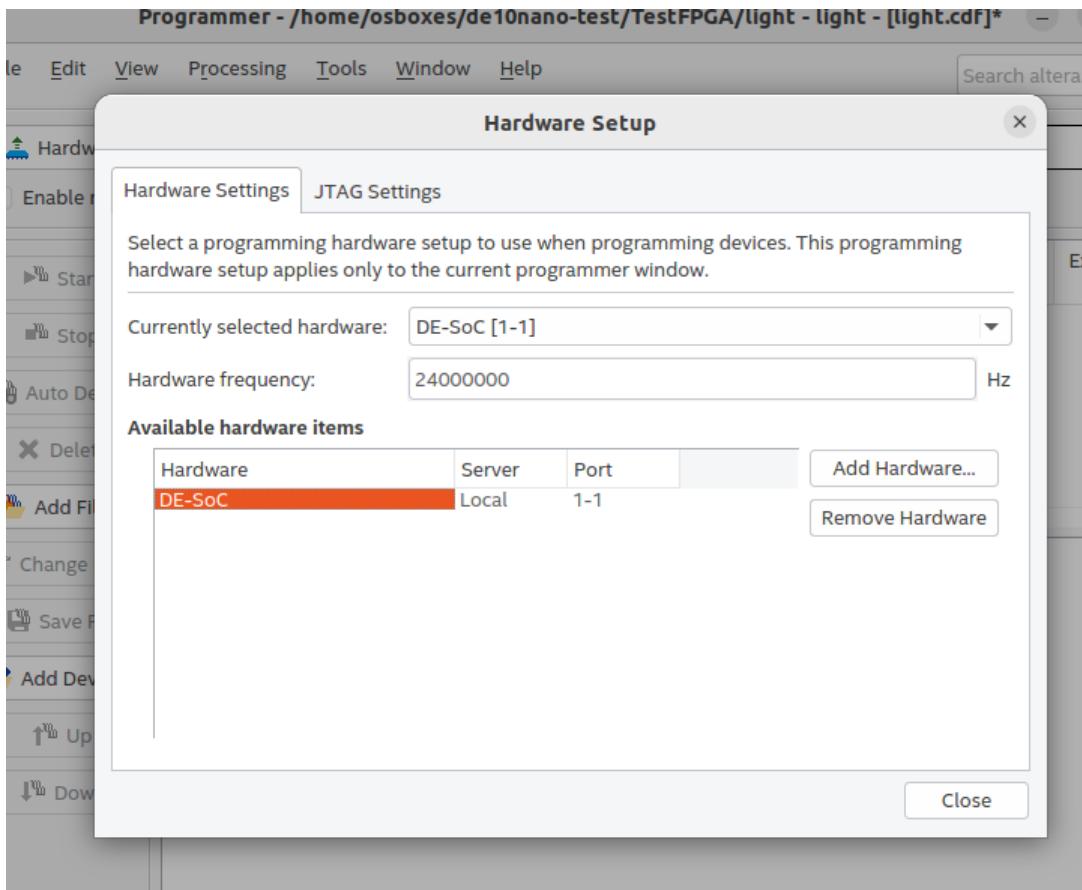
- **FPGA JTAG mode:** it will retain its configuration as long as the power remains turned on.
- Active Serial (AS) mode: a configuration device that includes some flash memory is used to store the configuration data



- Observe that the configuration file light.sof is listed in the programmer window. If the file is not already listed, then click Add File and select it

Step 7: Program the DE10 Board

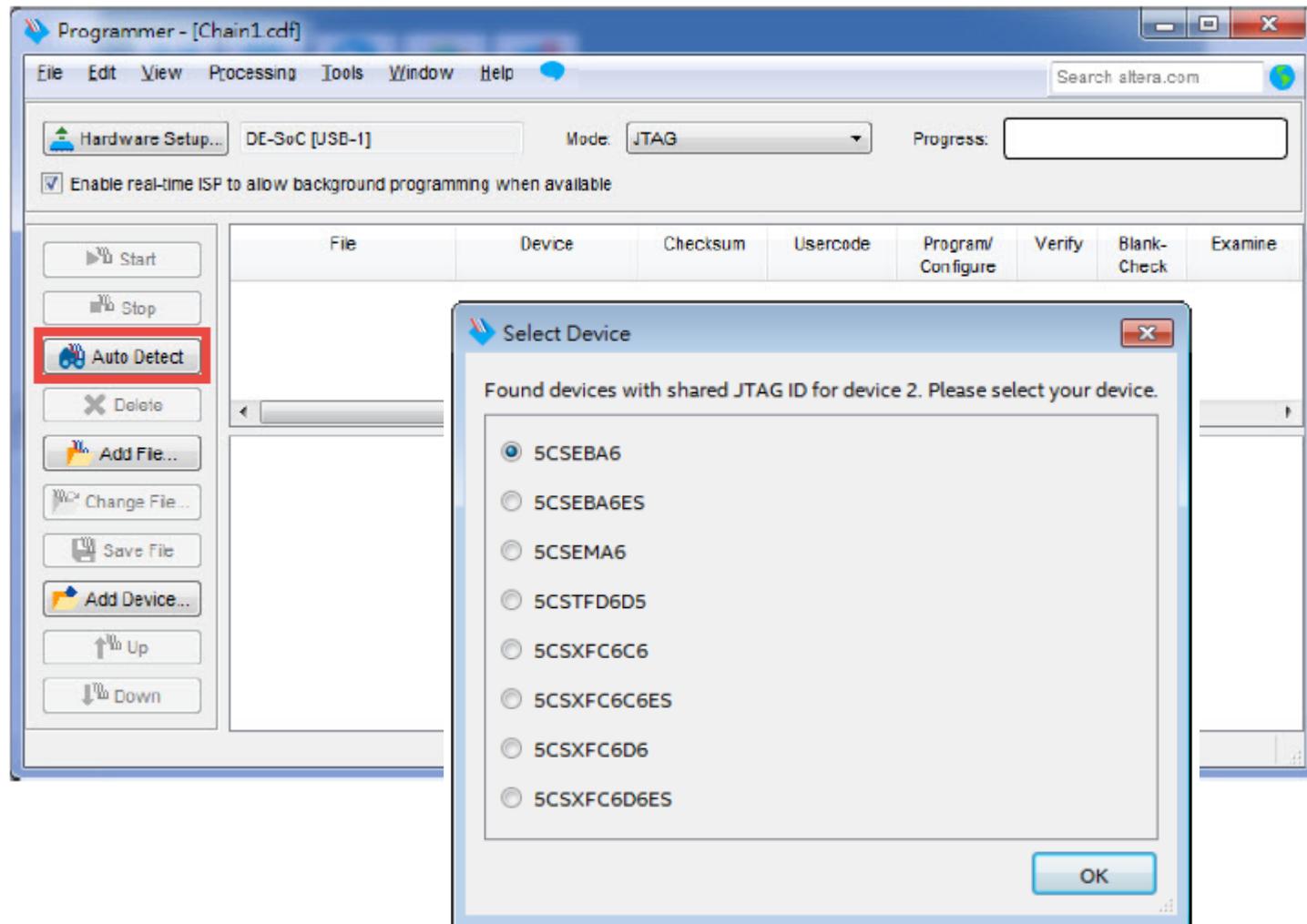
- Here it is also necessary to specify the programming hardware and the mode that should be used. If not already chosen by default, select JTAG in the Mode box.
- Also, if the USB-Blaster is not chosen by default, press the Hardware Setup... button and select the DE-SoC in the window that pops up



ALTERA®

Step 7: Program the DE10 Board

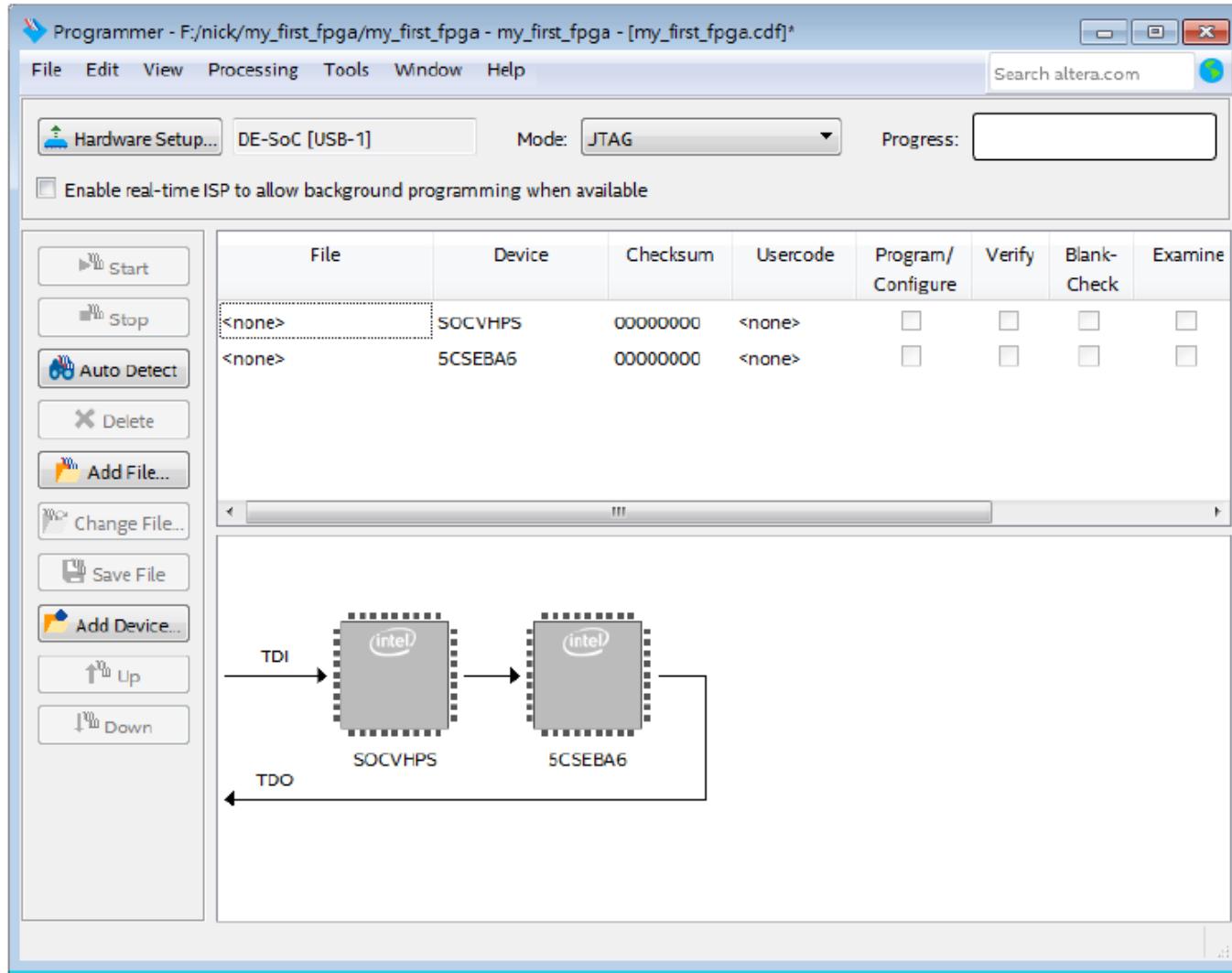
- Click “Auto Detect”
- Select the device associated with the board



ALTERA®

Step 7: Program the DE10 Board

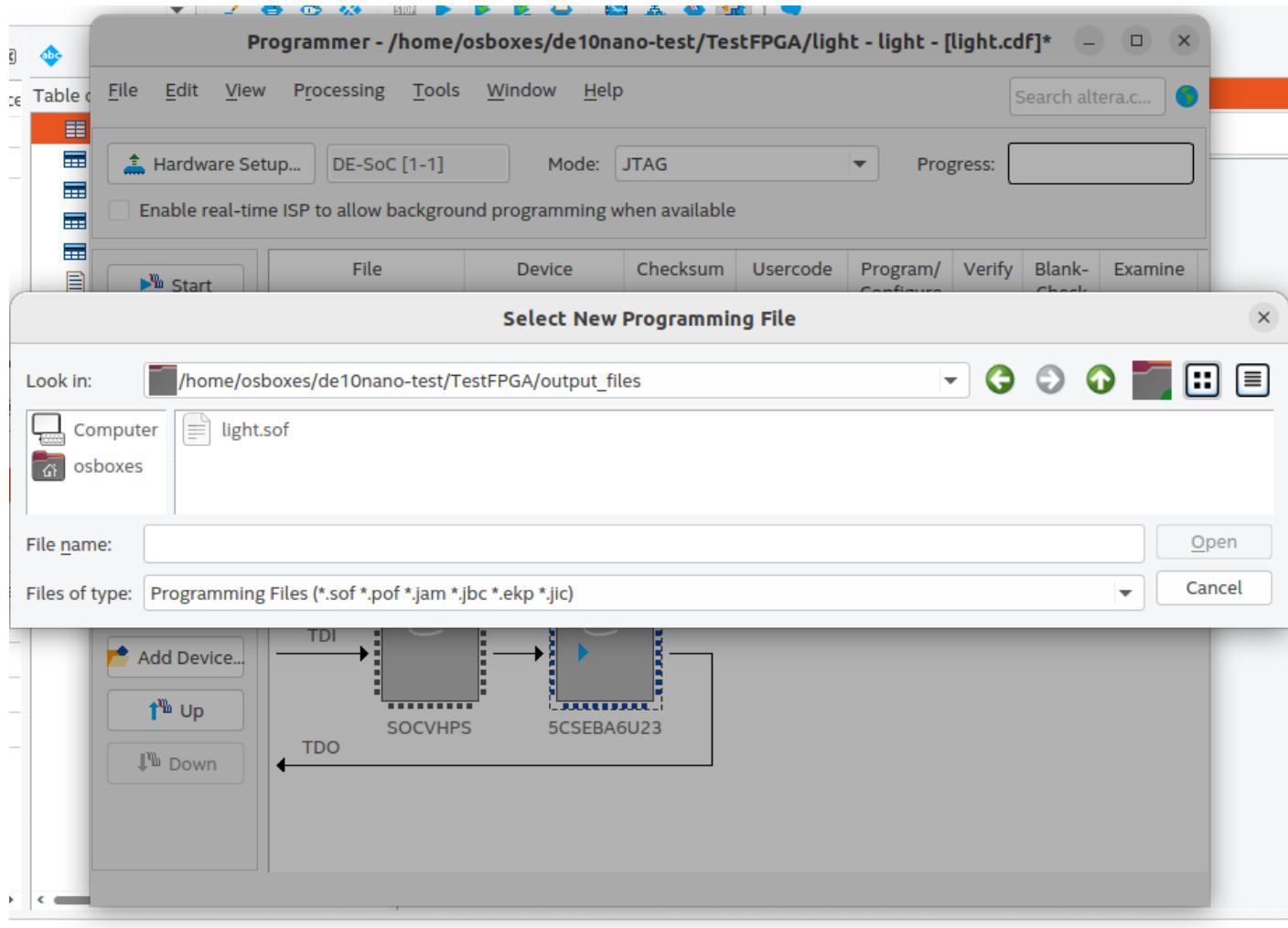
- FPGA and HPS devices are shown in the JTAG chain



ALTERA®

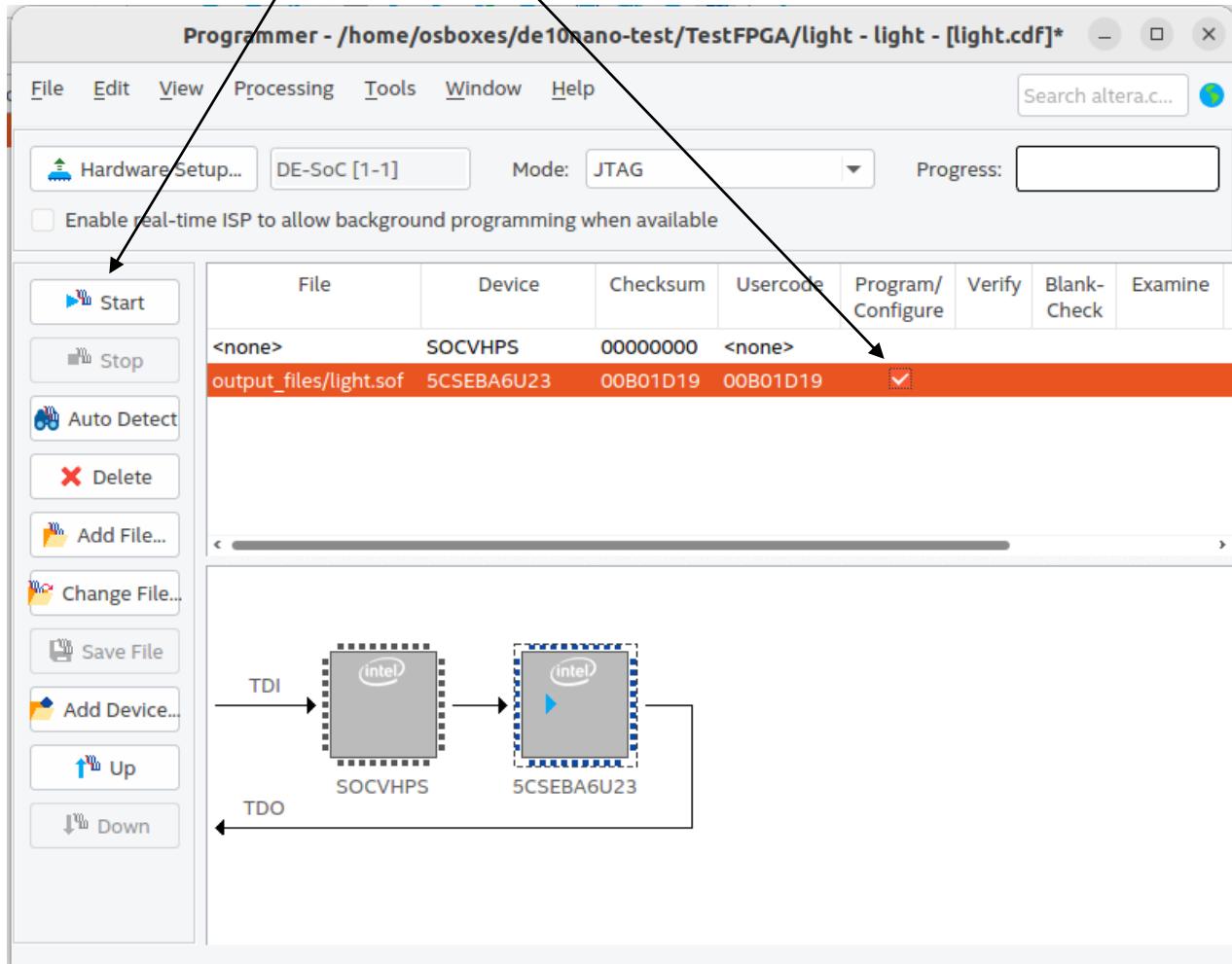
Step 7: Program the DE10 Board

- If needed, click “Change File..”, and then select .sof file for FPGA in the “output_files” subfolder



Step 7: Program the DE10 Board

- Click “Program/Configure” check box,
- and then click “Start” button to download .sof file into FPGA



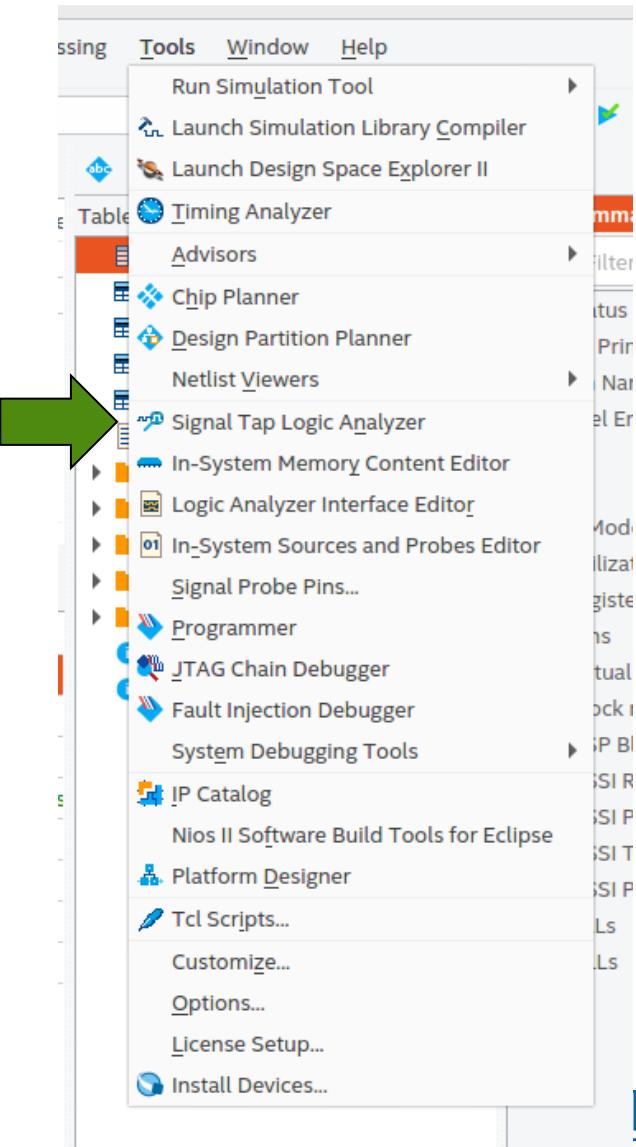
ALTERA®

Step 8: See your design work on the board

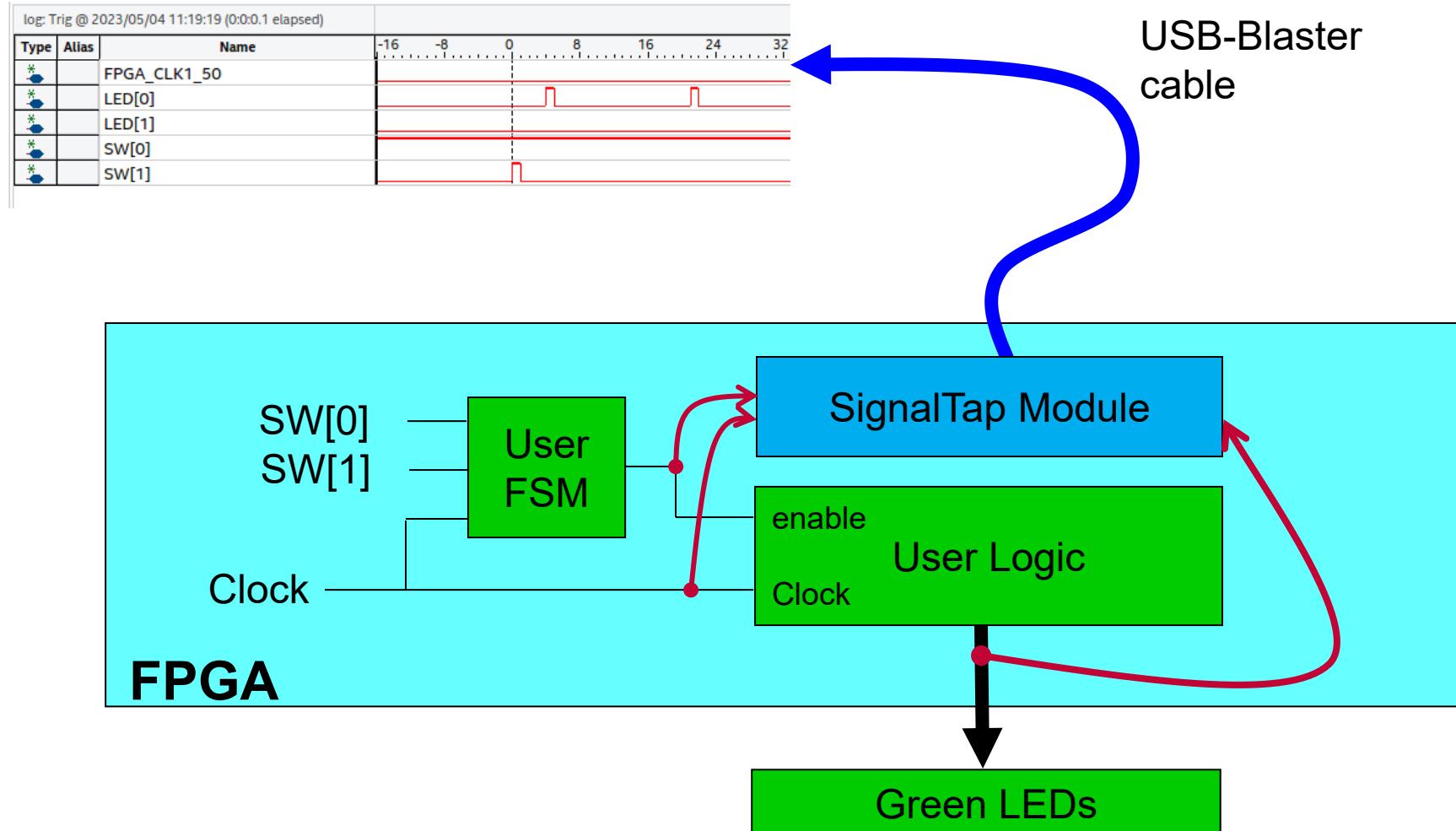
- Having downloaded the configuration data into the FPGA device, you can now test the implemented circuit.
- Try all four valuations of the input variables x_1 and x_2 , by setting the corresponding states of the switches SW1 and SW0.

SignalTap II Embedded Logic Analyzer

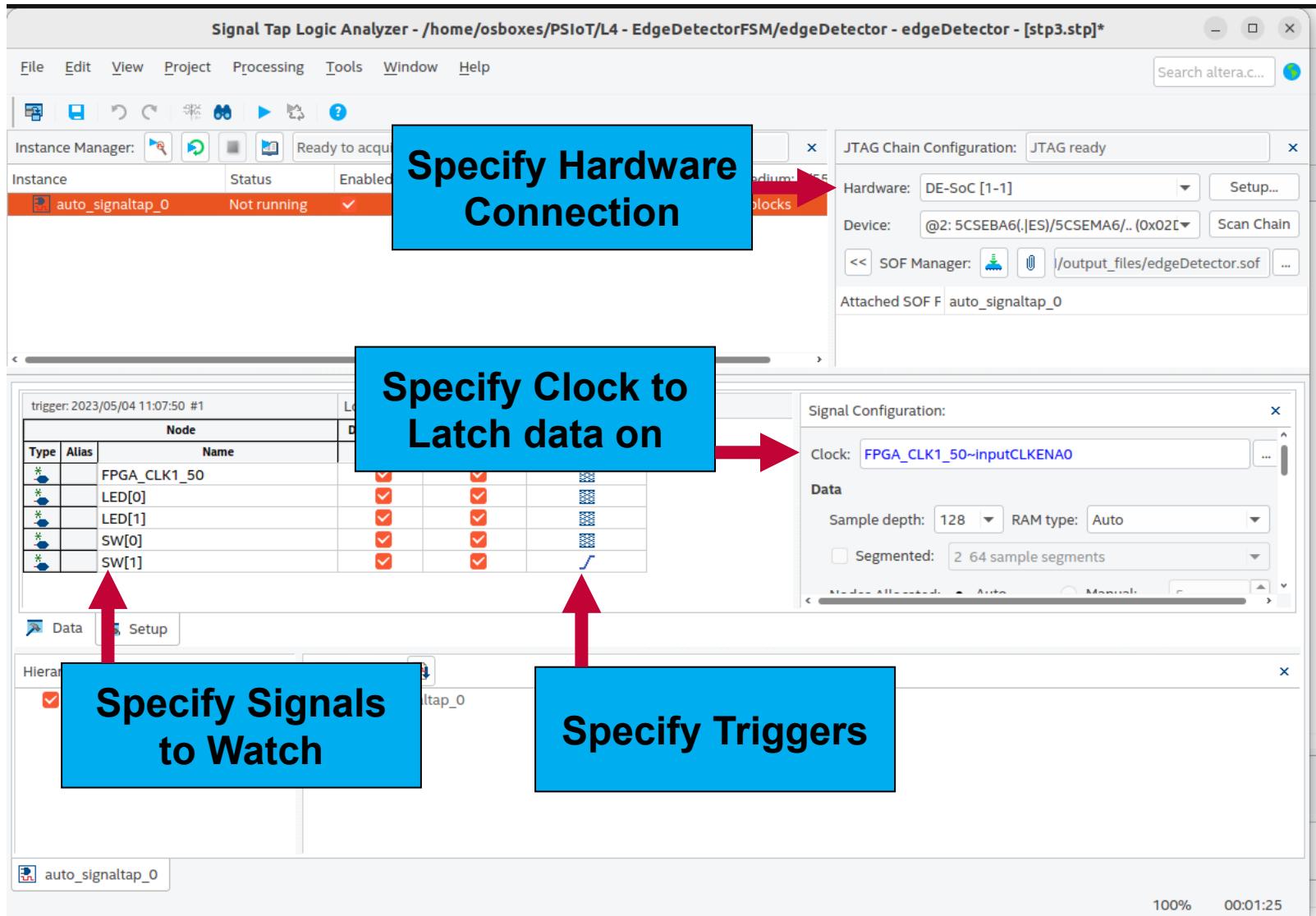
- A soft logic analyzer
 - Instantiate as a module in your design
- Connects to the board on which a design is running
- Collects data when a trigger event occurs
- Displays data on your computer
- How does it work?



SignalTap II Operation



Setup SignalTap II



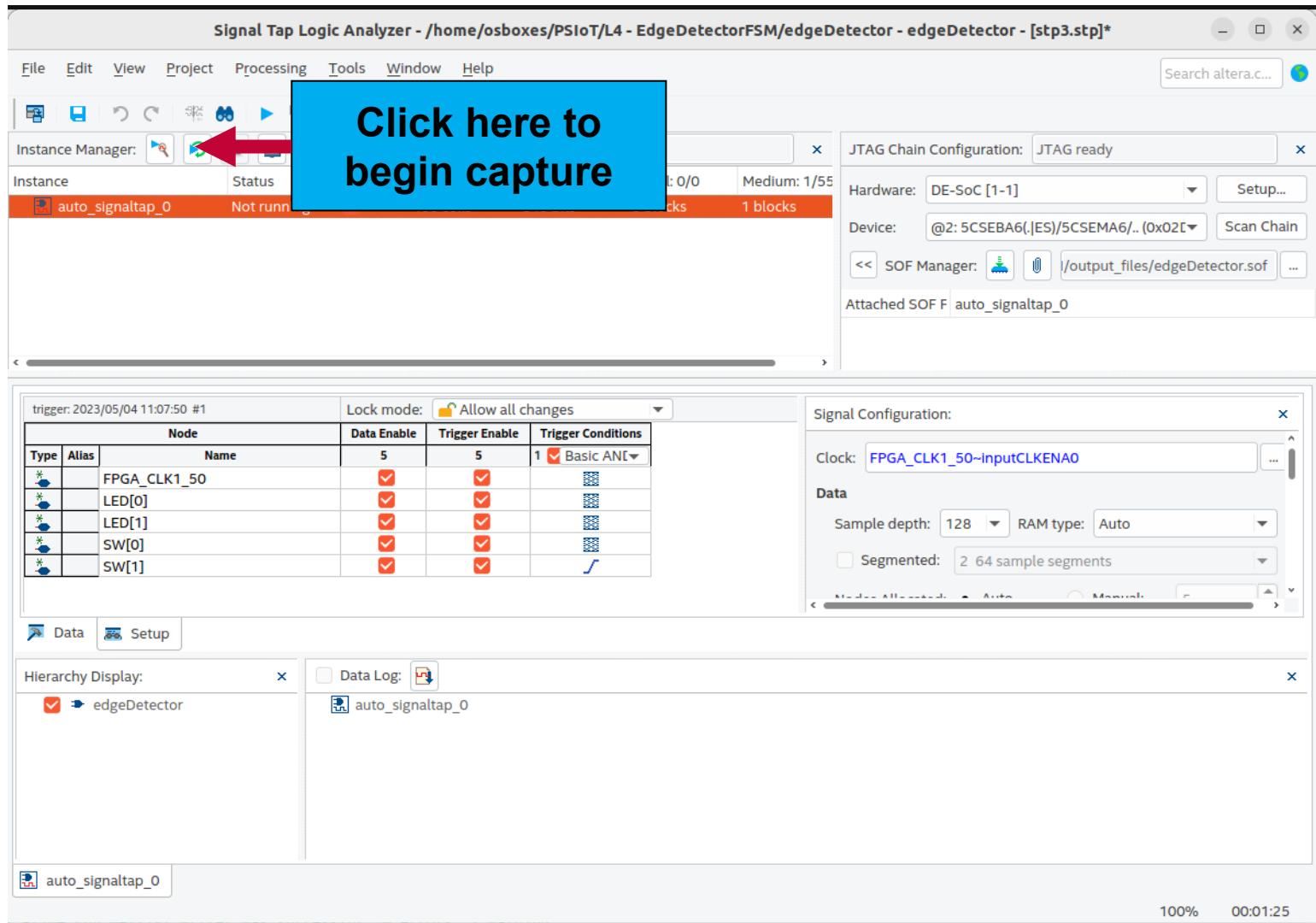
ALTERA®

Recompile Project

- For changes to take effect recompile project
- Once recompiled, download it to the board
- Note: The circuit will be larger than before
 - Memory is used to store captured data

Flow Summary	
	<<Filter>>
Flow Status	Successful - Thu May 4 11:18:14 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	edgeDetector
Top-level Entity Name	edgeDetector
Family	Cyclone V
Device	5CSEBA6U23I7S
Timing Models	Final
Logic utilization (in ALMs)	232 / 41,910 (< 1 %)
Total registers	434
Total pins	13 / 314 (4 %)
Total virtual pins	0
Total block memory bits	640 / 5,662,720 (< 1 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSS	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSS	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

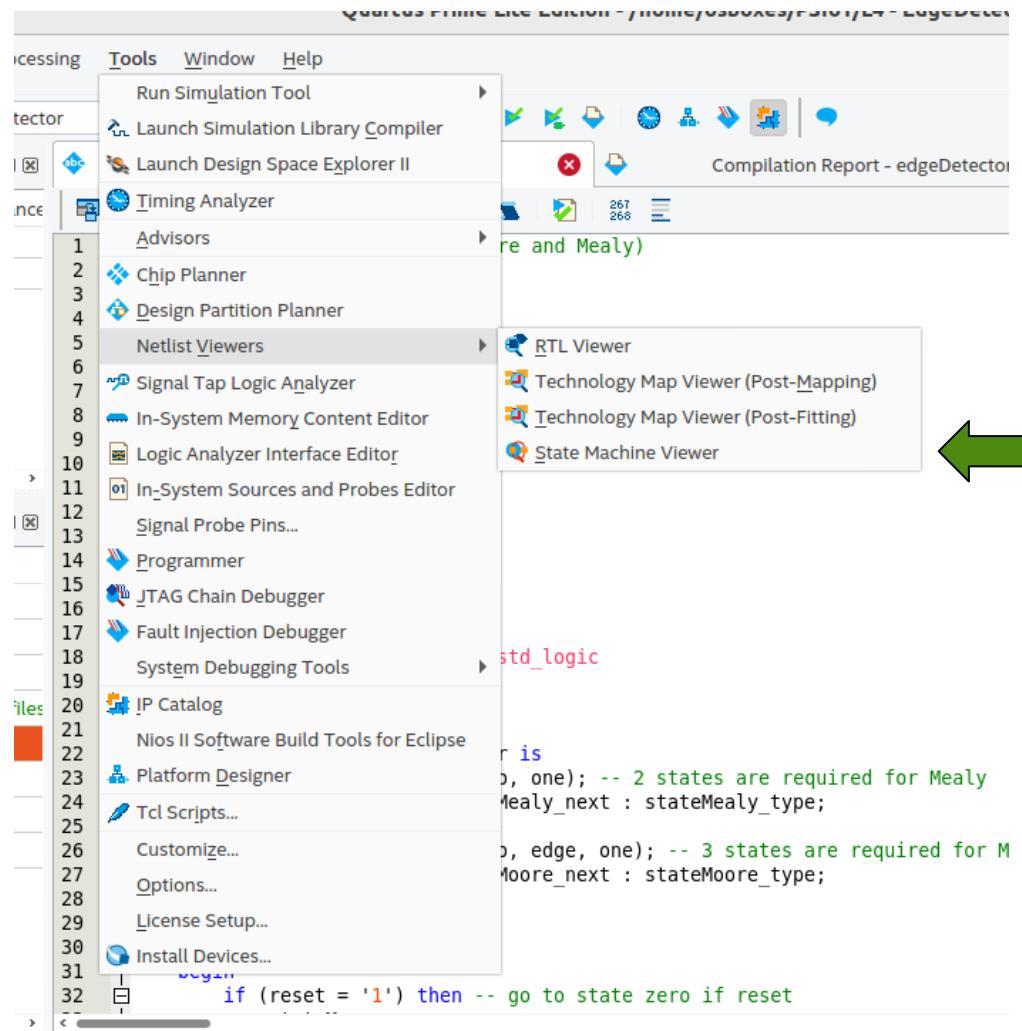
Setup Event Trigger



ALTERA®

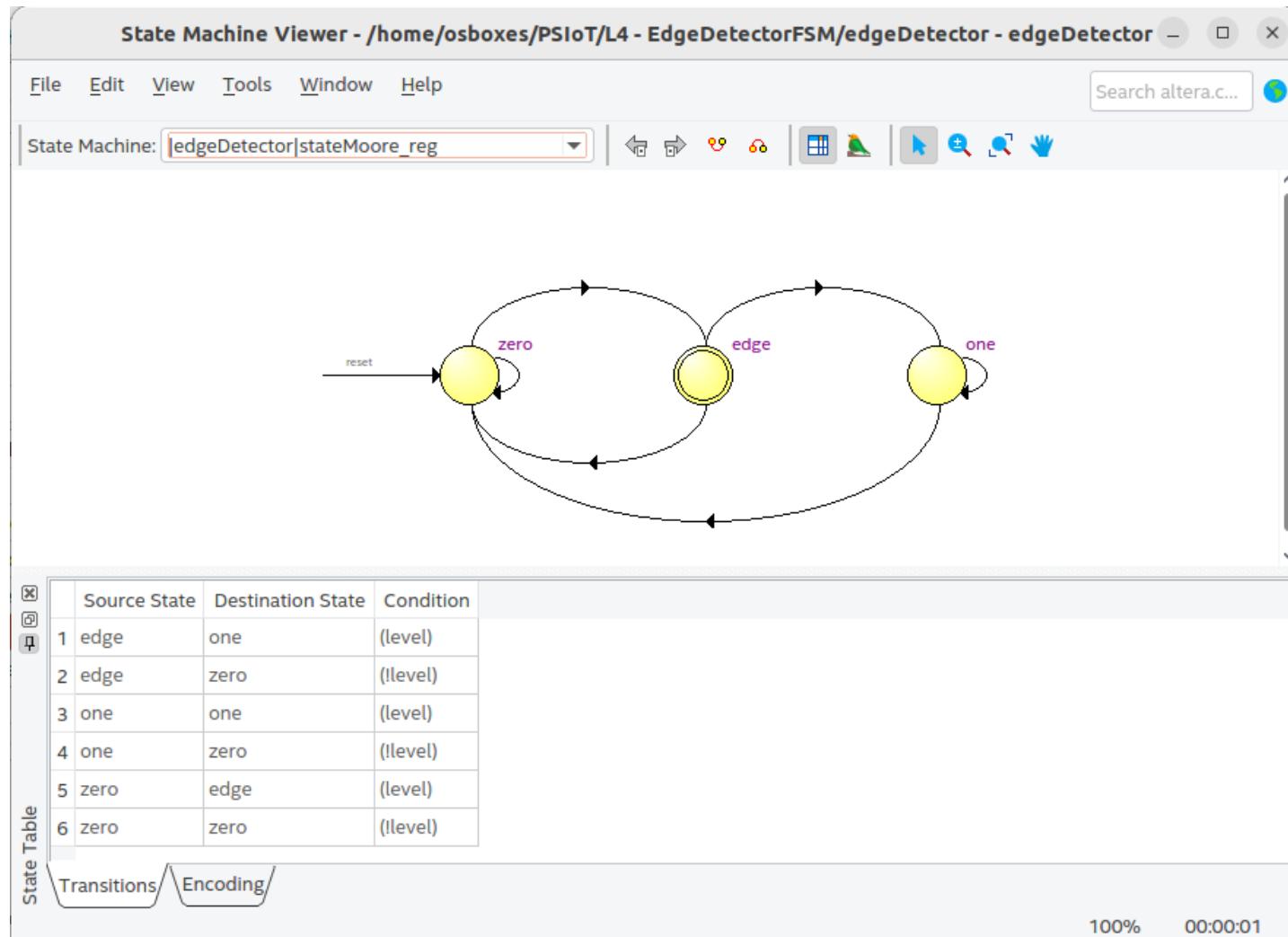
FSM Viewer

- Open the FSM Viewer
 - Click **Tools**
 - Expand **Netlist Viewers**
 - Click **State Machine Viewer**



ALTERA®

Examine State Machine



ALTERA®