	Study		Implementation					
Feature	**Verification requirements**	**Owner**	**Verification development**	**Testcases**	**Owner**	**Dev. Status**	**Start dev**	**End dev**
Which part is being tested:	***What is end goal of the test:***		***What will be checked and what is the expected result:***					
Memory driver	Driven by the input and the clock triggering Memory driver should start processing the data given	Emilija	Driven by the data_in input and clock on positive edge, Memory driver(FIFO) gets filled with data	memory_driver_data	Emilija	passed	25.01.2021	19.1.2021
Memory driver	The Mem Driver takes in 32bit data from the shit register and puts it in a FIFO buffer	Emilija	data_in is 32 bits	memory_driver_valid-in	Emilija	passed	25.01.2021	19.1.2021
Memory driver	If the memory is not full it then sends a write command to the memory by triggering the WR signal	Emilija	"write" signal is incremented at any time when a value of "valid_in"signal approaches	memory_driver_write	Emilija	passed	25.01.2021	19.1.2021
Memory driver	Write command to the memory by triggering the WR signal and specifying the address where the data should be written.	Emilija	"write" signal is incremented at any time when a value of "valid_in"signal approaches but it doesn't specify the address	memory_driver_write_address	Emilija	unpassed	25.01.2021	19.1.2021
Memory driver	The value of the address signal should be incremented by one on every data write until the memory is full.	Emilija	"address" signal is incremented but has no affection after the "memory_full" signal	memory_driver_address	Emilija	unpassed	25.01.2021	19.1.2021
Memory driver	The driver should send a stop signal to the counter if the FIFO is full and trigger high the "memory_full" signal when the memory is full	Emilija	"memory_full" and "stop" signals should be corrected because they don't affect the design	memory_driver_stop	Emilija	unpassed	25.01.2021	19.1.2021
Memory driver	"reset" signal is supposted to get the model reseted any time it gets a value of 1 (rising)	Emilija	"reset" signal is successfully resetting the module	memory_driver_reset	Emilija	passed	25.01.2021	19.1.2021