	Study		Implementation					
Feature	**Verification requirements**	**Owner**	**Verification development**	**Testcases**	**Owner**	**Dev. Status**	**Start dev**	**End dev**
Which part is being tested:	***What is end goal of the test:***		***What will be checked and what is the expected result:***					
Shift Register	Shift register to have two inputs from counter	Emilija	Shift should have One 8 bit data , other 1 bit valid_in inputs, corection should be made on the valid_in input	shift_input	Emilija	unpassed	25.01.2021	17.02.2021
Shift Register	Data_in Input should drive data to the shift register	Emilija	Input data_in checked, it drives the signal from the counter as 8 bit data	shift_counter_input	Emilija	passed	25.01.2021	17.02.2021
Shift Register	Output signal to be 32 bits	Emilija	Output data out is tested and it adaptes with qualifications	shift_output	Emilija	passed	25.01.2021	17.02.2021
Shift Register	Shift register is expected to be SIPO and to send output on every 4 valid counter inputs	Emilija	Shift tested and according the results it fullfil the requirments	shift_output_transfer	Emilija	passed	25.01.2021	17.02.2021