Design of Physical Coding Sublayer using 8B/10B Algorithm

N.Kiran Babu, P.S.Srinivas Babu

Abstract-In order to resolve the problem of base-line offset and unbalanced code flow during the fiber data transmission, thesis give a simple and practical solution 8B/10B encoder. This solution taking a method which integrate checking scheme and logic operation, through Verilog HDL description language, realize the design of encoder. The proposed circuit is simulated in Xilinx and Cadence. The results obtained in various tools are presented in this paper.

Keywords – Physical coding sub layer, 8B/10B algorithm, Synchronization, Verilog HDL, Cadence Encounter.

I. INTRODUCTION

Due the quick development of communication of technology, fiber communication is more and more popular for people, at the same time; its higher transmission speed and bigger capacity are required by people. But, high-speed fiber transmission bring problem as base-line offset and unbalanced code flow. So, based on such problems, we design the 8B/10B encode, because its low transmission mistake percent and DC compensation function, also with checking mistake function during the transmission and special function, it resolve the problem as base-line offset and unbalanced code flow, but also was used in high-speed bus.
The PCS and the PMA are both contained within the physical layer of the OSI reference model. The PCS and the Gigabit Media Independent Interface (GMII) communicate with one another via 8-bit parallel data lines and several control lines. The PCS is responsible for encoding each octet passed down from the GMII into ten bit code groups. The PCS is also responsible for decoding ten bit code groups passed up from the PMA into octets for use by the upper layers. The PCS also controls the auto-negotiation process which allows two separate gigabit devices to establish a link of which they are both capable of using.

II. PCS FUNDAMENTALS

2.1 8B/10B CODING:

The PCS examines each incoming octet passed down by the GMII and encodes it into a ten bit code group; this is referred to as 8B/10B encoding. Many serial data transmission standards utilize 8b/10b encoding to ensure sufficient data transitions for clock recovery.
The principle of encoder is mapping transfer the input 8 bits data into 10 bits data per the mapping principle, separate the 8 bits data into one group 3 bits data and another group 5bits data, after encoding of the 8B/10B encoder, output one group 4 bits data and another group 6 bits data, to make a 10 bit data. This coding scheme is used for high-speed serial data transmission.

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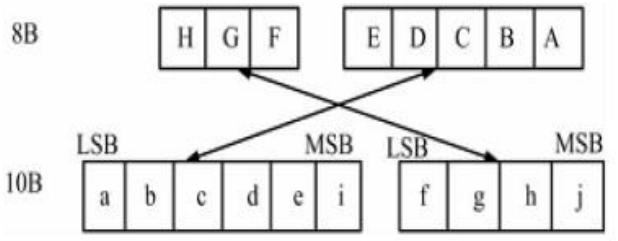

Figure 1. 8B/10B encoding relationship

It is important to ensure the DC balance of data flow during the transmission process, also need to think about the unbalance of DC data flow. As show in Table.2, for each 8B data, after encoding, it will be transferred into one kind of RD-&RD+. Encoder will decide the next 10B data based on previous RD and ensure the DC data flow balance.
The original status of encoder is RD-, it will check the data flow, if the quantity of number 1 and number 0 is the same, the polarity of next 10B data will keep RD-, and otherwise, it will turn to be RD+. If previous 10B polarity is RD+, and the quantity of number 1 and number 0 of previous 10B data keep same, the polarity of next 10B data will keep RD+.

2.2. Physical Coding Sublayer (PCS):

The PCS interface is the Gigabit Media Independent Interface (GMII) which provides a uniform interface to the Reconciliation sublayer for all 1000 Mb/s PHY implementations (e.g., not only 1000BASE-X but also other possible types of gigabit PHY entities). 1000BASE-X provides services to the GMII in a manner analogous to how 100BASE-X provides services to the 100 Mb/s MII.
The 1000BASE-X PCS provides all services required by the GMII, including:

a. Encoding (decoding) of GMII data octets to (from) ten-bit code-groups (8B/10B) for communication with the underlying PMA.

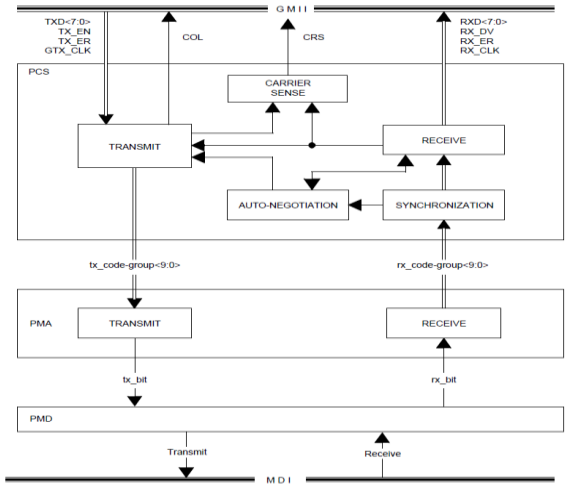

Figure 2. PCS Block Diagram

b. Generating Carrier Sense and Collision Detect indications for use by PHY's half-duplex clients.
c. Managing the Auto-Negotiation process, and informing the management entity via the GMII when the PHY is ready for use.

2.3. PMA (Physical Medium Attachment):

The PMA (shown in Figure2) serializes and de-serializes the coded group between the PCS and PMD. This is accomplished by recovery of the clock from the coded data from PMD and multiplying by 10 of the parallel data rate. The PMA also functions as recovering the clock from the incoming data stream.

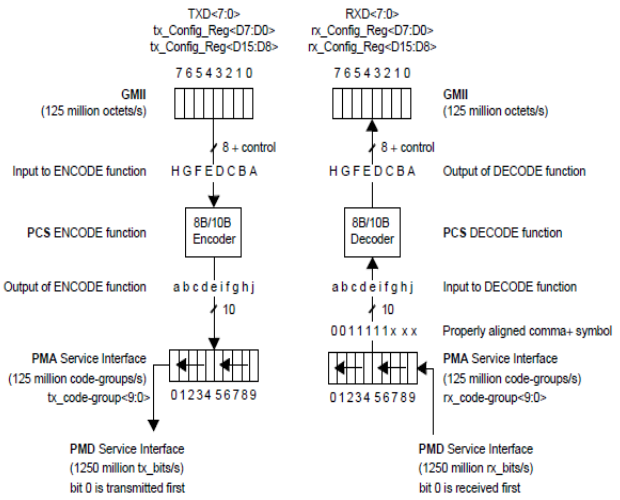

Figure 3.PCS reference diagram

a. Running Disparity:

Running Disparity is a technique used in digital communication in order to maintain a DC balance in digital transmissions. For ex: if there are too many ones bunched together in the data stream, then, Zero's are added to the data and vice-versa.

What this does is that, in average, the numbers of ones are equal to number of Zeros in a transmission stream. A DC balanced signal is more immune to noise and easier to recover at the end of the line.

Running disparity for the sub-blocks is calculated as follows:

a) Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011;

b) Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100.

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100

Table 4.1: 8B/10B running disparity encoding examples

c) Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub block.

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
K28.0	1C	000 11100	001111 0100	110000 1011
K28.1	3C	001 11100	001111 1001	110000 0110
K28.2	5C	010 11100	001111 0101	110000 1010
K28.3	7C	011 11100	001111 0011	110000 1100
K28.4	9C	100 11100	001111 0010	110000 1101
K28.5	BC	101 11100	001111 1010	110000 0101

Table 4.2. Valid special code-groups

The /K28.5/ special code-group is chosen as the first code-group of all ordered_sets which are signaled repeatedly and for the purpose of allowing a receiver to synchronize to the incoming bit stream (i.e., /C/ and /I/).

b. Carrier sense:

Carrier sense means that a transmitter uses feedback from a receiver to determine whether another transmission is in progress before trying to send. That is, it tries to detect the presence of a carrier wave from another station before attempting to transmit. If a carrier is sensed, the station waits for the transmission in progress to finish before initiating its own transmission.

The Carrier Sense process controls the GMII signal CRS:

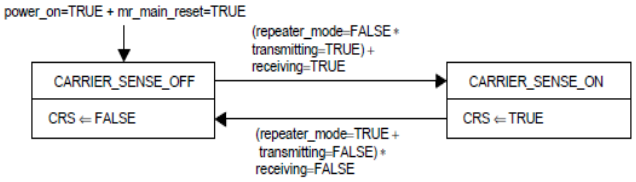

Figure 4-Carrier sense state diagram.

By using state diagram we can find the crs signal. If both transmitter and receiver are occur at same time we can get the crs signal as high, otherwise crs signal as low.

c. Synchronization:

The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions.

d. Auto-Negotiation:

The Auto-Negotiation process shall provide the means to exchange configuration information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities.

Auto negotiation is an Ethernet procedure by which two connected devices choose common transmission parameters, such as speed, duplex mode, and flow control. In this process, the connected devices first share their capabilities regarding these parameters and then choose the highest performance transmission mode they both support. In the OSI model, auto negotiation resides in the physical layer. For Ethernet over twisted pair it is defined in clause 28 of IEEE 802.3.

Auto negotiation was originally defined as an optional component in the fast Ethernet standard. It is backwards compatible with 10BASE-T. The protocol was significantly extended in the gigabit Ethernet standard, and is mandatory for 1000BASE-T gigabit Ethernet over copper.

- Provide easy, plug-and-play upgrades from 10 Mbps, 100 Mbps, and 1000 Mbps as the network infrastructure is upgraded.
- Prevent network disruptions when connecting mixed technologies such as 10BaseT, 100BaseTX, and 1000BaseT.
- Accommodate future PHY (transceiver) solutions
- Allow manual override of auto-negotiation
- Support backward compatibility with 10BaseT
- Provide a parallel detection function to recognize 10BaseT, 100BaseTX, and 100BaseT4 non-NWay devices.

Defines the valid data code-groups (D code-groups) of the 8B/10B transmission code. Defines the valid special code-groups (K code-groups) of the code. The tables are used for both generating valid code-groups (encoding) and checking the validity of received code-groups (decoding). each octet entry has two columns that represent two (not necessarily different) code-groups.

In this project, we used top-down methodology to complete our design. We divide the whole PHY into small locks, and these blocks can be further divided within themselves until each block is manageable. For example, his hierarchy tree of PCS is shown in figure 5.

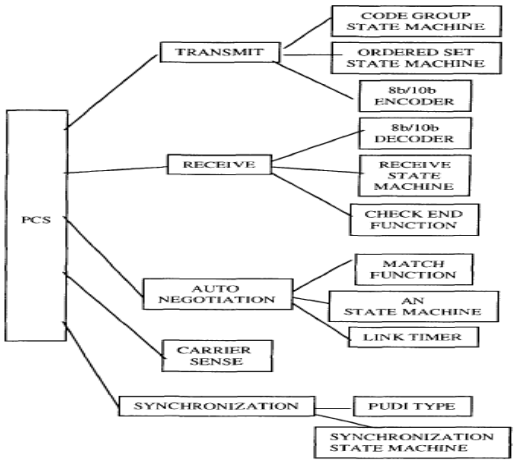

Figure 5. Hierarchy tree of the PCS

III. SIMULATION RESULTS

The simulation results shown are shown in fig5 and 6.Here the outputs are we get the both encoding and decoding by using 8B/10B coding algorithm. For transmitter side here we use the encoder and carrier sense.

The simulation results of encoder and carrier sense is shown below as Fig 6 & 7.

The following are the output waveforms in **Xilinx:**

Figure6--8B/10B encoder.

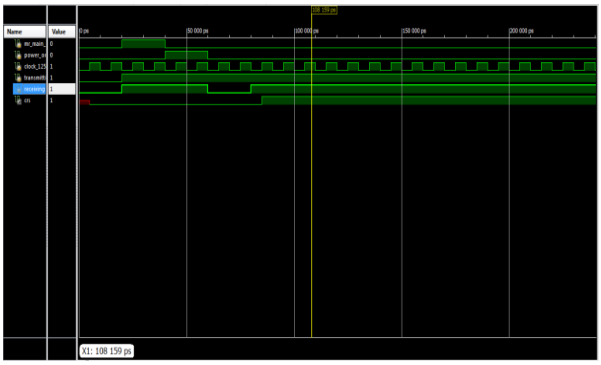

Figure7—Carrier sense.

The simulation results of decoder and SIPO is shown below as Fig 8& 9.

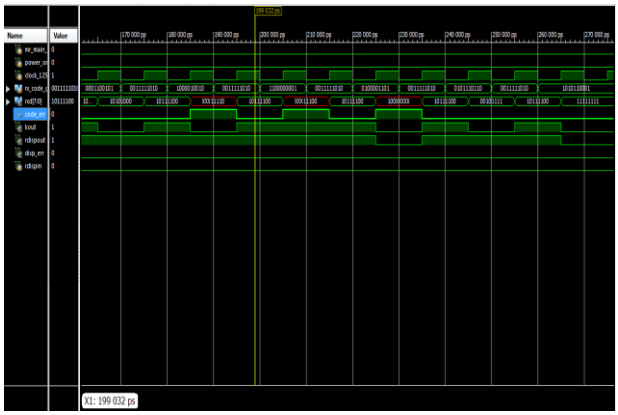

Figure8--8B/10B decoder.

Figure9--SIPO.

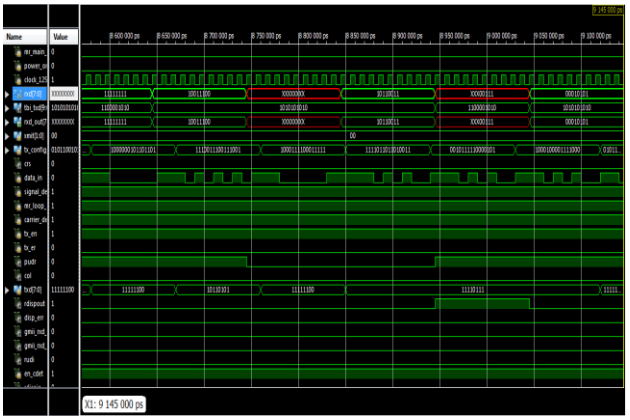

Figure10—final output waveform for PCS in Xilinx.

The simulation results of PCS are shown below as Fig 11.by using cadence Encounter and we get layout as Fig12.
The following are the output waveforms in **Cadence**:

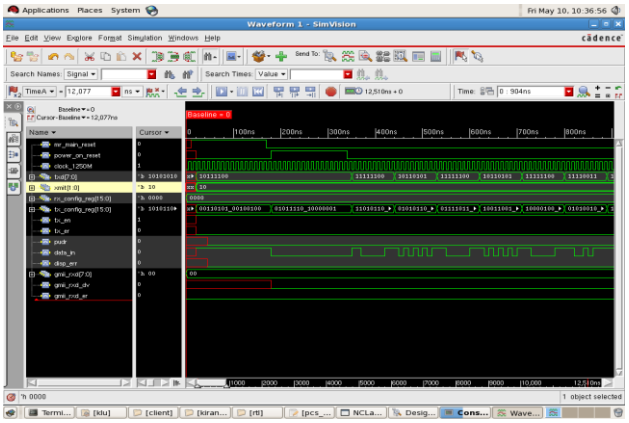

Figure11-- Output waveform in cadence for PCS.

Layout for PCS by using Cadence Encounter:

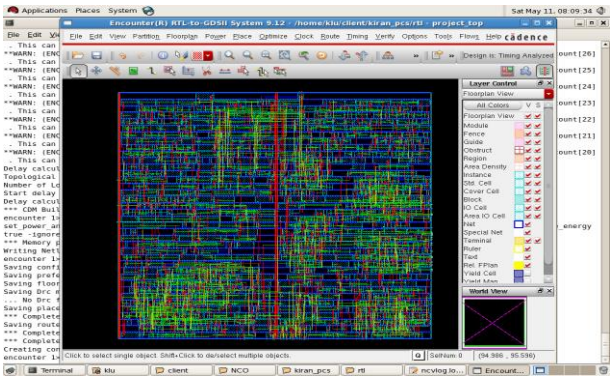

Figure12—layout in cadence for PCS

Power dissipation for layout in cadence – 452.210µW

IV. CONCLUSION

In this paper the design of 8B/10B encoder of PCS is part of FPGA optical fiber communication, the demand of simple program logic relation, clear level demarcate, fast speed is put forward in The plan, which can be achieved by simulation. This program can be used in need 8B/10B coding of optical fiber coding remote data transmission system.

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