# PHY PCIE/USB/SATA

Prof. Jorge Soto

IE-0523 Circuitos Digitales II

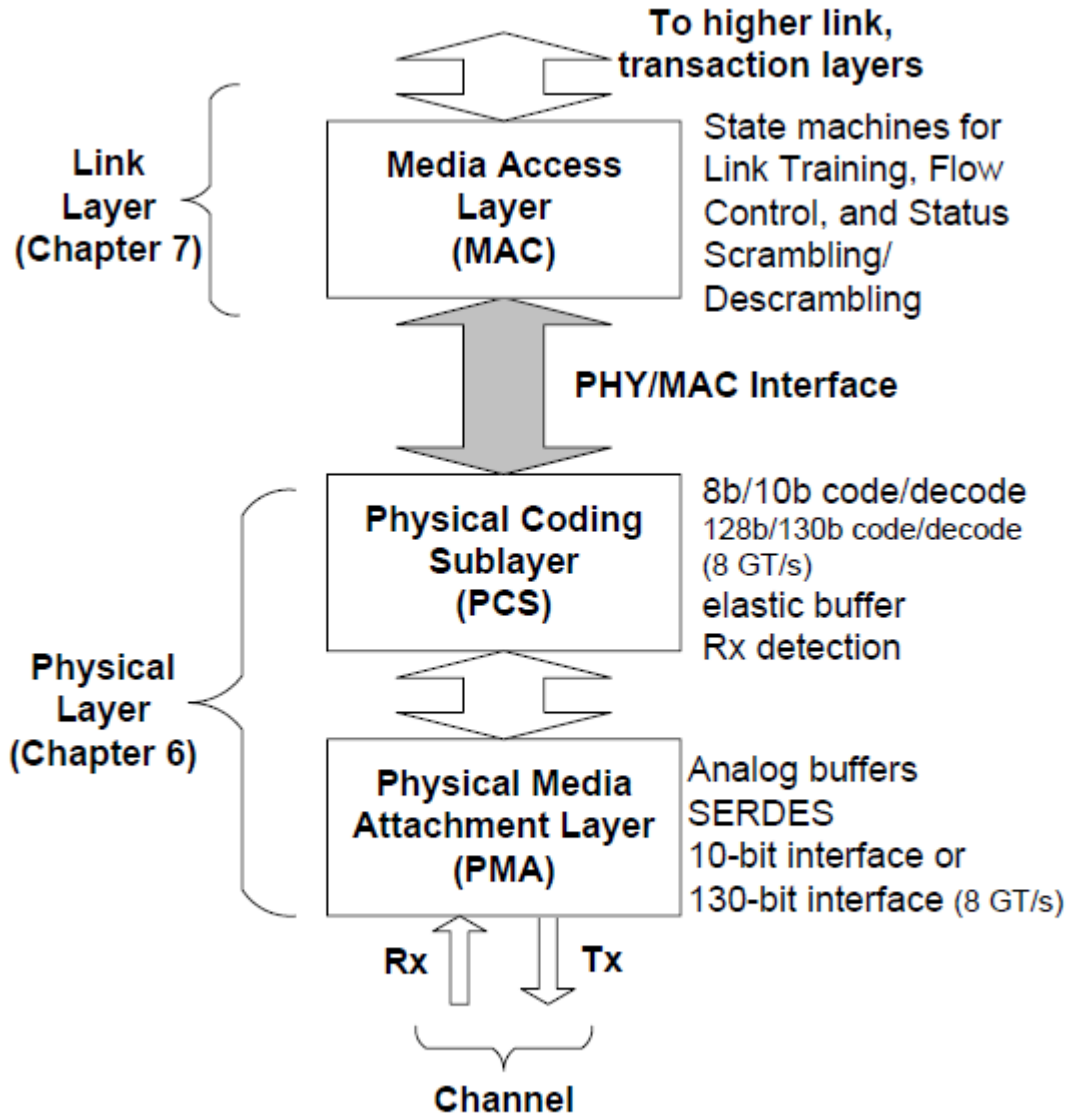
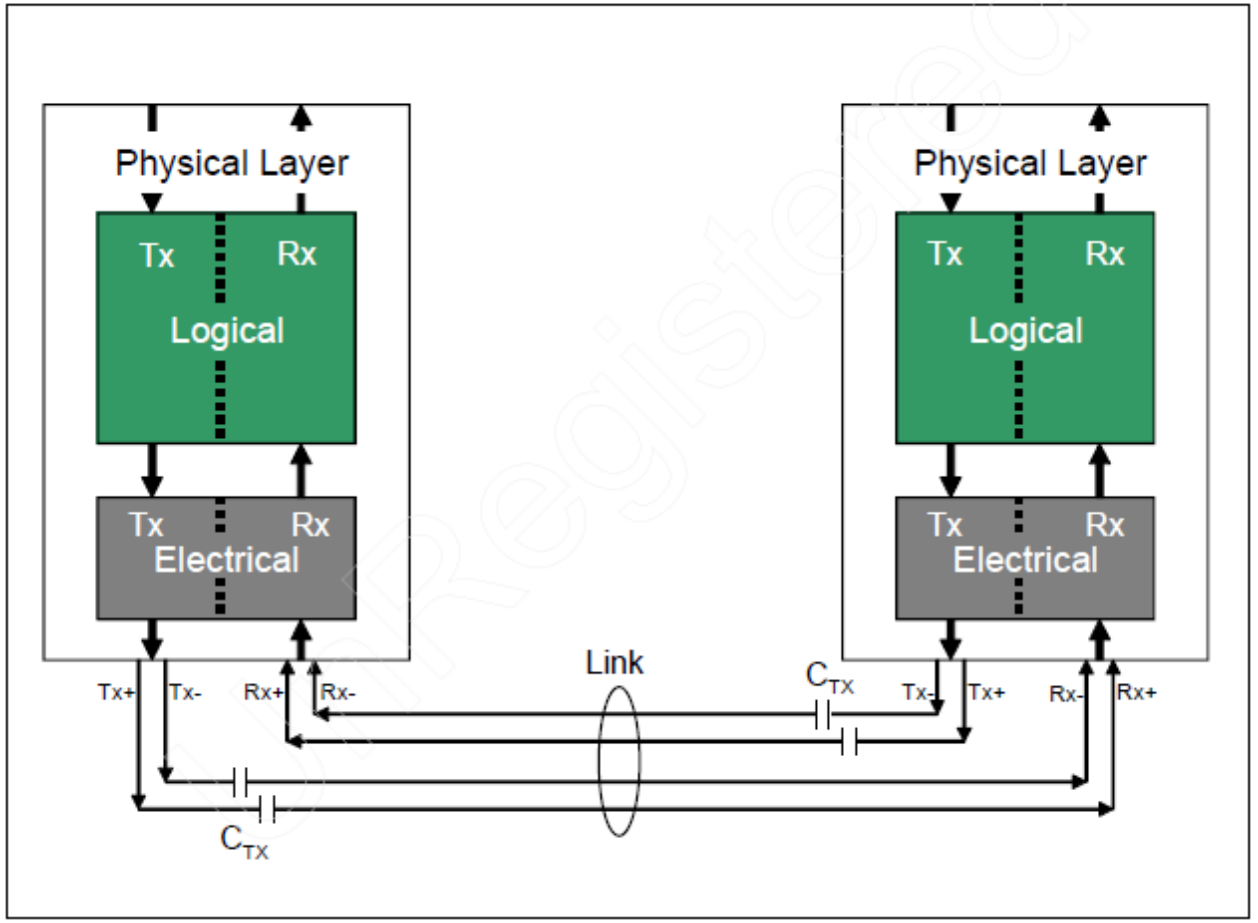



**Figure 2-2 Partitioning PHY Layer for USB SuperSpeed**

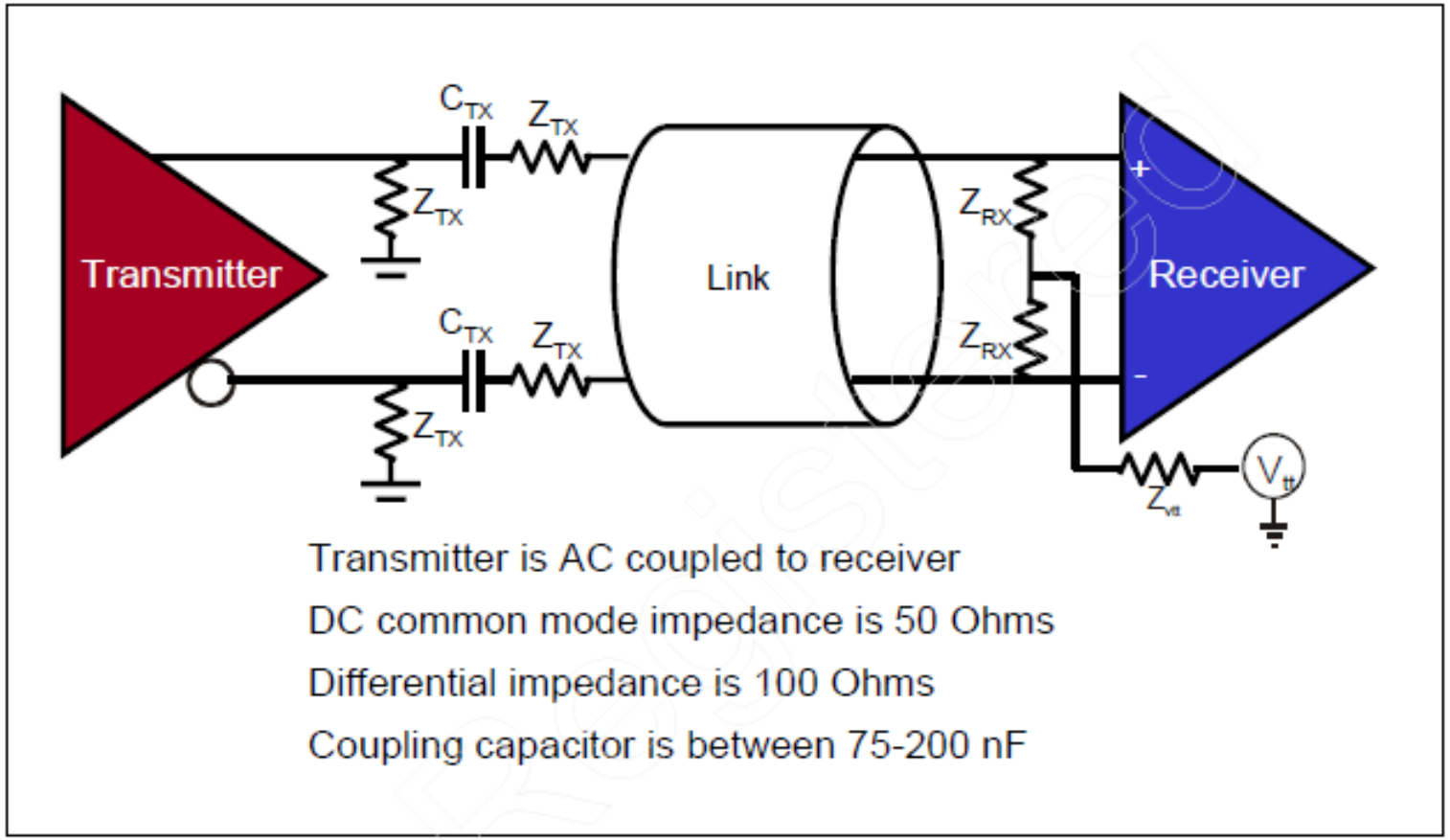
# Enlace de dos capas físicas

*Figure 11-2: Logical and Electrical Sub-Blocks of the Physical Layer*



# Capa física eléctrica

*Figure 2-30: Electrical Physical Layer Showing Differential Transmitter and Receiver*



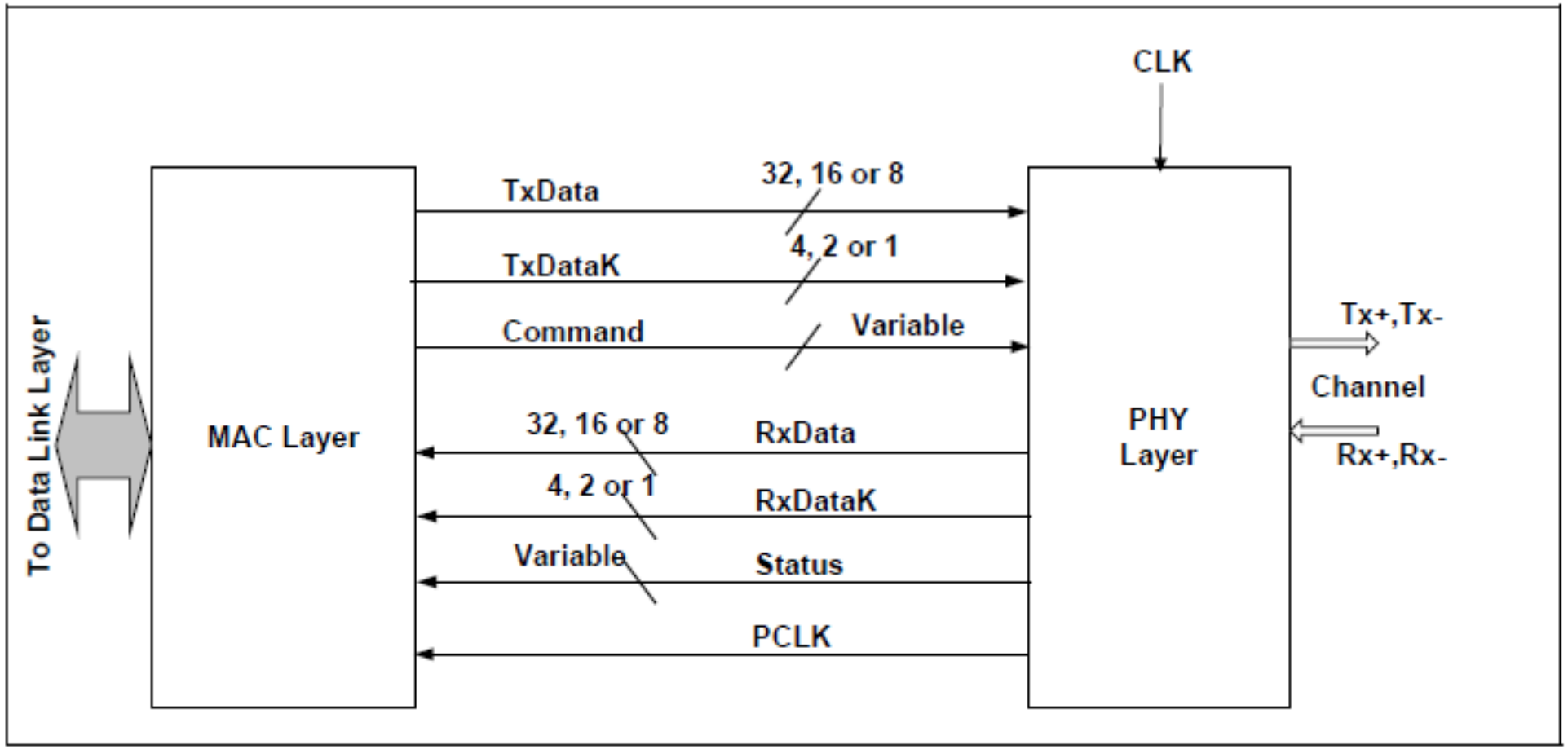



**Figure 3-1: PHY/MAC Interface**

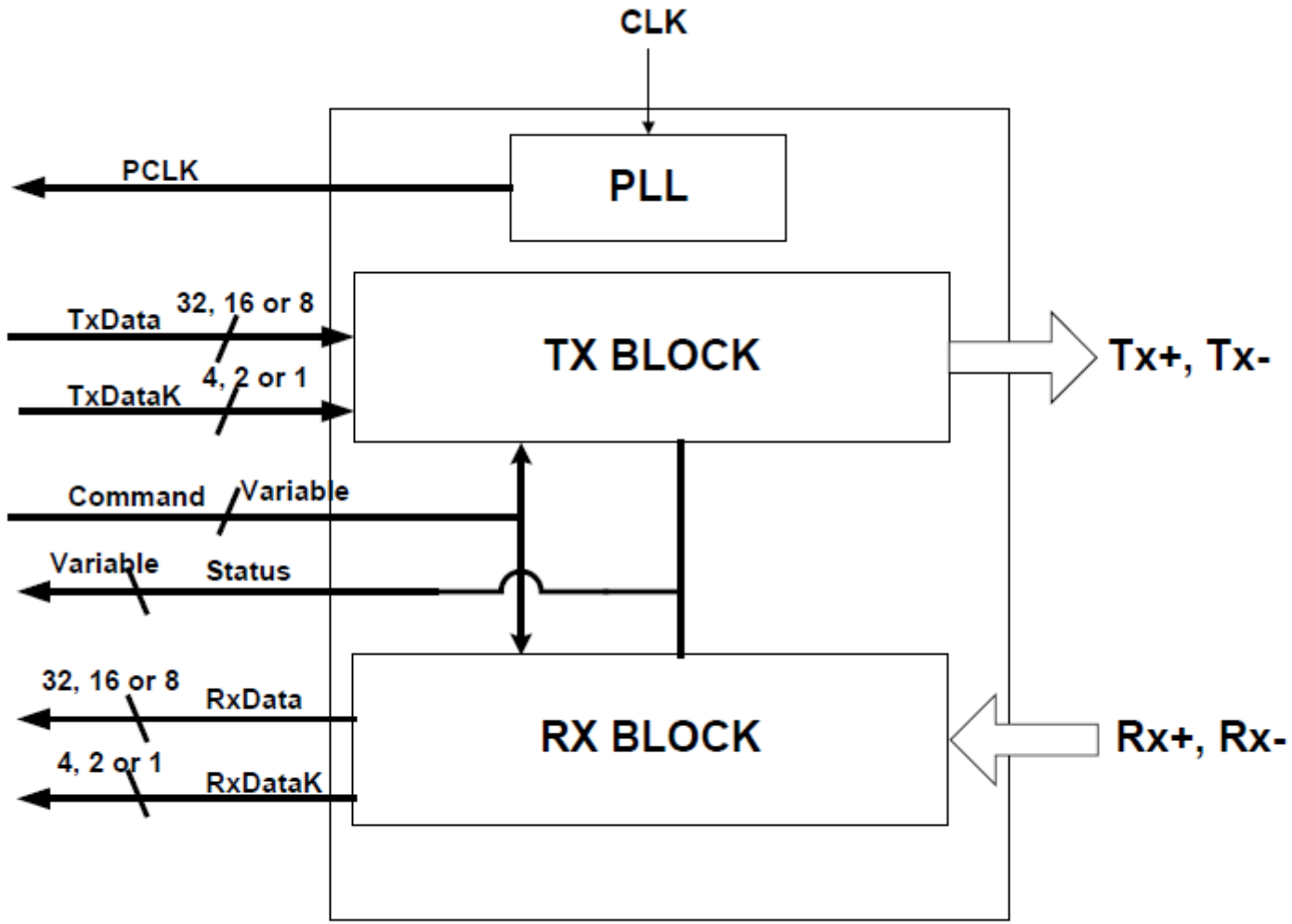



**Figure 4-1: PHY Functional Block Diagram**

## 4.1 Transmitter Block Diagram (2.5 and 5.0 GT/s)

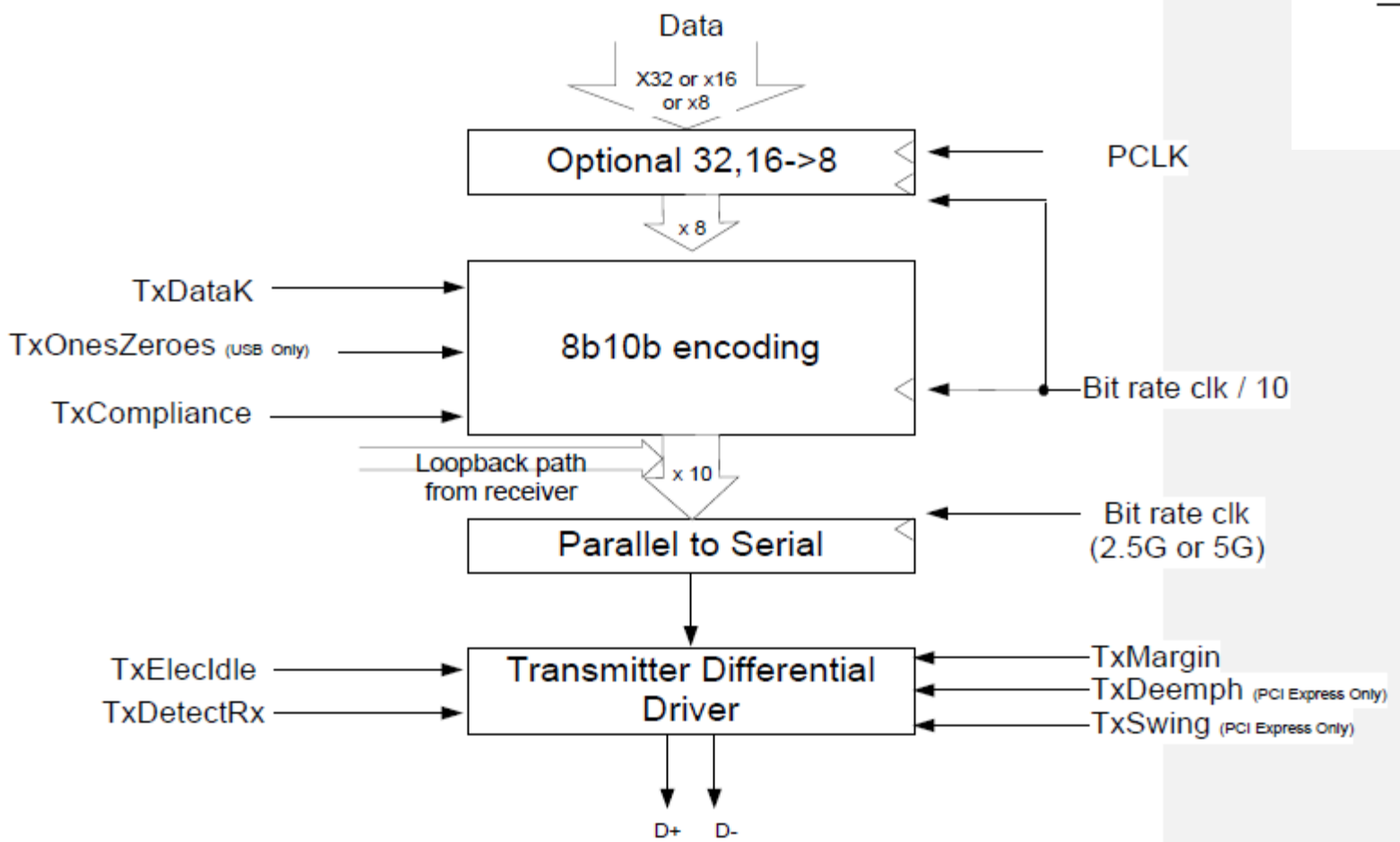



**Figure 4-2: Transmitter Block Diagram**

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## 4.5 Clocking

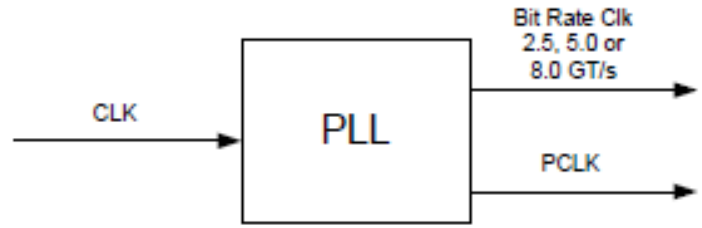


**Figure 4-6: Clocking and Power Block Diagram**

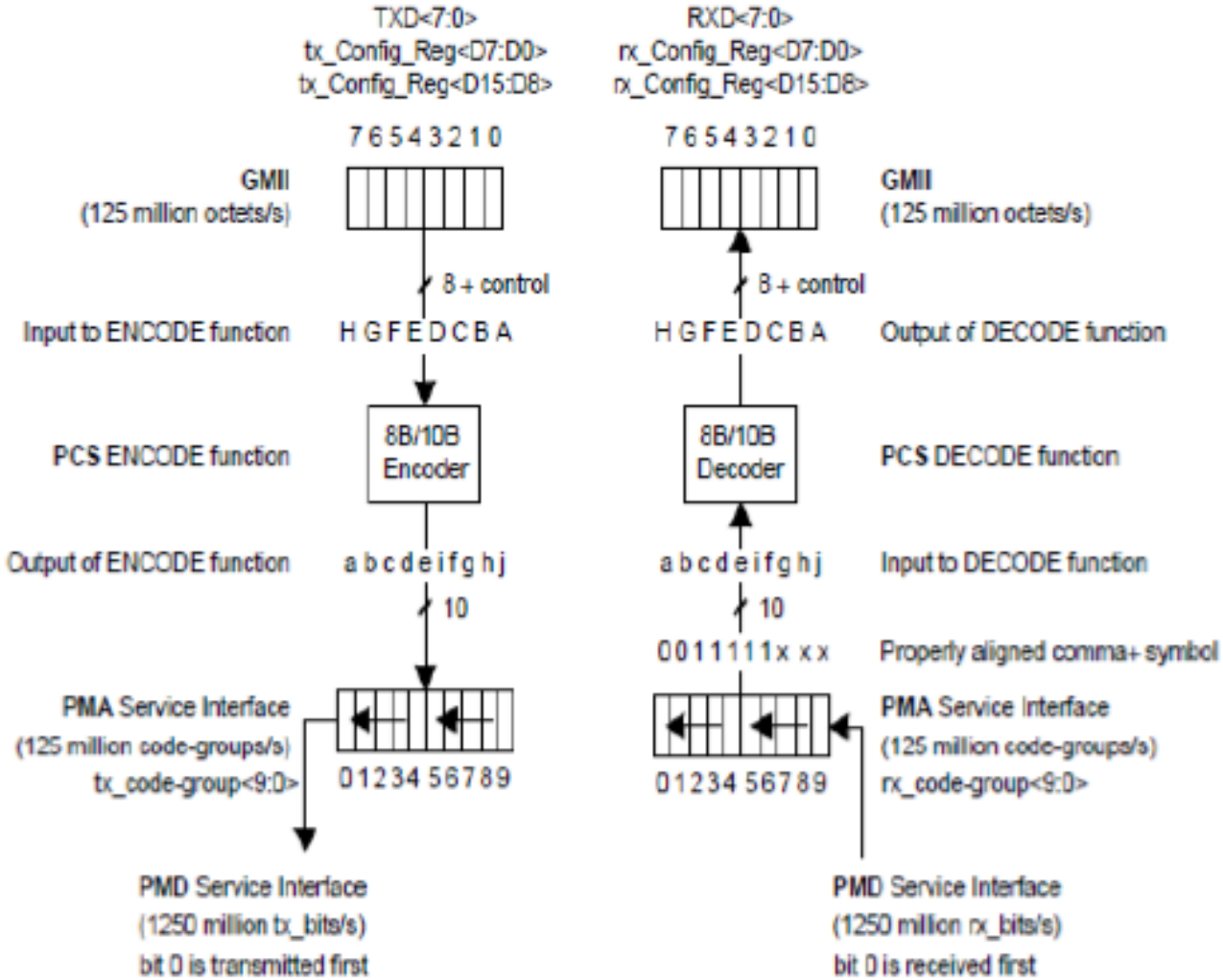


Figure 3.PCS reference diagram

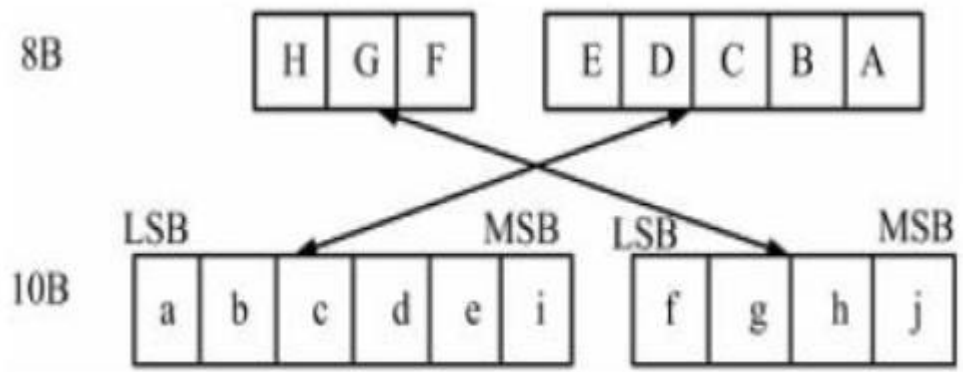


Figure 1. 8B/10B encoding relationship

# Algoritmo de codificación 8b/10b

**RC23408 (W0411-032) November 3, 2004**
**Electrical Engineering**

# IBM Research Report

## 8B/10B Encoding and Decoding for High Speed Applications

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Table B-2: 8b/10b Special Character Symbol Codes

| Data Byte Name | Data Byte Value | Bits HGF EDCBA | Current RD - abcdei fghj | Current RD + abcdei fghj |
|---|---|---|---|---|
| K28.0 | 1C | 000 11100 | 001111 0100 | 110000 1011 |
| K28.1 | 3C | 001 11100 | 001111 1001 | 110000 0110 |
| K28.2 | 5C | 010 11100 | 001111 0101 | 110000 1010 |
| K28.3 | 7C | 011 11100 | 001111 0011 | 110000 1100 |
| K28.4 | 9C | 100 11100 | 001111 0010 | 110000 1101 |
| K28.5 | BC | 101 11100 | 001111 1010 | 110000 0101 |
| K28.6 | DC | 110 11100 | 001111 0110 | 110000 1001 |
| K28.7 | FC | 111 11100 | 001111 1000 | 110000 0111 |
| K23.7 | F7 | 111 10111 | 111010 1000 | 000101 0111 |
| K27.7 | FB | 111 11011 | 110110 1000 | 001001 0111 |
| K29.7 | FD | 111 11101 | 101110 1000 | 010001 0111 |
| K30.7 | FE | 111 11110 | 011110 1000 | 100001 0111 |

TxDataK = 1

Table B-1: 8b/10b Data Symbol Codes

| Data Byte Name | Data Byte Value | Bits HGF EDCBA | Current RD - abcdei fghj | Current RD + abcdei fghj |
|---|---|---|---|---|
| D0.0 | 00 | 000 00000 | 100111 0100 | 011000 1011 |
| D1.0 | 01 | 000 00001 | 011101 0100 | 100010 1011 |
| D2.0 | 02 | 000 00010 | 101101 0100 | 010010 1011 |
| D3.0 | 03 | 000 00011 | 110001 1011 | 110001 0100 |

TxDataK = 0

...

# Símbolos de control

*Table 11-5: Control Character Encoding and Definition*

| Character Name | 8b Name | 10b (CRD-) | 10b (CRD+) | Description |
|---|---|---|---|---|
| COM | K28.5 (BCh) | 001111 1010 | 110000 0101 | First character in any Ordered-Set. Detected by receiver and used to achieve symbol lock during TS1/TS2 Ordered-Set reception at receiver |
| PAD | K23.7 (F7h) | 111010 1000 | 000101 0111 | Packet Padding character |
| SKP | K28.0 (1Ch) | 001111 0100 | 110000 1011 | Used in SKIP Ordered-Set. This Ordered-Set is used for Clock Tolerance Compensation |
| STP | K27.7 (FBh) | 110110 1000 | 001001 0111 | Start of TLP character |
| SDP | K28.2 (5Ch) | 001111 0101 | 110000 1010 | Start of DLLP character |
| END | K29.7 (FDh) | 101110 1000 | 010001 0111 | End of Good Packet character |
| EDB | K30.7 (FEh) | 011110 1000 | 100001 0111 | Character used to mark the end of a 'nullified' TLP. |

# TxCompliance (8b/10b)

Causa un retraso de 4 símbolos

| **Symbol** | K28.5 | D21.5 | K28.5 | D10.2 |
|---|---|---|---|---|
| **Current Disparity** | 0 | 1 | 1 | 0 |
| **Pattern** | 0011111010 | 1010101010 | 1100000101 | 0101010101 |

# TxOnesZeros

| | | | |
|---|---|---|---|
| TxOnesZeros | Input | High | USB SuperSpeed Mode: Used only when transmitting USB SuperSpeed compliance patterns CP7 or CP8. Causes the transmitter to transmit an alternating sequence of 50-250 ones and 50-250 zeros – regardless of the state of the TxData interface. Implementation of this signal is only required for PHYs that support USB SuperSpeed mode. |

### 4.3 Receiver Block Diagram (2.5 and 5.0 GT/s)

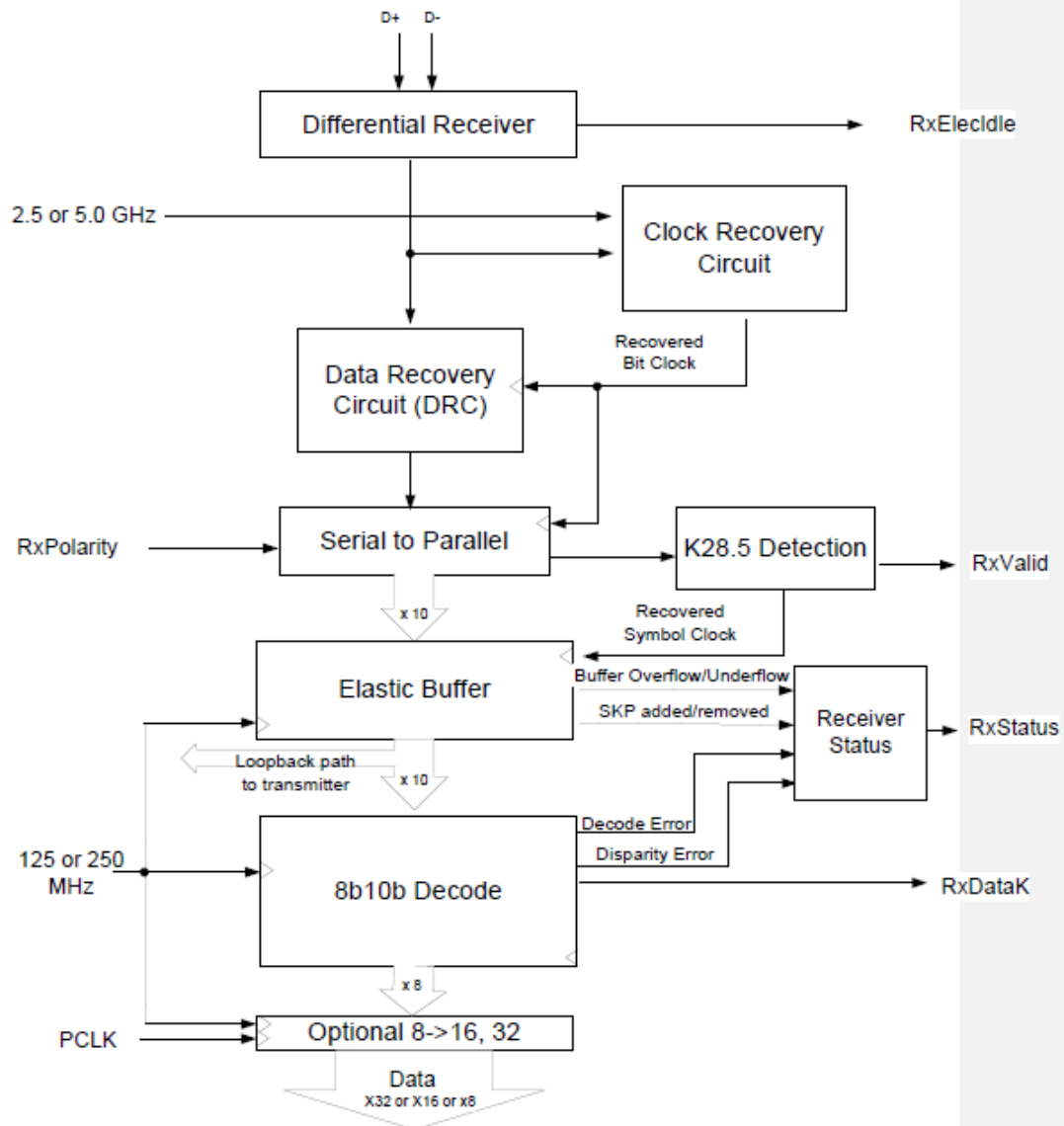
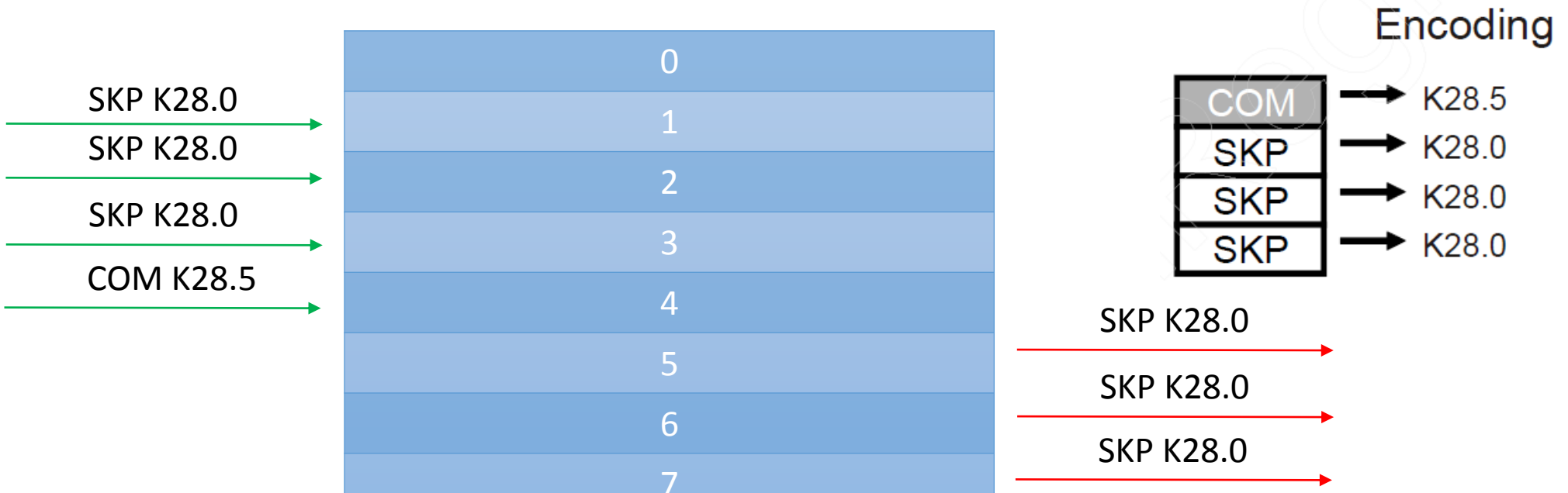



**Figure 4-4: Receiver Block Diagram**

Format

# Elastic buffer

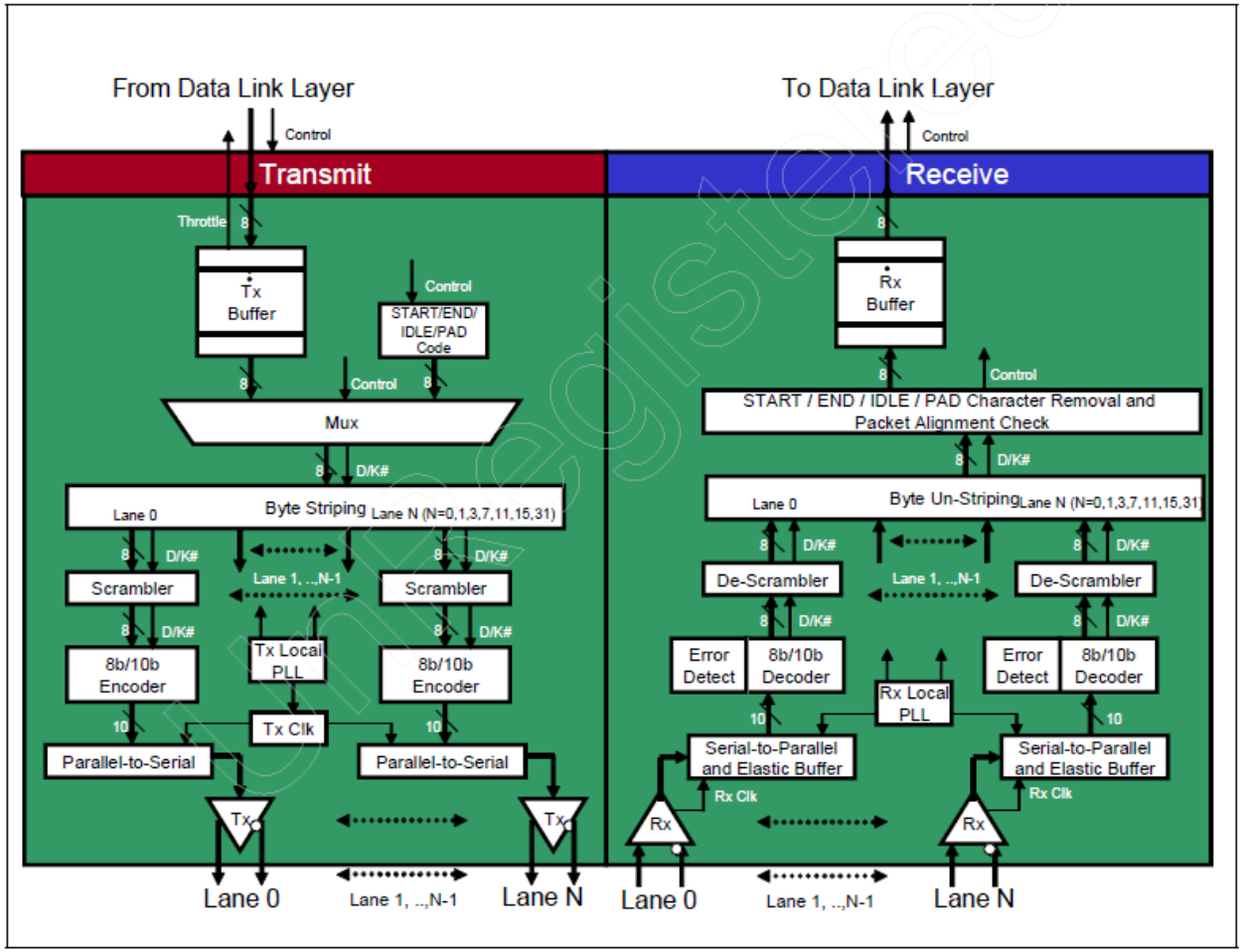
*Figure 11-19: SKIP Ordered-Set*




| | | | | |
|---|---|---|---|---|
| COM | K28.5 (BCh) | 001111 1010 | 110000 0101 | First character in any Ordered-Set. Detected by receiver and used to achieve symbol lock during TS1/TS2 Ordered-Set reception at receiver |
| SKP | K28.0 (1Ch) | 001111 0100 | 110000 1011 | Used in SKIP Ordered-Set. This Ordered-Set is used for Clock Tolerance Compensation |

# Detalles de la capa física en TX y RX

*Figure 11-3: Physical Layer Details*



# Lógica RX

*Figure 11-21: Receiver Logic's Front End Per Lane*