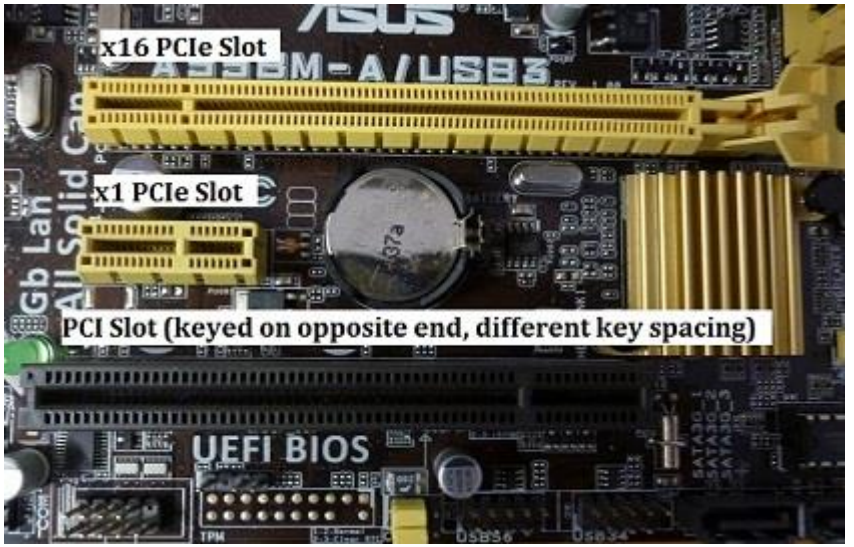
Arquitectura PCIe

Prof. Jorge Soto

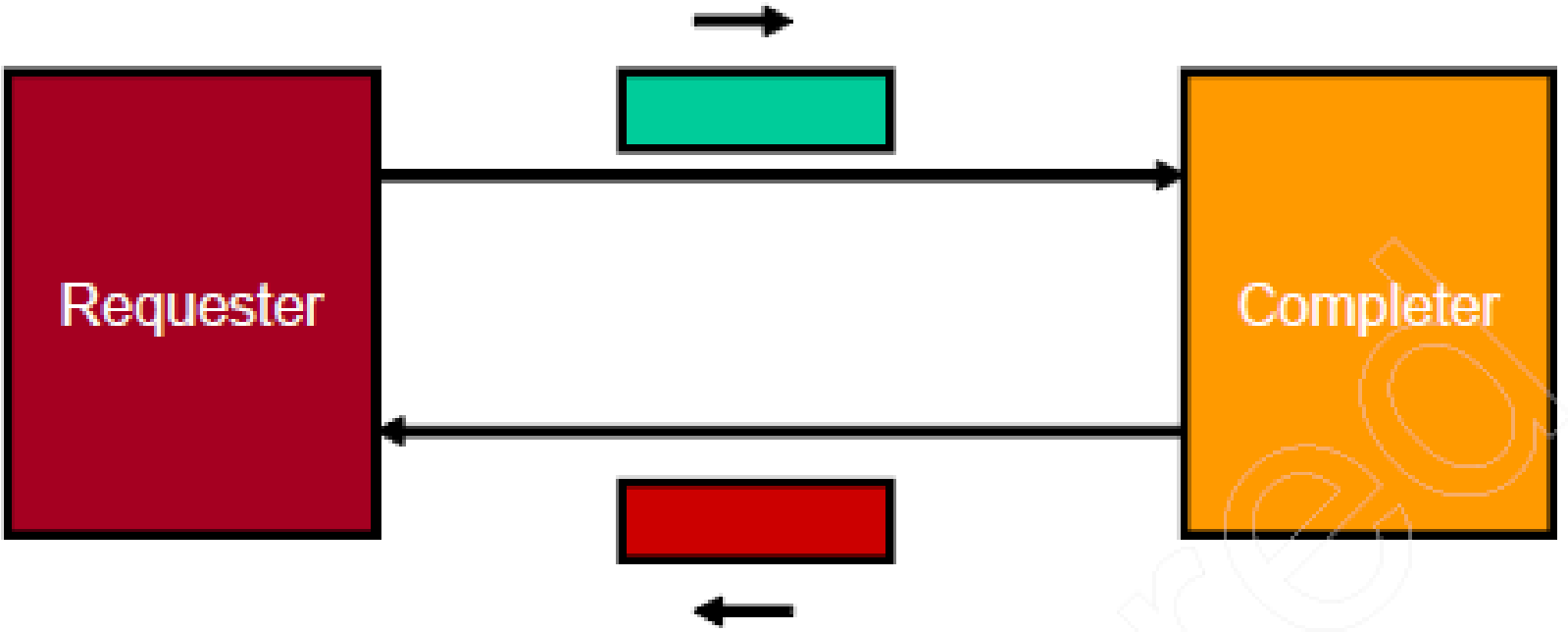
IE-0523 Circuitos Digitales II

Peripheral Component Interface



https://www.passmark.com/support/pcie-test-card-faq.htm
https://www.bhphotovideo.com/c/product/884564-REG/MOTU_9200_PCIe_424_Card_Card.html

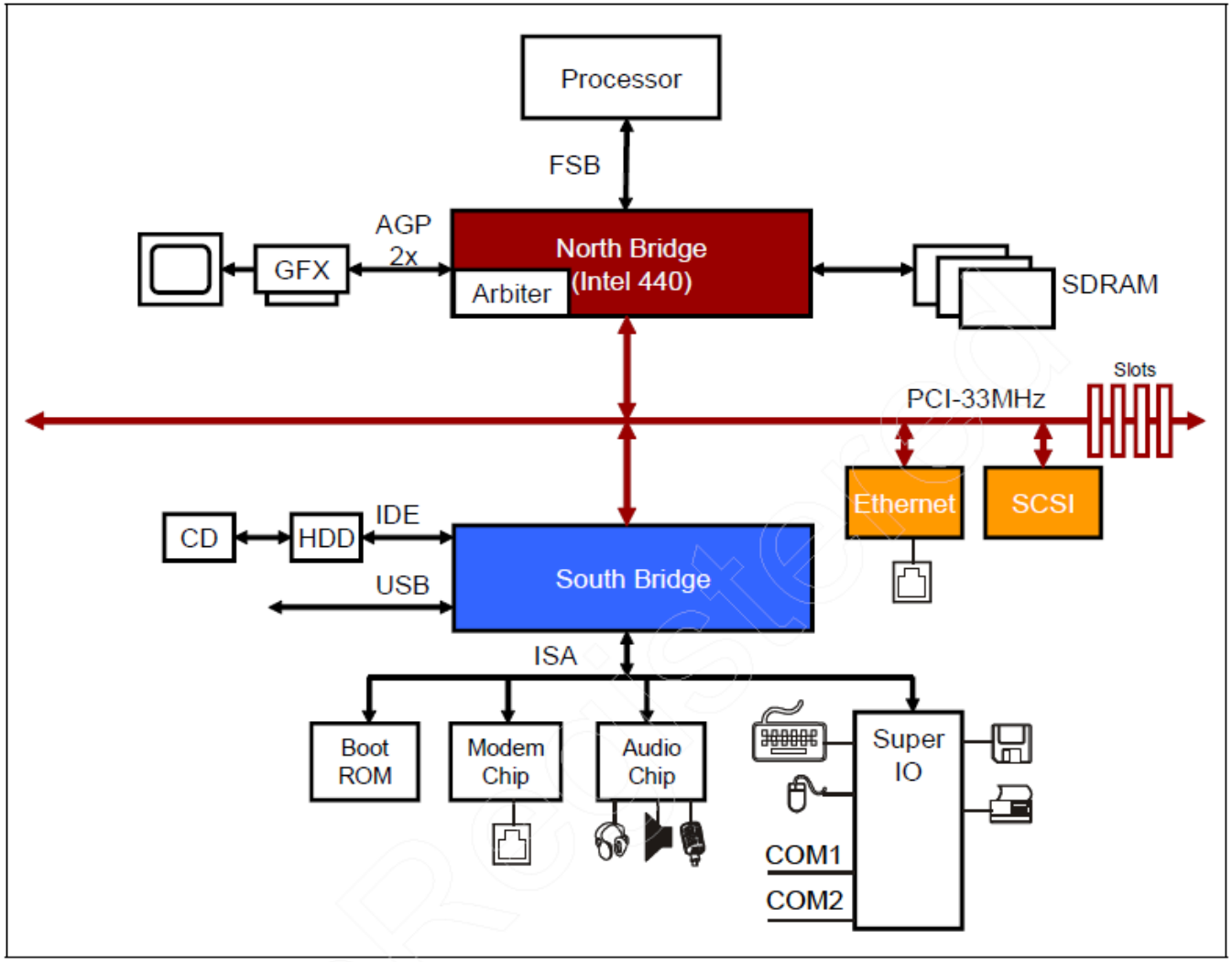
Enlace PCIe*



* PCI-SIG; PCI Express® Base Specification Revision 3.0; November 2010

Ejemplo de topología*

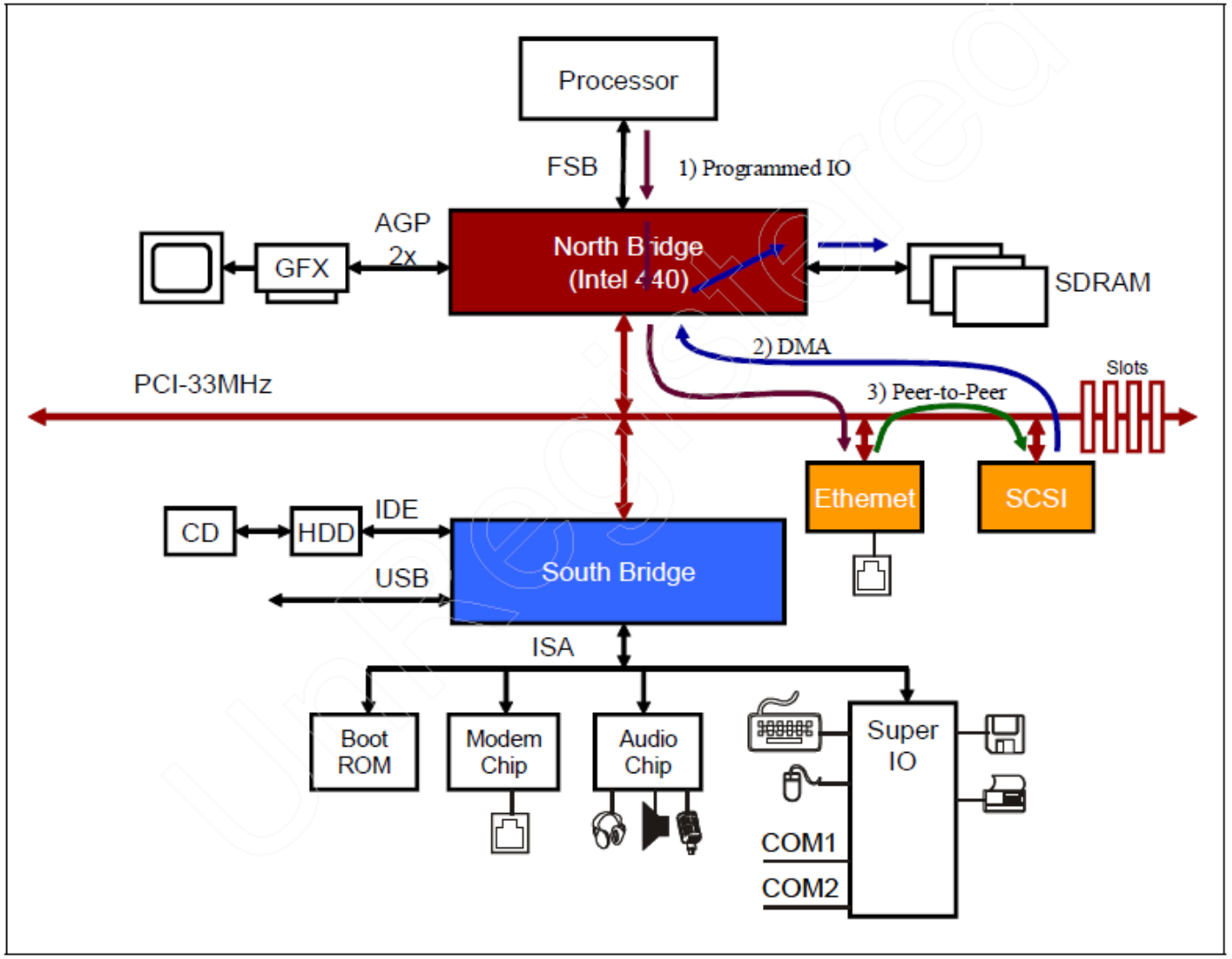
Figure 1-2: 33 MHz PCI Bus Based Platform



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Transacciones en PCI*

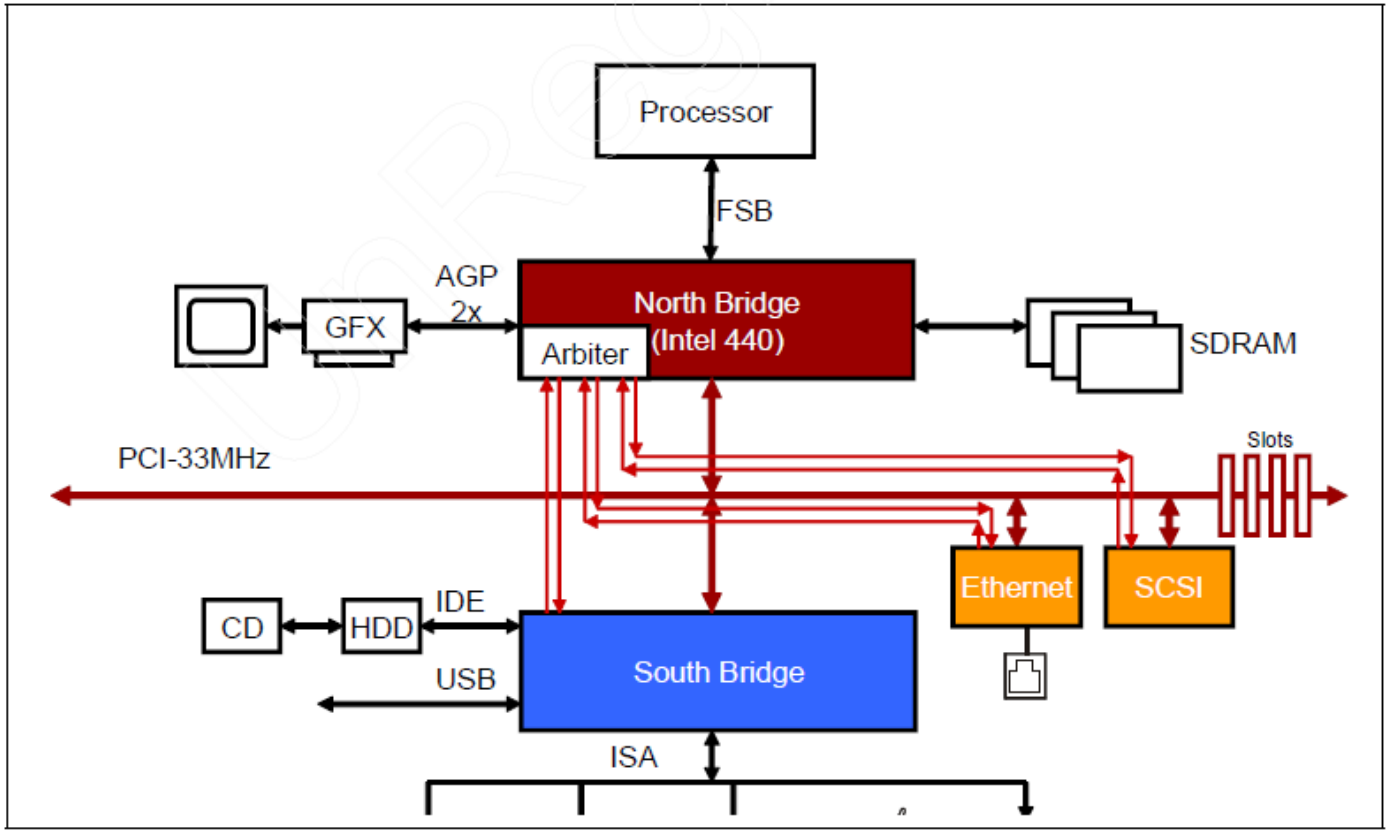
Figure 1-5: PCI Transaction Model



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Arbitraje en PCI*

Figure 1-6: PCI Bus Arbitration



↕ Arbitraje utilizando señales REQ(↑) y GNT(↓)

* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

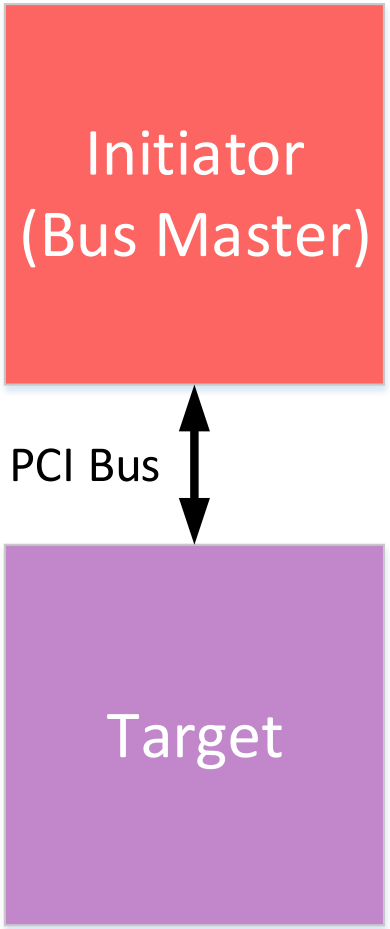
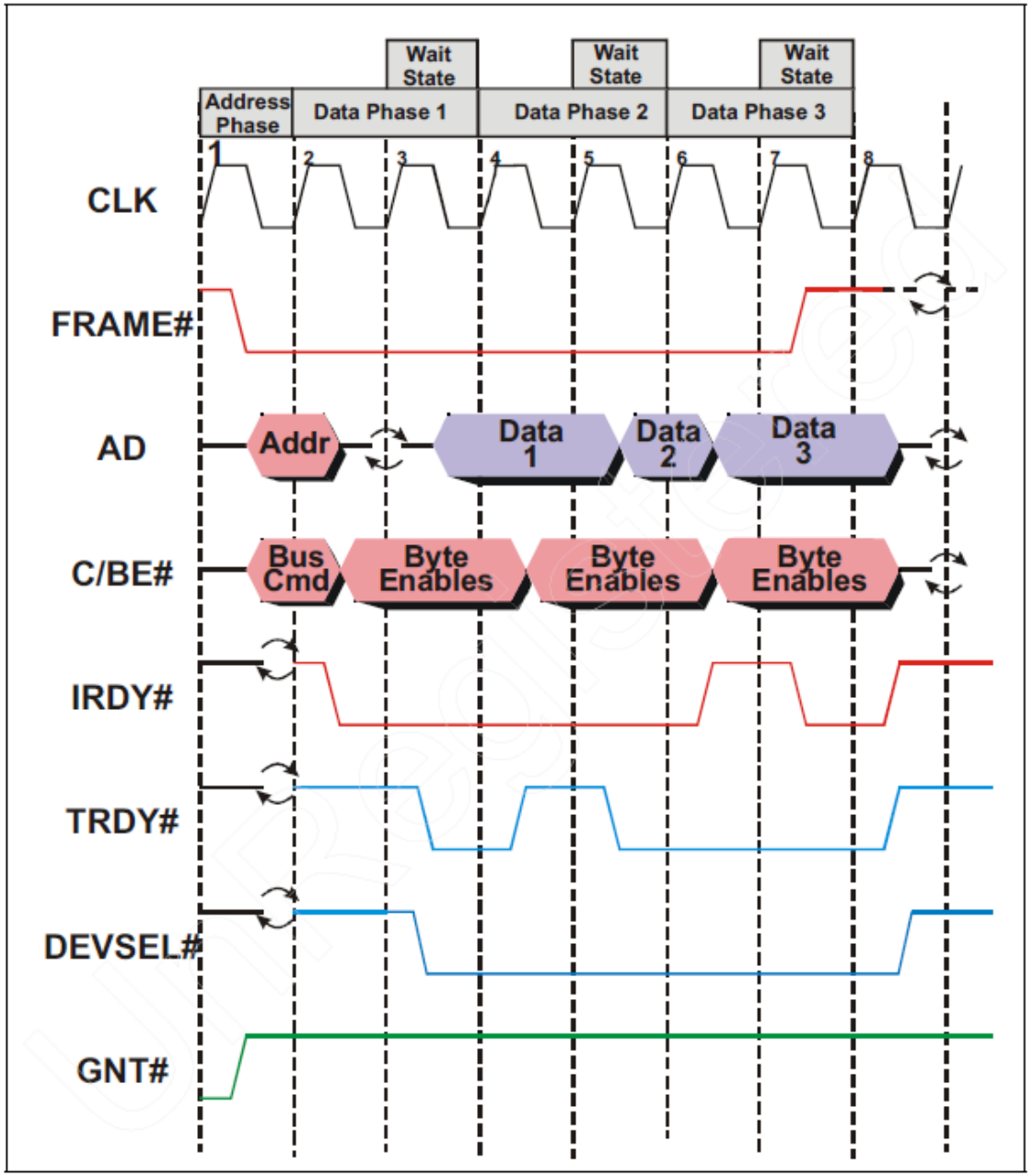


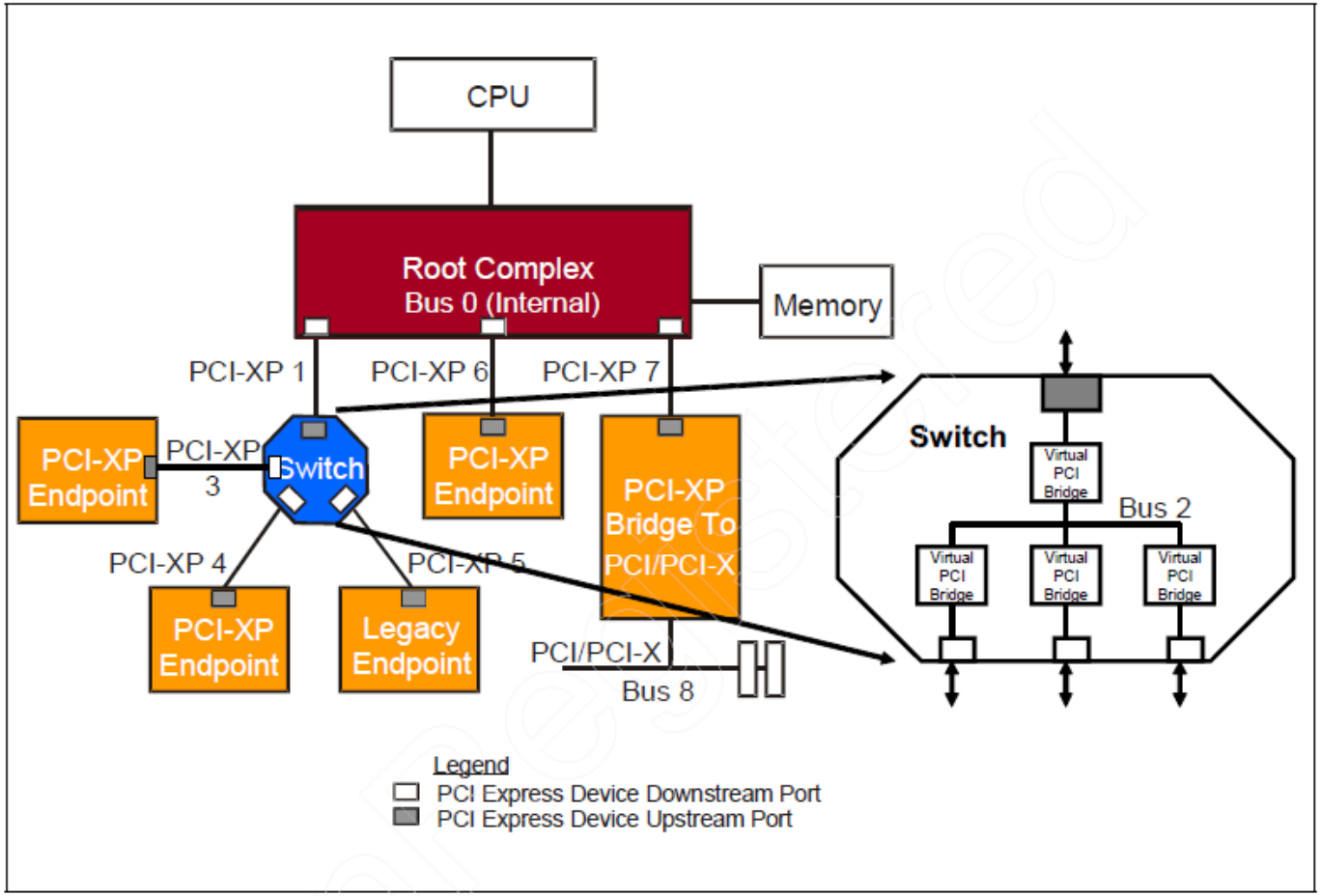
Figure 1-3: Typical PCI Burst Memory Read Bus Cycle



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Ejemplo topología PCIE

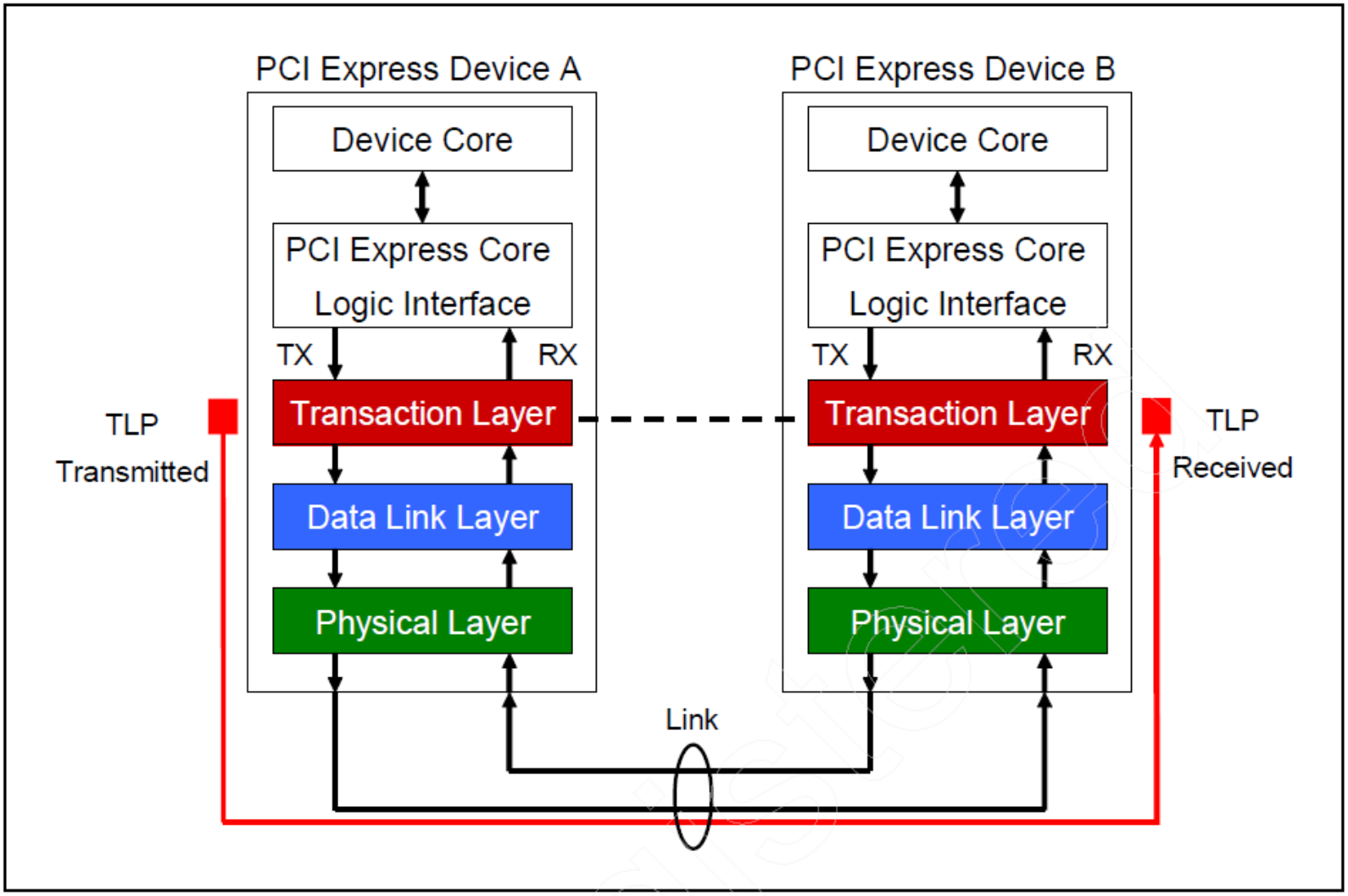
Figure 1-22: PCI Express Topology



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Diagrama de capas PCIE

Figure 2-11: TLP Origin and Destination



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Núcleo del dispositivo / Capa de Software (Device Core / Software Layer)

- Núcleo o cerebro del dispositivo.
- No está presente en el estándar ya que está por encima de la capa de transacción.
- Es el destino o la fuente de peticiones, con información como: tipo de transacción, dirección, cantidad de datos, entre otros.
- Comunicación en RX y TX con la capa de transacción.

Transacciones TLP

- Tipos:
  - Memoria
  - Entrada y salida (IO)
  - Configuración
  - Mensajes
- Transacción: combinación de paquete de solicitud (Request) y terminación (Completion)
- Transacción tipo “Non-posted”: Espera respuesta
- Transacción tipo “Posted”: No espera respuesta (Se revisa con protocolo Ack/Nak en DLL)

Tipos de peticiones

Table 2-1: PCI Express Non-Posted and Posted Transactions

Transaction Type	Non-Posted or Posted
Memory Read	Non-Posted
Memory Write	Posted
Memory Read Lock	Non-Posted
IO Read	Non-Posted
IO Write	Non-Posted
Configuration Read (Type 0 and Type 1)	Non-Posted
Configuration Write (Type 0 and Type 1)	Non-Posted
Message	Posted

* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Tipos de transacciones TLP

Table 2-2: PCI Express TLP Packet Types

TLP Packet Types	Abbreviated Name
Memory Read Request	MRd
Memory Read Request - Locked access	MRdLk
Memory Write Request	MWr
IO Read	IORd
IO Write	IOWr
Configuration Read (Type 0 and Type 1)	CfgRd0, CfgRd1
Configuration Write (Type 0 and Type 1)	CfgWr0, CfgWr1
Message Request without Data	Msg
Message Request with Data	MsgD
Completion without Data	Cpl
Completion with Data	CplD
Completion without Data - associated with Locked Memory Read Requests	CplLk
Completion with Data - associated with Locked Memory Read Requests	CplDLk

* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Capa de Enlace de Datos (Data Link Layer)

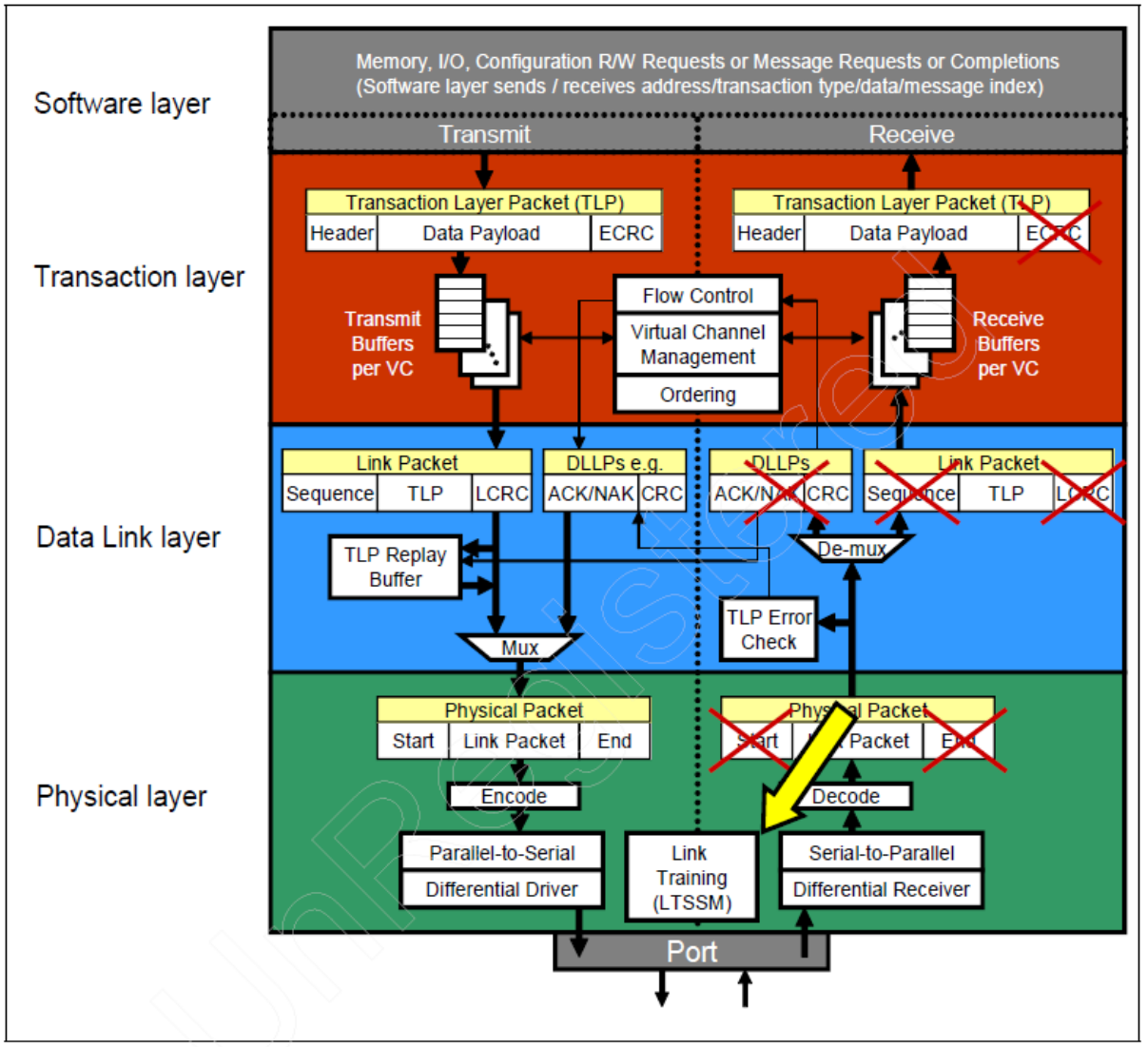
- Transmision (codificación) y recepción (decodificación) de paquetes DLLP.
- Detección y corrección de errores mediante el protocolo Ack/Nak.

Capa Física (PHY)
(Physical Layer)

- Creación y recepción de paquetes tipo “Ordered-Set”.
- Transmisión y recepción de paquetes TLP y DLLP.
- Contiene la máquina de estados de entrenamiento y estado del enlace (LTSSM).

Diagrama de capas PCIE

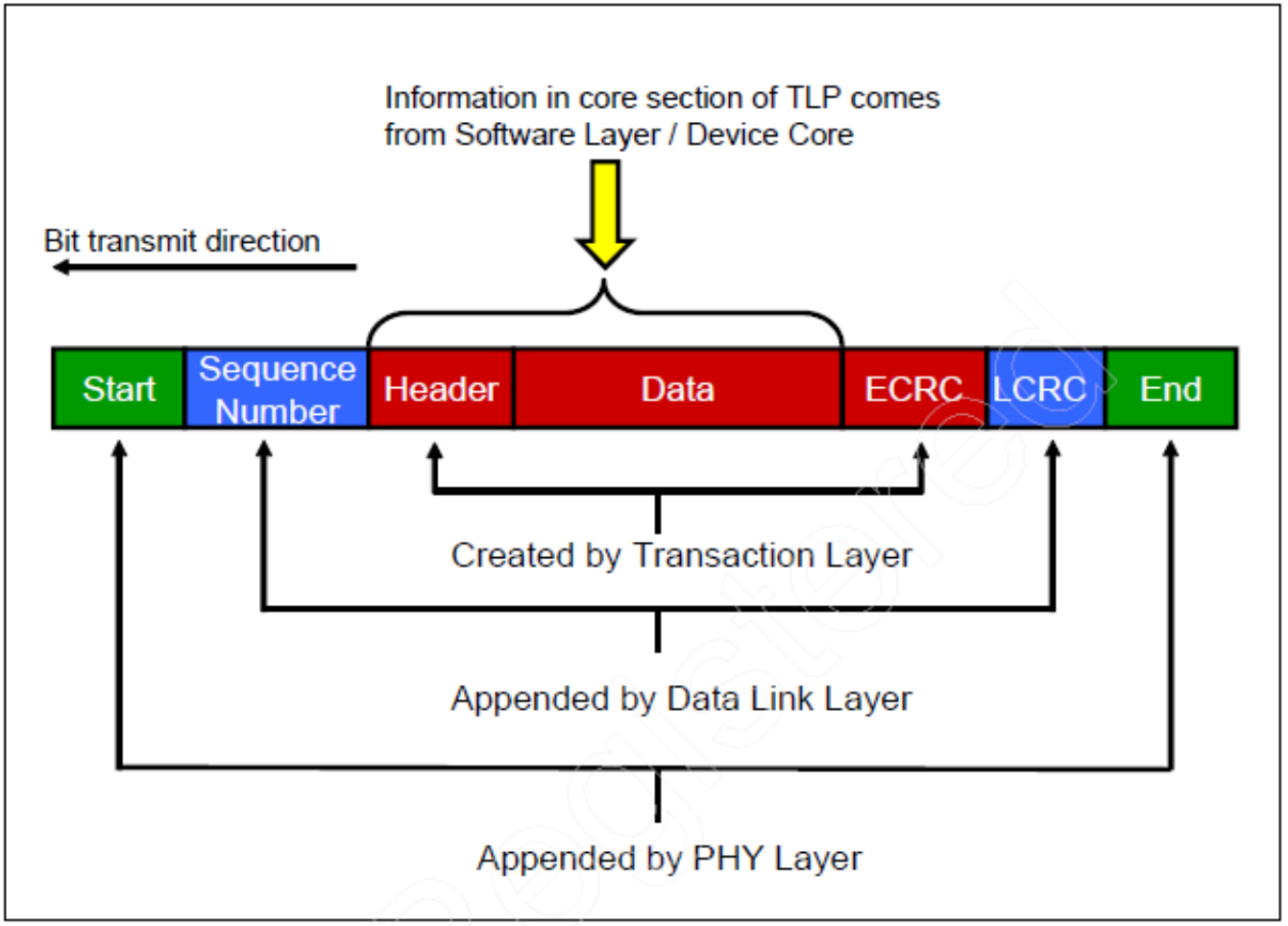
Figure 14-1: Link Training and Status State Machine Location



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Ensablaje de transacción TLP

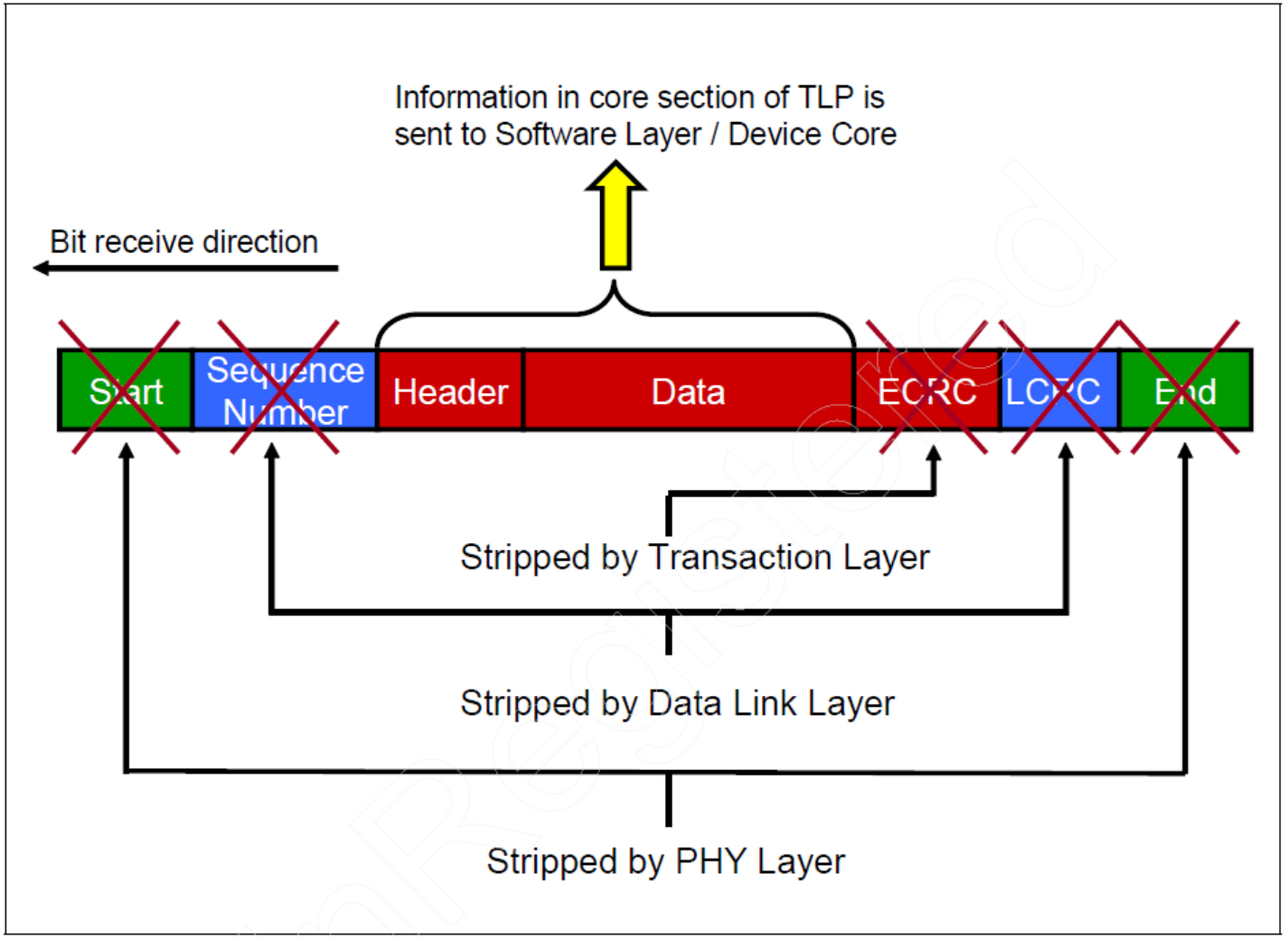
Figure 2-12: TLP Assembly



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Desensamblaje de transacción TLP

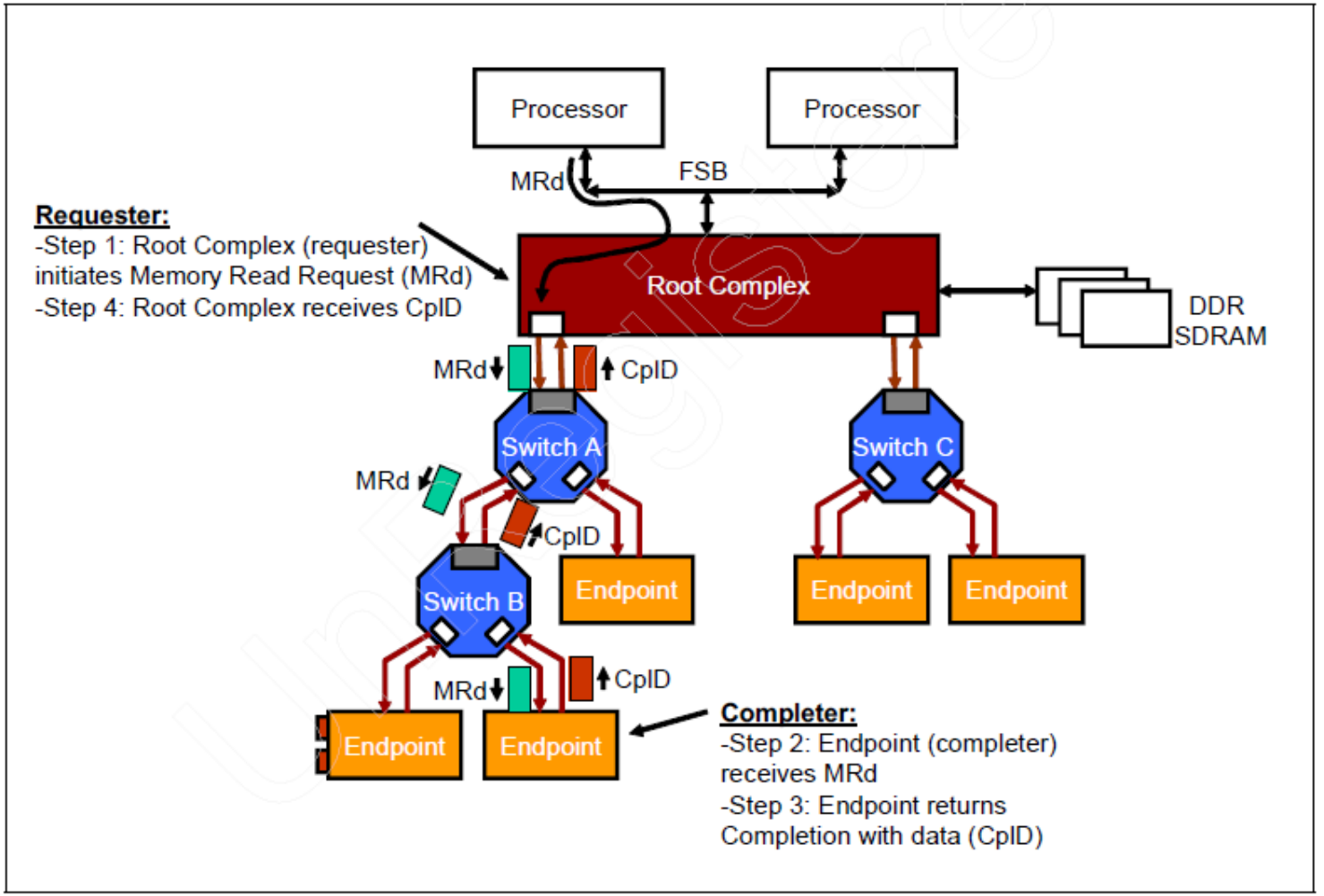
Figure 2-13: TLP Disassembly



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Lectura de Memoria por CPU

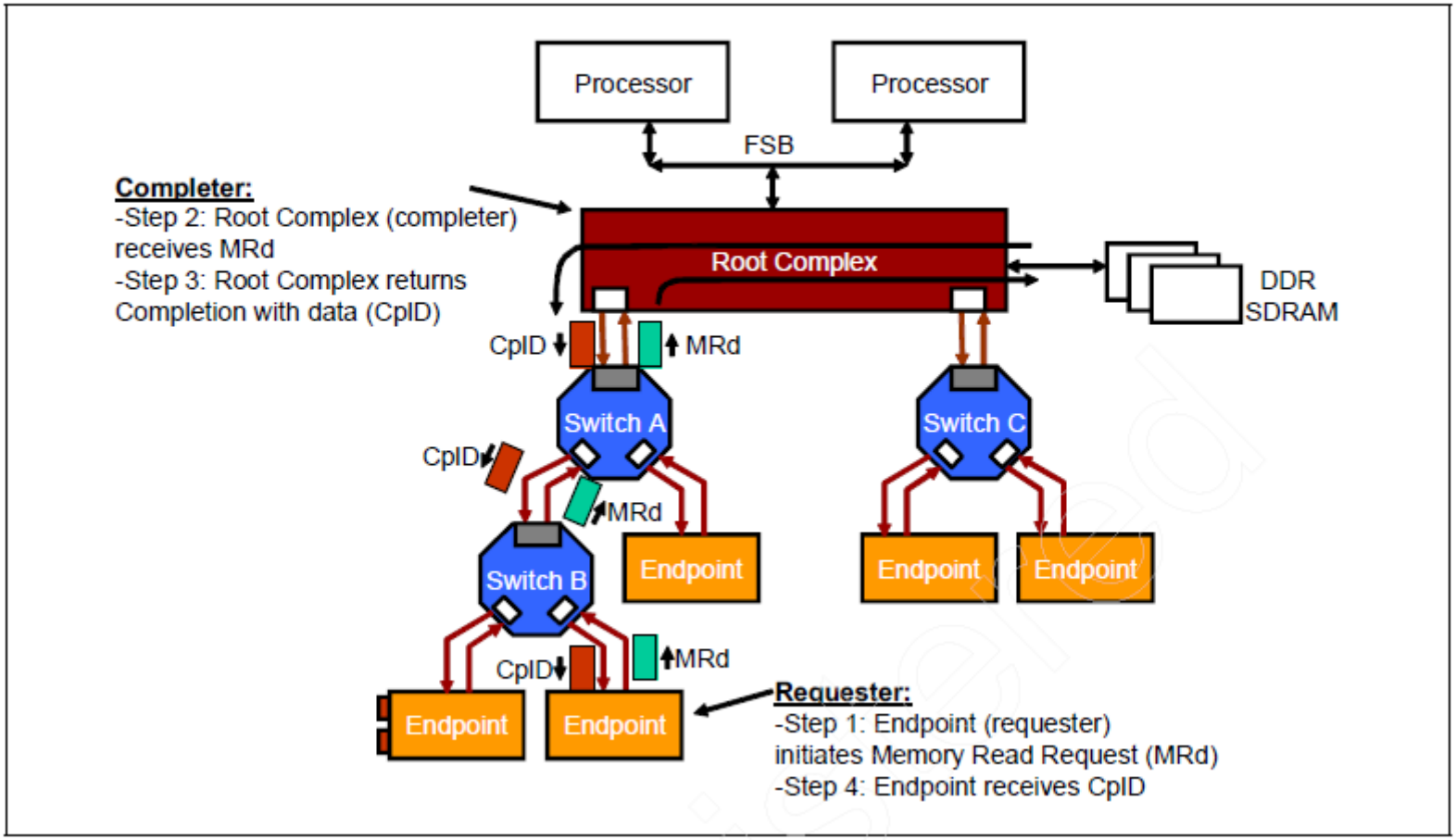
Figure 2-6: Non-Posted Memory Read Originated by CPU and Targeting an Endpoint



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Lectura de Memoria por punto terminal

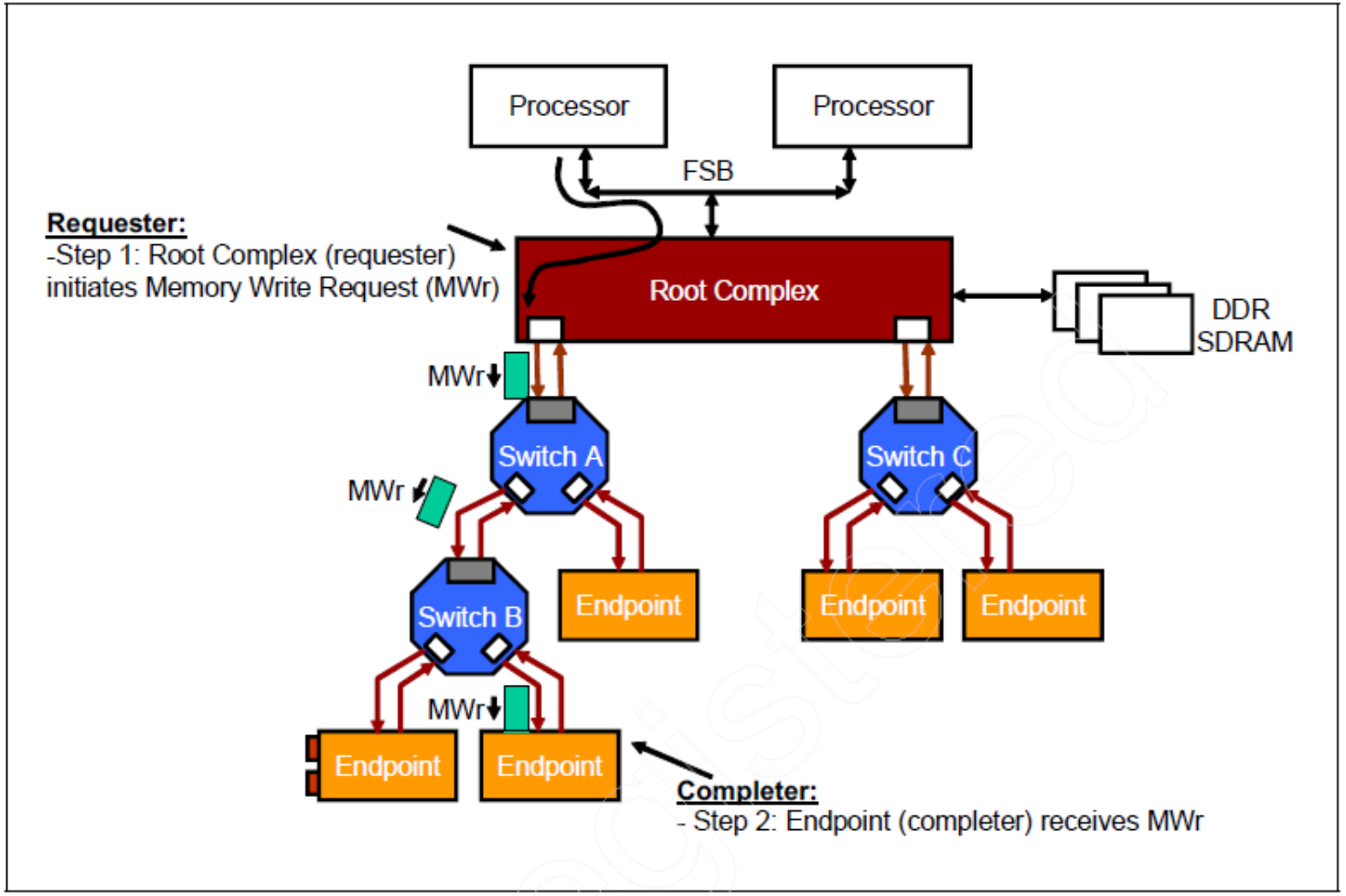
Figure 2-7: Non-Posted Memory Read Originated by Endpoint and Targeting Memory



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Escritura de Memoria por CPU

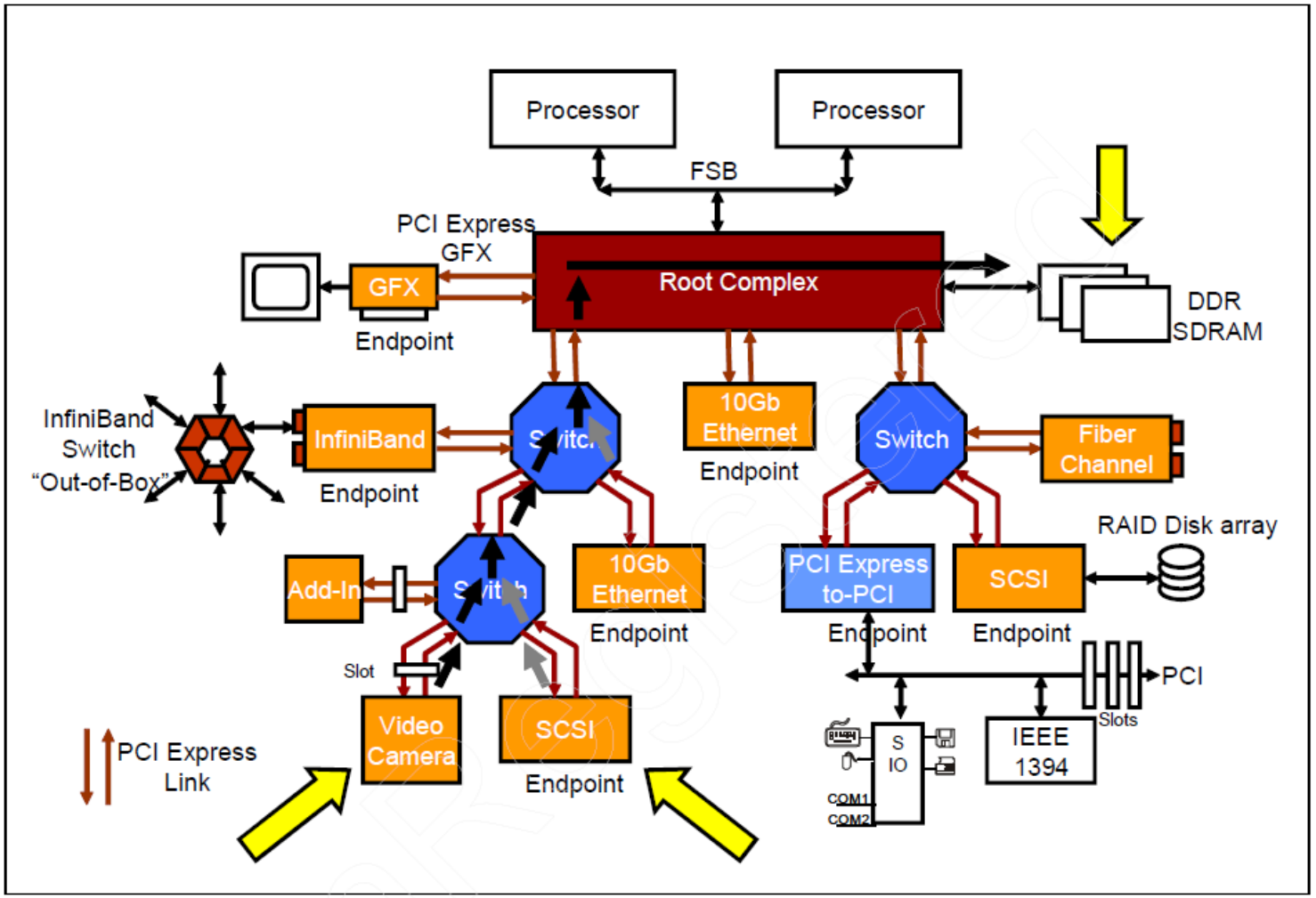
Figure 2-9: Memory Write Transaction Originated by CPU, Targeting Endpoint



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Calidad de Servicio (QoS)

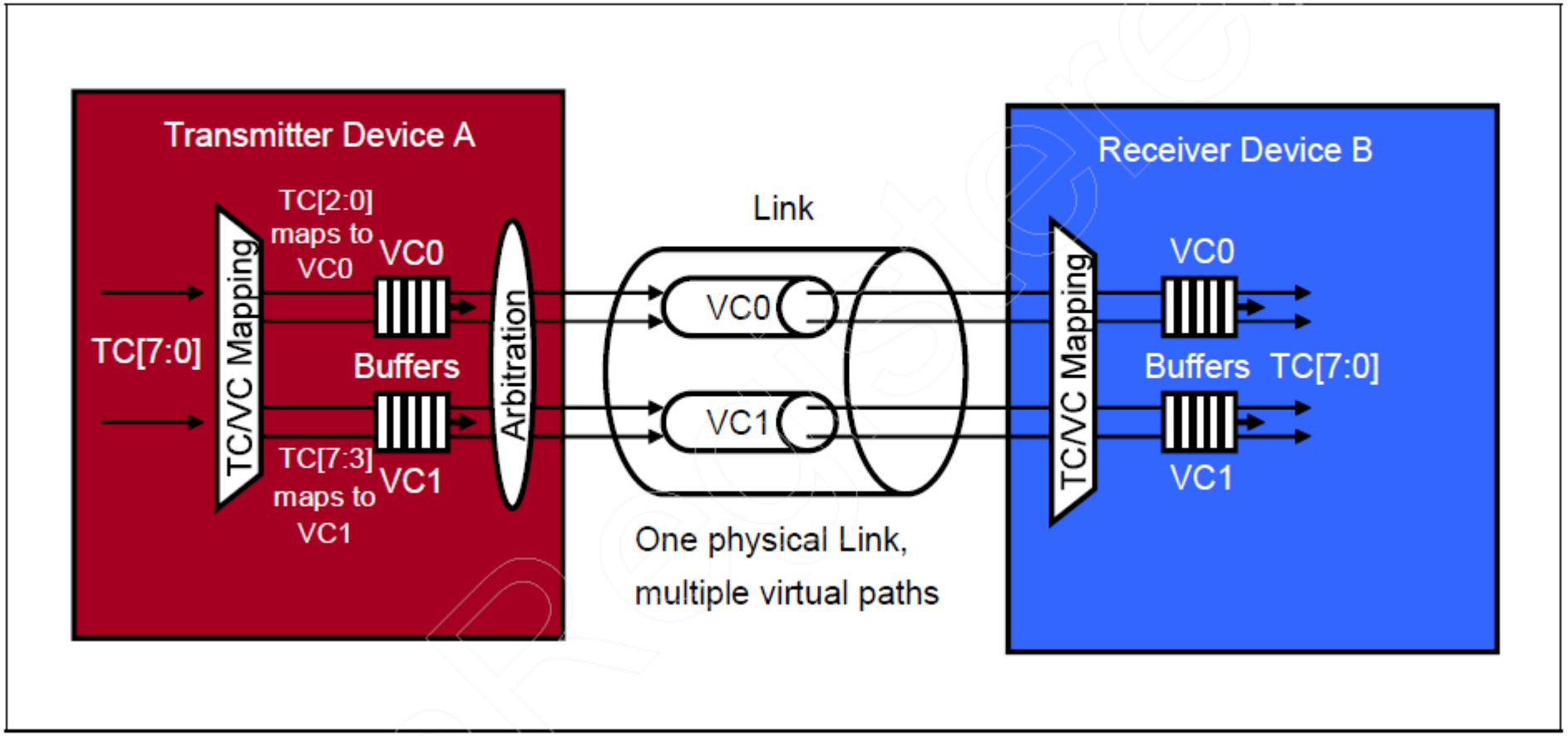
Figure 2-22: Example Showing QoS Capability of PCI Express



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

Clases de Tráfico y Canales Virtuales

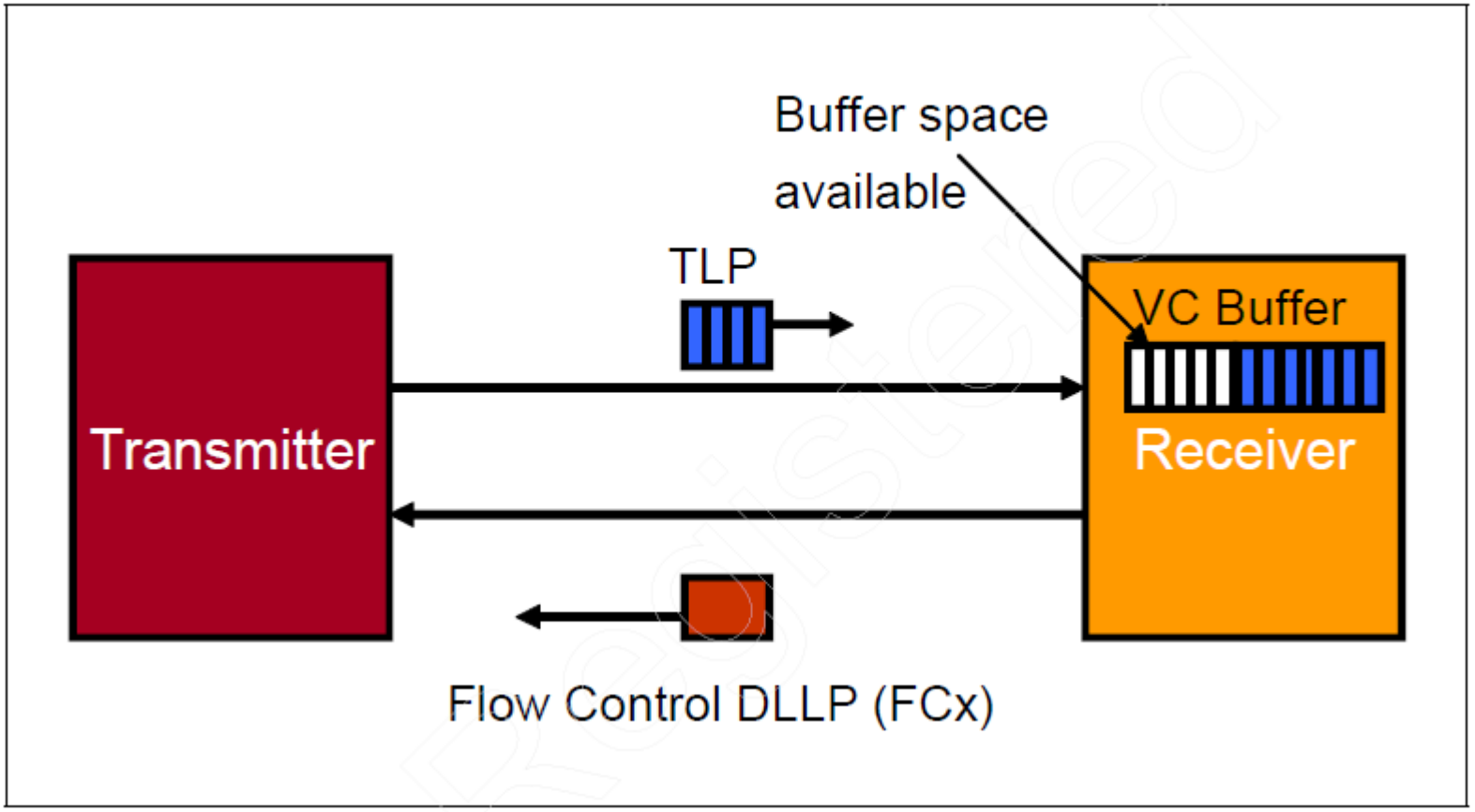
Figure 2-23: TC Numbers and VC Buffers



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

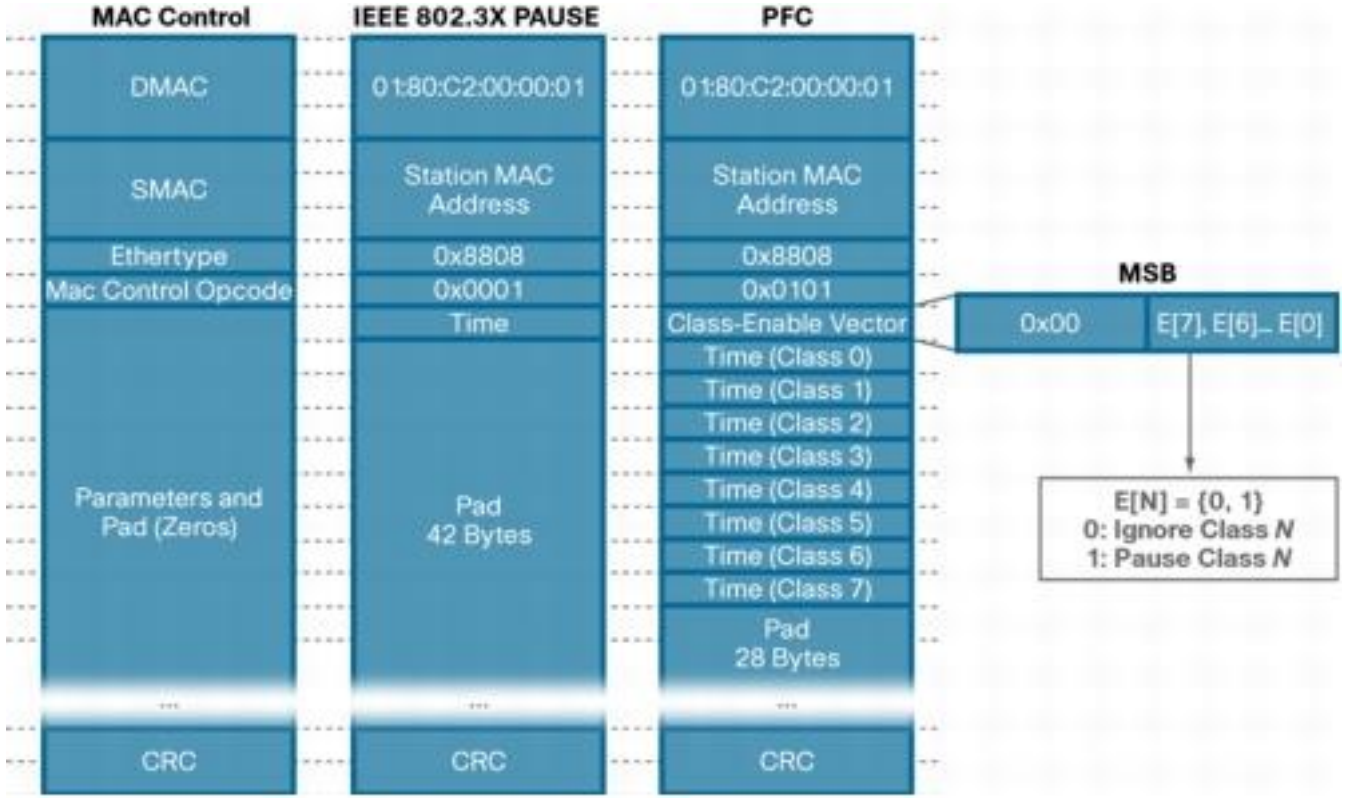
Control de Flujo (FC)

Figure 2-21: Flow Control Process



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

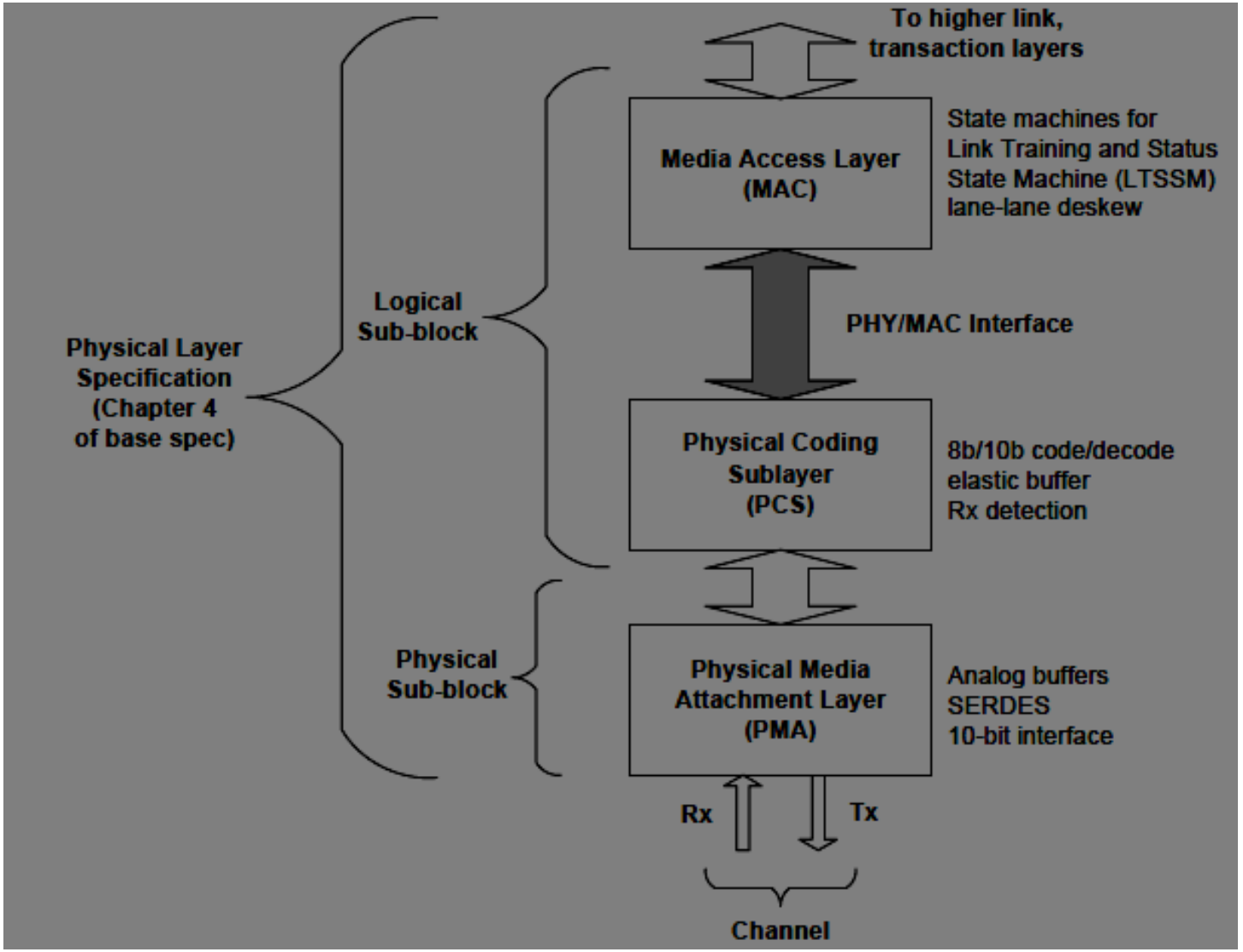
Control de Flujo con Prioridad (PFC) Estándar Ethernet, no PCIe



- IEEE 802.3x PAUSE and PFC Frame Format
- https://www.cisco.com/en/US/prod/collateral/switches/ps9441/ps9670/white_paper_c11-542809_ns783_Networking_Solutions_White_Paper.html

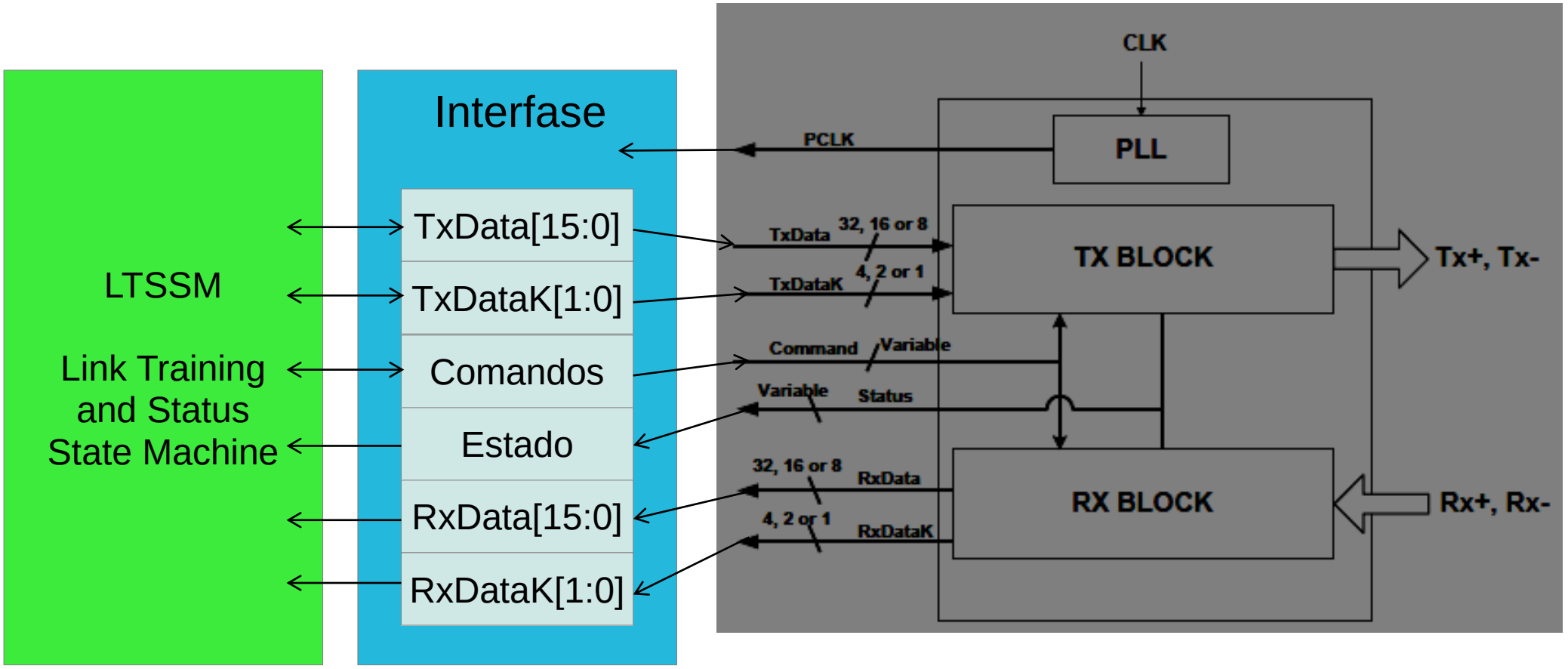
Capa física de PCIe

Capa física de PCIe*



* Intel Corporation; PHY Interface for the PCI Express, SATA, and USB 3.10 Architectures; 2007-2013

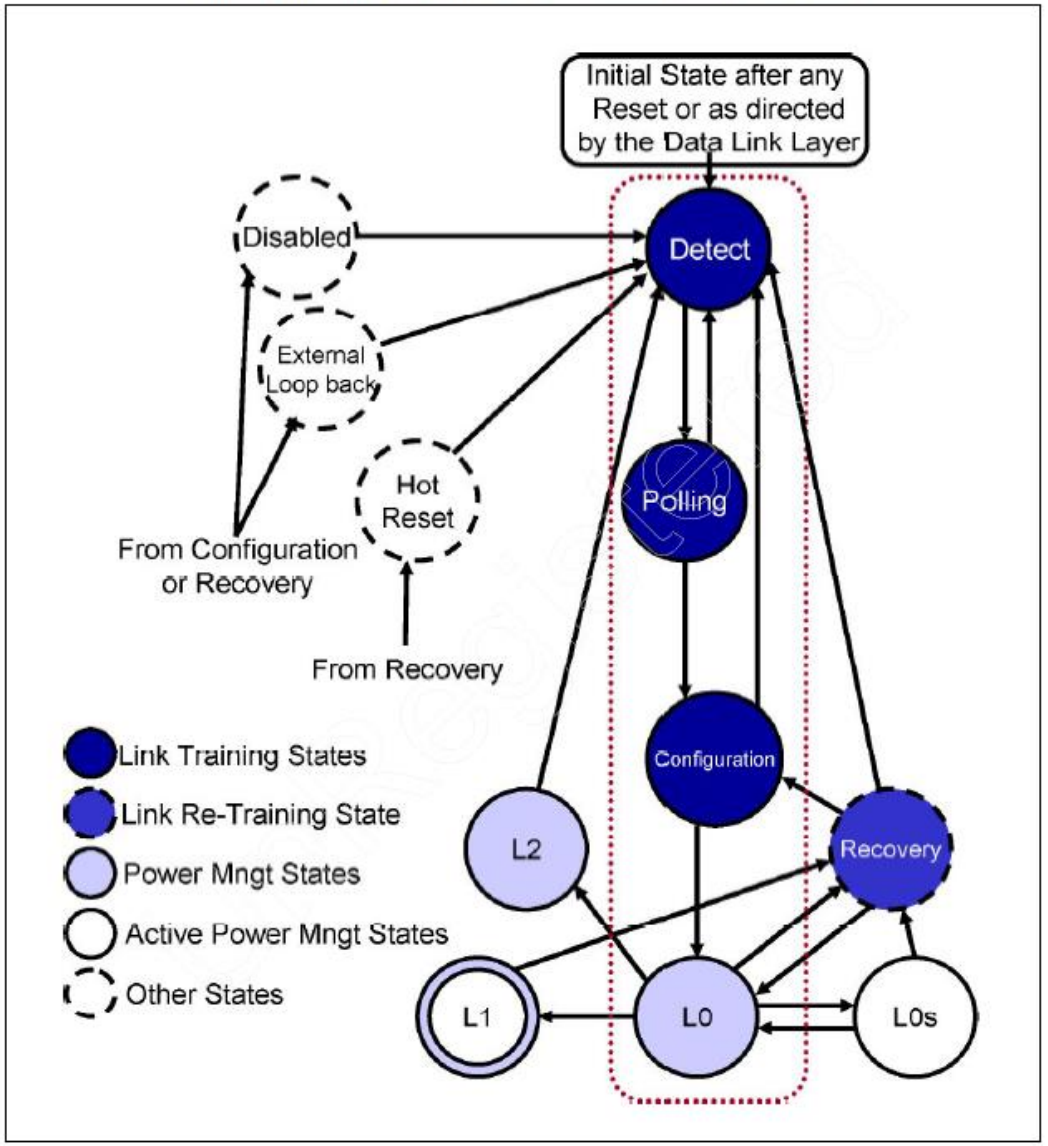
Arquitectura General PCIe



* Intel Corporation; PHY Interface for the PCI Express, SATA, and USB 3.10 Architectures; 2007-2013

Máquina de estados LTSSM*

Figure 14-5: Link Training and Status State Machine (LTSSM)



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008