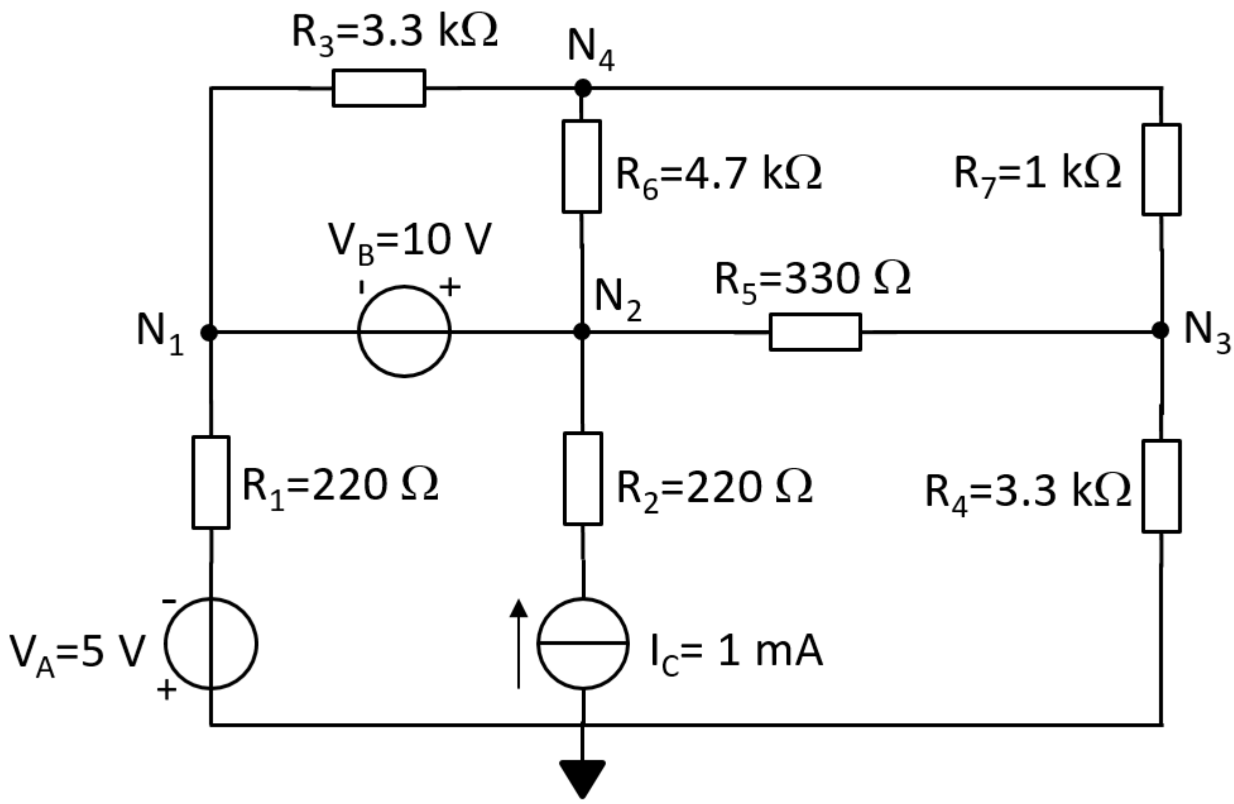
QUCS Lab

Embedded Electronics - IE1206

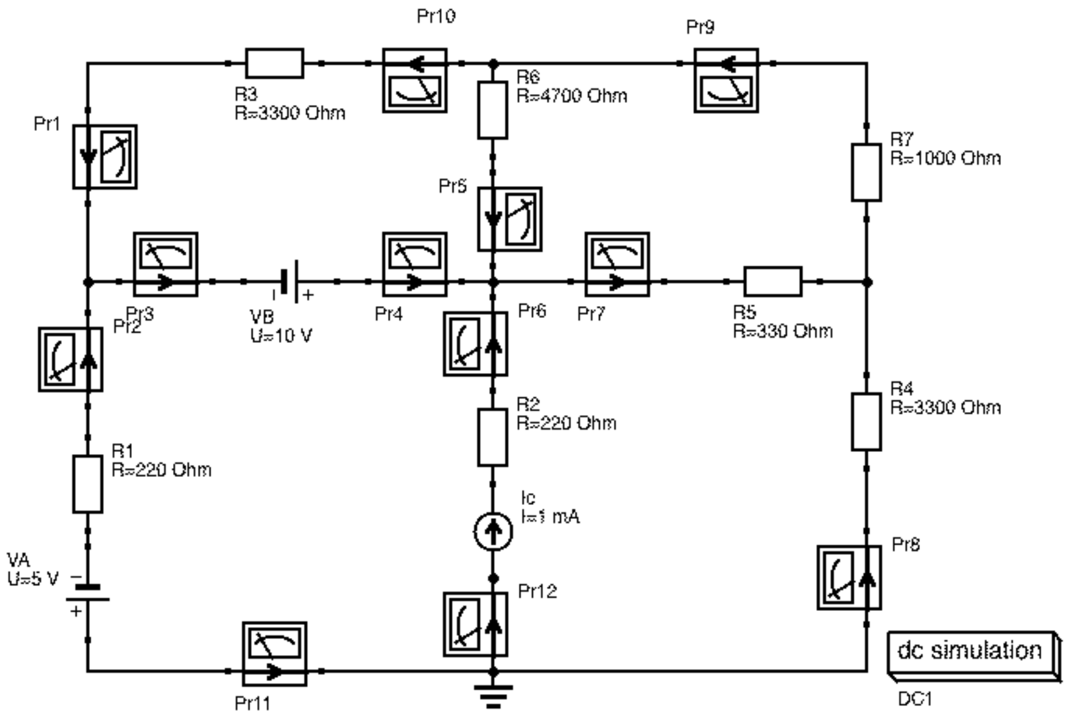
This report covers a number of circuit simulations in QUCS (Quite Universal Circuit Simulation). The first simulations involves Kirchhoff's circuit laws while the second task covers diodes and capacitors. In the third task a capacitor is charged and discharged. Finally, AC voltage over resistor in RLC series circuit is simulated in task 4.

Task 1. Resistive net with independent current and voltage sources



a) Show that Kirchhoff's Current Law holds in the five nodes (GND, N1, N2, N3 and N4) in the circuit.

Firstly, the circuit as shown in figure 1 was drawn in the simulator. In order to prove that KCL holds current probes was inserted on each wire in the circuit. The circuit used in the simulation is shown below:



number	Pr1.I	Pr2.I	Pr3.I	Pr4.I	Pr5.I	Pr6.I	Pr7.I	Pr8.I	Pr9.I	Pr10.I	Pr11.I	Pr12.I
1	0.00223	0.000212	0.00245	0.00245	-0.000559	0.001	0.00289	-0.00121	0.00167	0.00223	-0.000212	0

From the table above, we can prove that Kirchhoff's current law (KCL) holds in every node in the circuit. KCL states that the algebraic sum of currents in a network of conductors meeting at a point is zero.

N1: Pr1 + Pr2 = Pr3 gives 0.00223 + 0.000212 = 0.00245

N2: Pr4 + Pr5 + Pr6 = Pr7 gives 0.00245 - 0.000559 + 0.001 = 0.00289

N3: Pr7 + Pr8 = Pr9 gives 0.00289 - 0.00121 = 0.00167

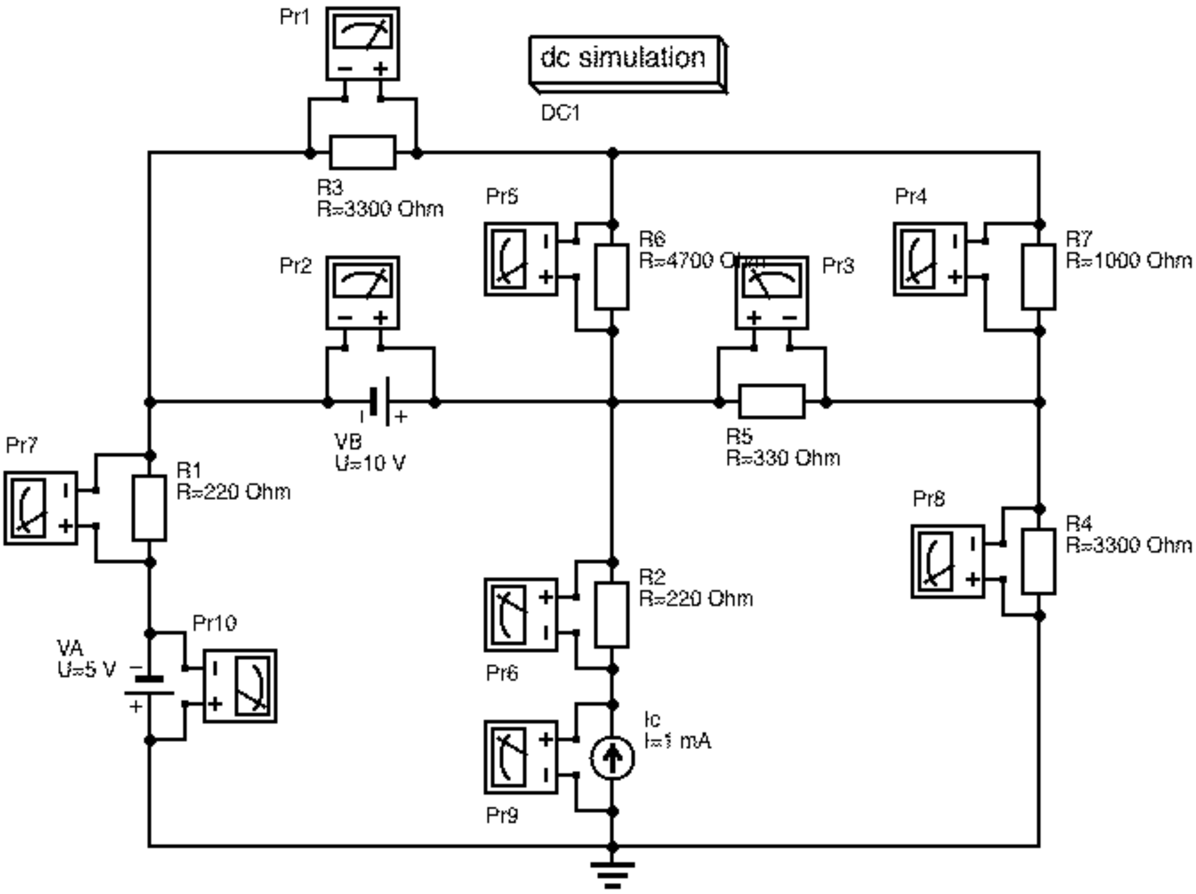
N4: Pr5 + Pr10 = Pr9 gives -0.000559 + 0.00223 = 0.00167

GND: Pr8 + Pr12 = Pr11 gives -0.00121 + 0 ≈ -0.000212

For the nodes N1-N4 the simulation can be said to be quite accurate with a margin of error of around 0.000001. This can be improved by using more digits in the calculations. The margin of error is a bit higher for the GND node where the error is around 0.0001. A potential explanation can be that Pr12 is not equal to 0A as shown in the simulation. However, the big picture of the simulation shows that KCL holds in every node of the circuit.

(b) Show that Kirchhoff's Voltage Law holds in the four loops of the circuit.

In order to prove that Kirchhoff's Voltage Law (KVL) holds in the four loops of the circuit, voltage probes was inserted on each wire in the circuit. The circuit used in the simulation is shown below:



number	Pr1.V	Pr2.V	Pr3.V	Pr4.V	Pr5.V	Pr6.V	Pr7.V	Pr8.V	Pr9.V	Pr10.V
1	7.372283	10	0.9527808	1.674936	2.627717	-0.22	0.0467012	-4.000518	5.173299	5

From the table above, we can prove that Kirchhoff's voltage law (KVL) holds in every node in the circuit. KVL states that the directed sum of the potential differences (voltages) around any closed loop is zero.

Loop 1(upper left): Pr2 + Pr5 + Pr1 gives 10 - 2.627717 - 7.732283 = -0,36

Loop 2(upper right): Pr3 + Pr4 + Pr5 gives -0.9527808 - 1.674936 + 2.627717 = 0.0000002

Loop 3(lower left): Pr9 + Pr6 + Pr2 + Pr7 + Pr10 gives -5.173299 + 0.22 + 10 - 0.0467012 - 5 = −0,0000002

Loop 4(lower right): Pr9 + Pr6 + Pr3 + Pr8 gives 5.173299 - 0.22 + 0.9527808 - 4.000518 = 0,0000002

c) Show that power is balanced in the circuit i.e. that the sum of the delivered power (from the circuit elements that deliver power to the circuit) is equal to the consumed power (by the circuit elements that consume power).

number	Pr1.I	Pr2.I	Pr3.I	Pr4.I	Pr5.I	Pr6.I	Pr7.I	Pr8.I	Pr9.I	Pr10.I	Pr11.I	Pr12.I
1	0.00223	0.000212	0.00245	0.00245	-0.000559	0.001	0.00289	-0.00121	0.00167	0.00223	-0.000212	0

number	Pr1.V	Pr2.V	Pr3.V	Pr4.V	Pr5.V	Pr6.V	Pr7.V	Pr8.V	Pr9.V	Pr10.V
1	7.372283	10	0.9527808	1.674936	2.627717	-0.22	0.0467012	-4.000518	5.173299	5

In order to prove that the power is balanced in the circuit we use P = V * I with the values obtained from a) and b). The power in the circuit is balanced if the power delivered from the voltage and current sources is equal to the power consumed by the resistors in the circuit. Additionally, the left most battery named *VA* is consuming power due to sign conventions of the currents. The power delivered/consumed for a given element is calculated by taking the voltage over that element times the current going thru it. The calculations for this is given below:

Total power delivered in the circuit:

VB = 10 V * 0.00245 A = 0.0245 W

Ic = 5.173299 V * 0.001 A = 0.005173299 W

<u>Total power delivered: 0.029673299 W</u>

Total power consumed by the circuit:

VA = 5 V * 0.000212A = 0.00106 W

R1 = 0.0467012 V * 0.000212 A = 0.0000099006544 W

R2 = 0.22 V * 0.001 A = 0.00022 W

R3 = 7.372283 V * 0.00223 A = 0.01644019109 W

R4 = -4.000518 V * 0.00121 A = 0.00484062678 W

R5 = 0.9527808 V * 0.00289 A = 0.002753536512 W

R6 = 2.627717 V * 0.000559 A = 0.001468893803 W

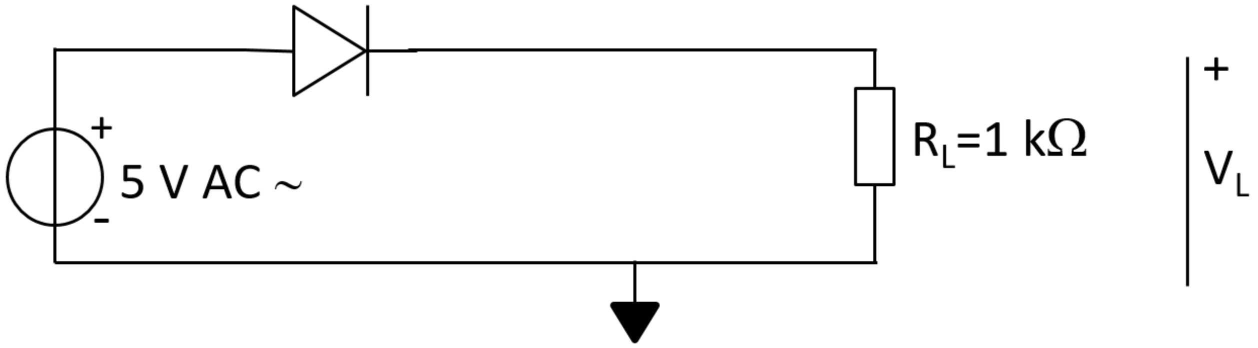
R7 = 1.674936 V * 0.00167 A = 0.00279714312 W

<u>Total power consumed = 0.02959029196 W</u>

The power consumed is reasonably close to the power delivered with a margin of error at 0.000083W (0.029673299 - 0.02959029196). The difference between delivered and consumed power is 0.2805%. This is as described in the previous tasks due to the number of digits used in the calculations. Moreover, when performing new calculations with the values obtained from the simulation the margin of error may increase a bit. However, the value is still approaching zero as expected which shows that the power in the circuit is balanced.

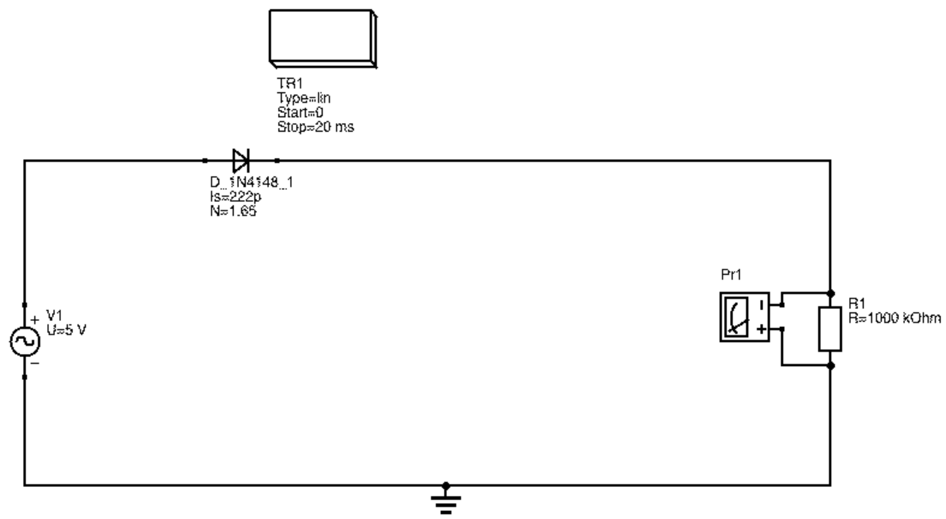
Task 2: Analysis of a rectifying diode circuit

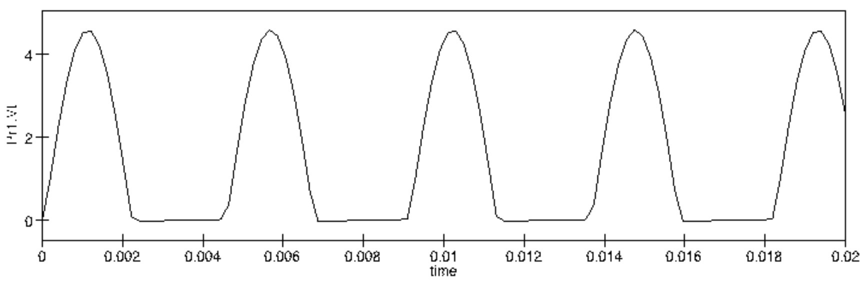
In this task a transient simulation from t = 0ms to t = 20ms was performed on the circuit shown below.



a) Analyze how well the circuit converts the AC sinusoidal voltage into a positive DC constant voltage over load resistor RL.

Firstly, the circuit as shown in the figure above was drawn in the simulator. The circuit used in the simulation is shown below:

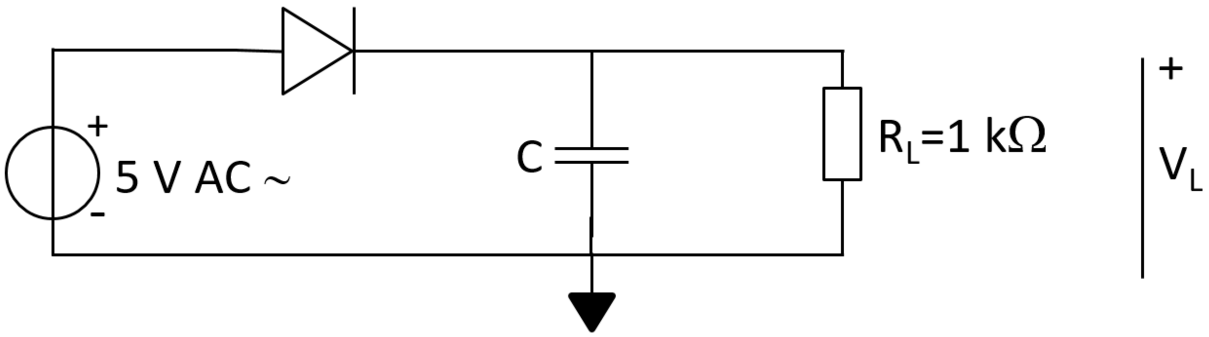




As can be seen in the graph generated by the simulation the diode in the circuit prevents the current from flowing in the opposite direction which in turn makes the voltage over the load resistor non-negative. In this way, the circuit converts the AC to a DC-like constant voltage over the resistor.

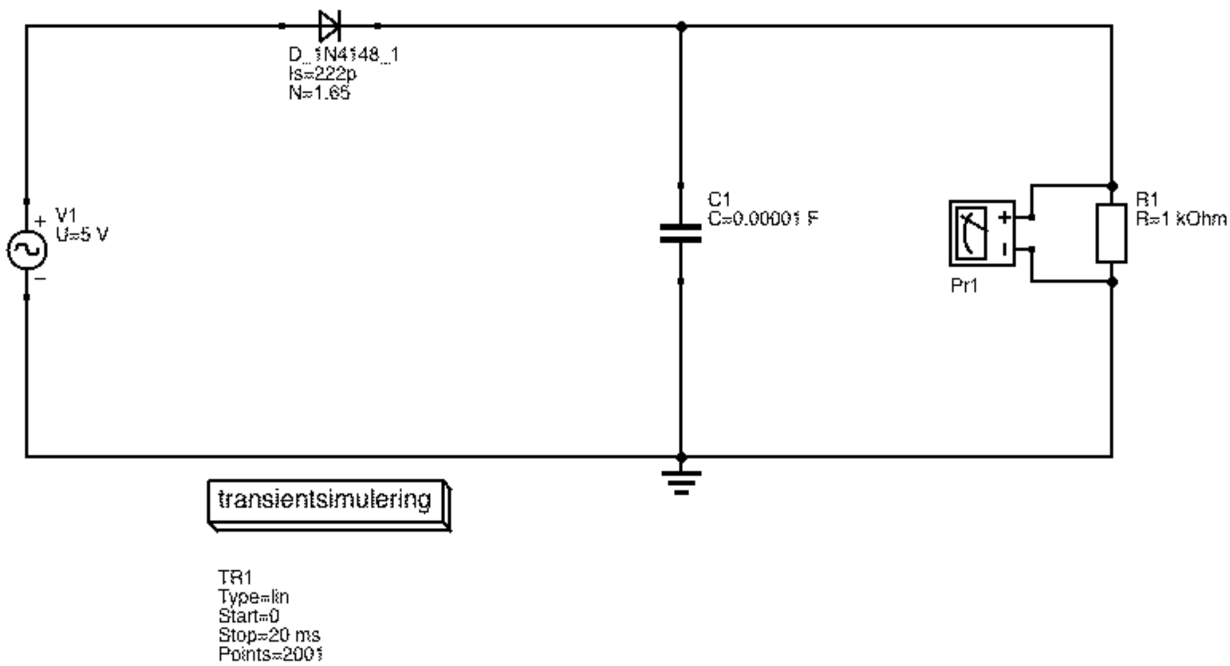
Moreover, the peak voltage over the resistor does not reach 5 V, as delivered from the voltage source, due to that the forward voltage of the diode is 0.7 V. When looking at the graph we can see that the voltage over the resistor is close to approximately 4.3 V (5 - 0.7). This hypothesis was confirmed by connecting a DC-voltage to the circuit and measuring the voltage of the diode as well as the resistor.

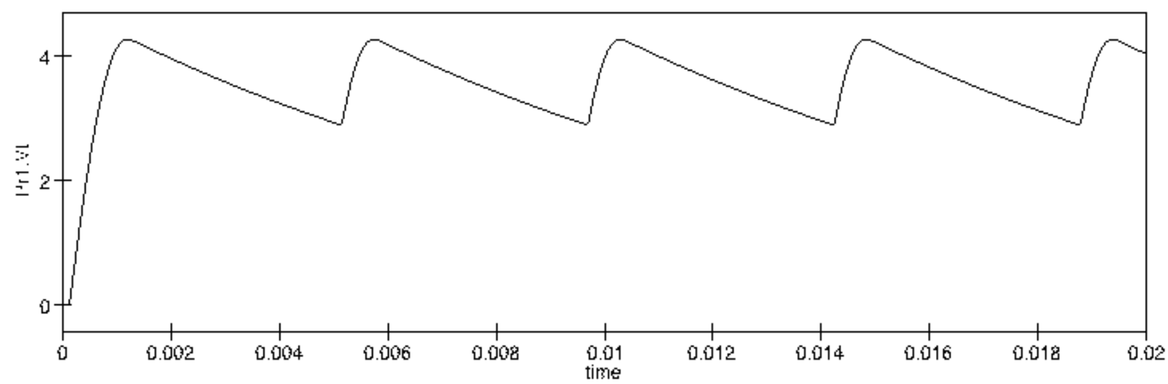
The conversion from AC to DC can be improved by adding a capacitor in parallel with the load as depicted in the schematic below.



b) Analyze how well the circuit converts the AC sinusoidal voltage into a DC constant voltage over load resistor RL when C=10 µF. Vary C and RL and describe how the AC to DC conversion is affected.

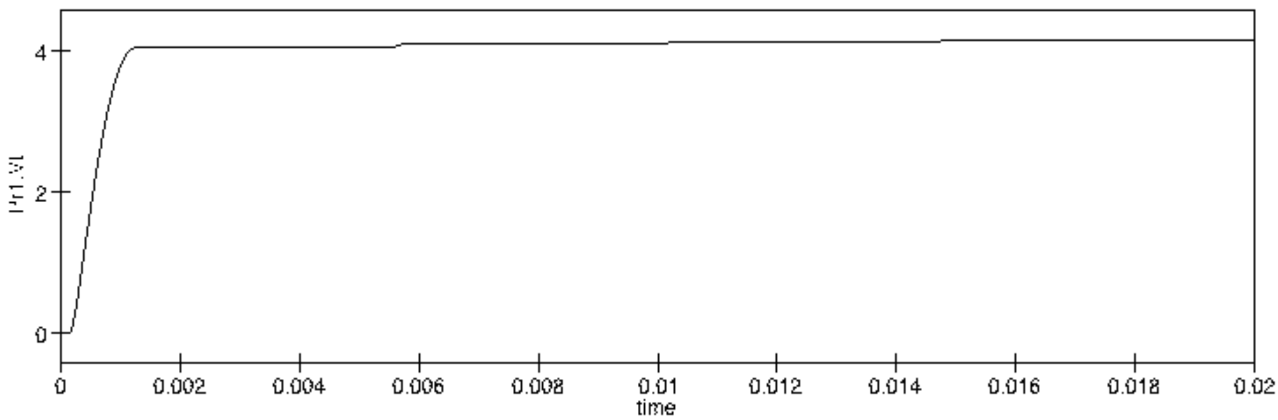
When a capacitor with a capacitance of 10 μF is inserted in the circuit as shown above the conversion changes as seen in the graph below:





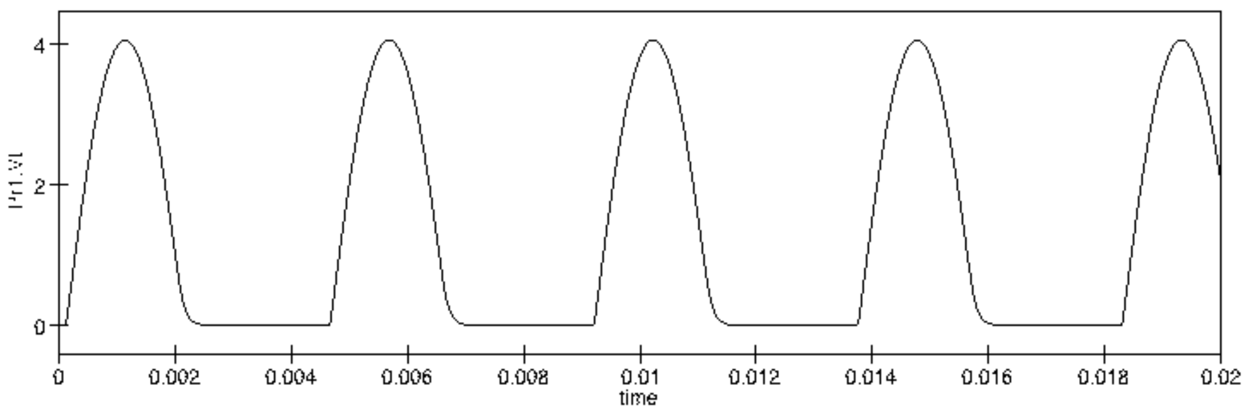
With a capacitor inserted in the circuit a voltage > 0 is obtained over the resistor that is closer to DC than in the previous example. All electrical systems has something called a time constant (τ) which explains the time delay of the circuit when an input voltage is applied. The time constant will mainly depend upon the reactive components, capacitive or inductive, connected to it. In this case we have a so called RC-time constant since the circuit consist of resistors and capacitors and refers to the rate of charge or discharge of the capacitor. The larger any or both of the two values, the longer it takes for a capacitor to charge or discharge. If the resistance is larger, the capacitor takes a longer time to charge, because the greater resistance creates a smaller current. If the capacitance of the capacitor is a larger value, the capacitor takes a longer time to charge because it holds a larger charge, therefore, it takes longer to fill up.

When increasing the resistance to 100.000 Ω of the capacitor we get the following result:



As in this case of a resistor in parallel with a capacitor, the resistor controls the discharge rate of the capacitor. Here we see that the voltage over the resistor gets closer to constant. This is because when a capacitor has a lower capacitance it charges up faster. In an AC circuit, current only passes through a capacitor during the time a capacitor is either charging or discharging. If a capacitor is fully charged or discharged, it acts like an open circuit and does not pass current, its impedance is infinite.

If we instead decrease the resistance of the resistor to 10 Ω and let C = 10 μF, we get the following behavior:



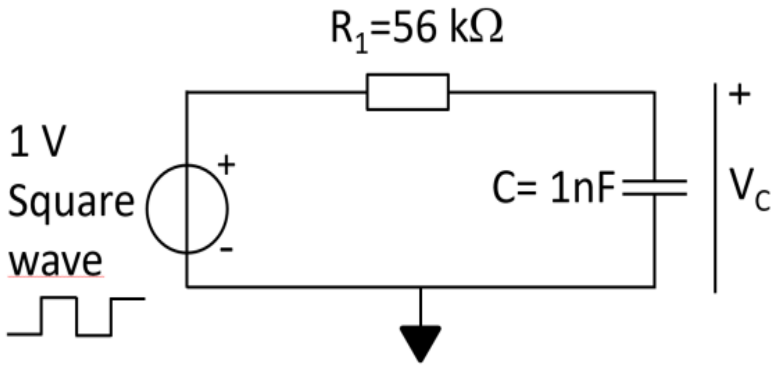
This behavior can be explained by the RC-time constant discussed above. Increasing the resistance reduces the current, which means the rate at which charge flows from the capacitor is reduced. The capacitor voltage stays high for a longer time. The same behavior holds for the capacitor itself where a higher capacitance results in a slower charge/discharge rate. This is consistent with the definition of the time constant, the product RC, which is a measure of how quickly the current, and potential differences, change in the circuit. Decreasing the time constant means that these quantities change more quickly. Or in other words, a lower resistance allows a higher current thru the resistance by which the capacitor can be discharged.

Difference between the three graphs

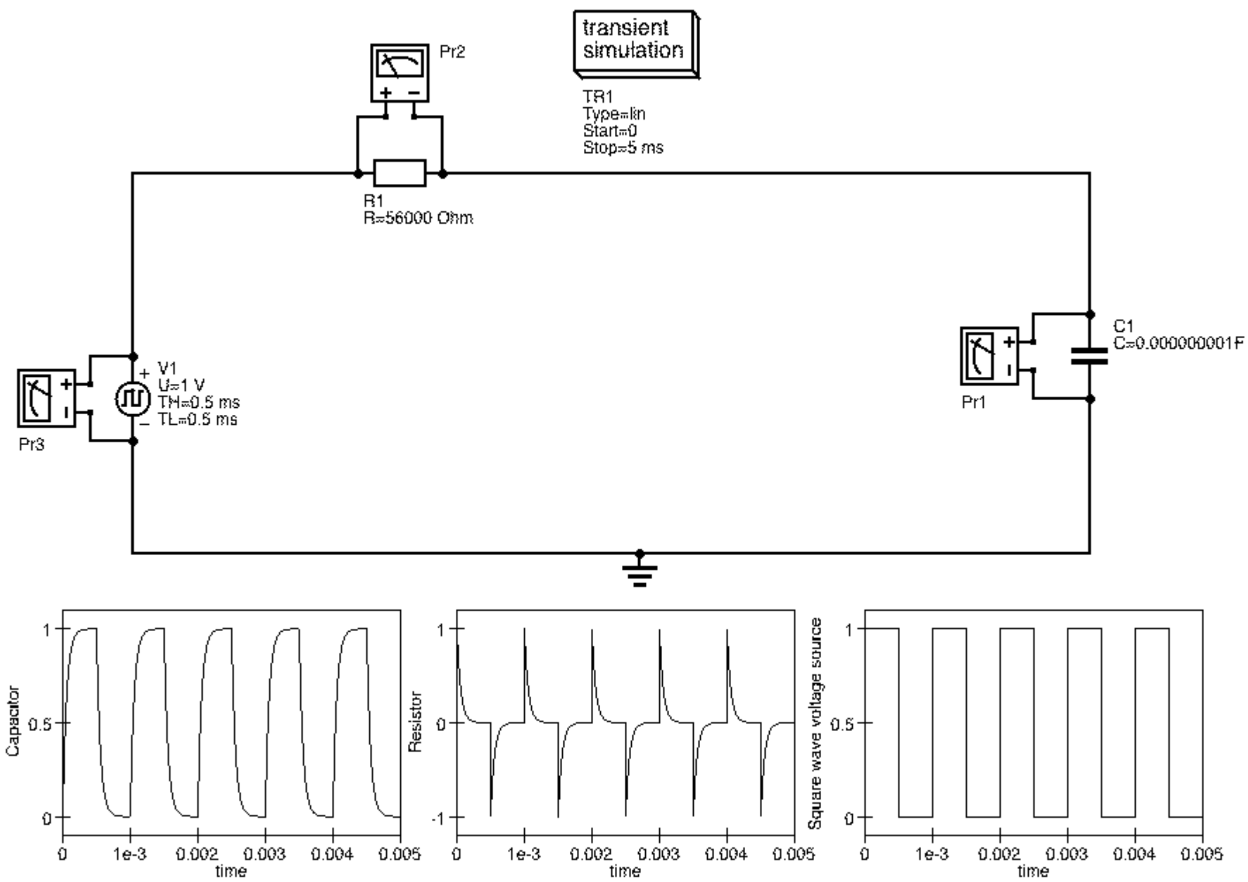
When performing the simulation with a resistance of 100.000 Ω the discharging of the capacitor is so slow so that it does not get discharged between the cycles. Thus, the graph shows a constant voltage after the first cycle. However, when lowering the resistance to 10 Ω the capacitor discharges all the way to 0 V and thus gives a periodic graph. However, the first graph which shows the result of the simulation with a capacitance of 10 μF and a resistance of 1.000 Ω is something in-between this two cases were the capacitor gets partially discharged within a cycle before it gets charged again.

Task 3: Charging and discharging of capacitor

In this task a transient simulation was performed on different intervals and frequencies of the voltage source. The circuit used is as follows:

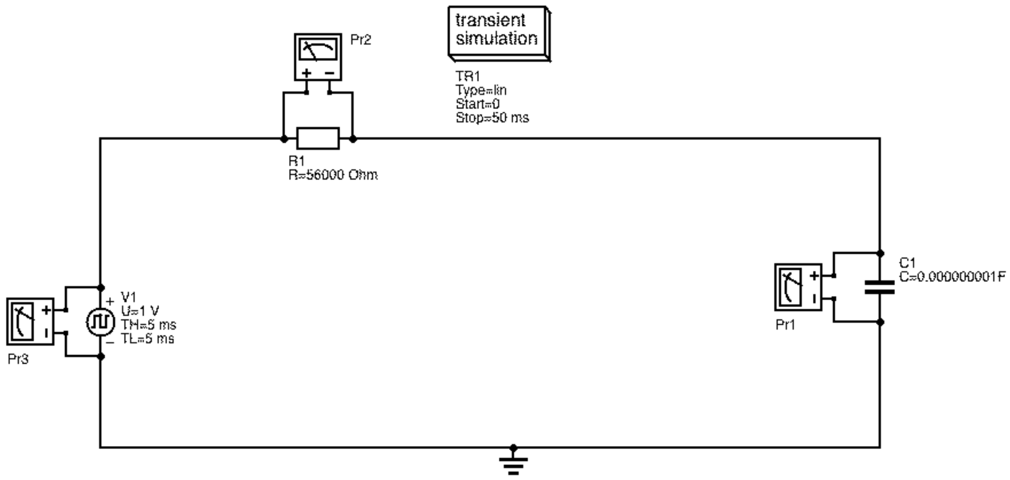


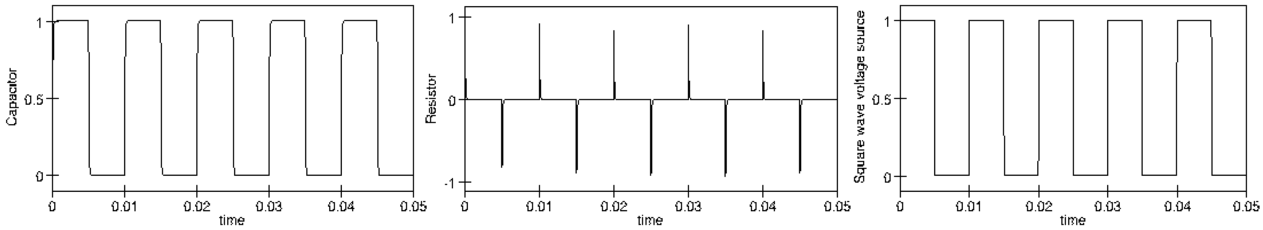
a) **Analyze how the voltage over the capacitor varies as a function of time and compare it to the square wave voltage source and the voltage over the resistor. Duration of high / low pulse = 0.5 ms and duration of simulation equals 5 ms. The following results was obtained:**



In the graph above we can see that the voltage over the resistor is initially at maximum as well as that the voltage over the capacitor increases as it charges. When the capacitor is fully charged no current will flow thru the circuit. As the current decreases this will also affect the voltage over the resistor. As can be seen in the graph the voltage over the resistor gets negative which is due to that the current changes direction as the time interval for the voltage source ends. When the capacitor is fully discharged the current as well as the voltage goes to 0.

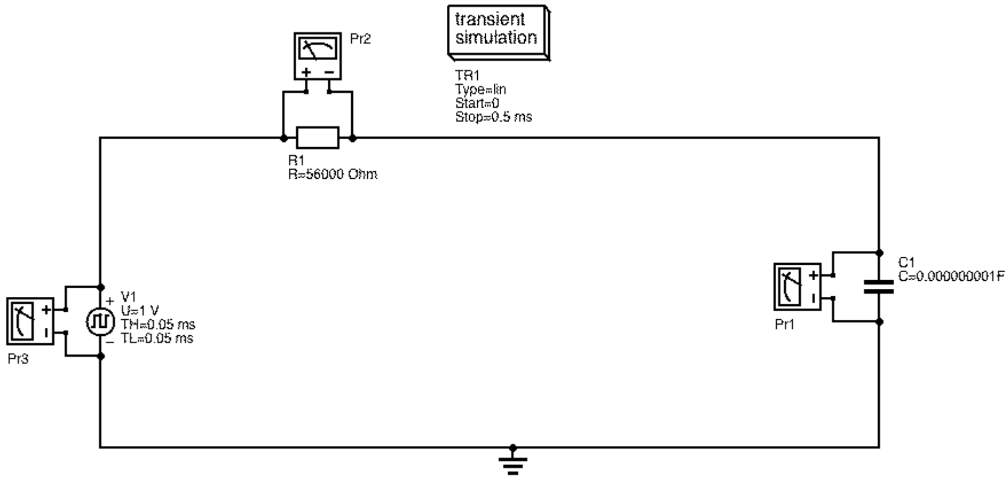
b) Analyze how the voltage over a capacitor varies as a function of time when the frequency of the source voltage decrease ten times compared to Task 3A. Perform a transient simulation from t=0 s to t=50 ms and change the times at high/low voltages to 5 ms.

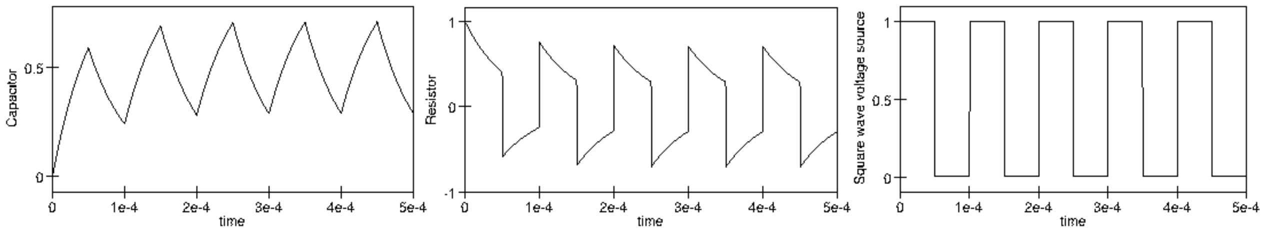




As the time interval of the voltage source decreases ten times from 0.5 ms to 5 ms it results in that the voltage source will deliver 1 V for a longer time. This will also result in that the capacitor will be fully charged for a longer time. Which as described in section a) means that the voltage over the resistor will be 0 for a longer time. The capacitor will act as the voltage source as it controls when current will flow and therefore also controls the voltage over the resistor.

c) Analyze how the voltage over a capacitor varies as a function of time when the frequency of the source voltage increase ten times compared to Task 3A. Perform the transient simulation from t=0 s to t=0.5 ms and change the times at high/low voltage to 0.05 ms.

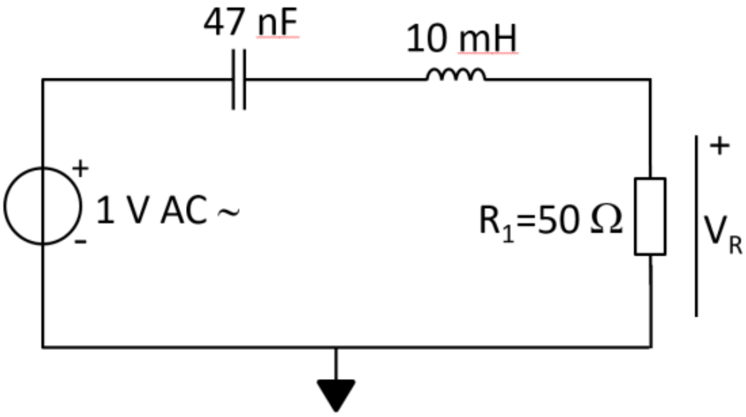




In the graph which displays the voltage over the capacitor we can see that it never fully charges up which means that a current will always flow thru the circuit until the voltage source stops delivering voltage and the capacitor later discharges. However, in the resistor graph we can see that the voltage over the resistor never goes to 0, but it slowly decreases and changes direction as the current changes direction. Due to that the capacitor never gets fully charged the current in the circuit will always be > 0 A which results in that the resistor first gets an voltage corresponding to that of the voltage source and then get a negative direction as the capacitor charges. The voltage over the resistor decreases as the capacitor charges.

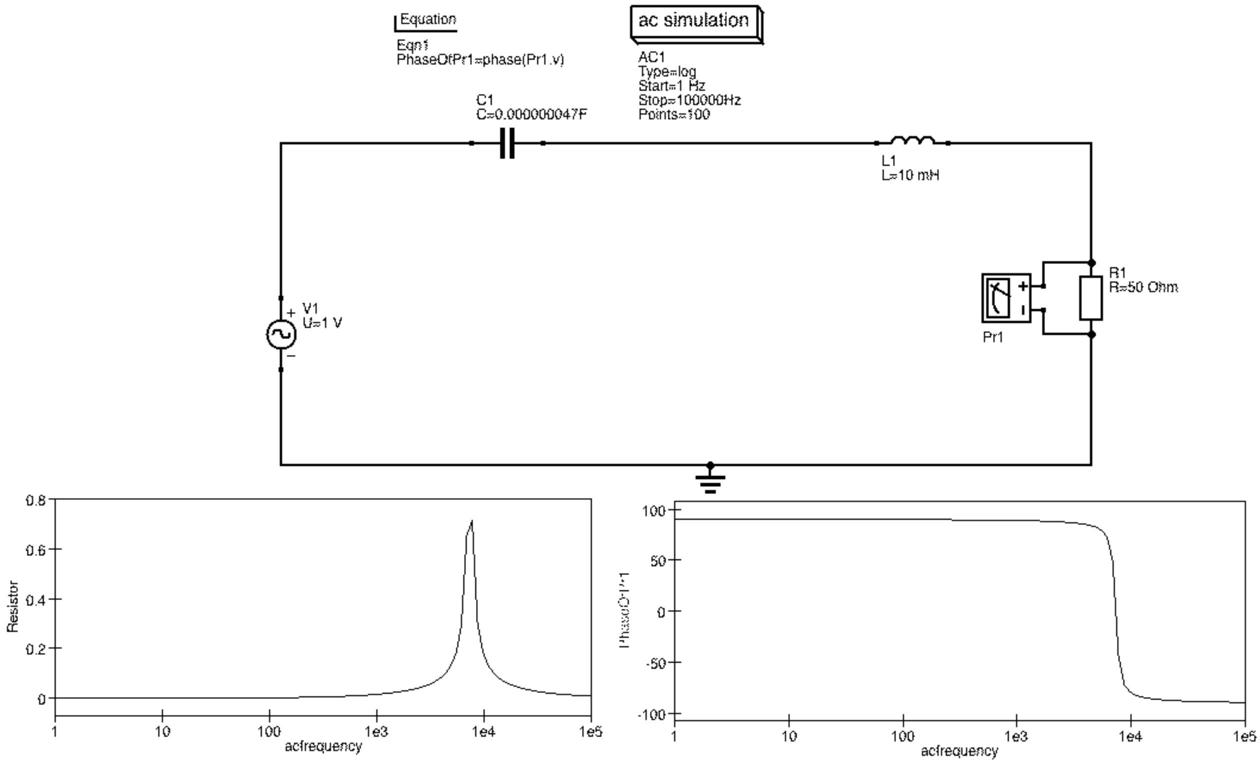
Task 4. AC voltage over resistor in RLC series circuit

In this task a AC simulation from 1 Hz to 100 kHz was performed on the circuit shown below:



a) Analyze what filter function is performed by the series RLC circuit by analyzing what frequencies are present over R with an amplitude close to the source amplitude. Also analyze how the phase of VR varies as a function of frequency? Describe why the amplitude and phase of VR varies as it does.

Firstly, the circuit shown above was drawn in the simulator and a AC simulation from 1 Hz to 100 kHz. The following results was obtained:



As we can see in the left graph above showing the voltage over the resistor the voltage is 0 V when the frequency is 0 Hz < *f* < 1.000 Hz. The voltage then rises quickly and going back to 0 V again.

This is because a low frequency gives a high resistance over the capacitor. This is due to that the impedance of capacitor is $z = \dfrac{1}{2\pi f C}$

When the frequency is 0 it results in a high impedance over the capacitor and blocks the current going to the resistor and the voltage over the resistor is consequently 0 V. On the other hand, when the frequency is high we also get a high impedance over the inductor. In this case we get a voltage of 0 V since the current is blocked by the inductor.

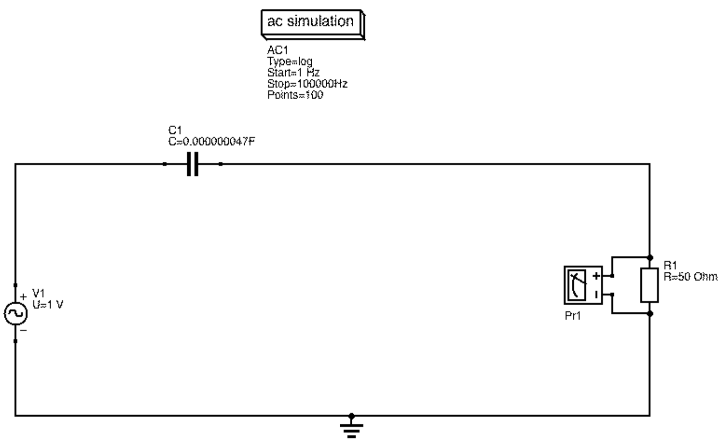
However, if the frequency is approximately 1.000 Hz $< f <$ 10.000 Hz the impedance of the capacitor and inductor will be equal to each other but with opposite signs (+/-) which results in a total impedance of 0. This results in that the voltage over the resistor is at its maximum. We can therefore conclude that the RLC circuit performs as a band-pass filter.

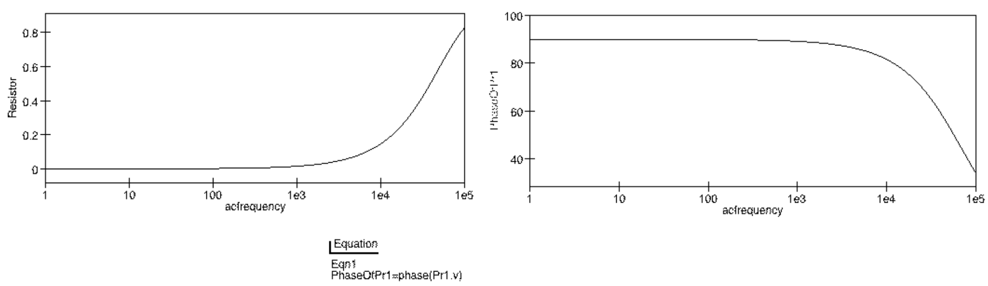
Regarding the right graph showing how the phase of V_R varies as a function of frequency we can see that a high frequency gives a high impedance over the inductor compared to the capacitor. Because of this we get an inductive circuit and an inductive phase shift which means a negative phase shift. Additionally, when $f \to \infty$ the phase shift is at its maximum and equal to -90°.

However, when the impedance over the capacitor is greater than that over the inductor we get a capacitive circuit and a capacitive / positive phase shift. The phase shift is at its maximum of 90° when $f \to 0$. But if the impedance is the same in the capacitor and the inductor we get a circuit where the current and voltage is in phase with each other which results in a phase shift of 0° which can be observed in the graph above.

b) Perform the same analysis as in Task 4A but remove the inductor from the circuit so that the circuit consists of the capacitor in series with the resistor.

The inductor was removed from the circuit and the same simulation as in a) was performed: The following results was obtained:



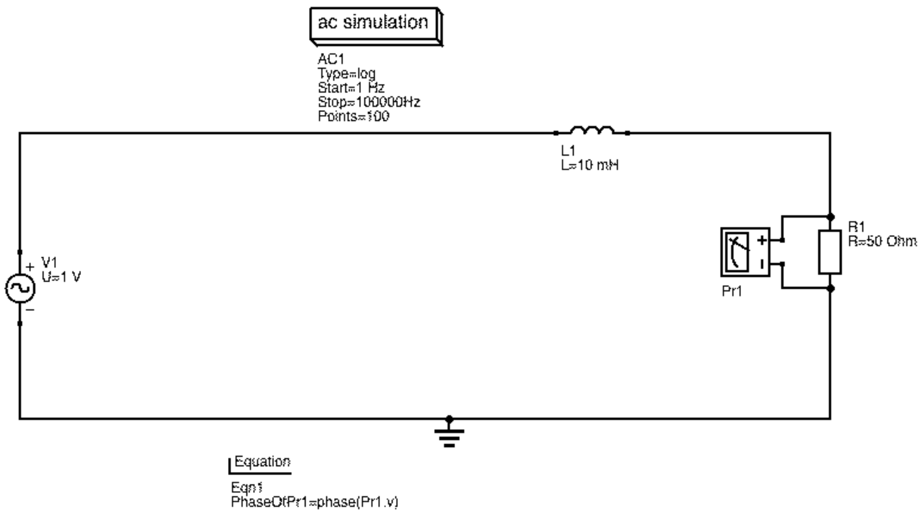


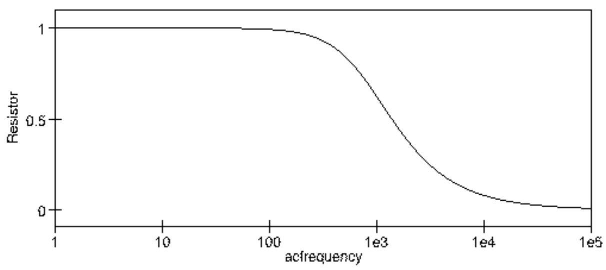
The results of this simulation is similar to that of a) but with the absence of the influence of the inductor. As described in section a) a low frequency gives a high resistance over the capacitor. So similar to the simulation in a) the voltage over the resistor is 0 when 0 Hz $< f <$ 1.000 Hz. The voltage over the resistor then start to rise when $f >$ 1.000 Hz. Since there is no inductor in the circuit the voltage over the resistor will not drop since the current is not blocked by the inductor. Regarding the phase shift we get a capacitive circuit and a positive phase shift.

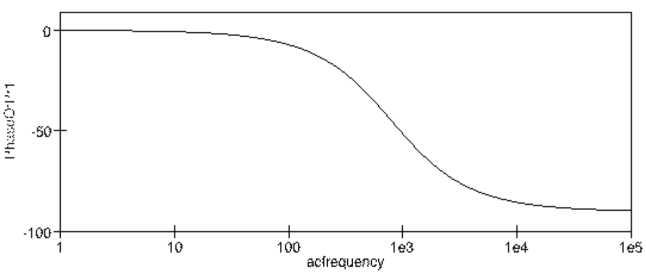
At low frequencies, the capacitor functions as an open circuit blocking any current. At high frequencies the capacitor functions as a short circuit and current can pass thru. With this information we can conclude that the circuit in this task functions as a high-pass filter since it passes current at high frequencies.

c) Perform the same analysis as in Task 4A but remove the capacitor from the circuit so that the circuit consists of the inductor in series with the resistor.

The capacitor was removed from the circuit and the same simulation as in a) was performed: The following results was obtained:







The results of this simulation is similar to that of a) but with the absence of the influence of the capacitor. As described earlier, when the frequency is low we get a low impedance over the inductor compared to that of the resistor, resulting in that the inductor function as a short circuit. At high frequencies, the inductor's impedance is high compared to that of the resistor and the inductor thus functions as an open circuit blocking any current. With this information we can conclude that the circuit in this task functions as a low-pass filter since it passes current at low frequencies.