

COMP4300 Spring 2022

Homework 2

Due 29 April 2022, 11:59pm

1. Suppose you are designing a cache for a machine with 32-bit addresses. The cache is 1MB in size. Cache blocks are 1024 bytes.
- How many blocks can be held in the cache
 - How many bits of the address are devoted to the offset?
 - If the cache is direct-mapped, how many bits are devoted to the tag and index?
 - If the cache is 8-way set associative, how many bits are devoted to the tag and index? How many sets are there?
 - If the cache is fully associative, how many bits are devoted to the tag and index?

$$a) 1 \text{ MB} = \frac{2^{20} \text{ bytes}}{\text{cache}} ; 1024 = \frac{2^{10} \text{ bytes}}{\text{block}}$$

$$\frac{2^{20} \text{ bytes}}{\text{cache}} / \frac{2^{10} \text{ bytes}}{\text{block}} = \boxed{\frac{2^{10} \text{ blocks}}{\text{cache}} = 1024}$$

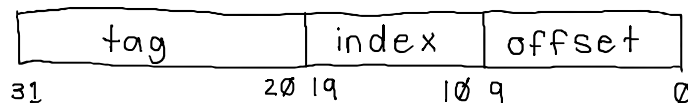
b) 1024 byte blocks

$$\Downarrow \\ 2^{10} \rightarrow \boxed{10\text{-bit offset}}$$



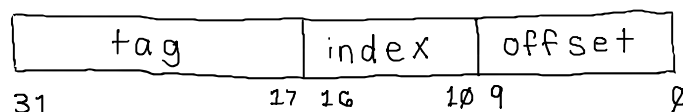
c) 1024 blocks / cache

$$\Downarrow \\ 2^{10} \rightarrow \boxed{\begin{array}{l} 10\text{-bit index} \\ 12\text{-bit tag} \end{array}}$$

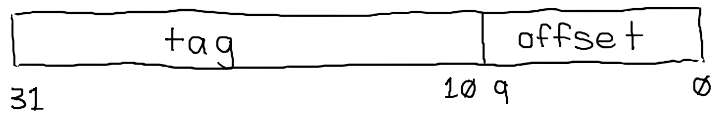


d) 8 blocks / set

$$1024 / 8 = 128 \text{ sets} \rightarrow 2^7 \text{ sets} \rightarrow \boxed{\begin{array}{l} 7\text{-bit index} \\ 15\text{-bit tag} \end{array}}$$



e) No index
22-bit tag



2. Suppose you have a machine with separate I- and D- caches. The miss rate on the I-cache is 2%, and on the D-cache 3%. On an I-cache hit, the value can be read in the same cycle the data is requested. On a D-cache hit, one additional cycle is required to read the value. The miss penalty is 100 cycles for either cache. 35% of the instructions on this RISC machine are LW or SW instructions, the only instructions that access data memory. A cycle is 2ns. What is the average memory access time?

$$\begin{aligned}
 &\text{avg mem access time split I/D cache} = \\
 &\left(\begin{array}{l} \% \text{ mem access} \\ \text{for instruction} \end{array} \right) \left(\begin{array}{l} \text{avg mem access time} \\ \text{for instruction load} \end{array} \right) \\
 &+ \left(\begin{array}{l} \% \text{ mem access for} \\ \text{data load/store} \end{array} \right) \left(\begin{array}{l} \text{avg mem access time} \\ \text{for data} \end{array} \right)
 \end{aligned}$$

I- cache

$$\begin{aligned}
 &\text{avg mem access time} = \\
 &\text{hit time} + \text{miss rate} (\text{miss penalty}) \\
 &= 1 + 0.02(100) = 3
 \end{aligned}$$

D- cache

$$\begin{aligned}
 &\text{avg mem access time} = \\
 &\text{hit time} + \text{miss rate} (\text{miss penalty}) \\
 &= 2 + 0.03(100) = 5
 \end{aligned}$$

split I/D cache

$$\begin{aligned}
 &\text{avg mem access time} = \\
 &\left(\frac{1}{1.35} \right) (3) + \left(\frac{0.35}{1.35} \right) (5) = 3.52 \text{ cycles}
 \end{aligned}$$

$$3.52 \text{ cycles} \times \frac{2 \text{ ns}}{\text{cycle}} = \boxed{7.04 \text{ ns}}$$