Lab 4 Tests

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These are the simulations described in the tutorial video on Canvas for regular/full credit

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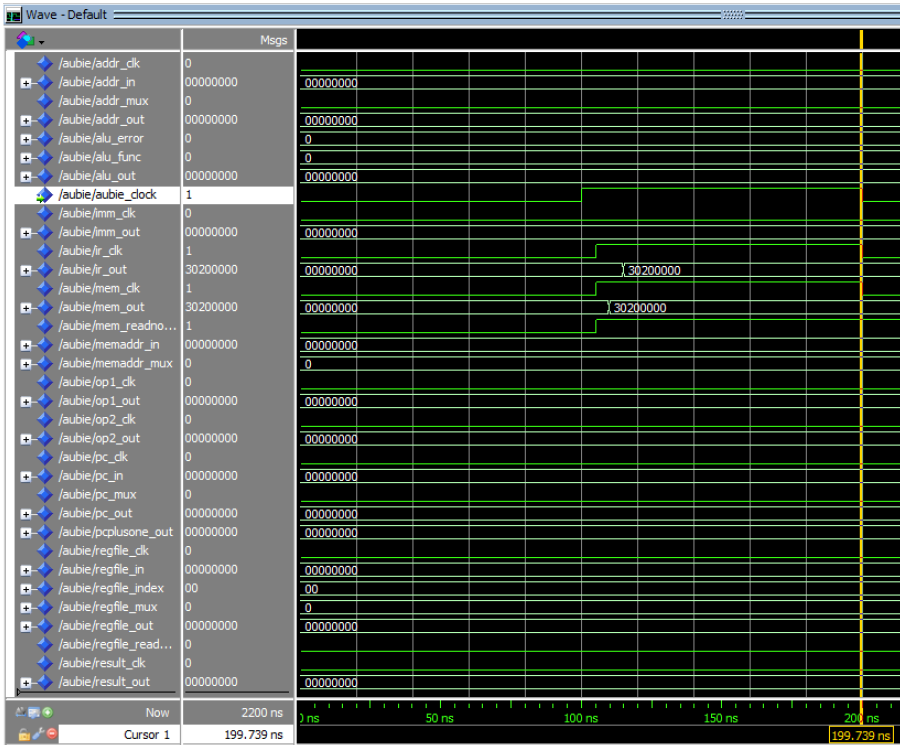
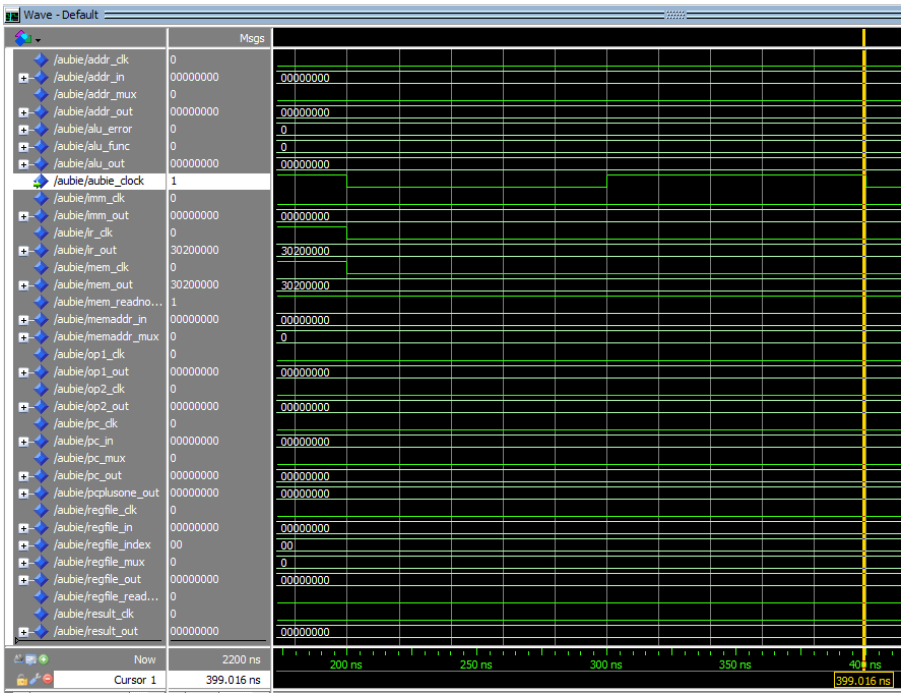
LD R4, 0x100

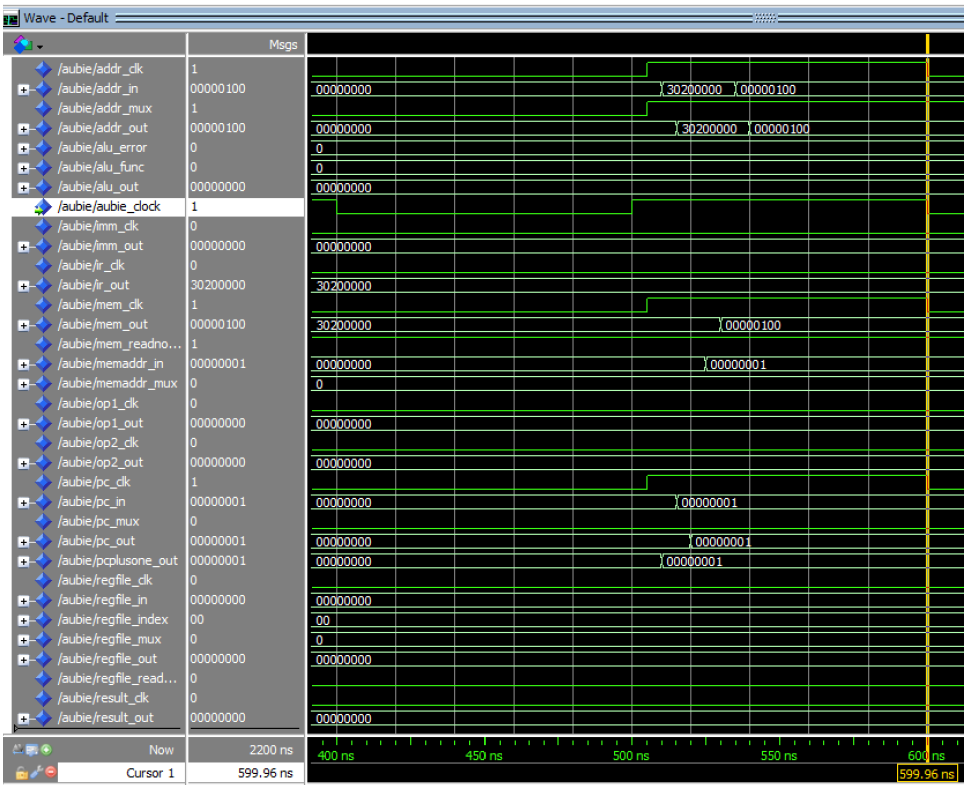
State 1: Mem[PC] -> InstrReg (0 – 200 ns)



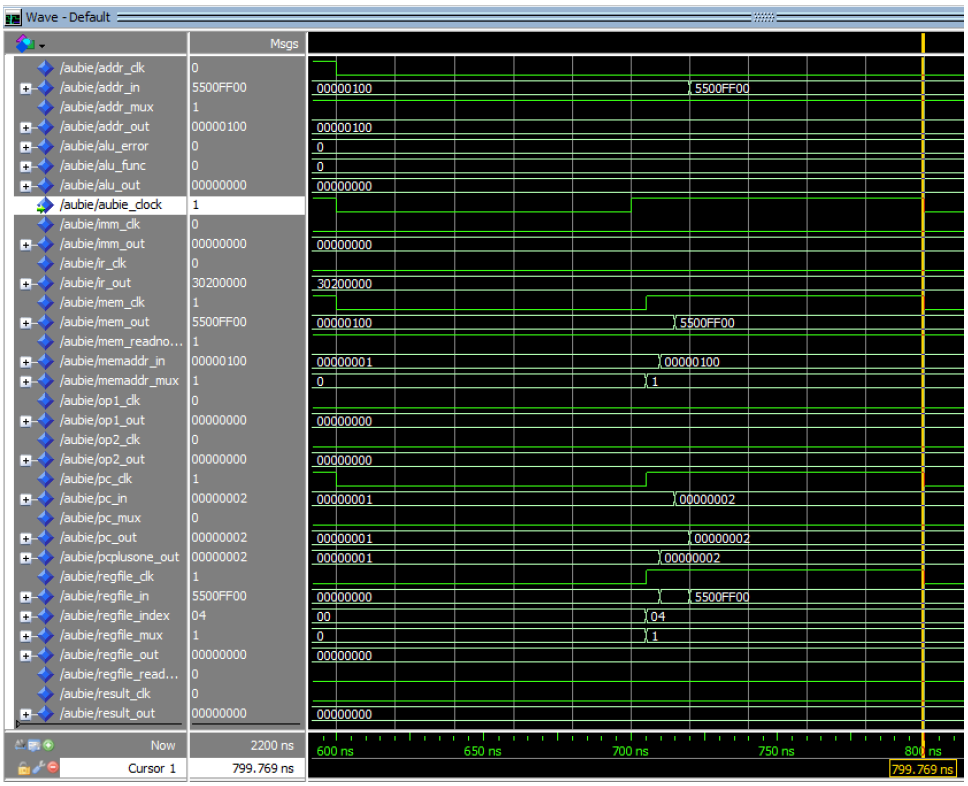
State 2: Nothing happens (changing states) (200 – 400 ns)



State 7: PC + 1 -> PC; Mem[PC] -> Addr (400 – 600 ns)

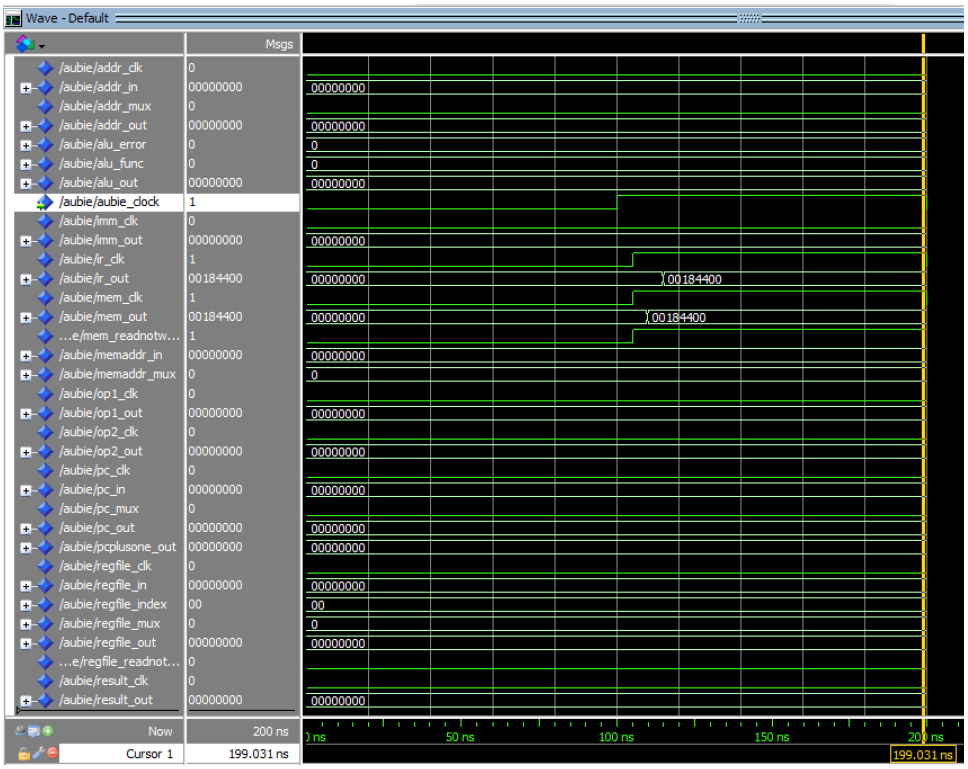


State 8: Mem[Addr] -> Regs[IR[dest]]; PC + 1 -> PC (600 – 800 ns)

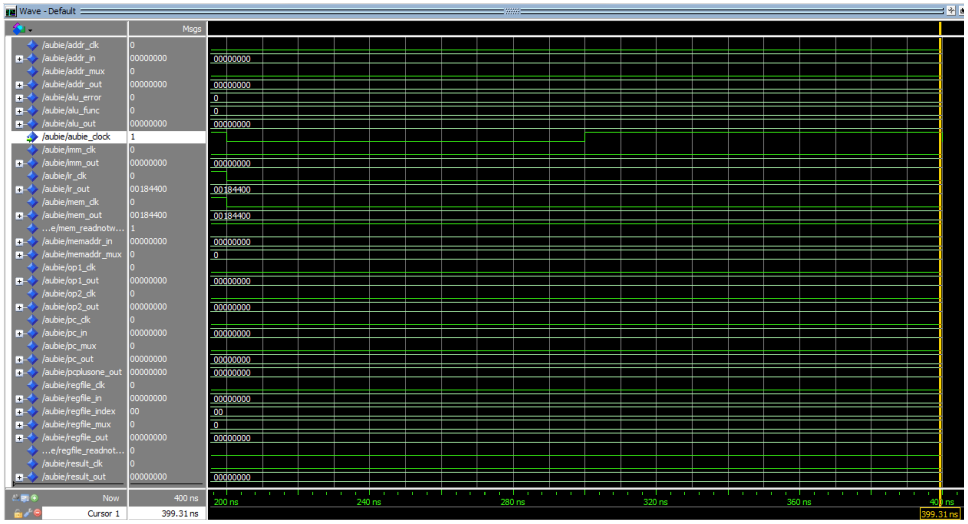


ADDU R3, R1, R2

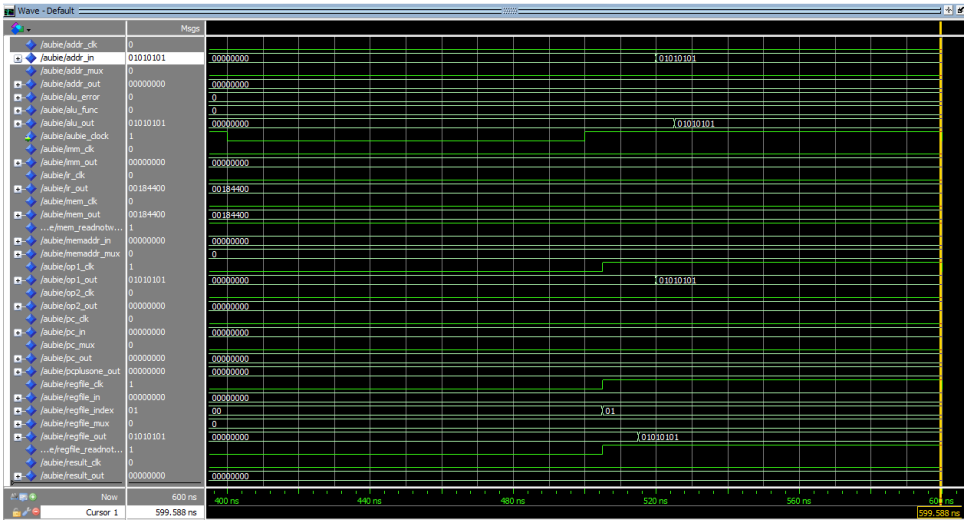
State 1: Mem[PC] -> InstrReg (0 – 200 ns)



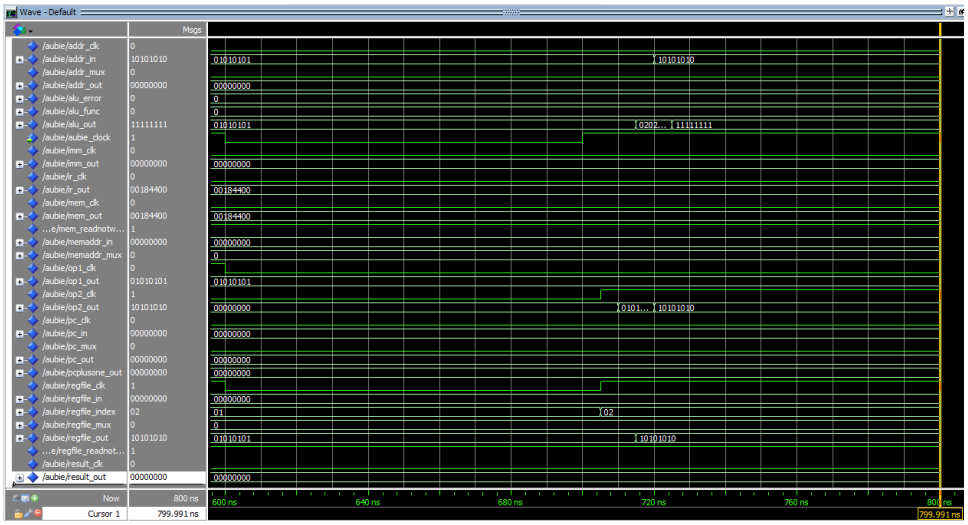
State 2: Nothing happens (changing states) (200 – 400 ns)



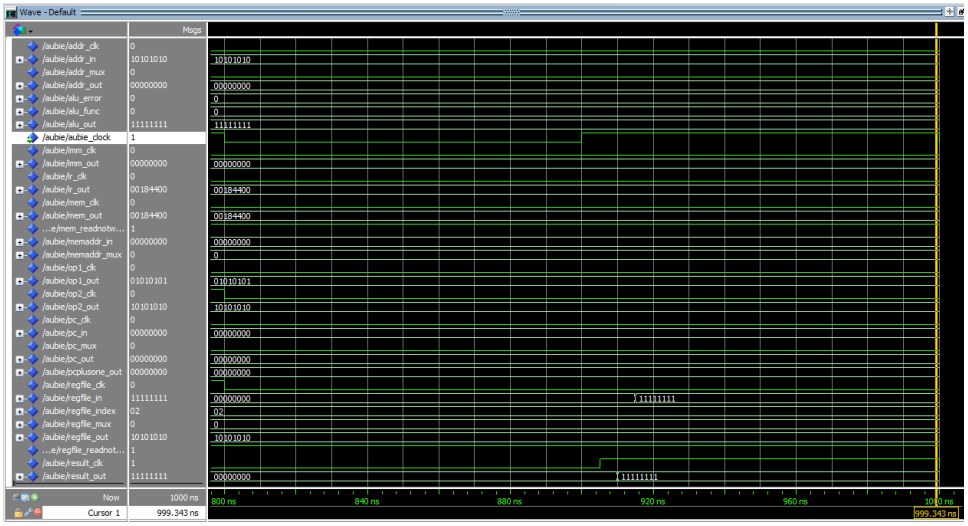
State 3: Regs[IR[op1]] -> Op1 (400 – 600 ns)



State 4: Regs[IR[op2]] -> Op2 (600 – 800 ns)



State 5: ALUout -> Result (800 – 1000 ns)



State 6: Result -> Regs[IR[dest]]; PC + 1 -> PC (1000 – 1200 ns)