EMILY YU

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Institute of Science and Technology Austria, Klosterneuburg, Austria

EDUCATION

Johannes Kepler University Linz, Austria 2019 – 2023
Ph.D. in Computer Science
Thesis: *Certifying Hardware Model Checking*
Supervisor: Prof. Armin Biere

Imperial College London, United Kingdom 2014 – 2018
M.Eng in Computing, *First Class Honours*
Integrated Master's degree: 3-year Bachelor + 1-year Master
Thesis: *Model Checking Temporal Epistemic Logic under Bounded Recall*
Supervisor: Prof. Alessio Lomuscio

Concord College, United Kingdom 2012 – 2014
GCE A-levels (High School)
Maths (A*), Further Maths (A*), Economics (A), and Physics (A).

RESEARCH INTERESTS

System Verification: both for hardware designs and AI-based systems;
Runtime Monitoring: ensuring runtime safety and correctness of complex dynamical systems.

PROFESSIONAL EXPERIENCE

Institute of Science and Technology Austria, Austria Sept 2023 – Sept 2025
Postdoctoral Researcher

· Working with Prof. Thomas A. Henzinger on runtime monitoring and neural control verification.

Woodpecker Technologies, Singapore Aug 2022 – Jan 2023
External Consultant

· Pre-silicon formal verification for chip designs.

Johannes Kepler University Linz, Austria 2019 – 2023
Project Assistant

· Formal Models and Verification Group, lead by Prof. Armin Biere.

Morgan Stanley, London, United Kingdom Apr – Sep 2017
Software Engineer

· Full-stack development during 6-month industrial placement.

BlackRock, London, United Kingdom Jun – Aug 2016
Software Engineer Intern

· Worked on internal web platform development.

Imperial College London, United Kingdom 2015 – 2016
Teaching Assistant

· Part-time employment. Courses: Discrete Maths, Logic, and Reasoning about Programs.

Imperial College London, United Kingdom Jul – Sep 2015
Research Assistant

· 20 hours per week. Group of Prof. Chris Hankin. Research on games and abstractions for cybersecurity.

CAREER BREAKS

Maternity leave 2021-2022.

LANGUAGE PROFICIENCY

English (fluent), Cantonese (fluent), German (B2), Mandarin (native)

HONORS & AWARDS

FWF ESPRIT Fellowship Awardee, Principal Investigator, 2025
RAVENS: Runtime Assurance and Verification of Neural Systems
Austrian Science Fund, EUR 346,505
Host Institute: Vienna University of Technology, Austria

Disruptive Idea Award, Neuro-symbolic Systems (NeuS) Conference, 2025
DARPA award, USD 100,000

ACADEMIC SERVICES AND OUTREACH

Member of Program Committee

· European Conference on Artificial Intelligence (ECAI), 2025;
· Int. Joint Conference on Artificial Intelligence (IJCAI), 2025;
· Int. Conference on Formal Methods in Computer-Aided Design (FMCAD), 2025;
· Int. Conference on integrated Formal Methods (iFM), 2024.

Member of Artifact Evaluation Committee

· Int. Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI), 2024;
· Int. Symposium on Formal Methods (FM), 2024;
· Int. Symposium on Automated Technology for Verification and Analysis (ATVA), 2024.

Journal Referee

· Formal Aspects of Computing Journal, 2025.

Conference (sub-)Referee

· Int. Conference on Neuro-symbolic Systems (NeuS), 2025;
· Int. Conference on Automated Deduction (CADE), 2025.

Scientific Referent for Funding Agencies

· French National Research Agency (ANR), 2025.

Event Organization

· CAV 2021, Virtual. A member of the volunteering team.
· QONFEST 2020, Vienna, Austria. A member of the volunteering team.
· Kurt Goedel Conference 2019, Vienna, Austria. A member of the volunteering team.

STUDENT SUPERVISION

PhD rotation supervisor at Institute of Science and Technology Austria (ISTA) for Fabian Kresse, Spring 2025. Project topic: *Verification of Logic Gate Neural Networks*

PhD rotation supervisor at Institute of Science and Technology Austria (ISTA) for Sergei Pankratov, Spring 2025. Project topic: *Certificate-based Neural Control*

PhD rotation supervisor at Institute of Science and Technology Austria (ISTA) for Fabian Kresse, Winter 2024. Project topic: *Predictive Runtime Monitoring for Complex Dynamical Systems*

TEACHING EXPERIENCE

2015-2016, Teaching assistant.
Imperial College London, London, United Kingdom.
Discrete Maths, Reasoning about programs, Logic.

RESEARCH VISITS & OTHERS

June-July 2024, Prof. Joost-Pieter Katoen, RWTH Aachen University, Aachen, Germany.

June-July 2024, Prof. Jürgen Giesl, RWTH Aachen University, Aachen, Germany.

Core contributor to an Intel funded project on certifying hardware model checking, proposed by Prof. Armin Biere.

Member of the ERC project VAMOS; PI: Prof. Thomas A. Henzinger.

Core developer of certificate checkers used for hardware model checking competitions.

Former member of an EPSRC project titled Games and Abstractions, under the supervision of Prof. Chris Hankin at Imperial College London.

ACADEMIC REFERENCES

Prof. Thomas A. Henzinger – `tah@ist.ac.at`
Prof. Armin Biere – `biere@cs.uni-freiburg.de`
Prof. Keijo Heljanko – `keijo.heljanko@helsinki.fi`
Prof. Martina Seidl – `mrtnseidl@gmail.com`

PEER-REVIEWED PUBLICATIONS

Note: the authorship in many publications is alphabetical.

1. Thomas A. Henzinger, Kaushik Mallik, **Emily Yu**, & Đorđe Žikelić. *Control Barrier Functions with Lookahead*. Submitted, 2025.

2. Nils Froleyks, **Emily Yu**, Armin Biere, and Keijo Heljanko. *Certifying Constraints in Hardware Model Checking.* Submitted, 2025.

3. Fabian Kresse, **Emily Yu**, Christoph H. Lampert, and Thomas A. Henzinger. *Logic Gate Neural Networks are Good for Verification.* In International Conference on Neuro-symbolic Systems (NeuS), 2025. **Disruptive Idea Award**

4. Nils Froleyks, **Emily Yu**, Mathias Preiner, Armin Biere, and Keijo Heljanko. *Certifying the Hardware Model Checking Competition.* In Computer Aided Verification (CAV), 2025.

5. Thomas A. Henzinger, Fabian Kresse, Kaushik Mallik, **Emily Yu**, & Đorđe Žikelić. *Predictive Monitoring of Black-Box Dynamical Systems*. Learning for Dynamics and Control Conference (L4DC), 2025.

6. **Emily Yu**, Đorđe Žikelić, & Thomas A. Henzinger. *Neural Control and Certificate Repair via Runtime Monitoring*. In proceedings of the Thirty-Ninth AAAI Conference on Artificial Intelligence, AAAI, 2025. **Selected for oral presentation.**

7. Nils Froleyks, **Emily Yu**, Armin Biere, & Keijo Heljanko. *Certifying Phase Abstraction*. In International Joint Conference on Automated Reasoning (IJCAR), pp. 284-303. Cham: Springer Nature Switzerland, 2024.
   DOI: `https://doi.org/10.1007/978-3-031-63498-7_17`

8. Nils Froleyks, **Emily Yu**, & Armin Biere. *Ternary Simulation as Abstract Interpretation (Work in Progress)*. MBMV 2024, 27. Workshop. VDE, 2024.

9. **Emily Yu**, Nils Froleyks, Armin Biere, & Keijo Heljanko. *Towards Compositional Hardware Model Checking Certification*. In Conference on Formal Methods in Computer-Aided Design (FMCAD), p. 44, 2023.
   DOI: `https://doi.org/10.34727/2023/isbn.978-3-85448-060-0_12`

10. Nils Froleyks, **Emily Yu**, and Armin Biere. *BIG Backbones*. In Formal Methods in Computer-Aided Design (FMCAD), pp. 162-167, 2023.
    DOI: `https://doi.org/10.34727/2023/isbn.978-3-85448-060-0_24`

11. **Emily Yu**, Nils Froleyks, Armin Biere, & Keijo Heljanko. *Stratified Certification for k-induction*. In Conference on Formal Methods in Computer-Aided Design (FMCAD), p. 11. TU Wien Academic Press, 2022.
    DOI: `https://doi.org/10.34727/2022/isbn.978-3-85448-053-2_11`

12. Francesco Belardinelli,Alessio Lomuscio, Vadim Malvone, & **Emily Yu**. *Approximating perfect recall when model checking strategic abilities: Theory and applications*. Journal of Artificial Intelligence Research 73: 897-932, 2022.
    DOI: `https://doi.org/10.1613/jair.1.12539`

13. **Emily Yu**, Armin Biere, & Keijo Heljanko. *Progress in Certifying Hardware Model Checking Results*. In Computer Aided Verification: 33rd International Conference, CAV 2021, Virtual Event, July 20–23, 2021, Proceedings, Part II 33, pp. 363-386. Springer International Publishing, 2021.
    DOI: `https://doi.org/10.1007/978-3-030-81688-9_17`

14. Francesco Belardinelli, Alessio Lomuscio, & **Emily Yu**. *Model Checking Temporal Rpistemic Logic under Bounded Recall.* In Proceedings of the AAAI Conference on Artificial Intelligence, vol. 34, no. 05, pp. 7071-7078. 2020.
DOI: `https://doi.org/10.1609/aaai.v34i05.6193`

15. **Emily Yu**, Martina Seidl, & Armin Biere. *A Framework for Model Checking against CTLK using Quantified Boolean Formulas.* In Formal Techniques for Safety-Critical Systems (FTSCS), Revised Selected Papers 7, pp. 127-132. Springer International Publishing, 2020.
DOI: `https://doi.org/10.1007/978-3-030-46902-3_8`

16. **Zhengqi Yu**, Armin Biere, & Keijo Heljanko. *Certifying Hardware Model Checking Results.* International Conference on Formal Engineering Methods (ICFEM). Cham: Springer International Publishing, 2019.
DOI: `https://doi.org/10.1007/978-3-030-32409-4_32`

TECHNICAL REPORTS

1. Nils Froleyks, **Emily Yu**, & Armin Biere. *Challenging Certificates from Model Checking.* Submitted to SAT Competition 2025.

2. **Emily Yu**, Nils Froleyks, Armin Biere, & Mathias Fleury. *Hardware Model Checking Certificates.* SAT Competition 2022: 56.

3. Nils Froleyks, **Emily Yu**, & Armin Biere. *Unique Reconfiguration Sequence.*
SAT Competition 2022: 64.

4. Nils Froleyks, **Emily Yu**, & Armin Biere. *ReconfAIGERation entering Core Challenge*, 2022.

INVITED TALKS

Leiden University, Leiden, Netherlands — April 2025
Trustworthy Formal Methods for Hardware Design Correctness

Lund University, Lund, Sweden — April 2025
Trustworthy Formal Methods for Hardware Design Correctness

ETH Zürich, Zürich, Switzerland — March 2025
Trustworthy Formal Methods for Hardware Design Correctness

RWTH Aachen University, Aachen, Germany — July 2024
Certifying Phase Abstraction

ETH Zürich, Zürich, Switzerland — January 2018
Model Checking Multi-Agent Systems under Recalls

OTHER PRESENTATIONS

TCS Seminar, Institute of Science and Technology Austria, Austria — November 2023
Towards Compositional Hardware Model Checking Certification

LogiCS Seminar, TU Wien, Austria — May 2023
Towards Compositional Certification for Hardware Model Checking

Int. Conference on Formal Methods in Computer-Aided Design, Trento, Italy — October 2022
Stratified Certification for k-induction

Int. Conference on Computer-Aided Verification (CAV), Virtual — July 2021
Progress in Certifying Hardware Model Checking Results

LogiCS Seminar, TU Wien, Austria May 2020
Increasing Confidence in Model Checking

LogiCS Seminar, TU Wien, Austria January 2020
Model Checking Temporal Epistemic Logic Under Bounded Recall

Int. Conference on Formal Engineering Methods, Shenzhen, China November 2019
Certifying Hardware Model Checking Results

FTSCS Workshop, Shenzhen, China November 2019
A Framework for Model Checking against CTLK using Quantified Boolean Formulas