MIDDLE EAST TECHNICAL UNIVERSITY

EE493 STATIC POWER CONVERSIONS – I

TERM PROJECT SIMULATION REPORT

HAPPY EE FRIENDS

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Introduction

In this project, a DC motor will be driven with an adjustable input of at most 180V. This input is created by a system of a three-phase diode rectifier and buck converter. The simulation results of the topology are discussed in this report in detail, which will be used as a reference during the implementation stages.

Topology Selection

When all the topologies are considered, a 3-phase diode full-bridge rectifier is selected. Single-phase rectifiers are ruled out because of the high output ripple voltage and output voltage loss as seen in Figure 1. Using three-phase will increase the average output voltage and lower the ripples while destroying the third harmonics completely. Three-phase full bridge rectifiers have low values of THD, which means the fundamental component is more dominant over the higher-order harmonics when compared to the single-phase rectifiers. Also, since each thyristor would need a gate driver signal, the resultant system would be very complicated. For the simplicity and advantageous nature of it, a three-phase full bridge diode rectifier topology is chosen. A total of 6 diodes will be used to realize this topology.

Comparison of Rectifiers

Type	Vout	ΔVout	f_{ripple}
Single Phase	$\frac{2\sqrt{2}}{\pi}V_{ph}$ = 207 V	$\sqrt{2}V_{ph} = 325V$	100 Hz
3-phase Half Bridge	$\frac{3\sqrt{2}}{2\pi}V_{l-l}$ = 270 V	$\frac{\sqrt{2}}{2}V_{ph} = 162.5V$	150 Hz
3-phase Full Bridge	$\frac{3\sqrt{2}}{\pi}V_{l-l}$ = 540 V	$(1-\frac{\sqrt{3}}{2})\sqrt{2}V_{l-l} = 75.8V$	300 Hz

Figure 1 Comparison of Various Rectifier Topologies

After the creation of three-phase diode rectifier, the output voltage is utilized to feed the input of the buck converter. The duty cycle of the buck converter is created by the 555 Timer this duty cycle determines the output voltage which is the input to the DC motor. It is required for the output of the buck converter to have at most 180V.

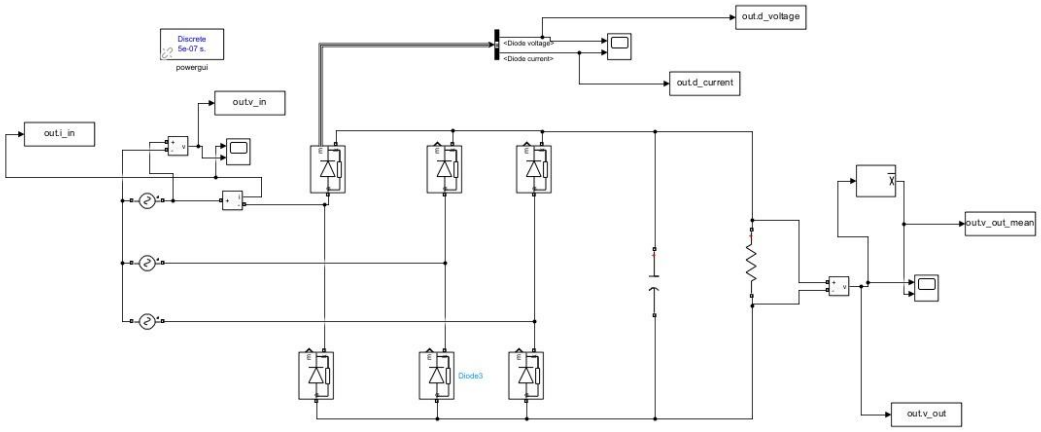

Figure 2 Three Phase Full Bridge Rectifier Topology

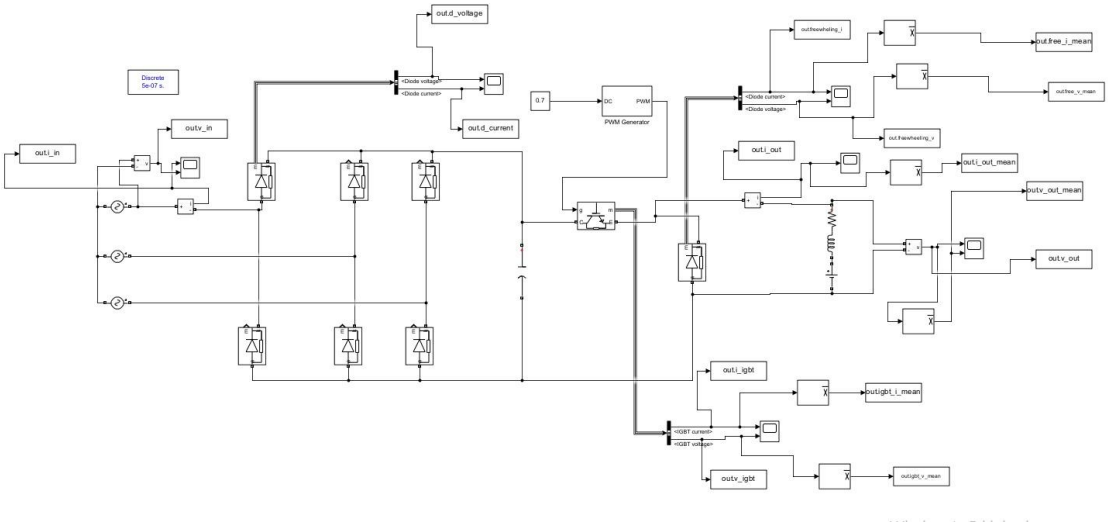

Figure 3 Diode Rectifier and Buck Converter Combined

Simulation Results:

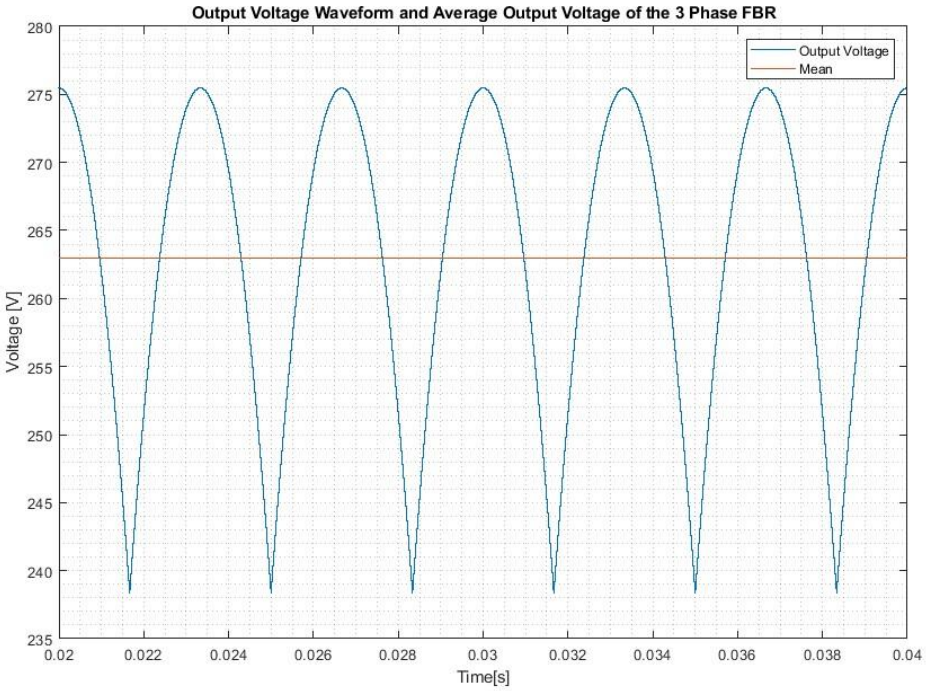

Figure 4 Three Phase Diode Rectifier Output Voltage Waveforms

Starting the simulations, it is decided that the duty cycle of the buck converter would be at most 0.7 because at higher values of duty cycle the non-idealities become more dominant. Considering the output of the buck converter should be at most 180V (input to the DC motor) we have decided to equate the output of the three-phase rectifier to be $\frac{180}{0.7} = 257.1\ V$. In Figure 2, this DC output voltage of the rectifier can be seen. Also to reduce the output voltage ripple of the rectifier, 47 uF of capacitance is placed at the output, however, the dominant filtering effect comes from the motor itself when the DC motor is connected to the rectifier. Since the DC motor is not currently connected to the rectifier, the filtering is not sufficient with a 14.4% ripple.

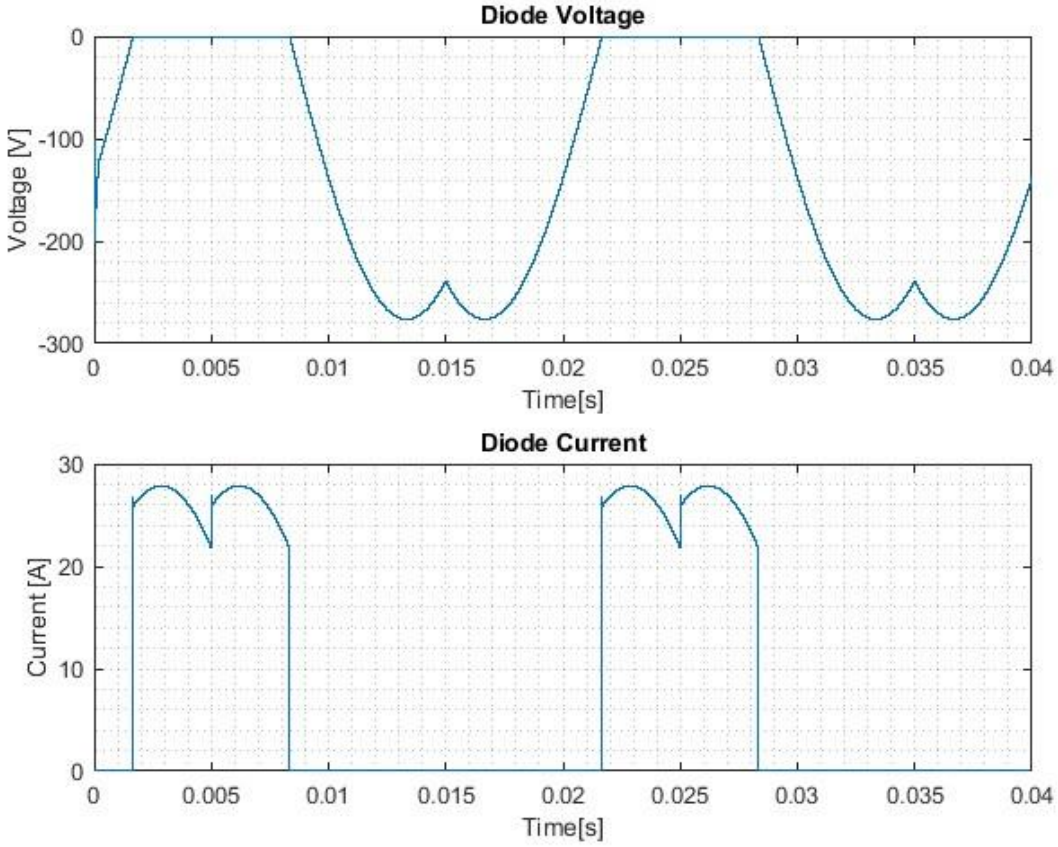

Figure 5 Rectifier Diode Voltages and Currents

The voltage and current on the diodes of the three-phase diode rectifier are shown in Figure 3. The diode components selected for this project are determined by the values of these waveforms. The reverse breakdown voltage of the diodes should be higher than the maximum magnitude of the diode voltage value. Also, the rated current of the diode should be selected according to the mean value of the diode current waveform in Figure 3.

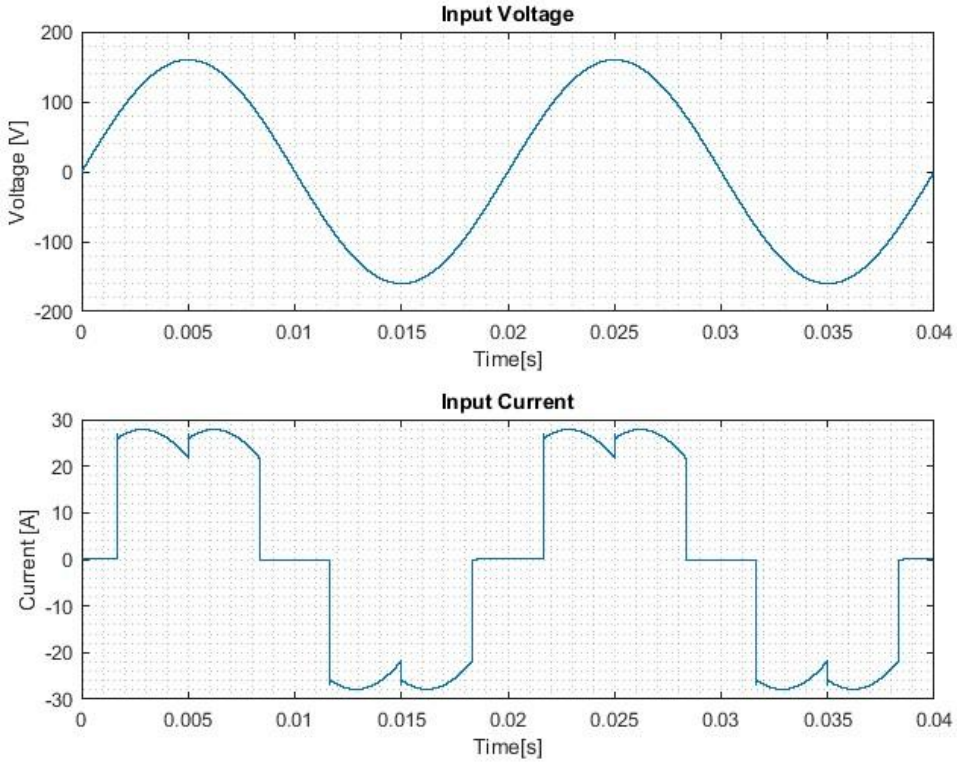

Figure 6 Input Voltage and Current Waveforms of Three Phase Full Bridge Diode Rectifier

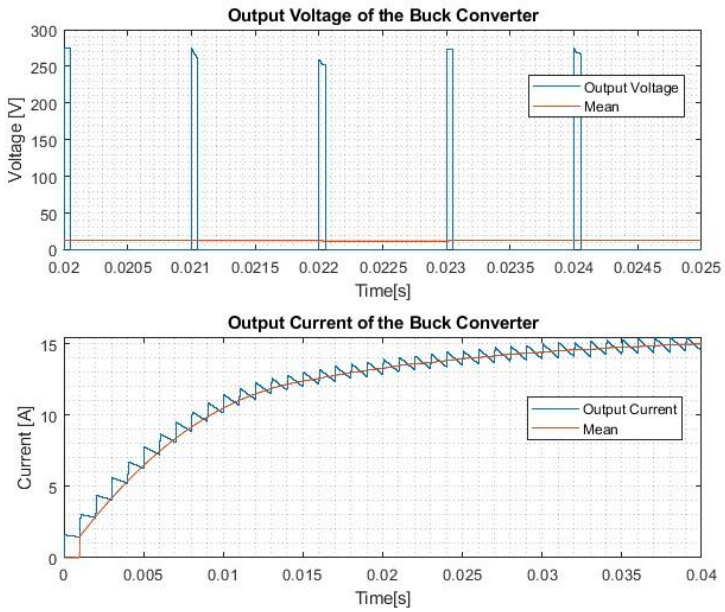

Figure 7 Buck Converter Output Voltage and Current Waveforms When Duty Cycle=0.05

The Buck converter is fed from the diode rectifier and the duty cycle of the converter is decided by the 555 IC Timer. Motor start-up simulation results can be seen in Figures 5, 6, and 7. Throughout the simulation, variac output is assumed to be at its maximum, which is determined as 160Vpeak. The motivation for simulating the start-up case is to determine the maximum drawn current by the DC motor. When the motor is stationary, the back emf of the motor is zero and the voltage only feeds the small resistance of the motor. Since a high output voltage can result in a huge motor current, the duty cycle of the buck converter should be small at the start-up. A smooth start-up will be achieved by smoothly increasing the duty cycle. In this simulation, the duty cycle is set to 0.05, and the back emf of the DC motor is selected as 0.05V.

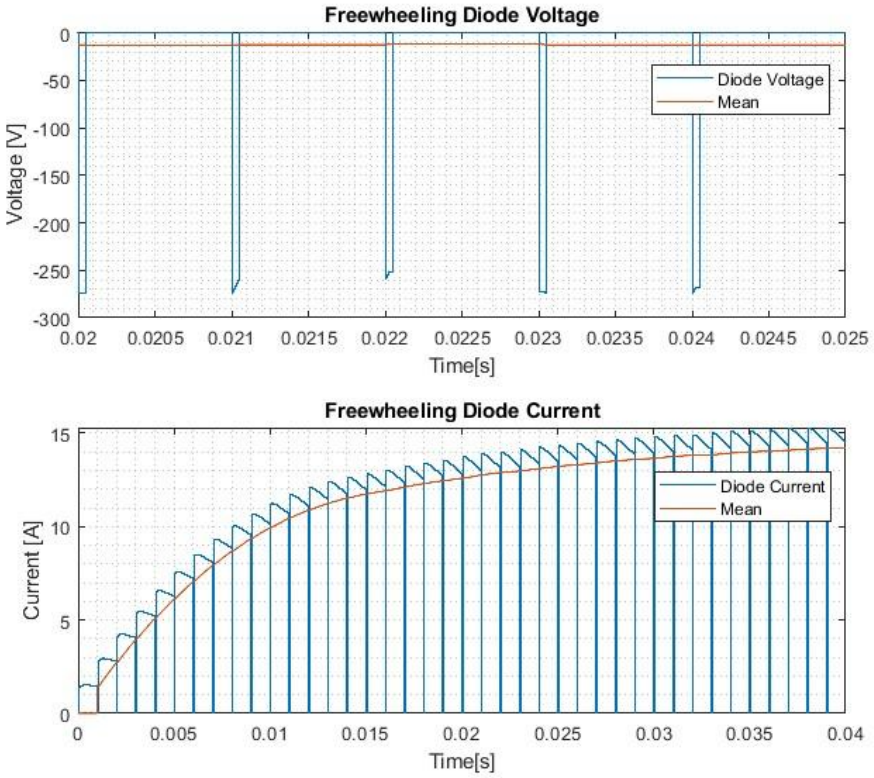

Figure 8 Freewheeling Diode and Current Waveforms When Duty Cycle=0.05

The freewheeling diode provides a path for the inductor (motor) current to circulate when the IGBT is off. This diode will be selected by looking at the mean current value and magnitude of the peak voltage value seen in Figure 6.

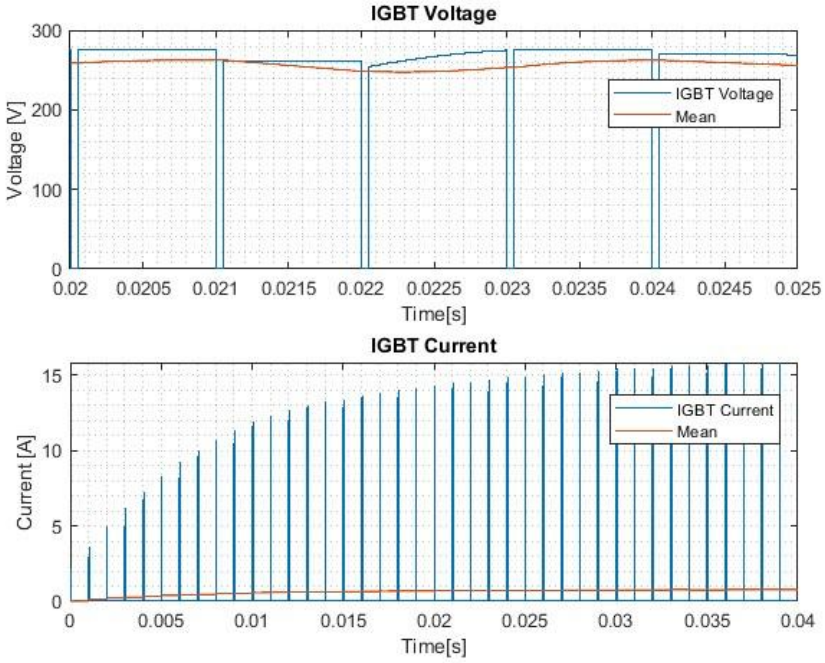

Figure 9 IGBT Voltage and Current when Duty Cycle=0.05

IGBT for this project will be selected according to the values provided in Figure 7.

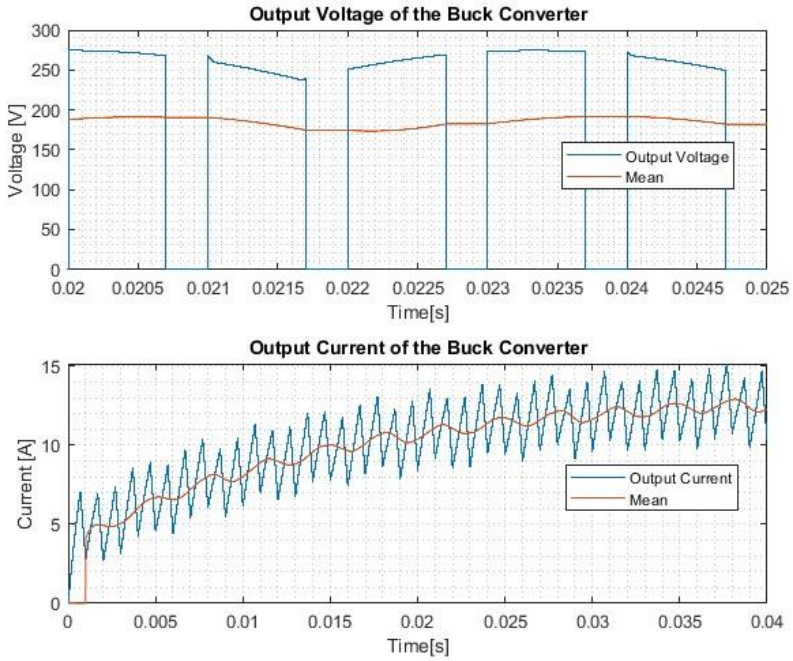

Figure 10 Buck Converter Output Voltage and Current Waveforms When Duty Cycle=0.7

In this part of the simulation, the DC motor is assumed to reach steady state rotation. Motor steady state simulation results can be seen in Figures 8, 9, and 10. The motivation for simulating the steady state case is to determine the operating conditions of the converter. The maximum desired duty cycle for this project is 0.7, thus the operating duty cycle of the buck converter is set to this value. Also, the back emf of the DC motor is set to 172 Volts, to create the required power with 180V buck converter output.

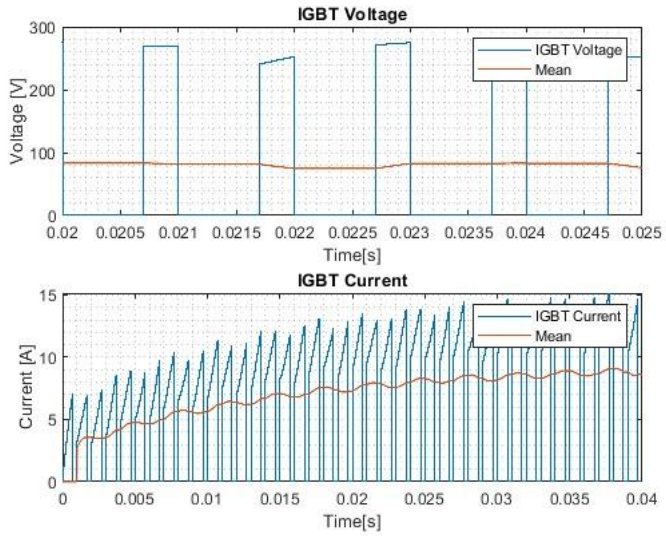

Figure 11 Freewheeling Diode and Current Waveforms When Duty Cycle=0.7

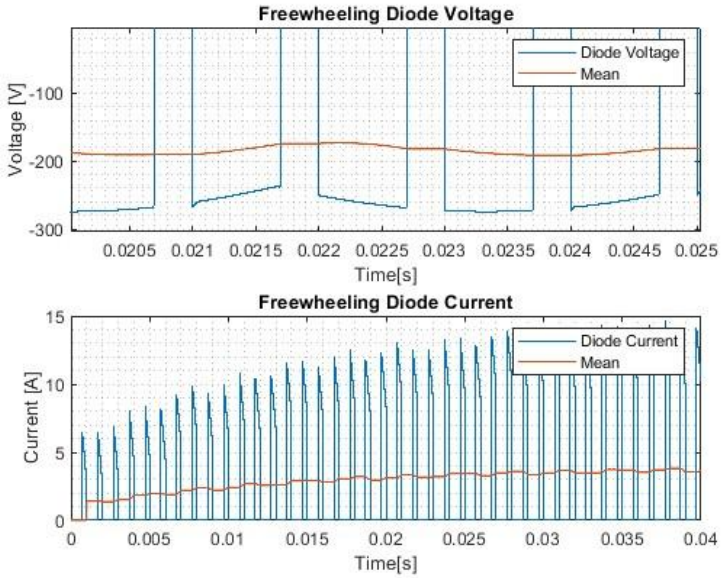

Figure 12 IGBT Voltage and Current when Duty Cycle=0.7

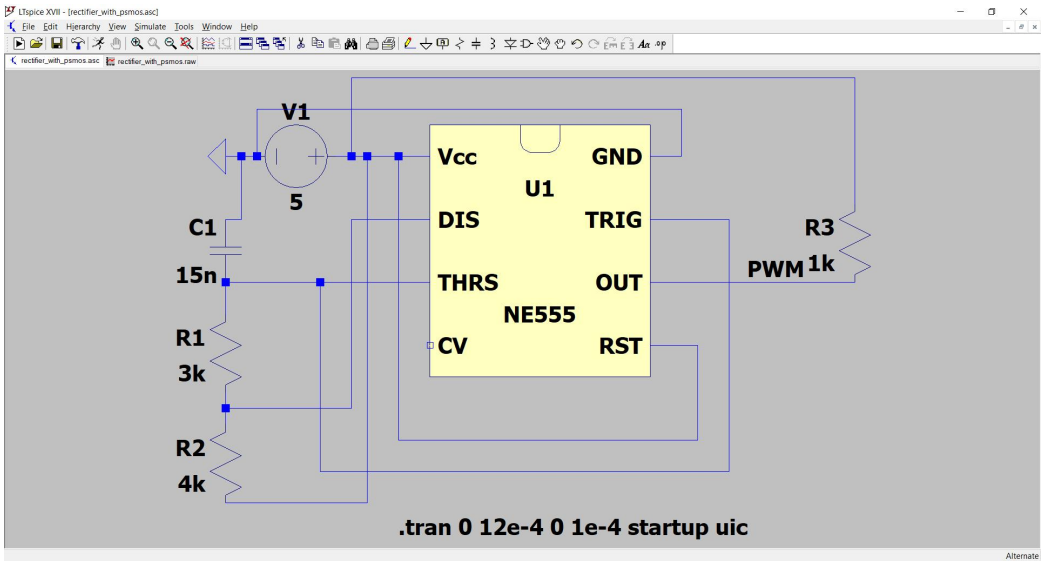

Figure 13 555 IC Timer Topology

PWM signal was achieved with a 555 timer. The corresponding duty cycle of the signal can be calculated as $R_1/(2R_1 + R_2)$. In Figure 13, the resistances were chosen for the duty cycle of 0.7 and the capacitor value was chosen to be 15nF to match the determined 1kHz switching frequency.

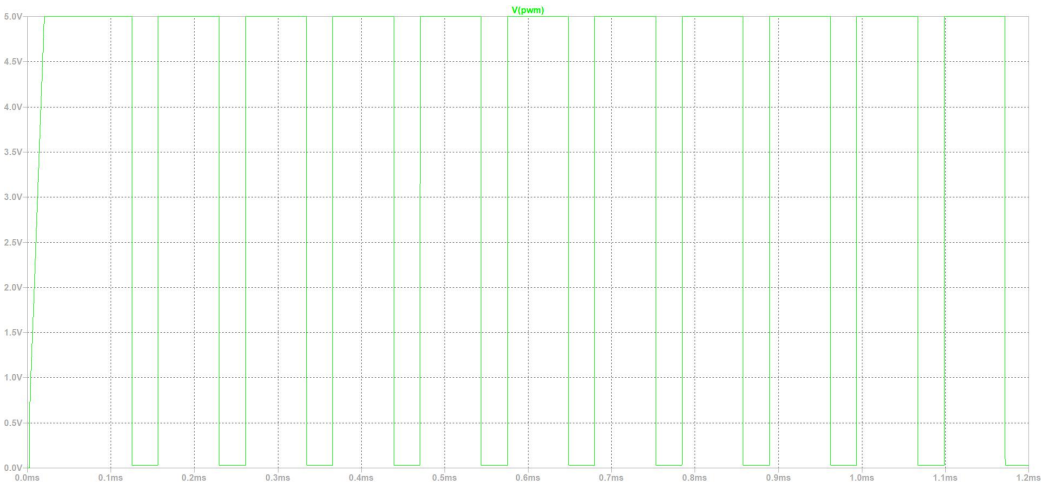

Figure 14 The output of 555 Timer is PWM with 0.7 Duty Cycle

In Figure 14, the generated PWM signal of 0.7 duty cycle at 1kHz can be observed. This signal will be used as input to the gate driver.

Component Selection:

Available components in the laboratory will be mostly used. The selection is based on the constraints of the project. The selected components by looking at the list on GitHub. LM555 Timer is used to create the PWM required for the buck converter. IXGH24N60C4D1 N Channel IGBT Transistor is used as the switch of the buck converter because none of the other components (MOSFETs) in the laboratory have safe margins of rated currents or voltages used in this system. A 25A fuse and fuse holder are chosen as safety. TO220 heatsink is chosen to dissipate the heat produced in the system because of the lossy components. DSEI30-06A diode is used in the full bridge rectifier because of its ability to carry currents up to 37A and block voltages up to 600V. For the freewheeling diode, DSEI8-06A is selected because of the ability to carry currents up to 8A and 600V.

Loss Analysis:

In this system, there are switching and conduction losses of the diodes. Switching losses occur when the switching between on and off states occurs and they are proportional to the frequency of switching, reverse voltage, maximum reverse current, and reverse recovery time. On the other hand, conduction losses occur when the diode is in forward conduction mode and its value depends on forward voltage and forward current values. Both can be formulated as:

$$P_{switching,diode} = 0.5 * f_{switching} * V_{reverse} * I_{reverse\,max} * t_{rr}$$

$$P_{conduction} = V_{forward} * I_{forward}$$

$$P_{switching,6\ diodes} = 6 * 0.5 * 50 * 130 * 50 * 10^{-6} * 50 * 10^{-9} = 48.75\ nW$$

$$P_{conduction,\ 6\ diodes} = 6 * 1.4 * 13 = 109.2W$$

$$P_{switching,freewheeling\ diode} = 0.5 * 1000 * 180 * 10 * 10^{-6} * 10^{3} * 10^{-9} = 45\ nW$$

$$P_{conduction,\ freewheeling\ diode} = 1.3 * 3 = 3.9W$$

Losses of IGBT can be formulated as:

$$P_{conduction,IGBT} = V_{CE,SAT} * I_{CE} = 3.9W$$

$$P_{switching,IGBT} = E_{switching} * f_{switching} = 1.46W$$

$$P_{conduction,IGBT} = 1.5 * 8 = 12W$$

$$P_{switching,IGBT} = 2.1 * 10^{-3} * 10^{3} = 2.1W$$

Discussion

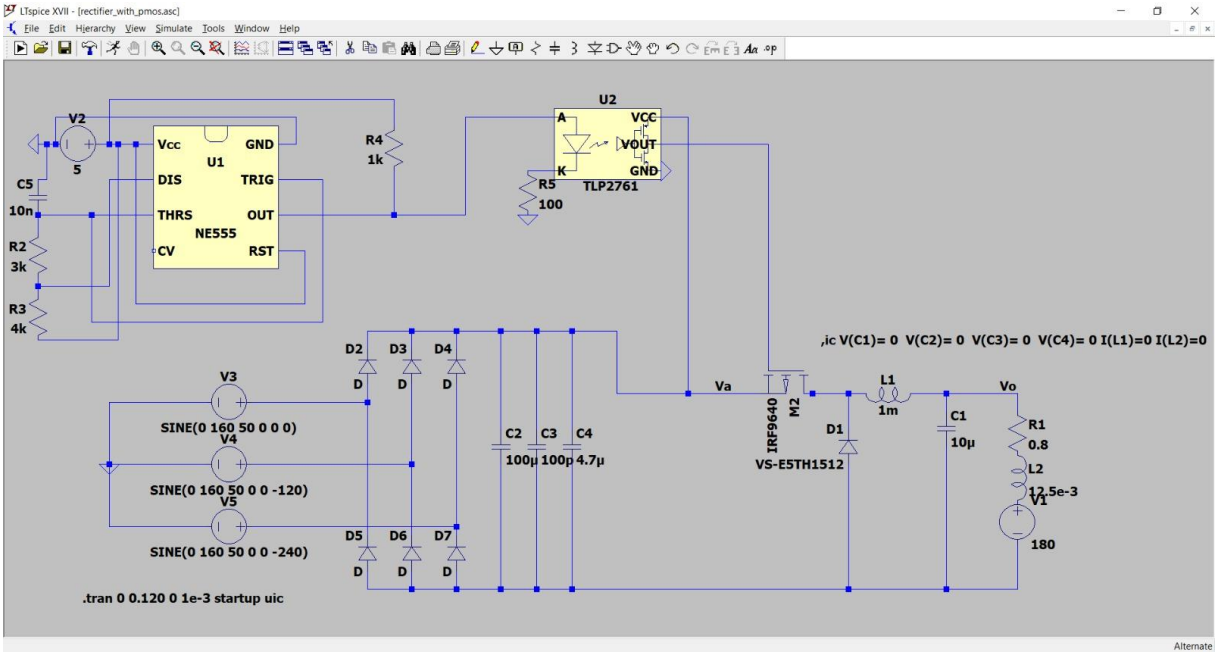

Figure 15 Alternate topology proposal including analog controller

The output of the 555 timer will be connected to a gate driver. The gate driver of choice was from the recommendation sheet which is TLP250, and we tried to make it function properly with an NMOS. We couldn't achieve proper switching with NMOS which led to a swap with a PMOS. This change allowed the gate signal to be driven properly and desired 180V was measured at the terminals of the equivalent armature of the motor.

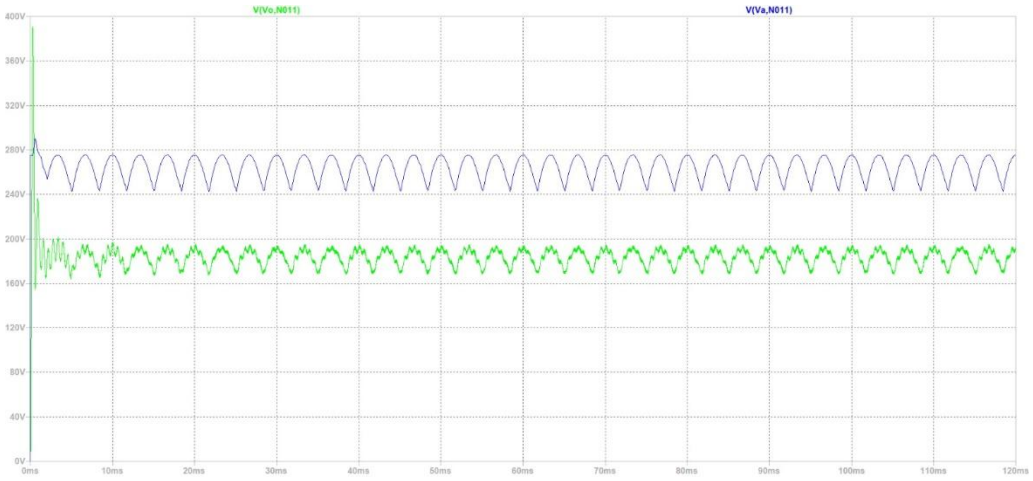

Figure 16 Voltage Waveforms with 0.7 Duty Cycle

Conclusion

In this report, the proposed design for the AC-DC converter for the term project is elaborated with the simulations of the design in Simulink and LTSpice software. In the simulation results, the operating conditions for each component of the converter were obtained, and the component selection was done in consideration of these obtained conditions. Moreover, the power losses were carefully calculated considering the maximum given parameters in the datasheets, which allows a safety measure for future thermal design.

References

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Appendix

[1] https://cdn.ozdisan.com/ETicaret_Dosya/2819_46942.pdf

[2] https://cdn.ozdisan.com/ETicaret_Dosya/2824_9316443.pdf

[3] https://pdf.direnc.net/upload/ixgh24n60c4d1-datasheet.pdf