

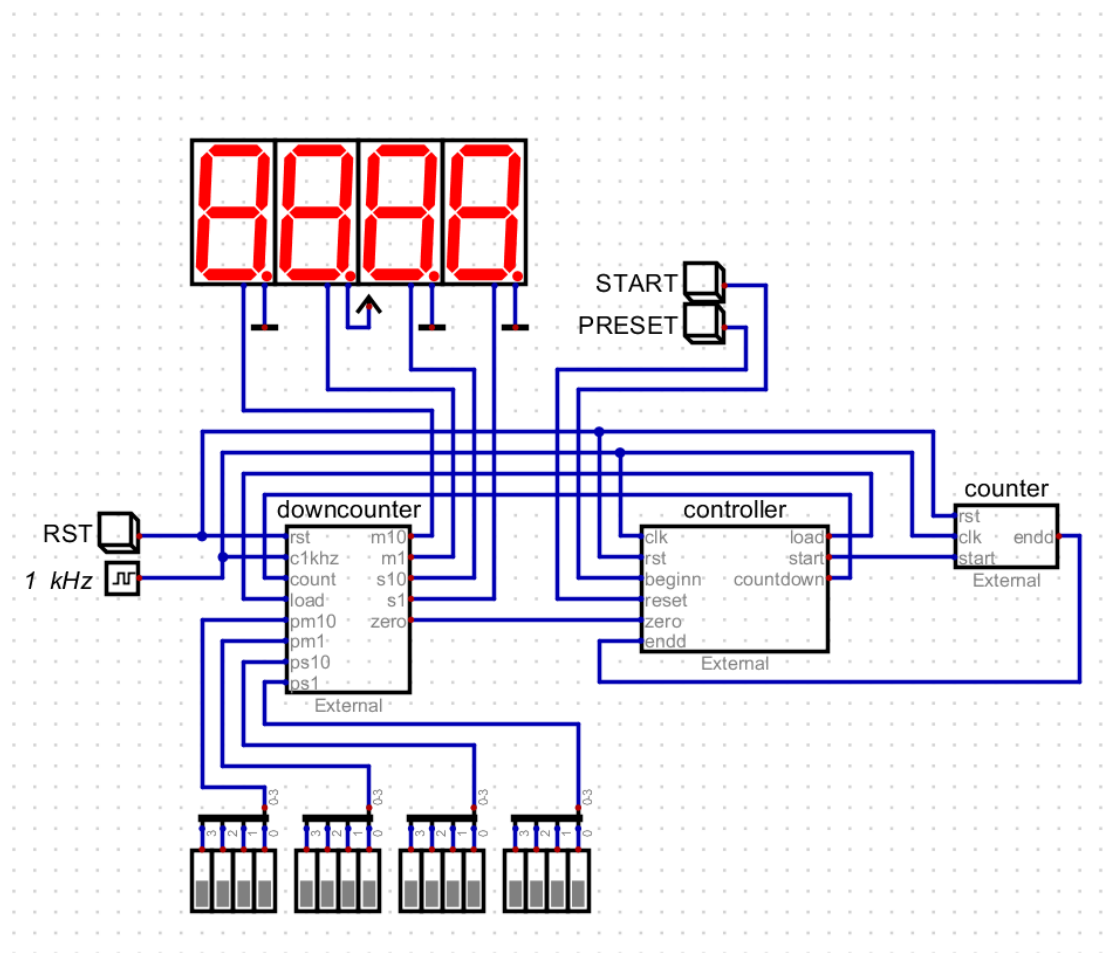
CS 303 LOGIC AND DIGITAL SYSTEM DESIGN PROJECT REPORT

**TOPIC: EGG TIMER
CONSTRUCTION**

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1- OBJECTIVE AND DESCRIPTION OF PROJECT

The purpose of this project is to determine the time to be kept by the user with the input keys, and to count down from this time until it reaches zero. In order to determine the numbers, 4 switches, consisting of 4 groups, were placed. After users enter the time they want to these switches, they must press the preset button to load the time into the counter. After that, they should start the counter by pressing the start button. If they want to reset the counter, they must press the reset button.



2- THE COMPONENTS OF DIGITAL DESIGN

- **DOWN COUNTER**

In this part, we have created a Verilog code that will count backward from the specified number (that was decided by the user) to zero. Firstly, it will upload the numbers that were entered. If the user pressed RST button it will directly turn into zero. Otherwise, if the clock is ticking and the number on the display is not equal to 0, it will start to count. The code is written so that each digit is reduced by 1 when the other digits are equal to zero before a particular digit. Likewise, it is ensured with this code that it does not return to F after being 0.

- **CONTROLLER**

In this section, we made it possible to start counting by just pressing the start button. When user pressed start button, it will make countdown variable as 1 which starts counting. If user press RST button, countdown will go back to zero. Also, after user enter the time input, user should press the PRESET button since in the controller

part PRESET is assigned to LOAD which shows the entered number.