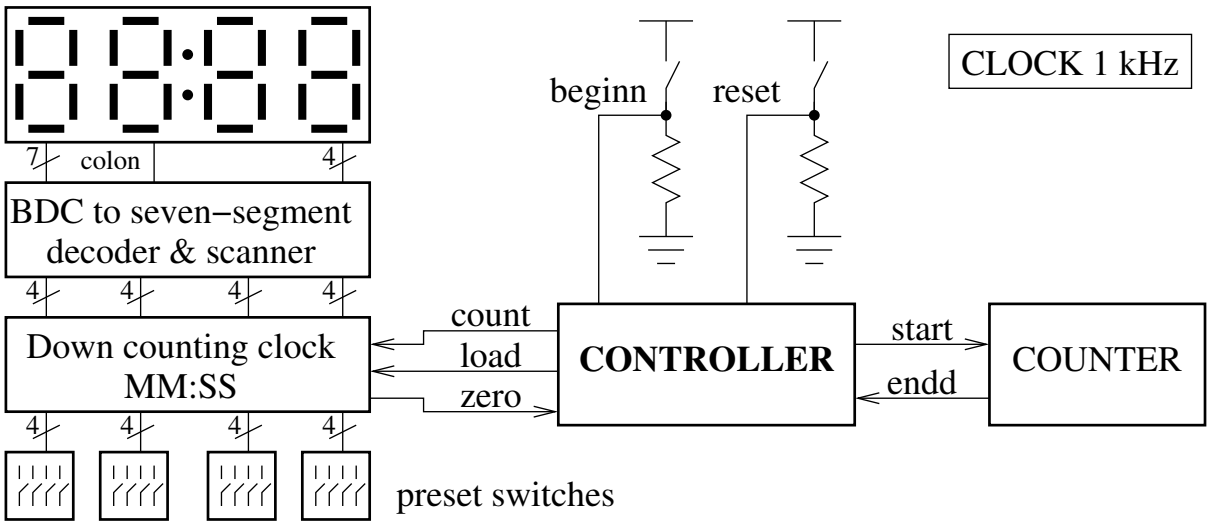
CS 303 Logic and Digital System Design Assigned : 30/05/2022
Laboratory Assignment #06 Demo : TBA

An Egg Timer

We would like to design an egg timer. The circuit will utilize an extended the previously designed 2-digit BCD downcounter to incorporate minutes. A state machine labeled CONTROLLER will be designed to sequence the events, as shown in the figure.



When the button labeled "reset" is pressed, the controller is expected to load the preset value to the downcounter, which is determined by the switches of the FPGA board. These switches will be grouped as four 4-bit blocks to input the initial timer setting as BCD digits, which might go up to 99:59. The countdown is to start immediately once "beginn" is pressed, and stop at 00:00. All FFs of the design will receive a clock of frequency 1 kHz. The controller will utilize another counter to make the timer to proceed in 1 s steps; this counter will be started by "start", and should signal the controller by the signal "endd" to indicate that a certain number of clock ticks have been counted. The exact number depends on the structure of the state machine of the controller.

Design the controller as an algorithmic state machine. Prepare a document describing its design. You may design the downcounter by extending your previous schematic entry in *Digital*, or writing it from scratch in Verilog. You are already provided with the display driver.

Demo

During next week's laboratory sessions, you may test your design on the Nexys A7 boards. The actual demo might be done later (the time and location of which will be announced.)

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