SW Implementation

Introduction

The purpose of this lab is to design a circuit that creates the desired voltage waveform in Figure 1, the design should be built by OPAMPs and RC circuits.

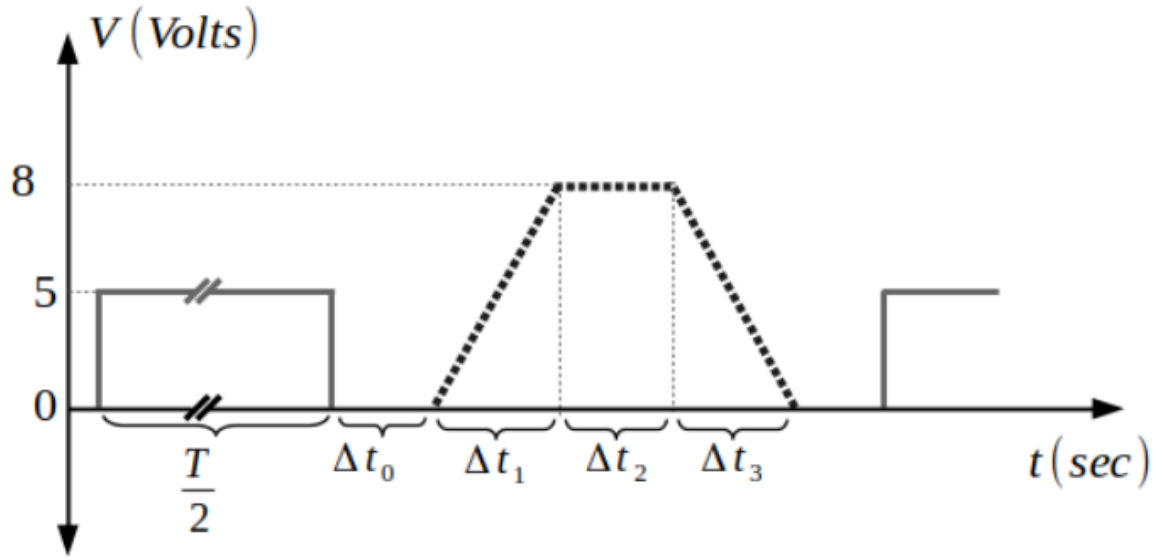

Figure 1: Desired Output (dashed)

It is specified that time intervals 0, 1 and 3 should be 2 ms, and the 2nd one should be 3 ms. The output voltage should be 8 Volts and the chosen frequency for this lab is 20 Hz. The solution is made up of a circuit that involves two delay creating circuits, two integrator circuits and one subtractor circuit for obtaining the desired time interval values by subtracting one delayed and later integrated signal from one another.

Analysis

In order to obtain a delayed trapezoid signal of desired period, three types of circuitry is necessary, delay, integrator and subtractor. The input pulse signal becomes delayed twice as 2 ms and 7 ms, they both get integrated to obtain the trapezoid shape, and these signals get subtracted in order to obtain the final desired signal.

For creating the 2 ms and 7 ms delayed signals, a comparator OPAMP is used and a reference voltage of 2.5 V is placed at the negative input for comparing the low and high parts of the input signal. There is an RC circuit connected to the positive input, and this is for creating the desired time intervals. The output is decided by the saturation of the OPAMP, if the voltage at the positive input is larger than the comparator voltage of 2.5 V, the output becomes Vcc+,

being chosen as 9.5 V for this lab as the OPAMP gets to the positive saturation region. Likely, it becomes 0 V when the input voltage is less than 2.5 V as the OPAMP gets to the negative saturation region.

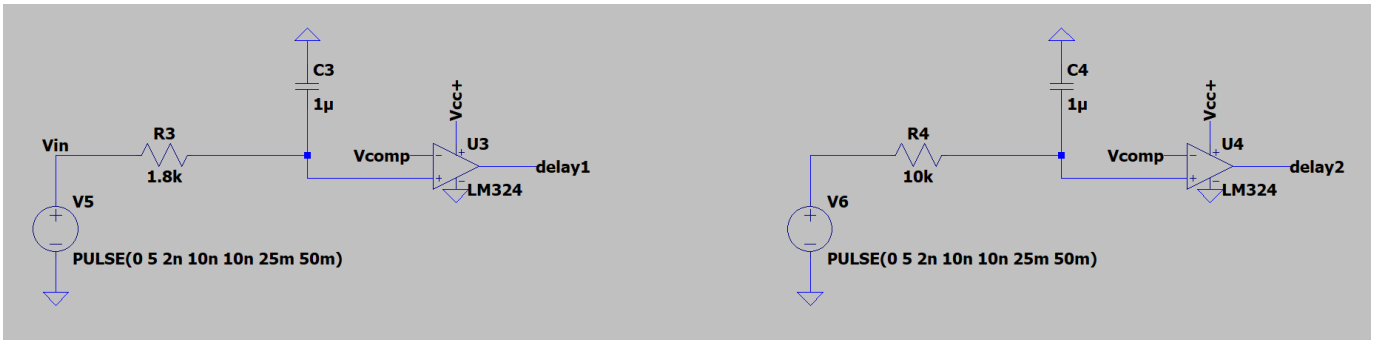

Figure 2: Delay Circuits

In order to find the R and C values in both circuits, node analysis is necessary. At the + input:

$$\frac{dv_c}{dt} * C + \frac{v_c - v_{in}}{R} = 0 \tag{1}$$

$$\frac{dv_c}{dt} + \frac{v_c}{RC} = \frac{v_{in}}{RC} \tag{2}$$

The characteristic equation of (2) can be found as:

$$r + \frac{1}{RC} = 0 \;\; => \;\; r = -\frac{1}{RC} \tag{3}$$

This makes the natural and forced responses:

$$V_{c,natural} = A_1 * e^{-\frac{t}{RC}} \;\; , \;\; V_{c,forced} = V_{in}$$

Making the total of Vc as (4) since at t=0 the capacitor voltage is 0, and the inputted voltage's high value is 5V.

$$V_c = -5e^{-\frac{t}{RC}} + 5 \tag{4}$$

Using (4), since at 2 ms and 7 ms Vc should be equal to comparator voltage of 2.5 V, the R1 times C1 and R2 times C2 values can be found.

$$2.5 = -5e^{-\frac{t}{RC}} \quad => \quad e^{-\frac{t}{RC}} = 0.5$$

(5)

For t = 2 ms R1 times C1 equals 0.00288, and for t = 7 ms R2 times C2 equals 0.01009. The values that satisfy these values are found as:

$$R_1 = 1.8\,k\Omega \;, \quad R_2 = 10\,k\Omega$$

$$C_1 = 1\,\mu F \;, \quad C_2 = 1\,\mu F$$

Later, the integrator circuits are implemented as in Figure 3. Again, node analysis is conducted to find R and C values, this time at the negative input of the OPAMP.

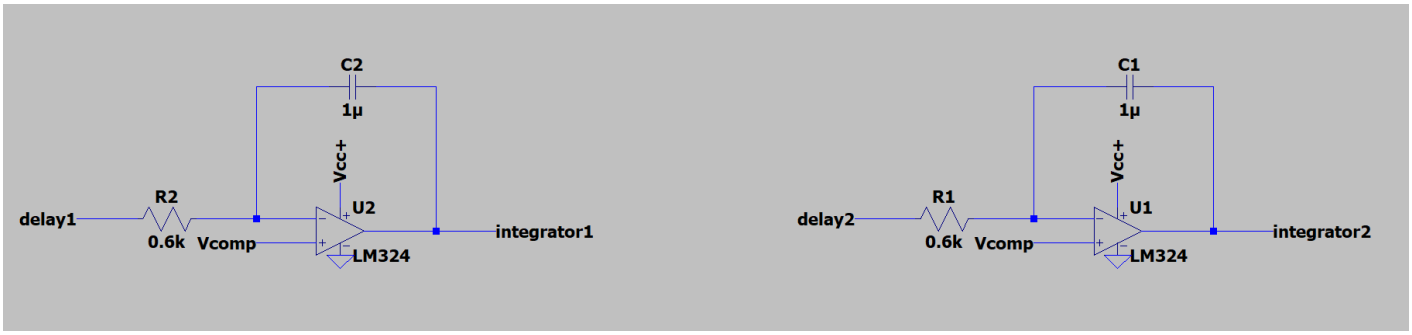

Figure 3: Integrator Circuits

$$\frac{dv_c}{dt} * C + \frac{v_- - v_{in}}{R} = 0$$

(6)

Since the OPAMP is in linear region, plus and negative terminals are equal.

$$\frac{dv_c}{dt} = \frac{v_{in} - v_+}{R} \quad => \quad \int \frac{v_{in} - v_+}{R} dt = v_c \quad => \quad v_c = \frac{v_{in} - v_+}{R} * t + B, B \in R$$

(7)

Since Vc is 0 at t=0, B can be found as 0. So, Vc can be written as:

$$v_c = \frac{v_{in} - v_+}{R} * t \quad => \quad v_c = \frac{2.5}{RC} * t$$

(8)

Since at 2 ms Vc should equal 8 V:

$$8 = \frac{2.5}{RC} * 2 * 10^{-3} \quad => \quad R * C = 0.000625$$

Trial and error gives the following values:

$$R = 0.6\ k\Omega, C = 1\ \mu F$$

The values of R and C are equal for both signals coming from delay circuits, since the desired time intervals for the increase and decrease of the trapezoid are equal for both signals.

Lastly, a subtractor circuit as in Figure 4 is necessary for obtaining the desired value for the constantly high section of the trapezoid. Node analysis at the positive and negative inputs of the OPAMP gives (9) and (10).

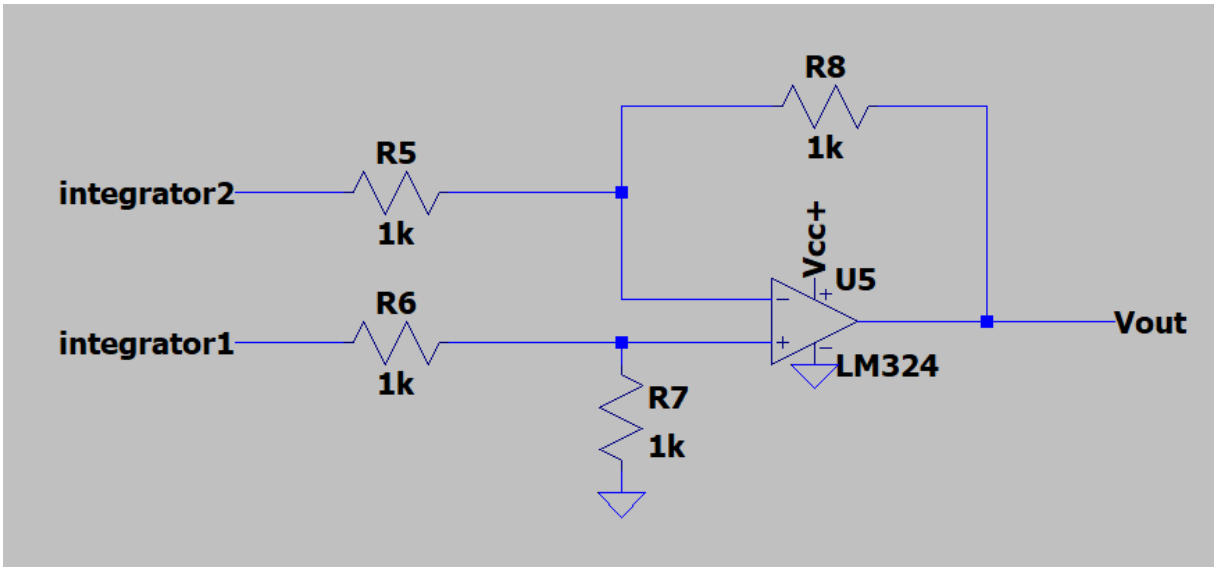

Figure 4: Subtractor Circuit and Final Output Signal

At the positive input of the OPAMP:

$$-\frac{V_{integrator1} - V_+}{R_7} + \frac{V_+}{R_7} = 0 \quad => \quad V_- = \frac{V_{integrator1}}{R_6(\frac{1}{R_6} + \frac{1}{R_7})} \tag{9}$$

At the negative input of the OPAMP:

$$\frac{V_- - V_{integrator2}}{R_5} + \frac{V_- - V_{out}}{R_8} = 0 \quad => \quad V_- = \frac{\frac{V_{integrator2}}{R_5} + \frac{V_{out}}{R_8}}{\frac{1}{R_5} + \frac{1}{R_8}} \tag{10}$$

Assuming the OPAMP to be in the linear region:

$$\frac{V_{integrator1}}{R_6(\frac{1}{R_6} + \frac{1}{R_7})} = \frac{\frac{V_{integrator2}}{R_5} + \frac{V_{out}}{R_8}}{\frac{1}{R_5} + \frac{1}{R_8}} \tag{11}$$

One can observe that choosing all R values to be equal reduces to equation to (12).

$$V_{out} = V_{integrator1} - V_{integrator2}$$

1 kΩ is chosen for all resistors in this implementation.

Simulations

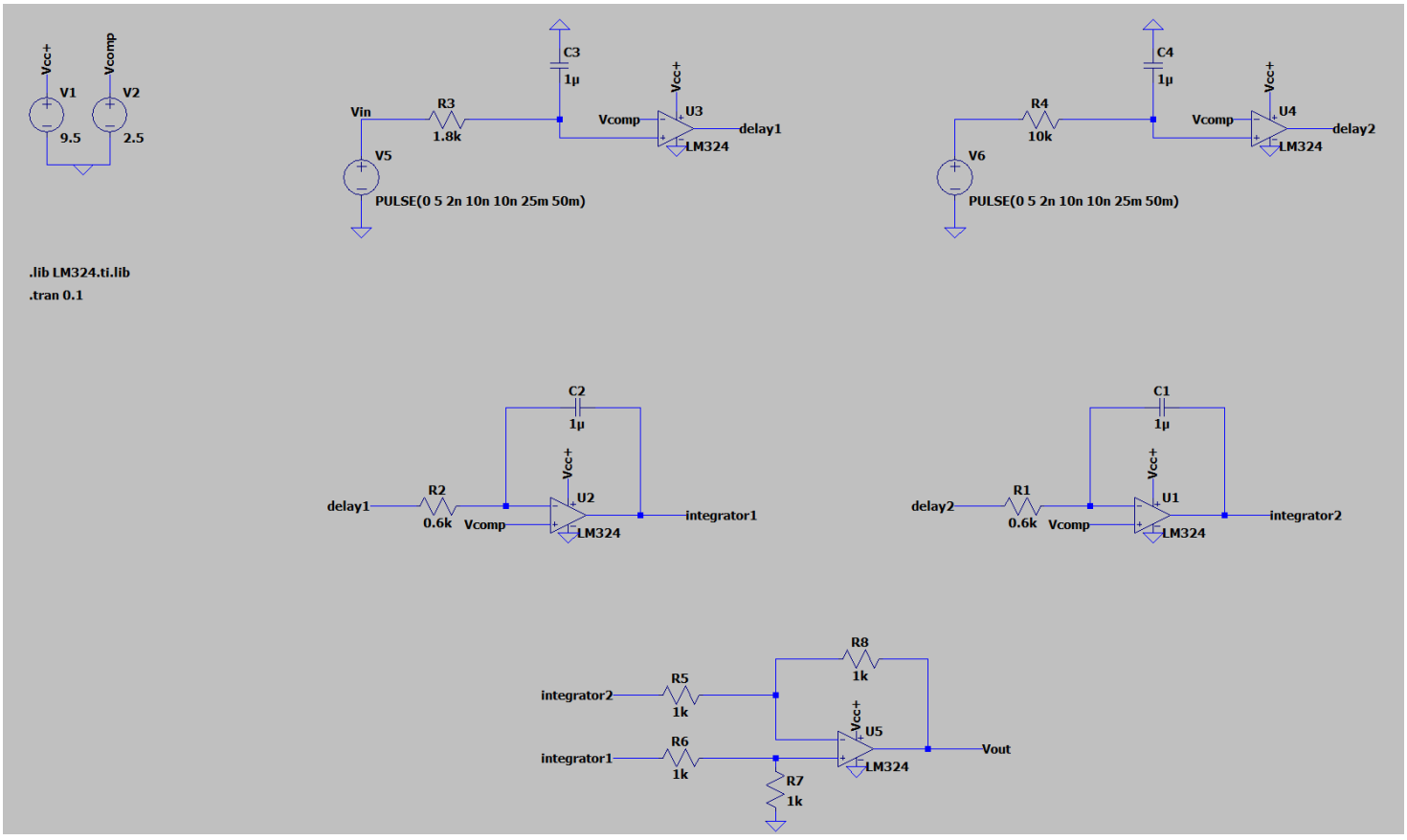

Figure 5: Final Implementation

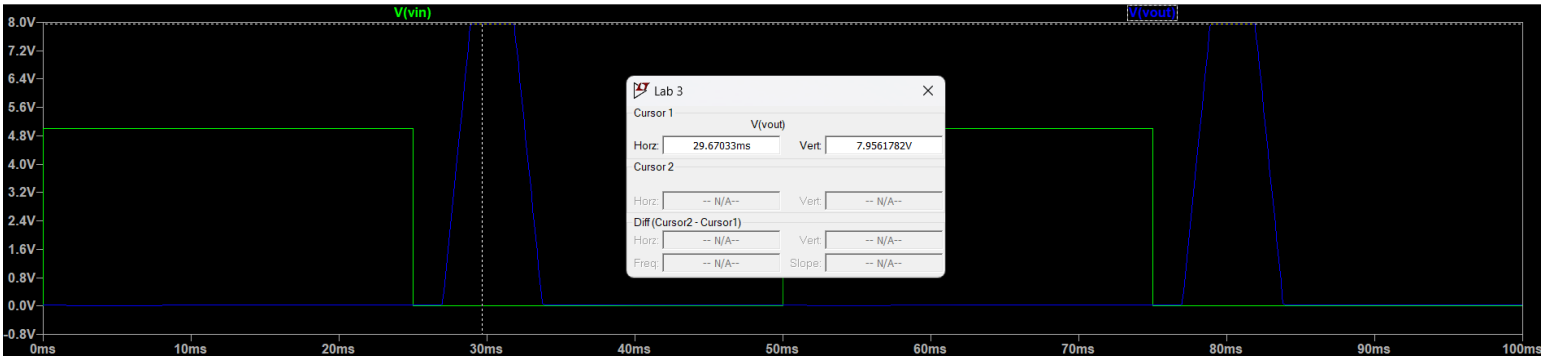

Figure 6: Total Output of the Circuit

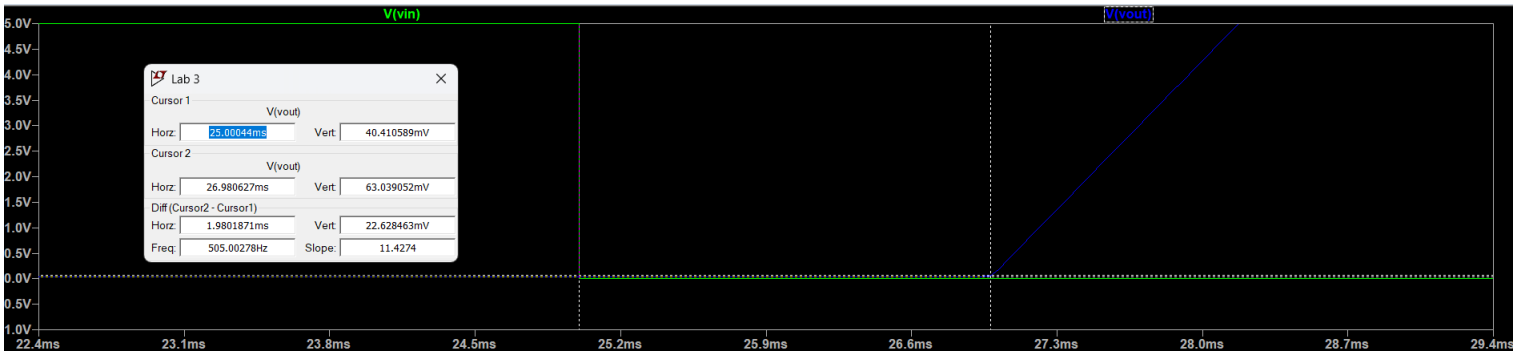

Figure 7: First Time Interval is 1.98 ms

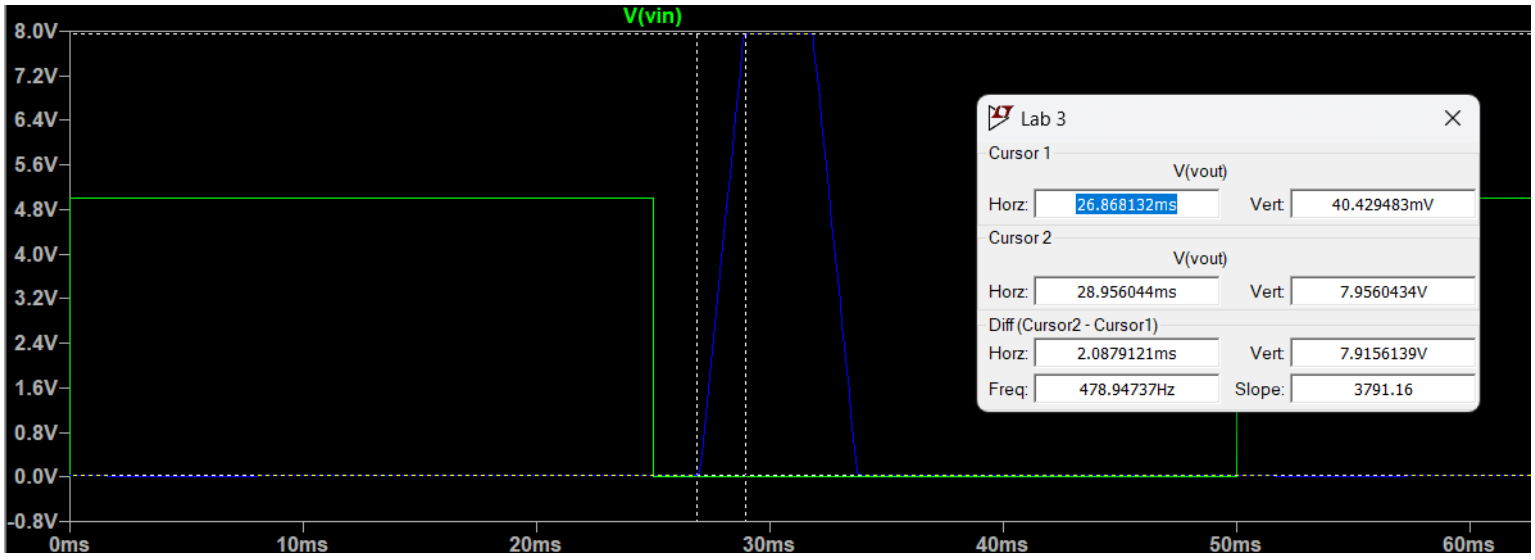

Figure 8: Second Time Interval is 2.09 ms

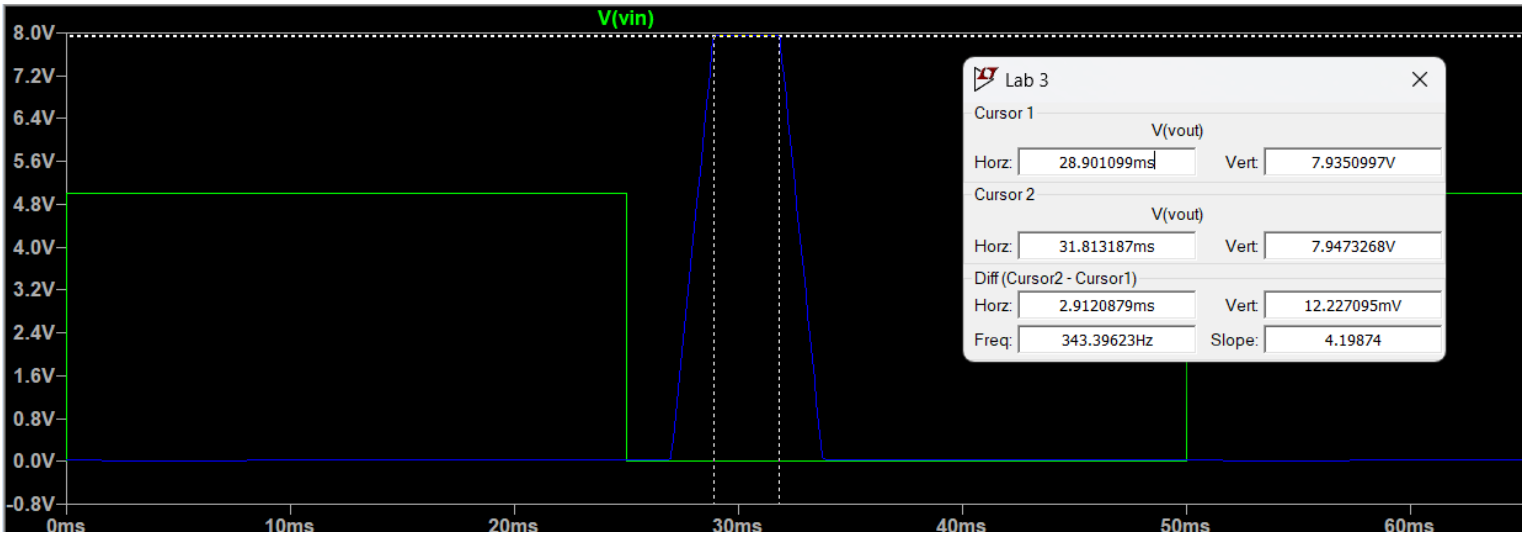

Figure 9: Third Time Interval is 2.91 ms

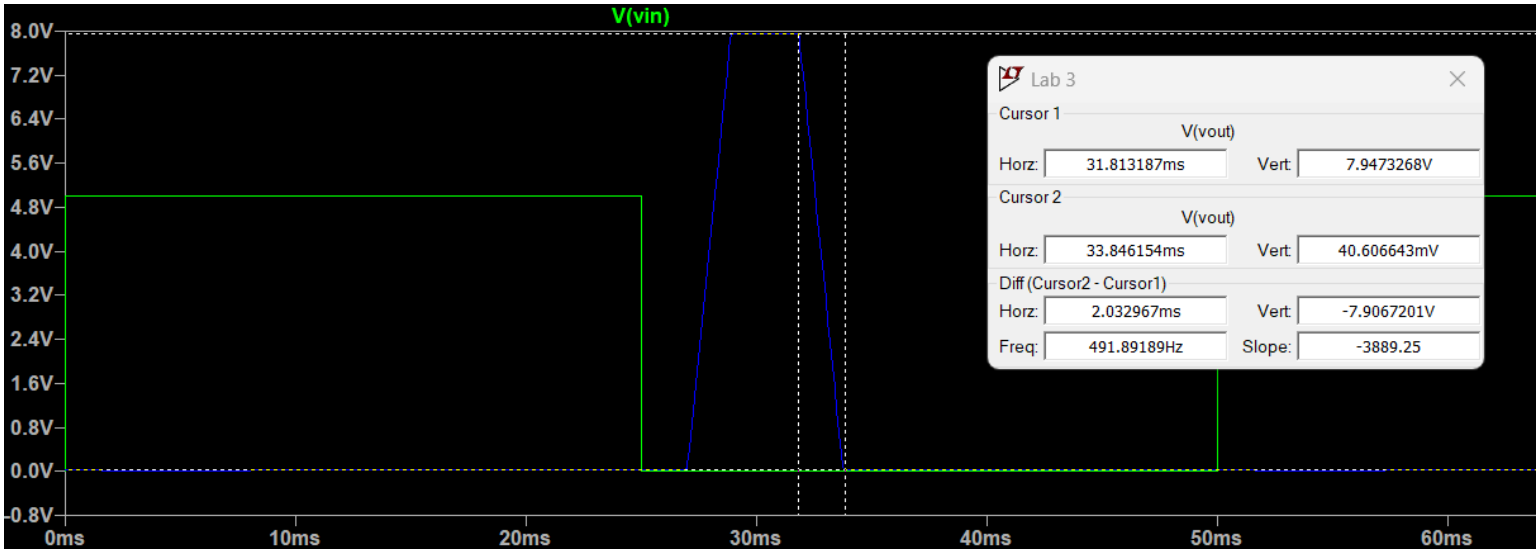

Figure 10: Fourth Time Interval is 2.03 ms

Figure 11: First Delay Circuit

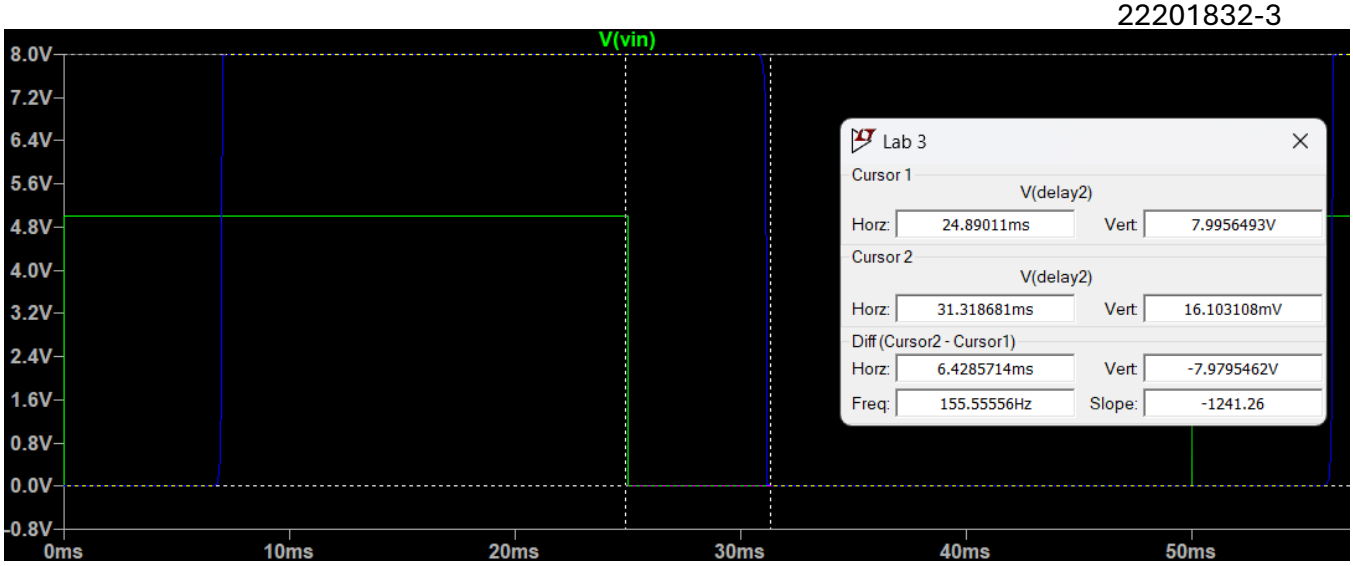

Figure 12: Second Delay Circuit

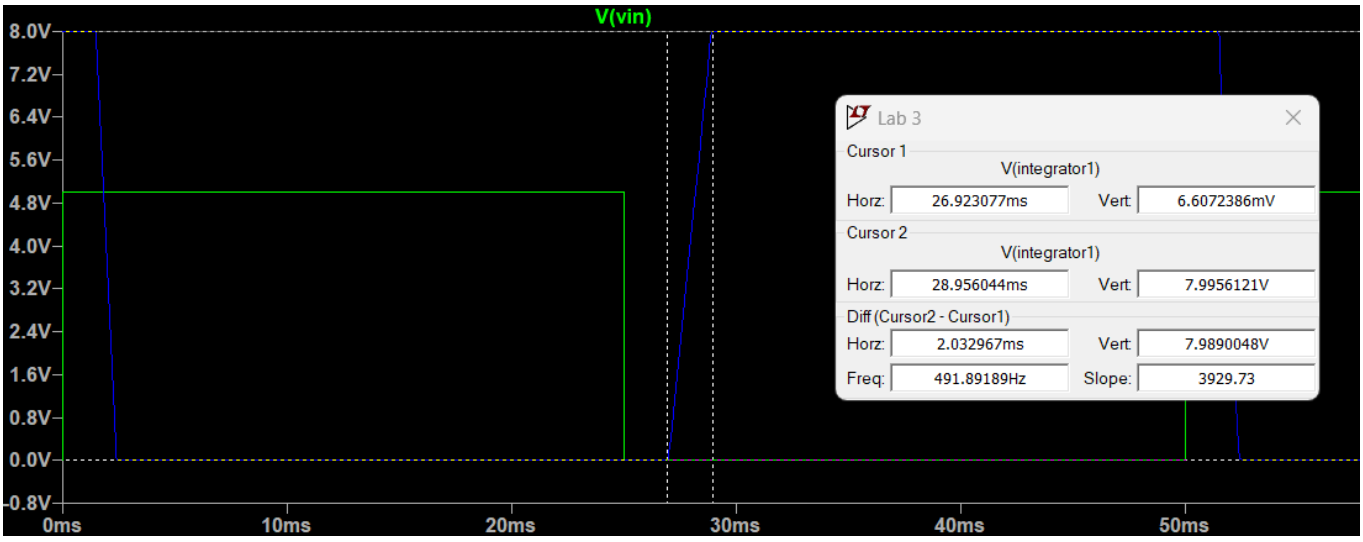

Figure 13: First Integrator Circuit

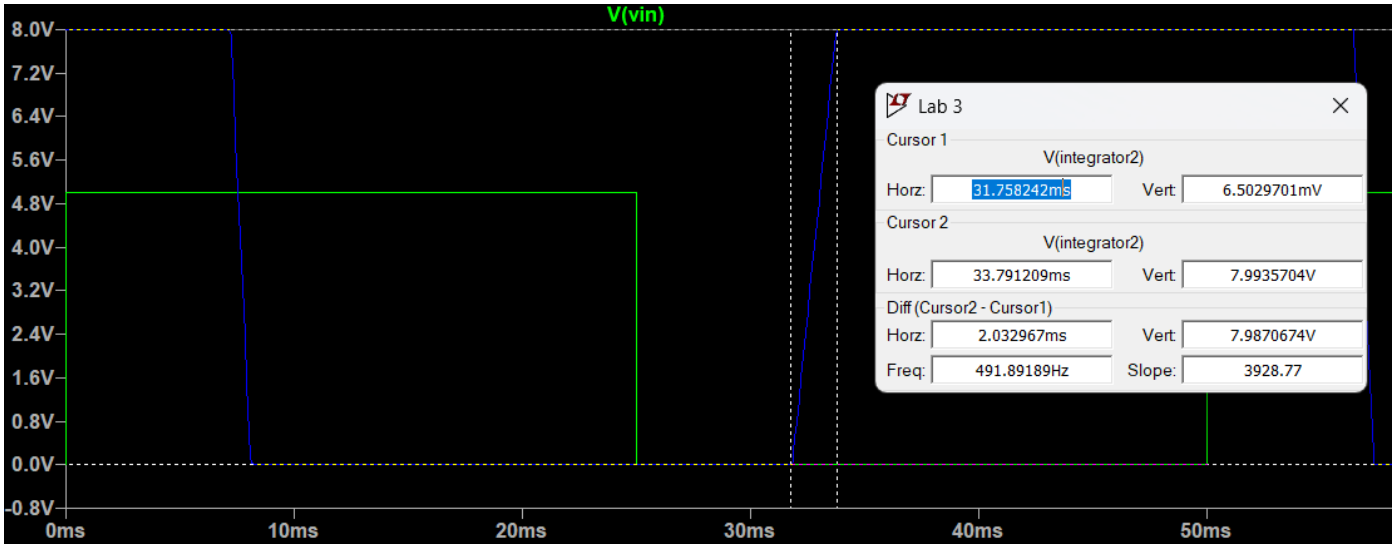

Figure 14: Second Integrator Circuit

	Δ_{t_0}	Δ_{t_1}	Δ_{t_2}	Δ_{t_3}	Maximum Output Voltage
Desired Value	2 ms	2 ms	3 ms	2 ms	8 V
Simulated Value	1.98 ms	2.09 ms	2.91 ms	2.03 ms	7.96 V
Error Percentage	-1%	4.5%	3%	1.5%	-0.5%

Table 1: SW Implementation Results

There was a slight extra error on the delay circuits that does not impact the total output voltage time intervals, as their values were changed to balance the inner delay of the integrator circuit.

HW Implementation

In the hardware implementation of the lab, two LM324 OPAMPs are used that each involve 4 inputs for implementing the total 5 circuits of delay, integrator and subtractor. The DC power supply gives Vcc+ input the value 9.5 V, and Vcc- is 0V. Figure 15 displays the design of the circuit.

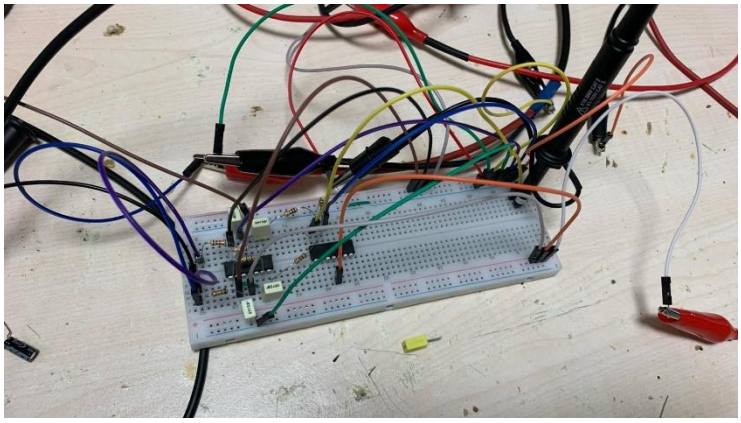

Figure 15: Implemented Design

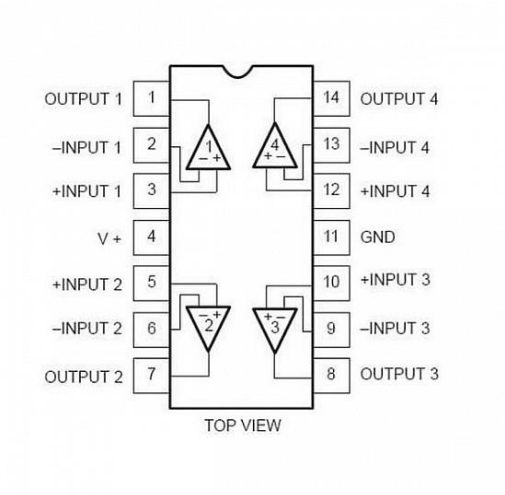

Figure 16: Pin Diagram of LM324

The inputted voltage is a 0V to 5V pulse wave that has 20 Hz frequency, and there is a 1.25 V offset for obtaining this voltage. Comparator voltage has the value of 2.5 V.

Figure 17: Input Frequency

Figure 18: Input Peak to Peak Voltage

Figure 19: Input Voltage Offset

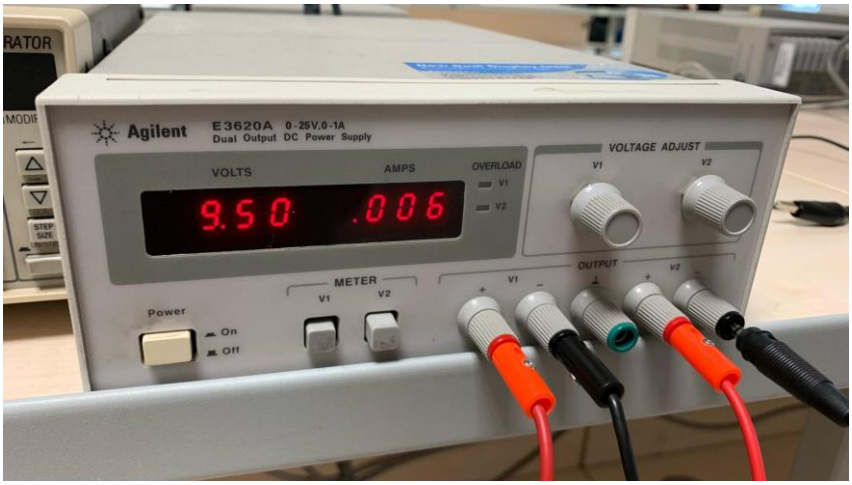

Figure 20: Vcc+

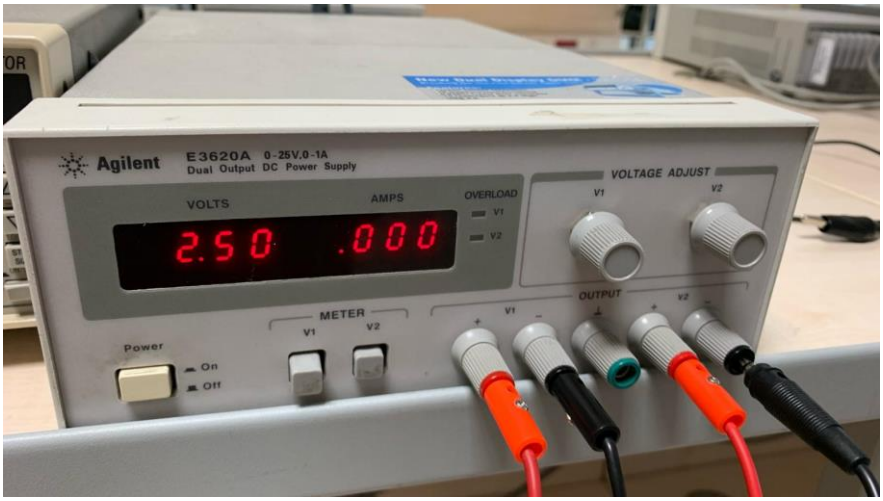

Figure 21: Comparator Voltage

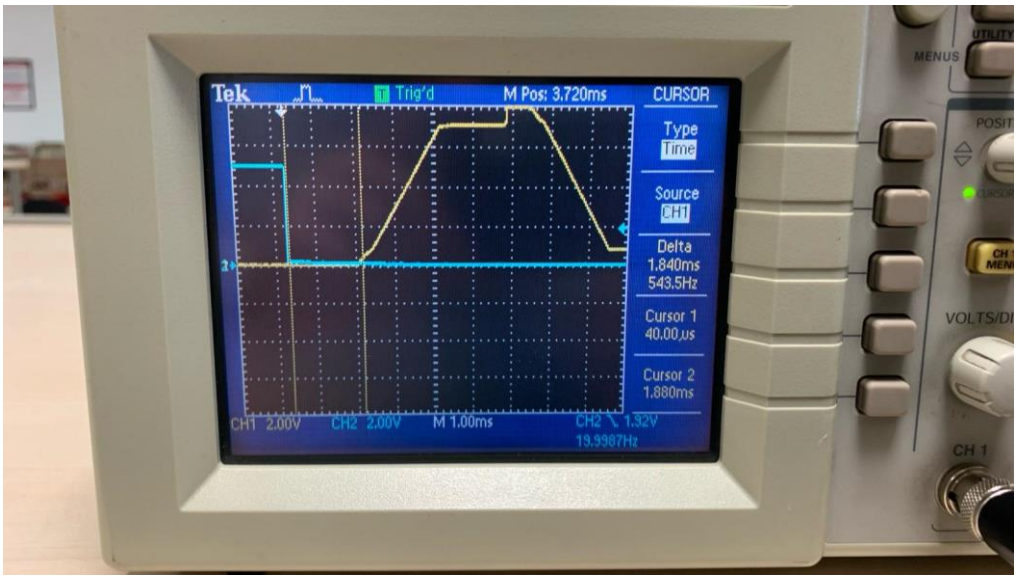

Figure 22: First Time Interval

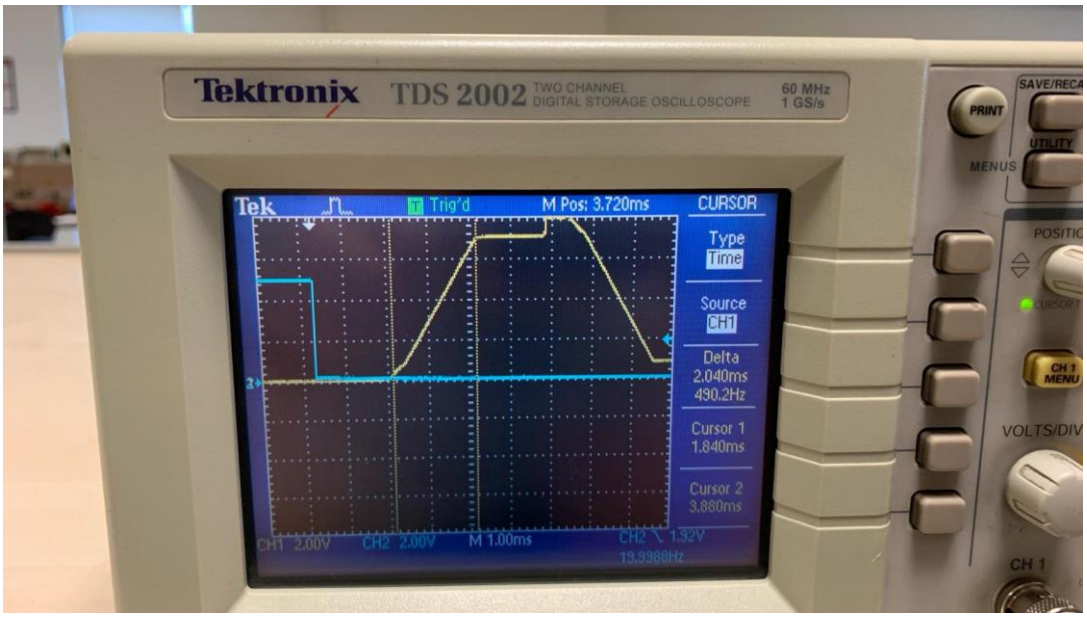

Figure 23: Second Time Interval

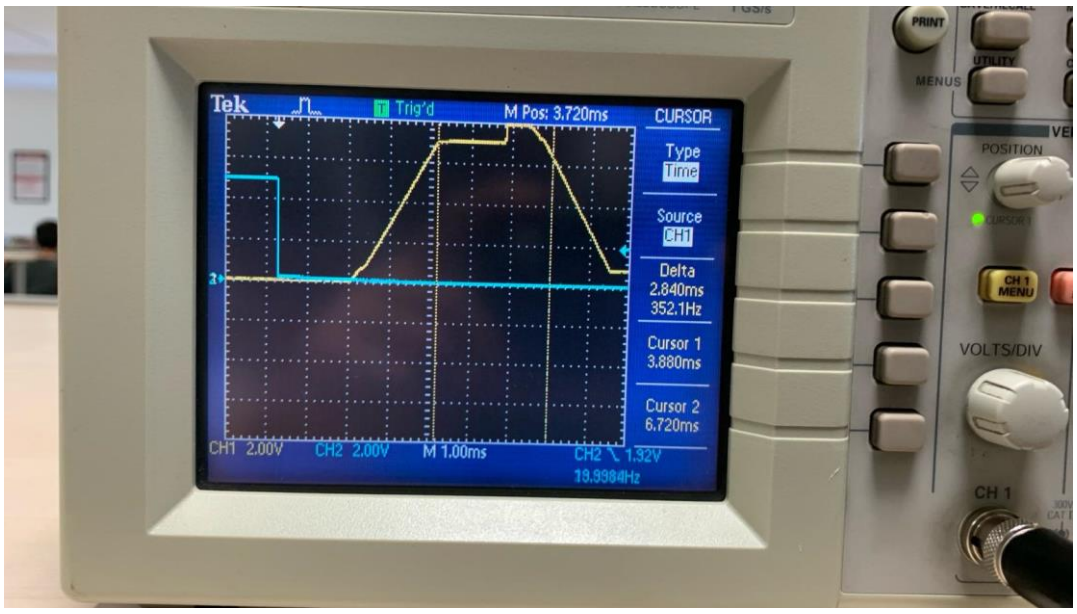

Figure 24: Third Time Interval

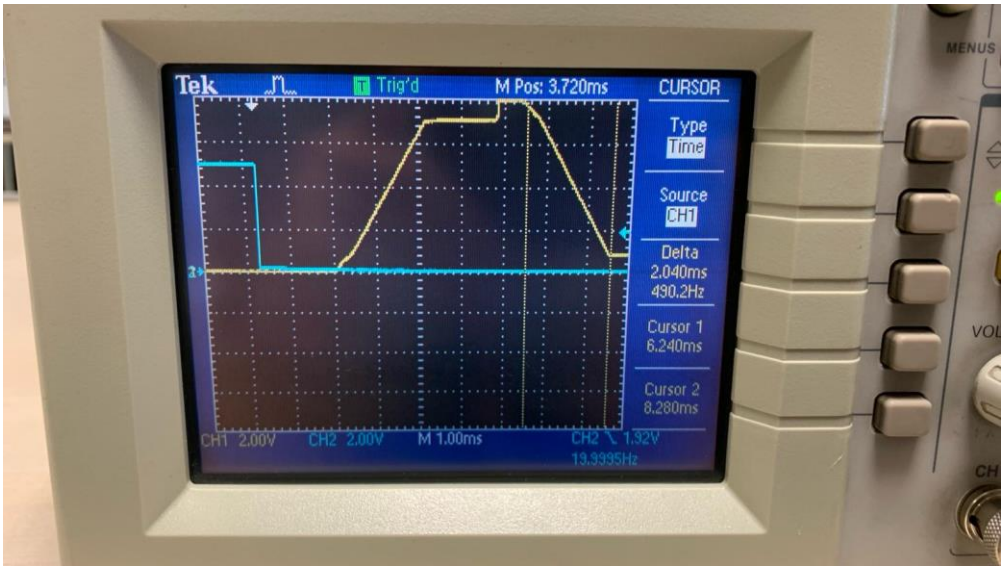

Figure 25: Fourth Time Interval

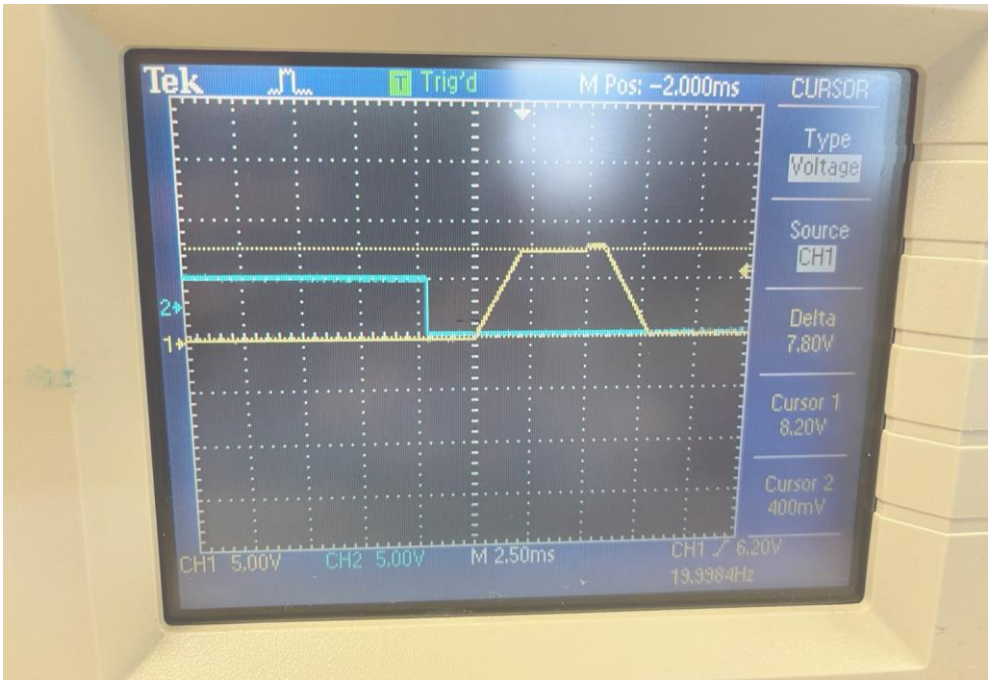

Figure 26: Output Voltage is 8.20 V

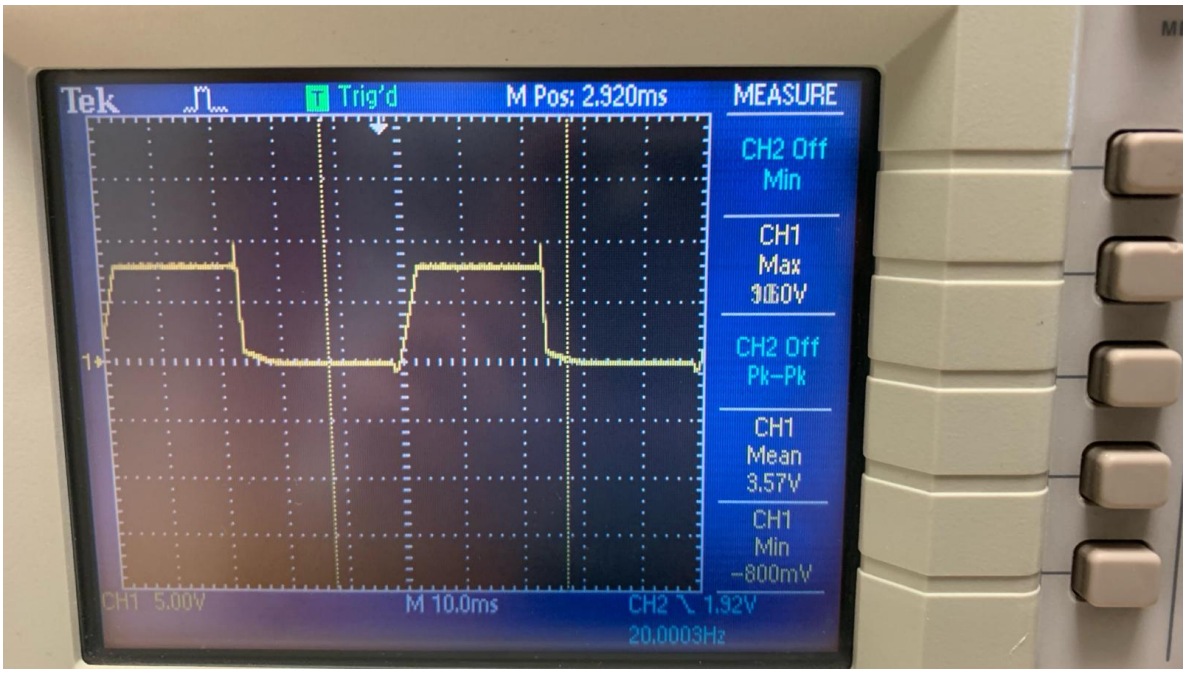

Figure 27: First Integrator

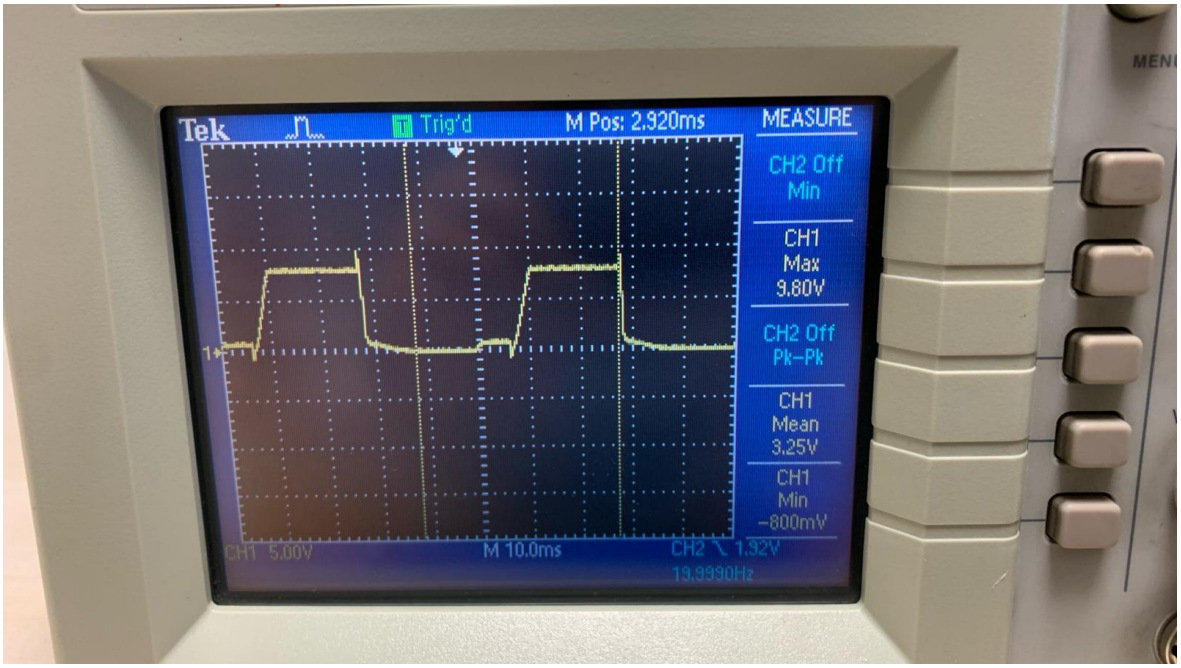

Figure 28: Second Integrator

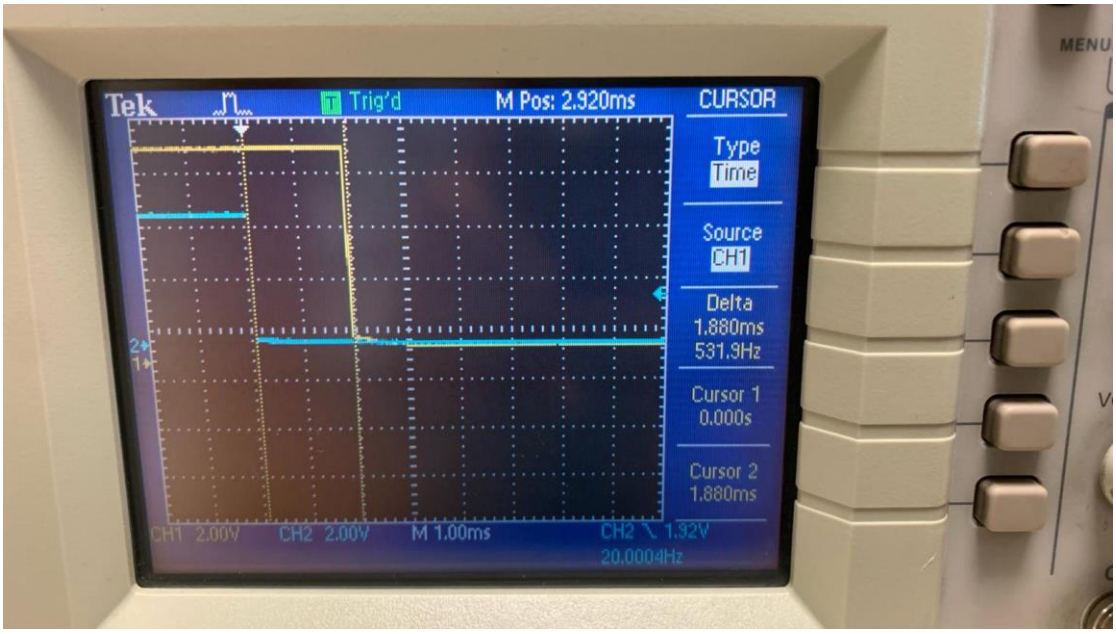

Figure 29: First Delay

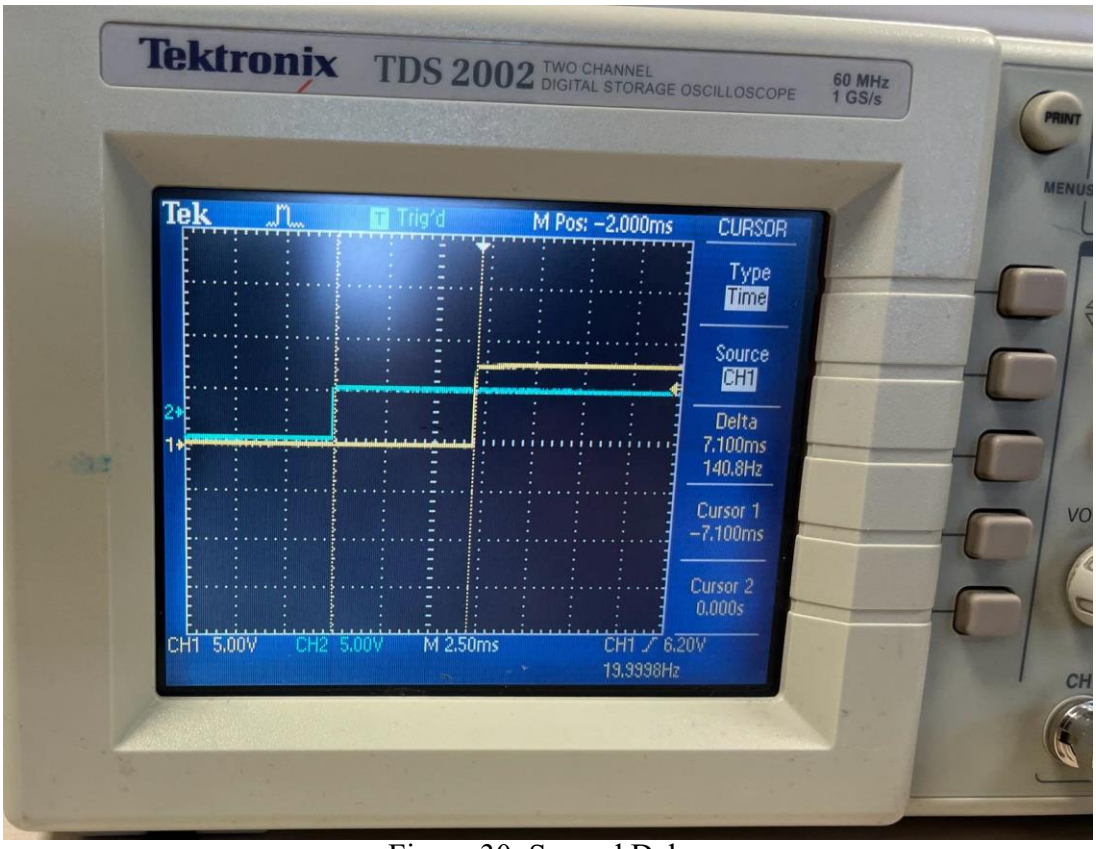

Figure 30: Second Delay

	Δ_{t_0}	Δ_{t_1}	Δ_{t_2}	Δ_{t_3}	Maximum Output Voltage
Desired Value	2 ms	2 ms	3 ms	2 ms	8 V
Observed Value	1.84 ms	2.04 ms	2.84 ms	2.04 ms	8.2 V
Error Percentage	-8%	2%	-5.33%	2%	2.5%

Table 2: HW Implementation Results

Conclusion

In the SW Implementation, the errors for the time intervals and the voltage value were as -1%, 4.5%, 3%, 1.5%, -0.5%. This may be due to the fact that I had specifically chose standard values for the resistor and capacitors, and they were not precisely fulfilling the found results from the circuit analysis. Further error could occur due to the inner delay of the integrator circuit, that made me change the delay circuit values to different standard values. Even though the derived equations and found numerical results are not exactly satisfied, the results are in the desired error range.

In the HW Implementation, the errors came out to be higher, being consecutively -8%, 2%, -5.33%, 2%, 2.5%. In the hardware implementation, I had to significantly change the values of the resistors and capacitors from the design on the software implementation in order to maintain the desired results in the lab manual. Such change might have been necessary due to the inner resistances and tolerances of the lab equipment, most specifically the resistors and capacitors. LM324 OPAMP also has inner resistances and a tolerance, just as any part of the implemented circuit on the breadboard. Furthermore, such difference in the subtractor circuit might have created discrepancies as the resistor values expected to be equal could have been different. Change of any circuit element value or replacement of any calculated equipment for practical usefulness could have significantly affected the final output and created the errors.

In general, the third lab was useful in the sense that it got students into manipulating circuits using OPAMPs and RC circuit elements, especially creating delayed trapezoid outputs of desired time intervals. The lab made the students practice analyzing OPAMP and RC circuits, learn about comparators and delay, integrator and subtractor type of circuits.

The lab results were satisfactory for obtaining the desired results and the three type circuit implementation was helpful in maintaining and manipulating the desired output. This lab revealed that such type of circuity creates certain types of output signals from inputted pulse waves, such as delayed or trapezoid shaped outputs, and the results could improve by reconsidering the inner delay of the integrator circuit, or further changing the values of the resistors and capacitors by making new attempts to achieve less error by the method of trial and error.