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EEE 313 Lab – 1

Low Dropout Voltage Regulator

Introduction

This lab consists of two separate parts, one being finding β of the BD136 pnp transistor, and the other being designing and implementing a low dropout voltage regulator (LDO) by applying certain conditions and phenomenon on circuit elements to find their correct values. The schematic of an LDO circuit can be seen as in Figure 1.

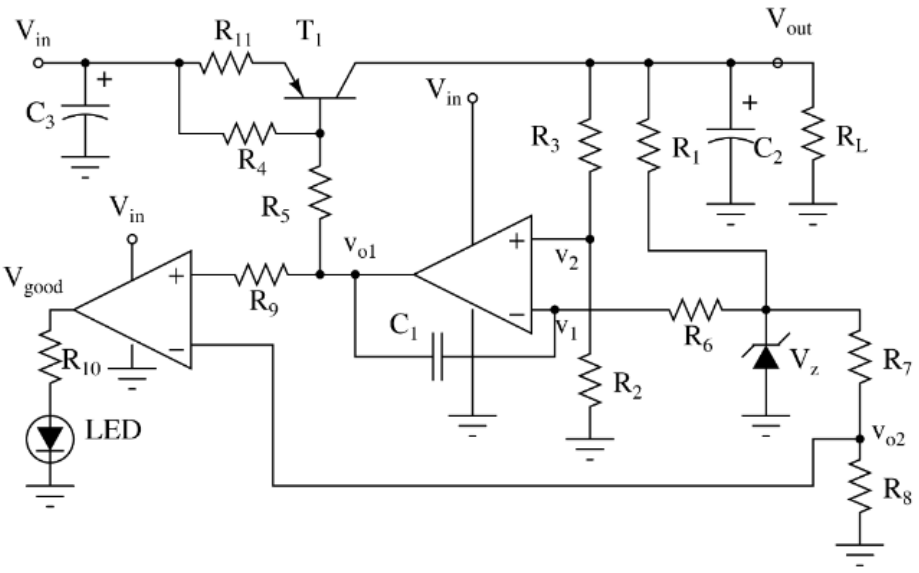

Figure 1: Schematic of LDO

Purpose

The purpose was to make use of basic circuitry to find β of a pnp transistor to understand its behavior, and then make use of the learned characteristics in order to design and implement an LDO on software and hardware.

Methodology and Design

First Part

A simple circuit was designed to evaluate the behavior and characteristics of BD136 pnp transistor and its β value. To do this, the simulated circuit in Fig. 2 was designed and implemented as in Fig. 3. The found currents of I_b and I_c revealed β. (I_c/I_b)

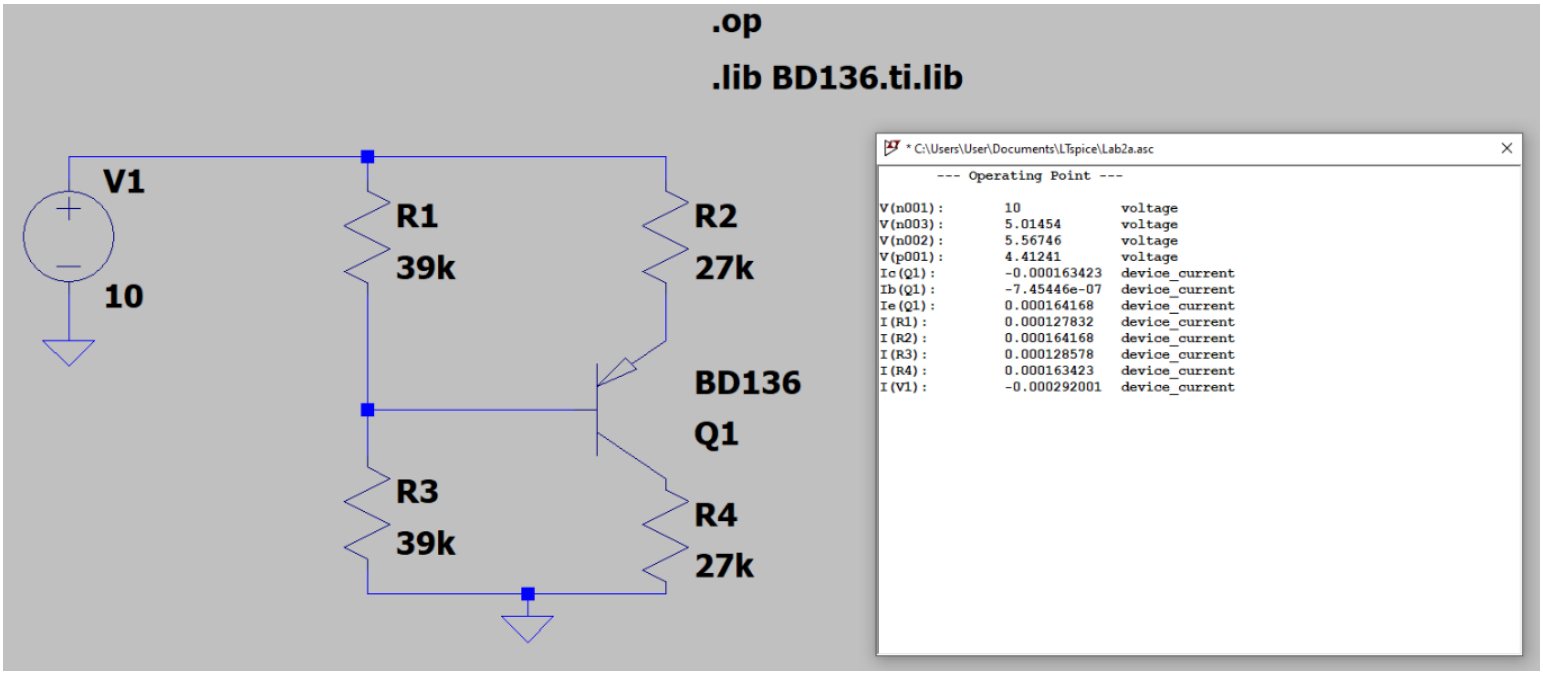

Figure 2: Designed Circuit to Evaluate PNP

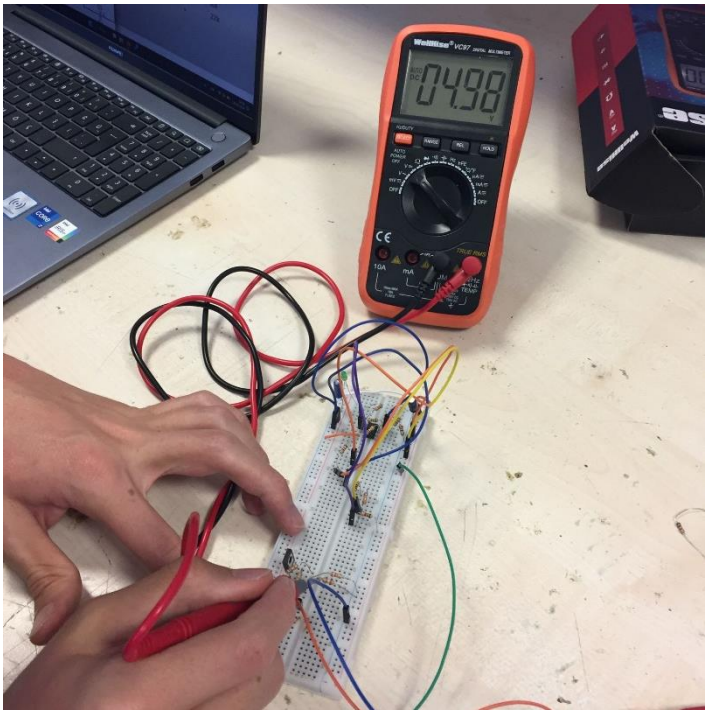

Figure 3: Voltage at B of PNP (Vin=8V)

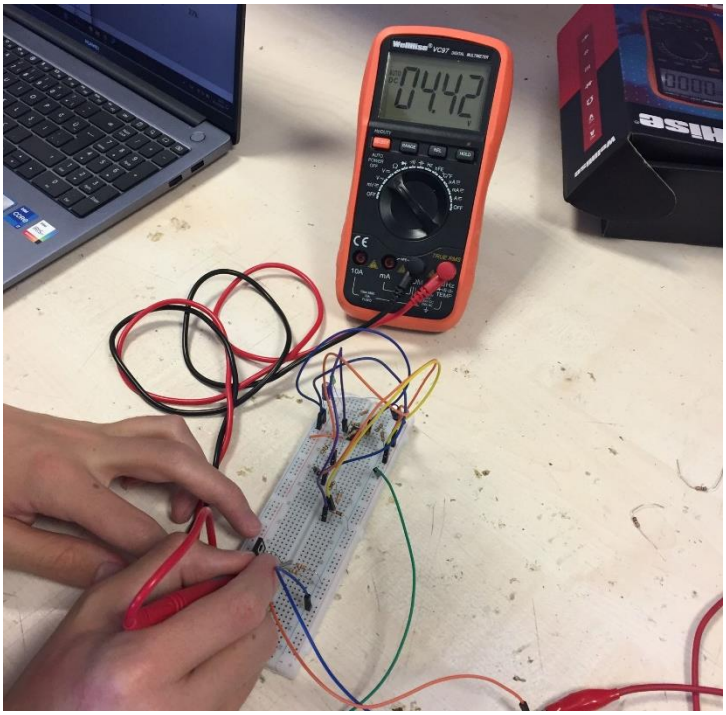

Figure 4: Voltage at C of PNP (Vin=8V)

To find the currents I_b and I_c, the corresponding voltages were used in node analysis for the circuit in Fig. 2. The results were as in Table 1.

	LTSpice	Hardware
I_b (A)	$7.45 * 10^{-7}$	$6.59 * 10^{-7}$
I_c (A)	$1.634 * 10^{-4}$	$1.637 * 10^{-4}$
β	219.2	248.4

Table 1: Part A Results

The error rate was must likely due to inner resistances, circuit elements being nonideal and measurement errors due to lab equipment. Here, the found β values were as in Table 1.

Second Part

A low dropout voltage regulator was designed with the following specifications (Vout=9.5V):
Specifications:

1. Line regulation: When V_{in} is varying between V_{out}+0.7 to V_{out}+6 at 100Hz, the output voltage, V_{out}, changes by no more than 20mV when the output current is 100mA (R_L=V_{out}/0.1).
2. Load regulation: When V_{in}=V_{out}+2, the output voltage, V_{out}, changes no more than 20mV when the output current changes between 0mA and 100mA at 100Hz. (In LTSpice, you can connect a sinusoidal current source at the output varying between 0 and 100mA.)
3. A green LED should turn on if the regulation is achieved. Otherwise, it should turn off, for example, because the input voltage is too low or the output current is too high.

The designed circuit in LTSpice is as in Figure 5.

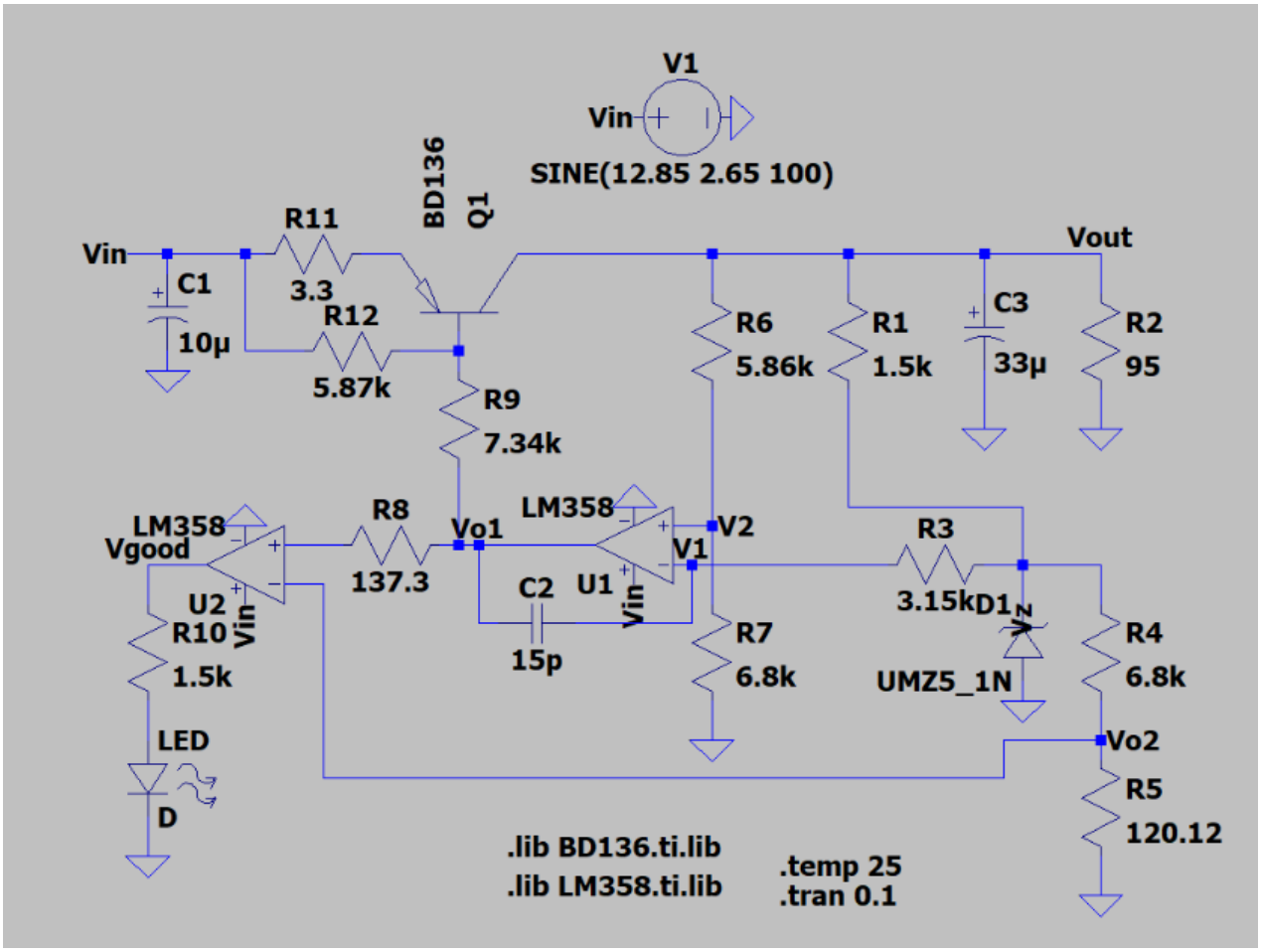

Figure 5: LTSpice LDO Design

Requirements to be addressed:

REQUIREMENT 1 – LINE REGULATION

Line regulation: When V_{in} is varying between V_{out}+0.7 to V_{out}+6 at 100Hz, the output voltage, V_{out}, changes by no more than 20mV when the output current is 100mA (R_L=V_{out}/0.1).

The following Figures 6-9 represent the unchanging Vout when Vin is between 10.2V and 15.5V and the output current is 100 mA.

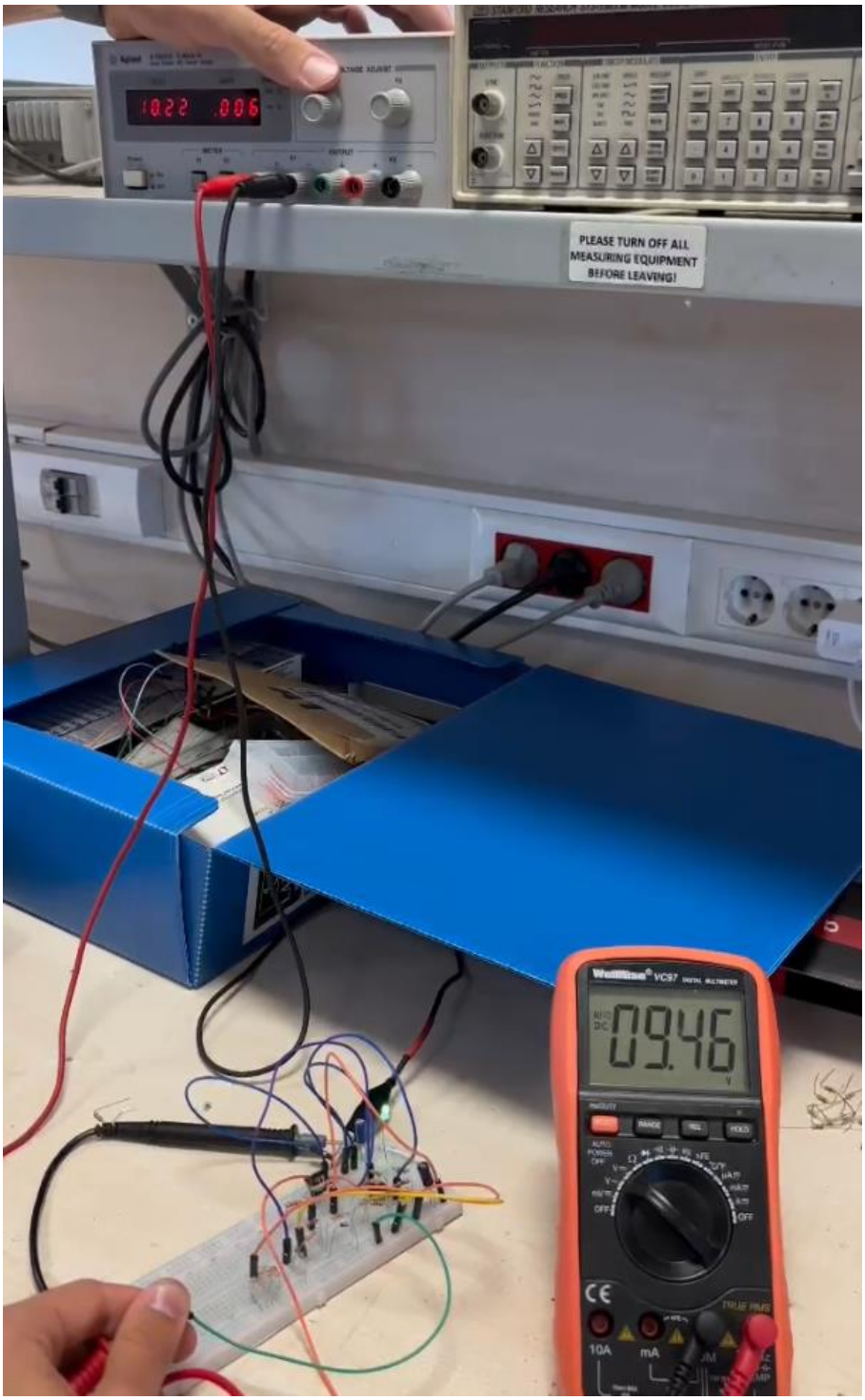

Figure 6: Vout = 9.46V at Vin = 10.22V

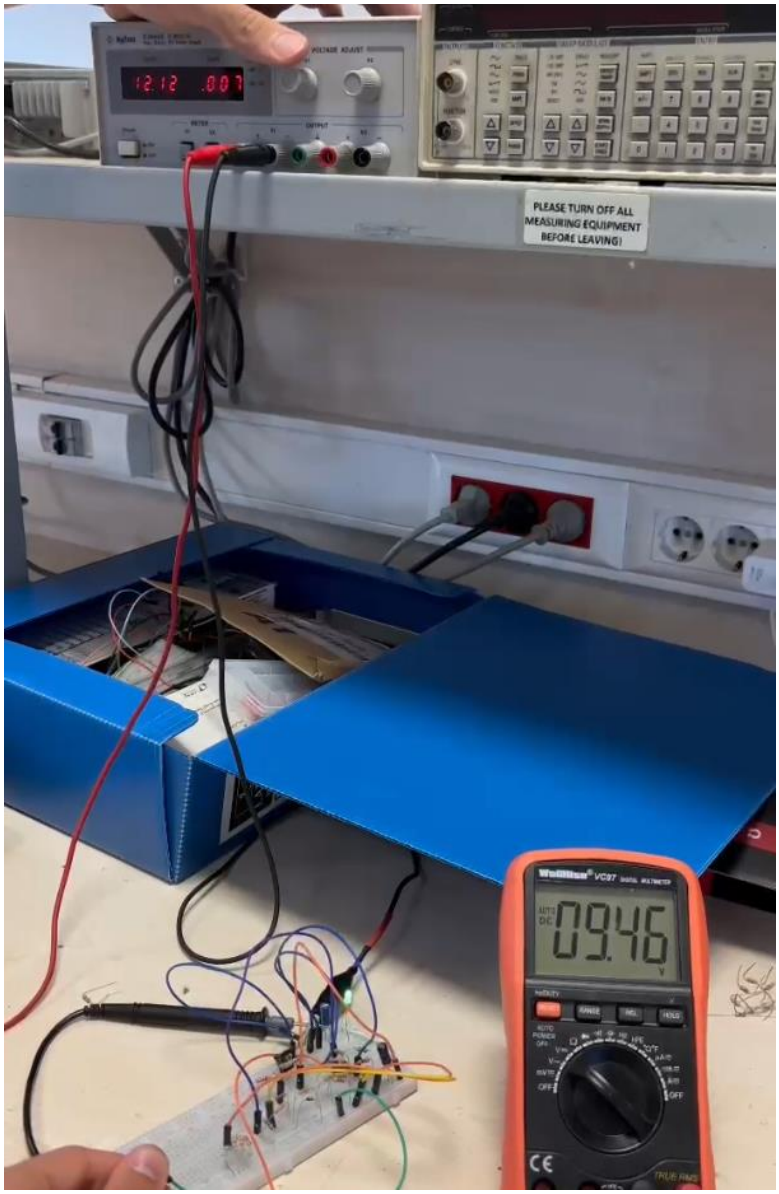

Figure 7: Vout = 9.46V at Vin = 12.12V

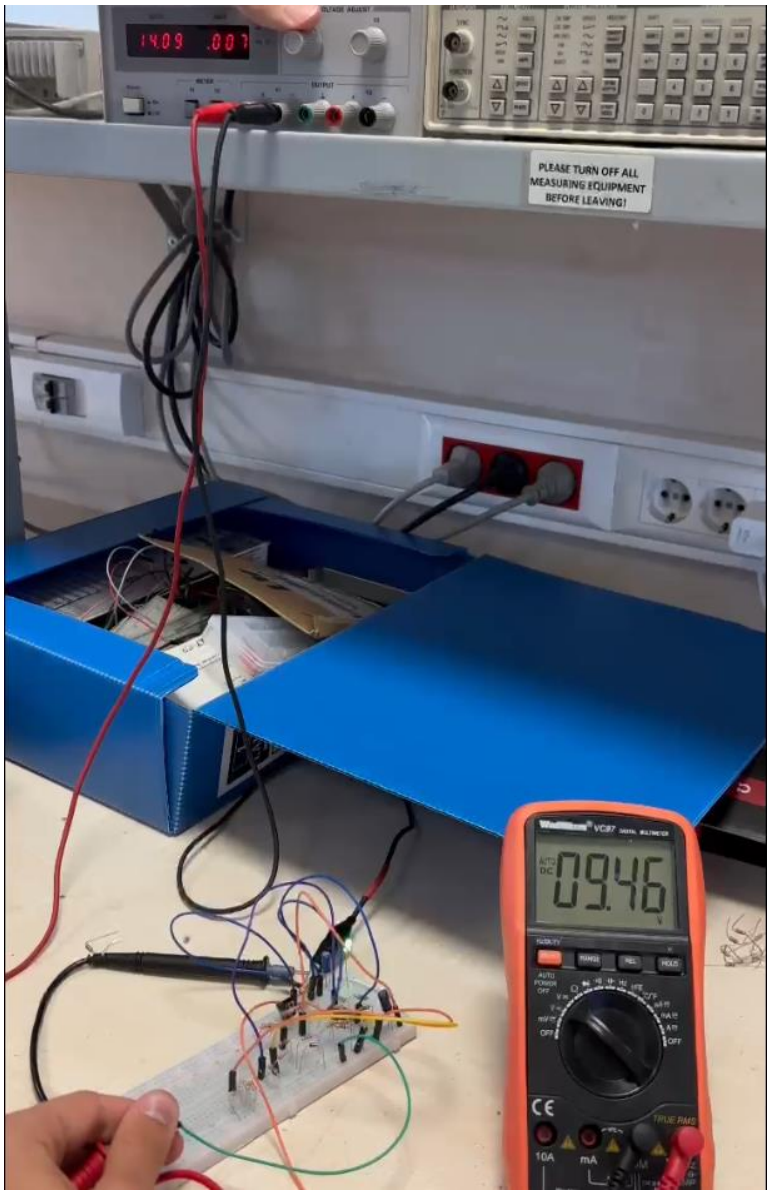

Figure 8: Vout = 9.46V at Vin = 14.09V

Through this input voltage increase, the LED is constantly ON. It can be spotted on the top left of the breadboard.

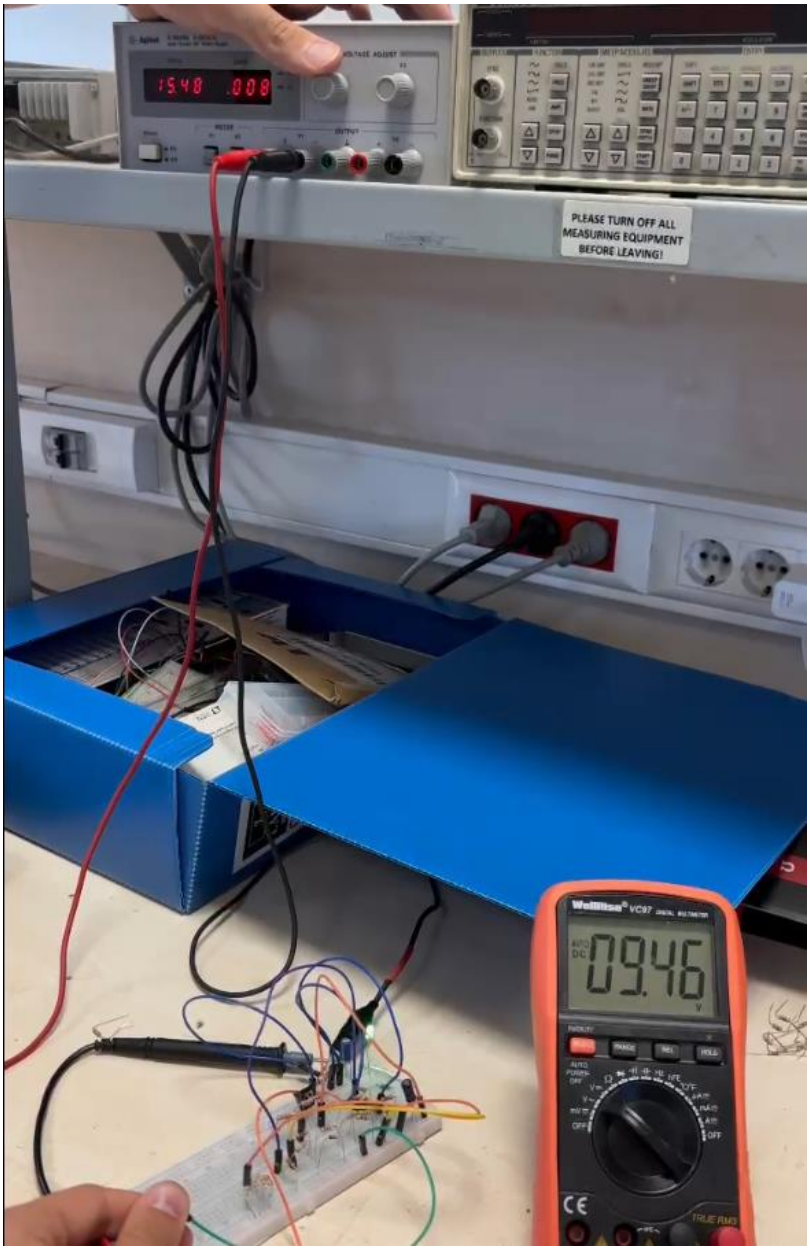

Figure 9: Vout = 9.46V at Vin = 15.48V

Input Voltage	10.22V	12.12V	14.09V	15.48V
Measured Vout	9.46V	9.46V	9.46V	9.46V
Simulated Vout	9.459V	9.459V	9.459V	9.459V
Error Rate (%)	~0	~0	~0	~0

Table 2: Requirement 1 Measurements

REQUIREMENT 2 – LOAD REGULATION

Load regulation: When $V_{in}=V_{out}+2$, the output voltage, V_{out}, changes no more than 20mV when the output current changes between 0mA and 100mA at 100Hz. (In LTSpice, you can connect a sinusoidal current source at the output varying between 0 and 100mA.)

The following Figures 10-12 represent the unchanging Vout when Vin = Vout + 2 for the case where the load resistor is removed from the circuit. Output current is between 0 mA, 100 mA.

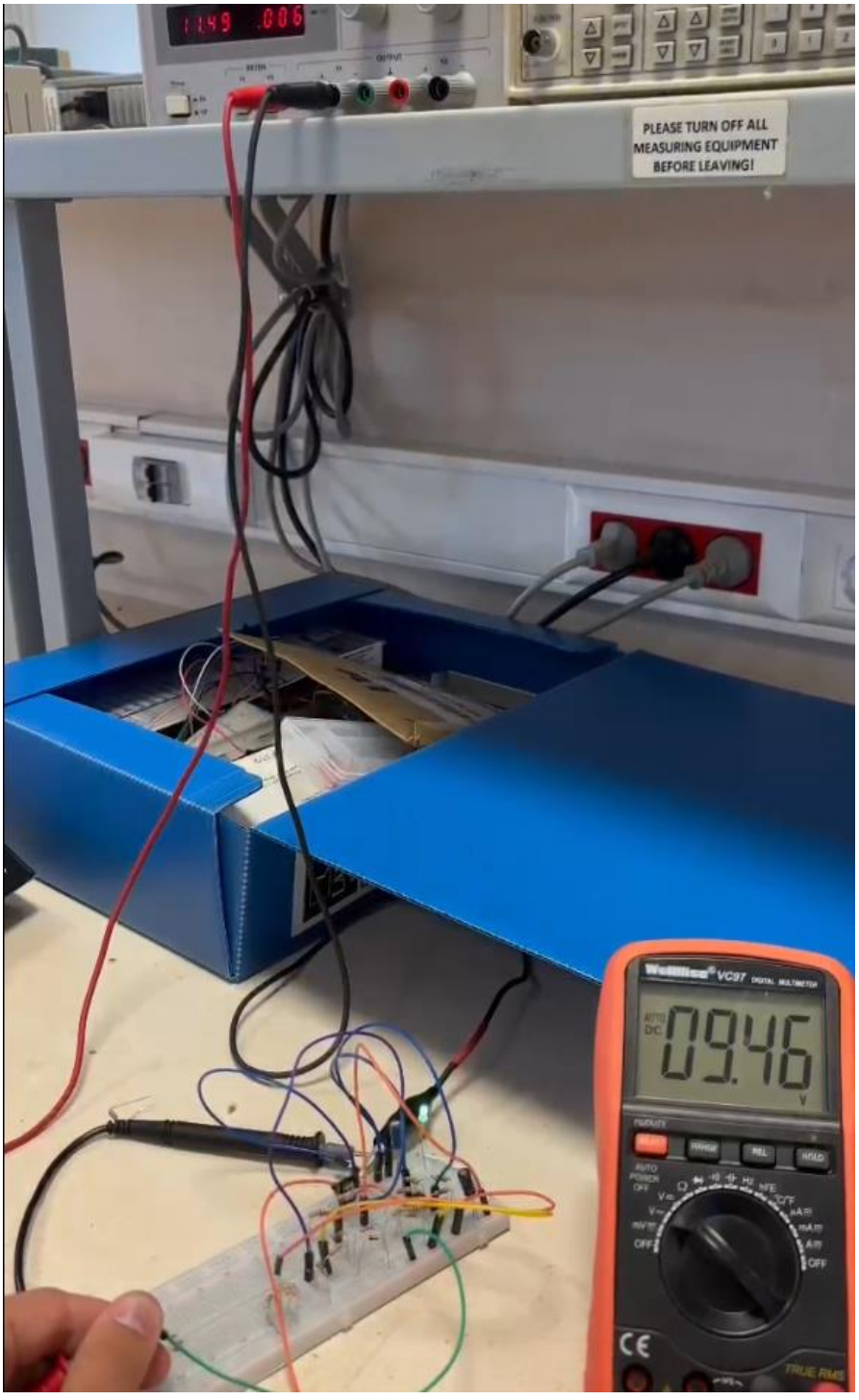

Figure 10: Load Resistor is Removed, Vout = 9.46V

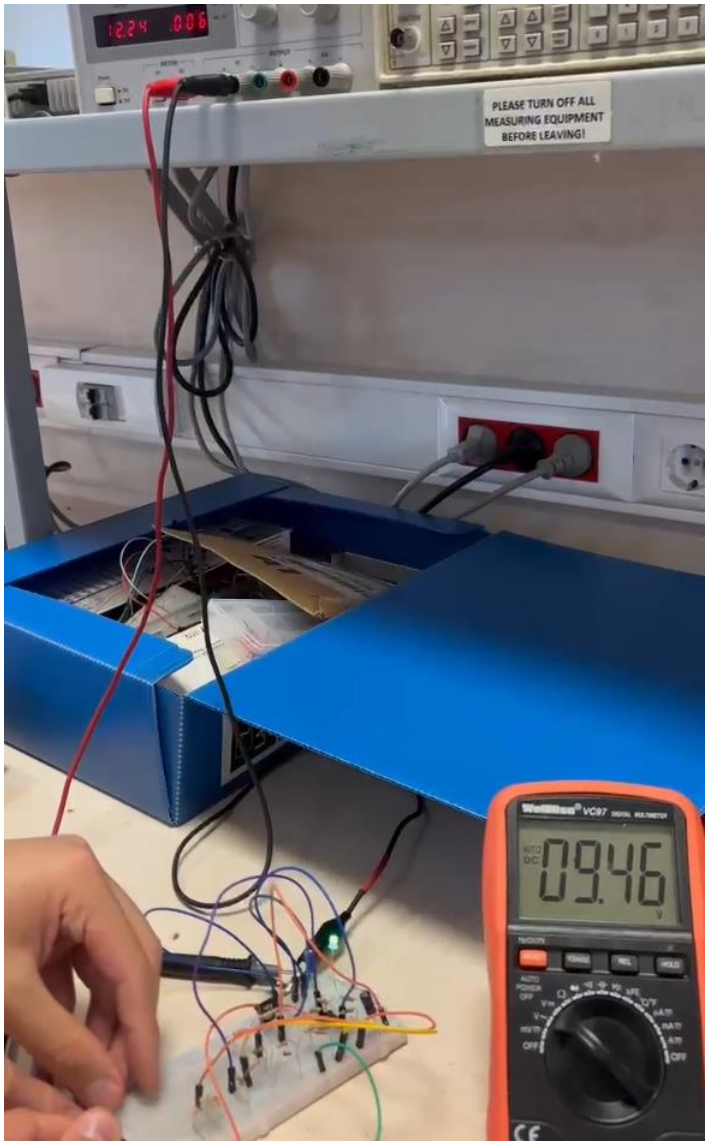

Figure 11: Load Resistor is Removed, Vout = 9.46V, Vin= 12.24 V

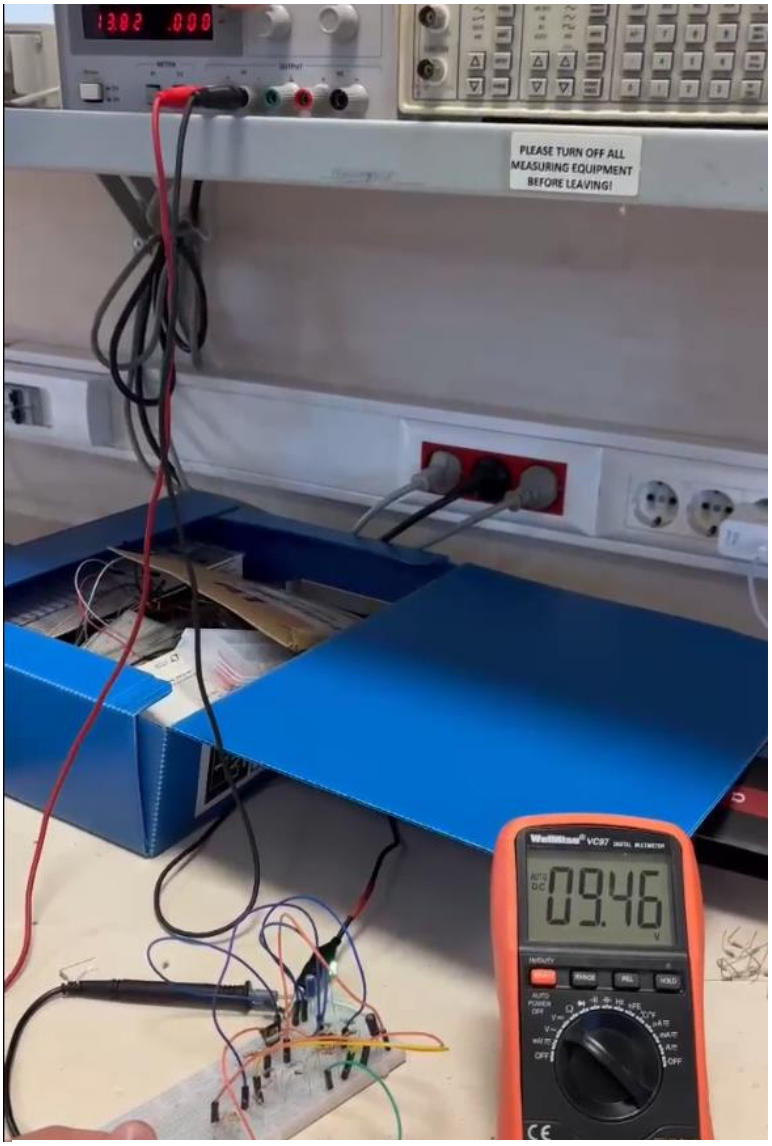

Figure 12: Load Resistor is Removed, Vout = 9.46V, Vin= 13.82 V

Here, the removal of the load resistor does not change the behavior of the unchanging Vout as desired to be in the range 20 mV (implying a ~0% error rate). Additionally, the LED is constantly ON.

REQUIREMENT 3 – LED OFF When not Regulated

A green LED should turn on if the regulation is achieved. Otherwise, it should turn off, for example, because the input voltage is too low or the output current is too high.
For this requirement, the LED is OFF when Vin < Vout + 0.7V = 10.2 V and it is ON when Vout + 6V >= Vin >= Vout + 0.7V as in Figures 13-16. This situation implies that there is 0 current when the LED is OFF.

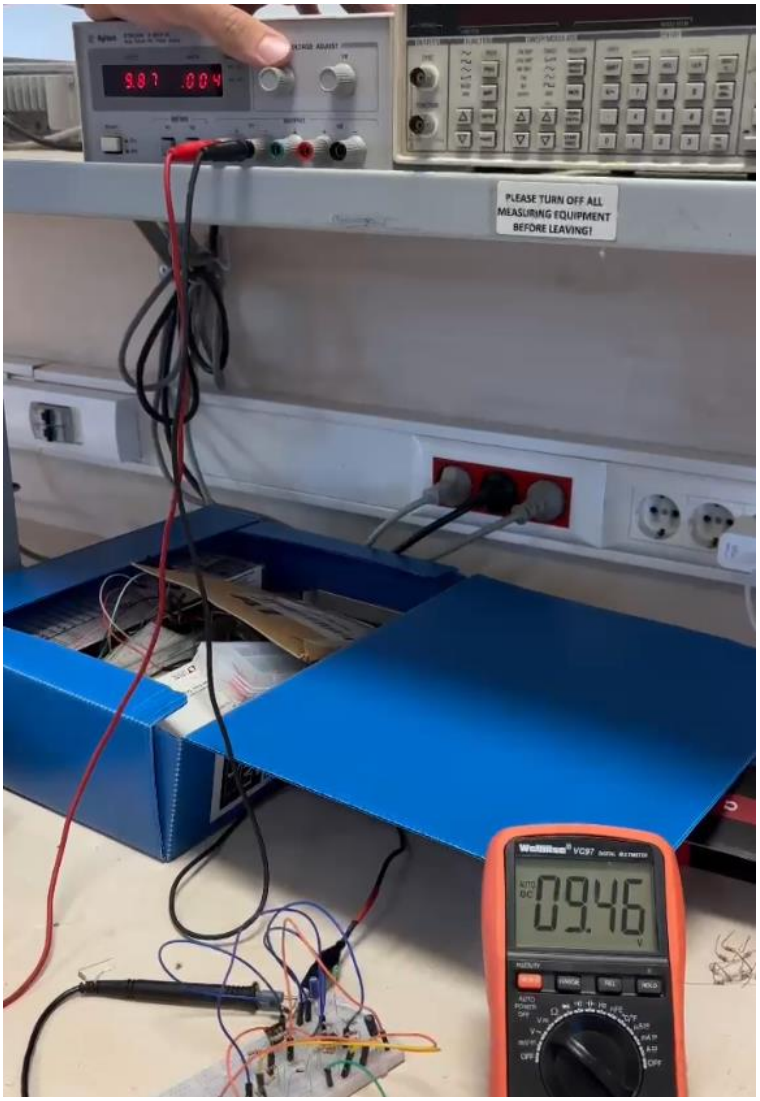

Figure 13: LED is OFF for Vin = 9.87V (multimeter connected to Vout) (LED at top left of breadboard)

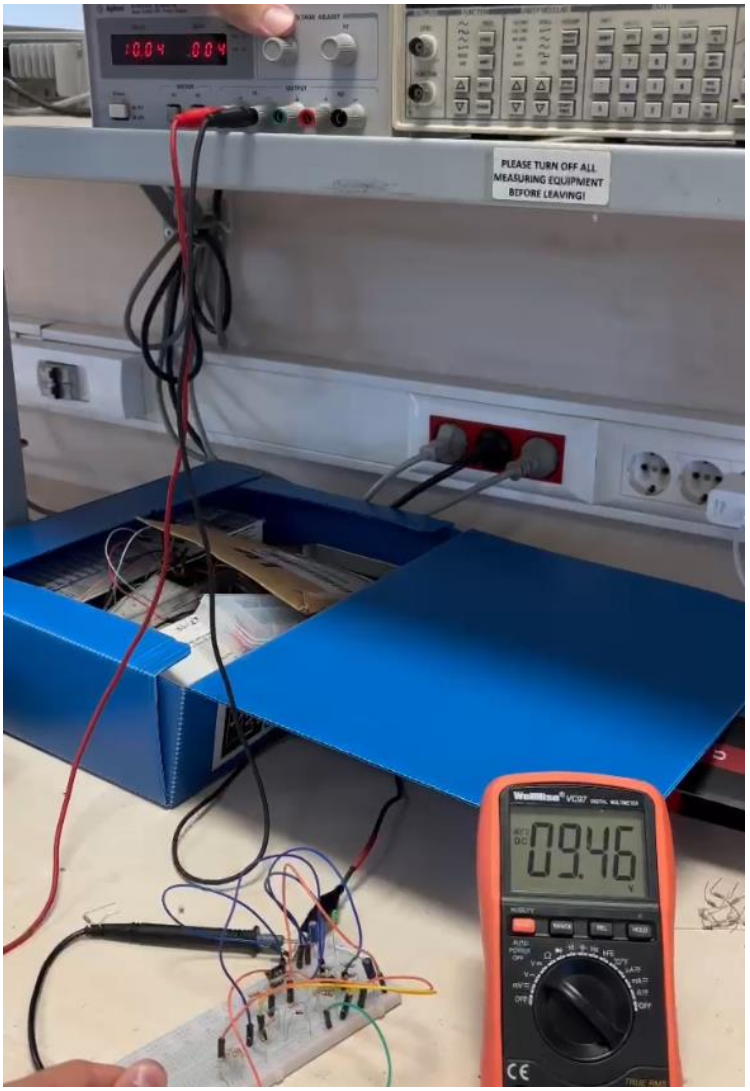

Figure 14: LED is OFF for Vin = 10.04V

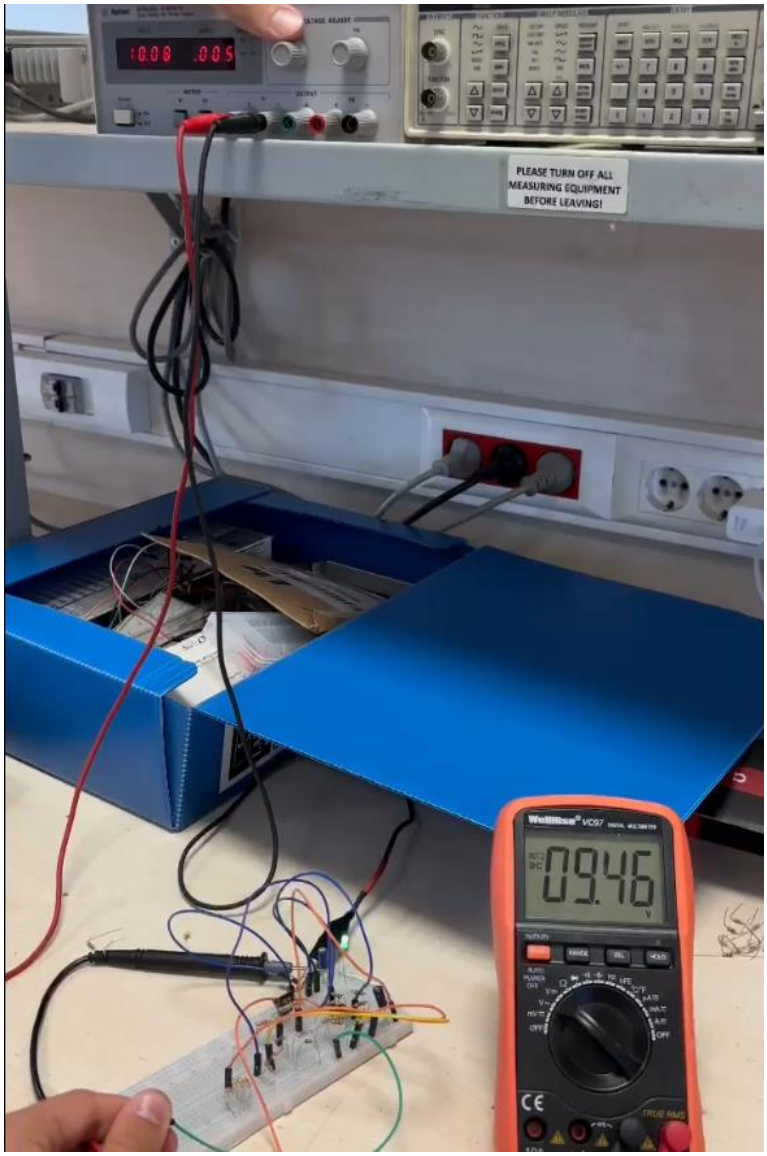

Figure 15: LED turns ON for Vin = 10.08V

Figure 16: LED is further ON for Vin = 12.24V

The LED on the top left of the breadboard is constantly ON after 10.08V (against desired 10.20V with error rate 1.17%), implying that regulation is achieved and sufficient current goes through the LED.

DISSIPATED POWER ON THE LOAD RESISTOR

Load resistance is 95Ω in LTSpice and 100Ω was used in the lab. Its value is measured as 98.7Ω on the multimeter. For Vout = 9.46V for 15.5V >= Vin >= 10.20V, dissipated power is $\frac{{V_{out}}^2}{R} = 0.907\text{W}$.

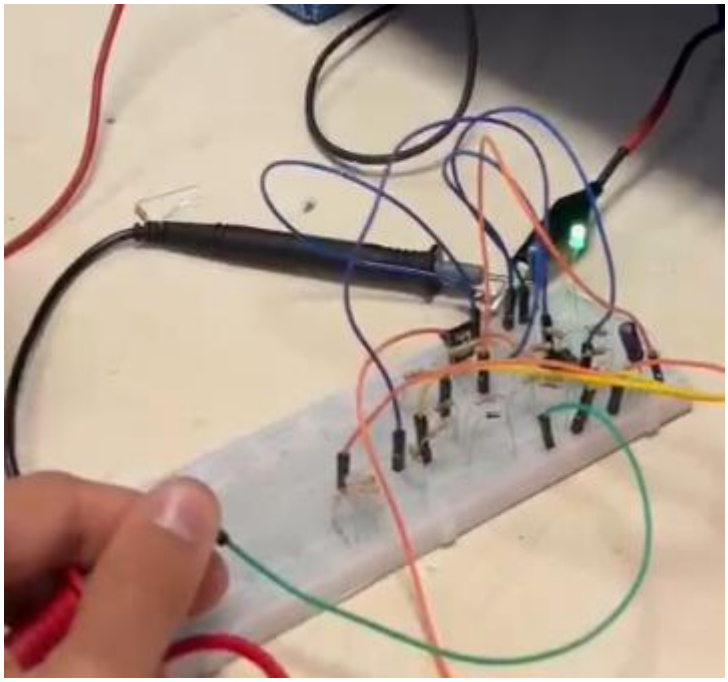

Figure 17: Overall Photo of Circuit on Breadboard (LED on top left)

Conclusion

The desired conditions for line and load regulations, β calculation, dissipated power calculation and LED's relation with regulation are satisfied. The error rates might be due to internal resistances, errors and tolerances of lab equipment and circuit elements. This lab was useful in terms of understanding the characteristics of of pnp transistors for further use, especially the BD136.