Emir Arda Bayer
22201832

PART A

I created the circuit in Figure 1 to reveal the gain of the BD136 pnp transistor, and simply calculated the ratio of the current at ‘c’ to ‘b’ to find this value.

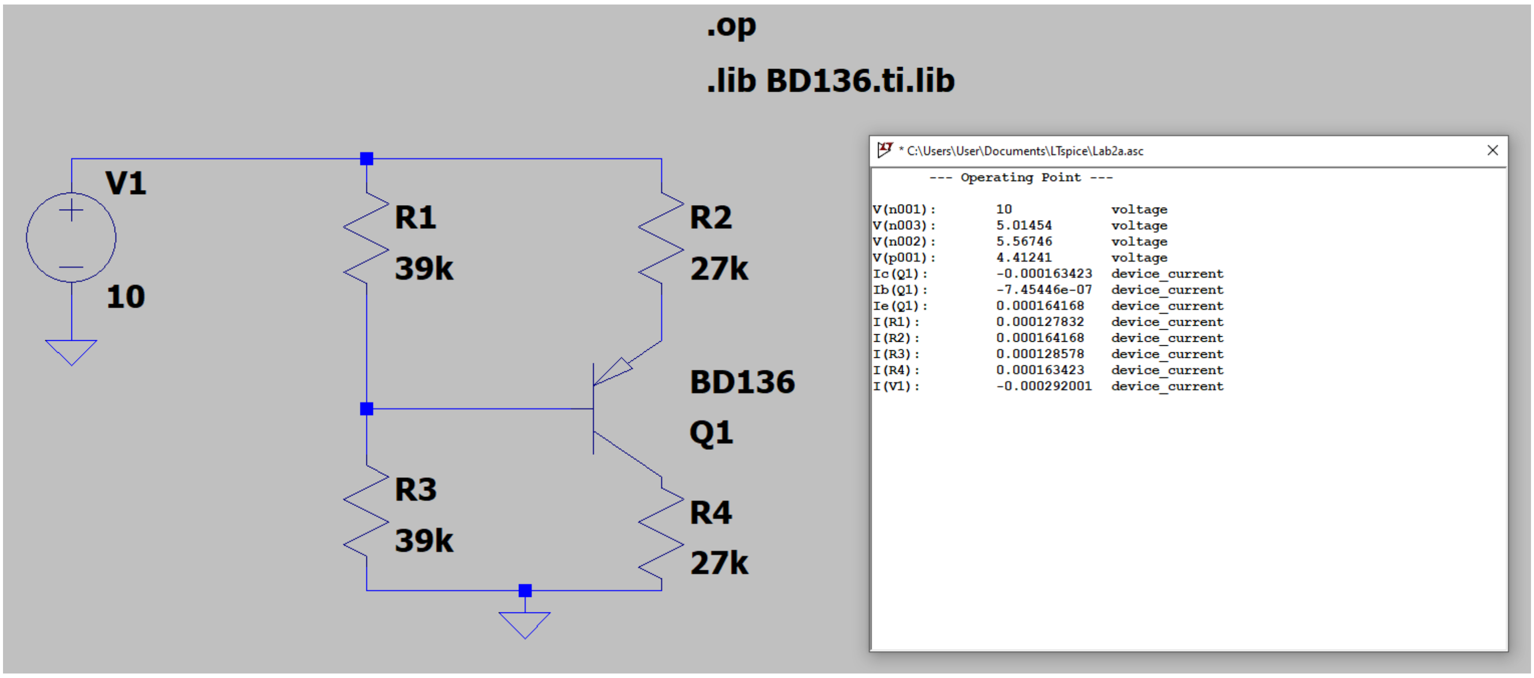

Figure 1: Designed Circuit for Measurement of PNP Gain

This measurement of current revealed β to be 219.2 (Ic/Ib).

PART B

A low-dropout voltage regulator was designed in Lab 2 with the following specifications as in Figure 2.

Specifications:

1. Line regulation: When V_{in} is varying between V_{out}+0.7 to V_{out}+6 at 100Hz, the output voltage, V_{out}, changes by no more than 20mV when the output current is 100mA (R_L=V_{out}/0.1).
2. Load regulation: When V_{in}=V_{out}+2, the output voltage, V_{out}, changes no more than 20mV when the output current changes between 0mA and 100mA at 100Hz. (In LTSpice, you can connect a sinusoidal current source at the output varying between 0 and 100mA.)
3. A green LED should turn on if the regulation is achieved. Otherwise, it should turn off, for example, because the input voltage is too low or the output current is too high.

The desired schematic is as in Figure 2 and the designed circuit can be seen in Figure 3.

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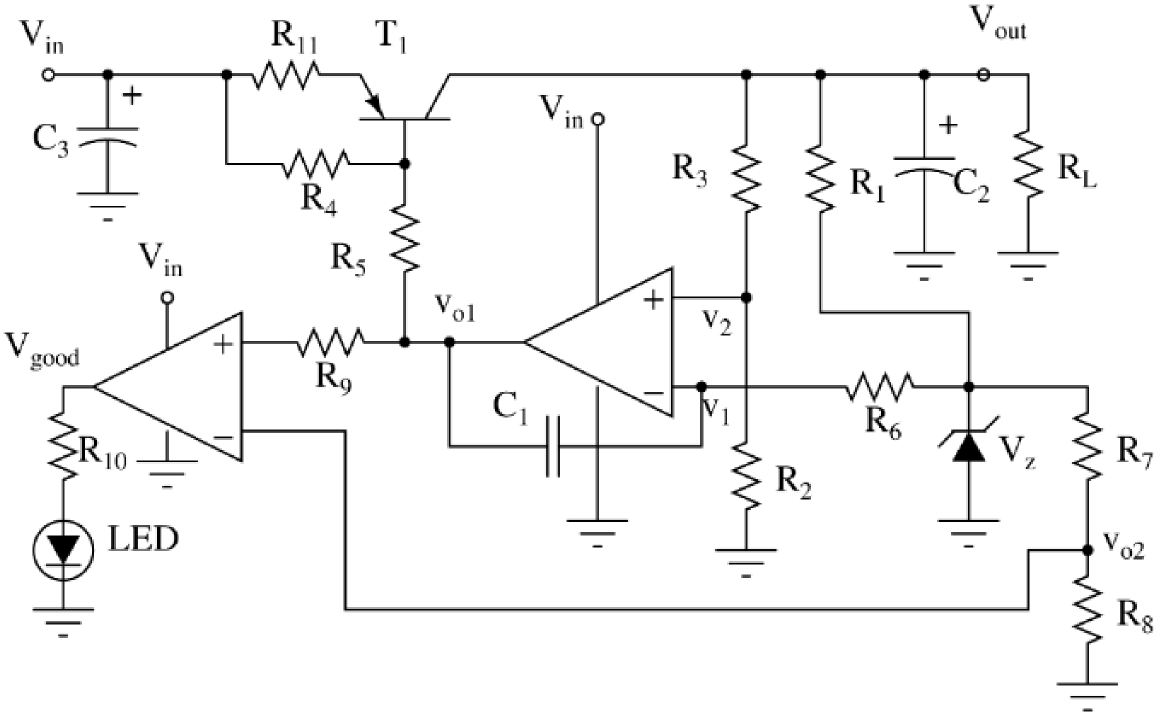

Figure 2: Desired Schematic

Requirements to be addressed:

REQUIREMENT 1 – Line Regulation

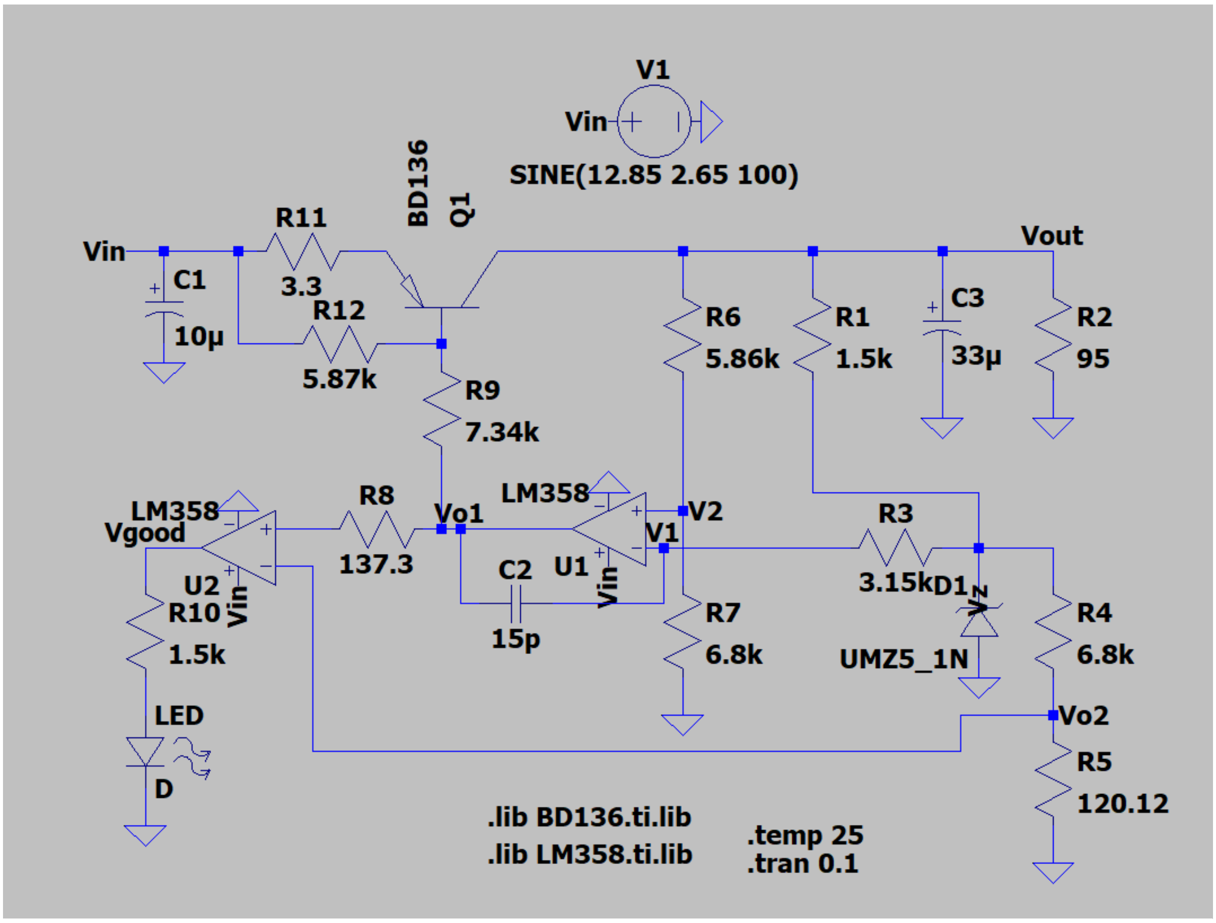

Figure 3: Designed LDO

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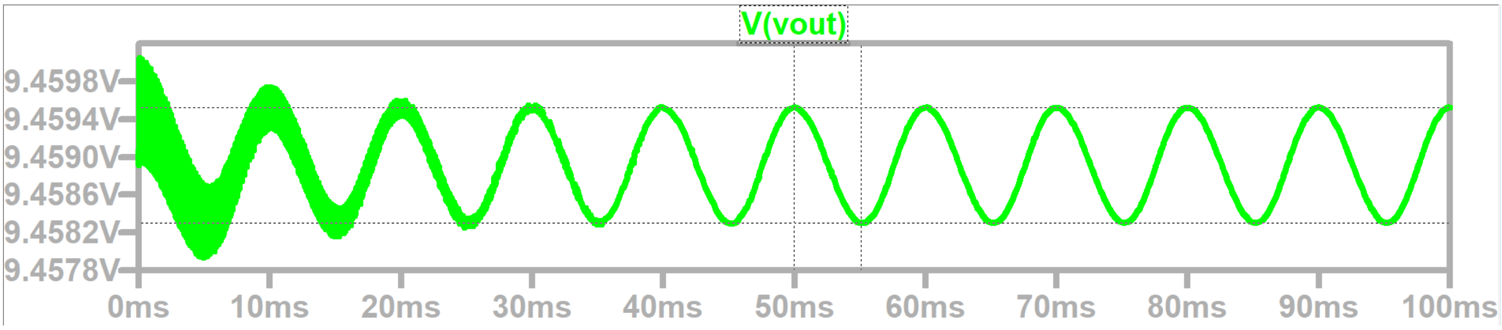


Figure 4: Requirement 1 Waveform of Vout

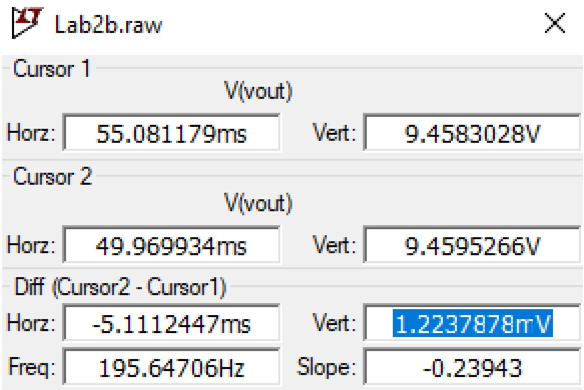


Figure 5: 1.22 mV < 20 mV

Line regulation: When V_{in} is varying between V_{out}+0.7 to V_{out}+6 at 100Hz, the output voltage, V_{out}, changes by no more than 20mV when the output current is 100mA ($R_L=V_{out}/0.1$).
Here, the voltage difference between the peaks is 1.22 mV, which is smaller than 20 mV. The requirement for the ripple to be in the range of 20 mV is here satisfied.

REQUIREMENT 2 – Load Regulation

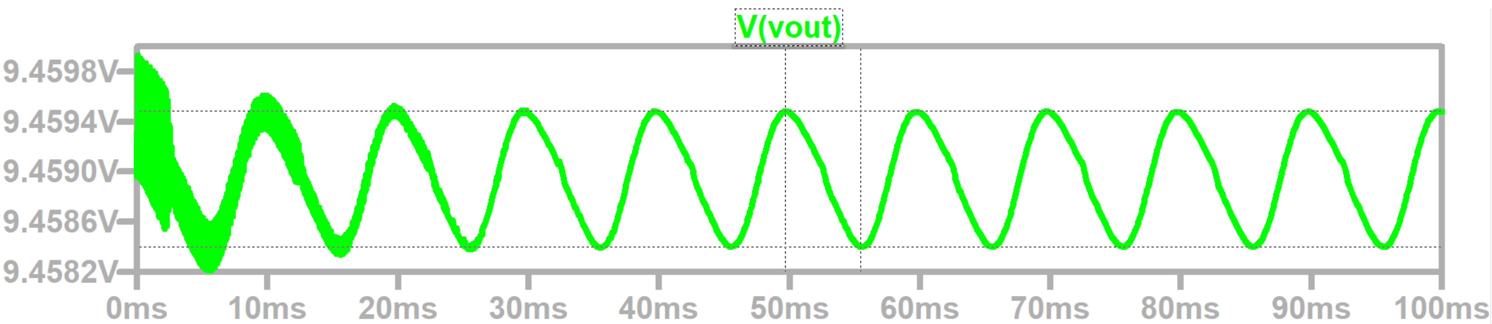


Figure 6: Vout for Requirement 2

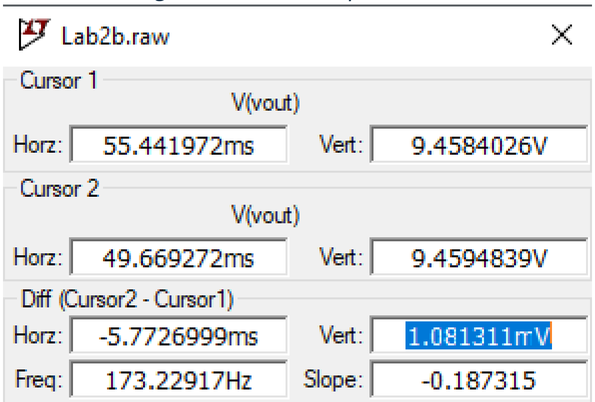


Figure 7: 1.08 mV < 20 mV

Load regulation: When V_{in}=V_{out}+2, the output voltage, V_{out}, changes no more than 20mV when the output current changes between 0mA and 100mA at 100Hz. (In LTSpice, you can connect a sinusoidal current source at the output varying between 0 and 100mA.)
Here, the ripple's peaks are in the range of 1.08 mV, satisfying the criteria to be less than 20mV.

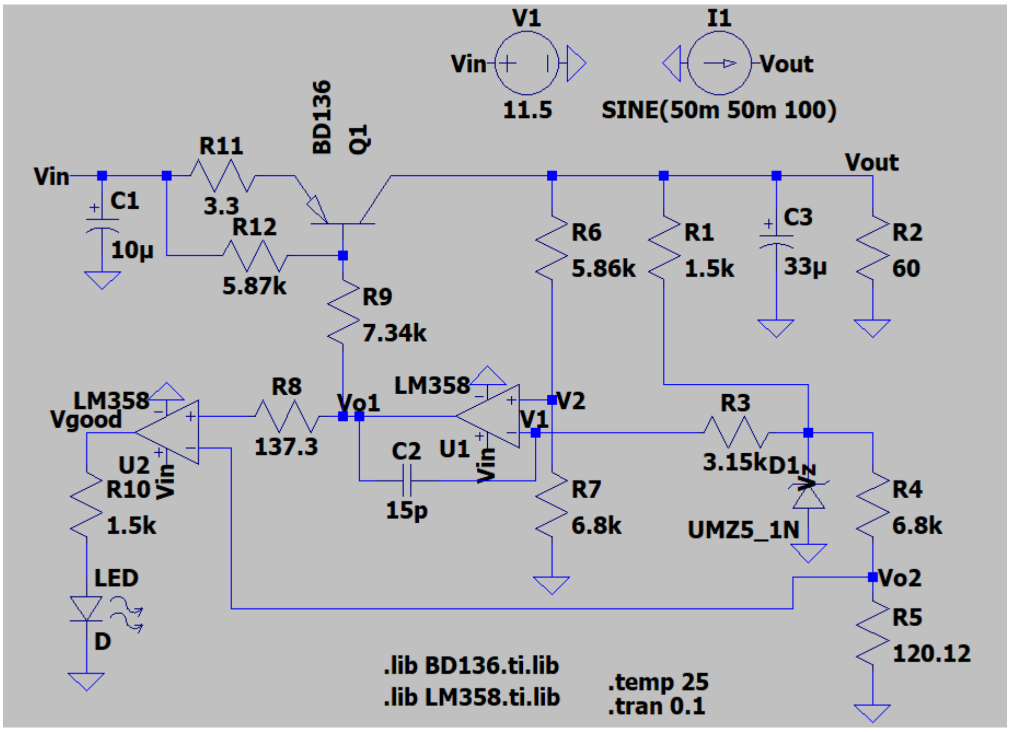


Figure 8: Sources for Requirement 2

REQUIREMENT 3 – LED OFF When not Regulated

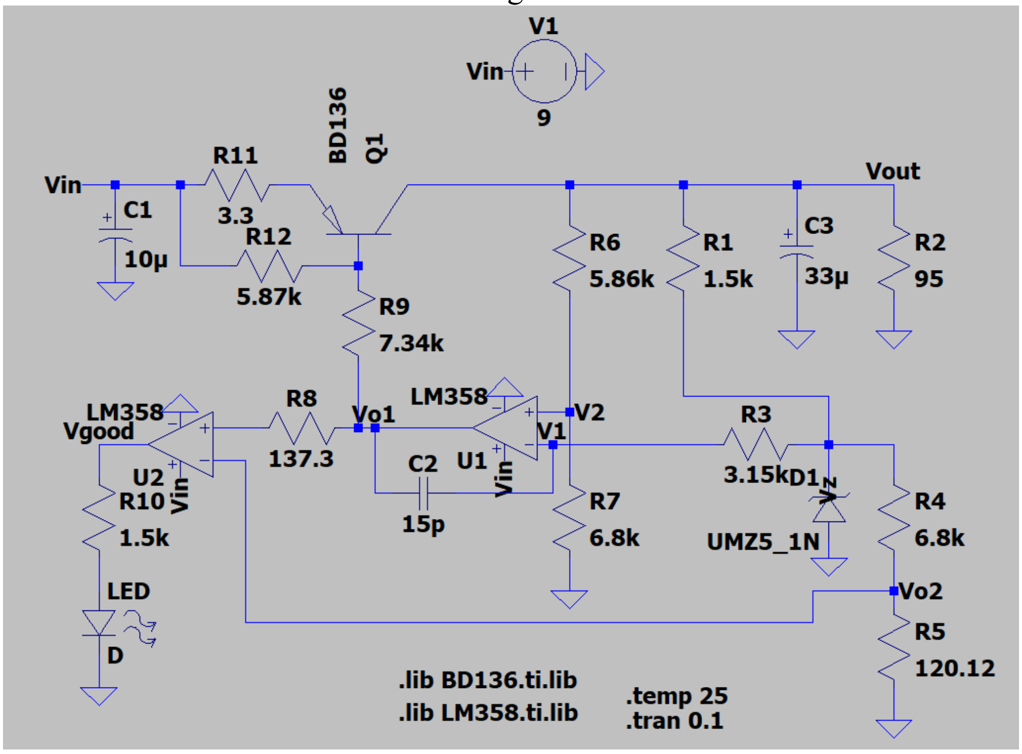


Figure 9: Sources for Requirement 3

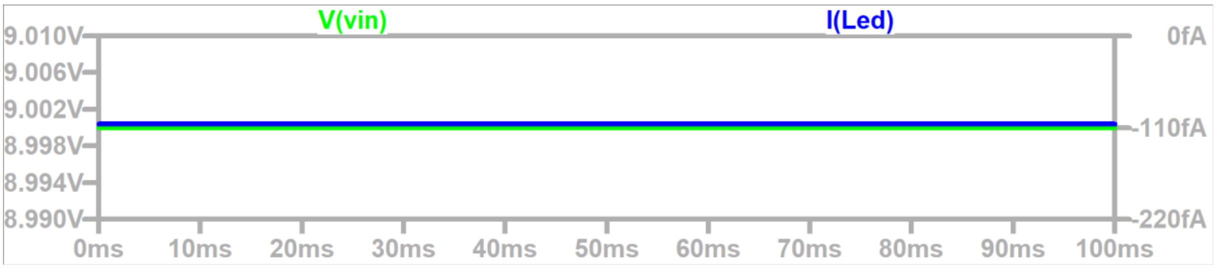


Figure 10: LED Current for Requirement 3 (Vin=9V)

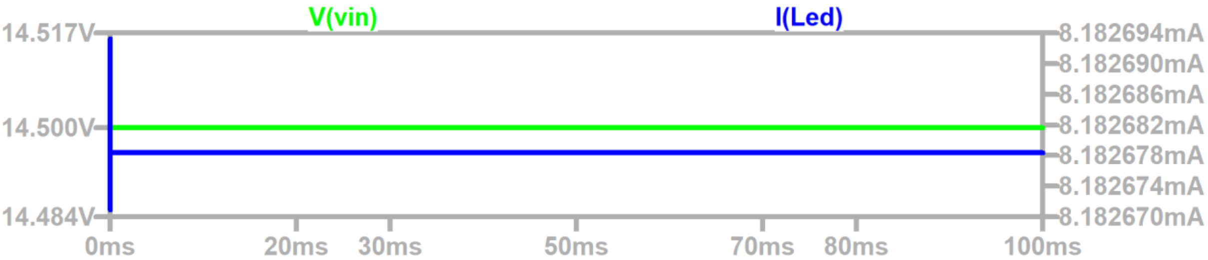


Figure 11: LED Current for Requirement 3 (Vin=14.5V)

A green LED should turn on if the regulation is achieved. Otherwise, it should turn off, for example, because the input voltage is too low or the output current is too high.

Here, the LED is off when Vin < Vout + 0.7V = 10.2 V, but is on when it is in the range Vout + 6V >= Vin >= Vout + 0.7V (when Vin = 14.5V). The LED has 0 current in the first case whereas it has 8.12 mA current in the second case. Additionally, the LED has 0 current in the case where the output current is too high (above 100mA) ,when output resistance is decreased, as in Figure 12.

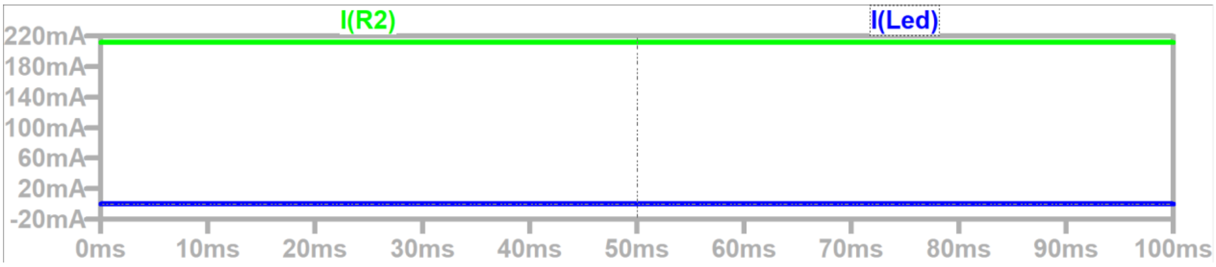


Figure 12: Currents for Output(R2) and LED

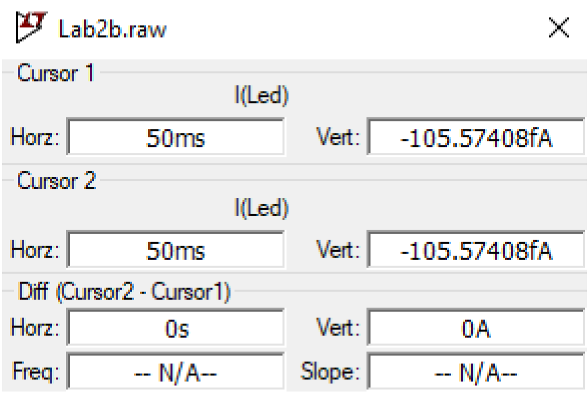


Figure 13: LED Current when Output Current Increases Significantly

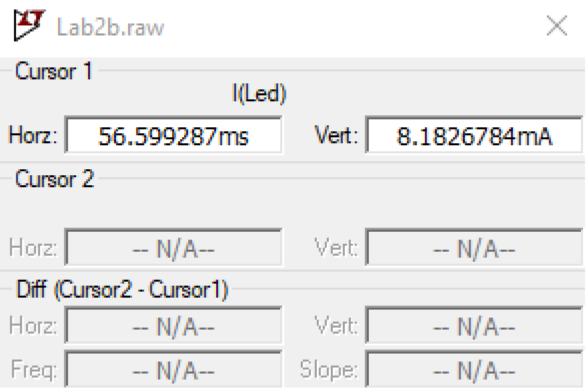


Figure 14: LED ON When Normal Output Current

TEMPERATURE ANALYSIS FOR BD136

Symbol	Parameter	Max value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	10	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	100	°C/W

Figure 15: Datasheet Values for BD136

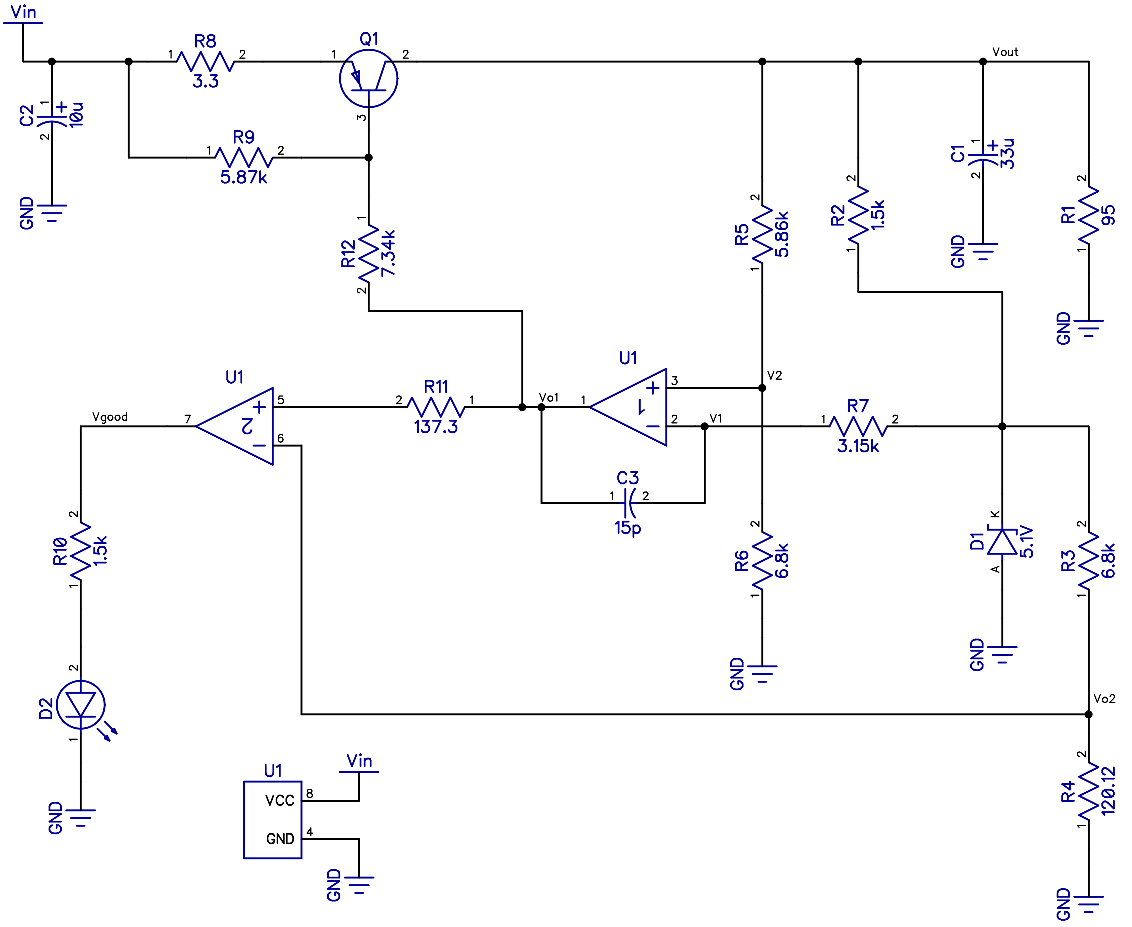
$$T_J = T_A + R_{\theta JA} P_D \text{ and } T_C = T_J - R_{\theta JC} P_D$$

where P_D is the power dissipation on the transistor ($P_D = (V_{in} - V_{out}) I_{out} = 0.3W$).

Since T_A equals 25°C, T_j = 55°C and T_c = 52°C.

DIPTRACE SCHEMATICS ARE AS BELOW

RevNo	Revision note	Date	Signature	Checked
		13.10.2024		



C1	33u	CAP100RP
C2	10u	CAP100RP
C3	15p	CAP100
D1	5.1V	DIO_ZENER
D2		LED
Q1		BD136G
R1	95	CFR25SJR-52-100K
R2	1.5k	CFR25SJR-52-100K
R3	6.8k	CFR25SJR-52-100K
R4	120.12	CFR25SJR-52-100K
R5	5.86k	CFR25SJR-52-100K
R6	6.8k	CFR25SJR-52-100K
R7	3.15k	CFR25SJR-52-100K
R8	3.3	CFR25SJR-52-100K
R9	5.87k	CFR25SJR-52-100K
R10	1.5k	CFR25SJR-52-100K
R11	137.3	CFR25SJR-52-100K
R12	7.34k	CFR25SJR-52-100K
U1		LM358N

Title
LDO Lab 2

Size	Number	Rev

Date
Filename
Drawn by
Emir Arda Bayer
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