EEE 313 Lab – 3
Single-Supply Push-pull Class-B Power Amplifier

Introduction

In this lab, a single-supply complementary push-pull Class-B power amplifier capable of delivering at least 0.95W to a 33Ω resistive load that had a chosen gain was designed on LTSpice and implemented on hardware that had certain requirements and specifications to operate as desired.

Purpose

The purpose was to achieve the following specifications in Figure 1 for a power amplifier with gain 22 dB (20+2) from sinusoidal voltages, and had Vcc = 24V for the – 3 dB bandwith covering 150Hz to 15kHz. The following design on LTSpice was created as in Figure 2.

Specifications:

1. The amplifier should deliver at least 0.95W power to a 33Ω resistance (16V_{pp} to a 33Ω power resistor) at 1KHz with the chosen gain value.
2. The harmonics (the highest is possibly the third harmonic) at the 0.95W output power level should be at least 40 dB lower than the fundamental signal at 1 KHz.
3. The power consumption at quiescent conditions should be less than 500mW.
4. The amplifier's efficiency (output power/total supply power) should be at least 40% at max power output (0.95W) at 1KHz.
5. The −3dB bandwidth of the amplifier should be at least 150Hz to 15KHz.

Figure 1: Specifications on the Manual

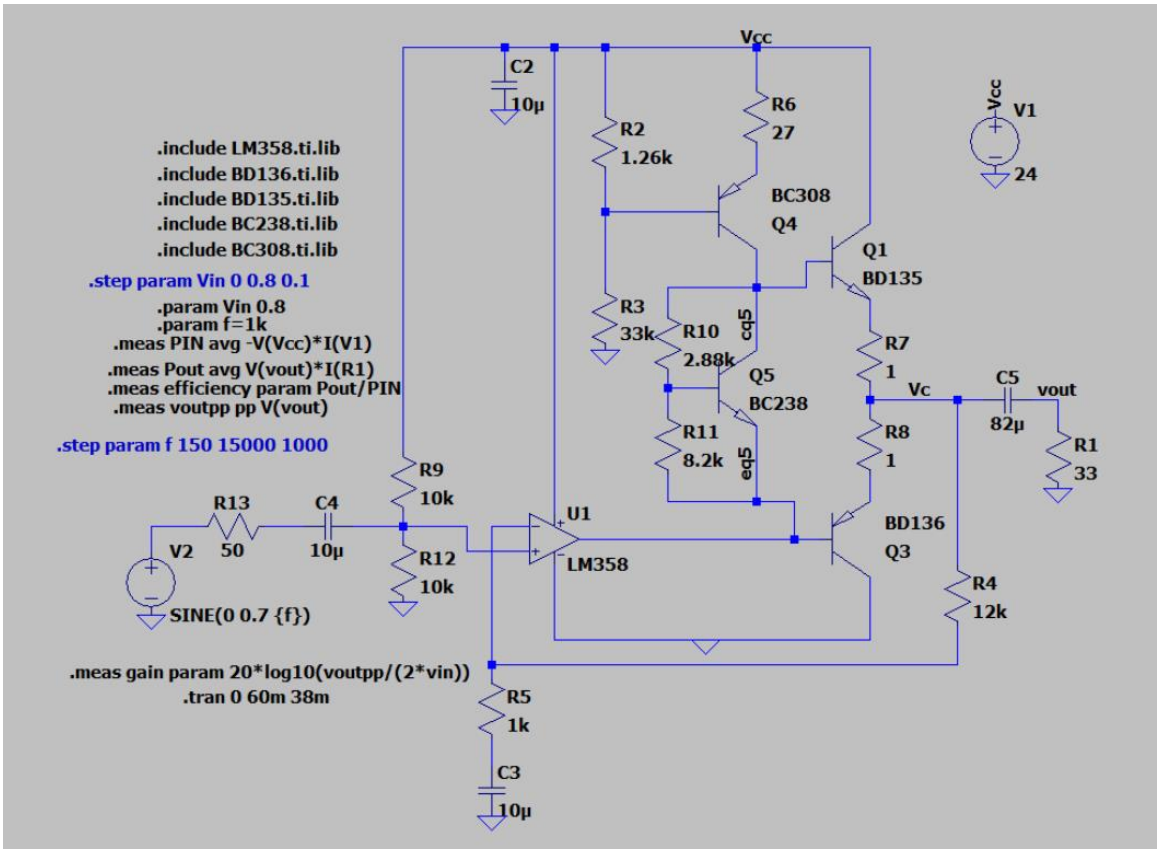

Figure 2: Design on LTSpice

Methodology and Design

As the desired requirements were met on simulation, the same circuit was implemented on hardware with the following lab setup in Figures 3 and 4. Later, the desired requirements were addressed. An 0.6V Vpp signal with changing frequency according to the requirements were given from the signal generator, whereas the DC supply is set to constant 24V.

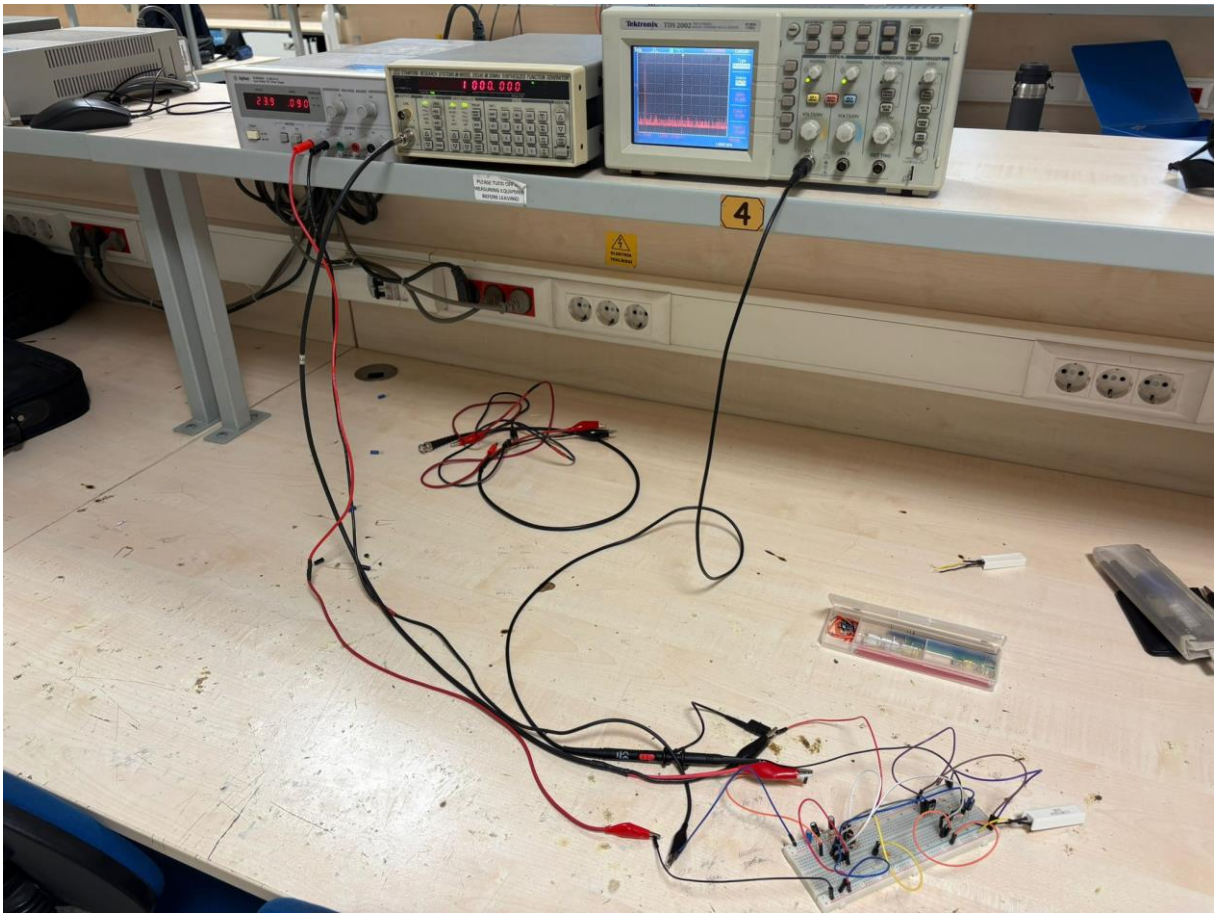

Figure 3: Hardware Setup

Figure 4: Inputs From Sources

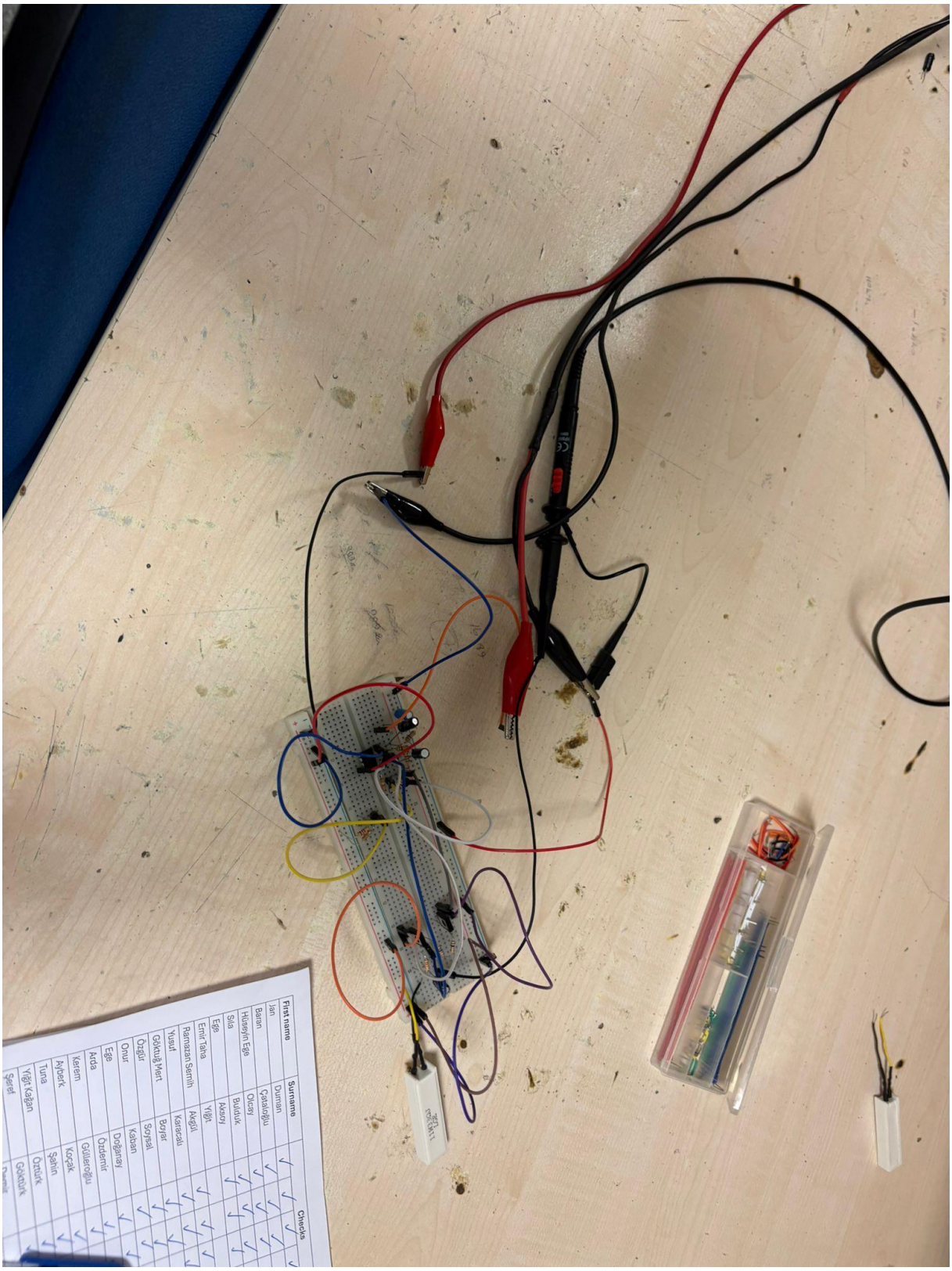

Figure 5: Breadboard Design

Requirements to be addressed:

REQUIREMENT 1

The amplifier should deliver at least 0.95W power to a 33Ω resistance ($16V_{pp}$ to a 33Ω power resistor) at 1KHz with the chosen gain value.

Figure 6 displays the voltage observed on node Vout (voltage on output resistor), to be used to calculate the power output.

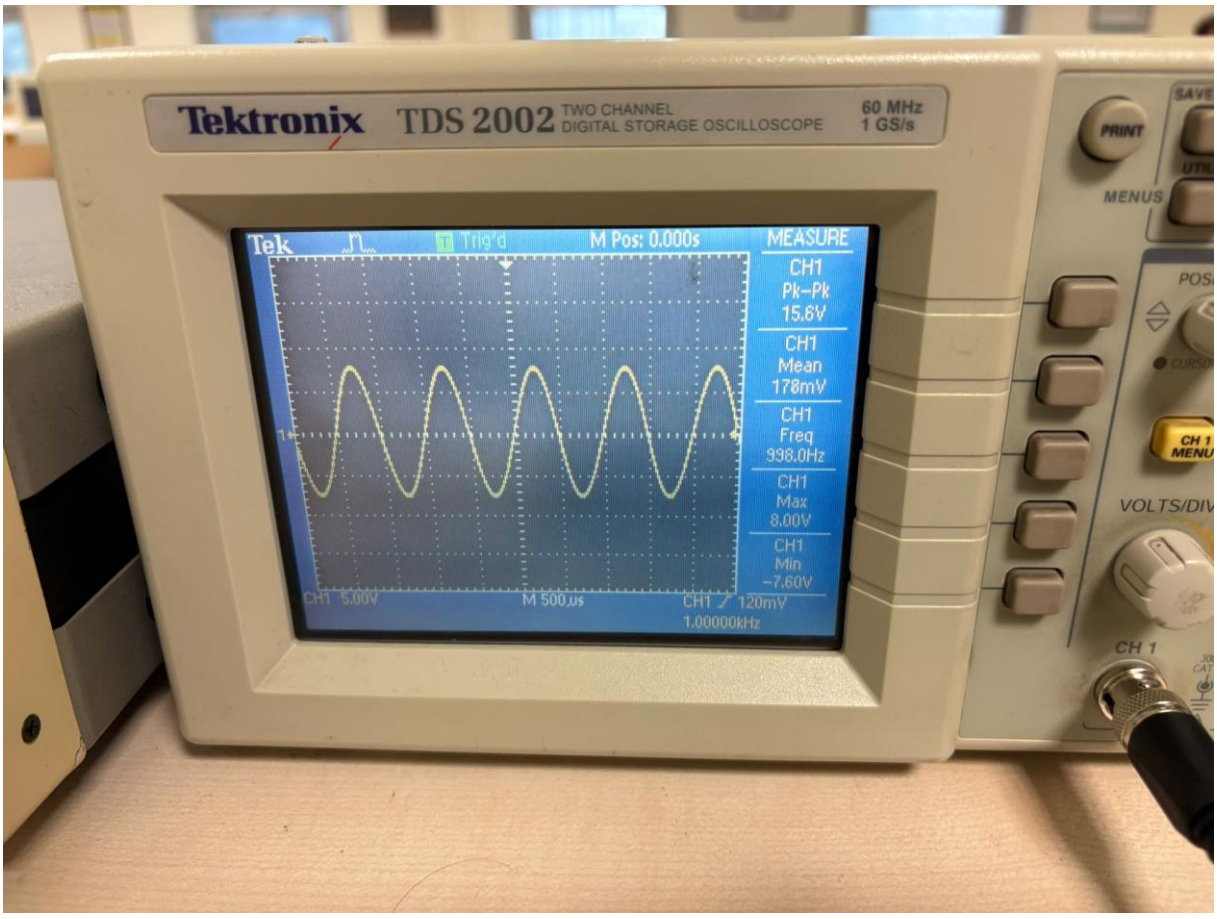

Figure 6: Voltage on Output Resitor for Req. 1

The desired Vpp for the output voltage is 16V, where it is 15.6V for the hardware implementation (2.5% error rate), satisfying the given condition for power. This output also implies that gain can be found with the following formula that satisfies the desired 22 dB gain:

$$20 \log\left(\frac{15.6}{2 * 0.6}\right) = 22.27886$$

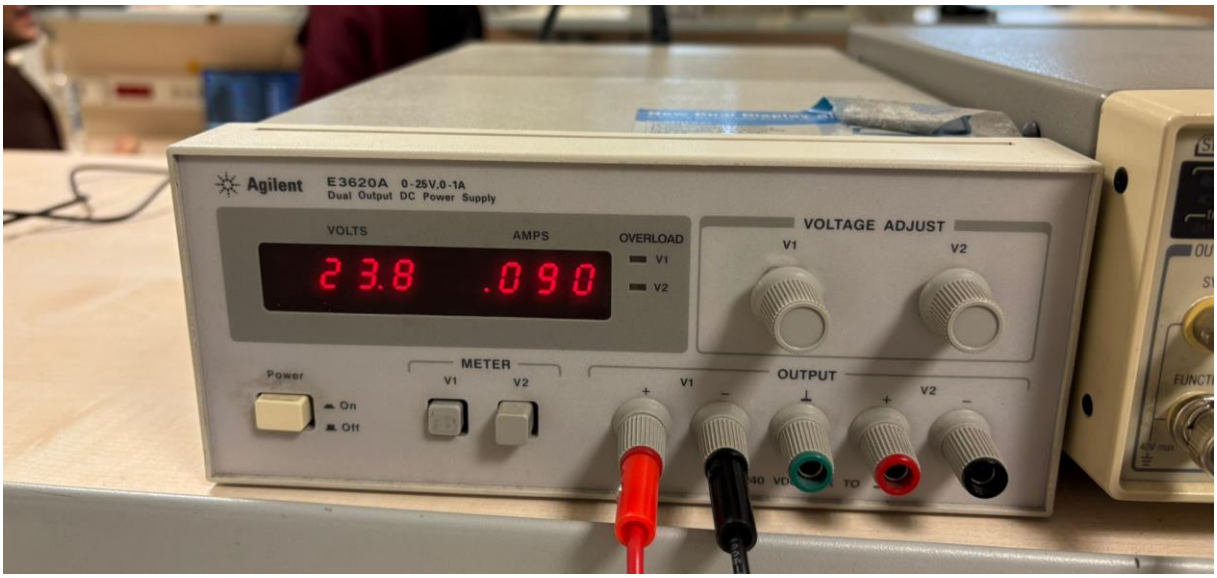

Figure 7: Input DC Singal for Req. 1

Figure 8: AC Signal for Req. 1 (Amp = 0.6V)

REQUIREMENT 2

The harmonics (the highest is possibly the third harmonic) at the 0.95W output power level should be at least 40 dB lower than the fundamental signal at 1 KHz.

The FFT function of the oscilloscope was used for the given requirement, and the first and third spikes were observed to later evaluate the gain difference between these harmonics. The output on oscilloscope is as Figure 9.

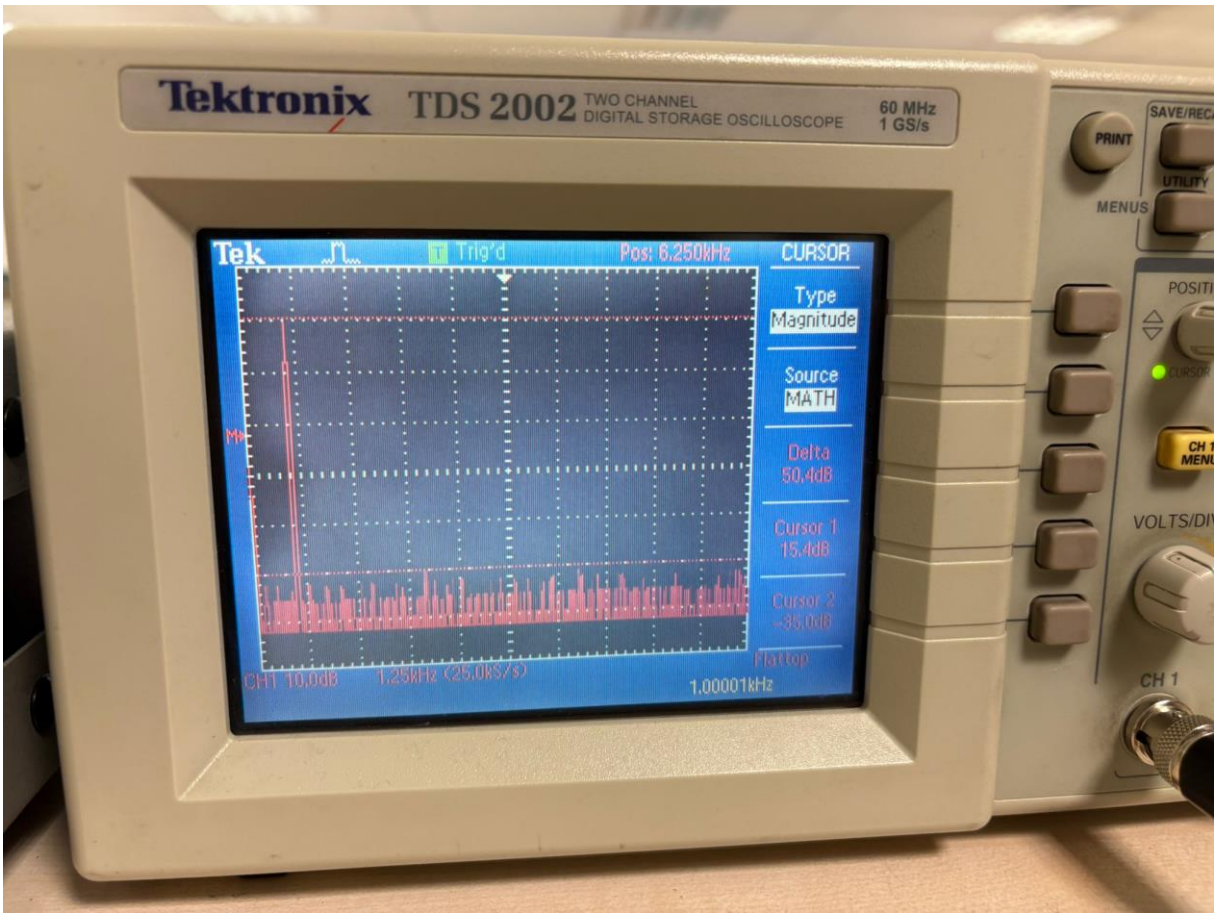

Figure 9: Output of FFT

These spikes are exactly placed at 1 kHz and 3 kHz where the first and third harmonics are placed, and as the delta on the oscilloscope displays there is a 50.4 dB difference satisfying the 40 kHz criteria.

REQUIREMENT 3

The power consumption at quiescent conditions should be less than 500mW.

The DC supply's voltage and the current that goes through it can be displayed from its display as in Figure 10 when quiescent condition is applied.

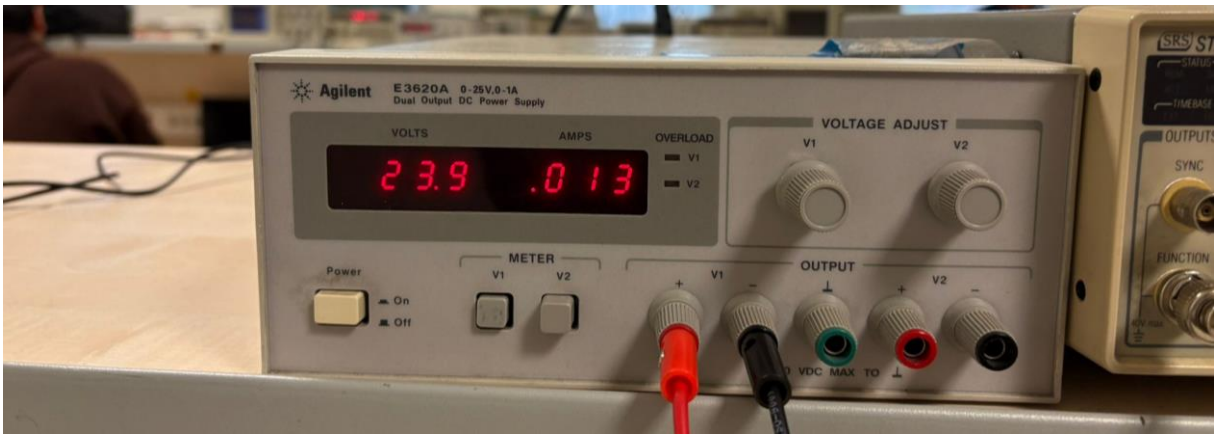

Figure 10: DC Supply under Quiescent Conditions

The power can be calculated by multiplying the voltage by the current as simply 23.9V x 13mV revealing a 311 mV power output, implying that the power consumption under quiescent conditions is below the criteria of 500 mV as desired.

REQUIREMENT 4

The amplifier's efficiency (output power/total supply power) should be at least 40% at max power output (0.95W) at 1KHz.

The maximum power output can be calculated as peak-to-peak voltage's square divided by 8 times output resistance. This equals 922 mW to be later compared with supply power from Figure 11.

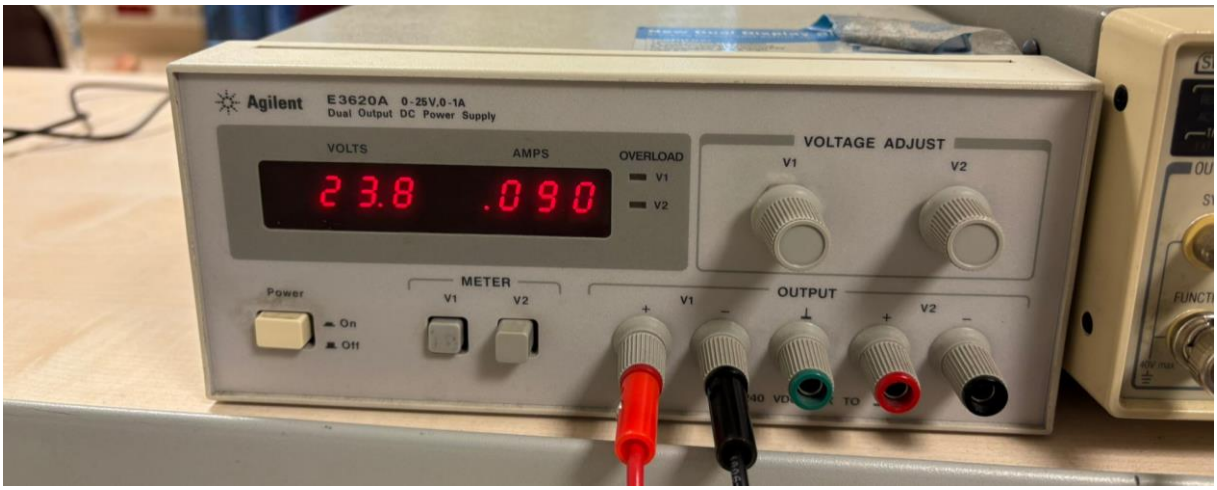

Figure 11: Voltage and Source for Source Power Calculation

23.8 V x 90 mA = 2.151 W, implying that the efficiency is 42.6%, above the required 40%.

REQUIREMENT 5

The –3dB bandwidth of the amplifier should be at least 150Hz to 15KHz.

The evaluated 15.6 Vpp has rms $15.6/\sqrt{2}=11.03$V. This implies that at the given frequencies the voltage value is required to be above 11.03V. These frequencies of 150 Hz and 15kHz, along with near frequencies were evaluated to meet the requirement. The input AC signal's frequency is changed several times to observe the output voltage as in Figures 12-17.

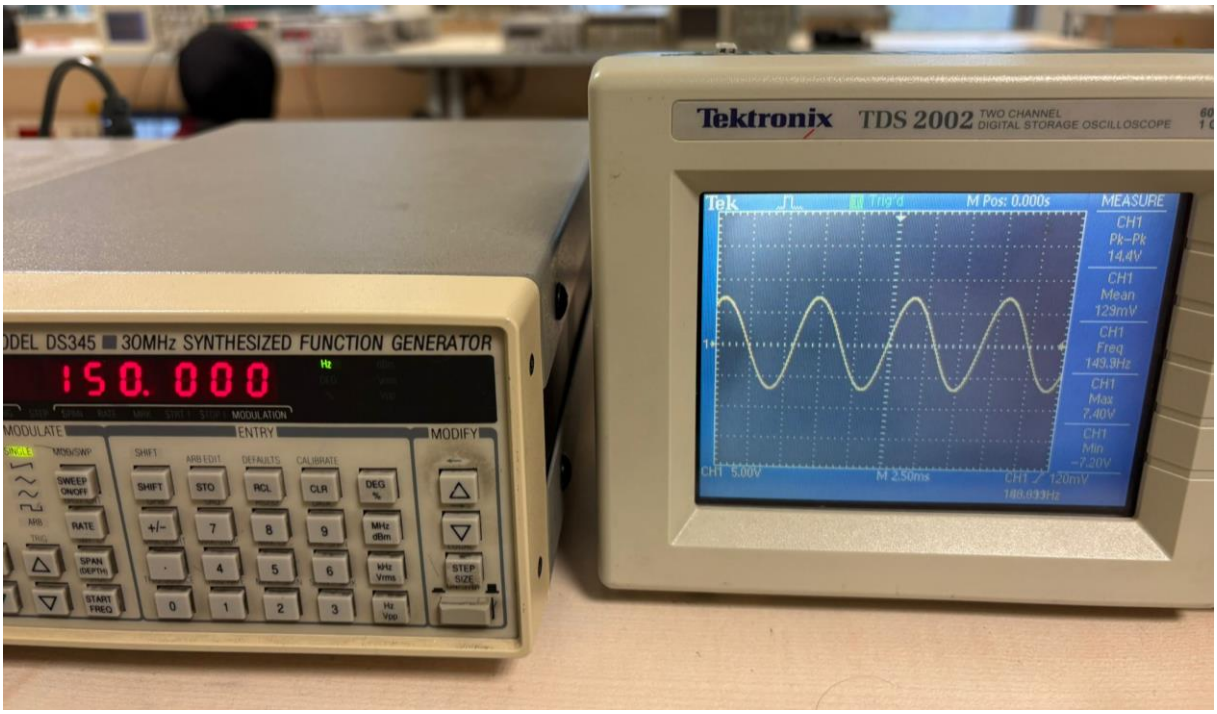

Figure 12: Frequency = 150 Hz (14.4V)

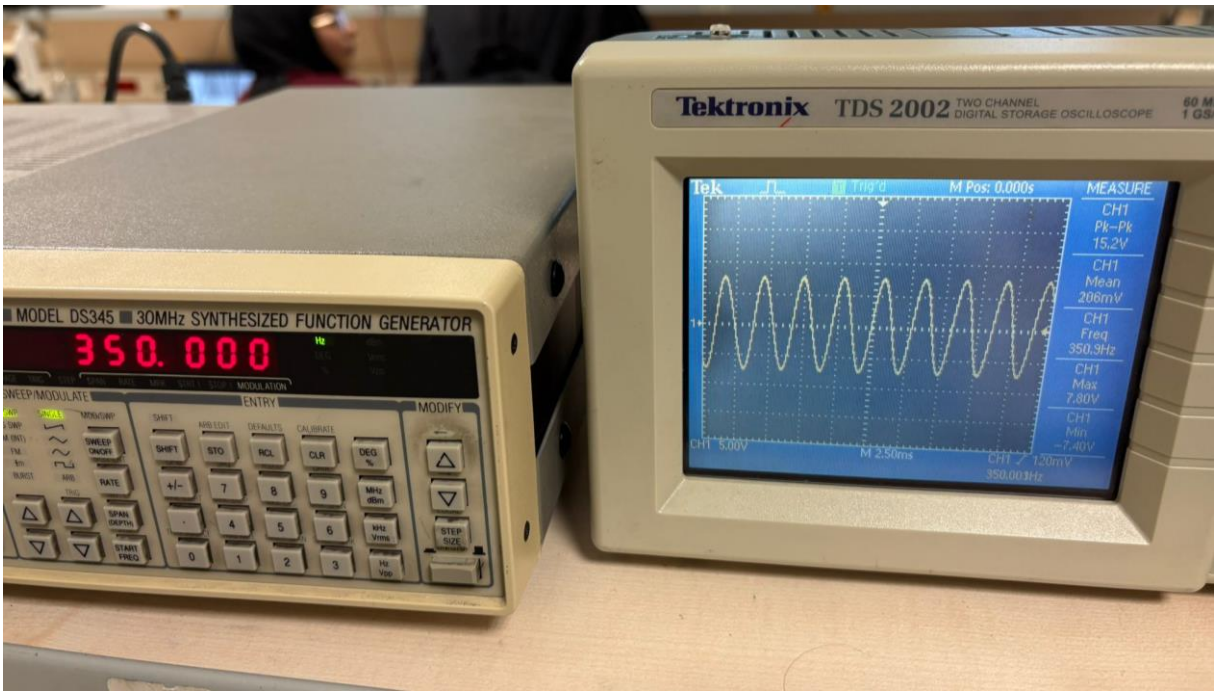

Figure 13: Frequency = 350 Hz (15.2V)

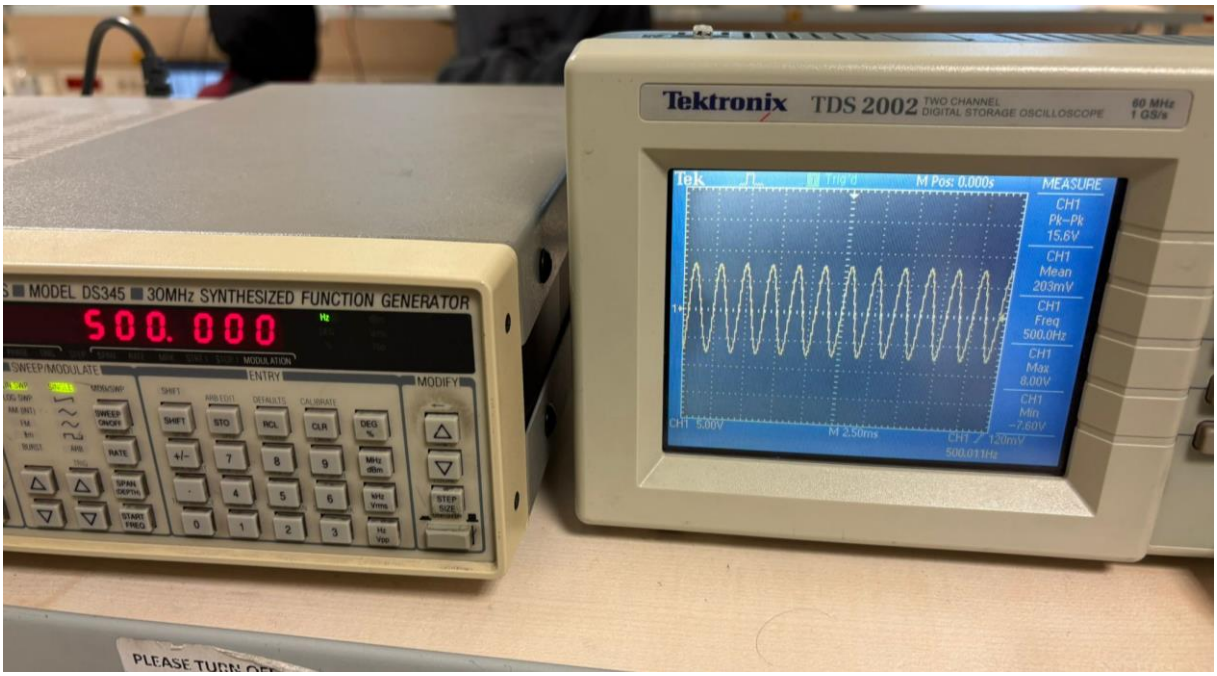

Figure 14: Frequency = 500 Hz (15.6V)

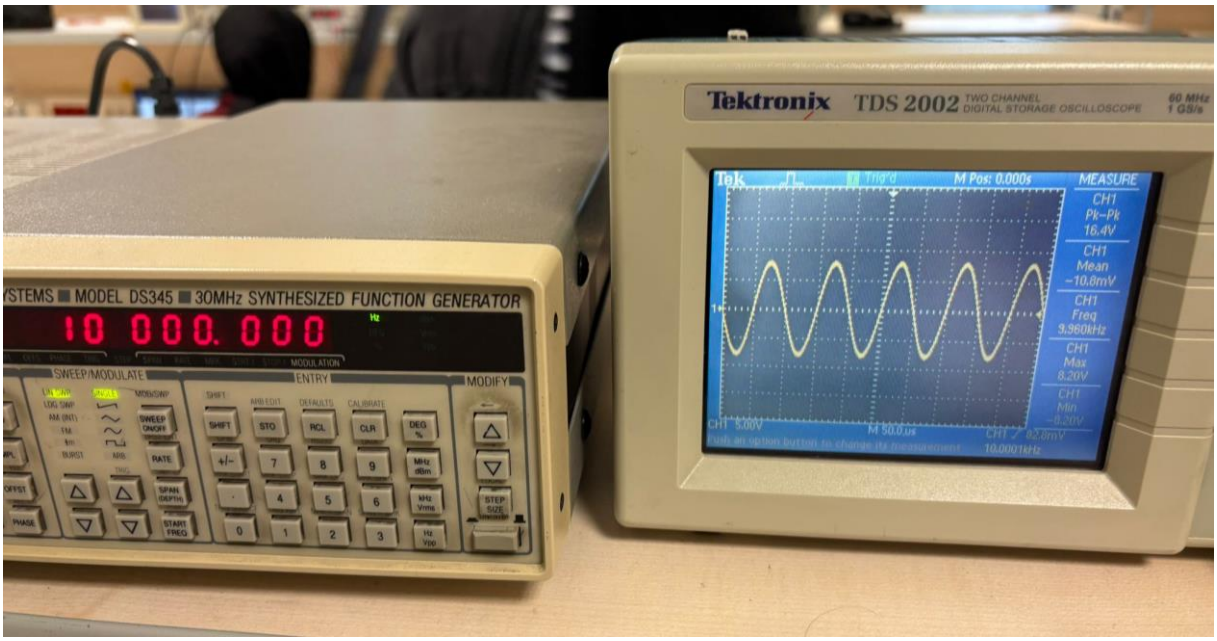

Figure 15: Frequency = 10 kHz (16.4V)

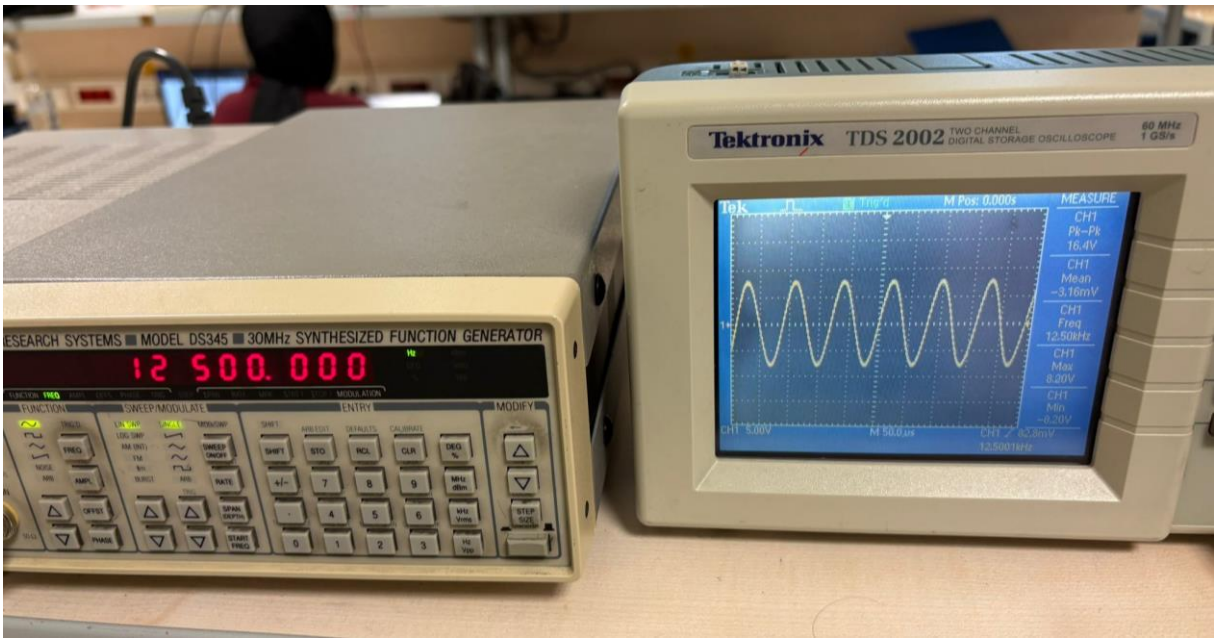

Figure 16: Frequency = 12.5 kHz (16.4 V)

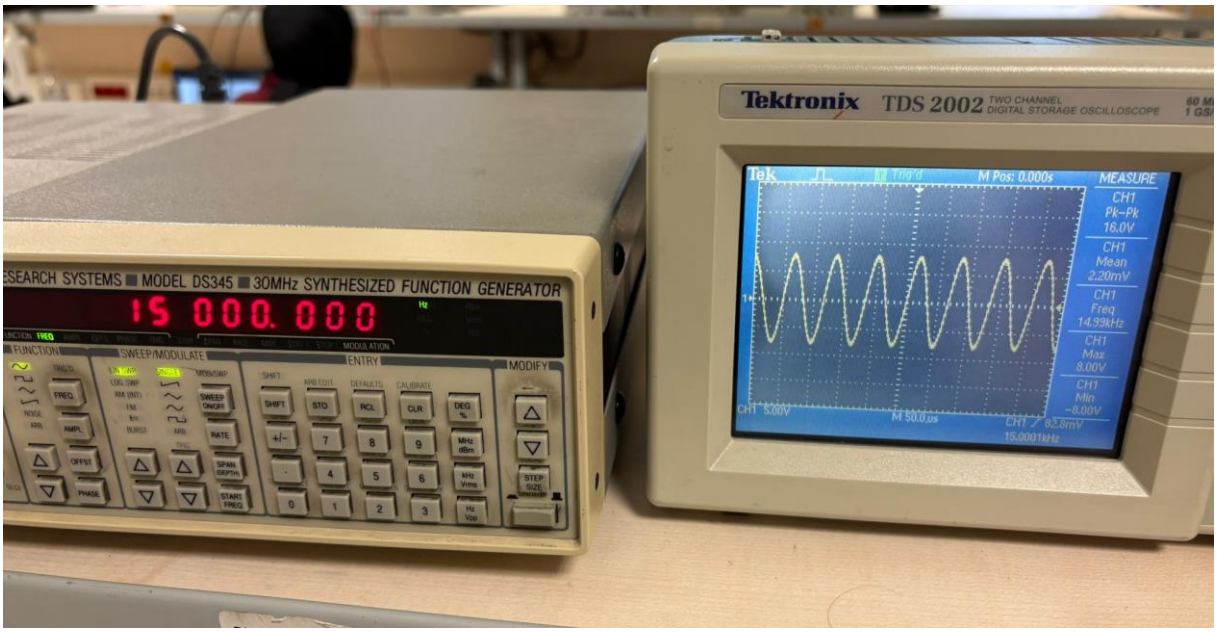

Figure 17: Frequency = 15 kHz (16.0 V)

Frequency (Hz)	150	350	500	10000	12500	15000
Output Voltage (V)	14.4	15.2	15.6	16.4	16.4	16
Gain (dB)	21.58	22.05	22.28	22.71	22.71	22.5

Table 1: Output Voltage Constantly Above 11.03V

As in Table 1, the output voltages are greater than 11.03V, satisfying the given requirement of minimum bandwidth for the amplifier. Below are the plots for the efficiency and gain.

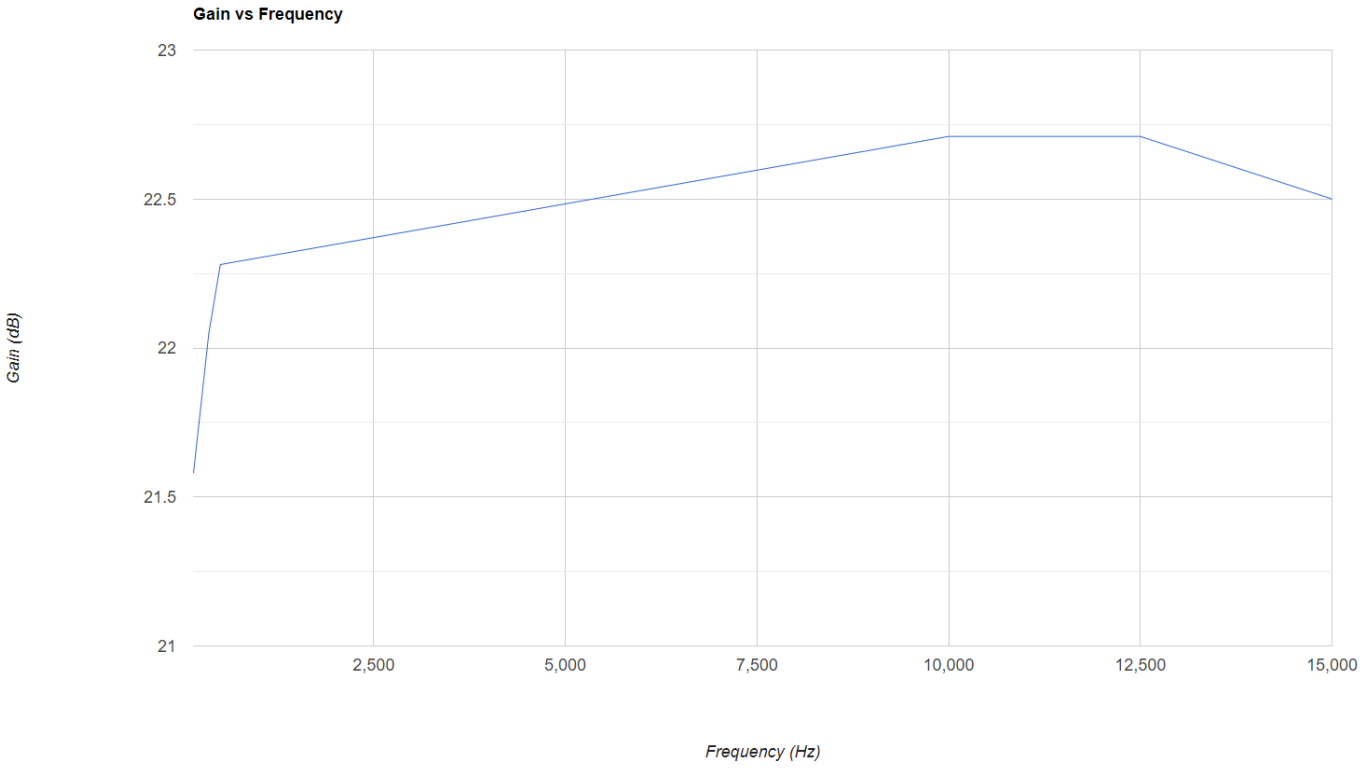

Figure 18: Gain vs Frequency Graph

The desired gain was 22 dB and was found as 22.28 dB for the hardware implementation. The cutoff frequencies are for this reason 25.28 dB and 19.28 dB.

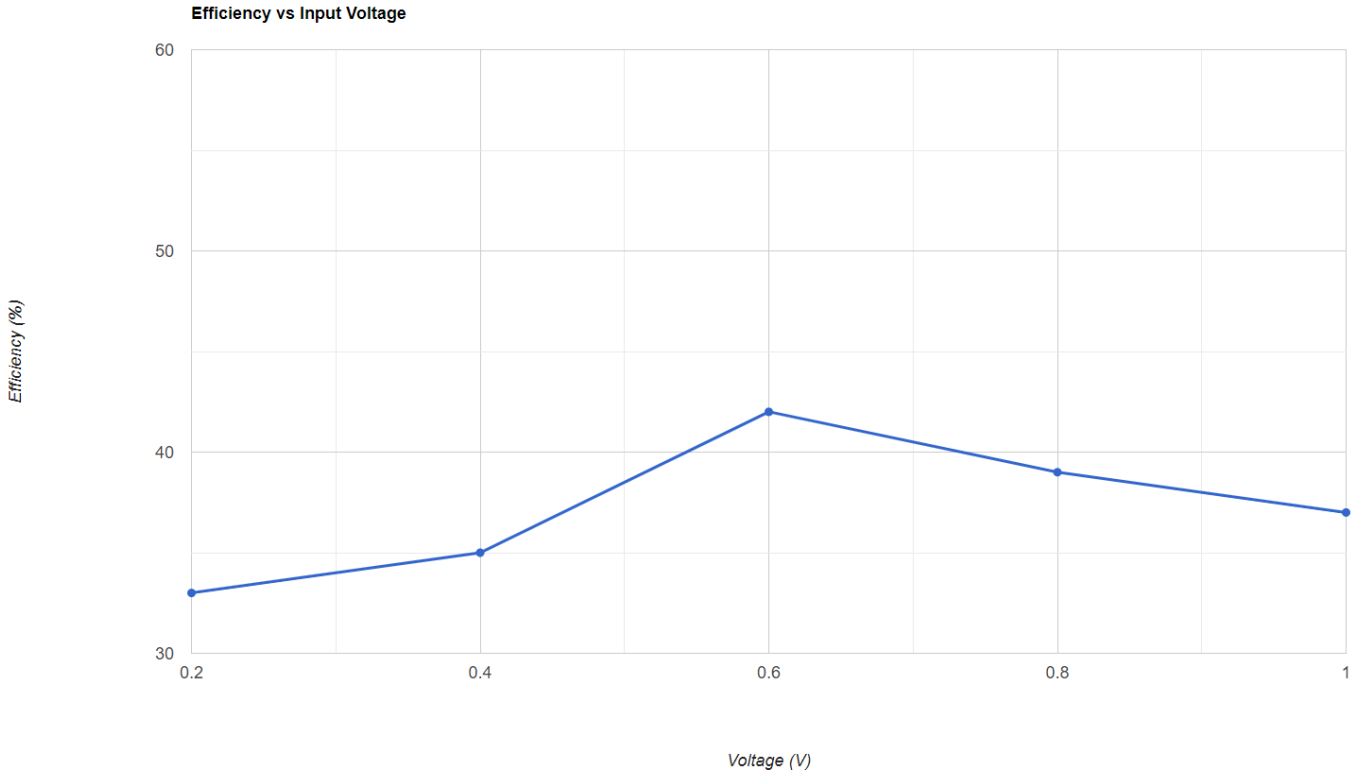

Figure 19: Efficiency vs Input Voltage Graph

Conclusion

All of the given requirements were satisfied and the desired plots were plotted. This lab was beneficial in terms of learning about power amplifiers, as we designed and implemented individual class B power amplifiers with personal gains, and changing characteristics for changing inputs.