2.05.2024 Emir Arda Bayer
22201832-4

Lab 7: Finite State Machine

Purpose

The goal of this lab was to make use of flip flops and combinational circuit elements in order to experiment and learn about finite state machines (FSM). In this lab, students made use of D type flip flops and learned its use in electronics as memory tools on breadboard designs of FSMs. They also had the chance to create the state transition diagrams for their designs.

Design

The proposed design is highly similar to a locking system that can be found in any conventional field such as cars. When the user pressed the only input button the system changes state, becomes locked if unlocked and vice versa. LED keeps turned on if the system is locked, and the D type flip flop keeps this data.

The system had a single input and a single output, one input button for changing the state (locked or unlocked) and one output LED for displaying the current state. This design is also a Moore machine since it does not depend on the initial values of the system. The button is connected to a transitionary LED that displays when the button is pressed, and this data goes to the input of an XOR gate. The other input of the 2 input XOR gate is the output Q of the D flip flop. The reason for selecting an XOR gate as the input is because the boolean expression $Q^+ = QX' + Q'X$ simplifies to a simple xor operation of Q and X.

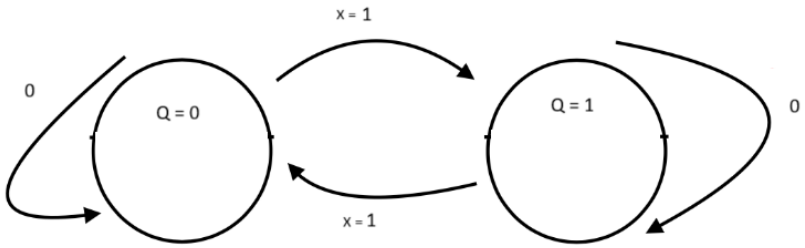

Figure 1: State Transifion Diagram of the Design

STATE 0 (UNLOCKED)	X	Q
	0	0
	1	1

Table 1: State Diagram of Unlocked State

STATE 1 (LOCKED)	X	Q
	0	1
	1	0

Table 2: State Diagram of Locked State

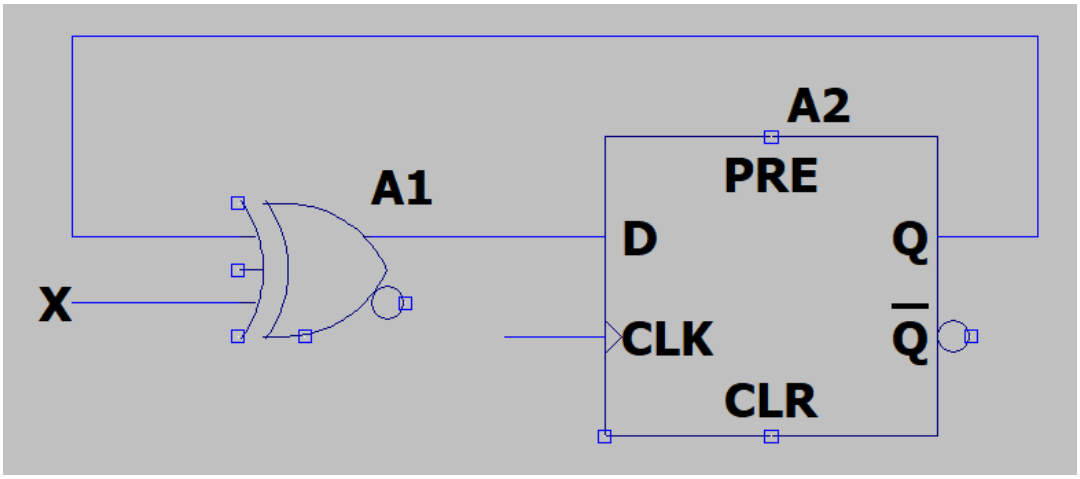

Figure 2: FSM Design

Methodology, Results

Having found the Boolean expression of an XOR operation involving the input X and the output Q of the D flip flop, the design was implemented on the breadboard using one 74HC74 D-type flip flop and one two input 74HC86 XOR gate. The Vcc and GND pins of both gates were connected to the consecutively + and – sides of the breadboard to later take voltage from the DC power supply, and 1CLR, 1PRE pins of the flip flop were also connected to the plus side. The CLK input of the flip flop was connected to the + of the signal generator cable, and its ground was at the – side of the breadboard. Lastly, the X input of the XOR gate was connected to the LED-button circuit on the end of the breadboard that was connected to the + side, and the other input was connected to the output Q of the flip flop. The output of the XOR gate was connected to the D input of the flip flop. The Q output was also observed with a red LED circuit with a jumper to observe the state.

Making the connections to the power supply and signal generator, the system worked as expected. The following are the pin diagrams of the gates and the states of the design on the breadboard.

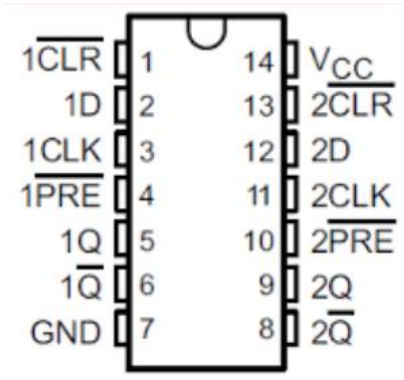

Figure 3: 74HC74 Pin Diagram

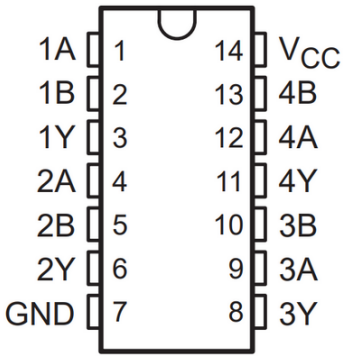

Figure 4: 74HC86 Pin Diagram

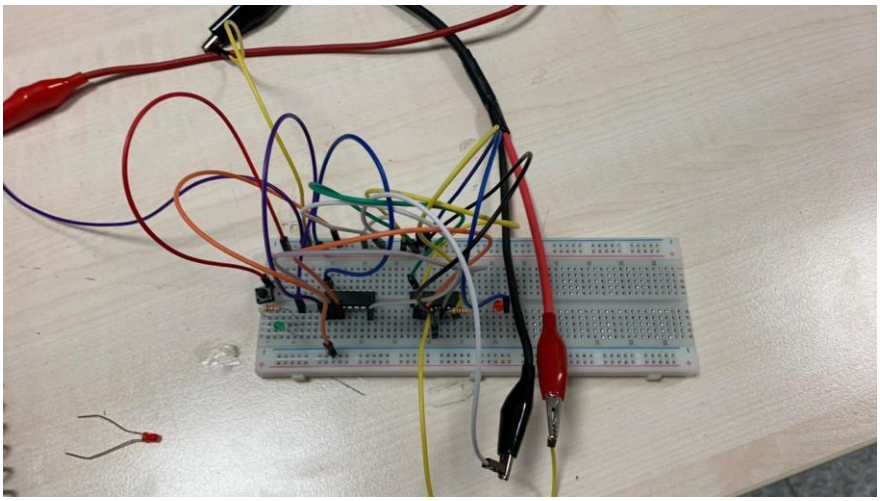

Figure 5: State 0, X = 0

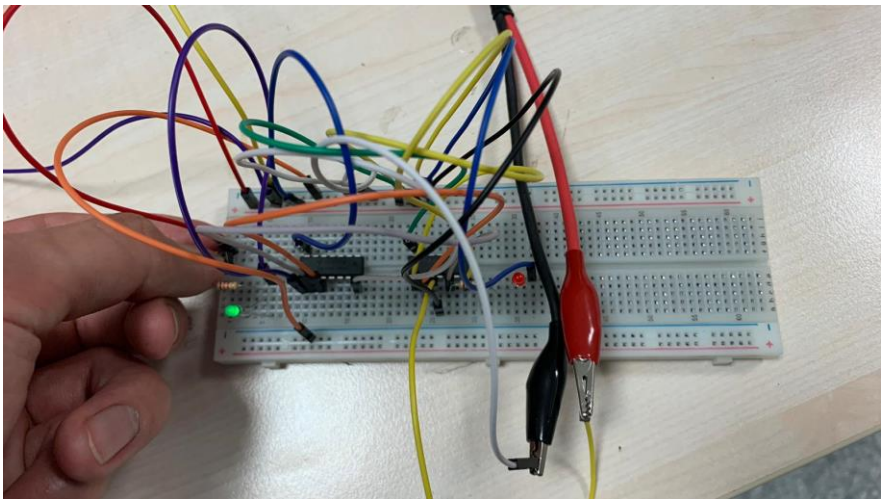

Figure 6: State 0, X = 1

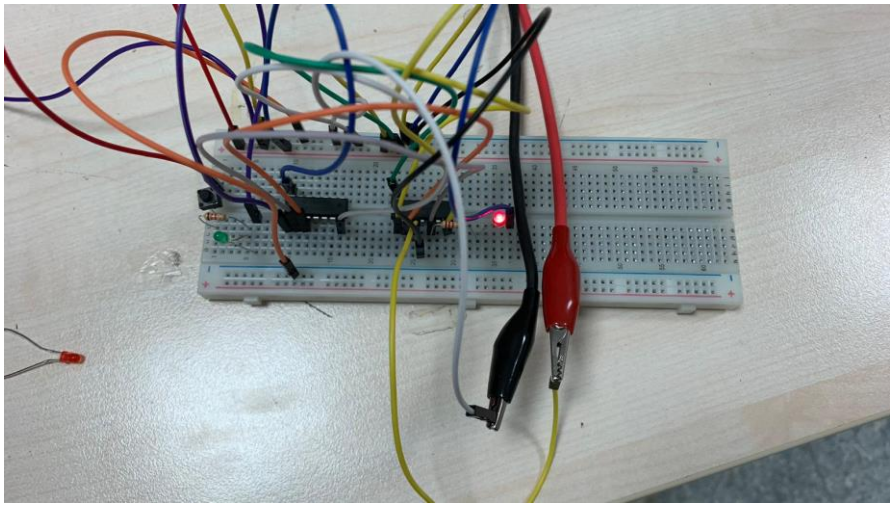

Figure 7: State Becomes 1, LED is on

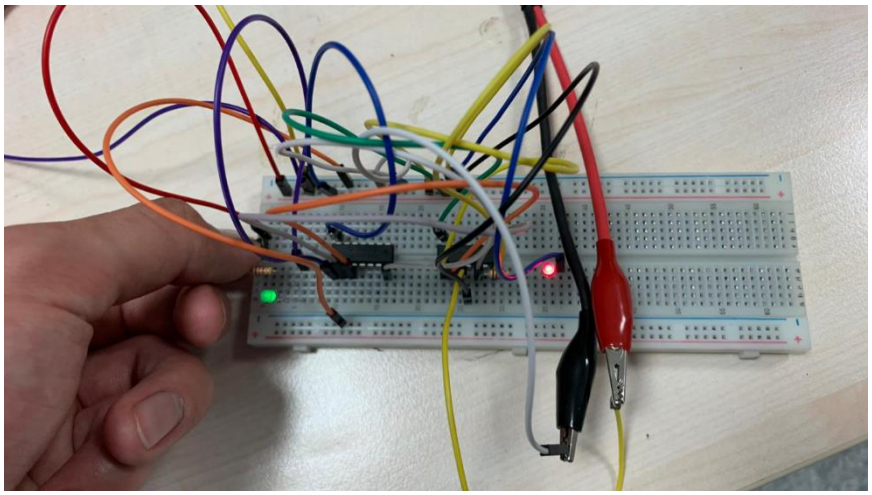

Figure 8: State 1, X = 1

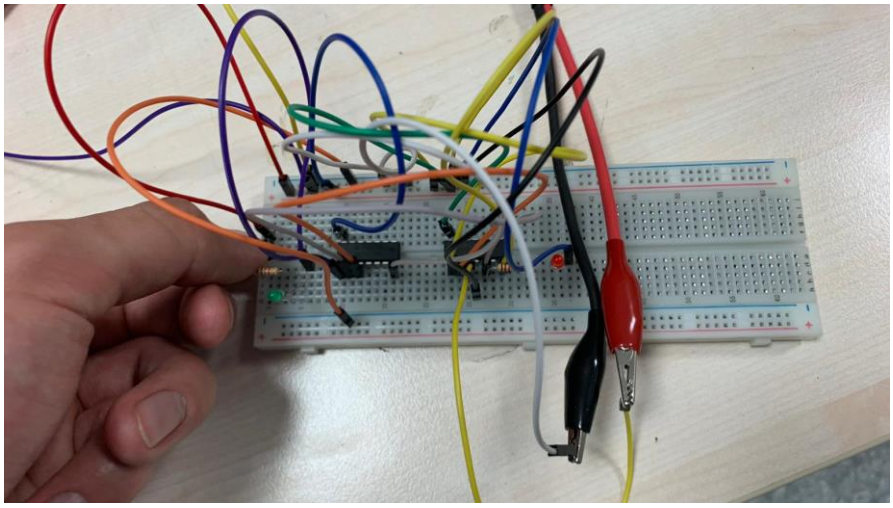

Figure 9: State Back to 0

Conclusion

The purpose of the 7th Lab was to teach students about flip flops, finite state diagrams and most importantly FSMs, while making them understand their principles by designing combinational circuits on breadboards. This taught them about D type flip flops and how they act as memory elements in electronics. The seventh lab was difficult in the sense that there were many steps and multiple jumpers were used. I made the error of connecting the button in the wrong order on the breadboard as it got short circuited, but I fixed it by plugging it through the empty side at the half of the breadboard, the transitionary green LED was constantly on before the change. This lab was useful for me because I learned about FSMs, spesifically D type flip flops, state transition diagrams and had the opportunity to make use of Boolean algebra with the given lab equipment and physical gates, useful concepts for someone learning about electronics.

References

https://www.eecs.tufts.edu/~dsculley/tutorial/flopsandcounters/flops1.html#:~:text=CLK%2%200is%20the%20clock%20pin,edge%20of%20the%20clock%20pulse

https://nick.blog/2017/04/08/using-a-74hc74-integrated-circuit/

https://www.crcibernetica.com/74hc86-xor-gates/

https://www.geeksforgeeks.org/d-flip-flop/