Full Custom Design in VLSI

A Seminar paper on the Full Custom Design approach in VLSI

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***Abstract*—Chip design in electronics is becoming increasingly complex and has already reached a state at which it is impossible to design a modern chip without a really capable team of engineers as well as numerous tools and design approaches to help decrease cost and development time. Semi custom design in VLSI, which is reusing older components in standard cell libraries has become the standard for most chip development processes, as it saves a vast amount of time and costs. VLSI with full custom design is not fully practicable anymore looking at bigger projects, but it still has its uses for smaller components or small systems in modern chip design, because full custom designed circuit generally have a higher performance than semi custom designed ones. With the current developments and Moores law still holding true to some extent, full custom design in VLSI faces big challenges. Overcoming these challenges might not be entirely possible, but it is instead important to determine the aspects in chip design in which full custom design can still be more beneficial in an otherwise semi custom designed chip.**

***Index Terms*—Full custom, Semi custom, Integrated Circuit, Design, Design flow, Electronics, VLSI**

I. Introduction

A tiny semiconductor-based electronic device made up of fabricated transistors, resistors, and capacitors is called an integrated circuit (IC). The fundamental components of the majority of electronic equipment and devices are integrated circuits. These ICs are part of almost every electronic device that we use today. Since the upsurge of digital technologies, the core components used for building digital circuits, the transistors, have gotten smaller and smaller. While getting smaller and more efficient, building digital circuits also became more complex over time and different design approaches were sought after. The general process of designing an integrated circuit is called Very large scale integration (VLSI) and it is a time intensive task only doable by an competent and coordinated team of engineers. It is important to note that VLSI is generally meant for circuits with 10.000- 100.000 transistors, however it is also used to describe designs that use far more transistors [1] [2].

For most circuits today, there are mostly 2 approaches for developing an ASIC:

1) semi custom design
2) Full custom design

Semi custom design aims to speed-up the design phase for circuits with high performance requirements. To achieve that, not everything is designed anew and common components like adders, memory elements or multiplexers are bought from vendors in the finished state. Therefore the design team only has to design the elements around the already bought components and can save a lot of time. Using FPGA functionalities to develop the intended system also falls under this category. While this approach can be fast and efficient alot of times, it might not be able to fulfill performance requirements every time. The second design approach, full custom design, focuses on improving in this part since it completely avoids reusing any components. Every element of the digital circuit is done without Hardware description languages or reusage of elements. Of course, designing an entire system in 2023 with a full custom design approach will be almost impossible since most systems (especially high performance) have millions to billions of transistors on a single chip. However, it can be really beneficial if smaller components are designed in a full custom design approach, thus potentially improving elemental parts of the overall system. furthermore certain components will be designed from the bottom up and can therefore be perfectly adjusted to the customers or company's needs. While this process takes a significant amount of time, it usually provides a higher performance for the affected circuits in comparison to the semi custom approach and more efficient hardware. This Paper focuses on Full Custom Design in VLSI while diving into VLSI itself and the differences from the semi custom design approach

A. History of VLSI

The integration of transistors on chips started in a small scale and continued growing due to moores law.

- Small-scale integration (SSI) technology emerged in 1960 and integrated 1-100 transistors on a single chip, e.g. Gates, flip-flops, op amps also seen in figure1 [2].
- Medium scale integration (MSI) developed in 1967 by integrating 100-1000 transistors on a chip, e.g Counters, MUX, 4-bit microprocessor also seen in figure 1 [2].
- Large scale integration (LSI) started in 1972 by integrating 1000-10000 transistors on one chip, e.g 8 bit microprocessors, ROM also seen in figure 1 [2].

- VLSI technology emerged in 1978 and integrates more than 10000 transistors on a single chip as mentioned earlier. It is the most common term used today even for chips with millions of transistors, although these also seperate terms. Examples are older microcomputers, peripherals and 16-32 bit microprocessors [3] [2].
- Ultra large scale integration (ULSI) technology integrates 1-10 million transistors on a single chip, e.g special purpose processors [2].
- Giant scale integration (GSI) integrates more than 10 million transistors on a single chip and is generally used for embedded systems or system on chip [2].

II. VLSI

The term VLSI refers to the amount of functionality integrable on a chip with current fabrication processes. As mentioned earlier, smaller scale chip designs used the lower grade terms such as SSI , MSI and LSI seen in Figure 1.

Table 2.
Components realizable at each level of circuit density.

	Combinational circuits	Sequential circuits
SSI	Gate	Flip-flop
MSI	Adder, multiplexer, encoder, decoder	Register, counter
LSI	ROM, PLA	RAM, PLA, microprocessor, PIO, USART
VLSI	ROM	Microcomputer, multifunctional devices

Fig. 1. Showcase of the used terms and their respective circuits in 1987 from [3].

The engineering resources required to create a VLSI design depend on the complexity. However, determining the complexity of a VLSI design is a challenging task in project difficulty estimation. Insightful comparisons can be drawn between the resources required for earlier designs if a similar methodology was applied. The ability to reuse current physical and logical intellectual property is a key factor to take into account when creating a project plan [1].

Having done the complexity determination, different objectives exist for the design to fulfill. These are typically:

- Power (power dissipation value) for determining aspects like battery life, electrical delivery and cooling. To fulfill this objective, power calculation flows are used [1].
- Performance (Clock speeds) like clock frequency or periods as well as timing constraints [1].
- full-chip area (PPA targets) determining the the final product cost [1].

A. VLSI Design Methodology and flow

Figure 2 illustrates the many hierarchical levels of a typical digital IC design flow. The flowchart depicts a generalized design flow that includes the front-end and back-end of full-custom/semi-custom IC designs [4]:

- The functionality, user interface, and general architecture of the digital circuit that needs to be designed are all described in abstract form in the design specifications. The functional description, timing requirements, propagation delays, necessary package type, and design constraints are all shown in block diagrams. Furthermore, they serve as a contract between the vendor and the design engineer [4].
- The fundamental architecture of the system is included in the architectural design level. A micro-architectural specification containing the functional descriptions of subsystem units is the result of this level.
- The functional description of the design is provided at the next level, the behavioral design level, which is typically written in Verilog HDL/VHDL. Using HDLs technically makes the design not full custom, however, it has become standard to use these tools even if the aim is to create a custom chip or component. Here, the functionality is described at a high level in the behavioral level, concealing the implementation details below. It is also possible to use High level synthesis tools (HLS), i.e. a tool that automatically converts high level language such as C or C++ code into the needed HDL.
- The netlist, or gate-level description for the high-level behavioral description, is generated by the logic synthesis tool. The gate-level netlist's compliance with the timing, area, and power requirements is guaranteed by the logic synthesis tool.
- Floor planning, placement, and routing are then carried out, after which large and complex systems are divided into smaller modules by means of system partitioning. The floor planner's main function is to estimate the amount of chip area needed to implement standard cell/module designs. It also handles optimizing the performance of the designs. Each block's routing is then carried out.
- Layout verification is the process of checking if the designed layout complies with the source schematic and electrical/physical design guidelines after placement and routing. The application of these procedures makes use of instruments like electrical rule check (ERC) and design rule check (DRC).
- The chip goes to the sign-off stage after the post-layout simulation, which is where parasitic resistance and capacitance extraction and verification are carried out [4].

Ultimately, There is more to the design methodology than just the steps that need to be taken. It also describes the model build configuration to represent the complete chip logical and physical definitions, as well as the policies in place for chip hierarchy data management. The use of electronic design automation (EDA) software tools at each stage, along with software for design data management and revision control is a crucial component of the design methodology. Furthermore

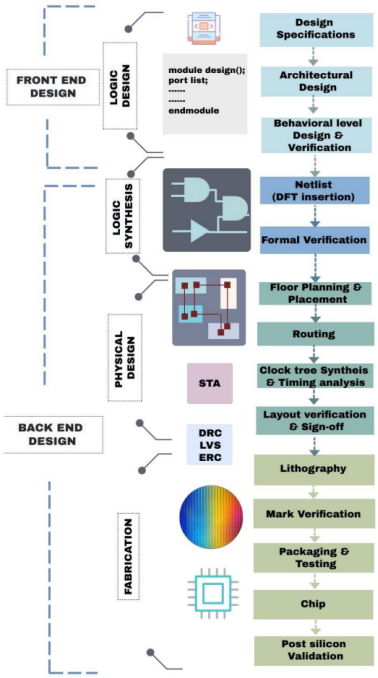

Fig. 2. Typical design flow of a modern chip leaving out CAD/VLSI Tools from [4].

it is important to manage the output formats of the files in the design methodology to be ready to be submitted to the next tool in the design flow or if it is the final chip design, the submission for fabrication. While the design methodologies for VLSI have not changed substanntially over the years, specific tools and data model features have changed constantly [1].

III. Future of Full custom design and VLSI

Considering the increasing amount of automation tool that are developed and used in VLSI and the unfathomable complexity of modern high performance processors, it is safe to say that modern chip development will most likely never be done again using the full custom design approach in a manner where the entire system is developed in that way without any standard cell libraries and general helptools. The obvious exceptions to this could be small systems like ALUs, Counters and Frequency Dividers, Digital-to-Analog converters and conversely Analog-to-Digital Converters and more.

The future of chip development could be defined by the recent AI breakthrough as it could take on several tasks for engineers during development and make help tools even more helpful.

A. AI in VLSI

Numerous issues have been effectively solved by artificial intelligence in a variety of fields. Artificial intelligence (AI) is based on the idea that human intelligence can be easily mimicked by machines to perform tasks of varying complexity. [3] AI includes machine learning (ML) as a subset. Learning, reasoning, predicting, and perceiving are the objectives of AI/ML. Large data sets can be quickly analyzed by AI/ML to find trends and patterns that help users make informed decisions. High computational speeds can be achieved by AI/ML algorithms when handling multidimensional and multivariate data. As these algorithms gain experience, their prediction accuracy and efficiency increase steadily. Additionally, they aid in decision-making by streamlining pertinent procedures. AI/ML algorithms have countless applications due to their many advantages [4].

A subset of machine learning, deep learning is especially well-suited for processing large amounts of data. The computer can create complex concepts from simpler ones thanks to deep learning. Quick advancements in various AI/ML domains are expanding the possibilities for developing solutions to tackle a wide range of diverse issues related to integrated circuit design and production. The applications of AI/ML at various abstraction levels of VLSI design and analysis—beginning with circuit simulation—are covered in the sections that follow [4].

An essential component of modeling IC devices is simulation. Because of the growing number of process and environmental variations, performance evaluation of designed circuits through simulations is becoming increasingly difficult in the nanometer regime. The potential of the simulation tools to identify functional and electrical performance variations early in the design cycle can increase the integrated circuit yield. Through the integration of AI/ML algorithms' automated learning capabilities with E-CAD tools, it is possible to improve chip performance and turnaround time while requiring less design work [4].

IV. Conclusion

Full Custom Design in VLSI has been the main approach to designing chips in the past, but as times have changed, systems have become more complex and numerous automation tools have been developed to assist in developing especially complex systems. Therefore, the semi custom design approach utilizing standard cell libraries, gate arrays and FPGAs has become the standard approach to developing more complex systems. Despite all that, smaller systems will and certain components of more complex systems will still benefit from a full custom design approach.

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Statement of authorship

Hereby, I declare that I have composed the presented paper independently on my own and without any other resources than the ones indicated. All thoughts taken directly or indirectly from external sources are properly denoted as such.

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