A 12-GHz High-Efficiency Tapered Traveling-Wave Power Amplifier With Novel Power Matched Cascode Gain Cells Using SiGe HBT Transistors

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***Abstract*—In this paper, we present the analysis, design, and implementation of an integrated power distributed amplifier (DA), fabricated in a low-cost 0.25-μm SiGe BiCMOS technology. The circuit consists of four novel inductively peaked cascode gain cells, which are capacitively coupled to the base line for power optimization and bandwidth enhancement. Due to the tapered collector line, no output termination resistor is required, which provides higher efficiency. Design tradeoffs for maximum bandwidth, gain, output power, and efficiency are discussed by means of analytical calculations and simulations. A gain of 11 dB with a gain flatness of ± 1 dB has been measured over a frequency range from 1 to 12 GHz. 19.5-dBm output power is obtained at the 1-dB compression point ($P_{1\,\mathrm{dB}}$) in the desired frequency range with an associated power-added efficiency of 22.1% and a maximum output third-order intercept point of 31.5 dBm. The power dissipation of the amplifier is 400 mW from a 5-V supply. On-chip biasing is implemented via low dropout voltage reference driven by a bandgap voltage source. To the authors' knowledge, this is the highest output power achieved by an HBT DA in SiGe technology in this frequency range. The chip size is 2.1 mm^2. Good agreement between simulation and measurement were achieved.**

***Index Terms*—BiCMOS, distributed amplifier (DA), integrated circuits, power amplifier, traveling-wave amplifier (TWA), silicon germanium (SiGe).**

I. Introduction

ULTRA-WIDEBAND (UWB) has received significant attention as a promising and strongly evolving technique for high data-rate communications, high-resolution short-range radar sensors, and high-precision local positioning systems. By spreading the signal power over a wide range of the radio spectrum, large frequency diversity, high spatial resolution, and high sensitivity can be achieved. Distributed amplifiers (DAs) are appealing aspirants for UWB systems due to their inherently large bandwidth. The two major challenges in designing distributed power amplifiers are maintaining high linearity over the entire bandwidth since narrowband linearization techniques cannot be utilized and achieving high output power and efficiency. Integrated traveling wave power amplifiers with high output power have already been published in leading-edge III/V technologies, like GaAs [1]–[3], providing high substrate isolation and $f_t BV_{ceo}$ values. More than 30-dBm output power at about 20% power-added efficiency (PAE) have been reported thus far [1].

The silicon germanium (SiGe) BiCMOS technology allows implementation of high-frequency integrated mixed-signal circuits for higher level of system integration on chip. Hence, BiCMOS constitutes an alternative for implementation of low cost and highly integrated RF circuits. However, silicon suffers from large parasitic elements both in active and passive devices. The main obstacles in the design of silicon-based traveling-wave amplifiers (TWAs) are the low quality factors of on-chip spiral inductors and transmission lines, which reduce gain and efficiency [4]. Recently, several silicon-based DAs have been published in SiGe BiCMOS [4]–[6] and CMOS technology [7]–[10] mostly for low-noise and low-power applications. In [11], a 90-GHz DA in 0.12-μm silicon-on-insulator (SOI) CMOS has been presented, which exhibits 12-dBm output power and a 210-mW supply. Significant performance advantages have been published in [12] utilizing combined multigated transistors and capacitance compensation. The maximum output power at the 1-dB compression point is 15.6 dBm with an associated PAE of 20%. However, the linearization is optimized for 5 GHz and more than 14-dBm output power can only be achieved over 4–7 GHz. A DA using an integrated 16 : 1 transformer and providing 21-dBm saturated output power from 0.6 to 2.8 GHz has been presented in [13]. In [14], a DA using a cascade of inductively coupled common source gain cells has been published providing a considerably higher transconductance and low power consumption.

In this paper, we discuss the analysis, design, and implementation of an HBT power DA delivering almost constant output power over the entire frequency range of 1–12 GHz. The circuit was fabricated in 0.25-μm IHP SGB25V value technology featuring a metal stack with four aluminum metal layers. A thick top-metal layer is included for implementing inductors. The novel inductively peaked cascode configuration delivers higher gain and excellent power matching for both transistors. With 19.5-dBm output power and 11 ± 1 dB gain up to 12 GHz, the presented DA significantly improves the state-of-the-art performance of HBT wideband power amplifiers.

II. Analysis

A. Distributed Amplification

The principle of distributed amplification using discrete transistors is a technique where the input and output capacitances of the transistors are combined with lumped inductors to form

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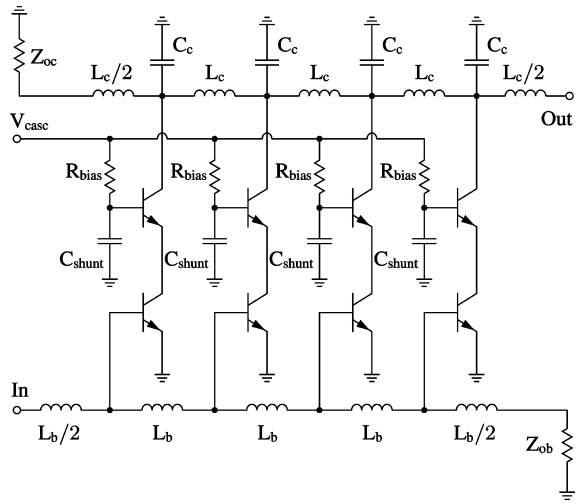

Fig. 1. Basic structure of a standard DA with four cascode stages.

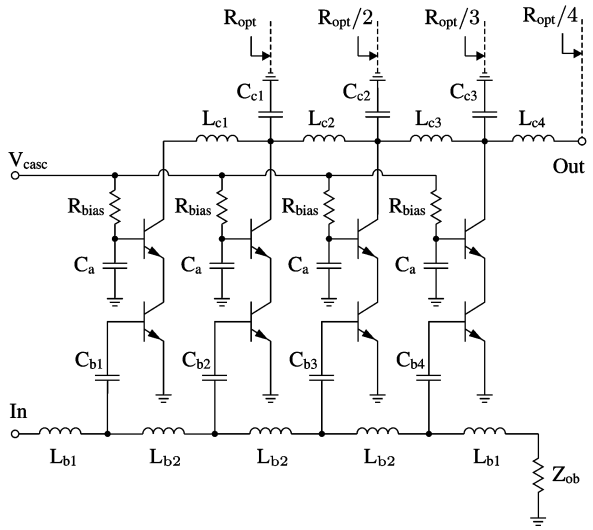

Fig. 2. Simplified schematic of a four-stage tapered DA with capacitive coupling.

artificial transmission lines. The characteristic impedance of a lossless artificial transmission line Z_o and its propagation constant β can be calculated as

$$Z_o = \sqrt{\frac{L}{C}} \tag{1}$$

$$\beta = \omega\sqrt{LC} \tag{2}$$

for $f \ll f_c$, where f_c is the 3-dB cutoff frequency of the lossless transmission line. It normally determines the bandwidth of the DA [14], given as

$$f_c = \frac{1}{\pi\sqrt{LC}}. \tag{3}$$

Fig. 1 shows the simplified schematic of a standard DA with four cascode stages [15]. Additional parallel capacitances C_c in the output line compensate the smaller $c_{\rm ce}$ values and achieve constructive RF signal addition.

The electrical lengths of the artificial transmission lines θ_{ck} and θ_{bk} will be determined by the coherent addition of the collector currents. This condition is given by

$$\theta_{bk} = \theta_{ck}, \qquad 1 \le k \le N. \tag{4}$$

However, output power, gain, and efficiency of conventional DAs are restricted by several limiting factors described in [16], such as the losses in the collector line termination resistor Z_{oc}. In Section III, methods are described to overcome these issues.

B. Power DA Design Topology

In order to achieve a high output voltage swing, a low transistor knee voltage V_k is required [17]. Since this goes along with a large emitter area in HBT transistors, the parasitic capacitances become very large. This strongly affects the resonant frequency of the DA according to (3). However, the inductor values of the base line L_b, as shown in Fig. 1, are given by their characteristic impedance Z_{ob} and the base–emitter–capacitance $c_{\rm be}$. Since $c_{\rm be}$ is larger than $c_{\rm ce}$, capacitive coupling has to be applied in order to increase the bandwidth and linearity [18]. This can be achieved by adding a capacitor C_{bi} $(1 \le i \le N)$, where N is the number of stages, as depicted in Fig. 2. The total capacitance $C_{bi}c_{\rm be}/C_{bi} + c_{\rm be}$ is a tradeoff between gain, linearity, and bandwidth since the capacitive voltage divider limits the voltage swing at the base–emitter diode.

The required inductance is calculated according to

$$L_b = \frac{Z_{ob}^2 C_{bi} c_{\rm be}}{C_{bi} + c_{\rm be}}. \tag{5}$$

The cutoff frequency of the capacitively coupled base line can be expressed by

$$f_c = \frac{1}{\pi}\sqrt{\frac{C_{bi} + c_{\rm be}}{L_b C_{bi} c_{\rm be}}}. \tag{6}$$

By varying the capacitances C_{bi}, the loss of the input line is compensated and the input drive at each gain cell is equalized [1].

Fig. 3 illustrates a general collector-line model for DAs. The parasitic capacitances and inductances are depicted as transmission lines for a clearer presentation. Assuming a uniform voltage distribution on the base line, each transistor, except the first one, can be matched to yield its optimum load [1]. Since the collector line is terminated by the dumping load conductance Y_{oc}, the admittance of the first gain cell G_1 is calculated as $G_{\rm opt} + Y_{oc}$, which results in a reduced output power of the first gain cell. For the given electrical lengths by (4), the optimum output power for an N-stage DA is

$$P_{\rm out} = \left(\frac{G_{\rm opt}}{G_{\rm opt} + Y_{oc}} + (N-1)\right) P_{\rm max} \tag{7}$$

where $P_{\rm max}$ is the maximum output power of each gain cell. The base-line attenuation determines the maximum number of sections and the output power [19]. The maximum output power can be achieved if $Z_{oc} \to \infty$, providing all power directly at the load. For this case, the total output power is

$$P_{\rm out} = N P_{\rm max} \tag{8}$$

according to (7). Therefore, each gain cell output has to see its optimum load impedance $R_{\rm opt}$ looking toward the load to yield its maximum output power.

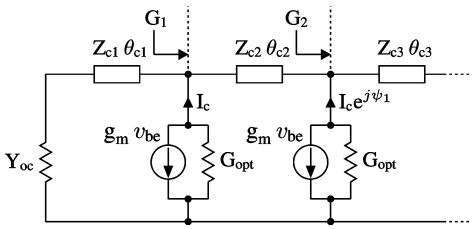

Fig. 3. Equivalent collector-line model.

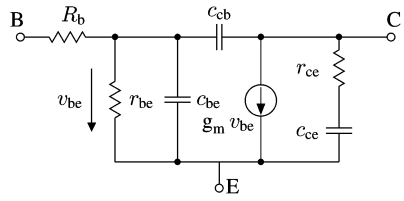

Fig. 4. SSM of 36.4-μm^2 emitter HBT at $V_{\rm ce} = 2.5$ V, $V_{\rm be} = 0.848$ V, $I_c = 20$ mA, $g_m = 525$ mS, $R_b = 2.7\ \Omega$, $r_{\rm be} = 200\ \Omega$, $r_{\rm ce} = 131\ \Omega$, $c_{\rm be} = 2$ pF, $c_{\rm cb} = 91$ fF, and $c_{\rm ce} = 28$ fF.

The equivalent load resistance of the N cell device R_L is simply the parallel combination of the optimum resistances

$$R_L = \frac{R_{\rm opt}}{N}. \tag{9}$$

The waves add together constructively when the length of the artificial collector transmission line compensates the delays of the conventional low-pass DA input circuit. Therefore, the equivalent capacitances of the gain cells are sequentially connected to an artificial collector line network, as shown in Fig. 2. The network consists of line segments with a special characteristic impedance, which changes from cell to cell and is, therefore, nonuniformly distributed. In order to achieve a coherent addition of the collector currents and a flat gain, additional shunt capacitances C_{ci} $(1 \le i \le N-1)$ are connected to the collectors of the cascode cells. Considering (2) and (3) the 3-dB cutoff frequency of the tapered collector line decreases with the number of stages as

$$f_{c,\rm taper} = \frac{1}{\pi N Z_o C_{\rm ce}}. \tag{10}$$

As a tradeoff for highest gain over the whole frequency range up to 12 GHz, four stages have been chosen. For a larger number of stages, the substrate losses degrade the RF gain rapidly at higher frequencies. The input and output impedances are $Z_o = 50\ \Omega$ so that the optimum output resistance $R_{\rm opt}$ of each of the four stages has to be 200 Ω according to Fig. 2. This value has to be considered in the load line behavior during the design procedure. The artificial transmission lines are formed by combining the capacitances of the transistors with spiral inductors to reduce chip size.

C. Device Characterization and Modeling

The DA was fabricated in 0.25-μm IHP SGB25V SiGe BiCMOS technology featuring a metal stack with four aluminum metal layers and a substrate resistivity of 20 $\Omega \cdot$ cm. Three different HBT transistors for standard, high-performance, and high-voltage purposes are available.

In Fig. 4, the small-signal model (SSM) of a 36.4-μm^2 emitter area transistor with a cutoff frequency f_t of 45 GHz is shown. Since, according to [17], the optimum load impedance for a class-A power amplifier is

$$R_{\rm opt} = \frac{V_{ceo} - V_k}{I_{\rm max}} \tag{11}$$

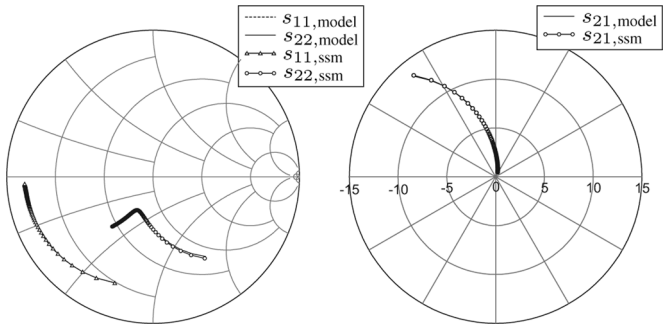

Fig. 5. Comparison between VBIC model and SSM S-parameter simulations of 36.4-μm^2 emitter HBT at $V_{\rm ce} = 2.5$ V, $V_{\rm be} = 0.848$ V, and $I_c = 20$ mA from 1 to 30 GHz.

the bias point has been set to $V_{\rm ce} = 2.5$ V and $I_c = 20$ mA for 4-V collector–emitter breakdown voltage V_{ceo} and $R_{\rm opt} = 100\ \Omega$ for each cascode transistor. The comparably large transistor size is essential to decrease the knee voltage V_k for high efficiency. The simulated S-parameters of the Vertical Bipolar Inter-Company (VBIC) model and the proposed SSM of Fig. 4 are depicted in Fig. 5. At this bias point, a f_t of 41.5 GHz and a $f_{\rm max}$ of 65.5 GHz were extracted.

In Section III, a novel cascode power-matching approach is introduced using the proposed model.

D. Novel Cascode Power Matching Approach

In order to increase the HBT distributed power amplifier performance, which is limited by the characteristic of the used active cells [3], alternative structures are investigated. The cascode cell is an appealing circuit due to its higher output impedance, higher breakdown voltage, and reduced Miller effect. Indeed, if the two transistors are loaded by the required impedance for optimum power, the maximum power should be available and the cascode output should be twice as high as compared to a single transistor. However, the conventional cascode configuration does not meet these conditions since the common base transistor's $(T_{\rm cb})$ low-input impedance restricts the output voltage excursion of the common emitter transistor $(T_{\rm ce})$. Therefore, it does not see its optimum power load impedance [1]. In addition, the power performance of the cascode cell becomes one of the most important challenges to obtain maximum output power over the required bandwidth. To be power optimized, another series capacitor C_a is added on the base of $T_{\rm cb}$ to avoid its early power saturation compared to $T_{\rm ce}$ [20]. An SSM of the modified

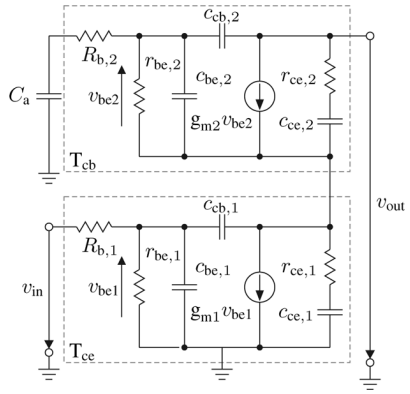

Fig. 6. SSM of the modified cascode gain cell.

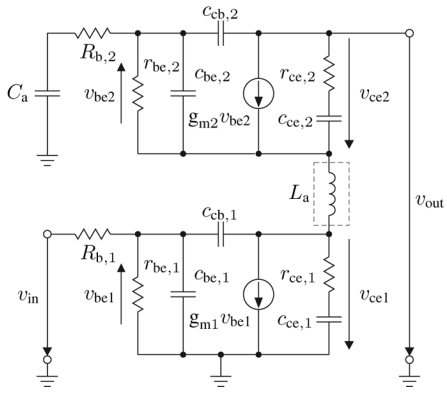

Fig. 7. SSM of the modified cascode cell with inductive peaking.

cascode gain cell is depicted in Fig. 6. The input impedance of $T_{\rm cb}$ can be calculated as

$$z_{{\rm be},i} = \frac{r_{{\rm be},i}}{1 + j\omega c_{{\rm be},i} r_{{\rm be},i}}$$
$$z_{{\rm cb},i} = \frac{1}{j\omega c_{{\rm cb},i}}$$
$$z_{{\rm ce},i} = \frac{1 + j\omega c_{{\rm ce},i} r_{{\rm ce},i}}{j\omega c_{{\rm ce},i}}$$
$$z_{\rm in,cb} = r_{\rm be,2} + R_{b,2} + \frac{1}{j\omega C_a} \tag{12}$$

for $i = 1, 2$; the output impedance of $T_{\rm ce}$ as

$$z_{\rm out,ce} = \frac{z_{\rm ce}\left(z_{\rm be,1} + z_{\rm cb,1}\right)}{z_{\rm ce,1} + z_{\rm be,1} + z_{\rm cb,1}}. \tag{13}$$

The capacitor C_a and input impedance $z_{\rm in,cb}$ act as a voltage divider between the optimum values for $v_{\rm ce1}$ and $v_{\rm be2}$. For HBT transistors with low input impedances and high input capacitances $c_{\rm be}$, this procedure strongly affects $v_{\rm be2}$ and the amplifier gain as well according to

$$v_{\rm out} \approx g_{m1}\, v_{\rm be1} \left[z_{\rm ce,1} \| \left(R_{b,2} + \frac{1}{j\omega C_a} + z_{\rm be,2} \right) \right] \times g_{m2}\, v_{\rm be2}\, z_{\rm ce,2} \tag{14}$$

with

$$v_{\rm be2} \approx \left(\frac{z_{\rm be,2}}{R_{b,2} + \frac{1}{j\omega C_a} + z_{\rm be,2}} \right) v_{\rm ce1} \tag{15}$$

whereby the impact of $c_{\rm cb}$ is neglected. Therefore, a tradeoff between high gain and output power has to be investigated [16], [21]. In order to achieve higher gain and more bandwidth, an additional inductor is added between the collector of $T_{\rm ce}$ and the emitter of $T_{\rm cb}$. The small-signal schematic of the modified cascode cell with inductive peaking is presented in Fig. 7.

The output resistance $z_{\rm out}$ of the modified cascode circuit can be written as

$$z_{\rm out} \approx z_{\rm ce,2} + \left[(j\omega L_a + z_{\rm ce,1}) \| \left(z_{\rm be,2} + R_{b,2} + \frac{1}{j\omega C_a} \right) \right] \tag{16}$$

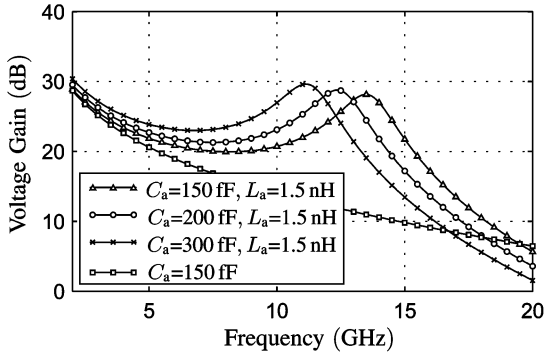

Fig. 8. Voltage gain of the cascode cell with and without additional inductor $L_a = 1.5$ nH and various capacitances C_a.

neglecting the influence of $c_{\rm cb}$. This leads to a resonance effect, which is dominated by L_a, C_a, and $c_{\rm be}$. The self-resonant frequency f_r of the *LC* low pass according to (3) can be calculated as

$$f_r = \frac{1}{\pi \sqrt{\frac{L_a\left(C_a + c_{\rm be,2}\right)}{C_a c_{\rm be,2}}}}. \tag{17}$$

The influence of a 1.5-nH inductor and various capacitances C_a on the voltage gain of the cascode cell is demonstrated in Fig. 8.

The resonant frequency shows good agreement with the theoretical considerations in (17). Another effect is that the output impedance of the cascode cell increases significantly from 2 to 15 GHz with the influence of the 1.5-nH inductor.

The initial values for L_a and C_a are then optimized under large-signal conditions using nonlinear simulations of the inductively peaked cascode circuit close to 1-dB compression point in order to obtain the maximum output power and efficiency. Thereby one single cell from Fig. 2 is used to synthesize the required ratio between the values of the inductor and capacitor. The test circuit is terminated with a 200-Ω resistor. The goal is to have equal deflections of the load lines both for the common emitter and common base transistor. Fig. 10 shows the intrinsic load lines, exemplarily at 6 GHz, of the two transistors with the optimized values $L_a = 1$ nH and $C_a = 130$ fF.

These results demonstrate that the proposed cascode configuration can obtain twice the output voltage swing compared to

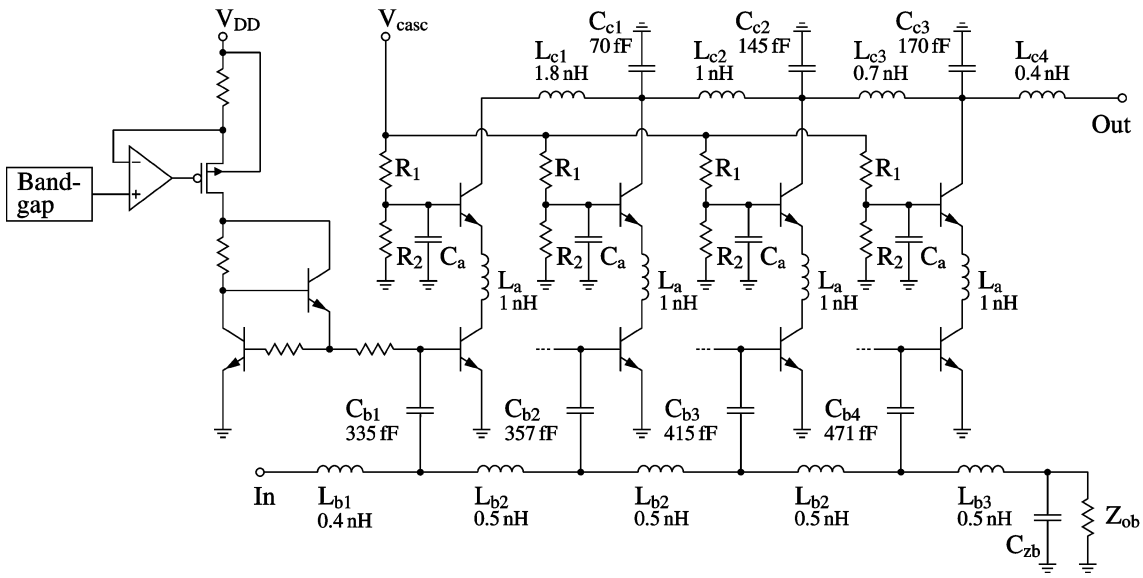

Fig. 9. Complete schematic representation of the implemented TWA structure.

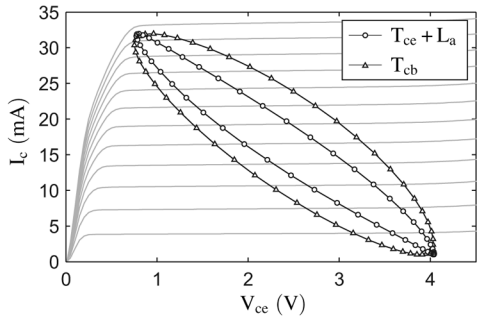

Fig. 10. Simulated intrinsic load lines of one cascode cell at 6 GHz for $L_a = 1$ nH and $C_a = 130$ fF.

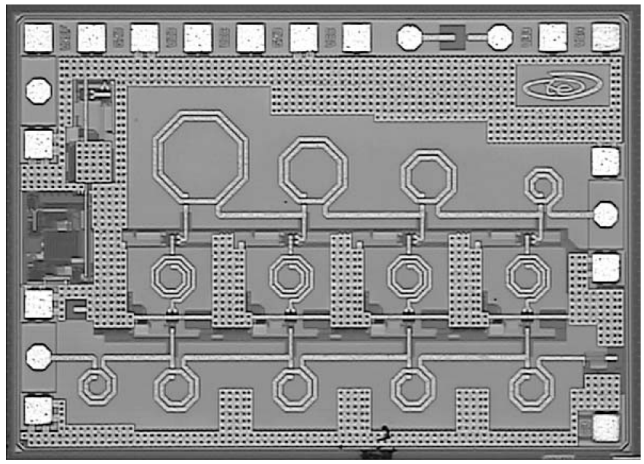

Fig. 11. Microphotograph of the fabricated 2.1 mm^2 traveling-wave power amplifier.

a single common emitter transistor at the same collector current so that twice the output power can be achieved.

III. Circuit Design and Layout

A four-stage tapered collector line TWA with capacitive coupling and power-matched cascode cells has been implemented using the methodology previously described. A simplified schematic is depicted in Fig. 9. Each gain cell consists of two 36.4-μm^2 transistors with BV_{ceo} of 4 V and a peak f_t value of 45 GHz, which are connected by a 1-nH inductor L_a, which exhibits a Q factor of 20 at 12 GHz. Staggered inductors $L_{c1} > L_{c2} > L_{c3} > L_{c4}$ together with shunt capacitances $C_{ci} \,||\, c_{\rm ce}$ $(1 \leq i \leq 3)$ form the tapered collector line to achieve a coherent addition of the currents and a flat gain over the entire bandwidth.

Biasing is implemented using current mirrors with a ratio of 32 : 1 and a low dropout (LDO) voltage reference driven by the bandgap voltage source. A chip microphotograph of the implemented circuit is shown in Fig. 11. The transistors are biased through the collector line by means of an external bias-tee. The bias point was selected at $V_{CC} = 5$ V and $V_{DD} = 2.6$ V. A power and ground grid facilitates a low-impedance connection and due to the low distance between the congruent metal grids a large capacitor is shaped. The chip size of the amplifier circuit is 2.1 mm^2.

IV. Measurement Results

The distributed power amplifier chip was tested via on-wafer probing. The measurements of the circuit were carried out using an Agilent N5242A PNA-X vector network analyzer. Fig. 12 shows the simulated and measured small-signal gain S_{21} and input return loss S_{11}.

The TWA exhibits a measured gain of 11 dB with a gain ripple of ± 1 dB up to 12 GHz and a 3-dB bandwidth of 13 GHz. Simulated and measured output return loss S_{22} and reverse isolation S_{12} are illustrated in Fig. 13. Both the input and output return losses are below -12 dB over the entire frequency range. The measured reverse isolation S_{12} remains below -35 dB. The circuit is unconditionally stable, also verified for large RF input signals.

TABLE I
STATE-OF-THE-ART OF UWB PA PERFORMANCE. AT 2-10-GHz FREQUENCY RANGE

Ref.	Technology	Bandwidth	Gain	P_{1dB}	P_{dc}	PAE	Chip size
[7]	0.13 μm CMOS	2–8 GHz	17 dB	3.5 dBm	84 mW	2.36 %	-
[8]	0.18 μm CMOS	3–10 GHz	10 dB	5.6–9.4 dBm	100 mW	3.0–7.8 %	1.76 mm^2
[10]	0.18 μm SiGe BiCMOS	0.1–11 GHz	8 dB	-6.1– -5.2 dBm	21.6 mW	1–1.2 %	0.76 mm^2
[11]	0.12 μm SOI CMOS	1–90 GHz	11 dB	12 dBm	210 mW	6.95 %	1.28 mm^2
[12]	0.18 μm CMOS	3.7–8.8 GHz	8.24 dB	12–15.6 dBm	154 mW	8.7–20 %	2.8 mm^2
[13]	0.13 μm CMOS	0.6–2.8 GHz	20 dB	14–17 dBm	-	3–6.5 %	3.6 mm^2
[14]	0.18 μm CMOS	0–11 GHz	11/16 dB	-	19.6/100 mW	-	1.44 mm^2
[16]	0.25 μm SiGe BiCMOS	2–12 GHz	9.5 dB	13–14.3 dBm	250 mW	7.71–9.6 %	1.16 mm^2
This Work	0.25 μm SiGe BiCMOS	1–12 GHz	12 dB	16.2–19.5 dBm[1]	400 mW	10.3–22.1 %[1]	2.1 mm^2

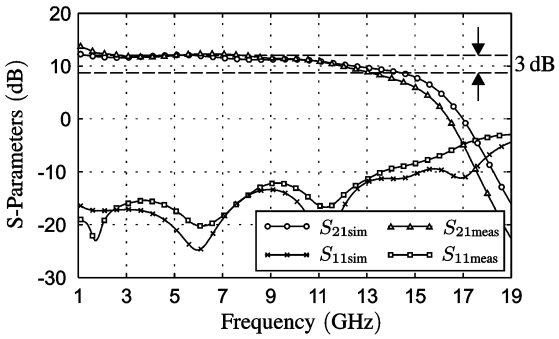

Fig. 12. Simulated and measured small-signal gain S_{21} and input return loss S_{11}.

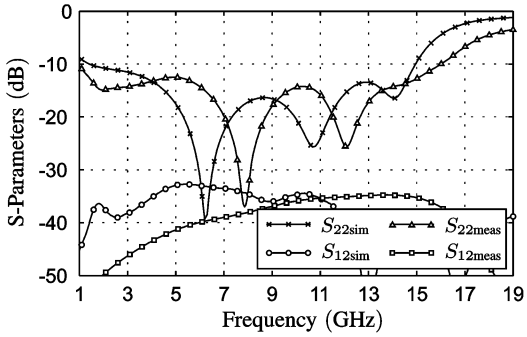

Fig. 13. Simulated and measured output return loss S_{22} and isolation S_{12}.

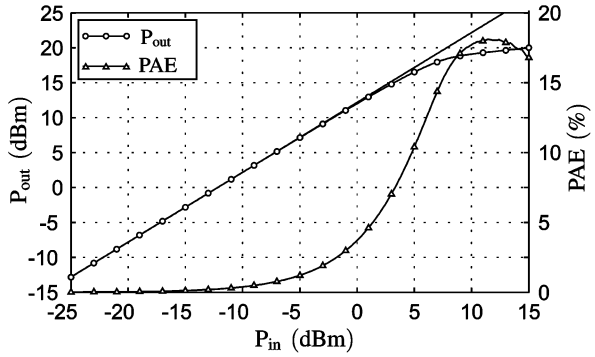

Fig. 14. Output power $P_{\rm out}$ and PAE at center frequency 7 GHz.

Fig. 14 shows the output power and PAE at the center frequency of 7 GHz. The 1-dB compression point is at 17.45 dBm with an associated PAE of 13.9%. The saturated output power

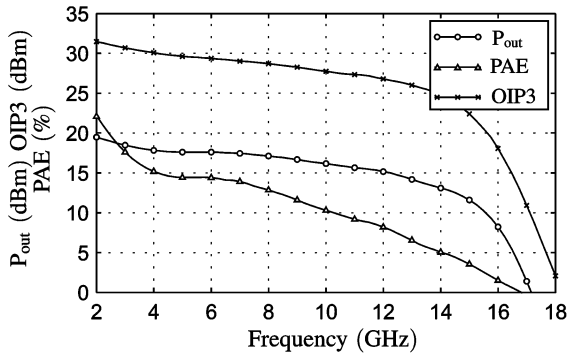

Fig. 15. Output power $P_{\rm out}$, PAE, and OIP3 measured at 1-dB compression point.

is 20 dBm and the maximum PAE is 22.1%. Output power at 1-dB compression point, corresponding PAE, and the output third-order intercept point (OIP3) are depicted in Fig. 15.

The output power at $P_{1\ \rm dB}$ varies from 16.2 to 19.5 dBm between 2–10 GHz with a PAE ranging from 10.3% up to 22.1%. An almost flat characteristic has been obtained over the entire bandwidth. The third-order intermodulation intercept point is better than 26.8 dBm up to 12 GHz and 31.5 dBm at its maximum.

The accomplished performance is compared with the state-of-the-art in Table I. The DA in [12], which is implemented in 0.18-μm CMOS, comes closest for comparison. Its maximum output power at a 1-dB compression point is 15.6 dBm with an associated PAE of 20% and 8.24-dB gain. The novel cascode power matching approach with an additional inductor shows significant improvement compared to [16] with 14-dBm output power and 9.5-dB gain.

This tapered DA achieves a maximum output power at $P_{1\ \rm dB}$ of 19.5 dBm and 11-dB gain with a flatness of ± 1 dB. To the authors' knowledge, the broadband performance is the best that has been published for SiGe BiCMOS thus far.

V. CONCLUSION

A tapered collector line traveling-wave power amplifier with a new cascode power matching approach has been implemented using a low-cost 0.25-μm SiGe BiCMOS technology. The optimum tradeoff between wide frequency range, high gain, and output power has been investigated and a demonstrator chip was designed. An efficient design procedure has been developed

considering the power distribution between the amplifier stages and their load line behavior. The SiGe DA was manufactured at the IHP, and, to the authors' knowledge, exhibits the best broadband performance ever reported for SiGe BiCMOS DAs in that frequency range.

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REFERENCES

[1] B. Campovecchio, B. L. Bras, M. Lajugie, and J. Obregon, "Optimum design of distributed power-FET amplifiers. Application to a 2–18 GHz MMIC module exhibiting improved power performances," in *IEEE Microw. Millimeter-Wave Monolithic Circuits Symp. Dig.*, May 1994, pp. 125–128.

[2] C. Duperrier, M. Campovecchio, L. Roussel, M. Lajugie, and R. Quere, "New design method of uniform and nonuniform distributed power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 12, pp. 2494–2500, Dec. 2001.

[3] J. P. Fraysse, J. P. Viaud, M. Campovecchio, P. Auxemery, and R. Quéré, "A 2 W, high efficiency, 2–8 GHz, Cascode HBT MMIC power distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2000, vol. 1, pp. 529–532.

[4] G. A. Lee, K. Hyunseok, and F. D. Flaviis, "Advanced design of broadband distributed amplifier using a SiGe BiCMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, vol. 1, pp. 189–192.

[5] M.-D. Tsai, K.-Y. Lin, and H. Wang, "A 5.4-mW LNA using 0.35 μm SiGe BiCMOS technology for 3.1–10.6 GHz UWB wireless receivers," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2005, pp. 335–338.

[6] D. Guckenberger and K. T. Kornegay, "Design of a differential distributed amplifier and oscillator using close-packed interleaved transmission lines," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 1997–2007, Oct. 2005.

[7] C. Grewing, K. Winterberg, S. van Waasen, M. Friedrich, G. L. Puma, A. Wiesbauer, and C. Sandner, "Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitters," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2004, pp. 87–90.

[8] C. Lu, A.-V. Pham, and M. Shaw, "A CMOS power amplifier for full-band UWB transmitters," in *IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2006, pp. 4–7.

[9] S. Jose, H.-J. Lee, and D. Ha, "A low-power CMOS power amplifier for ultra wideband (UWB) applications," in *IEEE Int. Circuits Syst. Symp.*, May 2005, vol. 5, pp. 5111–5114.

[10] P. Heydari, "Design and analysis of a performance-optimized CMOS UWB distributed LNA," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1892–1905, Sep. 2007.

[11] K. Jonghae, J.-O. Plouchart, N. Zamdmer, R. Trzcenski, R. Groves, M. Sherony, Y. Tan, M. Talbi, J. Safran, and L. Wagner, "A 12 dBm 320 GHz GBW distributed amplifier in a 0.12 μm SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2004, vol. 1, pp. 478–540.

[12] C. Lu, A.-V. Pham, M. Shaw, and C. Saint, "Linearization of CMOS broadband power amplifiers through combined multigated transistors and capacitance compensation," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 11, pp. 2320–2328, Nov. 2007.

[13] J. Roderick and H. Hashemi, "A 0.13 μm CMOS power amplifier with ultra-wide instantaneous bandwidth for imaging applications," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2009, vol. 1, pp. 374–376.

[14] X. Guan and C. Nguyen, "Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3278–3283, Aug. 2006.

[15] T. Wong, *Fundamentals of Distributed Amplification*, 1st ed. Norwood, MA: Artech House, 1993.

[16] B. Sewiolo and R. Weigel, "A novel 2–12 GHz 14 dBm high efficiency power distributed amplifier for ultra-wideband-applications using a low-cost SiGe BiCMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2008, pp. 1123–1126.

[17] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 1999.

[18] Y. Ayasli, S. W. Miller, R. Mozzi, and L. K. Hanes, "Capacitively coupled traveling-wave power amplifier," *IEEE Trans. Electron Devices*, vol. 31, no. 12, pp. 1937–1942, Dec. 1984.

[19] Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds, and R. A. Pucel, "A monolithic GaAs 1–13-GHz traveling-wave amplifier," *IEEE Trans. Electron Devices*, vol. ED-29, no. 7, pp. 1072–1077, Jul. 1982.

[20] A. Martin, T. Reveyrand, M. Campovecchio, R. Aubry, S. Piotrowicz, D. Floriot, and R. Quere, "Balanced AlGaN/GaN HEMT cascode cells: Design method for wideband distributed amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 44, no. 1, pp. 116–117, Jan. 2008.

[21] B. Sewiolo and R. Weigel, "A 2–12 GHz power distributed amplifier for broadband localization- and sensor systems based on PN-sequences," in *IEEE Int. Ultra-Wideband Conf.*, Sep. 2008, vol. 3, pp. 77–80.

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