31.6 An Outphasing Power Amplifier for a Software-Defined Radio Transmitter

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A software-defined radio (SDR) transmitter needs a universal modulator and power amplifier to support any modulation in any band. There is a simple solution, namely, a Cartesian I-Q upconverter followed by a linear power amplifier, but for complex modulations its power conversion efficiency is often under 10%. Therefore, the search continues for a more efficient solution. One possibility is to harness the high efficiency of a saturated power amplifier but somehow make it deliver amplitude-modulated waveforms. Polar modulation has found use in enabling EDGE on GSM handsets, but we believe outphasing [1], or linear amplification using nonlinear components (LINC), offers a more enduring solution for a broader class of modulations.

We present an SDR PA based on the outphasing technique. An arbitrary signal, shown in Fig. 31.6.1 as phasor $s(t)$, is decomposed into two constant amplitude phasors with amplitudes of $\max(|s(t)|)/2$. The outphasing angle ϕ determines the instantaneous amplitude. The constant amplitude phase-modulated vectors are applied to two identical, saturated PAs, whose *output powers* sum together to reconstruct the intended modulation.

Amplitude and phase mismatch in the two paths can cause distortion, but it is easier to match two nominally identical signal paths than to align two heterogenous paths as in polar modulation. The main challenge here is how to combine two PA outputs at constant envelopes without loss.

The two outputs of the PAs cannot merely be shorted, otherwise each will experience a variable power envelope at its output which degrades efficiency. Instead, each PA must produce constant power isolated from the other, but the sum of the power waveforms should produce an arbitrary modulation. A hybrid transformer is most often used, but its dummy load dissipates half the useful power, degrading efficiency.

Our main contribution is to devise a DSP-assisted method of lossless power combining. This is demonstrated in a 90nm CMOS prototype chip that reconstructs GMSK, EDGE, and WCDMA and shows the feasibility of the concept at output levels of about +20dBm peak; we do not address here the other needs of a practical transmitter, such as large dynamic range of power control, and high output power levels closer to +30dBm.

PA outputs can be combined with lossless components such as a wideband balun transformer or a narrowband LC combiner; however, the two PAs are no longer isolated and they would interact. As shown in Fig. 31.6.2, each PA load is a complex impedance, with a series reactance that depends on outphasing angle. This causes distortion in Class-B saturated PAs.

Adding reactive components in parallel to each PA output can eliminate the imaginary part of the apparent load. This reactive compensation is a function of carrier frequency, outphasing angle, and R_L (Fig. 31.6.3). A capacitance depending on ϕ can be added in parallel to one side, and subtracted from the other. This leaves a purely resistive apparent impedance, which after narrowband parallel-to-series transformation, would depend on ϕ, as $R_{app}=R_L\cos^2\phi$. To compensate for this dependence, the currents in the core PA transistors are scaled with ϕ to maintain the PA output voltage amplitude constant. It is found that this time-varying nonlinear system is externally linear.

Figure 31.6.4 shows one slice at the PA output. The FET is a 2.5V thick-oxide device that can sustain the large output swing (biased below threshold). It is driven by a gated digital signal. Note that the 90nm CMOS logic can toggle up to 5GHz. However, depending on the rise and fall times of the drive waveform, its efficiency can vary from 64% to 78%. The duty cycle of the driving signal can change its operation from Class C to AB. The bias voltage on S1 and S2 sets this duty cycle. The digital supply, nominally 1.2V, sets the drive amplitude. The transistors are partitioned into 255 independently switchable cells. An 8b binary-weighted bank of capacitors compensates for the varying reactance. Transistors and capacitors are controlled by a thermometer code and are laid out as 255 intermeshed cells for good matching and monotonic switching. The number of bits is determined by simulations for EDGE, WCDMA, and GSM masks. Bond wires are used as inductors in the tank. Circuit and electromagnetic simulations show that for every 8.3mW of output power, one ground bondwire of less than 1mm length is needed in the PA core, otherwise the efficiency degrades. In addition, a 6b capacitor array tunes the load to the desired band of operation.

To prove the concept for different standards, the core PA is designed for +20dBm maximum power. For lower/higher power the same PA core can be downsized/replicated. The peak efficiency of the PA is 56%. The actual efficiency depends on the probability density function (PDF) of the modulation. Efficiency decreases at small output amplitude, when some power is still dissipated in the transistors and the tank.

The chip is fabricated in a 90nm CMOS process. A high-speed on-chip digital engine generates the control words that switch FETs and capacitors. A PC pre-calculates the switching scheme, and sends the results to an FPGA which generates data at 68MHz for different on-chip blocks. The data rate should be high enough to ensure fast updates for on-chip registers. To ameliorate the 68MHz spurs at the output, the ON/OFF command applied to the capacitor cells has relatively slow rise and fall times, thus avoiding leakage of spikes directly into the tank. Although we measure acceptably small levels for those spurs (–60dBc), if required a higher clocking frequency can be used. A better option is an event-driven switching scheme where the cells switch on or off once certain thresholds are reached, as opposed to the current clock-driven switching. The data is externally fed through a high-speed interface to the chip by the FPGA.

The system is tested for three standards: GSM, EDGE and WCDMA. Due to the wire-bond inductace, the useful RF output stays below 1.4GHz. With flip-chip technology we believe that 3 to 5GHz operation would be possible. For GMSK, the power-conversion efficiency is 56% at +16dBm. In EDGE mode, efficiency falls to 44% at +14dBm rms output. This efficiency is higher than prior art in CMOS [3]. To achieve the stringent noise requirements at 20MHz offset, S1 and S2 data are filtered at baseband prior to upconversion. For WCDMA, efficiency declines to 30% at +13dBm rms output. Mismatches are manually calibrated by changing the supply levels for the two chains, and a small residual AM/PM conversion in the PAs is measured and worked into the input data. The PA meets all specifications on mask and EVM as summarized in Fig. 31.6.6.

References:

[1] H. Chireix, "High Power Outphasing Modulation," *Proc. IRE*, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.
[2] D. M. Pozar, *Microwave Engineering*, Addison-Wesley, 1990.
[3] T. Sowlati, D. Rozenblit, E. MacCarthy et al, "Quad-Band GSM/GPRS/EDGE Polar Loop Transmitter", *ISSCC Dig. Tech. Papers*, pp. 186-187, Feb. 2004.

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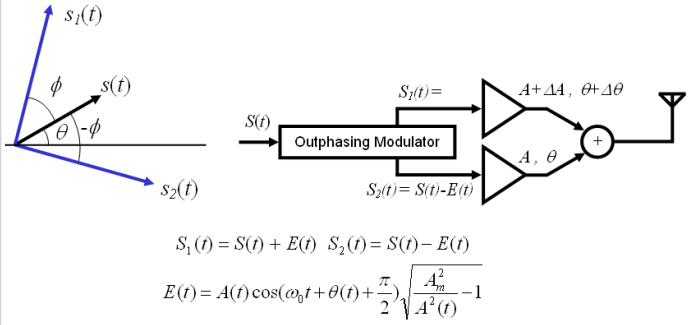


Figure 31.6.1: The outphasing principle.

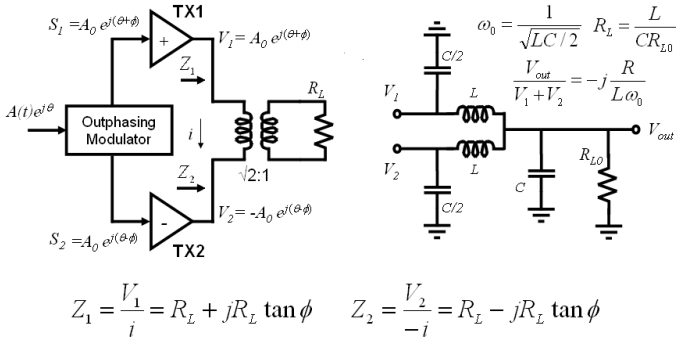


Figure 31.6.2: Passive combiner and problem of variable apparent load.

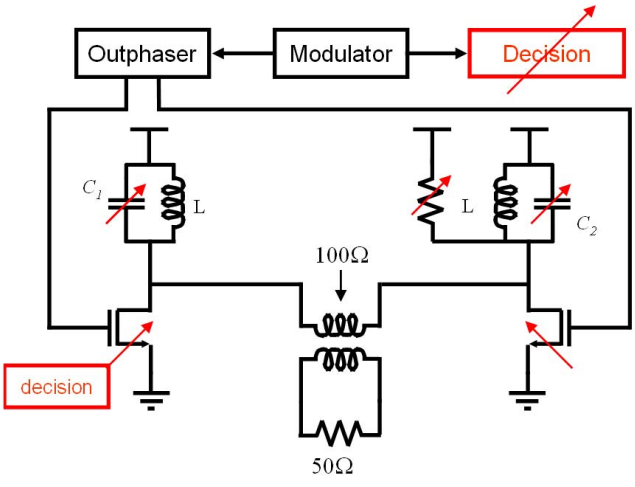


Figure 31.6.3: An outphasing system with proper compensation.

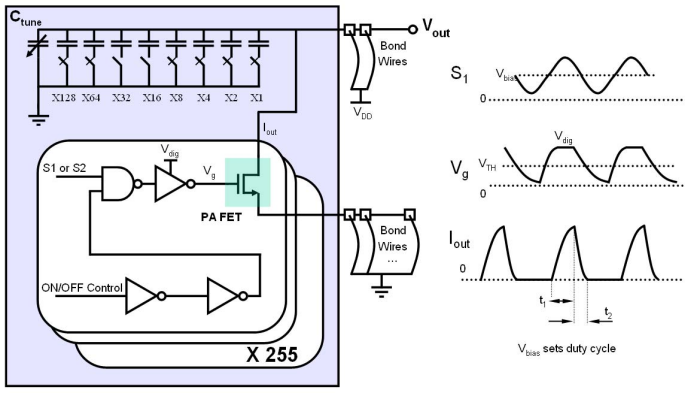


Figure 31.6.4: Details of transistor and capacitor banks.

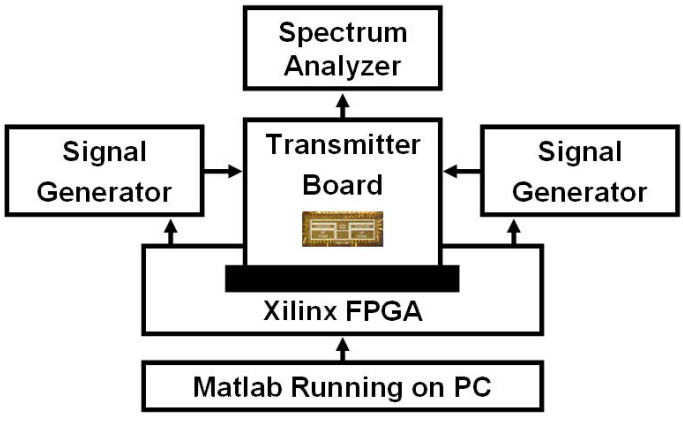
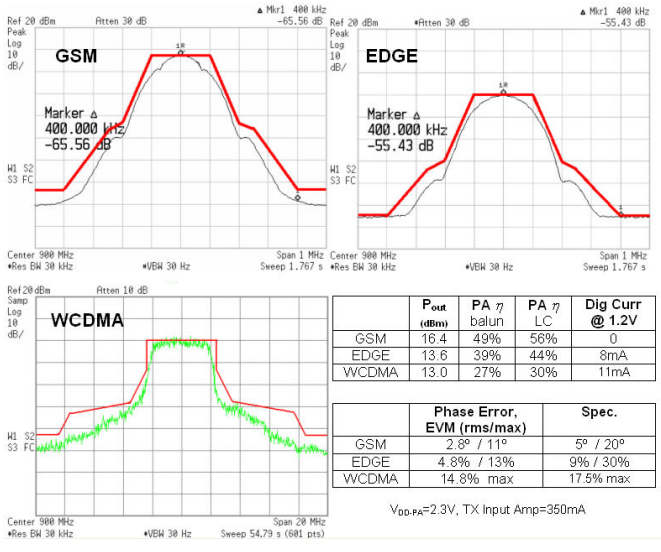


Figure 31.6.5: Generation of outphasing signals.



	P_{out} (dBm)	PA η balun	PA η LC	Dig Curr @ 1.2V
GSM	16.4	49%	56%	0
EDGE	13.6	39%	44%	8mA
WCDMA	13.0	27%	30%	11mA

	Phase Error, EVM (rms/max)	Spec.
GSM	2.8° / 11°	5° / 20°
EDGE	4.8% / 13%	9% / 30%
WCDMA	14.8% max	17.5% max

$V_{DD\text{-}PA}$=2.3V, TX Input Amp=350mA

Figure 31.6.6: Test results.

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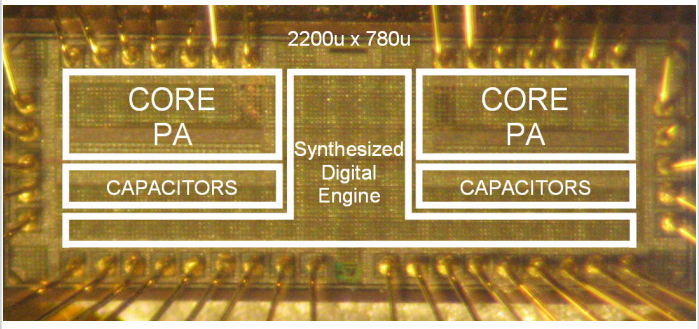

Figure 31.6.7: Chip micrograph.

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