A 0.1-1.2 GHz CMOS Ultra-Broadband Power Amplifier

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Abstract —A 0.1-1.2 GHz power amplifier using 0.18-μm CMOS technology is presented with a small chip area. With 3.3V supply, the measurement results in this band indicated that the gain is better than 20 dB, the S11 and S22 is less than - 18 dB and -10 dB, respectively. The saturated output power is 20.5 dBm and 19.5 dBm at 433 MHz and 900 MHz with the corresponding PAE of 27% and 19.5%, respectively. The chip area is only 0.414 mm^2.

Index Terms—Cascode, CMOS PA, resistive feedback, ultra-broadband.

I. INTRODUCTION

The radio frequency (RF) power amplifiers (PAs) play critical roles in various system applications, such as for the wireless/mobile communication, radar, satellite systems, etc [1]-[3]. Pushed by the low-cost requirements of consumers, the CMOS technology has become a desirable choice for the PA design due to its benefits of high-level integration and low cost implementation [4].

In recent years, the wireless communication has generated a strong demand for a mobile device with wideband, multi-standard and low-cost [3]-[7]. It has a long history to use the frequency range of 0.1-1.2 GHz, such as mobile communication [7], spacecraft [8], and parts of Industrial Scientific and Medical (ISM) [9], [10]. However, most of the reported PAs were designed with narrow bandwidth or only in one or a few frequency bands to meet only one or some particular applications [2], [8]-[10]. It is desired to develop a wideband RF PA to cover all those applications.

Recently, there have been some attempts to enlarge the operating bandwidth based on CMOS technologies. A distributed amplifiers show substantially wideband matching and small-signal gains, but occupying large chip area and having a low power-added efficiency (PAE) typically less than 15% [11]; the stacked structure can compromise the gain and flatness for a broad frequency range, but with complicated topology and high supply voltage requirement [12]; the RLC matching and transformer structure also suffers from the problem of large areas, and it also introduces losses which will degrade the efficiency[4]. Besides those methods, the resistive feedback has been demonstrated to be beneficial for gain flatness and multi-octave bandwidth performance, and usually occupies smaller chip area [5].

In this paper, a 0.1-1.2 GHz single-ended CMOS PA using 0.18μm CMOS technology with a small chip size is proposed and validated successfully by employing the resistive feedback. The good gain flatness and output matching are obtained without using any extra input matching networks which have been adopted commonly in the literature [4] so that the chip area can be reduced. Together with stability consideration, the input matching is finally well realized by the biased circuit of the first stage.

This proposed ultra-broadband CMOS PA has a three-stage configuration with cascode, common source (CS) and resistive feedback techniques. The first stage which employs a cascode structure is used to provide a high gain, good input matching and reverse isolation; the second stage is used for gain improvement and inter-stage matching; the flatness and high output power are achieved by a CS topology with resistive feedback technique at the last stage. The measured results indicate that the small signal gain is better than 20 dB, the input and output return loss is less than -18 dB and -10 dB, respectively. The output 1dB compression point is 19.1 and 17.1 dBm at 433 MHz and 900 MHz with the corresponding PAE of 27% and 19.5%, respectively.

II. ULTRA-BROADBAND PA CIRCUIT DESIGN

A detailed schematic of this proposed three-stage CMOS PA is shown in Fig. 1. The input and output DC blocking capacitors C1 and C4 and all the RF-choke inductors (L0~L2) are off-chip. This PA employs a conventional cascode topology at the first two stages and a CS structure with a resistive shunt feedback at the last stage. The on-chip DC blocking capacitors C2 and C3 at the inter-stage are set to 20 pF to extend the bandwidth down to 100MHz.

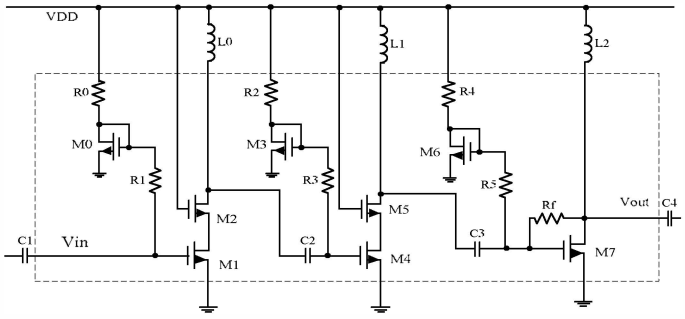

Fig. 1. A detailed schematic diagram of the proposed CMOS PA.

The first stage is a driver stage with a cascode structure for high gain and good input matching. This topology consists of two transistors M1 and M2. Transistor M2 is stacked on M1,

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providing a good isolation because of its high output impedance. Inductor L0 is chosen large enough to feed DC power to the drain as an RF choke.

Transistor M1 is biased by a current mirror topology formed by two resistors R0 and R1 together with transistor M0. The biased voltage can be calculated as:

$$V_{GS} = \frac{2V_{DD} + g_{m0}V_{TH}R_0}{2 + g_{m0}R_0} \quad (1)$$

where M0 is always biased in the saturated region and its transconductance is:

$$g_{m0} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \quad (2)$$

In Fig. 1, the total input impedance Z_{in} of this PA could be given as bellows:

$$Z_{in} = \left(R_0 \parallel \frac{1}{g_{m0} + j\,\omega C_{gs0}} + R_1\right) \parallel \frac{1}{j\,\omega C_{gs1}} \quad (3)$$

where the gate-source overlap capacitor C_{gs1} = 214fF, so the input impedance at 1 GHz can be simplified as below:

$$Z_{in} \approx R_0 \parallel \frac{1}{g_{m0} + j\,\omega C_{gs0}} + R_1 \quad (4)$$

When the values of g_{m0} and C_{gs0} are given, by selecting the values of *R0* and *R1* with the consideration of the stability, Z_{in} in (4) can be easily tuned to 50Ω.

The topology of the second stage is the same as the first one, coupled with the bias circuit. The implementation of this stage is for the gain improvement.

As the common source configuration has large voltage swings, the third stage employs a CS stage with the same biased circuit as the first two stages for a high output power and the gain improvement. The resistive shunt feedback is utilized to improve its gain flatness and broadband output matching without adopting any output matching circuits. The broadband output matching is achieved by *Rf* equals 840 Ω.

The simplified output impedance Z_{out} can be given by [13]:

$$Z_{out} = \left[\frac{1}{g_{m7}}\left(1 + \frac{R_f}{R_S}\right)\right] \parallel \left(R_f + R_S\right) \quad (5)$$

where g_{m7} is the transconductance of M7, and R_S is the input impedance of M7 which can be calculated as (6) :

$$R_S = R_4 \parallel \frac{1}{g_{m6} + j\,\omega C_{gs6}} + R_5 \quad (6)$$

Thus, the output impedance can be optimized to 50Ω by selecting the values of *Rf*, *R4* and *R5*.

III. Experimental Results

This ultra-broadband PA has been fabricated in 0.18-μm CMOS process technology with bond pads. Fig.2 shows the chip microphotograph of the PA. The chip size with pads is 0.74 mm × 0.56 mm, and no on-chip inductor was used in this layout. The off-chip DC blocking capacitors and RF choke inductors are replaced by Mini Circuit's DC block components and bias-tees in this test, which are not shown in this photograph. The chip with a 3.3 V supply voltage was tested on-wafer on the Cascade Microtech's probe station with two GSG RF probes, using the Rohde & Schwarz (R & S) vector network analyzer (VNA).

The measured small signal S-parameters are shown in Fig. 3. It can be seen that this ultra-broadband PA has a gain of approximately 22.5 ± 2.5 dB over the frequency range from 0.1GHz to 1.2 GHz. The input return loss S11 is less than -18 dB and the output return loss S22 is less than -10 dB, respectively. It also achieved an excellent reverse isolation of less than -40 dB over the whole frequency range. In Fig. 3 the stability factor (K-factor) is much larger than 1 which means this PA is stable in the interested frequencies range.

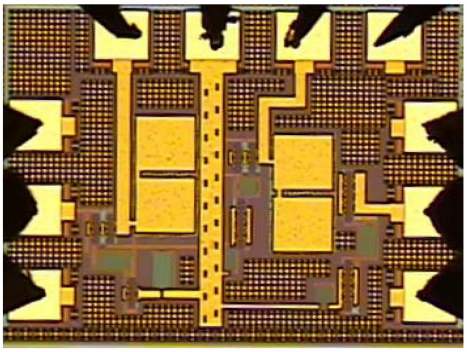

Fig. 2. Chip microphotograph of the CMOS PA.

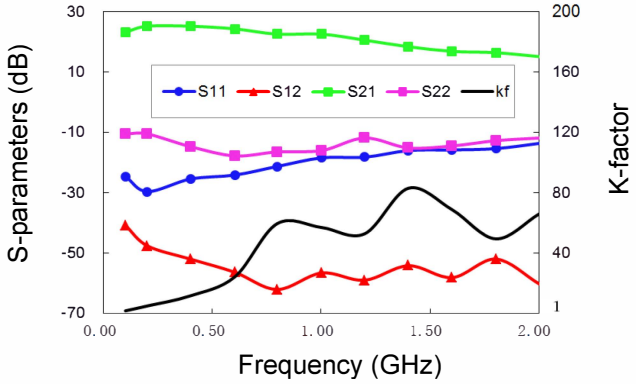

Fig. 3. Measured S-parameters and K-factor.

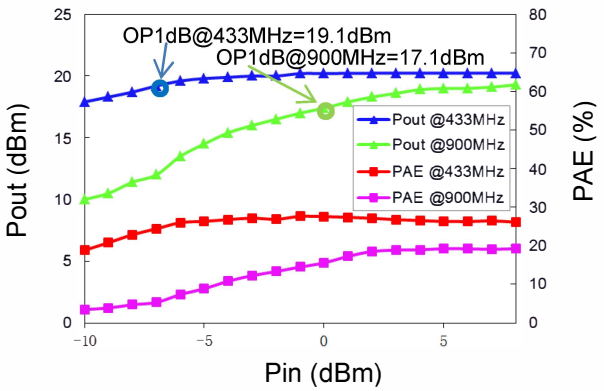

Fig. 4. Measured output P1dB and PAE at 433MHz and 900MHz.

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The measured 1-dB compression points are depicted in Fig.4. At 433 MHz and 900 MHz, the IP1dB for this PA is –8 dBm and 1 dBm and the OP1dB is 19.1 dBm and 17.1 dBm, respectively. The saturation output power is 20.5 dBm at 433 MHz and 19.5 dBm at 900 MHz, respectively. Fig. 4 shows that the calculated PAE is 27% and 19.3% at OP1dB of 433 MHz and 900 MHz, respectively. Fig.5 shows the PA's measured third-order intermodulation distortion (IMD3) results. A two-tone test was performed at a center frequency of 900 MHz and 433 MHz with tone-spacing of 1 MHz.

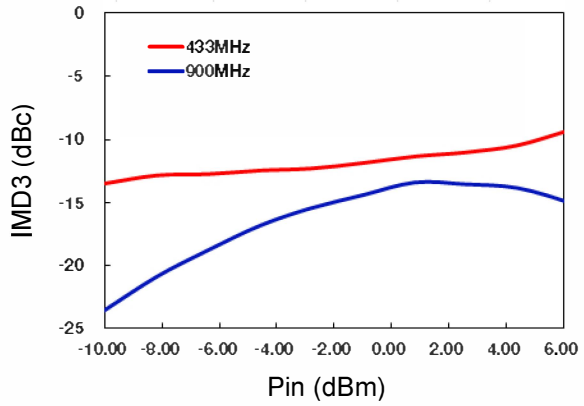

Fig. 5. Measured IMD3 at 433MHz and 900MHz.

A measurement summary and comparison with other reported broadband PAs are shown in Table 1. Compared with other reported works, this proposed PA exhibits high gain, excellent bandwidth, large output power, and small area. It is a good candidate for ultra-broadband system application.

TABLE I
COMPARISON WITH PUBLISHED BROADBAND PA PERFORMANCES

References	**This work**	**[5]**	**[6]**	**[11]**	**[14]**
Freq(GHz)	0.1–1.2	2.6–5	5.2–13	1–5	2–12
Gain(dB)	22.5±2.5	10.3±0.8	18.5	15–20	9±0.5
S11(dB)	<–18	<–5	<–10	<–5	<–15
S22(dB)	<–10	<–8	<–5	<–6	<–10
OP1dB(dBm)	19.1@433MHz 17.1@900MHz	8.0	22.6	18–20	14
PAE(%)	27@433MHz 19.5@900MHz	40.5	21.6	18–36	9
Size(mm^2)	0.414	0.969	0.698	0.684	1.16

IV. CONCLUSION

A high gain, 0.1 GHz to 1.2 GHz three-stage ultra-broadband PA in 0.18-µm CMOS process has been reported in this paper. By using the cascode, common source structure and resistive feedback topologies, this PA has a gain of over 20 dB from 0.1 to 1.2 GHz. At 433 MHz and 900 MHz, the PA demonstrates the saturation output power of 20.5 dBm and 19.5 dBm, output 1dB compression point of 19.1 and 17.1 dBm, and PAE of 27% and 19.5%, respectively. The chip occupies a small area of 0.74 mm × 0.56 mm with PADs. This proposed CMOS RF PA is suitable for the VHF/UHF broadband applications with a small chip size.

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