A SiGe PA with Dual Dynamic Bias Control and Memoryless Digital Predistortion for WCDMA Handset Applications

Junxiong Deng, Prasad Gudem, Lawrence E. Larson, Don Kimball and Peter M. Asbeck

Center for Wireless Communications, Dept of ECE, UCSD, La Jolla, CA 92093

Abstract — **This paper demonstrates a two-stage 1.95GHz WCDMA handset RFIC power amplifier (PA) implemented in 1.8mm^2 in a 250nm SiGe BiCMOS process. With an integrated dual dynamic bias control of the collector current *and* the collector voltage in the output stage, the average power efficiency of the two-stage PA is improved by over a factor of two. An off-chip memoryless digital predistortion is also adopted to improve the linearity of the power amplifier, satisfying the 3GPP WCDMA Adjacent Channel Power Ratio (ACPR) specifications with 26dBm average channel output power and a peak power-added efficiency of 27%.**

Index Terms — **Silicon Germanium, power amplifiers, WCDMA, average power efficiency, dynamic bias control, memoryless systems.**

I. Introduction

Silicon Germanium (SiGe) is an attractive candidate for the development of handset power amplifiers (PAs), because of its competitive performance in efficiency, linearity, cost and integration with BiCMOS technology [1]. In wireless communications systems, PAs are key components that consume a significant portion of the dc power budget in the transmitter. For third-generation cellular systems, like Wideband Code Division Multiple Access (WCDMA), more stringent linearity is required in terms of Adjacent Channel Power Ratio (ACPR) for higher spectral efficiency. Therefore, linearity and efficiency are the most critical parameters in WCDMA PA design. The design specifications for WCDMA PAs are listed in Table I.

Average power efficiency is the key factor determining the talk time and battery life for portable wireless applications [3]. To improve the average power efficiency of PAs, different dynamic biasing techniques [4]-[5] have been developed. Altering the dc *current* in response to changing power requirements – also known as Dynamic Current Biasing (DCB) – often results in significant amplifier gain variation. Adjusting the dc *voltage* according to the signal power level – also known as Dynamic Voltage Biasing (DVB) – typically requires the use of DC-DC converters with their associated large off-chip components and extra chip area and cost.

A dual dynamic bias (DDB) control scheme that does not require any additional off-chip components and maintains nearly constant gain is proposed in this paper to improve the average power efficiency. In addition, an off-chip memoryless digital predistortion (DP) [6] based on the measured AM-AM and AM-PM characteristics is employed to substantially improve the linearity of the PA. The resulting performance meets the WCDMA linearity specifications at significantly improved efficiency.

TABLE I
3GPP WCDMA Handset Power Amplifier Specifications [2]

Specification	Value
Operating Frequency	1.92 GHz – 1.98 GHz
Maximum Output Power	23 dBm – 35 dBm
Power Gain[1]	15 dB – 27 dB
PAE @ Maximum Output Power	~ 30%
ACPR (3.84 MHz main channel)	–33 dBc @ 5 MHz offset –43 dBc @ 10 MHz offset

[1]Reported maximum output power of the WCDMA TxIC driver stage is in the range between 6 dBm and 10 dBm. The average 8 dBm is used here.

In Section II, details of dual dynamic bias control are introduced. In Section III, the memoryless digital predistortion is presented. Measurement results are shown in Section IV and conclusions are given in Section V.

II. Dual Dynamic Bias Control for Efficiency Enhancement

To improve the average power efficiency for WCDMA applications, it is essential to increase the dc power efficiency when the PA enters into the low-power mode, either by decreasing the DC bias current and/or the DC bias voltage.

Fig. 1 shows the DC current consumption of a two-stage class AB power amplifier with fixed bias and a representative CDMA probability distribution function as a function of output power. At low output powers, the power amplifier is operated at a fixed bias current, and therefore, the efficiency is degraded; more than 90 percent of the output power occurs between −15 dBm and +15 dBm, where the efficiency is low.

The average power efficiency over the full range of output powers is:

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$$< \eta >= \frac{< P_{out} >}{< P_{dc} >} = \frac{\int P_{out}\, p(P_{out})\, dP_{out}}{\int \frac{P_{out}\, p(P_{out})\, dP_{out}}{\eta(P_{out})}}, \qquad (1)$$

where P_{out} is the output power, $p(P_{out})$ is probability of a certain output power P_{out}, and $\eta(P_{out})$ is the power-added efficiency at P_{out}. Using the PDF of Fig 1, the average power efficiency of a typical Class-AB amplifier is very low – typically below 2%.

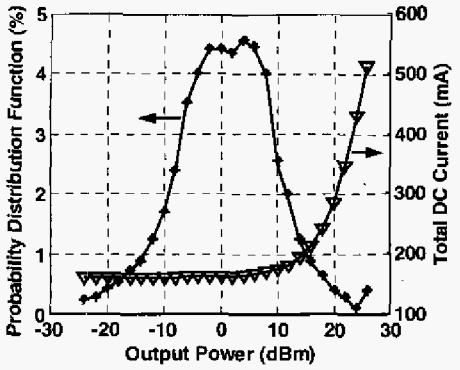

Fig. 1 DC current consumption of a two-stage class AB PA with fixed bias and a representative CDMA probability distribution function (PDF).

A. Principle of Dynamic Biasing

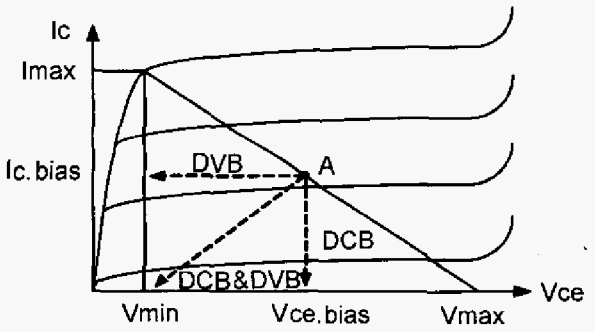

Fig. 2 BJT current versus voltage, demonstrating different dynamic biasing strategies (DC/VB: dynamic current/voltage biasing) [7].

As shown in Fig. 2, we propose an integrated dual dynamic bias control that reduces both the DC bias current and voltage (DCB *and* DVB) without the use of external DC-DC converters using a two-step approach with current re-use in the "low-power" group to reduce the dc voltage across the transistors.

The simplified schematic of the dual dynamic bias in the output stage of a two-stage PA is shown in Fig. 3. There are two groups of SiGe HBT transistors: a high-power group and a low-power group. In the high-power group, the transistors are biased at V_{CC}; whereas in the low-power group the transistors are series-connected and biased at $V_{CC}/2$. The switching between different power groups is controlled by low-loss NFET switches on the bases of the HBT transistors. When the PA enters the low power region, the high-power group is switched off and the low-power group is switched on. In addition to the lower DC bias voltage, the low-power group also operates with a lowered DC bias current; hence the DC power consumption is significantly reduced.

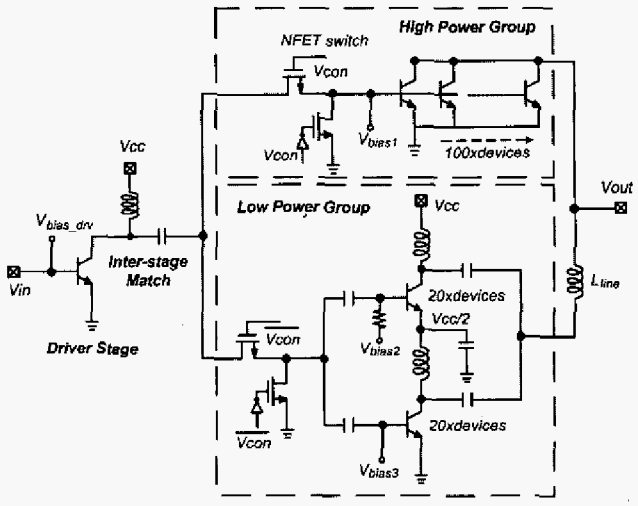

Fig. 3 Simplified schematic of a two-step dual dynamic bias in the output stage of a two-stage PA.

The bias network for CVB is composed of a helper and a low impedance buffer, to provide a constant voltage biasing and terminate the low-frequency components for improved linearity [8].

B. Gain Variation with Power Control

The gain of the PA should remain roughly constant as it switches from low-power to high-power operation. The following design methodologies are employed to achieve this goal.

- A constant collector current density is essential for achieving constant gain [9].
- The connection between two power groups adds parasitics to each individual group, which degrades the overall gain. However, this connection decreases the difference between the gains in two power modes since the input impedance of output stage with the connection changes little between high-power and low-power operations.
- The routing line inductance L_{line} from the output of the low-power group to that of the high-power

group is optimized to boost the gain in the low-power mode by partially resonating some parasitic capacitance.

C. Circuit Considerations

A simplified schematic of the two-stage power amplifier with dual dynamic bias control is shown in Fig. 3. The driver stage, low-power group, and high-power group are all biased in class AB mode, to achieve the best tradeoff of efficiency and linearity. The driver stage has 20 HBTs and the low-power group has 20 switches and 2x20 HBTs in series. The high-power group uses 100 HBTs and 100 NFET switches. Each HBT emitter is 48μm×0.44μm and each NFET switch is 45μm/0.25μm. The optimal design of the NFET switches for power gain and 1dB compression point has been analyzed in [9]. The matching networks are implemented with high-Q off-chip components.

III. Memoryless Digital Predistortion

Linearization techniques improve the linearity of power amplifiers as well as the maximum output power and efficiency. Off-chip Digital Predistortion (DP) is implemented here, because it is well suited to higher levels of digital integration. A block diagram of the DP system is shown in Fig. 4.

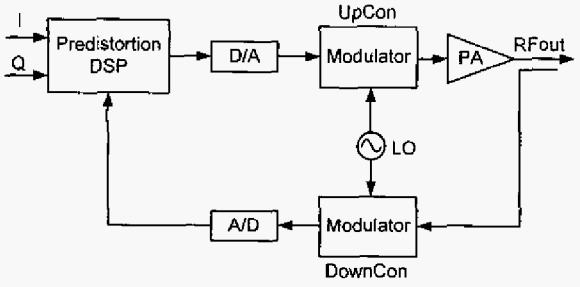

Fig. 4 Block diagram of memoryless digital predistortion.

The DP system downconverts a portion of the 1.95 GHz output signal to an analog IF of 140 MHz, which is then converted to a 12-bit digital second IF of 26.88 MHz at a sample rate of 107.52 MHz and fed to the DSP. After comparison with the corresponding input signal during a "training" period, the resulting error amplitude and phase signal are used to adaptively predistort subsequent input I/Q signals. The predistorted digital signal is converted to a 14-bit analog signal at an IF of 140 MHz, and then upconverted to the final 1.95 GHz output.

IV. Measurement Results

The prototype two-stage power amplifier with the dual dynamic bias control was fabricated in the 250nm IBM BiCMOS 6HP process. The die area is 1mm×1.8mm. A packaged die with bonding wires is shown in Fig. 5.

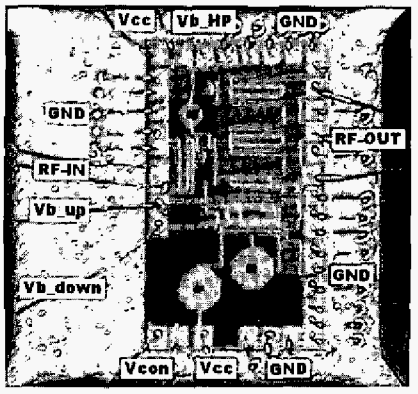

Fig. 5 Photograph of the packaged die of the prototype power amplifier. The die area is 1.8mm^2.

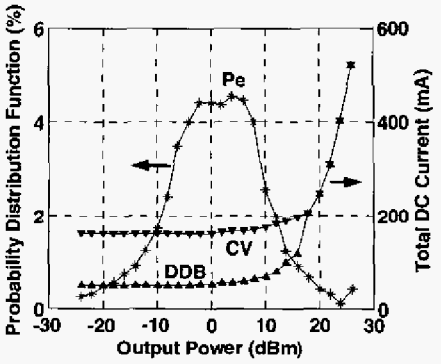

Fig. 6 Output power probability distribution function Pe and measured DC current comparison for different biasing techniques (CV: constant voltage biasing; DDB: dual dynamic biasing). The switching point from high-power mode to low-power mode is 16 dBm.

Fig. 6 compares the measured DC currents for different biasing approaches for the two-stage WCDMA power amplifier, superimposed on a representative probability distribution function for the output power. These approaches include constant base voltage (CV) biasing with a fixed number of parallel transistors (the traditional Class-AB approach) and the dual dynamic bias (DDB) proposed here.

Average power efficiencies are calculated from (1) to be: 1.9% for CV biasing, 3.8% for the Dynamic Current Biasing (DCB) approach proposed earlier [9] and 5.0% for DDB proposed here, all in two-stage PAs. This verifies

that DDB does achieve dramatically improved average efficiency for CDMA applications.

The linearity of the DDB amplifier was also measured with a WCDMA reverse-link signal with and without digital predistortion. The ACPR measurement at 5 MHz is shown in Fig. 7. Note that it is only necessary to utilize the predistortion in the high-power mode, so DP is not applied in the low-power mode; this is the reason for the large discontinuity in ACPR in the "after DP" curve. The ACPR is improved by at least 8dB with digital predistortion, and the maximum output power satisfying the WCDMA linearity specification is improved from 22.4dBm to 26dBm. This satisfies the WCDMA Class III requirement.

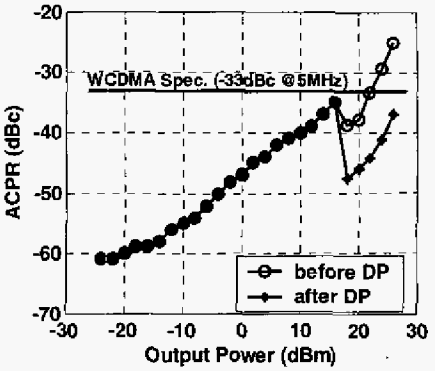

Fig. 7 Measured ACPRs of the DDB power amplifier with digital predistortion (DP) (before DP and after DP).

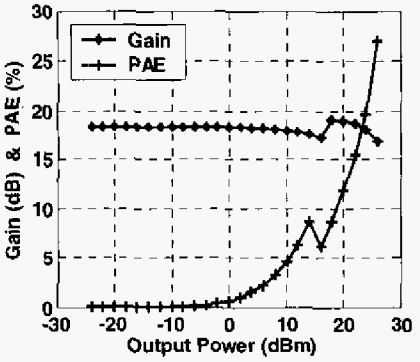

Fig. 8 Measured gain and power added efficiency (PAE) of the DDB power amplifier with DP.

Fig. 8 shows the measured gain and power added efficiency (PAE) of the DDB power amplifier with DP. The gain change for DCB is less than 1.8dB, which is much more constant than the case if the power amplifier is operated with dynamic bias without changing the device size. Since the linear maximum output power increases by 3.6dB (from 22.4 to 26 dBm), the peak PAE is improved by 10% (from 17% to 27%).

V. Conclusions

An integrated two-stage power amplifier chip with dual dynamic bias control and memoryless digital predistortion for WCDMA handset applications was fabricated and measured in a SiGe HBT BiCMOS technology. With the proposed DDB technique, the average power efficiency of the power amplifier is improved from 1.9% to 5.0%. With DP, the ACPR and the peak PAE of the power amplifier are improved by 8dB and 10% respectively. The measured maximum output power is 26dBm, and the peak PAE is 27%.

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