Design and Characterization of a 12 - 40 GHz Power Amplifier in SiGe Technology

Songhui Li, David Fritsche, Corrado Carta and Frank Ellinger

Chair for Circuit Design and Network Theory,
Technische Universität Dresden, Dresden, 01069, Germany

***Abstract*— This paper presents a power amplifier (PA) fabricated in a 0.13 µm-SiGe-BiCMOS technology, which can fully cover the Ku-, K- and Ka-band and delivers a saturated output power of about 20 dBm. The extremely-wide bandwidth results from a distributed structure. The gain cells, which consist of a cascode structure with one stacked transistor, are also optimized for high output power. AC-block transmission lines are used in this design for the DC supply, thus no external bias-tee is needed for circuit operation. Measurements of the fabricated distributed power amplifier (DPA) show a 3 dB-bandwidth of the output power from 12 GHz to 40 GHz. The maximum output power is 19.8 dBm at 1 dB-compression-point (P1dB) and 21.5 dBm in saturation, which to the best knowledge of the authors are the highest reported values for PAs in SiGe-technologies operating in these bands. Together with the peak gain of 13.9 dBm very high power added efficiencies (PAEs) of 13.4 % at P1dB and 20.1 % in saturation are achieved.**

***Index Terms*— broadband amplifier, distributed amplifiers, power amplifiers, BiCMOS integrated circuits.**

I. Introduction

The growing demand for wireless systems strongly motivates research on the development of high performance circuits. Among other applications, there is interest on novel imaging radar systems in Ku/K/Ka-band, which enjoy high resolution, quick real-time capability and large range. The design of circuits to match these requirements is challenging, particularly for power amplifier (PA) design. Compared with the widely for PA design used III/V technologies, SiGe-technologies enjoy a lower fabrication costs and higher integration possibilities with complex digital systems, while still providing transistors of sufficient performance for many applications. To achieve both high power and wide bandwidth in SiGe-technologies, a relatively complex circuit topology is needed. For high output power, a differential PA with transformers [1] and a pseudo-differential PA [2] have been reported. For multi-band applications a reconfigurable K-/Ka-band PA is presented in [3]. Since distributed amplifiers are well suited for large bandwidth, there are reported examples of distributed PAs for extremely broad bands [2] and multi-band applications [4]. Currently a novel OFDM-MIMO radar system is being developed for the future applications in aviation, security, automotive and automation sectors. In that a single-ended PA with $20\,\mathrm{dBm}$ of linear output power from $12\,\mathrm{GHz}$ to $40\,\mathrm{GHz}$ is specified: these requirements exceed the present state of the art. In this paper, we present the design for an extremely broadband PA in a $0.13\,\mu\mathrm{m}$-SiGe technology with f_t and f_max of $250\,\mathrm{GHz}$ and $300\,\mathrm{GHz}$, respectively. A distributed structure is used to achieve the extremely large bandwidth. The gain cell is optimized for high output power and at the same time to keep the $3\,\mathrm{dB}$-bandwidth of output power in the specified frequency range. With this approach, a good trade-off has been made between the output power and the frequency range, meeting the specifications.

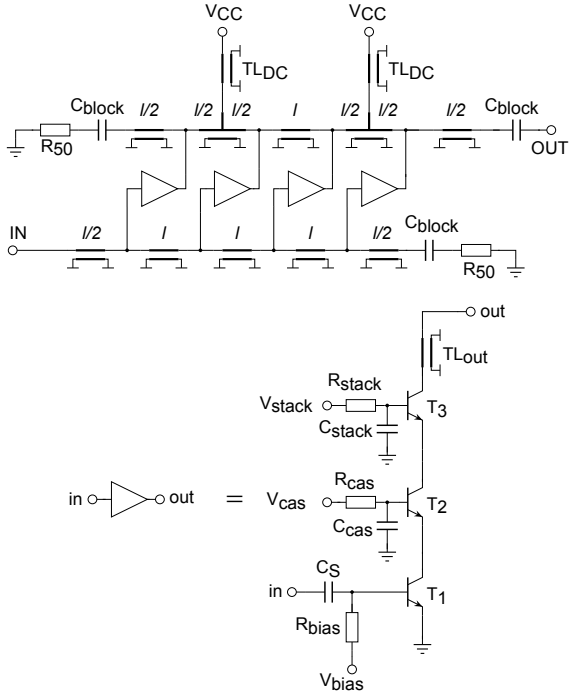

Fig. 1: Schematic of the fabricated distributed power amplifier

II. Circuit Implementation

The schematic of the presented distributed power amplifier (DPA) is shown in Fig. 1. It is a distributed structure with four identical gain cells. A $50\,\Omega$ resistor $\mathrm{R_{50}}$ in series with a DC-block capacitor $\mathrm{C_{block}}$ is used as terminator at the end of both input and output lines. Four gain cells,

which consist of a cascode structure with one additional stacked transistor, are combined by input and output lines to reach the specified output power. Transistors $T_{1/2}$ realize the cascode structure. Thanks to its good isolation between input and output, the input and output lines can be designed and operate independently. Transistor T_3 is placed to provide a larger voltage swing at the output, resulting in higher output power [5]. While the gain cells of conventional traveling wave amplifiers (TWAs) are optimized for small signal gain [6], [7], in a DPA they must be optimized for maximum output power. For the presented circuit, the gain cells are designed to deliver peak power through the output line over the load of $50\,\Omega$. The input and output physical transmission lines have a high characteristic impedance Z_c of $83\,\Omega$ ($L' = 531\,\mathrm{nH/m}$ and $C' = 77\,\mathrm{pF/m}$) and a length l of $400\,\mu\mathrm{m}$. The series capacitor C_S at the input of the gain cells and the series transmission line TL_{out} at their output are set such, that the input and output capacitances of the gain cells are both $70\,\mathrm{fF}$. For the synthetic transmission line the equivalent characteristic impedance is

$$Z_{c,\,equ} = \sqrt{\frac{L'}{(C' + C_{par}/l)}}. \qquad (1)$$

The $70\,\mathrm{fF}$-capacitance C_{par} is distributed over the input and output line realizing a synthetic line with $Z_{c,\,equ}$ close to $50\,\Omega$. To supply DC power to the DPA a transmission line TL_{DC} is used: with properly chosen length, it works as $\lambda/4$ shorted stub for a sufficiently high impedance in the frequency range of interest to serve as AC-block. The line width is selected to match two requirements: on one hand it must be wide enough to sustain the large DC current for the DPA and on the other hand it is designed to contribute to the in-band flatness of the gain. In this design, a pair of TL_{DC} with length, width and spacing to the side wall of $1250\,\mu\mathrm{m}$, $6\,\mu\mathrm{m}$ and $10\,\mu\mathrm{m}$ are placed. This avoids the use of an external bias-tee at the RF output node and simplifies significantly the integration in large systems on chip.

III. Measurement Results

As shown in Fig. 2 is a photograph of the fabricated DPA. The total chip area is $1166\,\mu\mathrm{m} \times 1020\,\mu\mathrm{m} = 1.19\,\mathrm{mm}^2$. In its nominal operation point, the circuit is biased with V_{bias}, V_{cas} and V_{stack} of $4\,\mathrm{V}$, $2\,\mathrm{V}$ and $3.2\,\mathrm{V}$, respectively. The supply voltage V_{CC} applied for characterization is $4.5\,\mathrm{V}$. The total DC current I_{DC} of $155\,\mathrm{mA}$ flows in two equal parts through a pair of TL_{DC} in the four gain-units. An emitter area of $A_E = 20 \times 1 \times 0.12\,\mu\mathrm{m}^2$ is chosen for the transistors in gain-unit. The DC current is then $1.9\,\mathrm{mA}$ per transistor.

The output power as a function of input power at $12\,\mathrm{GHz}$, $21\,\mathrm{GHz}$ and $40\,\mathrm{GHz}$ is shown in Fig. 3. As the input power increases the gain of the DPA remains constant then begins to drop, reaching the $1\,\mathrm{dB}$-compression-point (P1dB) and saturation. The maximum output power of

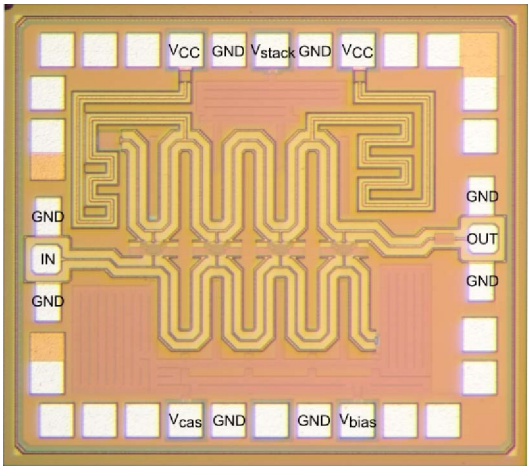

Fig. 2: Chip photograph of the DPA (total chip area: $1166\,\mu\mathrm{m} \times 1020\,\mu\mathrm{m}$)

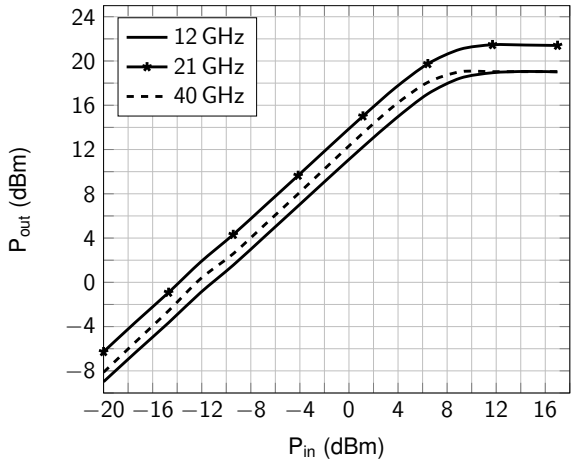

Fig. 3: Measured output power as a function of input power from -20 dBm to 16 dBm at 12 GHz, 21 GHz and 40 GHz

the available instrumentation is $12\,\mathrm{dBm}$ in the $32\,\mathrm{GHz}$-$50\,\mathrm{GHz}$-band, which is not sufficient to saturate the circuit.

The output power levels as a function of frequency at P1dB and in saturation are depicted in Fig. 4. The peak values of the output power at P1dB and in saturation are $19.8\,\mathrm{dBm}$ and $21.5\,\mathrm{dBm}$. The required frequency range from $12\,\mathrm{GHz}$ to $40\,\mathrm{GHz}$ is also fully covered in the $3\,\mathrm{dB}$-bandwidth of the output power from the DPA.

The measured circuit efficiency η and power-added-efficiency (PAE) of the DPA are shown in Fig. 5. In the target frequency range the PAE at P1dB has a peak value of $13.4\,\%$ and PAE in saturation of $20.1\,\%$. The maximum values of the η are $14.2\,\%$ at P1dB and $23.7\,\%$ in the saturation.

Table I compares this work with state-of-the-art PAs operating in the Ku-/K-/Ka-band and implemented in SiGe-technologies. The output power at P1dB and the saturated output power are the highest reported for PA designs

TABLE I: Comparison with state-of-the-art power amplifier

REF	Peak gain (dB)	$P_{\text{-1dB}}$ (dBm)	P_{sat} (dBm)	Peak PAE	Freq. range (GHz)	Technology
[1]	19.6	10.9	11.9	7.2 %	20-26	65 nm CMOS
[2]	10	$16.7^{(*)}$	$17.5^{(*)}$	13.2 %	DC-77	0.13 µm SiGe BiCMOS
[3]	16.3	9.6	11.1	55.9 %	24.3-35	0.18 µm SiGe HBT
[4]	17.1	2.9	8.8	7.1 %	10-40	0.18 µm SiGe BiCMOS
[8]	12	14.9	-	$9.7\,\%^{(**)}$	14-105	90 nm SiGe BiCMOS
this work	13.9	19.8	21.5	20.1 %	12-40	0.13 µm SiGe BiCMOS

(*): differential output, (**): at 1 dB compression point

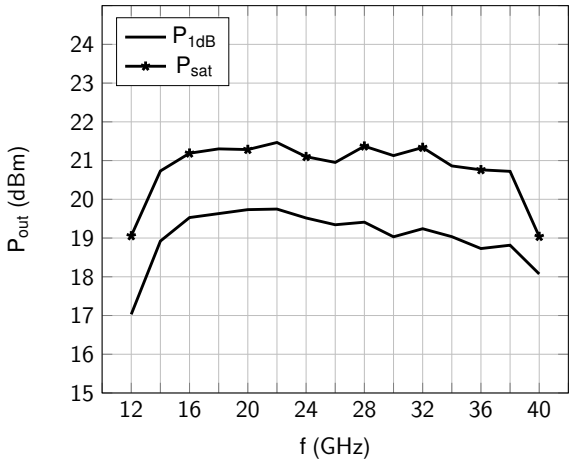

Fig. 4: Measured output power at P1dB and in saturation as a function of frequency from 12 GHz to 40 GHz

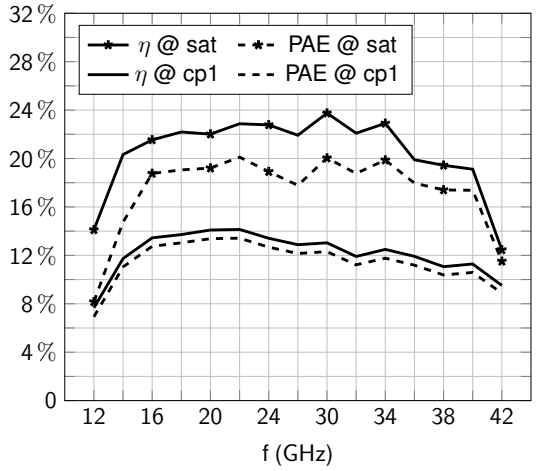

Fig. 5: Measured circuit efficiency η and PAE of DPA

in SiGe-technologies operating in these bands. The high output power also results in a high PAE.

IV. Conclusion

A distributed power amplifier was designed and integrated in a 0.13 µm SiGe BiCMOS technology. Aiming at an output power of about 20 dBm, four gain units, which consists of a cascode structure with one stacked transistor, were employed. Measurements of the fabricated chip show a gain of 13.9 dB over frequency range from 10 GHz to 40 GHz with 19.8 dBm output power at P1dB. The maximal output power in saturation is 21.5 dBm, corresponding to a PAE of 20.1 %.

Acknowledgment

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