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A Highly Linear 25-32 GHz Power Amplifier with 22-dBm Output Power and 30% PAE in 130-nm SiGe BiCMOS

Chun Deng[1,2], Li-Qun Ye[2], Min Gong[1]

[1] Department of Microelectronics, Sichuan University, Chengdu, China
[2] Corpro Technology Co., Ltd, Chengdu, China

***Abstract*—In this paper, a two-stage, two-way transformer combined power amplifier (PA) operated in 25-32 GHz frequency range in 130-nm SiGe BiCMOS technology is proposed. We propose the output cell parameters optimization targeting high gain, OP_{1dB}, and PAE for SiGe BiCMOS HBT. Based on the derived transformer model and graphical matching procedure, we present an optimization methodology to design low loss output, inter-stage and input transformers. The inductive source degeneration is utilized to broaden impedance matching bandwidth. Measurement results show that the proposed PA achieves 26 dB gain, 1-dB compressed output power of 22.1-dBm and 30% power-added efficiency (PAE) at 1-dB compression point.**

Keywords*—*5G, Power amplifier, Transformer, SiGe BiCMOS

I. Introduction

The 28-GHz spectrum is currently being proposed for the next fifth-generation (5G) cellular systems with gigabit-per-second access and backhaul networks. Recently, silicon-based standalone RF PAs have been reported in both SiGe BiCMOS and CMOS technology.

Stacked field transistors are used in CMOS millimeter-wave PAs to achieve higher voltage swing, while at the cost of low power efficiency and linearity degradation [1]. Another technique to increase output power of PAs is power combining technique. In [2], a transformer-based series-parallel combined PA is proposed to achieve higher output power while not degrading linearity. Recently, many high-linearity and high-efficiency millimeter-wave 5G PAs have been reported [3-5]. This work presents a two-stage transformer-based 28 GHz SiGe BiCMOS power amplifier.

II. Circuit Design

Fig.1 shows the schematic of the proposed differential transformer coupled power amplifier with power stage of PA and driver stage of DA. Cascode structures are used because of higher allowed voltage swing at collectors, higher gain and better inverse isolation. The base of common base transistors are terminated with high quality dual-layered MIM capacitors. Considering compromise between gain and stability, the CB bypass capacitor of PA and DA devices are set to 1pF and 0.4pF, respectively. Transformers are used to perform impedance matching in output, inter and input stage networks. Stacked transformers are implemented as vertical spirals utilizing top two thick metals, with width of 20μm for output transformer and 9μm for input-stage and inter-stage transformers.

A. Output stage power cell parameter optimization

Each power cell is composed of m× parallel CBEBC SiGe HBTs with an f_t of 260 GHz, emitter width and length of 0.12μm and 18μm, respectively. To choose optimal operation point, the load-pull simulation with RCL-extracted power cell is performed. The gain, 1-dB compression point output power (OP_{1dB}) and PAE versus the number of power cell m and bias current are illustrated in Fig. 2(a) and (b). To increase output power, more parallel cells could be used, while increased parasitics reduce both gain and bandwidth of PA, thus, there exists an optimal m to obtain maximum output power and PAE. For fixed m, the gain increase with the increase of J_{PA}. Therefore, m = 5 and J_{PA}=4mA/18μm are chosen to achieve considerable gain and output power with PAE of 40%.

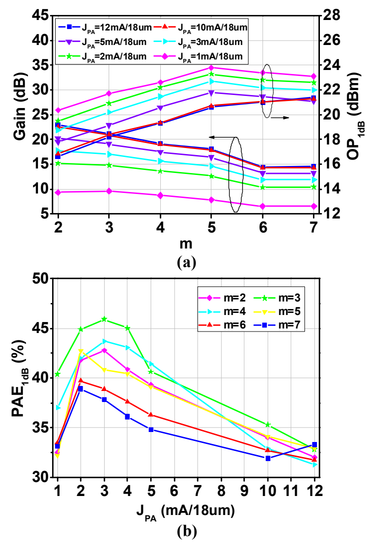


Fig. 2 Parameter optimization of output stage power cell. (a) Gain and OP_{1dB} versus parallel number of power cell. (b) PAE versus biased current density

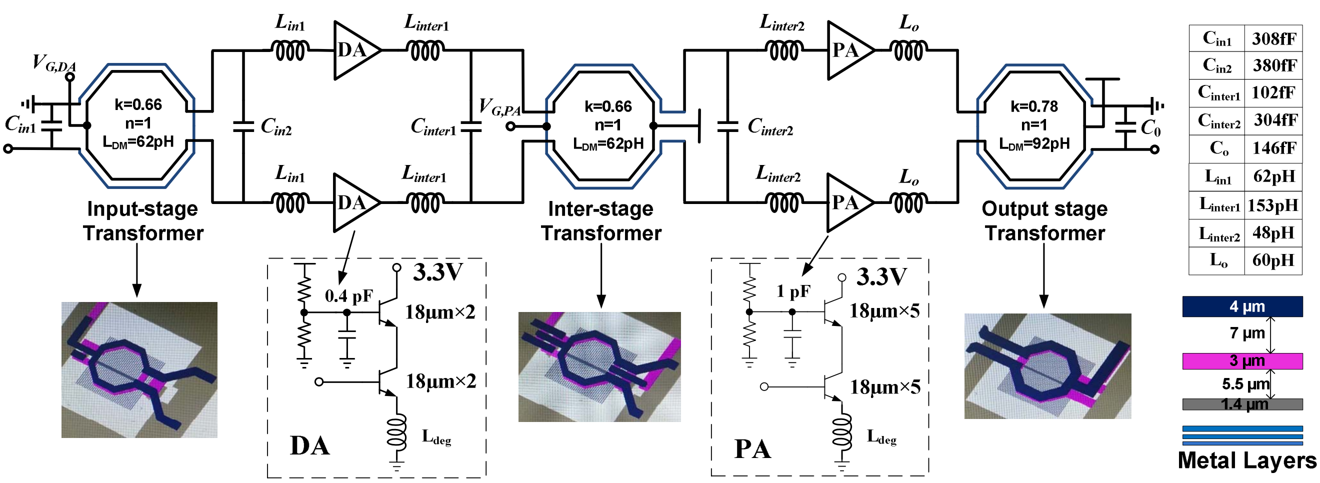


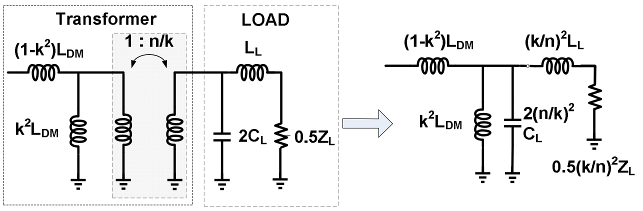
Fig. 1 Schematic of the two-stage transformer-coupled power amplifier

B. *Output, inter and input stage matching*

The load-pull simulations indicate that the single-ended cascade PA can achieve 22.2-dBm OP_{1dB} and 40.4% PAE_{1dB} for Z_{opt}= 10.9+j8.3 with current density of 4mA/18μm. The output transformer is designed to transform Z_{opt} to 50Ω. The inter-stage network which consists of inter-stage transformer, matching inductor (L_{inter1} and L_{inter2}) and matching capacitance (C_{inter1} and C_{inter2}) needs conjugate matching, starting from the input impedance of PA to the conjugate output impedance of DA. Compared to inter-stage matching, the transformation ratio of input matching is much larger thus causing less bandwidth. To broaden input matching bandwidth, the inductive degeneration technique is used.

C. *Transformer modeling*

Fig.3 shows the transformer equivalent half-circuit model and simplified model. The simplified model can be derived by removing the ideal transformer with load impedance transformation, which consists of a series leakage inductance $(1-k_2)L_{DM}$, a shunt magnetizing inductance k_2L_{DM}, where k denotes coupling coefficient between primary coil and secondary coil, n denotes turn ratio of secondary coil to primary coil, L_{DM} denotes half-equivalent inductance of primary coil. The capacitive load needs a factor of $(n/k)^2$, and inductive load needs a factor of $(k/n)^2$.



(a) (b)

Fig.3 (a) Transformer equivalent half-circuit model (b) Simplified model

III. MEASUREMENT RESULTS

The proposed 28 GHz PA is designed in 130-nm SiGe BiCMOS technology, and the die photograph is shown in Fig.4. The PA core occupied 1100×340μm². The S-parameter results are shown in Fig. 5, achieve peak S21 of 26.4 dB, less than 3-dB gain variation and better than 15-dB return loss. The large-signal characteristics at 28 GHz are presented in Fig. 6. The saturated output power and OP_{1dB} are 23-dBm and 22.1-dBm, respectively. The maximum PAE is 30.8% and PAE_{1dB} is 30%. Measurement results show that, the OP_{1dB} and PAE_{1dB} are higher than 21dBm and 29% across 25-32 GHz.

TABLE I. COMPARISON OF REPORTED POWER AMPLIFIERS

Reference	This work	[1]	[3]	[4]	[5]
Freq.(GHz)	28	24	28	30	28
Topology	2-stage Cascode	1-stage 3-stack	1-stage 2-stack	2-stage CS	2-stage Cascode
Gain(dB)	26	13	13.6	15.7	28.6
P_{SAT}(dBm)	23	25.3	19.8	14	23.7
OP_{1dB}(dBm)	22.1	23.8	18.6	13.2	23.2
PAE_{max}(%)	30.8	20	43.3	35.5	32.7
PAE_{1dB}(%)	30	N.A.	41.4	34.3	32.7
Core Area (mm²)	0.374	0.28	0.28	0.16	0.71
Technology	130-nm SiGe BiCMOS	45-nm SOI CMOS	28-nm CMOS	28-nm CMOS	180-nm SiGe BiCMOS

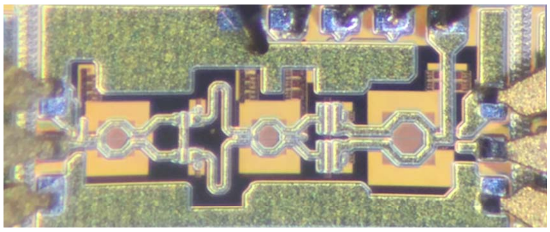


Fig.4 Die photograph of the proposed 28 GHz PA

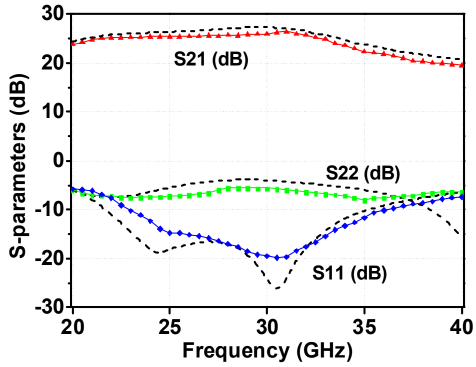


Fig.5 S-parameters measurement results
(Simulation results are shown with dashed curves).

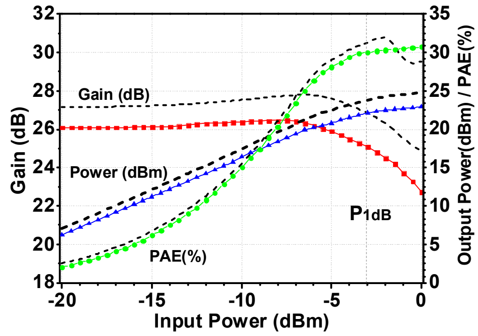


Fig.6 Swept power measurement results at 28 GHz
(Simulation results are shown with dashed curves).

IV. CONCLUSION

A high linear and efficient two-stage, two-way transformer combined power amplifier operating in 25-32 GHz using 130-nm SiGe BiCMOS technology is developed. We demonstrate an output cell parameters optimization methodology and output, inter-stage and input network matching procedure. Application of these techniques results in a high OP_{1dB} of 22.1-dBm and 30% PAE_{1dB} at 28 GHz.

REFERENCES

[1] S. R. Helmi, et al., "High-Efficiency Microwave and mm-Wave Stacked Cell CMOS SOI Power Amplifiers" *IEEE Trans. Microw. Theory and Techn.*, vol. 64, no. 7, pp. 2025-2038, June 2016.

[2] J. Kim, et al., "A Fully-Integrated High-Power Linear CMOS Power Amplifier With a Parallel-Series Combining Transformer" *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 599-614, Mar. 2012.

[3] B. Park, et al., "Highly linear mm-wave CMOS power amplifier" *IEEE Trans. Microw. Theory and Techn.*, vol. 64, no. 12, pp. 4535-4544, Dec. 2016.

[4] S. Shakib, et al., "A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS" *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3020-3036, Dec. 2016.

[5] A. Sarkar, et al., "A 28-GHz SiGe BiCMOS PA with 32% efficiency and 23-dBm output power" *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1680-1686, June 2017.