A CMOS RF Polar Transmitter of a UHF Mobile RFID Reader for High Power Efficiency

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***Abstract*—A CMOS radio frequency (RF) polar transmitter architecture for a UHF (860–960 MHz) RF identification (RFID) reader is proposed, which consists of a switch-mode CMOS power amplifier (PA) and an analog pulse-shaping filter implemented in 0.25-μm CMOS process. The amplitude modulation of a amplitude shift keying signal is performed by simply switching the common gate transistor of a cascode power amplifier. Extremely low power consumption is achieved when the PA is switched off. The power efficiency of the transmitter is enhanced not only by using switching power amplifier but also by employing this architecture.**

***Index Terms*—Amplitude shift keying (ASK), CMOS power amplifier, polar transmitter, radio-frequency identification (RFID) reader.**

I. Introduction

An emerging issue of mobile radio-frequency identification (RFID) readers is that the area occupied by the circuitry of the mobile RFID reader should be small enough for integration with other communication systems such as GSM and W-CDMA in a handset application. By virtue of its ability to be scaled down, CMOS technology is considered as the best way to integrate the whole transceiver of an RFID reader in a single chip at low cost. In order to realize full integration, the power amplifier should be also integrated in a single chip with CMOS process.

Some research has been made toward a fully-integrated CMOS power amplifier (PA) for RFID reader applications [1], [2]. Since the RFID reader adopts binary-amplitude shift keying (ASK), conventional transmitters of RFID readers with direct up-conversion architecture are based on the I/Q modulation scheme which utilizes a linear PA to convey data by means of the amplitude of the signal [Fig. 1(a)]. However, the linear PA in CMOS technology suffers from poor power efficiency, especially when the envelope of transmitted signal varies frequently. Thus, in order to increase the power efficiency, a polar transmitter with a switch-mode PA is preferable.

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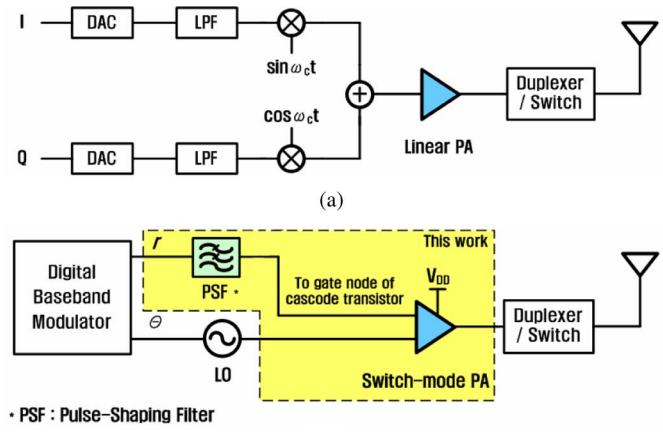

Fig. 1. (a) Conventional transmitter with a linear PA and (b) proposed transmitter with a switch-mode PA for a RFID reader.

In this letter we present a fully-integrated switch-mode CMOS PA fabricated in 0.25-μm CMOS process, and propose polar transmitter architecture, as shown in Fig. 1(b), for a UHF mobile RFID reader using binary-ASK. The CMOS PA is designed with a cascode structure and shows a class-E operation with more than 24 dBm of output power at 910 MHz and with more than 35 % of power-added efficiency (PAE) from 860 to 960 MHz under 2.5 V supply voltage. The polar transmitter with the CMOS PA modulates the amplitude signal by turning on and off the common gate transistors of the cascode structure. To comply with the transmit mask regulation of EPC global class-1 generation-2 [6], an analog pulse-shaping filter is attached in front of the cascode gate node of the PA.

II. Implementation

A. CMOS Power Amplifier

Fig. 2(a) is the schematic of the proposed CMOS power amplifier. With a fixed bias voltage at the gate of the cascode transistors ($\mathrm{M}_3, \mathrm{M}_4$), the power stage of the PA shows a class-E operation. To prevent the PA from a device breakdown, the power stage is composed of transistor stacks ($\mathrm{M}_1 - \mathrm{M}_4$) in a cascode configuration, and the entire circuit of the PA is designed in a differential structure to form an ac virtual ground which reduces the effect of the source degeneration inductance [3]. The driver stage, as proposed in [4], consists of a three-inverter chain with feedback resistors which operates in the class-D region. This configuration achieves high power efficiency due to the generation of a square wave signal to the power stage. To apply a

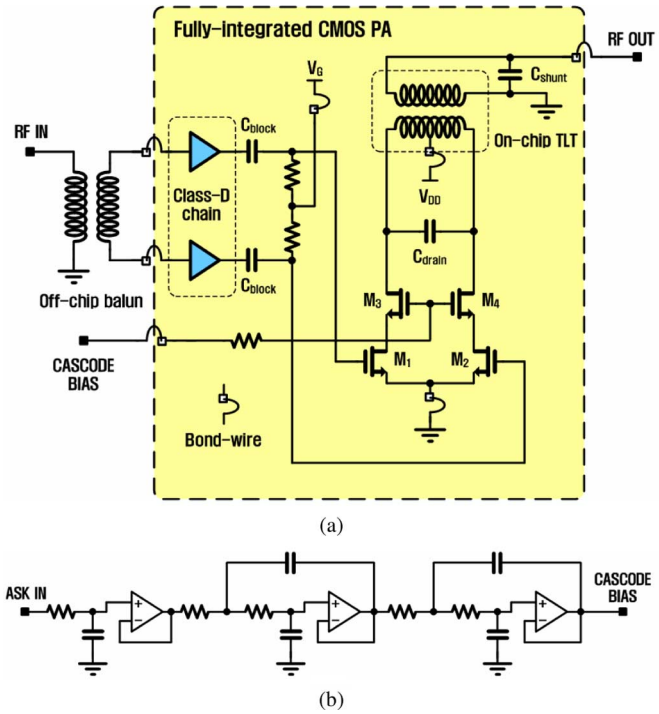

Fig. 2. (a) CMOS power amplifier and (b) an active low-pass filter for analog pulse-shaping.

proper bias at the gate of the common source transistors in the power stage, an additional supply of 0.9 V (V_G) is used. The output matching is implemented using an on-chip transmission line transformer, which is an amenable technique for the full integration of a PA in a single chip [3]. An off-chip balun is used because we suppose that RF input nodes of the PA connected with the output of an RF local oscillator are differential, and that the integration of the input balun is thus unnecessary.

B. PoLar Transmitter Supporting Binary-ASK

Since the binary-ASK is represented by on/off symbols, its implementation using polar transmitter architecture can be simplified. Although the transmit signal has a non-constant envelope, the transmit voltage has only two levels and the modulation can be realized by switching the bias of a switch-mode PA on and off. Therefore, power efficiency is improved through reduction of power consumption, especially when the PA is switched off, in contrast with a conventional transmitter using a linear PA, which consumes more power since the idle dc current still flows during the off-state.

In general, a modulated envelope signal in the polar transmitter is connected to the drain node of the switch-mode PA [5]. To control the drain voltage of the PA of a polar transmitter, a switching regulator or a low-dropout regulator is needed in the envelope modulation path, which makes the design of the transmitter more complicated. As shown in Fig. 1(b), the envelope signal of the proposed transmitter is directly introduced at the gate bias of cascode transistors which is indicated with "CASCODE BIAS" in Fig. 2(a). Thus, the complexity of the circuit design can be reduced.

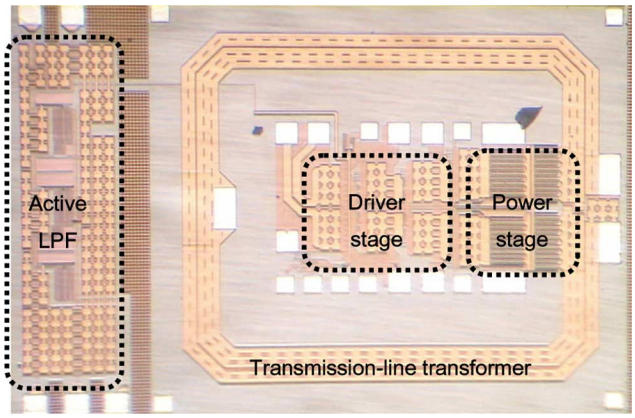

Fig. 3. Chip photograph.

However, the introduction of the square wave from a digital baseband modulator without pulse-shaping ruins the spectral property of the transmitter, causing interference to other channels in the practical wireless communication, which is undesirable [6]. To suppress interference to adjacent channels, a low-pass filter is attached before the gate of the cascode transistors to smooth the sharp transition of envelope signal.

C. Pulse-Shaping Filter

A general approach to generate a pulse-shaped waveform is implemented by combining a digital technique activating a read-only memory (ROM) which stores the levels of waveform with analog filtering for reconstruction of the signal [7]. In spite of the advantage of reducing the area otherwise occupied by a large analog filter, this method results in greater power consumption due to digital components and a D/A converter, especially when the sampling rate is high. In order to increase overall transmitter power efficiency, an analog pulse-shaping method using an active low-pass filter is adopted, as shown in Fig. 1(b). The active filter, shown in Fig. 2(b), is the fifth-order Bessel low-pass type to suppress the out-of-band components without distortion. The design complexity is also reduced in comparison with the digital and analog combination method.

III. Measurement Results

The photograph of the chip fabricated in 0.25 μm CMOS process is shown in Fig. 3. The total size of the chip, including a power amplifier and a pulse-shaping filter, is 1.6 mm $\times$ 2.2 mm. Fig. 4(a) shows the measurement results of a stand-alone type CMOS PA in the range of 860 to 960 MHz. The gate node of the common gate transistors is tied to V_{DD} of 2.5 V (CW mode), and the PA shows a class-E operation with 25.2 dBm of output power at 860 MHz. The peak of PAE is 42.5 % at 860 MHz. Fig. 4(b) implies that the PA operates at saturation mode with more than -1 dBm input power.

The test configuration of the proposed polar transmitter for a UHF RFID reader is as follows. An Agilent E4438C signal generator plays the role of a local oscillator, and a square wave which corresponds to data-0 and data-1 with 25 μs Tari, respectively [6] is continuously introduced to the input of the pulse-shaping filter, indicated as 'ASK IN' in Fig. 2(b), as a pulse

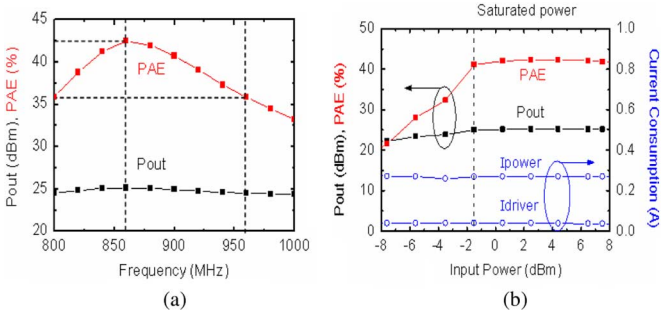

Fig. 4. Output power and PAE of the stand alone CMOS PA according to the variation of (a) the frequency and (b) the input power in the CW mode.

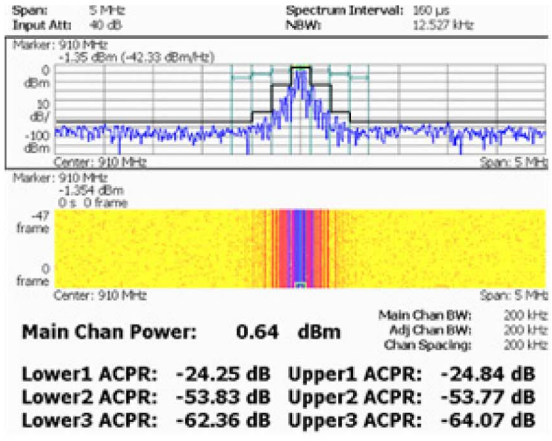

Fig. 5. Measurement results of ACPR (a) with data-0 input and (b) with data-1 input under 25 μs Tari condition respectively [6]

interval-encoded data input to transmit. The output spectrum is observed using a Tektronix WCA280A wireless communication analyzer with an RFID measurement setup. Each channel bandwidth and channel spacing is set to 200 kHz. Fig. 5 shows the adjacent channel power ratio (ACPR) measured with the real-time spectrum analyzer mode of WCA280A at the center frequency of 910 MHz, and the observed result complies with the transmit mask regulation of EPC global class-1 generation-2 for UHF RFID protocol. The measured main channel power is larger than 20 dBm. The comparison between the other measurement results and EPC global specification is summarized in Table I.

TABLE I
PERFORMANCE OF THE PROPOSED POLAR TRANSMITTER FOR A RFID READER*

Performance		Specification of EPC global [6]		Measured data	
		Data-0	Data-1	Data-0	Data-1
ACPR	1st adj. ch. (dBc)	< -20		-24.25	-29.66
	2nd adj. ch. (dBc)	< -50		-53.77	-58.07
	3rd adj. ch. (dBc)	< -60		-62.36	-62.46
Power up/down	Rise time (μs)	< 8.333		4.033	4.092
	Fall time (μs)	< 8.333		4.407	4.882
RF envelope	On width (μs)	> 6.625 < 13.125	> 19.875 < 39.375	12.97	37.38
	Off width (μs)	> 6.625 < 13.125	> 6.625 < 13.125	12.03	12.62
Modulation depth (%)		Min. 80 Typically 90		98.22	97.96

* The specification is based on the 25- μs Tari.
* The center frequency of the measured data is 910 MHz.

IV. CONCLUSION

A polar transmitter for a UHF RFID reader including a switch-mode CMOS PA and an analog pulse-shaping filter is proposed. The stand-alone CMOS PA with a fixed bias condition emits output power of more than 24 dBm with PAE of more than 35 % at 860 to 960 MHz. By turning on and off the common gate transistor in the cascode structure of the switch-mode CMOS PA, binary-ASK is realized in a more power-efficient manner than that of the I/Q modulation with a linear PA. The linear PA must have idle dc current during the off-state whereas a switch-mode PA suppresses it. In addition, the integrated pulse-shaping filter reduces interference of a transmit signal to adjacent channels. Moreover, the proposed transmitter is expected to be fully integrated with the digital baseband modulator in a single chip since the whole functional block is implemented using CMOS technology.

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