A Fully-Integrated 900-MHz CMOS Power Amplifier for Mobile RFID Reader Applications

Jeonghu Han, Younsuk Kim, Changkun Park, Dongho Lee, and Songcheol Hong

Dept. of Electrical Engineering and Computer Science, KAIST, Daejeon, 305-701, Korea

***Abstract* — A 900-MHz linear power amplifier has been fabricated for ultra-high-frequency (UHF) radio frequency identification (RFID) reader applications using a 0.25-μm CMOS technology. An on-chip transmission-line transformer is used for output matching network. Input and inter-stage matching components, and RF chokes are fully integrated in the designed amplifier so that no external components are required. The power amplifier provides linear output power of 27 dBm at 920 MHz with a 2.5-V supply. Power-added-efficiency (PAE) at 1-dB-gain-compression point (*P*1dB) is 28 %. Gain flatness over the full UHF RFID band, which covers from 860 MHz to 960 MHz, is 1 dB.**

***Index Terms* — CMOS power amplifiers, distributed active transformer, linear power amplifiers, radio frequency identification (RFID)**

I. Introduction

Radio frequency identification (RFID) is a wireless communication technology in which a reader captures data encoded in tags using radio waves [1]. RFID technology realizes automatic identification of remote objects to which RFID tags are attached. As the worldwide RFID market has been growing tremendously, RFID has become an essential field of research in modern industry [1]–[3]. Potential applications of RFID are currently driving hardware developers to merge RFID readers into mobile devices such as PDAs and cell phones, which will enable individual customers in a *smart shop* to acquire product information through their own RFID readers [1], [2]. In the integrated-circuit (IC) design field, therefore, great efforts are directed to develop a fully-integrated CMOS single-chip solution for an RFID system. One of the most difficult parts to implement in silicon is power amplifier. Because of low breakdown voltage and poor passive devices in a CMOS process, it is challenging to design a fully-integrated CMOS power amplifier with high output power, efficiency, and linearity [4].

Recent studies have demonstrated that class-E CMOS power amplifiers can provide high efficiency above 40 % when fully integrated [4] and above 60 % with external matching components [5]. Linear power amplifiers in CMOS, however, generally have much lower efficiency at linear output power. Several papers have reported the development of CMOS linear power amplifiers for wireless local area network (WLAN) applications, and their power-added-efficiency (PAE) are typically 15 % to 25 % at 1-dB gain-compression point (*P*1dB) [6] –[10].

This paper demonstrates a two-stage linear power amplifier for mobile RFID reader applications. The amplifier was fabricated in a 0.25-μm CMOS technology. An on-chip *transmission-line transformer* is used for output impedance-matching and power-combining, based on a *distributed-active-transformer* (DAT) which was originally proposed by I. Aoki *et al.* [4]. Input and inter-stage matching networks, RF chokes, and an input balun transformer are all integrated on-chip so that no external components are needed. Although reading-range in mobile RFID systems is assumed to be less than a meter, maximum output power from a reader should be larger than 24 dBm to provide enough power for the IC in a tag to power up and transmit a response. The fabricated power amplifier achieves linear output power of 27 dBm and PAE of 28 % at *P*1dB with a 2.5-V supply. The amplifier has small-signal gain flatness of 1 dB over the whole ultra-high-frequency (UHF) band of RFID, which covers from 860 MHz to 960 MHz.

II. CMOS Power Amplifier Design

Power transistor is a key element determining maximum available output power and efficiency. In this work, power transistors were designed by combining n-channel 2.5-V MOSFETs with gate length of 0.25 μm. The width of a unit gate-finger is 5 μm. To prevent the transistors from breakdown, cascode topology is used, in which common-source and common-gate stages are connected in series. Fig. 1 shows the schematic of the 900-MHz CMOS power amplifier designed for mobile RFID reader applications. The power stage in this amplifier has two differential pairs of cascode-transistors and an output matching network combining the transistors. A width of 5.12 mm was chosen for the gate of the power transistors, *M*5 to *M*12, in order to achieve high output power more than 27 dBm. The output matching network is realized by a magnetically-coupled on-chip transformer in a similar way to a DAT

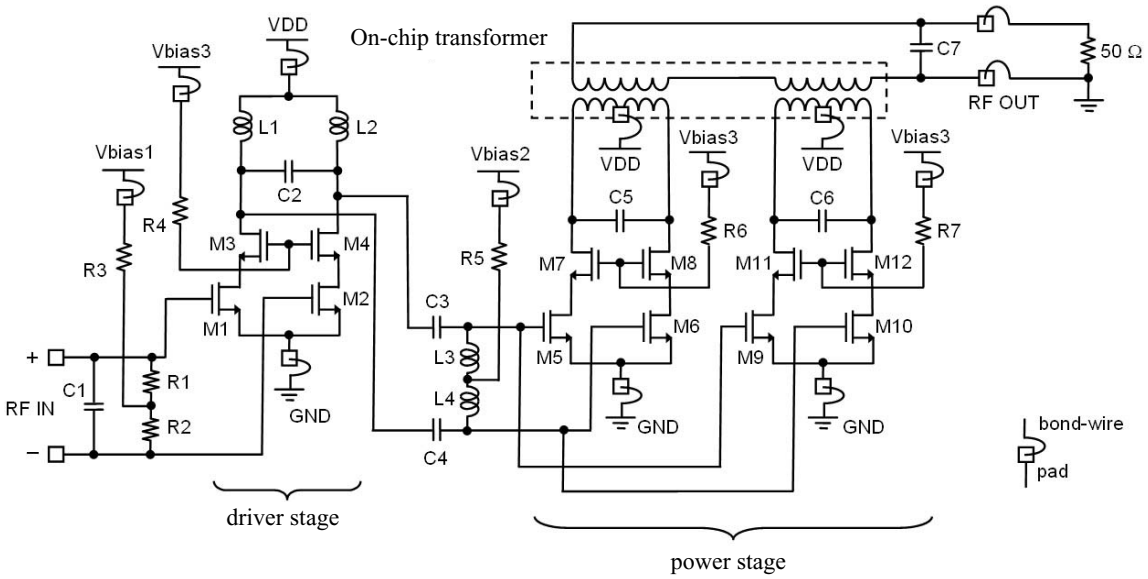

Fig. 1. Schematic of the two-stage differential CMOS power amplifier with an on-chip transmission-line transformer.

proposed in [4]. Inductance of the output transformer determines the frequency band for maximum power transmission, together with shunt capacitors, *C*5 and *C*6. Layout and operation of the output transformer will be discussed in Section III.

The driver stage in Fig. 1 consists of a differential pair of cascode-transistors and RF choke inductors. The gate width is 1.28 mm for the transistors in this stage, *M*1 to *M*4. Resistors, *R*1, *R*2, and a capacitor, *C*1 are input-matching components. The other on-chip components, *L*1, *L*2, *L*3, *L*4, and *C*2 are used for inter-stage matching, and their values were chosen so as to achieve high output *P*1dB. Both the driver and power stages operate in class-AB, or near class-B according to a trade off among high gain, *P*1dB, and efficiency.

III. Layout and Simulation

A. Output Transformer Layout

A microphotograph of the fabricated chip is shown in Fig. 2. In order to achieve high quality factor, the output transformer is designed using half-turn inductors and a single-turn metal strip instead of spiral coupled-inductors [4]. The half-turn inductors, forming the primary loop of the transformer, combine output power from a couple of the differential pairs of power transistors. The power is then magnetically coupled to the secondary loop, and delivered to the load. The widths of the primary and secondary loops are 80 μm and 60 μm, respectively, while the spacing between them is 5 μm. The size of the on-chip transformer is 1.5 mm × 2.2 mm. The total length and the area of the transformer will be reduced for operating frequencies higher than 1 GHz. Both the primary and secondary parts are made of a top metal layer only. The physical thickness of the top metal layer is 1.5 μm.

Inter-stage matching inductors, *L*3 and *L*4, DC-blocking capacitors, *C*3 and *C*4, shunt capacitors, *C*5 and *C*6, and power transistors, *M*5 to *M*12 are placed inside the output transformer, whereas the driver stage, RF chokes, and input-matching components are outside. Any of the circuit components, interconnects, and dummy-metal patterns are located at least 150 μm away from transformer metal lines, except the RF feeding-lines shown in Fig. 2, and *C*5, *C*6, *M*7, *M*8, *M*11, and *M*12 which are directly connected to the transformer. This layout helps to reduce the power loss caused by magnetic-flux leakage, whereas it consumes more chip area.

B. Circuit Simulation

It is important to accurately predict the characteristics and performance of the output transformer because it is the most crucial component in this circuit: transforming impedance, converting differential signals to single-ended, combining output power, and having relation with operating frequency. In this work, therefore, quasi-3D electro-magnetic (EM) simulation was performed using Ansoft Designer to characterize the transformer and its layout effect. Metal patterns, such as pads and interconnects, were also considered in the EM simulation when adjacent to the transformer. Finally, the overall circuit was designed and simulated using Agilent ADS with device models and multi-port *S*-parameter data describing the layout effects given by the EM simulator.

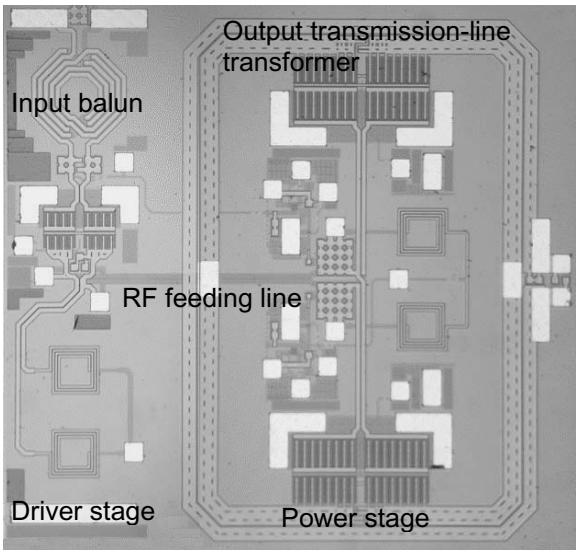

Fig. 2. Microphotograph of the power amplifier fabricated in a 0.25-μm CMOS technology.

TABLE I
SUMMARY OF THE PERFORMANCE OF THE POWER AMPLIFIER FOR A MOBILE RFID READER

Frequency (MHz)	860	920	960
VDD / Vbias (V)	2.5 / 0.5		
DC current (mA)	92		
Small-Signal Gain (dB)	15	14.5	14
Peak Gain (dB)	16.8	16	15.2
P1dB (dBm)	25.5	27	27
PAE @ P1dB (%)	20	28	28
DC power @ P1dB (W)	1.65	1.8	1.8

IV. EXPERIMENTAL RESULTS

A 27-dBm 900-MHz linear power amplifier was implemented in a 0.25-μm CMOS technology. A printed circuit board (PCB) for testing the power amplifier was also fabricated. The chip is glued to a grounded heat sink of the PCB using an electrically and thermally conductive adhesive. Ground pads of the chip are wire-bonded to the heat sink, while signal pads to the gold-plated metal lines on the PCB. Input and output pads are wire-bonded to 50-Ω microstrip lines.

The measured output power, gain, and PAE are shown in Fig. 3. The frequency of the input signal is 920 MHz.[1]

[1] UHF band for RFID is from 902 MHz to 928 MHz in North America, 908.5 MHz to 914 MHz in Korea, 865 MHz to 868 MHz in Europe, and 952 MHz to 954 MHz in Japan.

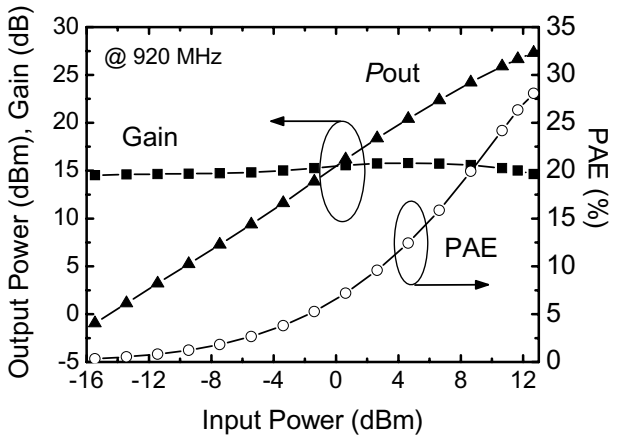

Fig. 3. Output power, gain, and PAE of the designed power amplifier when measured at 920 MHz.

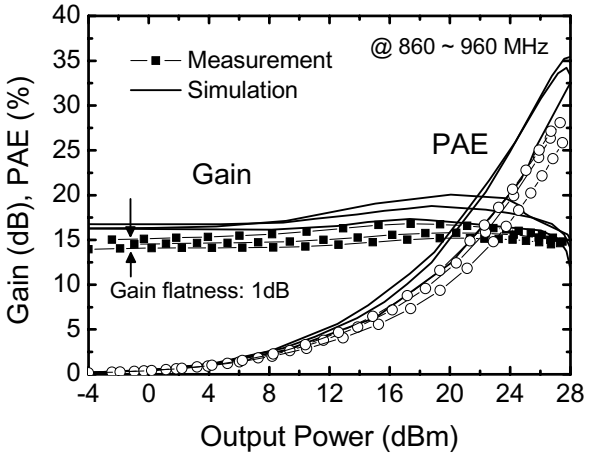

Fig. 4. Measured and simulated power gain and PAE at the frequencies of 860 MHz, 920 MHz, and 960 MHz.

With a supply voltage of 2.5 V and gate bias voltages of 0.5 V, the amplifier consumes DC current of 92 mA and provides small-signal gain of 14.5 dB and output P1dB of 27 dBm. PAE of 28 % is achieved at the P1dB. An input balun transformer is appended to the circuit to generate differential input signals for the power amplifier. The measured data include the gain and power loss caused by the on-chip balun and bonding-wires. Fig. 4 shows the measured and simulated gain and PAE at the frequencies of 860 MHz, 920 MHz, and 960 MHz.[1] Small-signal gain flatness is 1 dB over the full UHF band of RFID. The simulated results are illustrated as dashed lines in Fig. 4. The difference between the measured and the simulated gain is 2 dB, which appears to result from insufficient

TABLE II
SUMMARY OF THE PERFORMANCES OF CMOS LINEAR POWER AMPLIFIERS

Freq. (GHz)	VDD (V)	Num. of Stages	Gain (dB)	P1dB (dBm)	PAE @ P1dB (%)	Matching Components	CMOS Process (μm)	Ref.
5.25	1.8	3	21	14.5	13	Fully-integrated	0.18	[6]
5.2	1.8	2	15.1	15.4	22	Fully-integrated	0.18	[7]
5	1.8	-	7.1	19.2	17.5	Fully-integrated	0.18	[8]
1.9	2.5	2	24.6	22	24	Off-chip	0.35	[9]
0.9	-	1	5	17.4	26	Fully-integrated	0.6	[10]
0.92	2.5	2	14.5	27	28	Fully-integrated	0.25	This work

accuracy of RF power transistor models. The measured performance is summarized in Table I.

V. CONCLUSION

A fully-integrated 900-MHz linear power amplifier has been fabricated for mobile RFID reader applications in a 0.25-μm CMOS process. The designed amplifier consists of two stages with input and output transformers integrated. With a 2.5-V supply voltage, the amplifier provides power gain of 14.5 dB and P1dB of 27 dBm, when measured at 920 MHz without any external components. PAE of 28 % is achieved at the P1dB, which is a good result compared with those of the previously reported CMOS linear power amplifiers [6]–[10]. The previous works are summarized in Table II.

ACKNOWLEDGEMENT

This research was supported by University IT Research Center Project and Samsung Electro-Mechanics Co.

REFERENCES

[1] S. Sandoval-Reyes and J. L. Soberanes Perez., "Mobile RFID reader with database wireless synchronization," *Int. Conf. on Electrical and Electronics Engineering,* pp. 5–8, September 2005.

[2] K. Penttila, N. Pere, M. Sioni, L. Sydanheimo, and M. Kivikoski, "Use and interface definition of mobile RFID reader integrated in a smart phone," in *Proc. of Int. Symp. on Custormer Electronics*, pp. 353–358, June 2005.

[3] J. Zhang, Z. Xie, S. Lai, and Z. Wu, "A design of RF receiving circuit of RFID reader," in *Proc. of Int. Conf. on Microwave and Millimeter Wave Technology*, pp. 406–409, August 2004.

[4] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE Jour. of Solid-State Circuits*, vol. 37, no. 3, pp. 371–383, March 2002.

[5] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, "A 1.4 GHz – 2 GHz wideband CMOS class-E power amplifier delivering 23 dBm peak with 67 % PAE," *IEEE Radio Frequency Integrated Circuits (RFIC) Symp., Dig. of Papers*, pp. 425–428, June 2005.

[6] Y. Eo and K. Lee, "A fully integrated 24-dBm CMOS power amplifier for 802.11a WLAN applications," *IEEE Microwave Wireless Compon. Lett.*, vol. 14, no. 11, pp. 504–506, November 2004.

[7] W. Zhang, E-S. Khoo, and T. Tear, "A low voltage fully-integrated 0.18um CMOS power amplifier for 5 GHz WLAN," in *Proc. of Eur. Solid-State Circuits Conf.*, pp. 215–218, September 2002.

[8] Y. Eo and K. Lee, "High efficiency 5 GHz CMOS power amplifier with adaptive bias control circuit," *IEEE RFIC Symp., Dig. of Papers*, pp. 575–578, June 2004.

[9] A. Giry, J-M. Fournier, and M. Pons, "A 1.9 GHz low voltage CMOS power amplifier for medium power RF applications," *IEEE RFIC Symp. Dig. of Papers*, pp. 121–124, June 2000.

[10] B. Baliweber, R. Gupta, and D. J. Allstot, "Fully-integrated CMOS RF amplifier," in *Proc. IEEE Int. Solid-State Circuits Conf.*, pp. 72–73, February 1999.