A Fully Integrated Triple-Band CMOS Class-E Power Amplifier With a Power Cell Resizing Technique and a Multi-Tap Transformer

Woo-Young Kim, Hyuk Su Son, Joon Hyung Kim, Joo Young Jang, *Student Member, IEEE*, Inn Yeal Oh, *Member, IEEE*, and Chul Soon Park, *Senior Member, IEEE*

***Abstract*—This letter presents a fully integrated triple-band CMOS class-E power amplifier (PA) for the 0.8/1.9/2.4 GHz frequencies. The operating frequency band is tuned by a power cell resizing technique and by changing the supply bias position with a multi-tap transformer for the required capacitance and inductance values for optimum class-E operation. The PA achieves output powers of 28/29.6/26.5 dBm and power-added efficiency of 40/45/37% at each frequency band. The PA is implemented in a 0.18 μm CMOS process without multiple transformers or input/output matching networks. The total chip size is 1.5×1.5 mm^2.**

***Index Terms*—Class-E, CMOS, multi-band, power amplifier (PA).**

I. Introduction

RECENTLY, the advent of a new generation of mobile wireless communications demands the facilitation and guarantee of backward compatibility. Therefore, multi-band system implementation is required. In the PA design, to support multi-band operation, many approaches have been reported, including a varactor based tunable matching network [1], MEMS switches for multiple output matching networks [2], and parallel input/output matching networks [3]–[5]. However, these techniques incur a significant penalty of the chip area, cost, and hardware complexity. Also, many efforts related to a system on a chip (SOC) on a CMOS process have been reported. For a true CMOS SOC system, the CMOS PA is a challenging issue due to the drawbacks of the low breakdown voltage of CMOS devices, and a lossy substrate compared to compound semiconductors devices. To solve the breakdown voltage problem of the CMOS device, a distributed active transformer (DAT) [6] was reported. In addition, double primary sides of an on-chip transformer have been used to reduce the resistance of the transformer [7].

In this letter, we demonstrate a fully integrated triple-band : 0.8/1.9/2.4 GHz such as low-band (LB), mid-band (MB) and high-band (HB) class-E PA with on-chip input and output matching networks in a 0.18 μm CMOS process. Multi-band operation can be realized by a power cell resizing technique and by changing the supply bias position with a multi-tap transformer for tunable capacitance and inductance values.

Manuscript received July 26, 2013; revised September 11, 2013; accepted September 19, 2013. Date of publication October 07, 2013; date of current version November 28, 2013. This work was supported by the National Research Foundation of KoreaGrant funded by the Korean Government (220-2011-1-D00082), (2012-0000703), and by the MSIP (Ministry of Science, ICT&Future Planning), Korea in the ICT R&D Program 2013.

The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-732, Korea. (e-mail: wykim@kaist.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2013.2283874

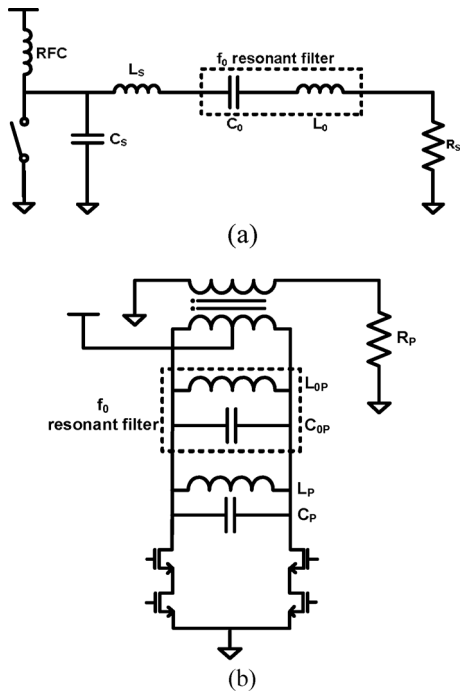

Fig. 1. (a) Simplified class-E output matching network circuit, and (b) differential class-E output matching circuit with a parallel resonant circuit.

II. A Triple-Band Class-E PA Design

A. Output Matching Principle for Class-E Operation

Fig. 1(a) shows a simplified class-E output matching network circuit. Here, C_S and L_S are derived from a zero-voltage switching (ZVS) condition and L_0 and C_0 are determined by the loaded quality factor Q_L [8]. A single-ended class-E PA can be transformed into a differential class-E PA, as shown in Fig. 1(b). The operation of this transformation was analyzed and output network design equations were derived in earlier work [9]. The series resonant filter (L_0, C_0) and series *RL* circuit (R_S, L_S) can be transformed into a parallel resonant filter (L_{0P}, C_{0P}) and a parallel *RL* circuit (R_P, L_P) in differential class-E design, respectively. The transformation equations are shown in (1) and (2), respectively

$$L_{0P} = \frac{R_P}{\omega Q_L}, C_{0P} = \frac{Q_L}{\omega R_P} \tag{1}$$

$$L_P = 0.8677\frac{R_P}{\omega}, C_S = 0.4275\frac{1}{\omega R_P}. \tag{2}$$

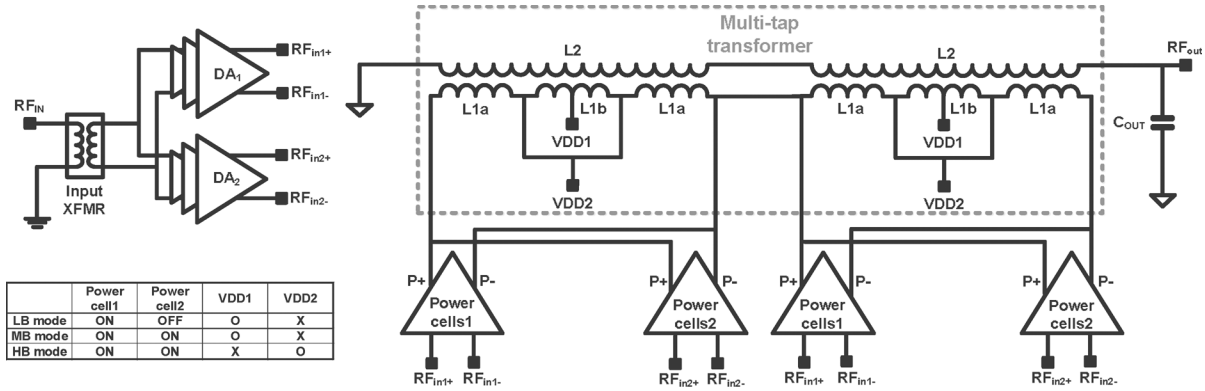

Fig. 2. Schematic of the proposed triple-band CMOS class-E PA.

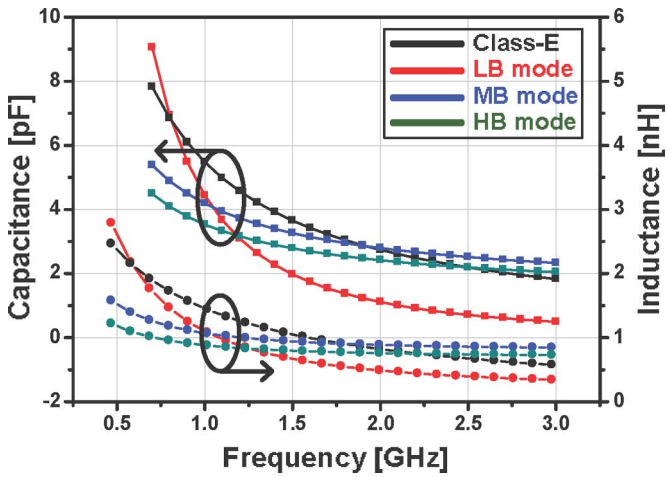

Fig. 3. Design parameters as a function of the frequency.

TABLE I
DESIGN PARAMETERS FOR CLASS-E OPERATION

	Class-E		LB mode		MB mode		HB mode	
	L_T [nH]	C_T [pF]	L_T [nH]	C_T [pF]	L_T [nH]	C_T [pF]	L_T [nH]	C_T [pF]
0.8GHz	2.1	6.8	2.1	6.9	1.4	4.8	1.1	4.1
1.9GHz	0.9	2.8	0.5	1.2	0.9	2.8	0.8	2.5
2.4GHz	0.7	2.2	0.4	0.7	0.8	2.5	0.7	2.2

Moreover, L_P and C_S can be merged into the parallel resonant circuit components L_{0P} and C_{0P}, respectively. That is, the design parameters can be simplified to only two variables: L_T and C_T.

The L_T and C_T variables can be expressed as follows:

$$L_T = L_{0P}//L_P, C_T = C_{0P}//C_P. \tag{3}$$

B. Operation Principle of Triple-Band PA

We proposed a triple-band class-E PA with a power cell resizing technique and a multi-tap transformer without multiple matching networks, as shown in Fig. 2. There are two differential power amplifiers and a 1:1 transmission line transformer (TLT) for voltage combining without CMOS device breakdown limitation. In a differential amplifier, there are two power cells and a multi-tap transformer for the tunable capacitance and inductance values, as shown in (4) and (5). The output capacitance of the power cells is a combination of the transistor's

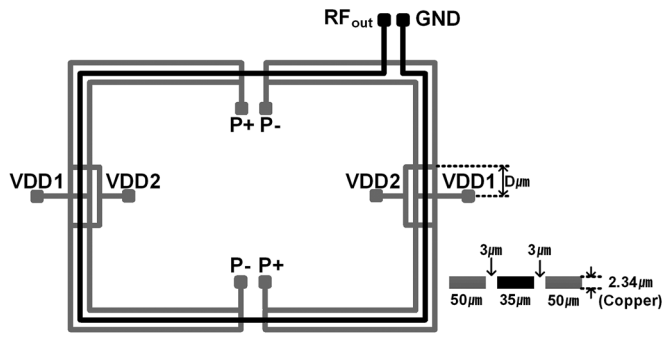

Fig. 4. Block diagram of the proposed multi-tap transformer.

gate-drain capacitance (C_{GD}) and the drain-source capacitance (C_{DS}); this, value can be controlled by turning ON and OFF the common-gate stage bias of the cascode topology of the power cells, and the inductance value of the output matching network can be controlled by the parasitic inductance of the power cells and by changing primary side supply bias position of the transformer. The LB, MB, and HB modes condition are summarized, in Fig. 3

$$C_T = C_{GD\_Power\,cell1} + C_{DS\_Power\,cell1} + C_{GD\_Power\,cell2} + C_{DS\_Power\,cell2} \tag{4}$$

$$L_T = 2L_{1a} + L_{1b}. \tag{5}$$

From (1)–(5), L_T and C_T values for optimum class-E operation can be derived for each frequency 0.8/1.9/2.4 GHz as summarized in Table I.

C. Multi-Tap Transformer

The proposed multi-tap transformer for a triple-band PA is shown in Fig. 4. It employs two kinds of taps for the supply bias connection, a center tap for VDD1 with the other taps for VDD2. When one tap is connected to the supply node, the other is in an open state to eliminate signal leakage. The primary part is split into two lines to reduce the parasitic resistances and the insertion loss of 1.1/1.3/1.5 dB at 0.8/1.9/2.4 GHz, respectively, with a 1:1 transformation ratio.

In this study, we proposed that primary side inductance can be controlled by changing the bias position of the transformer. The inductance value is a function of the distance from the center position. We can choose a distance value of 300 μm for a value

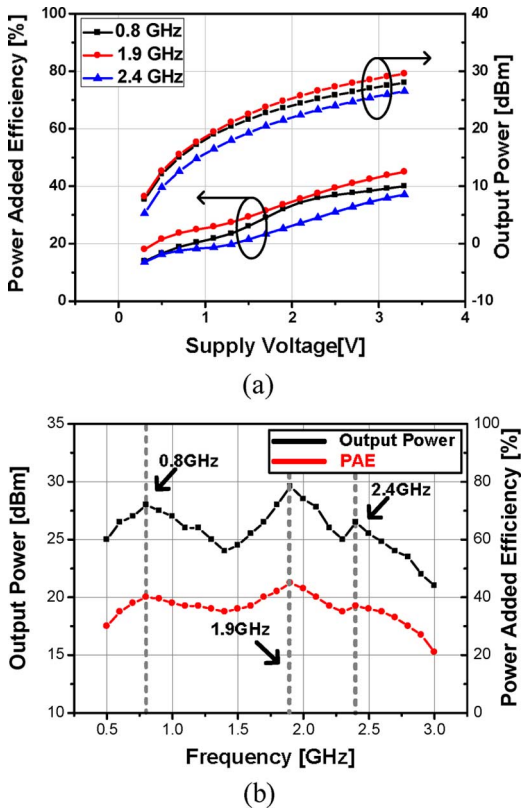

Fig. 5. (a) Measured output power and PAE versus the supply voltage. (b) Measured output power and PAE the versus frequency.

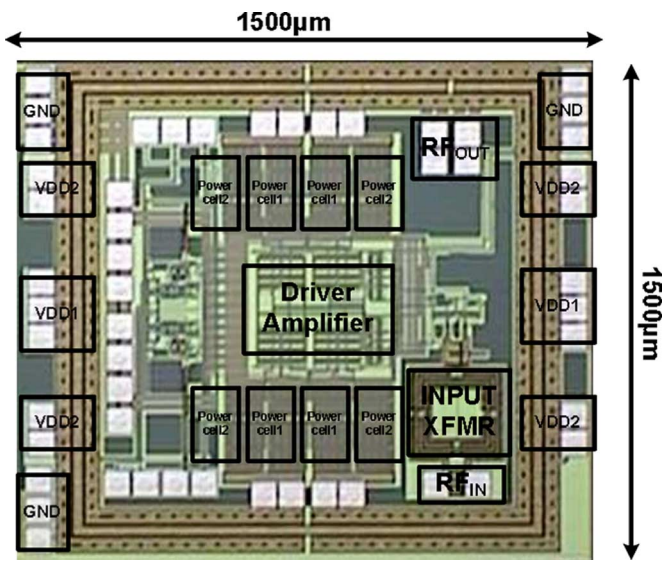

Fig. 6. Chip photograph of the implemented power amplifier.

of 0.7 nH to operate the 2.4 GHz HB mode with a coupling coefficient of 0.75, as shown in the simulation result.

III. Measurement Results

The measurement results are presented in Figs. 5 and 6 shows a chip photograph of the fully integrated triple-band PA fabricated in a 0.18 μm CMOS process. The peak output power and PAE of the PA for each frequency band (0.8/1.9/2.4 GHz) are 28/29.6/26.5 dBm and 40/45/37% with RF input power of 0 dBm under 3.3 V supply voltage with 0.8 V common source bias voltage and 3.3 V common gate bias voltage, respectively, in the CW test including on-chip input and output balun loss and driver stage power consumption. The on-chip input balun loss is 0.8/1.1/1.2 dB for LB, MB and HB modes. The driver amplifier is composed of three-stage and 30 dB gain with 50 mW power consumption. The chip size is 1.5×1.5 mm^2 with the input and output matching networks on-chip without external components. As shown in Table II, this PA performance shows comparable results [10], [11].

TABLE II
Comparison Table of the Performance

Ref.	This Work	[10]	[11]
Frequency[GHz]	0.8/1.9/2.4	1.9/2.3/2.6/3.5	0.45~0.73
Pout[dBm]	28/29.6/26.5	24/23/23/20	20
PAE[%]	40/45/37	48/44/40/35	46
External Components	NO	YES	YES
Process	CMOS 0.18-μm	CMOS 0.18-μm	CMOS 0.18-μm
Size	1.5x1.5mm^2	0.9x1.8mm^2	0.7x0.8mm^2

IV. Conclusion

We demonstrated a fully integrated triple-band CMOS class-E PA with a single transformer. The triple-band modes can be controlled by means of a power cell resizing technique and a multi-tap transformer. The proposed technique can be applied to a reconfigurable wireless communication system such as WCDMA and LTE with a hybrid-EER and polar transmitter.

References

[1] W. C. E. *et al.*, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2166–2176, Sep. 2006.

[2] A. Fukuda, H. Okazaki, and S. Narahashi, "A novel reconfigurable quad-band power amplifier with reconfigurable biasing network and LTCC substrates," in *IEEE MTT-S Int. Dig.*, Jun. 2008, pp. 867–970.

[3] C. Zhang and A. E. Fathy, "A novel reconfigurable power amplifier structure for multi-band and multi-mode portable wireless applications using a reconfigurable die and switchable output matching network," in *IEEE MTT-S Int. Dig.*, Jun. 2009, pp. 913–916.

[4] K. Y. Kim, J. H. Kim, Y. S. Noh, and C. S. Park, "Cellular/PCS dual-band MMIC power amplifier of a newly devised single-input single-chain network," in *Proc. IEEE Gallium Arsenide Integr. Circuit Symp.*, Feb. 2003, pp. 131–134.

[5] H. S. Son, W. Y. Kim, J. Y. Jang, H. J. Lee, I. Y. Oh, and C. S. Park, "A fully integrated CMOS class-E power amplifier for reconfigurable transmitters with WCDMA/WiMAX applications," in *Proc. IEEE 26th Int. Conf. VLSI Design & 12th Int. Conf. Embedded Syst.*, 2013, pp. 169–172.

[6] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active transformer architecture," *J. Solid-State Circuits*, vol. 37, no. 3, pp. 371–383, Mar. 2002.

[7] S. Shim and S. Hong, "A 1-W, 800-MHz, switch-mode CMOS RF power amplifier using an on-chip transformer with double primary sides," in *Proc. IEEE Radio Wireless Symp.*, Feb. 2009, pp. 538–541.

[8] F. H. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, no. 12, pp. 725–735, Dec. 1977.

[9] D. H. Lee *et al.*, "A load-shared CMOS power amplifier with efficiency boosting at low power mode for polar transmitters," *IEEE Microw. Theory Tech.*, vol. 56, no. 7, pp. 1565–1574, Jul. 2009.

[10] K. Y. Kim, W. Y. Kim, H. S. Son, I. Y. Oh, and C. S. Park, "A reconfigurable quad-band CMOS class-E power amplifier for mobile and wireless communication," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 5, pp. 380–382, Jul. 2011.

[11] J. Hur, O. Lee, C. H. Lee, K. Lim, and J. Laskar, "A multi-level and multi-band class-D CMOS power amplifier for LINC system in the cognitive radio application," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 6, pp. 352–354, Jun. 2010.