

Integrated Inverse Class-F Silicon Power Amplifiers for High Power Efficiency at Microwave and mm-Wave

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Abstract—This paper presents two 2-stage inverse class-F power amplifiers (PAs) at 24 GHz and 38 GHz, integrated in 0.13 μm SiGe BiCMOS technology. The PAs are composed of an inverse class-F output stage proceeded by a class-AB driving amplifier. An inter-stage matching network between the driver and output stage delivers an optimal inter-stage power to the output stage with a maximum PAE in the driver amplifier. The output stage's load network based on multi-resonance LC resonators terminates harmonic impedance explicitly up to the third of the fundamental signal. By leveraging a native low capacitive reactance, the class-F⁻¹ load network shapes a quasi-rectangular current waveform that effectively contains up to the fifth harmonic spectral component. A high impedance control is limited up to the second harmonic, shaping a half-sinusoid voltage peaking induced by DC, fundamental, and the second harmonic voltage spectra. The 24 GHz PA achieves 50% peak PAE, 16 dBm OP_{-1dB}, 18 dBm P_{sat}, and 19 dB saturated power gain with 2.3 V supply voltage at 24 GHz. The 24 GHz PA can maintain >45% PAE over 23.5–25.5 GHz and 1.5–2.4 V supply voltage range, manifesting a PAE robustness to the frequency and supply variations. For 38 GHz PA, measurements show 38.5% peak PAE, 15 dBm OP_{-1dB}, 17 dBm P_{sat} with 15 dB of saturated power gain at the OP_{-1dB} point when 2.4 V supply voltage is applied. The 38 GHz PA can sustain >35% PAE over 36–39 GHz and 1.5–2.5 V supply variation. The PAs also are tested under the input of band-limited signals modulated by various modulation schemes including 8-PSK, QAM, 16-QAM, 64-QAM, and 128-QAM, and test results are presented in this paper. The chip size is 0.95 \times 0.6 mm² for 24 GHz PA and 0.93 \times 0.55 mm² for 38 GHz PA, including all pads.

Index Terms—5G, 24 GHz, 28 GHz, 38 GHz, class-F, class-F⁻¹, harmonic tuned power amplifier, inverse class F, SiGe PA.

I. INTRODUCTION

HARMONICALLY tuned amplifier topologies, classified as class-F and inverse class-F (F⁻¹), are widely investigated to achieve a high power efficiency in high frequency power amplifiers (PAs) [1]–[6]. In ideal class-F PAs, by

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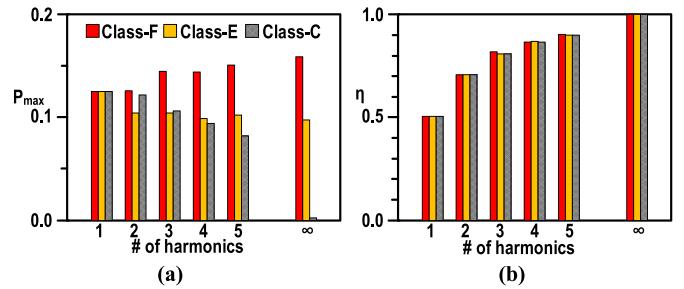


Fig. 1. Performance of ideal PAs with various number of harmonics [3]: (a) output power capability (maximum output power normalized by the power by peak voltage and current) at the PA output and (b) drain (or collector) efficiency.

terminating all odd and even harmonic impedances to be open-circuit and short-circuit, respectively, the PAs can shape a rectangular voltage and half-sinusoid current waveform at the collector (or drain) output. The circuit duality allows interchanging of the even and odd harmonics impedances, inverting the collector voltage and current waveform in ideal class-F⁻¹ PAs. Both architectures enable non-overlapped zero-voltage or zero-current switching. This completely eliminates the spectral power of any harmonic components, and thus leads to 100% power conversion efficiency from a DC supply to a fundamental radio frequency (RF) signal by a generator [2]. It is well known that the harmonically tuned PAs provide near optimum solution for a maximum output power, P_{max} in Fig. 1(a), while achieving equivalent or better drain efficiency, η in Fig. 1(b), by controlling a number of harmonics [3]. This implies that the class-F or class-F⁻¹ PAs can achieve better power gain and thus higher power-added-efficiency (PAE) than the other types of PAs in Fig. 1.

At high frequencies, the authentic circuit impedance control for the class-F or class-F⁻¹ waveform shaping is often opted for up to the third harmonic of a fundamental frequency because higher than the third-order harmonic impedance control may not be easy, nor be practical in terms of size and loss [1]–[3]. Prior state-of-the-art class-F or class-F⁻¹ PAs with the bi-harmonic (second and third harmonic) impedance tuning exhibit outstanding PAE over 70% [7]–[11]. However, major design efforts have been focused on discrete PAs at RF by leveraging a packaged high-power transistor such as LDMOS FET or GaN HEMT [10], [11], or GaAs-based MMIC implementation at microwave frequencies [7]. So far, little research effort has been exerted for realizing harmonically tuned integrated PAs in the silicon process. This is partly because, for highly efficient integrated silicon PAs at

RF, the class-F or class-F⁻¹ topology may not be an optimal choice over other switching-mode PAs due to the difficulty in realizing a high-Q LC resonance load network; a high passive component loss will sacrifice the power efficiency substantially and PAE improvement by the class-F or class-F⁻¹ topology may not be prominent at RF.

However, the passive component loss, mainly inductor loss, becomes smaller at microwave and higher frequencies thanks to the scale down of the passive components size. This provides a good opportunity of implementing low-loss and compact high-Q LC resonators for an optimal harmonic impedance modulation for the integrated class-F or class-F⁻¹ PAs. Indeed, recent on-chip class-F or class-F⁻¹ PAs reported in [12]–[14] by the authors have increased PAE of silicon PAs substantially at the crossroad of microwave and mm-wave regimes. The class-F⁻¹ technique is particularly more attractive and effective than the class-F technique in achieving a high PAE at microwave and mm-wave bands. This is because developing a high impedance at a second-harmonic band will be much more robust to parasitic effects and less vulnerable to passive components Qs than at a third-harmonic band at such high frequencies.

In this work, two class-F⁻¹ PAs employing a multi-resonance LC harmonic filter are designed at 24 GHz and 38 GHz in a SiGe BiCMOS technology to explore potentials and limitations of the harmonic tuning technique in achieving a high PAE at microwave and mm-Wave bands. The PAs produce 50–70 mW output power on a 50- Ω load at saturation, and achieve 50% and close to 40% PAEs at 24 GHz and 38 GHz, respectively, some of the highest PAEs reported so far in integrated PAs in both silicon and III-V technologies. The saturated output power has been defined optimally and maximally to the extent that a power transistor can sustain the output power without suffering breakdown, and at the same time, maintain a high f_T (>180 GHz) in the given 0.13 μm SiGe BiCMOS technology. Namely, the P_{sat} is the outcome of a compromise between the output power and device speed, which is an ingrained tradeoff in silicon technologies. Larger output power could be produced by aggregating the output power with configuring a PA array utilizing the proposed designs as a unit PA cell.

In this paper, Section II discusses details on the major PAE limiting factors in class-F⁻¹ PAs. LC resonators can generate a frequency-dependent impedance, and thus they can be used for modulating the PA load impedance dependent on harmonic frequencies. Section III provides an original configuration of cascading multiple LC resonators in parallel and series for the required class-F⁻¹ impedance modulation at harmonic bands. The design details on the 2-stage PAs, a cascade of a class-AB driver and a class-F⁻¹ output stage, are described in section IV. The small-signal and large-signal measurement results, including modulation signal tests, are provided in Section V, and finally the paper is concluded in Section VI.

II. INVERSE CLASS-F POWER EFFICIENCY LIMITING FACTORS

Let i_{fund} and v_{fund} be peak magnitudes of fundamental current and voltage components at a generator output, then

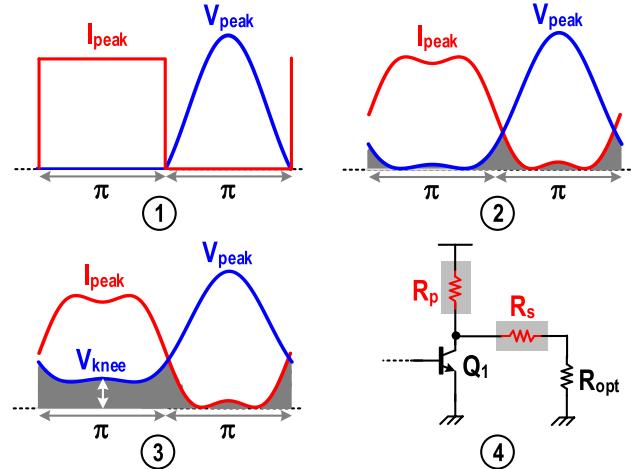


Fig. 2. PAE limiting factors in the inverse class-F PAs: ① Ideal non-overlapped inverse class-F V/I waveforms. ② Finite number of harmonic impedance control. ③ Finite knee voltage in the power transistor. ④ Finite resistive losses from parallel resonance load (R_p) and series resonance load (R_s) at f_0 .

collector (or drain) efficiency will be

$$\eta_c = \frac{1}{2} \left(\frac{i_{\text{fund}}}{I_{DC}} \right) \left(\frac{v_{\text{fund}}}{V_{DC}} \right). \quad (1)$$

V_{DC} and I_{DC} are DC voltage and current, respectively. In ideal non-overlapped rectangular current and half-sinusoidal voltage waveforms, shown in Fig. 2①, $i_{\text{fund}}/I_{DC} = 4/\pi$ and $v_{\text{fund}}/V_{DC} = \pi/2$, resulting in 100% η_c .

A. Finite Number of Harmonics Control

In reality, only finite number of harmonics will be present at the generator load due to the band limiting nature of a passive load, causing nontrivial collector voltage and current overlap in Fig. 2②, where the generator dissipates an active power. When restricting the harmonics control up to the third of a fundamental frequency, the following class-F⁻¹ collector voltage and current polynomials have been suggested for the maximum efficiency [1]:

$$v_{CE}(\theta) = V_{DC} \left(1 - \sqrt{2} \cos \theta + \frac{1}{2} \cos 2\theta \right) \quad (2)$$

and

$$i_{CE}(\theta) = I_{DC} \left(1 - \frac{2}{\sqrt{3}} \cos \theta + \frac{1}{3\sqrt{3}} \cos 3\theta \right) \quad (3)$$

which results in

$$\eta_{c,\max} = \frac{1}{2} \left(\frac{i_{\text{fund}}}{I_{DC}} \right) \left(\frac{v_{\text{fund}}}{V_{DC}} \right) = \frac{1}{2} \times \frac{2}{\sqrt{3}} \times \sqrt{2} = 0.816. \quad (4)$$

B. Finite Knee Voltage, V_{knee}

The efficiency will be decreased further because of the finite knee voltage of a power transistor (Q1), V_{knee} in Fig. 2③. To investigate the V_{knee} effect on the efficiency, let's redefine the collector voltage as

$$v_{CE}(\theta) = V_{DC} - v_{\text{fund}} \cos \theta + v_{2\text{nd}} \cos 2\theta, \quad (5)$$

where v_{2nd} is peak magnitude of the second harmonic component of the collector voltage waveform. In the half-sinusoid voltage, the minimum of (5) needs to be V_{knee} and at the minimum points should be flat for a maximum flatness during the half cycle, imposing the signal condition of $v_{CE,min} = v_{CE}(\theta_o) = V_{knee}$ and $\partial v_{CE}(\theta)/\partial\theta = 0$ at $\theta = \theta_o$. θ_o is the angle where the collector voltage reaches its minimum value. This enforces the following relationships:

$$V_{DC} - v_{fund}\cos\theta_o + v_{2nd}\cos 2\theta_o = V_{knee} \quad (6)$$

and

$$\begin{aligned} \frac{\partial v_{CE}(\theta)}{\partial\theta} &= 0 \text{ at } \theta = \theta_o (-\pi \leq \theta_o \leq \pi) \\ \Rightarrow &\begin{cases} \cos\theta_o = \frac{v_{fund}}{4v_{2nd}}, & \text{if } \frac{v_{2nd}}{v_{fund}} > \frac{1}{4} \\ \theta_o = 0, & \text{if } \frac{v_{2nd}}{v_{fund}} < \frac{1}{4}. \end{cases} \end{aligned} \quad (7)$$

Plugging (7) into (6) gives

$$\begin{aligned} \frac{v_{fund}}{V_{DC}} &= \begin{cases} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \left(\frac{v_{2nd}}{v_{fund}} + \frac{v_{fund}}{8v_{2nd}}\right)^{-1}, & \text{if } \frac{v_{2nd}}{v_{fund}} > \frac{1}{4} \\ \left(1 - \frac{V_{knee}}{V_{DC}}\right) \left(1 - \frac{v_{2nd}}{v_{fund}}\right)^{-1}, & \text{if } \frac{v_{2nd}}{v_{fund}} < \frac{1}{4}. \end{cases} \end{aligned} \quad (8)$$

Consequently, η_c will be

$$\begin{aligned} \eta_c &= \frac{1}{2} \times \frac{2}{\sqrt{3}} \\ &\times \begin{cases} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \left(\frac{v_{2nd}}{v_{fund}} + \frac{v_{fund}}{8v_{2nd}}\right)^{-1}, & \text{if } \frac{v_{2nd}}{v_{fund}} > \frac{1}{4} \\ \left(1 - \frac{V_{knee}}{V_{DC}}\right) \left(1 - \frac{v_{2nd}}{v_{fund}}\right)^{-1}, & \text{if } \frac{v_{2nd}}{v_{fund}} < \frac{1}{4}. \end{cases} \end{aligned} \quad (9)$$

In (9), the maximum efficiency happens when $v_{2nd}/v_{fund} = 1/2\sqrt{2} \approx 0.354$ and is given by

$$\eta_{c,max} = 0.816 \times \left(1 - \frac{V_{knee}}{V_{DC}}\right). \quad (10)$$

The optimal collector voltage waveform including the knee voltage will be

$$\begin{aligned} v_{CE}(\theta) &= V_{DC} \left\{ 1 - \sqrt{2} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \cos\theta \right. \\ &\quad \left. + \frac{1}{2} \left(1 - \frac{V_{knee}}{V_{DC}}\right) \cos 2\theta \right\}. \end{aligned} \quad (11)$$

Apparently, when $V_{knee} = 0$ (11) will be reduced to (2). V_{DC} depends on output power and is limited strictly by a device breakdown voltage (V_{BK}) which is relatively low and traded with speed in the silicon process. Thus, the efficiency could be restricted severely by the knee voltage in high frequency silicon power amplifiers, particularly when the output power level is not high. For instance, if $V_{DC} = 2.3$ V and $V_{knee} = 0.4$ V, then theoretical maximum collector efficiency would be limited to around 67.4%.

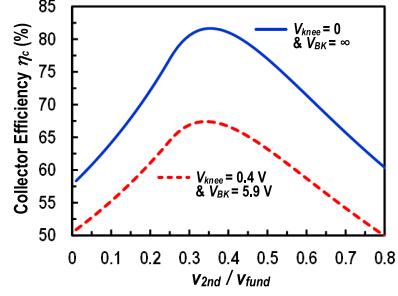


Fig. 3. Collector efficiency (η_c) versus v_{2nd}/v_{fund} .

C. Transistor Breakdown Voltage, V_{BK}

More complete expression on the collector efficiency can be derived when the maximum output signal is bounded by a breakdown voltage as following. In (5), the maximum happens when $\theta = \pm\pi$ but is capped to V_{BK} , conditioning

$$v_{CE,max} = V_{DC} + v_{fund} + v_{2nd} = V_{BK} \quad (12)$$

which can be processed further as

$$\begin{aligned} V_{DC} + v_{fund} + v_{2nd} - V_{knee} &= V_{BK} - V_{knee} \\ \rightarrow 1 - \frac{V_{knee}}{V_{DC}} &= \frac{\frac{V_{BK}}{V_{DC}} \cdot \left(1 - \frac{V_{knee}}{V_{BK}}\right)}{1 + \left(1 + \frac{v_{2nd}}{v_{fund}}\right) \left(\frac{\frac{v_{fund}}{V_{DC}}}{1 - \frac{V_{knee}}{V_{DC}}}\right)}. \end{aligned} \quad (13)$$

Since at the maximum η_c , $v_{2nd}/v_{fund} = 1/2\sqrt{2}$ and $v_{fund}/V_{DC} = \sqrt{2} \cdot (1 - V_{knee}/V_{DC})$, (13) is simplified to

$$\begin{aligned} 1 - \frac{V_{knee}}{V_{DC}} &= \frac{1}{1.5 + \sqrt{2}} \times \frac{V_{BK}}{V_{DC}} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right) \\ &\cong 0.343 \times \frac{V_{BK}}{V_{DC}} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right). \end{aligned} \quad (14)$$

The substitution of (14) into (10) leads to

$$\eta_{c,max} = 0.28 \times \frac{V_{BK}}{V_{DC}} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right). \quad (15)$$

In continuing the previous example, when $V_{BK} = 5.9$ V, $V_{DC} = 2.3$ V, and $V_{knee} = 0.4$ V, $\eta_{c,max}$ becomes 67%, a slight decrease compared with the unbounded case. Fig. 3 shows η_c versus v_{2nd}/v_{fund} in two cases: a solid line for the ideal case ($V_{knee} = 0$ and $V_{BK} = \infty$) and a dotted line for a realistic case in this work ($V_{knee} = 0.4$ V and $V_{BK} = 5.9$ V). In this example, the peak voltage magnitude, V_{peak} in Fig. 2, is ~ 5.9 V from (11).

D. Resistive Losses from Passive Load Network

So far, it has been assumed that the class-F⁻¹ passive load network is ideal with no loss from the load. This could be a valid assumption in discrete PA designs on a printed-circuit board, where extremely high Q off-the-shelf Ls and Cs would be readily available. However, in integrated PAs, particularly in the silicon process, the passive load suffers from substantial loss because of a limited Q from the integrated passive components. In Fig. 2④, R_p and R_s represent equivalent

loss resistances at a fundamental frequency from the parallel and series loads, respectively. R_{opt} is an optimum PA load. The resistor network divides collector current and voltage, dissipates DC power, and thus causes RF fundamental power loss (P_{loss}) which can be expressed as

$$P_{loss} = \underbrace{\left(\frac{R_p}{R_p + R_s + R_{opt}} \right)}_{\text{current loss}} \cdot \underbrace{\frac{R_{opt}}{R_s + R_{opt}}}_{\text{voltage loss}}. \quad (16)$$

P_{loss} is factored out by the current and voltage losses. When including this power loss, the peak collector efficiency in (15) will decrease to $\eta_{c,max} \times P_{loss}$.

In fact, the loss factors in (16) disclose a tradeoff in choosing R_{opt} to desensitize the impact of the passive components losses on the efficiency: namely, to minimize the current loss smaller R_{opt} is desirable, whereas larger R_{opt} is preferable in order to desensitize the effect of R_s on the voltage loss. The sensitivity of $\eta_{c,max}$ on R_p can be evaluated systematically by a sensitivity function given as

$$S_{R_p}^{\eta_{c,max}} = \frac{R_p}{\eta_{c,max}} \times \frac{\partial \eta_{c,max}}{\partial R_p} = \left(1 + \frac{R_p}{R_s + R_{opt}} \right)^{-1}. \quad (17)$$

Similarly, the sensitivity of $\eta_{c,max}$ on R_s can be appreciated by

$$S_{R_s}^{\eta_{c,max}} = \frac{R_s}{\eta_{c,max}} \times \frac{\partial \eta_{c,max}}{\partial R_s} \approx - \left(1 + \frac{R_{opt}}{R_s} \right)^{-1} \quad (18)$$

where negative sign manifests degradation of $\eta_{c,max}$ with the increase of R_s . In general supply (or breakdown) voltage constraint silicon power amplifiers, R_{opt} tends to be small, typically ranging ~ 1 's Ω to ~ 10 's Ω , while R_p could be an order of magnitude higher than R_{opt} . When an output impedance matching network is incorporated, the matching network loss could be noticeable and R_s could be comparable to R_{opt} . This implies that the efficiency degradation may be highly sensitive to R_s . For instance, if $R_{opt} = 20 \Omega$ and $R_s = 5 \Omega$, then $S_{R_s}^{\eta_{c,max}} = -0.2$ from (18), claiming another efficiency reduction by 20% even if R_p is infinite. In this work, we choose $R_{opt} = 50 \Omega$ to eliminate the impedance matching loss and thus to minimize the loss (R_s) in the series signal path. This confines the maximum achievable output power for efficiency, revealing the tradeoff between output power and efficiency in a supply constraint integrated silicon PA.

E. Other Nonidealities

A number of other non-idealities could affect the efficiency further. First, any deviation from the 180° conduction angle may alter the collector efficiency. This, however, does not necessarily degrade PAE since biasing slightly larger than *ideal* class-B, so-called *deep* class-AB biasing, will improve the power gain, resulting in a better PAE. In fact, due to the difficulty in defining an *exact* class-B bias point in practical designs, a common tactic for searching optimum bias point is to push the power transistor biasing gradually from a class-AB point toward *close enough* to a class-B operation while securing adequate gain, not to sacrifice the PAE in simulations.

Second, non-open second harmonic impedance or non-zero third harmonic impedance will spawn finite second harmonic current and third harmonic voltage spectrum, respectively, causing extra DC power dissipation by the generator and sacrificing efficiency thereof. Particularly, the non-ideal magnitude of second harmonic impedance may result in a suboptimal v_{2m}/v_{1m} in (9), waning the achievable maximum efficiency lower than the $\eta_{c,max}$ in (10).

Finally, for the sake of simplicity, the order of controlled harmonics is limited up to a third order. However, higher-order harmonics could be load-pulled depending on the frequency response of a load network. If higher-order even or odd harmonics are present exclusively in the voltage or current waveform, not both, it could improve the waveform flatness and thus enhance efficiency. For instance, because of a natural low reactance by the parasitic load capacitance at high order harmonic frequencies in class-F⁻¹ PAs, the fifth-order harmonic current is often notable, as can be seen in section IV. When including the fifth harmonic current, [2] has suggested following numerical polynomial for the maximally flat current waveform:

$$i_{CE}(\theta) \cong I_{DC} (1 - 1.207 \cdot \cos\theta + 0.28 \cdot \cos 3\theta - 0.073 \cdot \cos 5\theta). \quad (19)$$

This increases the ratio of i_{fund}/I_{DC} from $2/\sqrt{3} \cong 1.155$ in (3) to 1.207, and thereby enhances the $\eta_{c,max}$ from 67% to 70% when taking into account a 5.9 V V_{BK} and 0.4 V V_{knee} in the previous example ($V_{DC} = 2.3$ V). However, if the higher order harmonics are present commonly in the collector voltage and current, it could create an active harmonic power. This will impair efficiency although the impairment may not be conspicuous due to a smallness of the higher-order harmonic power compared with the fundamental signal power.

III. INVERSE CLASS-F LOAD NETWORK

A. Multi-Resonance Parallel Load

Fig. 4(a) shows a multi-resonance load network driven by a frequency-dependent nonlinear current source emulating the power amplifiers output current. C_L represents the PA's output load capacitance including the generator's output parasitic capacitance and is presumed to have no frequency dependency. The LC tanks can be replaced equivalently with frequency-dependent inductors, $L_{eq1}(\omega)$ in (20) and $L_{eq2}(\omega)$ in (21), of which the inductance varies widely from a positive to a negative (or capacitive), depending on the operation frequency.

$$L_{eq1}(\omega) = \frac{L_1}{1 - (\omega/\omega_{o1})^2}, \quad \text{where } \omega_{o1} = 1/\sqrt{L_1 C_1}. \quad (20)$$

$$L_{eq2}(\omega) = \frac{L_2}{1 - (\omega/\omega_{o2})^2}, \quad \text{where } \omega_{o2} = 1/\sqrt{L_2 C_2}. \quad (21)$$

Explicit harmonic control is limited up to the third harmonic of a fundamental frequency (ω_0) and the PA current is approximated to a nonlinear current, dependent on ω_0 , $2\omega_0$, and $3\omega_0$ in Fig. 4. Suppose that the local resonance frequencies by the L_1 - C_1 tank (ω_{o1}) and L_2 - C_2 tank (ω_{o2}) satisfy $\omega_0 < \omega_{o1} < 2\omega_0 < \omega_{o2} < 3\omega_0$. Then, the equivalent circuits at ω_0 ,

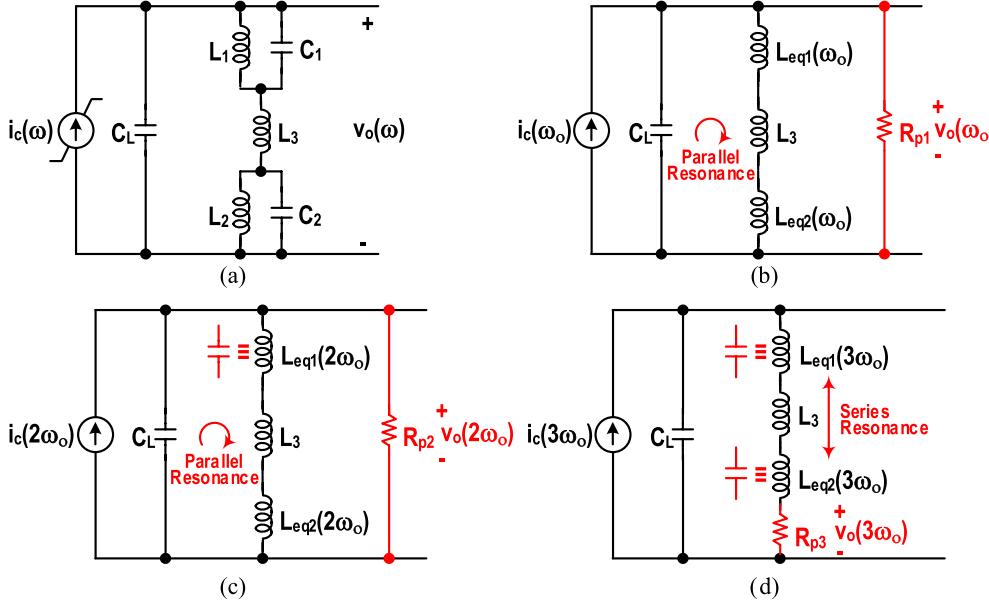


Fig. 4. (a) Multi-resonance parallel LC load network driven by a nonlinear current source emulating power amplifier output current. (b) Equivalent load networks with a finite loss (R_{p1}) at fundamental frequency (ω_0). (c) Equivalent load networks with a finite loss (R_{p2}) at second harmonic ($2\omega_0$). (d) Equivalent load networks with finite loss (R_{p3}) at third harmonic ($3\omega_0$).

$2\omega_0$, and $3\omega_0$ can be reconfigured as shown in Fig. 4(b)–(d), respectively.

For an inverse Class-F operation, the choice of the passive components shall satisfy the following design equations:

$$L_{eq1}(\omega_0) + L_{eq2}(\omega_0) + L_3 = 1 / (\omega_0^2 C_L) \quad (22)$$

$$L_{eq1}(2\omega_0) + L_{eq2}(2\omega_0) + L_3 = 1 / (4\omega_0^2 C_L) \quad (23)$$

$$L_{eq1}(3\omega_0) + L_{eq2}(3\omega_0) + L_3 = 0. \quad (24)$$

Equations (22) and (23) express the parallel resonances at ω_0 and $2\omega_0$ in Fig. 4(b) and (c), respectively. Equation (24) indicates series resonance in the inductor branch in Fig. 4(d). In Fig. 4, R_{p1} and R_{p2} represent effective tank losses after the resonances at ω_0 and $2\omega_0$. R_{p3} expresses a series loss in the series resonance path. For a given technology, different combinations of L_s and C_s will give different tank losses. The best practice for determining the optimum component set will be to choose the component combinations causing a power loss minimally in the passive networks.

This can be achieved by the following optimization process. First, for a given ω_0 we choose a particular set of $\{\omega_{01}, \omega_{02}\}$ subjected to $\omega_0 < \omega_{01} < 2\omega_0 < \omega_{02} < 3\omega_0$. Then, using (22)–(24) we determine a components set of $\{L_1, L_2, L_3, C_1, C_2\}$ and characterize corresponding R_{p1} , R_{p2} , and R_{p3} through EM simulations. By sweeping $\{\omega_{01}, \omega_{02}\}$ two dimensionally and repeating the loss characterization for each components set, contour plots of the loss resistances can be obtained, and optimum design window for a minimum tank loss can be found graphically.

Figs. 5 and 6 illustrate this design process. Fig. 5 plots all possible combinations of $\{L_1, L_2, L_3, C_1, C_2\}$ by sweeping f_{01} ($= \omega_{01}/2\pi$) and f_{02} ($= \omega_{02}/2\pi$). For 24 GHz

PA, the range of f_0 is $23 \text{ GHz} < f_0 < 25 \text{ GHz}$, requiring two-dimensional frequency sweeping of $26 \text{ GHz} < f_{01} < 47 \text{ GHz}$ and $55 \text{ GHz} < f_{02} < 72 \text{ GHz}$. C_L is around 60–65 fF (see Section III-B). Under the f_{01} and f_{02} sweepings, the ranges of the passive components are found by applying (22)–(24): $80 \text{ pH} < L_1 < 200 \text{ pH}$ [Fig. 5 (a)]; $10 \text{ pH} < L_2 < 120 \text{ pH}$ [Fig. 5 (b)]; $15 \text{ pH} < L_3 < 200 \text{ pH}$ [Fig. 5 (c)]; $40 \text{ fF} < C_1 < 200 \text{ fF}$ [Fig. 5 (d)]; and $50 \text{ fF} < C_2 < 500 \text{ fF}$ [Fig. 5 (e)].

In these variations of the passive components, typical on-chip spiral inductors' Q is 18 at the f_0 -band, 21 at the $2f_0$ -band, and 24 at the $3f_0$ -band according to EM modeling. For T-line inductors, Q is ~ 35 for all bands. The Q of MIM capacitors is typically 35 at the f_0 -band, and diminishes to 25 at the $2f_0$ -band and 12 at the $3f_0$ -band. These component Qs are applied to estimate R_{p1} , R_{p2} , and R_{p3} in first order. Fig. 6 shows the contour plot of R_{p1} , R_{p2} , and R_{p3} versus $\{f_1, f_2\}$. As mentioned, a $50\text{-}\Omega$ has been chosen for the PA's optimum load and the optimum design window are selected by the following criteria: $R_{p1} > 20 \cdot R_{opt}$ (1 k Ω), $R_{p2} > 3 \cdot R_{opt}$ (150 Ω), and $R_{p3} < 0.2 \cdot R_{opt}$ (10 Ω). The grey dots in Fig. 6 show the design point applied in this work, resulting in $f_{01} = 30 \text{ GHz}$ and $f_{02} = 58 \text{ GHz}$ and $\{L_1, L_2, L_3, C_1, C_2\} = \{153 \text{ pH}, 43 \text{ pH}, 111 \text{ pH}, 184 \text{ fF}, 175 \text{ fF}\}$.

The same optimization strategy has been applied for 38 GHz PA design ($C_L = 60 \text{ fF}$), resulting in $\{f_{01}, f_{02}\} = \{50 \text{ GHz}, 90 \text{ GHz}\}$ and $\{L_1, L_2, L_3, C_1, C_2\} = \{105 \text{ pH}, 27 \text{ pH}, 70 \text{ pH}, 90 \text{ fF}, 110 \text{ fF}\}$. One particular distinction for the 38 GHz PA is that the MIM capacitors given in the library models suffer from a low Q at the target mm-wave bands. So, as illustrated in Fig. 7, the MOM capacitors are custom made, utilizing BEOL lower metal layers and silicon dioxide as a dielectric to guarantee at least Q ~ 80 at a fundamental frequency and Q > 20 up to a third harmonic band over 100 GHz. After setting

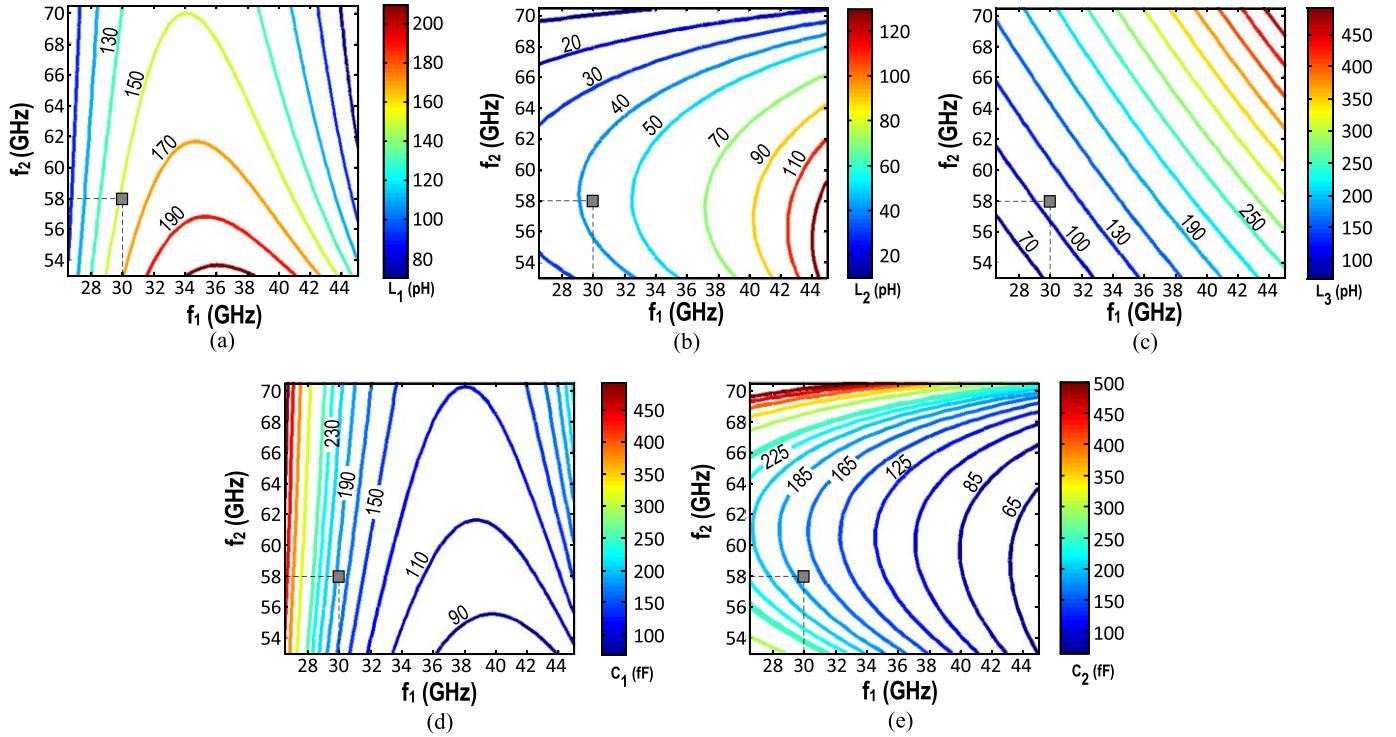


Fig. 5. Contour plots of the passive L and C components values as the function of $\{f_1, f_2\}$ satisfying the equations of (22)-(24): (a) L_1 (pH), (b) L_2 (pH), (c) L_3 (pH), (d) C_1 (fF), and (e) C_2 (fF).

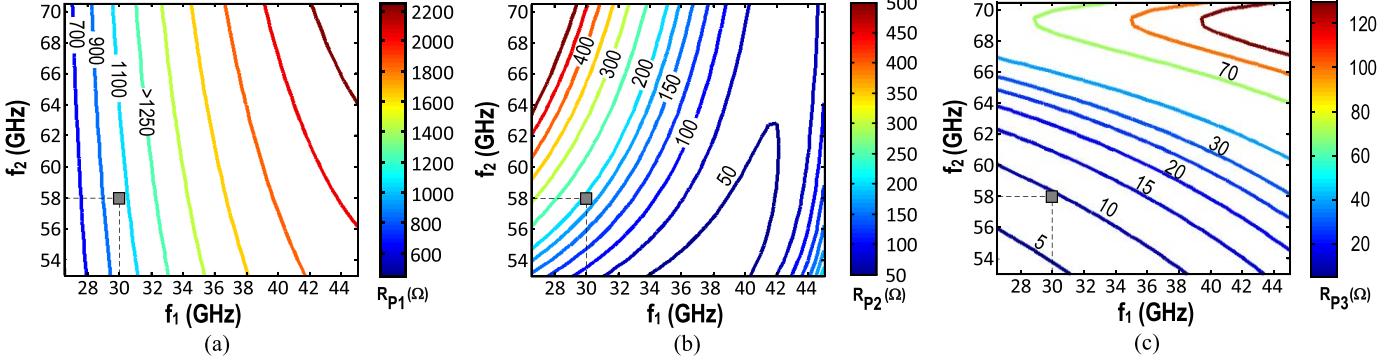


Fig. 6. Contour plots of equivalent loss resistances when $\{L_1, L_2, L_3, C_1, C_2\}$ vary as in Fig. 5: (a) R_{P1} , (b) R_{P2} , and (c) R_{P3} in Fig. 4, respectively. The rectangular dot is the design point chosen in this work, i.e. $f_1 = 30 and $f_2 = 58.$$

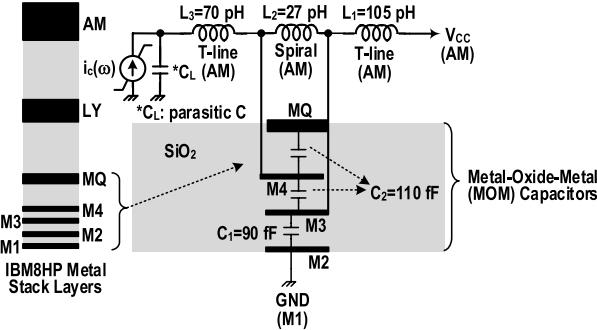


Fig. 7. IBM8HP SiGe BiCMOS process metal stack layers [15] and implementation of the parallel multi-resonance load network for 38 GHz PA.

the passive component values, full EM simulations have been conducted for a fine optimization and extraction of more exact loss resistances.

B. Dual-Resonance Series Load

Fig. 8 completes the inverse class-F load network by cascading a dual resonance series LC resonator with the multi-resonance parallel load described in the previous section. The role of the series network is obvious: L_s - C_s tank resonates at $2\omega_0$, isolating a PA load from the generator at the second harmonic band to maintain a high impedance at the generator's collector node. At a ω_0 -band, the $2\omega_0$ -resonator becomes inductive ($\sim 4/3 \cdot L_s$) which is resonated out in series with C_M , enabling the PA to fully deliver an active power to the PA's optimum load. As in the parallel load, to minimize the loss in the series path, the choice of the passive component needs an iterative optimization. For a high Q, the L_s - C_s tank is implemented with the custom-made MOM capacitor as illustrated in Fig. 7.

Tables I and II summarize the optimized passive component values and major parasitic resistances characterized with EM

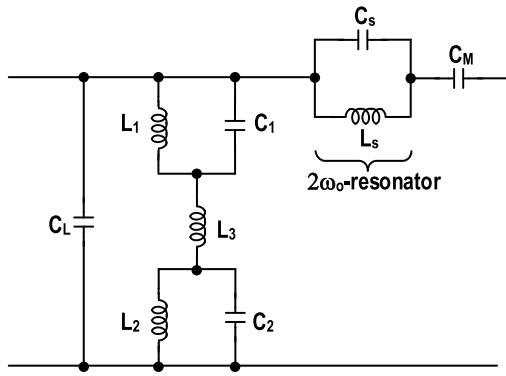


Fig. 8. Complete inverse Class-F load network by adding a series dual resonance network. The L_s-C_s tank resonates at the $2\omega_0$ band and at ω_0 band the effective inductance from the L_s-C_s tank will be resonated with the C_M .

TABLE I

SUMMARY OF THE PASSIVE VALUES OF THE CLASS-F⁻¹ LOAD NETWORK

	C_L (fF)	L_1 (pH)	L_2 (pH)	L_3 (pH)	C_1 (fF)	C_2 (fF)	L_s (pH)	C_s (fF)
24 GHz PA	65	153	43	111	184	175	108	100
38 GHz PA	60	105	27	70	90	110	70	65

TABLE II

SUMMARY OF THE EQUIVALENT PARASITIC RESISTANCES

	R_{P1} (Ω) @ f_0	R_{P2} (Ω) @ $2f_0$	R_{P3} (Ω) @ $3f_0$	R_S (Ω) @ f_0	R_S (Ω) @ $2f_0$
24 GHz PA	1000	240	5	2	480
38 GHz PA	900	200	6	3	420

simulations including output RF pad. With eliminating output impedance matching circuit and by a careful optimization, the effective R_s is suppressed to below 2 Ω at 24 GHz and below 3 Ω at 38 GHz. R_{p1} is 1 k Ω and 0.9 k Ω at 24 GHz and 38 GHz, respectively. From (16), the P_{loss} is estimated to 0.914 at 24 GHz and 0.891 at 38 GHz. Thus, in continuing the previous example ($V_{BK} = 5.9$ V, $V_{knee} = 0.4$ V, and $V_{DC} = 2.3$ V) with assuming the bi-harmonic control, the maximum achievable collector efficiency can be estimated as

$$\begin{aligned}\eta_{c,max} &= 67\% \times P_{loss} \\ &= 61.2\% @ 24 \text{ GHz and } 59.7\% @ 38 \text{ GHz.}\end{aligned}\quad (25)$$

The $\eta_{c,max}$ increases by a few % when the current waveform contains an ideal 5th harmonic content in (19), resulting in

$$\begin{aligned}\eta_{c,max} &= 70\% \times P_{loss} \\ &= 64\% @ 24 \text{ GHz and } 62.4\% @ 38 \text{ GHz.}\end{aligned}\quad (26)$$

It is important to guarantee the validity of the passive components models up to at least the third harmonics of the design frequencies for the integrity of the second and third harmonics impedance control. For this, individual passive components are modeled with 2-port S-parameters valid up to ~ 240 GHz using the EM field solver.

IV. TWO-STAGE CLASS-F⁻¹ POWER AMPLIFIER DESIGN

Fig. 9 shows the proposed two-stage 24 GHz power amplifier comprised of a class-AB driving amplifier followed by an

inverse class-F output PA which adopts the harmonically tuned load described in the previous section. The same 2-stage PA topology has been used for 38 GHz PA design [13]. Target saturated output power (P_{sat}) is in the range of 50-70 mW, a compromise for the best PAE performance. The design step is first to design the output stage to produce the required P_{sat} with a maximum possible PAE. Then, based on a saturated power gain, the class-AB driver is designed to deliver an optimum inter-stage driving power to the output stage, followed by the design of an inter-stage matching network that concurrently meets an optimum power matching between the driver and the output PA with a maximum PAE in the driver stage as well.

A. Inverse Class-F Output Power Amplifier

1) *Circuit Design:* To produce 17-18 dBm of 1-dB compressed output power (OP_{-1dB}) on 50- Ω R_{opt} , the required fundamental peak voltage swing is 2.3-2.4 V. In order to meet the peak swing requirement after taking 400-450 mV V_{knee} into account, the optimum supply voltage, V_{DC} from (11), is in the range of 2.3-2.4 V (V_{CC1} in Fig. 9). This will create a maximum of about 5.9 V of sinusoidal peaking at the collector of Q_1 . In the given 0.13 μm SiGe BiCMOS technology, the BV_{CEO} of a SiGe HBT is 1.8 V. However, in practical circuit designs the base node will not be open but terminated with a finite resistance by a DC bias network which provides a discharging path from the base to ground, preventing the base charge accumulation and thus avoiding the early collector impact ionization [16], [17]. Realistically, in such circumstance the breakdown voltage of the transistor would be limited by BV_{CBO} . The BV_{CBO} of the given SiGe HBT technology is 6 V [15], relieving the reliability issue when developing the target P_{sat} over the 50- Ω load.

In Fig. 9, the base of Q_1 ($l_e = 2 \times 16.5 \mu\text{m}$ for 24 GHz, $l_e = 2 \times 14.5 \mu\text{m}$ 38 GHz) is biased at ~ 0.83 V (V_{BB1}), conducting ~ 8 mA of quiescent collector current and pushing Q_1 into a deep class-AB point when driven by 0 dBm input power (P_{in}). The size of Q_1 is optimized to have a current density of $J_C = 1.4 \text{ mA}/\mu\text{m}$ to achieve a peak 180 GHz f_T at 15 dBm OP_{-1dB} ($I_{DC} = 40$ mA). This maintains ~ 9.5 dB power gain (G_p) at 24 GHz and 7 dB G_p at 38 GHz until the output reaches 1-dB gain compression point. The base bias path provides $<150 \Omega$ of DC resistance to prevent the early collector breakdown. The $\sim 0.5 \text{ nH}$ of L_B is realized by a narrow or meandered transmission line for a small form factor (see Fig. 16) and isolates the bias circuit from Q_1 in AC-wise. Therefore, the bias circuit causes negligible loading to the amplifier. Once establishing the Q_1 size and bias conditions ($V_{CC1} = 2.3$ V), a series of DC, AC load lines and load pull simulations are conducted, which estimates $\sim 800 \Omega$ of the transistor's large signal output resistance and 60-65 fF of parasitic output load capacitance (C_3). About 15 fF of parasitic capacitance stemmed from the layout interconnects are modeled using an EM field solver [18] and absorbed into C_3 in Fig. 9.

2) *Time-domain Simulation Waveform Analysis:* The CAD simulation results on the AC load lines at the output stage collector node, time-domain V-I waveforms, and corresponding

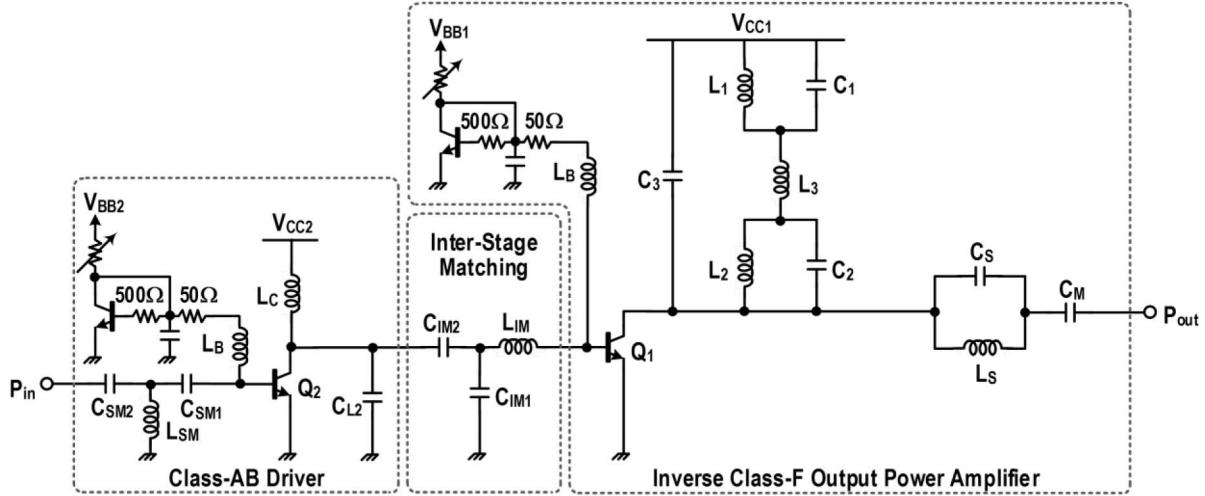


Fig. 9. Schematic of the 2-stage power amplifier, cascade of Class-AB driver followed by inverse Class-F output stage. Inter-stage matching is applied to achieve an optimum power delivery to the PA with a maximum PAE in the driver.

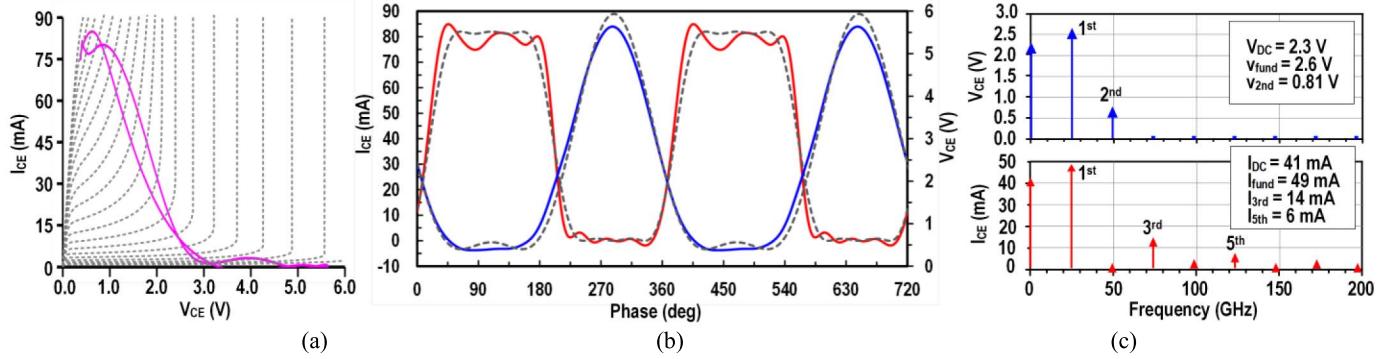


Fig. 10. Time domain simulation results for 24 GHz PA at $P_{out} = 18$ dBm (OP_{-1dB}): (a) AC load line, (b) collector voltage and current waveforms, and (c) spectrum of the collector voltage and current. In the time domain V-I waveforms, dot lines are ideal class-F $^{-1}$ waveforms based on (19) and (11) for the current and voltage, respectively, where $V_{knee} = 0.4$ V.

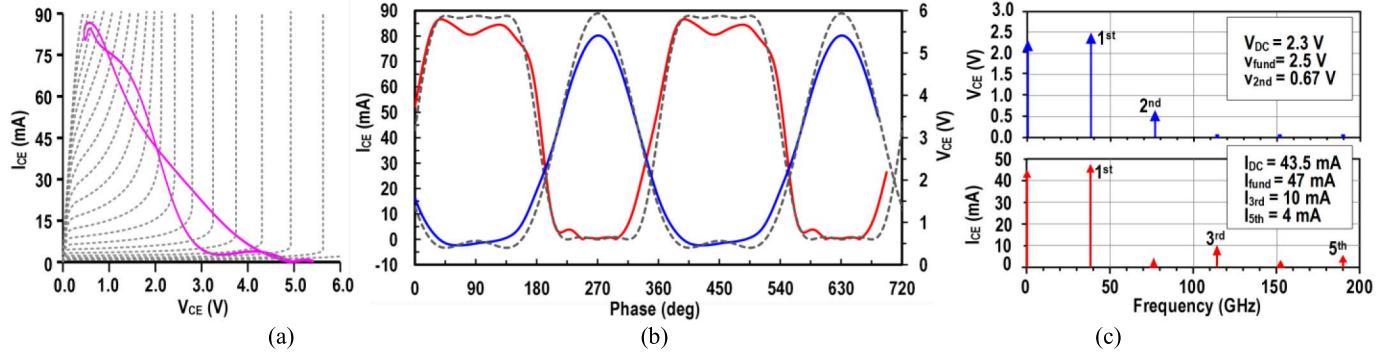


Fig. 11. Time domain simulation results for 38 GHz PA at $P_{out} = 17.5$ dBm (OP_{-1dB}): (a) AC load line, (b) collector voltage and current waveforms, and (c) spectrum of the collector voltage and current. In the time domain V-I waveforms, dot lines are ideal class-F $^{-1}$ waveforms based on (19) and (11) for the current and voltage, respectively, where $V_{knee} = 0.4$ V.

spectrum analyses are shown in Figs. 10 and 11 for 24 GHz and 38 GHz PAs, respectively. In the simulations, the output power is 18 dBm for 24 GHz PA and 17.5 dBm for 38 GHz PA. In the time domain waveforms in Fig. 10 (b) and Fig. 11 (b), dot lines are ideal current and voltage waveforms based on (19) and (11), respectively, where $V_{knee} \approx 0.4$ V. In the current spectra, analyzed in Figs. 10 (c) and 11 (c), due to a natural short-like capacitive impedance contributed by the PA load

at high-order harmonic frequencies, non-negligible fifth harmonic current spectra is observed for both PAs. This enhances the transition sharpness of the current switching, shaping better rectangular waveform which is fairly well matched with the ideal curves, and thus improving η_c . Note that this is a unique benefit in class-F $^{-1}$ PAs, since in class-F PAs it requires a large impedance at the fifth harmonic frequency to shape similar quality rectangular voltage waveform, which will be much

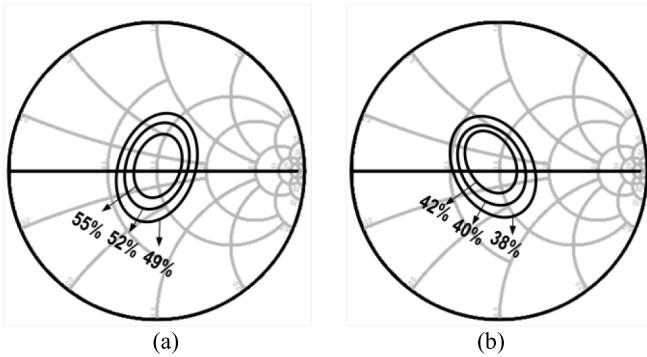


Fig. 12. Output class-F⁻¹ stages PAE load-pull simulation results: (a) 24 GHz PA (output stage gain: 9.5 dB and $\eta_c = 61\%$ on $50\Omega R_{opt}$) and (b) at 38 GHz PA (output stage gain: 7 dB and $\eta_c = 51.5\%$ on $50\Omega R_{opt}$).

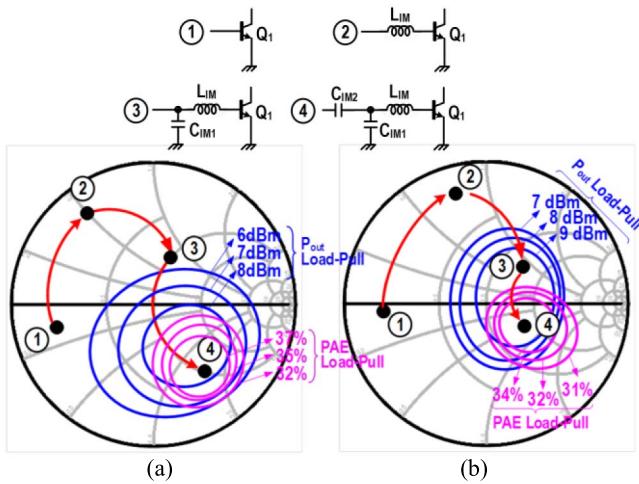


Fig. 13. Load-pulls (P_{out} and PAE) design of the interstage impedance matching network to achieve an optimum interstage power delivery at a maximum PAE in the class-AB driver: (a) 24 GHz PA (inter-stage gain: 9.5 dB and $\eta_c = 41.5\%$) and (b) 38 GHz PA (inter-stage gain: 8 dB and $\eta_c = 40\%$).

more challenging task than creating a low impedance because of increasing passive component loss at higher order harmonic bands.

The native low reactance effectively terminates the voltage spectra that are higher than the second harmonic, shaping the $2\omega_0$ induced half-sinusoidal voltage peaking. The v_{2nd}/v_{fund} is ~ 0.29 at 24 GHz and 0.26 at 38 GHz, while the optimal value is ~ 0.354 based on the analysis in (9), which causes about 0.4–0.5 V smaller peaking than the ideal 5.9 V_{peak}. From the spectrum analyses, $\eta_c = 67.5\%$ at 24 GHz and $\eta_c = 58.7\%$ at 38 GHz at the collector node of each PA. The efficiency is, however, decreased on the $50\Omega R_{opt}$ due to the power loss caused by a finite Q of the load network. When considering $P_{loss} = 0.914$ at 24 GHz and 0.891 at 38 GHz, the net collector efficiency becomes $\eta_c = 61.7\%$ at 24 GHz and $\eta_c = 52.3\%$ at 38 GHz. Compared with the theoretical estimation in (26), the simulation result at 24 GHz is only 2.3% less than the theoretical value. Because of the finite unity current gain frequency (f_T), the current driving capability (g_m) of the power transistor becomes smaller as

TABLE III
SUMMARY OF THE PASSIVE VALUES IN THE DRIVING STAGES

	Input Matching		Driver Load		Inter-Stage Matching			
	C_{SM1} (fF)	C_{SM2} (fF)	L_{SM} (pH)	L_C (pH)	C_{L2} (fF)	L_{IM} (pH)	C_{IM1} (fF)	C_{IM2} (fF)
24 GHz PA	105	170	223	350	32	165	115	51
38 GHz PA	90	130	150	220	38	130	100	60

the frequency increases. Further, because of lower second harmonic impedance, the second harmonic voltage is smaller at 38 GHz in Fig. 11 than at 24 GHz in Fig. 10. These claim more DC power at 38 GHz than at 24 GHz to develop similar P_{out} and harmonic voltage and current contents, diminishing the collector efficiency and thus widening the error from a theoretical maximum: the η_c at 38 GHz is about 10% lower than the theoretical value.

Since the power gain is 9.5 dB at 24 GHz and 7 dB at 38 GHz, the PAE will be 56% and 42% at 24 GHz and 38 GHz, respectively, which agrees well with the load-pull simulation results shown in Fig. 12. Apparently, the limited power gain due to insufficient f_T or f_{max} of the silicon transistor reduces the PAE substantially from the collector efficiency, causing about 6% and 10% efficiency reduction from the $\eta_{c,max}$ at 24 GHz and 38 GHz, respectively.

B. Class-AB Driving Amplifier

The tuned common-emitter driver in Fig. 9 is biased at a class-AB point ($V_{BB2} = 0.83$ V and $I_{CE,Q2} = 3.2$ mA). The size ($l_e = 10\mu m$ for 24 GHz PA, $l_e = 16\mu m$ for 38 GHz PA) and supply voltage ($V_{CC2} = 2V$ for 24 GHz PA, $V_{CC2} = 1.5V$ for 38 GHz PA) of Q_2 are optimized to drive the output power stage to saturation when the driver output power reaches near 1-dB compression point (7 dBm @24 GHz PA, 8 dBm @38 GHz PA), resulting in a high PAE (37%@ 24GHz PA, 34%@38 GHz PA) from the driver. Input is matched to 50Ω using T-network composed of the transmission (T)-line inductor L_{SM} and MIM capacitors, C_{SM1} and C_{SM2} . The T-line inductor L_C resonates out only a portion of C_{L2} to provide a capacitive impedance at ω_0 , which is necessary to achieve simultaneous matching for both optimum output power and maximum efficiency. In Fig. 13 the impedance locus on the Smith Chart which is dependent on the inter-stage matching elements is illustrated in a step-by-step manner.

In the inter-stage matching network formed by the T-line inductor L_{IM} and MIM capacitors, C_{IM1} and C_{IM2} , in Fig. 9, L_{IM} and C_{IM1} establish an optimum power matching. This matching network transforms the small impedance seen from the base of Q_1 in Fig. 13 ① to an optimum power impedance point in Fig. 13 ③, thus driving the PA output stage with $>8\text{--}9$ dBm of inter-stage power. In order to achieve the highest possible PAE in the driver, C_{IM2} is cascaded to move the impedance matching point further to the overlapped capacitive region in Fig. 13 ④ where the peak P_{out} and PAE contours form a common impedance area. This allows the driver stage to achieve both optimum power matching and a maximum inter-stage PAE concurrently. Table III summarizes the passive component values in the driving stage.

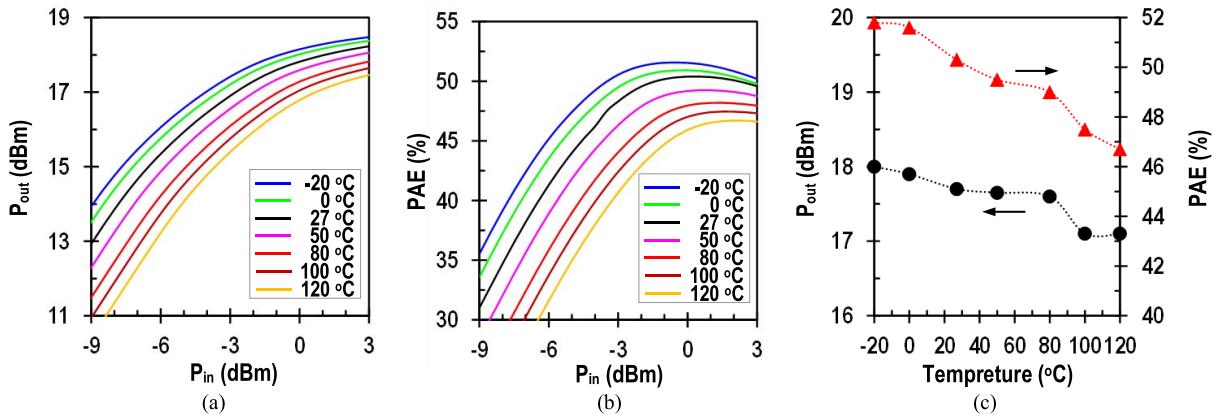


Fig. 14. Simulation results of P_{out} and PAE over temperature variation from -20° to 120° at 24 GHz: (a) P_{out} , (b) PAE, and (c) summary of the peak PAE and corresponding output power for the temperature variation range.

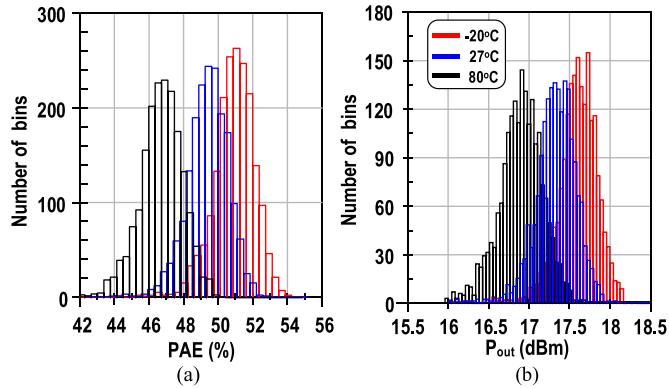


Fig. 15. Monte-Carlo simulations of the 24 GHz PA over process variations at three different temperatures (-20° , 27° , and 80°): (a) peak PAE and (b) P_{out} corresponding to the peak PAE.

The inter-stage PAE load-pull simulations are conducted at the driver's output 1 dB gain compression point where the power gain of the driver is 10 dB and 8.5 dB at 24 GHz and 38 GHz, respectively.

After cascading the driver and output stages, the overall gain at OP_{-1dB} point is 19 dB, $\eta_c = 53\%$, and $PAE = 51\%$ at 24 GHz in simulations. At 38 GHz, the simulated 1 dB compressed gain = 15 dB, $\eta_c = 41.5\%$, and $PAE = 39\%$. The input impedance matching bandwidth for $S_{11} < -10$ dB is 20–30 GHz for 24 GHz PA, and 30–50 GHz for 38 GHz PA. Fig. 14 presents the P_{out} and PAE simulation results of the 24 GHz 2-stage PA over the temperature variations when the PA is biased with a constant current mirror. The saturated output power decreases from 18.5 dBm to 17 dBm by increasing the temperature from -20° C to 120° C [Fig. 14 (a)]. This is mainly due to the degradation of the current gain β (or f_T) of HBTs over the temperature increase, which results in degradation in peak PAE from 52% at -20° C to 47% at 120° C in Fig. 14(b). In summary, when the temperature changes in the range of $-20 \sim 120^{\circ}$ C, there is ± 0.5 dB variation in output power and $\pm 3\%$ variation in peak PAE compared with the nominal values at the room temperature (27° C). To characterize the PA performance drift over the process variations, Monte-Carlo simulations are performed with 2000 number of iterations at three different temperatures of -20° C,

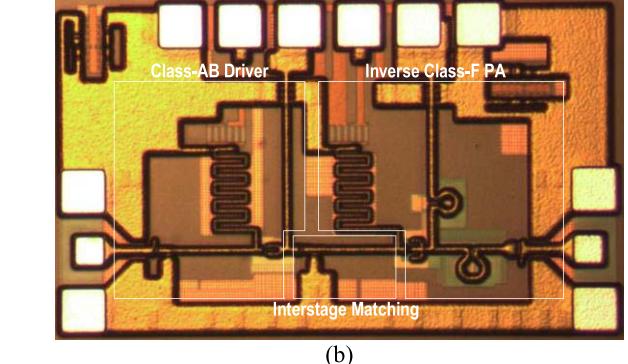
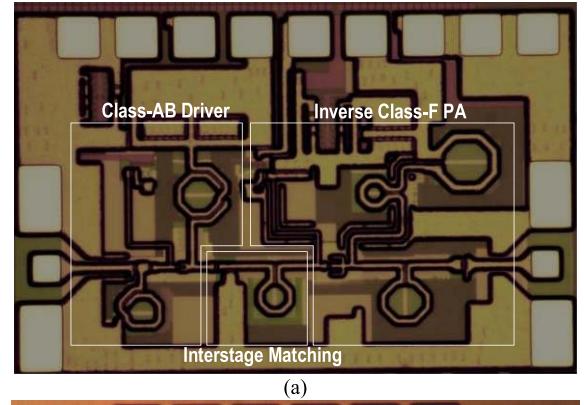


Fig. 16. Chip photographs: (a) 24 GHz PA (size: 0.6×0.95 mm 2) and (b) 38 GHz PA (size: 0.55×0.93 mm 2 including pads).

27° C, and 80° C (Fig. 15). At 27° C, the peak PAE and corresponding P_{out} have Gaussian distributions with mean value of 50% and 17.3 dBm with 3σ deviations of $\pm 1.5\%$ and ± 0.75 dBm. When the temperature increases to 80° C the peak PAE and corresponding P_{out} degrades to $46.5 \pm 2\%$ and 16.8 ± 0.5 dBm, respectively, within the 3σ standard deviations.

V. EXPERIMENTAL RESULTS

The PAs are fabricated in GF8HP 0.13 μ m SiGe BiCMOS process ($f_T/f_{max} = 180/220$ GHz) and Fig. 16 shows the die photographs of the PAs. The PA size is 0.6×0.95 mm 2 for 24 GHz PA [Fig. 16(a)] and 0.55×0.93 mm 2 for 38 GHz PA [Fig. 16(b)], including all pads. On-wafer small-signal

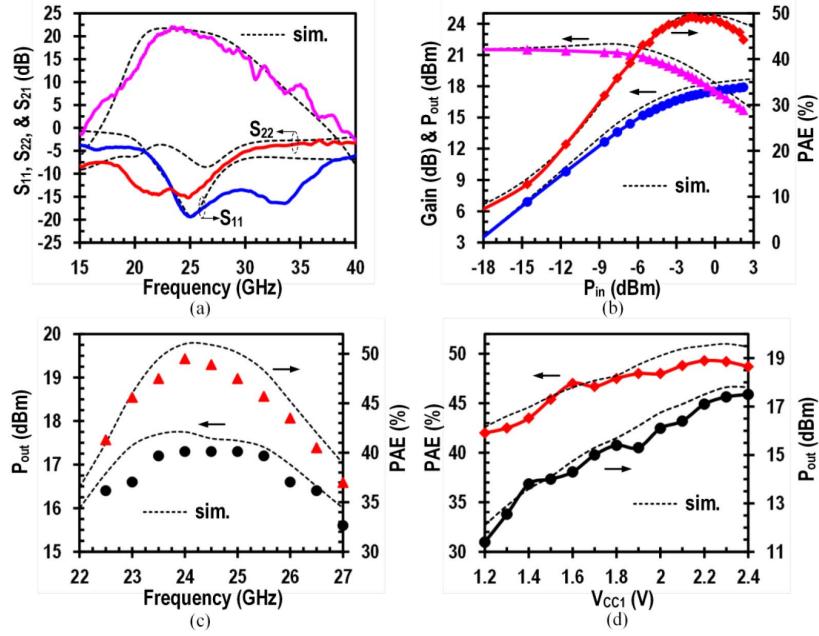


Fig. 17. 24 GHz PA measured performances: (a) gain, input and output matching, (b) power gain, output power, and PAE versus input power, (c) peak PAE and corresponding output power versus frequency, and (d) peak PAE and corresponding output power versus supply voltage of the output stage.

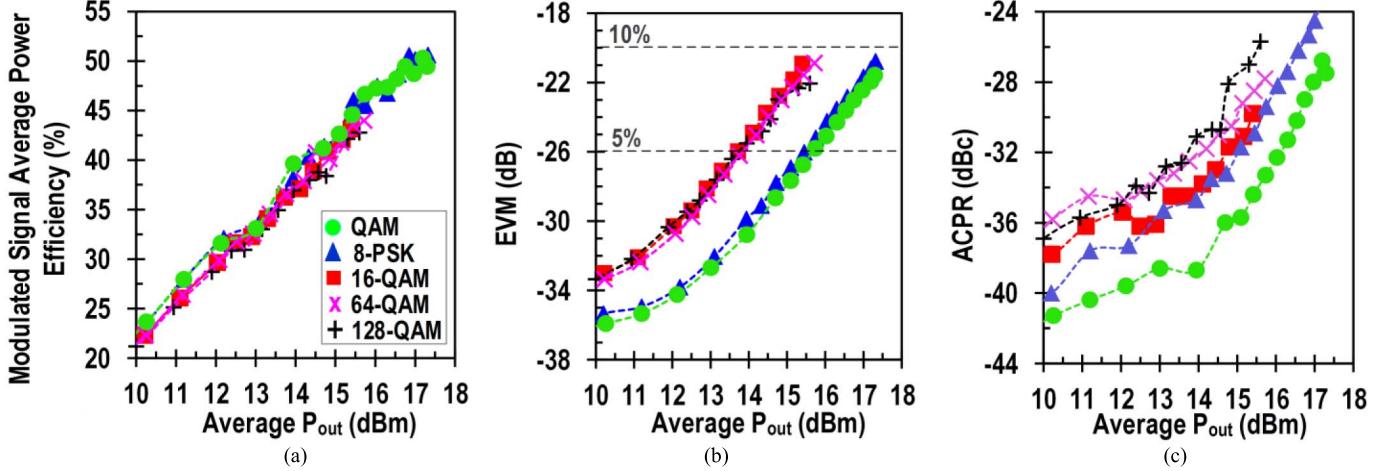


Fig. 18. 24 GHz PA measured modulation power efficiency, EVM, and ACPR versus average output power at 24 GHz for different modulation platforms: (a) power efficiency, (b) EVM, and (c) ACPR at 8 MHz offset bands. ACPR is presented in absolute magnitude scale.

S-parameter measurements are performed after SOLT calibrations. For large signal measurements, the PAs input power is sampled using a directional coupler and the sampled input and PA output powers are evaluated using R&S power sensors and power meters. RF cable loss is characterized and de-embedded carefully over the operational frequency range. The PAs are stable over all measured frequencies.

Modulated signals are also applied to the PAs to characterize in-band and out-of-band linearity performances. The R&S signal source SMW200A provides the PAs with 23-bit pseudo random binary sequence with an arbitrary digital modulation at a carrier frequency variable of up to 40 GHz. After a raised cosine filtering with 0.2 roll-off factor the maximum available bandwidth is 8.4 MHz. The PAs input signal is modulated using various modulation schemes having different peak-to-average power ratio (PAPR) including QAM, 8-PSK, 16-QAM, 64-QAM, and 128-QAM, which result in the bit-rate of 14, 21, 28, 42, and 49 Mbps, respectively. The PA output is fed to the R&S spectrum analyzer, FSW67, to evaluate EVM and ACPR, and corresponding average output power ($P_{out,ave}$) and average power efficiency of the modulated signals. The EVM of the signal source itself is less than 0.9% (-41 dB) for all different modulation schemes at 20-40 GHz. In the PAs testing, ACPR is measured at 8 MHz offset from the carrier center frequency.

16-QAM, 64-QAM, and 128-QAM, which result in the bit-rate of 14, 21, 28, 42, and 49 Mbps, respectively. The PA output is fed to the R&S spectrum analyzer, FSW67, to evaluate EVM and ACPR, and corresponding average output power ($P_{out,ave}$) and average power efficiency of the modulated signals. The EVM of the signal source itself is less than 0.9% (-41 dB) for all different modulation schemes at 20-40 GHz. In the PAs testing, ACPR is measured at 8 MHz offset from the carrier center frequency.

A. 24 GHz Inverse Class-F PA Measurement Results

Fig. 17 shows the small signal and large signal measurement results with biasing $V_{CC1}/V_{CC2} = 2.3/2$ V and $I_{CE1}/I_{CE2} = 11.5/2$ mA. $S_{11} < -10$ dB @22.5-36.5 GHz, $S_{22} < -10$ dB @15-28 GHz, and $S_{21} = 19-22$ dB @ 21.5-27.2 GHz [Fig. 17 (a)]. Fig. 17(b) shows the large signal

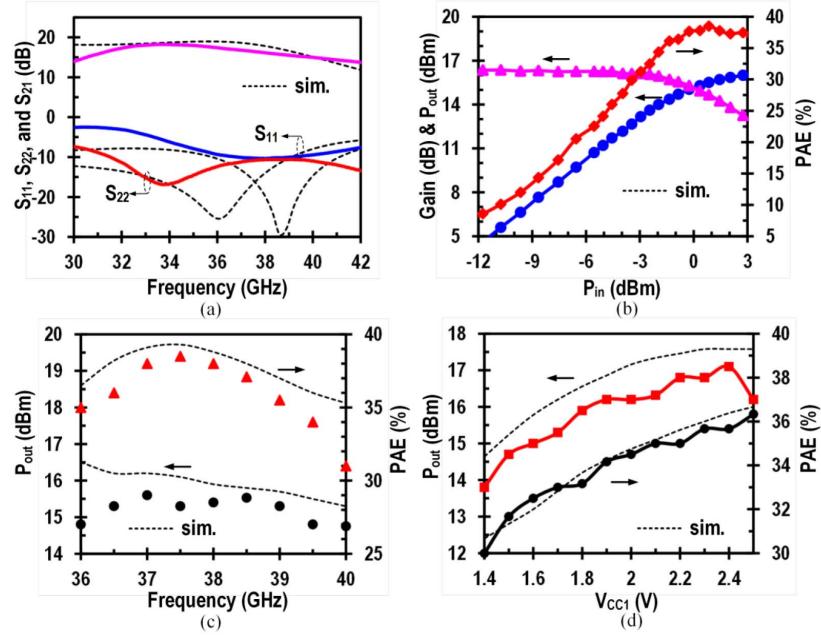


Fig. 19. 38 GHz PA measured performances: (a) gain, input and output matching, (b) power gain, output power, and PAE versus input power, (c) peak PAE and corresponding output power versus frequency, and (d) peak PAE and corresponding output power versus supply voltage of the output stage.

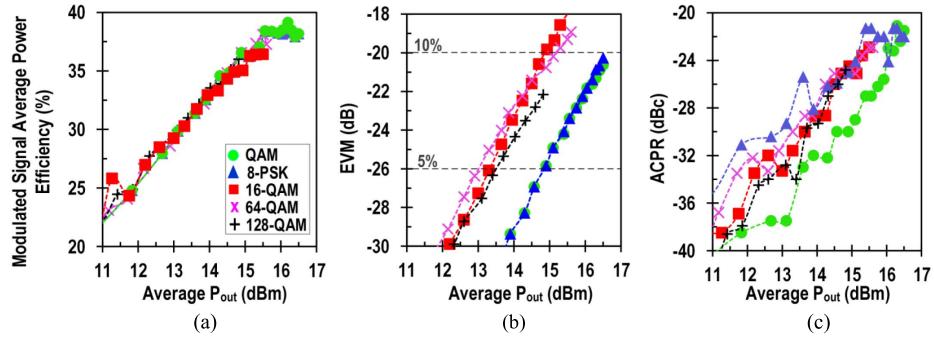


Fig. 20. 38 GHz PA measured modulation power efficiency, EVM, and ACPR versus average output power at 38 GHz for different modulation platforms: (a) power efficiency, (b) EVM, and (c) ACPR at 8 MHz offset bands. ACPR is presented in absolute magnitude scale.

TABLE IV

THE MEASURED PAs PERFORMANCE SUMMARY AND COMPARISON WITH RECENT STATE-OF-THE-ART INTEGRATED SILICON AND III-V PAs

Authors	Freq.(GHz)	PAE (%)	P_{sat} (dBm)	OP_{-1dB} (dBm)	Gain (dB)	Size (mm ²)	Supply (V)	Technology	Feature
This Work	24	50	18	16	21	0.6	2.3	0.13 μ m SiGe	2-stage Class-F ⁻¹
	38	38.5	16.5	15	16.5	0.5	2.4		
CICC 2015 [12]	28	42	17.1	15	21.2	0.49	2.4	0.13 μ m SiGe	2-stage Class-F ⁻¹
ISSCC 2014 [13]	28	40.7	17.1	15	10.3	0.27	2.2	0.13 μ m SiGe	1-stage Class-F ⁻¹
SIRF 2014 [19]	28	35.3	18.6	15.5	15.3	0.43	3.6	0.13 μ m SiGe	2-stage Class-F ⁻¹
BCTM 2011 [28]	37.5	26.2	14.8	NA	5.6	0.74	2.5	0.13 μ m SiGe	2-Stage Class-B
JSSC 2014 [20]	41	36	18.1	NA	21.2	0.49	2.4	0.13 μ m SiGe	1-stage Class-E
RFIC 2012 [22]	42.5	34.4	18.6	17.5	9.5	0.3	2.7	45 nm SOI CMOS	3-stack Class-AB
RFIC 2012 [26]	24	29	18	NA	NA	0.91	1.2	65 nm CMOS	2-stage Class-AB
IMS 2012 [38]	24	24	19	15.7	19	0.4	3.6	0.18 μ m CMOS	2-stage Class-AB
RFIC 2014 [39]	18	41.4	15.9	13.3	11	0.62	2	45 nm SOI CMOS	Cascode Class-E
TMTT 2007 [7]	24	44.5	20	NA	8	3	2.4	GaAs HEMT	1-stage Class-F ⁻¹
TMTT 2012 [40]	24	40	23.5	22	9	1.5	4	GaAs HEMT	1-stage Class-AB
IMS 2012 [41]	29	30	37	NA	25	4.8	20	GaN HEMT	3-stage Class-AB

power measurement results at 24 GHz. The PA achieves peak 50% PAE at 17 dBm P_{out} . The measured P_{sat} is 18 dBm and OP_{-1dB} is 16 dBm. The compressed power gain at the peak

PAE is around 19 dB, well matched with the simulation result. The measured PAE at the 6-dB back-off from the OP_{-1dB} is 22.5%, exhibiting a high PAE at the linear mode as well.

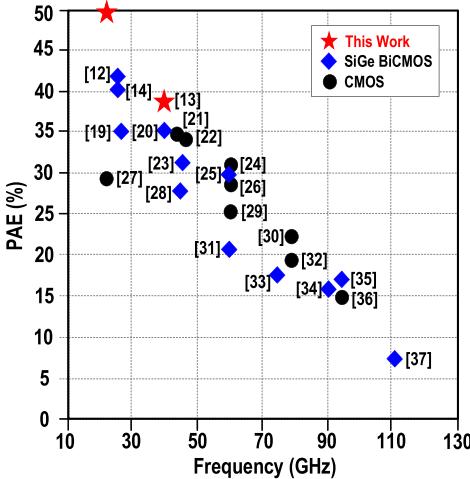


Fig. 21. PAE comparison with state-of-the-art microwave and mm-wave silicon PAs.

To characterize the frequency response of the power efficiency, the PAE is measured over 22–27 GHz. The measurement results of peak PAE and corresponding output power versus frequency is disclosed in Fig. 17(c). The PAE is higher than 45% over the range of 23.5–25.5 GHz with ~ 17.5 dBm of corresponding output power. The trend of measured frequency response of the PAE is well aligned with simulation curve with only 1–2.5% error around the peak PAE point. The PAE is also measured by sweeping the supply voltage of the output stage from 1.2–2.4 V at 24 GHz to characterize the supply dependency of the PAE, and the results are shown in Fig. 17(d). The PA can maintain higher than 45% of peak PAE over 0.9 V supply variations from 1.5–2.4 V, while the output power corresponding to the peak efficiency increases from 14 dBm to 17.5 dBm as the supply voltage increases.

The modulation test results for different modulation schemes are summarized in Fig. 18. The center frequency of the modulation signal is 24 GHz. Obviously, the average power efficiency is proportional to the $P_{out,ave}$ and exceeds 50% when the $P_{out,ave}$ increases over 17 dBm in Fig. 18(a). This shows a good correlation with the monotone test in Fig. 17(b). The measured EVM is plotted in dB scale for better contrast. The QAM and 8-PSK are the least PAPR modulation formats and exhibit the best power efficiency for a given EVM: the $P_{out,ave}$ corresponding to 5% EVM is around 16 dBm for both QAM and 8-PSK in Fig. 18(b). At 5% EVM the PA achieves 47.3% of modulation power efficiency in Fig. 18(a) with < -35 dBc ACPR in Fig. 18(c). For 16-, 64-, and 128-QAM signals, the range of $P_{out,ave}$ for <5% EVM (-26 dB) is 13–13.5 dBm, and the corresponding average power efficiency is around 30–32% with <-32 dBc of ACPR.

B. 38 GHz Inverse Class-F PA Measurement Results

For the 38 GHz PA, Fig. 19(a) and (b) show measured small-signal and large-signal characteristics with a nominal class-AB biasing of $V_{CC1}/V_{CC2} = 2.4/1.5$ V, $I_{CC1}/I_{CC2} = 8/4$ mA; $S_{11} < -10$ dB, $S_{22} < -10$ dB, and $S_{21} = 15\text{--}17$ dB over 36–40 GHz [Fig. 19 (a)]. At 38 GHz with the class-AB

biasing, the PA achieves peak PAE of 38.5% with corresponding 15.5 dBm P_{out} , 15 dBm OP_{-1dB} , and 17 dBm P_{sat} in Fig. 19(b). The measured PAE at the 6-dB back-off from the OP_{-1dB} is 19%. The saturated power gain at the OP_{-1dB} is 15 dB as expected in the design section. The PAE is $>35\%$ over 36–39 GHz in Fig. 19(c) and over 1.5–2.5 V supply voltage variation in Fig. 19(d), manifesting the PAE robustness to the frequency and supply variations. The PAE discrepancy between the measurement and the simulation is $<2\%$ at 37–39 GHz.

As seen in the modulation test results summarized in Fig. 20, the average modulation signal power efficiency reaches around 38–39% when $P_{out,ave}$ exceeds 15.5 dBm. The average PAE in Fig. 20(a) is well matched with the PAE result in Fig. 19(b). The $P_{out,ave}$ for $< 5\%$ EVM is around 15 dBm and 13.5 dBm for QPSK/8-PSK and 16/64/128-QAM signals, respectively, in Fig. 20(b). When the $P_{out,ave}$ is capped for $<5\%$ EVM, the average power efficiency is $\sim 36\%$ for QPSK/8-PSK with $-26\text{--}-27$ dBc ACPR in Fig. 20(c). The efficiency decreases to 30–32% with <-32 dB ACPR when the high spectral-efficiency modulation schemes of 16/64/128-QAM signals are applied to the PA.

Table IV summarizes and compares major measurement PA performance metrics with recent state-of-the-art silicon and III-V based integrated PAs at similar frequency bands. Fig. 21 compares the PAE of recent microwave and mm-Wave silicon PAs more graphically and reveals a trend of diminishing PAE as operational frequency increases. This demonstrates a common tradeoff between power-added efficiency and speed in silicon PAs. While recent PAs based on class-F or class-F⁻¹ technique demonstrate outstanding PAE performance over other high efficiency techniques, the proposed class-F⁻¹ PA adopting a high-order multi-resonance harmonic filter load achieves one of best power efficiency at each frequency band. The measured PAEs are even higher than or comparable to those of recent III-V PAs in Table II.

VI. CONCLUSION

In this paper, two integrated silicon inverse class-F PAs are successfully implemented and demonstrated at microwave and mm-Wave frequencies. This paper fully discusses the potentials and limitations of the class-F⁻¹ technique in achieving a high PAE at microwave and higher frequencies, especially for integrated PAs based on silicon process; the impact of a finite number of harmonics control, knee voltage, limited breakdown voltage, and finite losses from passive components on the PAE has been analyzed. In order to shape better class-F⁻¹ voltage and current waveforms, the PAs adopt multi-resonance parallel and series loads that modulate the load impedance cooperatively to pull the PAs with an optimal impedance which is variable depending on fundamental, even, and odd harmonic bands. An inter-stage matching is also applied in order to achieve optimum inter-stage power transfer with a maximum PAE in the driver stage. This leads to overall 50% peak PAE at 24 GHz and 38.5% PAE at 38 GHz, some of the highest PAEs in the integrated PAs reported so far for both silicon and III-V technologies. Certainly, the PAs can process an ultrahigh

speed modulation signal with a high efficiency since the signal bandwidth for power gain, impedance matching, and PAE is greater than several GHz, thus suitable for the application of the next generation high-speed wireless communications.

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