A 25 dBm Outphasing Power Amplifier With Cross-Bridge Combiners

Lei Ding, *Member, IEEE*, Joonhoi Hur, *Member, IEEE*, Aritra Banerjee, *Member, IEEE*, Rahmi Hezar, and Baher Haroun, *Fellow, IEEE*

***Abstract*—In this paper, we present a 25 dBm Class-D outphasing power amplifier (PA) with cross-bridge combiners. The Class-D PA is designed in a standard 45 nm process while the combiner is implemented on board using lumped elements for flexibilities in testing. Comparing with conventional non-isolated combiners, the elements of the cross-bridge combiner are carefully chosen so that additional resonance network is formed to reduce out-of-phase current, thereby increasing backoff efficiency of the outphasing PA. The Class-D outphasing PA with the proposed combiner is manufactured and measured at both 900 MHz and 2.4 GHz. It achieves 55% peak power-added efficiency (PAE) at 900 MHz and 45% at 2.4 GHz for a single tone input. For a 10 MHz LTE signal with 6 dB PAR, the PAE is 32% at 900 MHz with −39 dBc adjacent channel power ratio (ACPR) and 22% at 2.4 GHz with −33 dBc ACPR. With digital predistortion (DPD), the linearity of the PA at 2.4 GHz is improved further to reach −53 dBc, −50 dBc, −42 dBc ACPR for 10 MHz, 20 MHz, and 2-carrier 20 MHz LTE signals.**

***Index Terms*—Class-D, CMOS power amplifier, digital predistortion, LINC, non-isolated combiner, outphasing.**

I. Introduction

HIGH-EFFICIENCY power amplifiers (PAs) are always desirable in a communication system since it leads to lower operating expense for operators and longer battery life for mobile users. They are difficult to design given the stringent linearity requirement and high peak-to-average power ratios (PAR) of modern communication signals [1]. Although linear PAs are still dominant in today's market, there have been a lot of research on utilizing switched-mode PAs in modern communication systems because of their potential for higher efficiency. Switched-mode PAs [2] offer significantly higher peak efficiency than their linear counterparts but lack support for high-PAR signals. Architectures that allow switched-mode PAs to be used for high-PAR signals can be roughly divided into three categories.

The first category is polar modulation [3], in which the original signal is decomposed into an envelope signal and a phase modulated signal with constant envelope. The phase modulated signal allows the use of switched-mode PA for efficient amplification. The envelope information is reconstructed through modulating the supply [4]–[6], pulse-gating the phase modulated signal [7], or varying number of PA branches being combined [8]. The key challenges with polar modulation includes timing alignment between the phase and envelope paths and efficient dynamic supply design, which are difficult to achieve especially for wideband signals. The second category is pulse-width modulation [9], [10] and delta-sigma modulation [11], in which the original signal is turned into a switching signal with varying pulse width. The key challenges of this approach include how to maintain PA efficiency with random switching sequences and deal with the out-of-band noise generated when reducing the original high-resolution signal into a bit switching stream. Although pulse-width modulation has been used extensively in audio applications, it has limited success in RF applications. The third category, outphasing modulation [12]–[17], also referred to as linear amplification using nonlinear components (LINC), has attracted a lot of attentions recently and shows great potential. In outphasing (see Fig. 1), the high-PAR baseband signal $s(t) = a(t)e^{j\varphi(t)}$ is separated into two constant envelope signals $s_{1,2}(t)$ as

$$s_{1,2}(t) = Ae^{j[\varphi(t)\pm\theta(t)]} \tag{1}$$

where the outphasing angle

$$\theta(t) = \cos^{-1}\left[\frac{a(t)}{(2A)}\right] \tag{2}$$

and the amplitude A is defined as the maximum of $a(t)/2$. The constant envelopes of the two new signals allow the use of switched-mode PAs on each signal. The outputs of the two PAs are then combined together to reconstruct the original signal. The combiner here is critical for achieving desired efficiency and linearity.

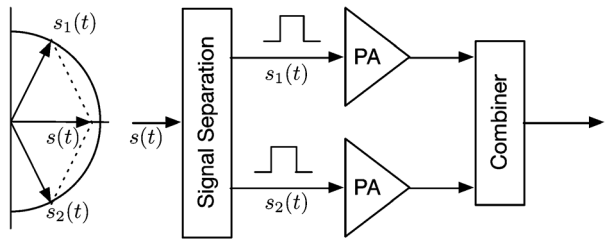


Fig. 1. Outphasing PA architecture.

Manuscript received September 02, 2014; revised December 11, 2014; accepted January 30, 2015. Date of publication March 06, 2015; date of current version April 30, 2015. This paper was approved by Guest Editor Ranjit Gharpurey.

The authors are with Texas Instruments, Dallas, TX 75243 USA (e-mail: ding@ti.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2015.2403316

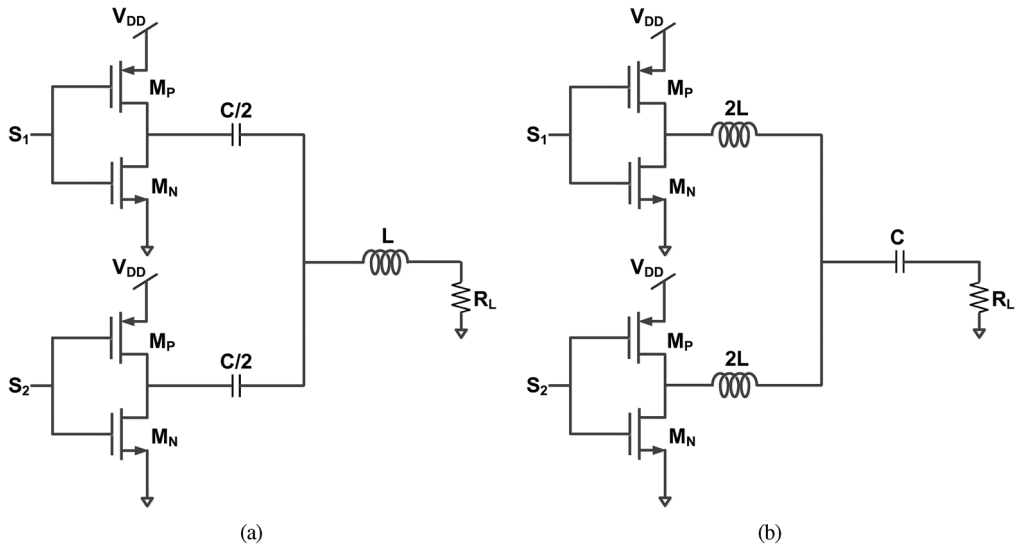


Fig. 2. Proposed combiner: basic configuration. (a) Dual-cap configurationl; (b) dual-inductor configuration.

If an isolated combiner, such as the Wilkinson combiner, is used, the two PAs have less interactions, which results in great linearity. But it leads to low efficiency since the isolation is achieved at the expense of wasted RF power when signals have large phase angles. Multi-level outphasing [14] or asymmetrical outphasing [16], [17] can be applied to reduce the large phase angles, thereby increasing efficiency. But it requires fast and complex supply switching. A non-isolated power combiner, on the other hand, does not create perfect isolation between the two PAs and has reduced power loss. It offers high efficiency but has worse linearity due to interactions of the two PAs, which can be corrected by linearization techniques, such as digital predistortion (DPD). However, despite its efficiency improvement, the conventional non-isolated combiners [18] typically require bulky quarter-wave transmission lines, which are difficult to integrate. Replacing the quarter-wave transmission lines directly with lumped-element equivalent circuits not only requires significant number of components but also increases loss through the network and creates frequency-dependent behavior that limits RF bandwidth.

In this paper, we propose several non-isolated combiners that require very few lumped elements. These combiners explore different behaviors of the combiner circuits for in-phase and out-of-phase operation and allow additional resonance network to be formed in out-of-phase operation. This reduces unnecessary current generation for large phase angles, thereby increasing backoff efficiency of the PA. The performance of the new combiner is demonstrated through a 25 dBm Class-D outphasing PA designed using a standard 45 nm CMOS process.

II. Cross-Bridge Combiners

In this section, we first present two basic lumped element combining networks for outphasing amplifiers. We then propose different ways of adding cross-bridge components to the basic combiners for increasing backoff efficiency and show that additional harmonic rejection and injection networks can be added for further efficiency improvement. Finally, we discuss the tradeoffs in selecting different combiners and compare the proposed combiners with existing combiners in the literature.

A. Basic Combiner Configuration

The purpose of the outphasing combiner is to reconstruct the original modulated RF signal from the summation of two constant envelope phase modulated signals. In addition to provide the sum function, it also needs to be a tuned circuit so as to reject harmonic contents generated by high-efficiency amplifiers, such as Class-D amplifiers. These two functions can be achieved by a simple LC resonant circuit tuned to the carrier frequency $f_c = 1/[2\pi\sqrt{LC}]$ as shown in Fig. 2. The tuned circuit can be arranged in two basic configurations:

(i) Dual capacitors perform the combining operation, and the inductor creates a series resonant circuit with the capacitors at the carrier frequency as shown in Fig. 2(a).

(ii) Dual inductors perform the combining operation, and the capacitor creates a series resonant circuit with the inductors at the carrier frequency as shown in Fig. 2(b).

The operations of the basic combiner can be analyzed in terms of in-phase and out-of-phase components of $s_1(t)$ and $s_2(t)$ signals generated by the PAs. The in-phase components add up at the output and contribute to load power while the out-of-phase components result in power loss. With power backoff, phase angle difference between $s_1(t)$ and $s_2(t)$ increases, which in-turn generates smaller in-phase components and larger out-of-phase components. As a result, the efficiency of the PA drops quickly with power backoff.

B. Bridge Circuit

To improve the overall efficiency of the PA, backoff efficiency has to be increased by reducing current generated by out-of-phase components without affecting in-phase components. This objective can be achieved by adding a bridge circuit between the outputs of the Class-D PAs.

If the basic combiner is designed as in Section II-A(i) with dual capacitors and a series inductor, then a bridge inductor (L-Bridge) can be added between the drains of the PAs as shown

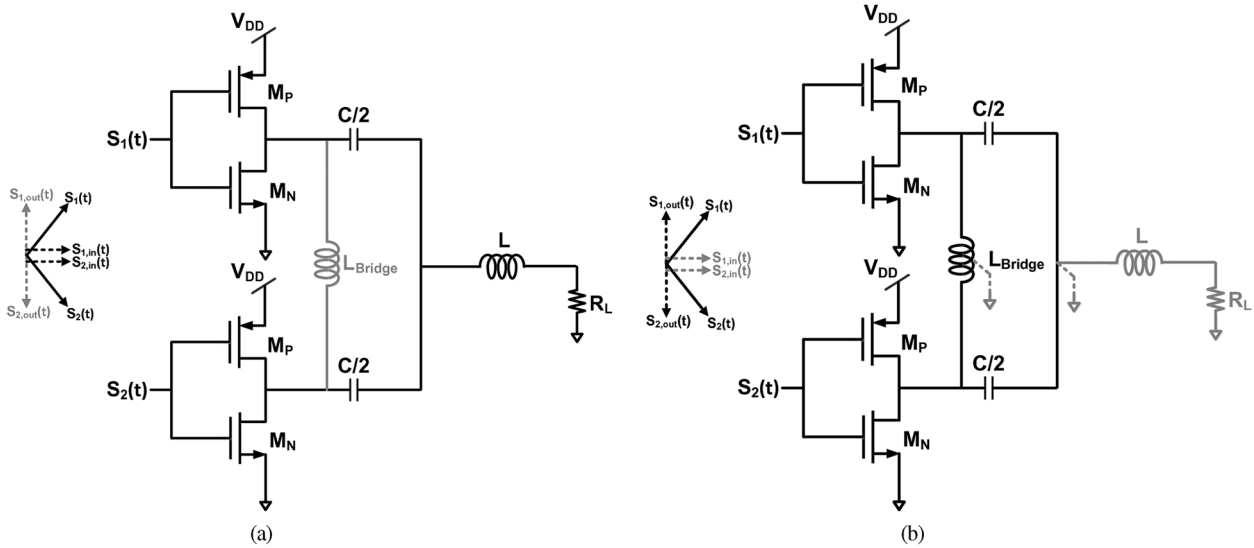


Fig. 3. Proposed combiner with improved backoff efficiency: configuration 1. (a) In-phase mode; (b) out-of-phase mode.

in Fig. 3. The operation of this circuit for in-phase components is shown in Fig. 3(a). The in-phase components generate same voltage waveforms at both sides of the L-Bridge. Since no current flows through the L-Bridge, it does not affect the in-phase components. On the other hand, for out-of-phase components, the summing node, where the inductor is connected with the capacitors, behaves as virtual ground, as shown in Fig. 3(b). The L-Bridge is designed such that it creates a parallel resonant circuit with output parasitic capacitors of the Class-D amplifiers and the capacitors of the combiner at the carrier frequency. This parallel resonant circuit provides a very high impedance and reduces current contribution of the out-of-phase components.

If the combiner is designed as in Section II-A(ii), where dual inductors are used for combining and the capacitor tunes the inductors, the bridge circuit can be designed as inductive or capacitive depending on the residual capacitance or inductance that has to be tuned, respectively, in order to create parallel resonance at the carrier frequency for out-of-phase components. In other words, if the combining inductor dominates the output capacitor of Class-D stages at the frequency of interest for out-of-phase components, then the effective inductance can be tuned with a capacitive bridge. In case the parallel combination of the output capacitor (of Class-D) and the combining inductor looks capacitive at the carrier frequency, then an inductive bridge circuit will be required to create parallel resonance.

Instead of using cross-bridge components, an alternative configuration of the proposed combiner is shown in Fig. 4. In this case, the inductor of the basic combiner is split into multiple inductors. Two inductors are used for combining the outputs of the power amplifiers and perform the same operation of the bridge circuit while the third inductor provides extra inductance needed to create series resonance with the capacitor C. The operation of this alternative configuration for in-phase and out-of-phase components is shown in Fig. 4(a) and (b) respectively. For in-phase components, the three inductors and the capacitor provide series resonance as explained in Section II-A. For out-of-phase components, the node, where the two combining inductors and the capacitor are connected, behaves as a virtual ground, and the combining inductors create parallel resonance circuit with the output capacitance of the Class-D amplifiers and reduce out-of-phase current by providing very high impedance at the carrier frequency. The inductance needed to create the parallel resonance is not same as the inductance needed for the series resonance at the carrier frequency. The extra inductance which may be needed for series resonance is provided by the third inductor.

Similar combiner with bridge circuit [19] can be built with Class-E power amplifiers where the design of the LC combiner becomes different due to the zero voltage switching operation and corresponding loading requirement of Class-E switches.

C. Harmonic Rejection Circuit

In Section II-B, it has been shown how the bridge circuit can create a parallel resonant network to provide very high impedance at the carrier frequency. But the PAs also generate higher harmonics of the carrier frequency at their output due to the Class-D operation. To further improve the backoff efficiency of the PA, out-of-phase current contributions of these higher harmonics have to be reduced. This can be achieved by adding harmonic rejection filters at the outputs of the power amplifiers. For example, LC parallel circuit tuned to the third harmonic of the carrier frequency can be added as shown in Fig. 5 to suppress third harmonic current going to the load. Though this circuit affects both in-phase and out-of-phase components of the signals, it does not hamper the operation of the outphasing PA as the third harmonic signal is undesirable for the in-phase analysis as well. Similarly, higher order harmonic rejection filters can be added to the output of the PAs too. These harmonic rejection filters contribute to further backoff efficiency enhancement of the outphasing PA.

D. Harmonic Injection Circuit

The high-side and low-side switches of the Class-D power amplifiers can be driven by separate switching signals to allow creating dead time between the turn-on time of the high-side switch and low-side switch. This dead time helps to avoid any

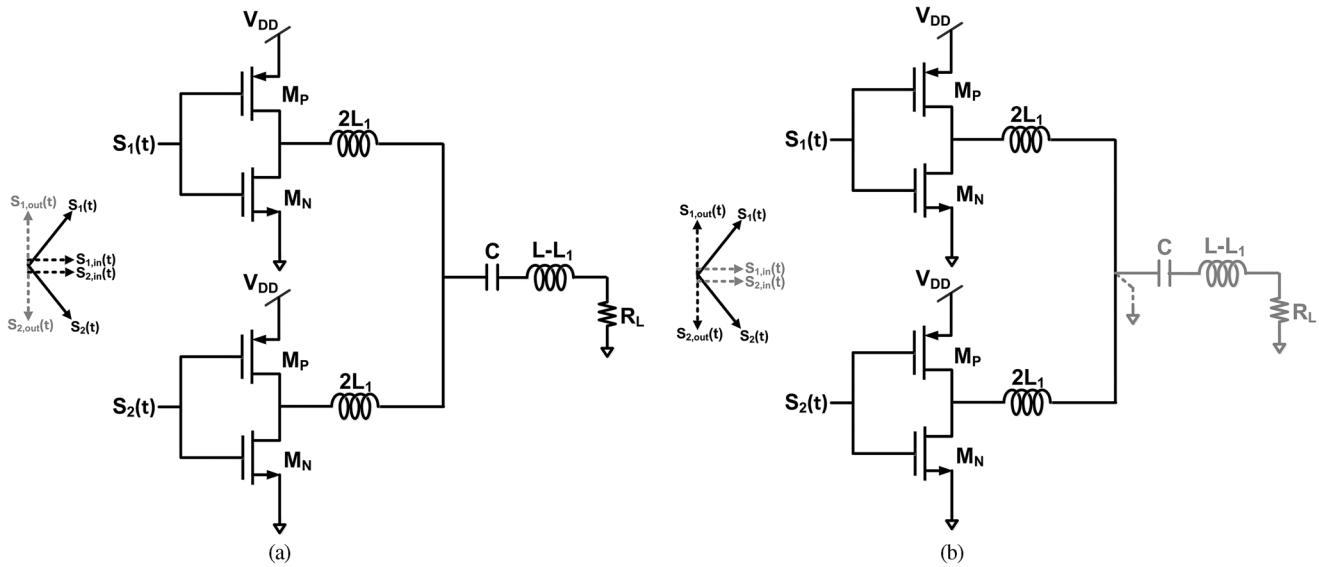


Fig. 4. Proposed combiner with improved backoff efficiency: configuration 2. (a) In-phase mode; (b) out-of-phase mode.

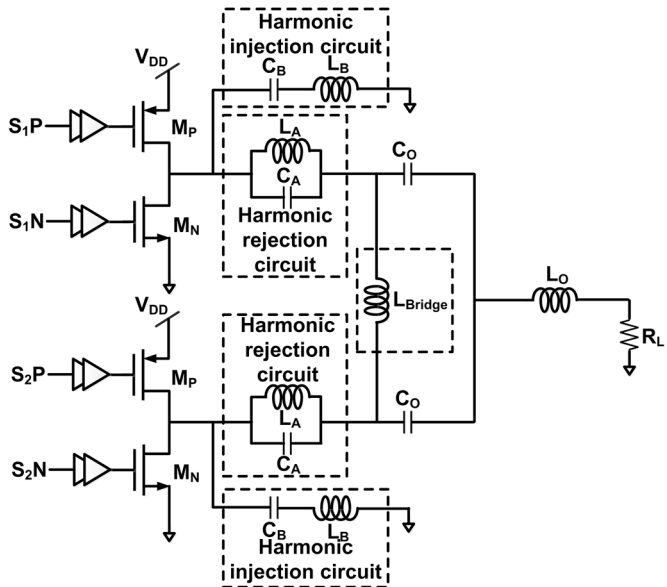


Fig. 5. Proposed combiner with cross-bridge, harmonic injection, and harmonic rejection circuits.

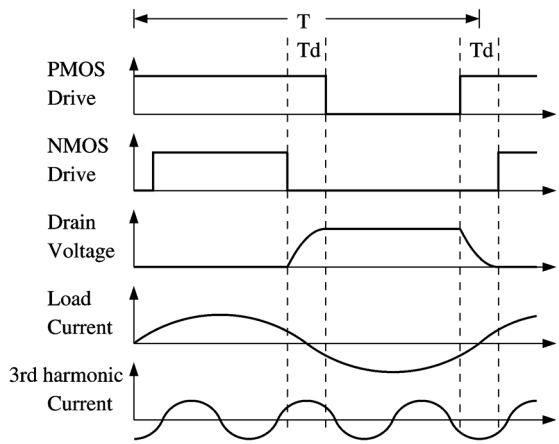


Fig. 6. Time-domain waveform of a Class-D switching stage with a 3rd harmonic network.

direct current path from supply to ground. The output terminal of the Class-D stage becomes a high-impedance node during this dead time. Harmonic injection circuit can be provided at the output of the Class-D stages such that it can inject third or higher order harmonic current during the dead time interval and shape the voltage at the output node. This voltage shaping helps to reduce dynamic switching loss caused by charging and discharging of the output node of the Class-D stages and hence improves the efficiency of the PA. In Fig. 5, this harmonic injection circuit is shown as a series LC circuit tuned to the third harmonic of the carrier frequency. Fig. 6 shows the time-domain switching waveform of a Class-D stage as an example. During the time interval marked as T_d, both NMOS and PMOS transistors are shut off. The load and 3rd harmonic network currents pass through parasitic capacitors associated with the Class-D switching stage. By tuning the 3rd harmonic network, the combined currents shape the drain voltage to the right level before the next switching event.

Drain efficiency (DE) of a Class-D outphasing PA at 900 MHz with different combiners was simulated and is compared in Fig. 7. The simulations were done using off-chip Murata lumped elements and 45 nm devices without layout parasitic extractions. The bottom curve in the figure shows the drain efficiency with an isolated combiner similar to the Wilkinson combiner. It is shown as a baseline for comparison. The middle curve is the simulation result with the proposed cross-bridge combiner. Significant improvement in efficiency compared to isolated combiner is evident from the plot. The top curve in the figure is the simulation result with cross-bridge, harmonic rejection, and harmonic injection circuits. We see that further efficiency imrovement can be achieved by adding harmonic rejection and harmonic injection circuits to the

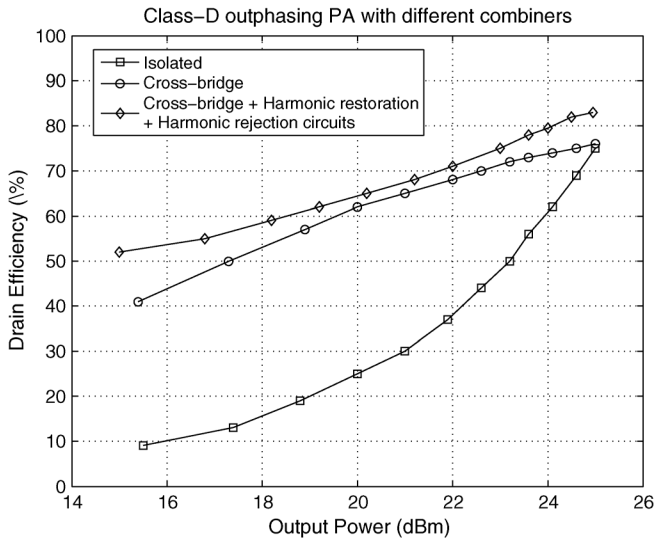


Fig. 7. Drain efficiency comparison of Class-D outphasing PA with different combiners.

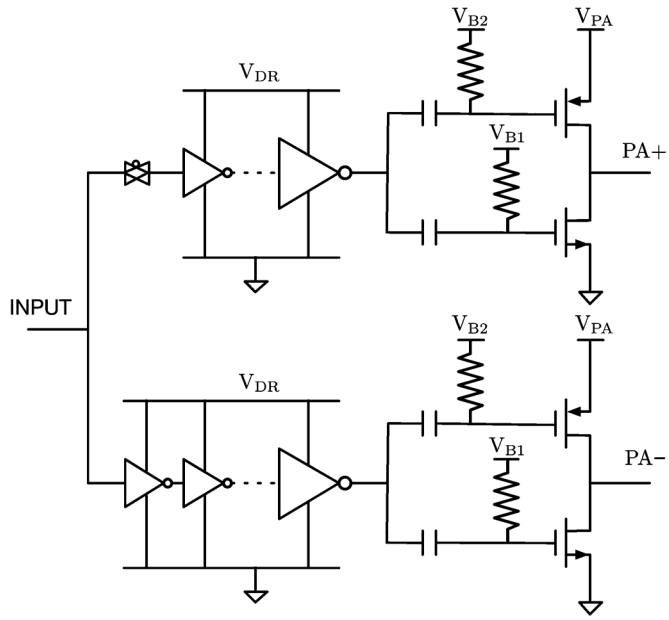


Fig. 8. Simplified schematics of the Class-D PA.

cross-bridge combiner at the expense of increased component counts and complexity.

E. Trade-Offs Among Different Topologies

While different alternative topologies described here perform similar operations, they have different trade-offs in terms of implementation. For example, the combiner in Section II-A(i) with L-bridge has less number of inductors (two inductors) compared to the combiner in II-A(ii) with L-bridge which has three inductors. This makes the former option more desirable for on-chip implementation as this will require smaller silicon area. On the other hand, for off-chip implementation the latter option is better as the combiner inductors can be designed such that the bond-wire inductors can be taken into account, or the whole inductors can be implemented using bond-wires.

F. Comparison With Other Combiners

While isolated combiners can provide very good linearity, backoff efficiency is generally poor due power loss at the isolating resistor. Chireix combiner [18] has been reported in the past, which improves backoff efficiency of the outphasing power amplifier by adding reactive elements at the output of the individual PAs. This technique improves efficiency of the outphasing PA at a certain backoff power level by canceling the reactive loads corresponding to the phase angle required at that power level. On the other hand, the combiner proposed in this paper improves backoff efficiency at all backoff output power levels by operating differently for in-phase and out-of-phase components of the signal.

III. Circuit Design

In this section, we describe implementation details of the Class-D PA and the combiner. The Class-D stages and associated circuits are implemented in silicon while the combiner is implemented using discrete passive components on the printed circuit boards (PCBs).

A. Design of the Test Chip

The Class-D PA and associated circuits including the driver chain are implemented in standard 45 nm CMOS process. Fig. 8 shows a simplified schematic of the Class-D PA test chip. The test chip is designed to generate two differential outputs for one input RF signal, either $s_1(t)$ or $s_2(t)$. The outputs of two test chips are combined together through the proposed combiners to generate the final output (see Fig. 9). For generating the differential signals, one path has one extra inverter in the driver chain. Its delay is balanced in the other path by using a transmission gate, the delay through which can be controlled by adjusting the gate voltages of the NMOS-PMOS pair of the transmission gate. For the final Class-D stages, transistors with minimum gate length are used to achieve the best efficiency and linearity tradeoff. The size of the transistors was optimized to balance the conduction loss associated with the transistor's ON resistance and the switching loss associated with the transistor's capacitance. Increasing transistor size reduces ON resistance of a transistor but increases its capacitance. A tradeoff has to be made to reduce overall loss. The final stage of the PA operates from 1.7 V supply to reach peak output power level around 25 dBm. To verify the reliability of the design, we simulated with 20% higher voltage and confirmed that there is no gate oxide breakdown possibility in our design. We also confirmed in simulation there is not significant performance drop from HCI and NBTI with 20% higher supply voltage after 10 years of operation. Each driver chain of the Class-D PA has multiple stages and operates from a 1.2 V supply. The outputs of the driver are level-shifted using a simple RC network to allow flexibility in PA testing. The nominal biasing voltage for the NMOS input is 0.6 V. For the PMOS input, it is 1 V. The driver chains are designed to accept small input signals, such as -10 dBm. A chip micrograph of the Class-D PA die is shown in Fig. 10. The die area of the test chip is 1.1 mm $\times$ 1.1 mm, which is mostly determined by the number of pads required

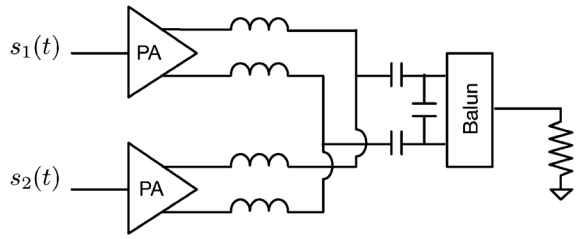


Fig. 9. Simplified diagram of the board setup with the PA test chips and the proposed combiner.

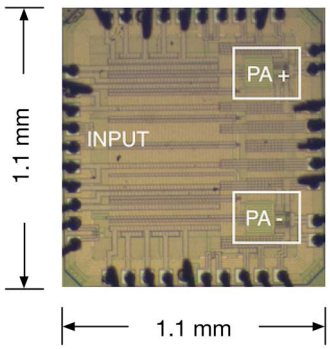


Fig. 10. Die photo of the Class-D PA test chip.

while the area occupied by the PA (including PA+ and PA- in Fig. 10) is 0.3 mm $\times$ 0.4 mm.

B. Design of the PCB

A 6-layer printed circuit board is designed, and the test chip is directly wirebonded on the PCB. The combiner with alternative configuration shown in Fig. 4 is implemented on the PCB using discrete passive components. The combiner is implemented on the board and not on the chip so that different versions of the combiner can be built tuned at different frequencies and performance of the PA can be measured at those frequencies using the same test chip. A picture of the implemented PCB is shown in Fig. 11. One of the challenges in switched-mode PAs is the supply and ground noise contributed by supply and ground bondwire inductances during switching current. This type of supply and ground bounce effect increases the noise floor and degrades the adjacent channel power ratio (ACPR) performance. Differential implementation of the PA helps to reduce this noise to certain extent. Further noise suppression is done by placing on-chip and on-board decoupling capacitors. Decoupling capacitors in a very small package size are placed very close to the test chip to reduce the effects of inductances of the supply and ground board traces. On the RF output side, the discrete components of the combiner are placed as compactly as possible to reduce parasitics. Parasitics coming from the signal traces are estimated, and the values of the discrete components are adjusted accordingly. Two set of PCB boards are designed and tested. The first set operates at 900 MHz with a TDK HHM1776B3 balun. The second set operates at 2.4 GHz with a TDK HHM1902B1 balun.

The output capacitor immediately before the balun in Fig. 9 is used for the purpose of load impedance transformation. To obtain higher output power from the Class-D PA without changing the supply voltage, the 50 ohm load impedance is transformed to a lower value at the output of the Class-D stages. As power loss increases with higher transformation ratio, the component values are determined to obtain optimal output power and efficiency.

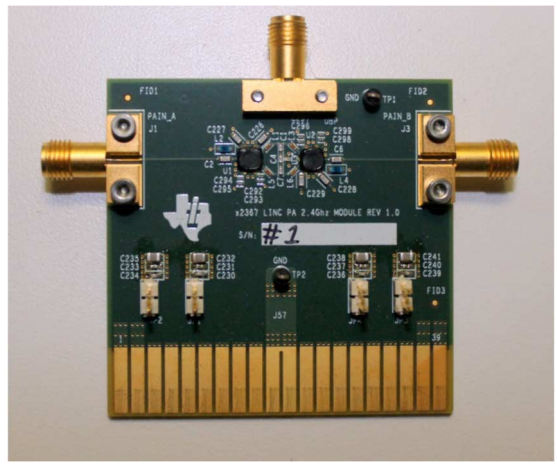


Fig. 11. Printed circuit board of the Class-D outphasing PA.

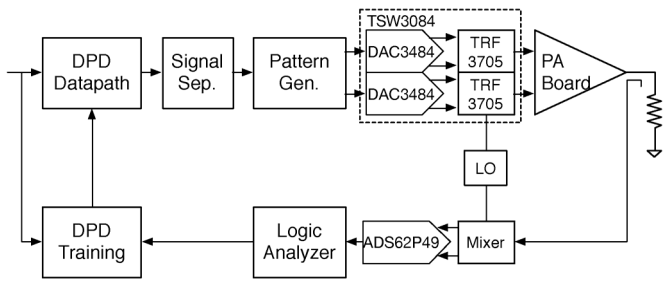


Fig. 12. Diagram of measurement setup.

IV. Measurement Results

A diagram of the measurement setup is shown in Fig. 12. It can be configured to perform both PA characterization and DPD. For PA characterization, the DPD datapath and feedback path are not active. The signal separation is done in Matlab on a PC. The data is then downloaded to a pattern generator and played out continuously to a dual-RF channel TSW3084 board with a DAC3484 running at 307.2 MHz. The DAC output is centered around a digital IF frequency of -153.6 MHz and IQ modulated with a local oscillator (LO) signal to generate final desired RF signal at 900 MHz or 2.4 GHz. The digital IF frequency is selected to avoid IQ image and LO leakage from the IQ mixing falling into the band of interest. However, these distortions can be calibrated out if they do become an issue in overall system design. When DPD is enabled, the DPD datapath and training is also done in Matlab on the PC before outphasing signal separation. The feedback path for DPD training is composed of an IQ demodulator, an ADS62P49, and a logic analyzer. The DPD datapath runs at the DAC rate of 307.2 MHz while the ADC in the complex IQ feedback path runs at 153.6 MHz. The mismatch between the DPD and ADC rates is handled by the subsampling algorithm developed in [20].

TABLE I
OUTPHASING PA COMPARISON

	Power combiner	Peak eff	6dB backoff eff	$\frac{\text{6dB backoff eff}}{\text{peak eff}}$	Technology	Frequency
[15]	Wilkinson w/ $\lambda/4$ lines	50%	12%	24%	0.18um	700 MHz
[18]	Chireix w/ $\lambda/4$ lines	60% (DE)	35% (DE)	58 %	0.18um	800 MHz
[24]	Transformer	35%	21%	60%	32nm	2.4 GHz
This work	Simple lumped elements	55%	32%	58%	45nm	900 MHz

* Efficiency shown is power-added efficiency except for [18], which is drain efficiency.

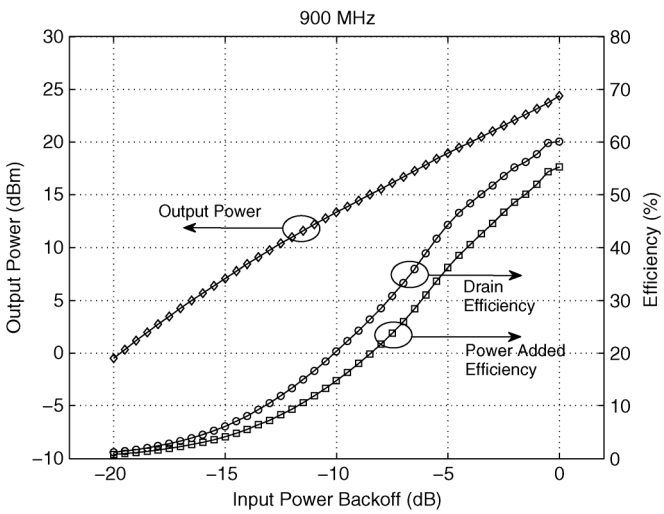


Fig. 13. Measured output power, drain efficiency, and power-added efficiency vs. input power backoff at 900 MHz.

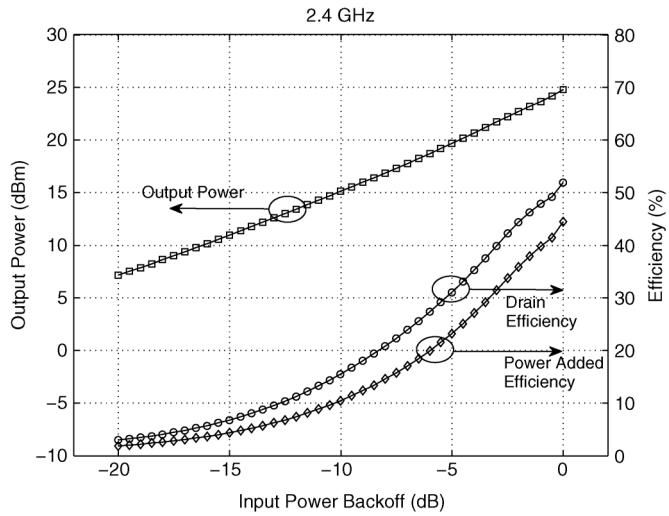


Fig. 14. Measured output power, drain efficiency, and power added efficiency vs. input power backoff at 2.4 GHz.

For a single tone input with different backoff power levels, the measured output power, drain efficiency (DE) of the final PA stage, and power-added efficiency (PAE) of the entire PA are shown in Fig. 13 for 900 MHz and in Fig. 14 for 2.4 GHz. Note that since this is a switched-mode PA, the input power backoff is achieved not by reducing the input signal power but by changing the outphasing angle of the two outphased input signals based on (1). As input power backoff reduces, the PA output power increases fairly linearly both in the 900 MHz and 2.4 GHz cases despite the non-isolated nature of the combiner and Class-D operation of the PA switching stages. At 900 MHz, the PA achieves 55% PAE at peak output power of 24.4 dBm for a single tone input. At 2.4 GHz, the PAE is 45% at 24.9 dBm. In addition to the high peak efficiency, the efficiency rolls off slower at backoff when compared with linear PAs or outphasing PAs with isolated combiners. For a 10 MHz LTE signal with 6 dB PAR, the PAE of the PA is 32% at 900 MHz with -39 dBc ACPR and 22% at 2.4 GHz with -33 dBc ACPR. For these measurements, the loss of the combiner was de-embedded to understand the performance of the PA itself without being affected by the Q factors of the lumped elements used in the combiner. The decrease of efficiency from 900 MHz to 2.4 GHz is primarily due to increased switching loss. Both the driver and final stages of the PA were designed to support broad band operation. Better performance can be achieved by optimizing the PA to a narrow range of carrier frequencies.

Table I compares the performance of the outphasing PA presented in this paper with other state-of-the-art outphasing PA designs. The presented PA achieves good efficiency with compact combiner based on lumped elements. In the table, we also added a column showing the ratio between 6 dB backoff power efficiency and peak efficiency. This ratio is a good metric for evaluating how the PA's peak efficiency is maintained at backoff power levels. As expected, non-isolated combiners used in [18], [24], and this work maintain peak efficiency much better at 6 dB backoff than isolated combiners used in [15].

The spectra of the PA before DPD is shown in Figs. 15 (900 MHz) and 16 (2.4 GHz) for a 10 MHz LTE signal. Please note that only ACPR numbers in Figs. 15–19 are accurate. The absolute carrier power readings in the figures were not calibrated to reflect power loss through couplers and cables. The absolute powers reported in the paper were measured using calibrated power meters. There are several sources contributing to the nonlinear behavior of the PA. The first one is the non-isolated nature of the combiner, which causes signal-dependent interactions between the two Class-D PAs. The second one is ground and supply bounces caused by high supply current flowing from switching activities of the Class-D stages and the associated $L(di/dt)$ from supply and ground bond wires. Differential implementation of PA and careful design of the on-chip decoupling capacitors help to reduce this signal dependent noise in supply and ground. Packages that minimizes supply and ground bond wire inductance are also critical for

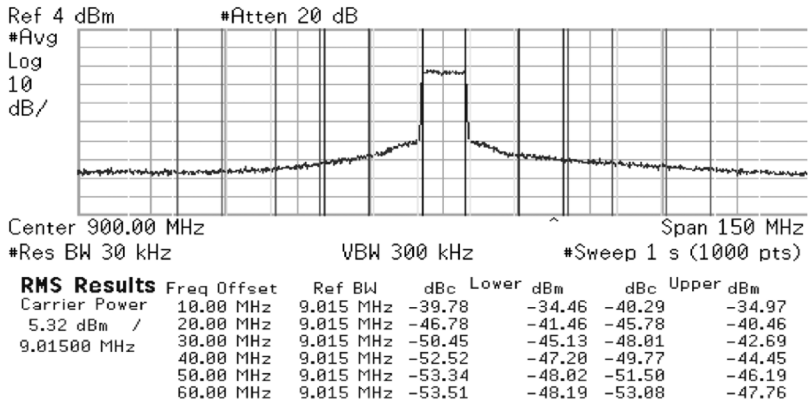


Fig. 15. PA output spectrum for 10 MHz LTE at 900 MHz without DPD.

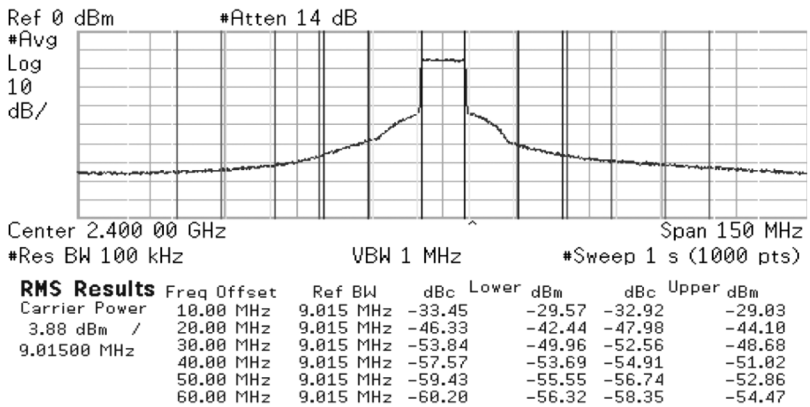


Fig. 16. PA output spectrum for 10 MHz LTE at 2.4 GHz without DPD.

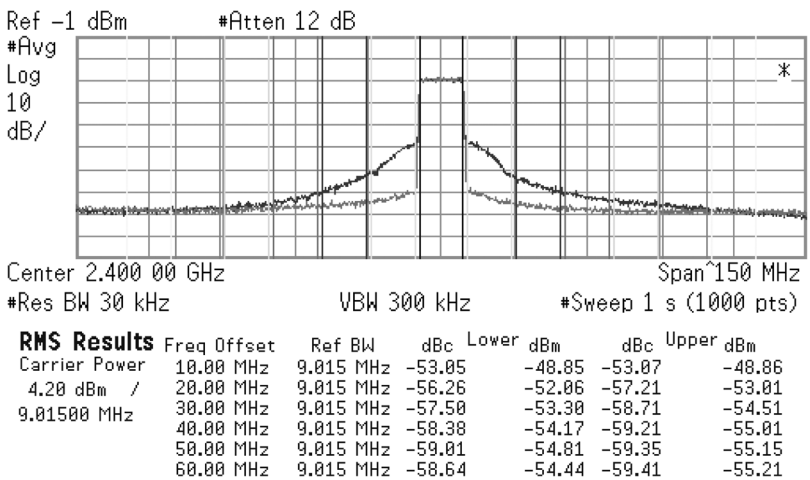


Fig. 17. PA output spectrum for 10 MHz LTE at 2.4 GHz with and without DPD.

reaching desired linearity requirements in commercial products. Another source that contributes to the PA nonlinearity is the amplitude and delay mismatches between the two outphasing branches. Calibration techniques, such as those presented in [21] and [22], have to be used to minimize these mismatches.

With DPD, the linearity of the PA is improved significantly. The spectra of the PA after DPD is shown in Figs. 17, 18, and 19 for 10 MHz, 20 MHz, and 2-carrier 20 MHz LTE signals, respectively, at 2.4 GHz carrier frequency. After DPD, the ACPR measurements at the adjacent carrier offset reach -53 dBc, -50 dBc, and -42 dBc for 10 MHz, 20 MHz, and 2-carrier 20 MHz LTE signals, respectively. The DPD models applied in this measurement is 3-tap simplified Volterra model similar to the one presented in [23]. We found that cross terms in the model is also beneficial to linearize outphasing PAs and provides additional 3–4 dB ACPR improvements comparing with models without cross terms for the 2-carrier 20 MHz LTE signal. The benefit of using cross terms is less for the signals with less signal bandwidth. Note that the linearization performance for wideband signals is partially limited by the

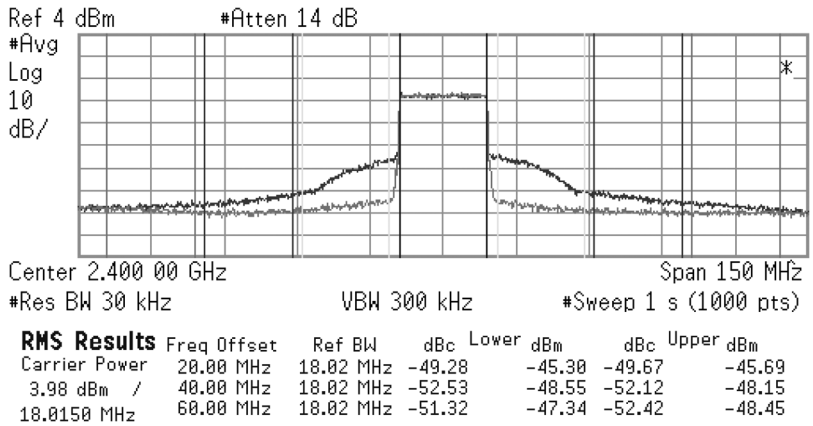


Fig. 18. PA output spectrum for 20 MHz LTE at 2.4 GHz with and without DPD.

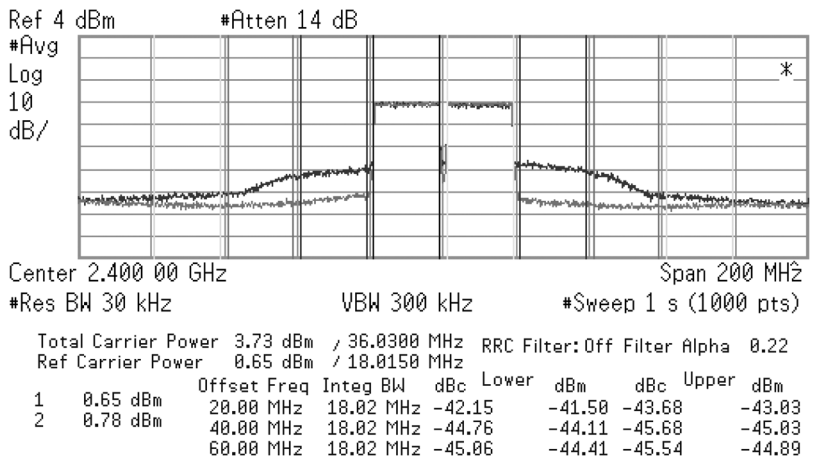


Fig. 19. PA output spectrum for 2-carrier 20 MHz LTE at 2.4 GHz with and without DPD.

bandwidth of the DAC3484, which is 307.2 MHz in our setup, given typical 5 to 10× bandwidth expansion during outphasing signal separation. Interestingly, we see that linearity improvement extending to a 180 MHz band for the 2-carrier LTE signal despite the bandwidth constraint.

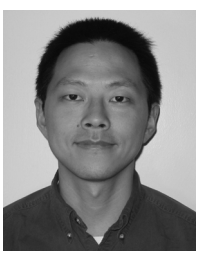
V. Conclusions

This paper presents a 45 nm Class-D outphasing PA with cross-bridge combiners. The cross-bridge configuration allows additional resonance networks to be formed for reducing outphasing current in the combiner, thereby increasing the PA efficiency at backoff. Further efficiency improvement can be obtained by additional harmonic rejection and injection networks. Implementation details and measurement results are presented at both 900 MHz and 2.4 GHz. The results demonstrated excellent linearity and efficiency of the Class-D PA with the proposed combiner. With DPD, the linearity of the PA can be significantly improved over a very wide bandwidth.

References

[1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Boston, MA, USA: Artech House, Jan. 2006.
[2] A. Grebennikov, N. O. Sokal, and M. J. Franco, *Switchmode RF and Microwave Power Amplifiers*. New York, NY, USA: Academic Press, 2012.
[3] P. Reynaert, "Polar modulation," *IEEE Microw. Mag.*, vol. 12, no. 1, pp. 46–51, 2011.
[4] L. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952.
[5] J.-H. Chen, K. U-yen, and J. Stevenson Kenney, "An envelope elimination and restoration power amplifier using a CMOS dynamic power supply circuit," in *Proc. IEEE Int. Microw. Symp.*, 2004, vol. 3, pp. 1519–1522.
[6] F. Wang *et al.*, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4086–4099, Dec. 2006.
[7] J.-H. Chen, H.-S. Yang, H.-C. Lin, and Y.-J. Chen, "A polar-transmitter architecture using multiphase pulsewidth modulation," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 2, pp. 244–252, Feb. 2011.
[8] S.-M. Yoo, J. Walling, E.-C. Woo, B. Jann, and D. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.
[9] J. Walling *et al.*, "A Class-E PA with pulse-width and pulse-position modulation in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1668–1678, Jun. 2009.
[10] J. Lu and R. Gharpurey, "Phase-locked loop based PWM wireless transmitter," in *Proc. IEEE Int. Symp. Circuits Syst., ISCAS*, 2013, pp. 177–180.
[11] T.-P. Hung, J. Rode, L. Larson, and P. Asbeck, "Design of H-bridge Class-D power amplifiers for digital pulse modulation transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2845–2855, Dec. 2007.
[12] H. Chireix, "High power outphasing modulation," *Proc. IRE*, vol. 23, pp. 1370–1392, 1935.
[13] D. Cox, "Linear amplification with nonlinear components," *IEEE Trans. Commun.*, vol. COM-22, no. 12, pp. 1942–1945, 1974.

[14] K.-Y. Jheng, Y.-J. Chen, and A.-Y. Wu, "Multilevel LINC system designs for power efficiency enhancement of transmitters," *IEEE J. Sel. Topics Signal Process.*, vol. 3, no. 3, pp. 523–532, 2009.
[15] J. Hur, O. Lee, C.-H. Lee, K. Lim, and J. Laskar, "A multi-level and multi-band Class-D CMOS power amplifier for the LINC system in the cognitive radio application," *IEEE Microw. Compon. Lett.*, vol. 20, no. 6, pp. 352–354, Jun. 2010.
[16] J. Hur, O. Lee, K. Kim, K. Lim, and J. Laskar, "Highly efficient uneven multi-level linc transmitter," *Electron. Lett.*, vol. 45, no. 16, pp. 837–838, 2009.
[17] P. A. Godoy, S. W. Chung, T. W. Barton, D. J. Perreault, and J. L. Dawson, "A 2.5-GHz asymmetric multilevel outphasing power amplifier in 65-nm CMOS," presented at the IEEE Radio Wireless Conf., Jan. 2011.
[18] T.-P. Hung, D. Choi, L. Larson, and P. Asbeck, "CMOS outphasing Class-D amplifier with Chireix combiner," *IEEE Microw. Compon. Lett.*, vol. 17, no. 8, pp. 619–621, 2007.
[19] A. Banerjee, R. Hezar, L. Ding, N. Schemm, and B. Haroun, "A 29.5 dBm Class-E outphasing RF power amplifier with performance enhancement circuits in 45 nm CMOS," in *Proc. 40th European Solid State Circuits Conf. (ESSCIRC 2014)*, Sep. 22–26, 2014, pp. 467–470.
[20] L. Ding, F. Mujica, and Z. Yang, "Digital predistortion using direct learning with reduced bandwidth feedback," in *Proc. IEEE Int. Microw. Symp.*, 2013, pp. 1–3.
[21] X. Zhang, L. Larson, P. Asbeck, and P. Nanawa, "Gain/phase imbalance-minimization techniques for LINC transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 12, pp. 2507–2516, Dec. 2001.
[22] J. Hur, H. Kim, O. Lee, K.-W. Kim, K. Lim, and F. Bien, "An amplitude and phase mismatches calibration technique for the LINC transmitter with unbalanced phase control," *IEEE Trans. Veh. Technol.*, vol. 60, no. 9, pp. 4184–4193, 2011.
[23] D. Morgan, Z. Ma, J. Kim, M. Zierdt, and J. Pastalan, "A generalized memory polynomial model for digital predistortion of RF power amplifiers," *IEEE Trans. Signal Process.*, vol. 54, no. 10, pp. 3852–3860, Oct. 2006.
[24] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. El-Tanani, and K. Soumyanath, "A flip-chip-packaged 25.3 dBm Class-D outphasing power amplifier in 32 nm CMOS for WLAN application," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596–1605, Jul. 2011.



Lei Ding (S'01–M'05) received the B.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1997, the M.S. degree in biomedical engineering from the University of Alabama at Birmingham, AL, USA, in 2000. In 2004, he received the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA.

He is currently a Systems Engineer with the Embedded Processing Systems Lab, Texas Instruments, Dallas, TX, USA, working in the area of signal processing design and implementation for RF and analog systems. He was a Digital Design Engineer with Cirrus Logic, Austin, TX, USA, designing low-power audio data converters from 2004 to 2008. During the summers of 2001 and 2002, he worked as an intern at the Wireless Research Laboratory, Bell Laboratories, Lucent Technologies.

Joonhoi Hur (S'07–M'11) received the B.S. degree in electrical engineering from Korea University, Seoul, Korea, in 2002. From 2002 to 2005, he worked at WinTelecom in Seoul, Korea, where he was involved in wireless network systems design. In 2006, he joined the Microwave Applications Group (MAG) at the Georgia Institute of Technology, Atlanta, GA, USA. He was the recipient of the Korean government scholarship program for graduate studies. He received the M.S. and Ph.D. degrees in electrical and computer engineering from Georgia Institute of Technology in 2008 and 2010, respectively.

In the summer of 2010, he worked as a system engineer in Texas Instruments, Dallas, TX, USA. From January 2011 to March 2013, he worked as an RF/Analog IC designer in Kilby Labs Research Center, Texas Instruments, Dallas. Currently he is working at Qualcomm Technology, San Diego, CA, USA. His research interests include RF/analog circuits and systems.

Aritra Banerjee (S'10–M'14) received the B.E. degree in electronics and telecommunication engineering from Jadavpur University, Kolkata, India, in 2009 and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2011 and 2013, respectively.

He joined Kilby Labs of Texas Instruments, Dallas, TX, USA, in 2013 as an Analog and RF Design Engineer and he is currently working on switched-mode CMOS RF power amplifier and integrated RF transceiver design. Previously, he held internship positions with the Kilby Labs of Texas Instruments, Dallas, in 2011 and 2012. He has published more than 40 international conference and journal papers and has four patents pending. His research interests include high-efficiency, low-power mixed-signal and RF circuits and systems design, and nanoelectronics.

Dr. Banerjee was a recipient of the IEEE Microwave Theory and Techniques Society Graduate Fellowship in 2012 and the IEEE Circuits and Systems Society Student Travel Award in 2013.

Rahmi Hezar received the B.Sc. degree in electrical and electronics engineering from Bogazici University, Istanbul, Turkey, in 1993. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 1994 and 2000, respectively, with specialization in digital signal processing.

He joined Texas Instruments Wireless Business Unit, Dallas, TX, USA, in 2000, initially working to develop DSP cores for cellular phones. He later became part of the first CMOS analog mixed signal integration team in TI where he developed high-speed ADC and DAC architectures for a variety of applications ranging from radio to audio. He is now part of the TI Kilby Labs' team of researchers working on digital transmitters and power amplifiers, and most recently he has been focusing on EMI/EMC mitigation in power management circuits and systems. Dr. Hezar's expertise is in continuous-time sigma-delta ADCs/DACs, power amplifiers, power management systems, mixed-signal processing, system design and modeling. He holds 27 U.S. patents and has 20 IEEE conference/journal publications in related fields.

Baher Haroun (F'10) received the Bachelor and Master degrees in electrical engineering from Ain Shams University, Egypt, and the Ph.D. degree from the University of Waterloo, Ontario, Canada, in 1990.

He is a senior fellow at Texas Instruments (TI) in Dallas, TX, USA. He manages the Embedded Processing Systems Labs in the EP Business Unit at TI. He joined Texas Instruments in 1995. He later managed technical teams to integrate Rf, analog and mixed-signal modules into digital CMOS in TI's wireless business unit. He has also led multiple teams at Kilby Labs on mmWave/sub-Thz systems, advanced ADCs and RF signal paths. Prior to joining TI, he was an Assistant and Associate Professor of electrical and computer engineering at Concordia University, Montreal, Quebec, Canada. He has over 40 published presentations and papers, and over 80 patents to his credit. He is interested in research areas such as THz signal paths, ultra-low power and low-voltage mixed-signal wireless ICs, GHz serial interfaces, and embedded processing system architectures.