# A Fully Integrated Dual-Mode CMOS Power Amplifier With an Autotransformer-Based Parallel Combining Transformer

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***Abstract*— This letter presents a fully integrated dual-mode power amplifier (PA) with an autotransformer-based parallel combining transformer (ABPCT), fabricated with a standard 40-nm CMOS process. In comparison with a parallel combining transformer, the proposed ABPCT can offer high-efficiency performance in both high-power (HP) and low-power (LP) modes, and does so with a compact die area. With an 802.11g signal (64-QAM 54 Mbps) of 20-MHz channel bandwidth, the fully integrated dual-mode PA achieves 19.7 and 15.7 dBm average output powers with PAEs of 17.1% and 13%, in HP and LP modes, respectively, while satisfying a −25 dB error vector magnitude and spectral mask requirements. Operating the PA in the LP mode can save more than 40% of the current consumption at a 10-dBm average output power when compared with that in the HP mode.**

***Index Terms*— CMOS technology, dual-mode power control, high efficiency, power amplifier (PA), power combining transformer, WLAN.**

## I. Introduction

THE explosive growth in demand for low-cost, small-size mobile devices has fostered much research on single-chip RF transceiver design. The efficiency performance of the power amplifier (PA) in the low-output power region is much more important than that in the high-output power region, because the PAs operate in this low-output power region during most of the time [1]. To improve the efficiency at low-output power region, several methods for multimode operation have been introduced. In the transistor resizing method [2], [3], a PA adopts reduced size power devices to improve efficiency in the low-power (LP) mode. In addition, a tunable matching method has been introduced to provide optimum loads at each operation mode [2], [4]. Multimode operation using power combining transformers has also been introduced. Series combining transformers (SCTs) or parallel combining transformers (PCTs) have been used in multimode operations [2], [5], [6]. In this method, multiple individual amplifiers are connected to multiple primary windings, and each individual amplifier is separately controlled for operation in the different modes. In addition, CMOS PAs with an autotransformer or a modified autotransformer have recently been proposed as a means to improve efficiency with a compact die area [7], [8].

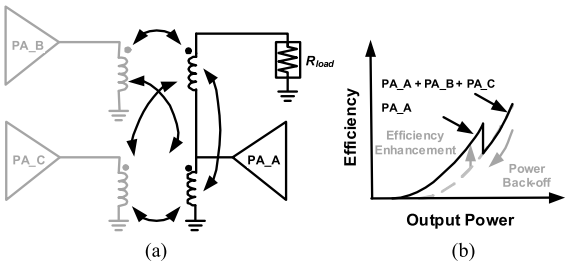


Fig. 1. (a) Discrete power control scheme with ABPCT. (b) Efficiency versus output power with discrete power control using ABPCT.

In this letter, we propose a dual-mode CMOS PA with an autotransformer-based PCT (ABPCT). In the proposed transformer, a PCT is constructed based on an autotransformer to improve efficiency in both LP and high-power (HP) modes.

## II. Dual-Mode CMOS PA With Autotransformer-Based PCT

Fig. 1 shows the circuit diagram of the proposed ABPCT and its operation for discrete power control. In the proposed ABPCT, one individual amplifier, PA_A, is connected to a part of the secondary winding unlike a PCT, so that the secondary winding itself acts as an autotransformer. The other individual amplifiers, PA_B and PA_C, are connected to multiple primary windings, as in typical PCT. In the HP mode, all individual amplifiers (PA_A, PA_B, and PA_C) are enabled. In the LP mode, one or two individual amplifiers can be selectively enabled among the three. In this letter, only PA_A, which is connected to the autotransformer part, is enabled in the LP mode. The SCT arrangement is typically lager in size than the PCT for an equivalent number of combined individual amplifiers; therefore, the die area required for a multimode PA using SCT is relatively larger than that using PCT. In addition, the size of the ABPCT can be smaller than that of the PCT arrangement, because an additional primary winding is not required for combining the power from PA_A. Fig. 2 shows example layouts of PCT and ABPCT for the differential case. In Fig. 2, the PCT and ABPCT sizes are, respectively, 0.723 mm × 0.560 mm and 0.643 mm × 0.443 mm. The transformers are designed with a

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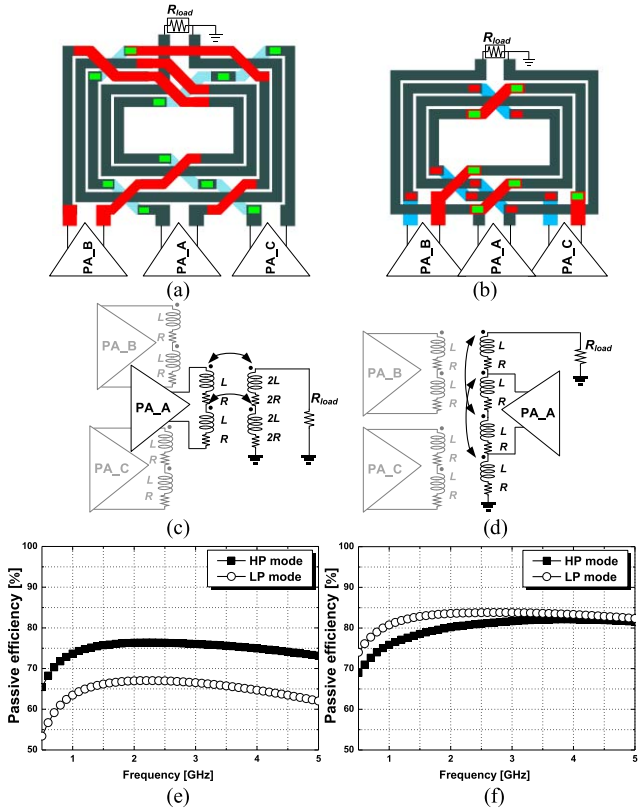


Fig. 2. Layout of (a) PCT and (b) ABPCT. Equivalent lumped element models of (c) PCT and (d) ABPCT. Simulated passive efficiency characteristics in LP and HP modes of (e) PCT and (f) ABPCT.

3.4-$\mu$m-thick $Cu$ top metal layer, a 30-$\mu$m width, and 10-$\mu$m spacing. Electromagnetic simulations are performed using ADS momentum. Fig. 2(c) and (d) shows the equivalent lumped element models for differential PCT and ABPCT. Fig. 2 also shows the simulated passive efficiency performances of both PCT and ABPCT in dual-mode operation. In the HP mode, all three transformer inputs are enabled. In the LP mode, only the transformer input relative to PA_A is enabled. With the PCT structure, passive efficiencies of 76.1% and 66.8% are obtained in HP and LP modes, respectively, at 1.75 GHz. The minimum insertion loss, which is the inverse of the maximum available gain, has been used to evaluate the passive efficiency [9]. On the other hand, with the proposed ABPCT structure, passive efficiencies of 79.6% and 83.3% are, respectively, obtained in HP and LP modes, for the same operating frequency. The lumped element models also show similar characteristics (PCT: 85% at HP mode, 75.6% at LP mode, ABPCT: 86.8% at HP mode, 89.6% at LP mode, assuming $L = 1$ nH, $R = 1\ \Omega$ (i.e., $Q = 11$), and $k = 0.7$ at 1.75 GHz). In general, autotransformers offer lower power losses than two-winding transformers, because the primary winding in an autotransformer serves as a part of the secondary one, thus reducing the total series resistance [7]. Because PA_A in the ABPCT structure is connected to the autotransformer and is always enabled in both LP and HP modes, both modes achieve high-efficiency performances, as shown in Fig. 2. Fig. 3 shows the schematic of the dual-mode PA. Each individual amplifier includes an input transformer as the input matching network. The three amplifiers (PA_A, PA_B, and PA_C) are applied to ABPCT as an output matching

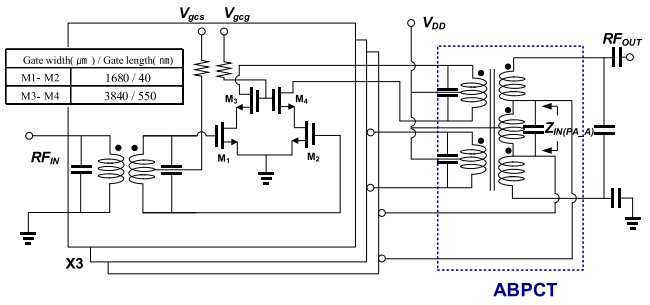


Fig. 3. Total schematic of the designed CMOS PA.

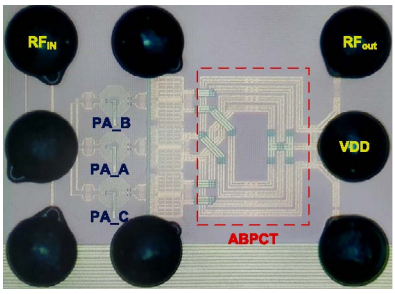


Fig. 4. Microphotograph of the fully integrated proposed CMOS PA.

network. All individual amplifiers share a single VDD ball, because the center taps of the transformer for each individual amplifier are combined together. In the design of each individual amplifier, the thick-oxide 0.55-$\mu$m device for the common gate (CG) stage and thin-oxide 40-nm device for the common source (CS) stage are stacked in the cascode stage to reduce the voltage stress of each device. The simulated load impedances looking from PA_A amplifier ($Z_{\mathrm{IN(PA\_A)}}$ in Fig. 3) are $11.5+j40.6$ and $4.8+j17$ at HP and LP modes, respectively. For selection of the LP and HP modes, the gate bias of the individual amplifiers is controlled. In addition, the gate bias of the PA_A amplifier is decreased from class AB to deep class AB to further reduce current consumption in the LP mode.

## III. Measurement Results

A fully integrated one-stage CMOS PA was fabricated using a standard 40-nm CMOS process with wafer-level package (WLP) technology. Fig. 4 shows a die photograph of the dual-mode PA. The size of the chip is $1.6\times1.6$ mm$^2$, including the input and output transformers, so that additional off-chip matching elements are not required. Four additional WLP balls were added to apply $V_{\mathrm{gcs}}$ and $V_{\mathrm{gcg}}$ bias voltages of each individual amplifier. During the characterization, the losses of the printed circuit board lines were carefully deembedded, but the loss from WLP balls and voltage drops of the bias cable were included in the measurement results. Fig. 5 shows the power gains and power added efficiencies (PAEs) of both HP and LP modes with a 1.75-GHz single-tone continuous wave (CW). For dual-mode operation, power control is performed according to the output power. With a 2.8-V supply, the PA in the HP mode (PA_A + PA_B + PA_C) achieves a 12.4-dB power gain; in the LP mode (PA_A only), it achieves a 5.9-dB power gain. If a driver stage is included, gain can greatly be improved. The saturated output powers, $P_{\mathrm{SAT}}$, are 26.8 and 24.7 dBm for the HP and LP modes, respectively. The peak PAEs for the HP and LP modes are 34.4% and 38.1%, respectively. The peak PAE of the LP mode is higher than that

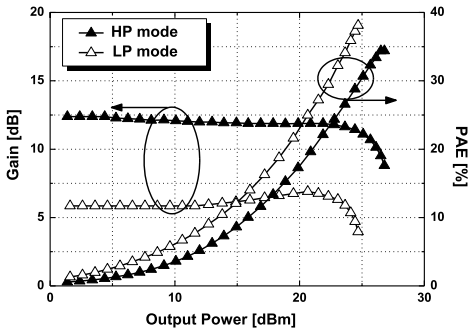


Fig. 5. Measured gain and PAE versus output power; 1.75-GHz CW signal.

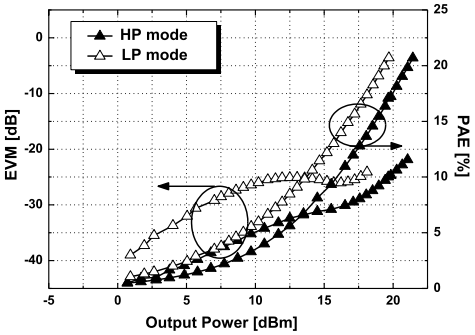


Fig. 6. Measured EVM and PAE versus output power; 802.11g WLAN, 54 Mbps, 64-QAM, OFDM signal.

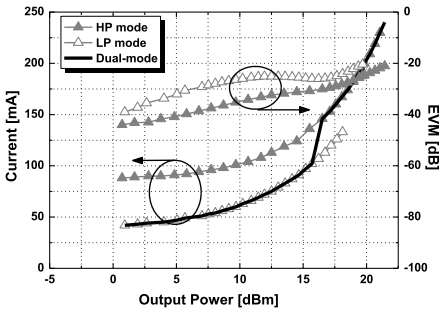


Fig. 7. Measured EVM and current versus output power; 802.11g WLAN, 54 Mbps, 64-QAM, OFDM signal.

of the HP mode because the passive efficiency is higher in the LP mode than in the HP mode. To evaluate the linearity performance, the PA was measured with WLAN 802.11g, 54 Mbps, 64-QAM, and OFDM [error vector magnitude (EVM) limit $< -25$ dB] signals at 1.75 GHz. Fig. 6 shows the measured EVM and PAE versus output power. The PA in the HP and LP modes achieves output powers of 19.7 and 15.7 dBm with PAEs of 17.1% and 13%, respectively, while meeting the $-25$ dB-EVM requirement. Deep class AB in the LP mode can increase PAE, while sacrificing the EVM and gain performance, resulting in increased backoff from the $P_{SAT}$. Fig. 7 shows the measured EVM and operating current in both modes. Since the operations in both modes satisfy the linearity requirements up to 15.7 dBm, the operation in the LP mode is advantageous in that range to improve efficiency performance. In fact, LP mode operation can reduce the current consumption by more than 40% at a 10 dBm output power level (16.8 dB backoff) when compared to the HP mode operation. The solid black lines in Fig. 7 represent the trajectories of the average operating currents obtained by optimal selection of the operation mode, while satisfying the $-25$ dB EVM and spectral mask requirements. In Table I, the performance of the proposed PA is compared with those of other state-of-the-art WLAN dual-mode CMOS PAs. As shown in Table I, the fully integrated CMOS PA achieves a higher efficiency in both HP and LP modes at $-25$ dB EVM. Because in the proposed ABPCT the passive efficiency in the LP mode is higher than that in the HP mode, the biggest efficiency advantage of the proposed PA is obtained in the LP mode, with much better performance than that in other works.

TABLE I

COMPARISON OF RECENTLY REPORTED WLAN DUAL-MODE CMOS PAS WITH THAT PROPOSED IN THIS LETTER

| Reference | | [2] | [3] | [4] | This work |
|---|---|---|---|---|---|
| Technology | | 0.18-$\mu$m CMOS | 55 nm CMOS | 0.18-$\mu$m CMOS | 40 nm CMOS |
| Signal | | 11g | 11n | 11g | 11g |
| Frequency | | 2.5 | 2.45 | 2.4 | 1.75 |
| Method | | Resizing, PCT, TM | Resizing | TM | ABPCT |
| Fully integrated? | | YES | YES | NO | YES |
| $P_{SAT}$ (dBm)/ Peak PAE (%) | | 31 / 34.8 | 24.3/ 16.5* | 27 † / 26.1 | 26.8 / 34.4 |
| PAE@ 7dB/ 11 dB Back-offs (%) | | 12.5* / 9.2* | 7.2* / 4.5* | 7.5*/ 6.5* | 17.2/ 13.1 |
| $P_{out}$ @-25dB EVM (dBm) | HP | 21 | 17.5* | 24* | 19.7 |
| | LP | 15 | 2.8* | 18.4* | 15.7 |
| PAE @-25dB EVM (%) | HP | 5.8* | 7.3* | 15.8* | 17.1 |
| | LP | 7.5* | 0.8* | 9.7* | 13 |

* graphically estimated, † output P1dB, TM: tunable matching

## IV. CONCLUSION

This letter has proposed a dual-mode CMOS PA with an autotransformer-based PCT. Using the proposed structure, the dual-mode PA achieves high-efficiency performance with a compact die area. The fabricated dual-mode PA delivers saturated output powers of 26.8 and 24.7 dBm with 34.4% and 38.1% PAEs, in the HP and LP modes, respectively.

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