A Multi-path Multi-rate CMOS Polar DPA for Wideband Multi-standard RF Transmitters

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***Abstract*—A two-path digital power amplifier (DPA) in 1.2V 65nm CMOS is presented. This highly reconfigurable and frequency agile block is designed to be used as an envelope modulator in a wideband multi-standard polar transmitter. Each path is composed of a 12-bit DPA ensuring the modulation of the envelope of the RF signal. The DPAs are controlled by envelope code words (ECW) at different sample rates. This diversity strongly attenuates the images produced by the direct digital to RF conversion, avoiding passive filtering. The baseband sample rate conversion can easily be reconfigured. The proposed front-end can manage spurious emissions depending on the standard, the carrier frequency and the required power. The DPAs also integrate active input impedance compensation cells in order to limit the input impedance modulation when switching the DPA cells. The two-path DPA covers a 0.9-1.9 GHz bandwidth with 16.7dBm output 1dB compression point and 12.4% PAE. 64-QAM presents -28dB EVM while active area occupies 1x0.25mm^2.**

***Keywords*—Multi-path, multi-rate, multi-standard, digital power amplifier (DPA), polar transmitter, software-defined radio (SDR), Lagrange interpolation, Cognitive Radio (CR).**

I. Introduction

Front-ends of hand-held devices need to deal with several generations of standards like GSM/EDGE or UMTS, and new standards such as Long Term Evolution and WiMAX. Which tend to improve the spectral efficiency, but also introduce tough specifications. The Cognitive Radio (CR) approach is able to sense its environment and detect the spectral areas offering better communication efficiency. Then, the user's experience could be greatly improved if the front-end was able to reconfigure itself in order to take advantage of unused bands by switching from one standard to another, depending on usage. The traditional implementation of multi-standard front-end requires the use of several transmitters and power amplifiers designed for a single band [1]. Disadvantages are the lack of configurability and the cost and area increase with the number of frequencies to address. All-digital transmitters are good candidates for multi-standard and reconfigurable front-ends. The digital-to-RF conversion (DRFC) [2] and the digital power amplifier (DPA) architecture [3] [4] are two promising approaches extending the digital processing up to the antenna. However, the direct baseband digital signal to RF conversion suffers from the lack of anti-aliasing filters and leakage between the digital and RF blocks. The images are up-converted by the RF carrier and are located at multiples of the baseband sample rate and can violate the emission mask at many points. A straightforward solution would be to use a baseband signal sampled with high oversampling ratio (OSR), in order to shift the images out of the system bandwidth. This solution is easy to implement for narrow-band systems (around 500MHz), but becomes infeasible for wideband systems (e.g: 0.8-3GHz) in which the baseband signal needs to be sampled at a rate close to the carrier frequency. Besides the battery life aspect, the design of converters with such sample rates is highly constraining. The circuit presented in this paper introduces a multi-path multi-rate approach. The idea is to split the strong images into smaller ones [5] in order to meet the spurious emission level, as shown in Fig.1. The paper is organized as follows. First, the principle of the multi-rate approach will be explained in Section II. Then, the on-chip DPA and compensation cells will be detailed in Section III. Section IV will details the implemented system. Finally, Section V will present the measurement results obtained with the prototype.

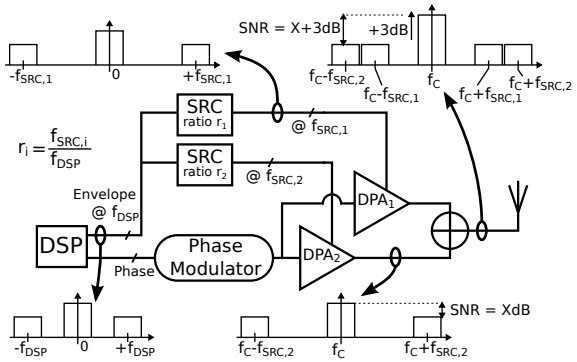

Fig. 1. Proposed polar multi-path multi-rate architecture

II. Multi-rate Architecture

Multi-path PA with power recombination, such as transformer-based combiner [6], have been used in advanced CMOS processes, due to the limited voltage supply and the need for high output power. The proposed architecture takes advantage of the multi-path approach and the high digital processing density of advanced technologies.

A. Multi-path approach principle

The images produced by the direct digital to RF conversion are related to the sample rate. In the architecture of Fig.1, each path comprises a sample rate converter (SRC) with a specific conversion ratio r_i. If all the conversion ratios are different, the images are not located at the same frequencies. Then, the images do not recombine while the fundamentals do. Fig.1 shows a 2-path polar architecture

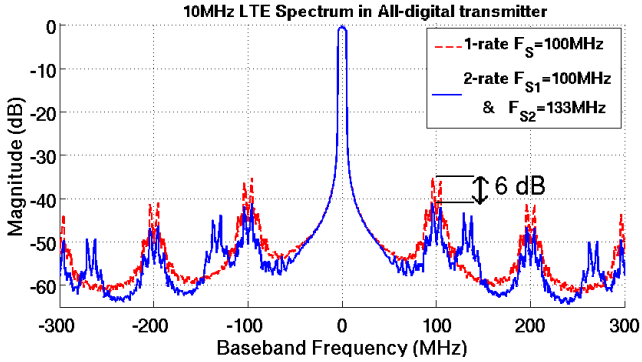

Fig. 2. Comparison standard all-digital Tx vs 2-rate architecture

with different sample rates. The fundamentals recombine at f_C, resulting in a 3dB gain at the transmitter output. On the contrary, the images keep the same magnitude. So, in a 2-path architecture, the SNR defined as the ratio between the fundamental and images is increased by 3dB, which is similar to an attenuation of 3dB of the images compared to a 1-rate transmitter. Finally, an architecture with N different sample rates will attenuate the images by:

$$Att(N) = 10 * \log(N) \quad (1)$$

B. Polar transmitter and impedance mismatch

Two additional aspects can help increase the images attenuation. First, polar transmitters perform different processes on the envelope and phase signals. The recombination of the filtered phase and envelope results in attenuated and distorted images as explained in [7]. This effect is represented in Fig.2 where a 2-rate polar system spectrum beside a standard 1-rate polar transmitter are shown. The second effect impacting the image attenuation comes from the impedance mismatch at the power combiner. In fact, the power combiner is designed to present the optimum impedance to all the RF modulators at the fundamental. But, the impedance presented to the RF modulators at image frequencies differs from the optimum. If only one path generates an image at one frequency, then the power combiner configuration can be approximated at this frequency as one active path while other paths are loaded by the output impedance of the RF modulators. In this case, the impedance presented to the power stage of the RF modulator is different from the optimum. Then, the power delivered to the power combiner is lower than the optimum case. In addition, the power is split between the antenna port and the other ports. To summarize, the total images attenuation depends on the number of images at the same frequency, the impedance mismatch and the power lost in inactive paths. Taking into account these three effects leads to the general approximation given in (2).

$$Att(N,K) = 10 * \log\left(\frac{P_{ANT}}{P_{ANTopt}}\right) = 20 * \log\left(\frac{K}{N}\right) \quad (2)$$

With N the total number of paths, and K the number of paths with images at the same frequency. Table I lists the total attenuation of images depending on N and K.

TABLE I. TOTAL IMAGES ATTENUATION

N\K	1	2	3	4	5	6
1	0					
2	-6.0	0				
3	-9.5	-3.5	0			
4	-12.0	-6.0	-2.5	0		
5	-14.0	-8.0	-4.4	-1.9	0	
6	-15.6	-9.5	-6.0	-3.5	-1.6	0

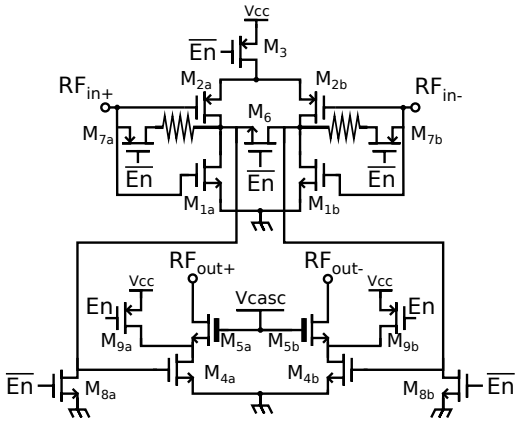

Fig. 3. Two-stage unit-amplifier cell

III. DIGITAL POWER AMPLIFIER

A dual DPA has been implemented in a 65nm CMOS process to cover a large frequency band and to support data rates up to 160Ms/s for the digital input. Architecture simulations show that a 12-bit resolution leaves enough margin for handling different modulation schemes, such as LTE, WCDMA or OFDM WLAN. The DPAs are implemented in a segmented form. The 4 LSBs drive a binary weighted matrix while the 8 MSBs control a 256 unit cells matrix. Fig.3 shows the schematic of a two-stage unit amplifier cell (UC) based on [4]. The first stage is a self-biased complementary common-source amplifier directly coupled to the output stage. This last stage is a Class-A amplifier with thick oxide cascode transistors which allow increasing the output swing to 4V. When the cell is ON, M_3 supplies the first stage and $M_{7a;b}$ allow self-biasing. Otherwise, when the cell is OFF, M_6 & $M_{8a;b}$ tie the last stage input to the ground while $M_{9a;b}$ reduce the leakage current and limit source voltage swing of the cascode transistors. The input impedance presented by a DPA is set by the input impedances of the UCs in parallel, and can be approximated by $Z_{IN} = (N_{ON} * Y_{ON} + N_{OFF} * Y_{OFF})^{-1}$, in which $\{N_{ON};\ N_{OFF}\}$ and $\{Y_{ON};Y_{OFF}\}$ represent the number of cells and the admittance presented by a UC in ON and OFF states. As explained in [4], the input differential capacitance can be supposed constant and equal to $C_{in} = N_{cell} * (C_{gs1a;b} + C_{gs2a;b})/2$. However, the switching of the self-biasing path introduces significant variations of the resistive input impedance. In order to limit the resulting signal distortions, a special compensation cell (CC) has been added to the DPA input. A CC is added every two columns of the MSB matrix and is controlled by the column activation signal as can

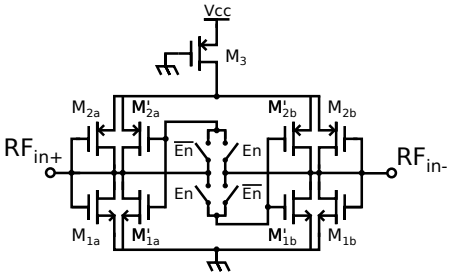

Fig. 4. Compensation cell

TABLE II. COMPENSATION CELL INPUT IMPEDANCES

State	Differential Mode	Common Mode
ON	$(2 * g_{ds1} + 2 * g_{ds2})^{-1}$	$(2 * g_{m1} + 2 * g_{m2})^{-1}$
OFF	$(2 * g_{m1} + 2 * g_{m2})^{-1}$	$(2 * g_{m1} + 2 * g_{m2})^{-1}$

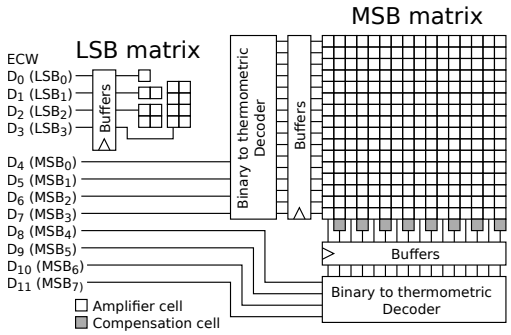

Fig. 5. DPA with Compensation cells

be seen in the DPA floorplan in Fig.5. One additional compensation cell is enabled for every 512 ECW step. Fig.4 shows the schematic of the compensation cell, which is matched to the input stage of the elementary amplifier cell. It is composed of two branches, $M_{1a;b}$ and $M_{2a;b}$ define the main branch, $M'_{1a;b}$ and $M'_{2a;b}$ the auxiliary branch. When the cell is enabled, the branches are in cross-coupled configuration. In differential mode (DM) , the transconductances $g_{m1a;b}$ and $g_{m2a;b}$ are cancelled by $g'_{m1a;b}$ and $g'_{m2a;b}$ while adding in common mode (CM) . On the contrary, in the off-state, branches are in parallel in both DM and CM. The resulting impedances presented between RF_{in+} and RF_{in-} are listed in Table II. Fig.5 shows the LSB and MSB matrix of the DPA with compensation cells beside the columns and rows controllers. Their differential resistive impedance variation is inversely proportional to the envelope code word, which compensates the one induced by the UC switching. Fig.6 shows the resistive input impedance variations as a function of the ECW. When no compensation cell is present, the input impedance strongly varies from $8K\Omega$ down to 32Ω. Adding the CC limits the impedance variation to less than 10Ω. The resistive impedance is always comprised between 27Ω and 38Ω. Furthermore, the CC have low CM impedance which stabilizes the DPA.

IV. Implemented System

In order to demonstrate the images attenuation in a multi-rate architecture, a 2-path digital polar PA was implemented in a 65nm CMOS process from ST Microelectronics. The die micrograph is represented on Fig.7. The circuit is pad limited. Thus, the 12-bit ECWs are serialized in a double data rate format on 3 bits in order to limit the number of pads dedicated to digital control, the resulting data clock speed is two times the sample rates and goes up to 320MHz. 20 pads are dedicated to power supplies, 10 to RF signals and 10 to digital signals. The active area occupies 0.25mm^2. The overall prototype setup is shown in Fig.8. Each symbol is separated into envelope and phase components. The phase signal modulates the carrier frequency thanks to a vector signal generator. The envelope signal is interpolated by an FPGA to two new signals at sample rates f_{S1} and f_{S2}. The SRC are based on highly reconfigurable Lagrange interpolators. Input and output impedance matching is performed on-board while single-ended to differential conversion and power combination are done with external components.

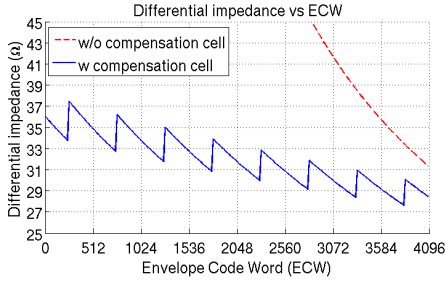

Fig. 6. Compensation cells impact on input impedance

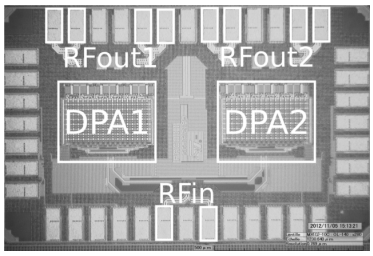

Fig. 7. Die micrograph

V. Measurements Results

Fig.9 shows the power characteristic of the amplifier when all the cells are enabled. Fig.12 represents the 1dB compression point output power and PAE over frequency after de-embedding of the on-board matching network and off-board power combiner for a one-tone signal, when both paths are enabled and set to the maximum ECW. The maximum output power is obtained at 1.1GHz and is equal to 16.7dBm with a maximum PAE of 12.4%. The circuit draws 130.2mA from the 2.5V supply and 39.3mA from the 1.2V supply. The logic interfaces and matrix buffers draw less than 5mA from the 1.2V supply. The amplifier was designed to cover a frequency band from 0.8 to 3GHz. However, the useful frequency range is limited by the on-board matching network to 0.9-1.9GHz. Fig.10 and 11 show the spectra for 10 MHz LTE channels when different couples of sample rates are chosen. The

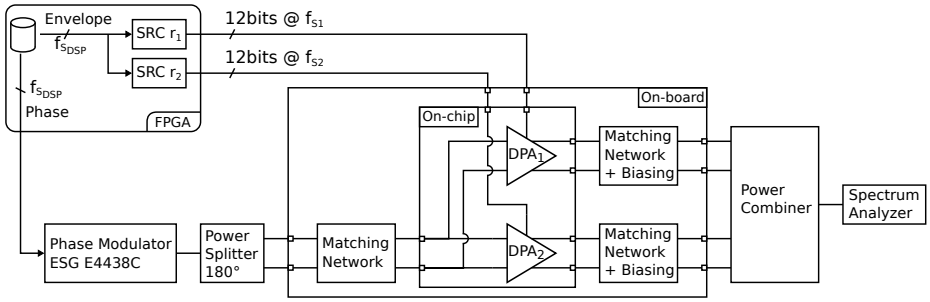

Fig. 8. Implemented System

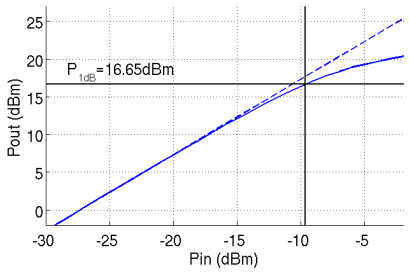

Fig. 9. P_{out} vs P_{in} for a 1.1GHz sine wave with full ECW

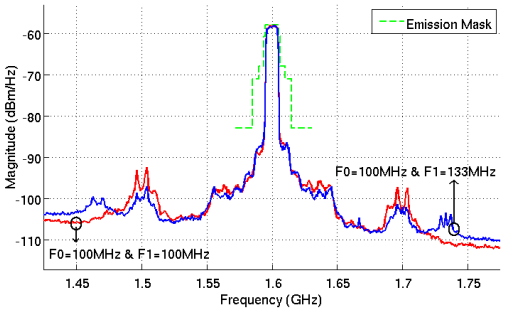

Fig. 10. Comparison between 1-rate and 2-rate spectrum

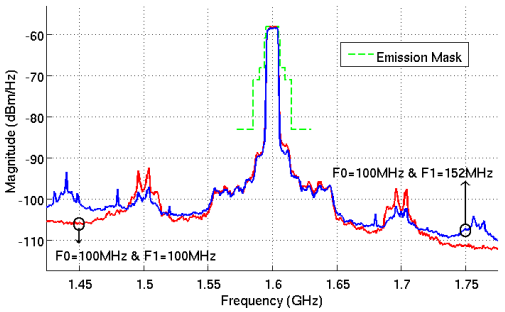

Fig. 11. Comparison between 1-rate and 2-rate spectrum

images are effectively reduced by 6 dB with the 2-path approach, and can be placed at arbitrary frequency offsets from the carrier. A -28dB EVM was measured for a 64-QAM modulation with a 10 MHz symbol rate and -10dBm input power corresponding to the input 1dB compression point, whatever the envelope sample rates.

VI. Conclusion

A wide-band digital polar amplifier based on a multi-path multi-rate approach has been demonstrated. The amplifier possesses two parallel DPAs controlled by two envelope signals with different reconfigurable sample rates. The amplifier delivers up to 16.7 dBm over a 0.9 - 1.9 GHz band while providing 12.4% PAE.

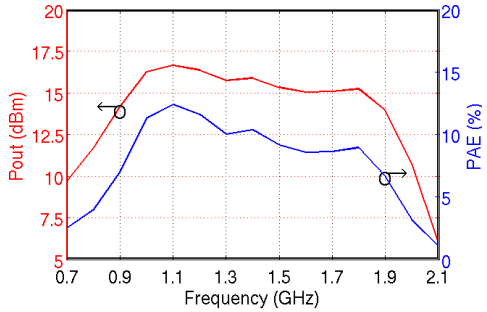

Fig. 12. P_{1dB} and PAE vs frequency

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