A Digital Polar CMOS Power Amplifier With a 102-dB Power Dynamic Range Using a Digitally Controlled Bias Generator

Hyunseok Choi, *Student Member, IEEE*, Yumi Lee, and Songcheol Hong, *Member, IEEE*

***Abstract*—A digitally modulated CMOS power amplifier (DPA) for a polar transmitter with a high dynamic range is presented. To improve local oscillator (LO) leakage, which limits the minimum output power of the DPA, the unit amplifier cell of the DPA employs a balanced mixer-type LO canceller at the power stage and a virtual ground is introduced in the layout of the output-power combining networks. A high dynamic range of the output power is simply achieved by adjusting gate-bias voltage of a cascode transistor in each power amplifier (PA) cell using a digitally controlled bias generator. This architecture allows a few-mA drain current at a low Tx power level without degrading the linearity. An array of unit PA cells is segmented to have a 10-bit amplitude resolution, and the bias generator is designed to have 8-bit control of the average output power. The peak output power is 24.4 dBm with an overall efficiency of 43% at 800 MHz. The total output dynamic range is 102.8 dB. A simple static pre-distortion helps the DPA achieve an average efficiency of 35% with a root mean square error vector magnitude of 3.59% while delivering linear output power of 22 dBm for WCDMA. The range of the digital transmit-power control for the WCDMA signal is 49.7 dB. This chip is fabricated in a 65-nm RF CMOS process.**

***Index Terms*—CMOS RF power amplifier (PA), digital amplitude modulation, digitally modulated PA, dynamic range, local oscillator (LO) leakage, polar transmitter, Tx power control, WCDMA.**

I. Introduction

THE GROWING demand for high-speed wireless data transfers with handheld mobile devices has been unprecedented. For a cost-effective integrated solution, the CMOS power amplifier (PA) has been intensively investigated in an effort to improve the efficiency while preserving the linearity requirements for large peak-to-average ratio (PAR) signals. Moreover, in order to accommodate various communication environments with high integrity, the support of multi-band/multi-mode operation in transmitter designs has attracted interest to reduce the size and lower cost of the overall system.

Since nonlinear switching PAs are more efficient and flexible than linear PAs, a polar transmitter for linear amplification with a switching transistor is a promising candidate [1]–[3] compared to the conventional I/Q-based transmitter as CMOS technologies are scaled down to the deep-submicrometer range [4] . However, the conventional analog polar transmitter is associated with a number of critical drawbacks, such as a bandwidth (BW) efficiency tradeoff in the supply modulator [5], [6], spectral regrowth caused by nonideal signal reconstruction, and a restricted dynamic range [7], [8]. Therefore, it is difficult to be popularly used for modern wideband applications such as WCDMA and long-term evolution (LTE).

Recently, digitally modulated CMOS power amplifiers (DPAs) for polar transmitters have been studied considerably as a highly prospective alternative. In previous studies, after the DPA successfully demonstrated the basis of the digital amplitude modulation for a polar transmitter [9], the DPA was investigated in an effort to solve several challenging problems and improve its performance. A highly efficient DPA with watt-level output power was implemented with stacked field-effect transistors (FETs) in a CMOS process [10]. Although the DPA showed a sufficient spectral margin for in-band spectral mask specifications, due to quantization noise and spectral images, it unfortunately still requires much greater development to satisfy the out-of-band noise requirements. In order to suppress the spectral image for sufficiently low far noise, fourfold interpolation [11] and advanced effective digital filtering [12] techniques for use with the amplitude path have been extensively studied. The nonlinearity of the DPA, which is characterized as digital amplitude control words (ACWs)-AM/PM distortion, is compensated with adaptive digital pre-distortion using a lookup table (LUT) [13]. The switched-capacitor RF PA has also shown excellent low-distortion characteristics [14]. Although the DPA is based on highly efficient switching PAs, theoretically the back-off efficiency curve of the DPA is equivalent to that of a Class-B PA. To enhance the efficiency at a low output power, a dual-power mode output-matching network for the DPA is necessary [15].

Since a conventional analog polar transmitter suffers from a small transmit power control (TPC) range due to the limited control range of the supply voltage and local oscillator (LO) leakage at a low output power, it is still remained as a great challenge of the DPA, which is based on a polar architecture.

Manuscript received August 28, 2013; revised December 18, 2013; accepted December 20, 2013. Date of publication January 14, 2014; date of current version March 03, 2014. This work was supported by the Korea Government (MSIP) under National Research Foundation of Korea (NRF) Grant 2005-0049408.

H. Choi and S. Hong are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST). Daejeon 305-701, Korea (e-mail: spiony@kaist.ac.kr).

Y. Lee is with System LSI Business, Samsung Electronics Company Ltd., Yongin, Kyoungki-Do 446-711, Korea.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2014.2298386

Most of all, it is practically limited in terms of implementation to cover a very wide TPC range with only an amplifier cell array for amplitude resolution. In order to express the modulated RF signal with an allowable amount of quantization noise, it is necessary to use a suitable bit resolution for amplitude modulation. For example, amplitude resolution of at least 5–6 bits is required to meet the adjacent channel leakage ratio (ACLR) specification for WCDMA [13]. Therefore, the minimum output power generated by one unit cell in a DPA should be even lower than the minimum RF transmit power, while the instantaneous power dynamic range is needed to be much larger than the required TPC range. This causes the DPA to be divided into extremely small unit cell amplifiers for very low output power and a high resolution of the amplitude while the complexity is accordingly increased. To improve the effective amplitude resolution and to lower the output power given the practical limitations of the unit cell implementation, digital signal processing (DSP) techniques such as delta–sigma modulation or pulsewidth modulation are partially or fully adopted in the transmitter [16]–[18], but it is a non-negligible burden for a DPA to cover a wide TPC range with large unit amplifier cells at a high output power. Moreover, the large parasitic capacitors of the switching transistors in the PA form essentially an undesired LO leakage path from the LO to the RF output [19]. A DPA consisting of many unit amplifier cells must have long and complicated RF paths. This exacerbates the LO leakage problem, which make it difficult to decrease the minimum output power of the DPA. Consequently, several previous works [13], [15], [20] employ analog TPC methods with external components to cover a wide transmit power range.

In this paper, we proposed a DPA with a high dynamic range using a digitally controlled bias generator. LO leakage-cancellation schemes are also employed in the unit amplifier cell and in LO input/RF output paths. The DPA using the proposed structures achieved an output dynamic range of 102.8 dB with a digital TPC range of 49.7 dB for WCDMA without additional components such as a variable gain amplifier (VGA) or a variable attenuator (VATT).

This paper is organized as follows. Section II describes the conventional and proposed DPA architectures. The circuit design and the layout strategy of the DPA for very low LO leakage are explained in Section III. The measurement results are shown in Section IV and concluding remarks are given in Section V.

II. Proposed Architecture

Given that the phase-modulated LO signal at the input of a polar transmitter should retain the same envelope even at a low output power for the switching operation, large LO leakage through the parasitic capacitors of the switching transistors makes it difficult to reduce the minimum output power for a high output dynamic range.

Generally, DPAs based on a polar architecture have the same leakage problem. In order to obtain high output power with high efficiency, the size of the DPA (the number of unit amplifiers and the size of each unit amplifier) should be carefully increased to have smaller on-resistances of the switching transistors. However, due to the larger parasitic capacitors in the DPA, the minimum output power can be limited by the larger LO leakage, as shown in Fig. 1 [19].

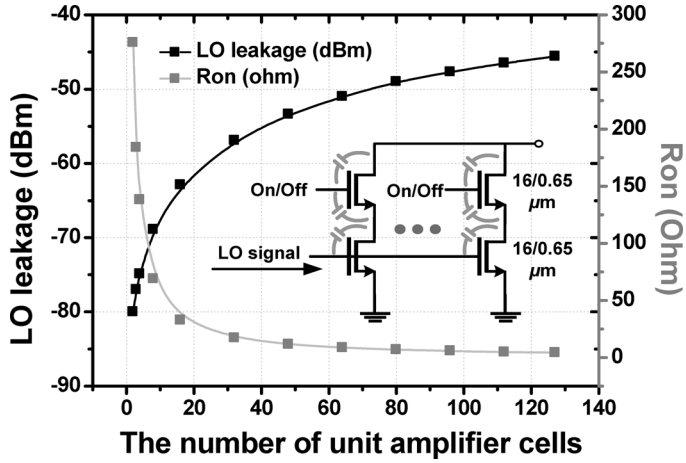

Fig. 1. Simulated total LO leakage and Ron-resistance of all the unit amplifiers in a DPA versus the number of unit amplifier cells (W/L of each transistors of the unit cascode amplifier: 16 μm/0.065 μm).

Previous works [13], [15], [20] employ two different transmit power-control schemes to support a large dynamic range. The first is a digital transmit power control (digital TPC) scheme for a high power range, and the second is an analog transmit power control (analog TPC) scheme for a low power range. In the digital TPC range, because the number of control bits is much higher than that necessary to satisfy ALCR specifications at the maximum output power, it is possible to decrease the output power simply by decreasing the ACW. This is valid as long as the ACLR specifications are not violated for each application while keeping the phase- modulated LO signal input power ($P_{\rm in}$) equal.

In the analog TPC range, additional components, such as a VGA and a VATT, can be utilized to reduce the LO signal input power ($P_{\rm in}$) of the DPA or the reconstructed RF signal at the following DPA to expand the output power dynamic range, as shown Fig. 2. However, this analog TPC method increases the complexity and cost of the overall Tx system.

In this work, we present a new DPA architecture for a high dynamic range. A digitally controlled bias generator is introduced to control the output power. Furthermore, a novel PA cell and layout method for a power-combining network in the DPA are introduced to reduce the LO leakage.

A. Dynamic Range of a DPA Based on a Polar Transmitter

In a conventional analog polar transmitter, the dynamic range is determined by the variable range of the supply voltage. In order to have a large dynamic range, the minimum supply voltage should be as low as possible. However, a low supply voltage inevitably degrades the overall efficiency of the supply modulator. In addition, LO leakage, which also causes phase distortion, hinders the reduction of minimum output power. The dynamic range of an analog polar PA is described as follows:

$$\begin{aligned}\text{Dynamic Range} &= P_{\text{OUT max}} - P_{\text{OUT min}} \\ &= 20\log\frac{VDD_{\max}}{VDD_{\min}}\ (\text{dB}). \end{aligned} \tag{1}$$

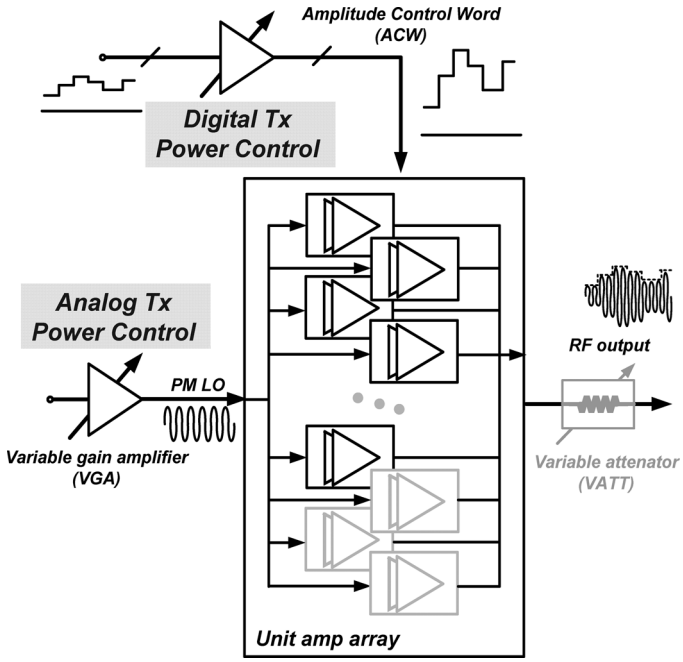

Fig. 2. Conventional digital and analog Tx power control schemes for DPAs for polar transmitters.

In a digital polar transmitter, which works on the principle of adding RF-switched conductances for a digital amplitude modulation, each unit amplifier cell operates as an RF-switched current source through the ACW. The output power of the transmitter is represented as (2); the relationship between the ACW and bit resolution n is shown in (3) as follows:

$$P_{\mathrm{OUT}} = a \cdot [\mathrm{ACW} \cdot I_{D\ \mathrm{out}}]^2 \cdot Z_{\mathrm{Load}} \tag{2}$$

$$n = \log_2 \mathrm{ACW} \tag{3}$$

where a is the coefficient of the fundamental component at the RF carrier frequency, $I_{D\ \mathrm{out}}$ is the drain current of a unit amplifier cell, and Z_{Load} is the load impedance.

Using these equations, the dynamic range of the ideal DPA can be expressed as follows:

$$\text{Dynamic Range of an ideal DPA} = 10 \log \mathrm{ACW}^2 \cong 6\ \mathrm{dB} \cdot n. \tag{4}$$

However, the DPA has ACW-AM compression, in which the output amplitude voltage is not exactly proportional to the increase in the ACW. This reduces the dynamic range of the DPA by a few dB, while the effective amplitude resolution is decreased. Moreover, in order to design a DPA with a high dynamic range, a DPA is required to have higher maximum output power and lower minimum output power as much as possible. Thus, the total size of switching transistors in an array should be large for a high maximum output power as mentioned before. Simultaneously, the size of the unit amplifier cell needs to be small for minimum output power as well as a high amplitude resolution. Therefore, the LO leakage from all of the switching transistors can eventually exceed the output power of one unit amplifier. This is a major obstacle when attempting to enlarge the dynamic range of the DPA. In this case, the dynamic range of the DPA in dB is represented as

$$\text{Dynamic Range of the DPA} \cong 6 \cdot n - P_{\mathrm{diff,AM}} - (P_{\mathrm{LO\ leakage}} - P_{\mathrm{out,unit}})\ (\mathrm{dB}) \tag{5}$$

where $P_{\mathrm{diff,AM}}$ is the difference between the maximum output power of the ideal DPA and that of the non-ideal DPA caused by the ACW-AM distortion, $P_{\mathrm{LO\ leakage}}$ is the LO leakage power, and $P_{\mathrm{out,unit}}$ is the output power from one unit amplifier. Therefore, it remains a challenge to achieve a sufficiently wide power dynamic range with a high output power and high amplitude resolution with a DPA.

B. Proposed DPA Architecture and Tx Power Control

Fig. 3 illustrates the proposed high dynamic-range DPA architecture and the TPC scheme. Compared to a conventional DPA, a high dynamic range can be achieved without reducing the LO input for a low level of LO leakage using additional components such as a VGA or a VATT. In order to ensure very low LO leakage, a balanced mixer-type LO leakage cancellation structure is applied to the unit amplifier cell and a new layout scheme of a RF input/output differential combining path is introduced. The circuit design and the layout details are explained in Section III.

The proposed DPA has a large dynamic range with a digitally controlled bias generator. The bias generator makes digitally stepped bias voltage applied to the gate of the common-gate (CG) transistor of the power cell in each unit amplifier cell. Compared to linear PAs, the linearity of the amplitude modulation in the DPA is mainly determined by the amplitude resolution. Although the ACW-AM/PM distortions can change according to the CG gate bias voltage, these also can be compensated by digital pre-distortion. In consequence, the bias voltage of each amplifier cell can be adjusted from the supply voltage to approximately the subthreshold voltage without concern over the linearity degradation of the amplitude modulation. This makes it possible very simply to control the output power range of the DPA. Moreover, by reducing the bias voltage, the total drain dc current of the DPA can also be drastically decreased at a low output power.

Therefore, the output power is controlled by two digital control words, the ACW and the bias control word (BCW). Two control methods are applied simultaneously for a wide TPC range while a constant amplitude of the phase-modulated LO input signal is maintained. Each control method for the TPC is described in detail as follows.

- *ACW TPC: The ACW is utilized not only to modulate the envelope of the desired RF signal, but also to control a Tx power level as in previous works [13], [15], [20], the number of activated unit amplifier cells for amplitude modulation can be scaled down while not violating the ACLR specifications at each CG bias level.*
- *BCW TPC: The BCW scales the output power of each amplifier cell through adjusting its CG gate bias voltage. The digitally controlled bias generator provides bias voltages by the BCW. This can change the effective size of the unit amplifier cell to have the 6-dB output power step per one bit of the BCW.*

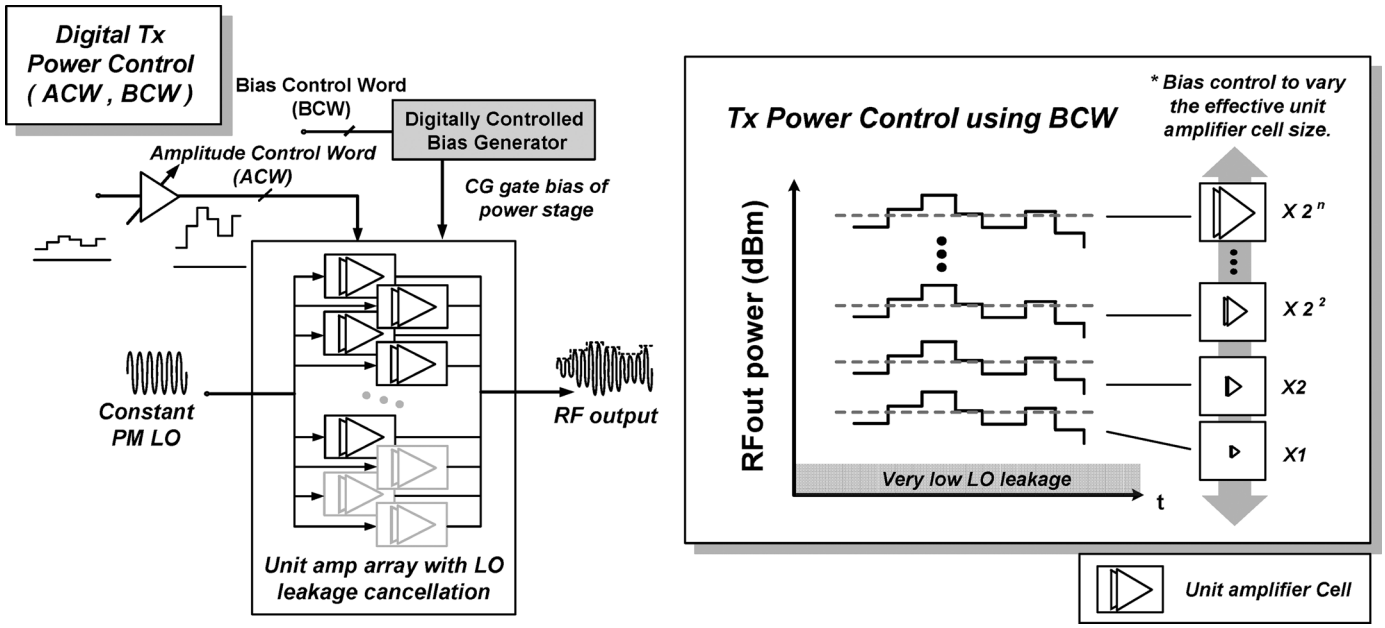

Fig. 3. Proposed high dynamic-range DPA architecture and TPC scheme.

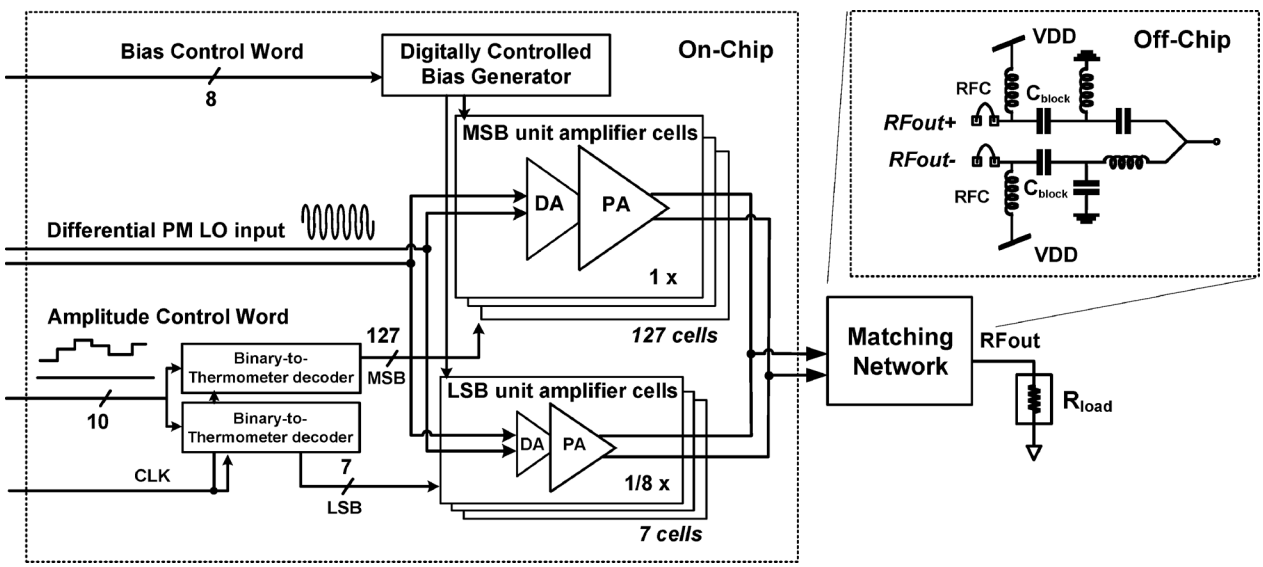

Fig. 4. Block diagram of the proposed high dynamic-range DPA architecture and off-chip matching network.

While the BCW TPC method simply scales the output power of each amplifier cell, the amplitude resolution implemented with an amplifier cell array can be fully utilized with the ACW at each BCW state.

III. Implementation

A block diagram of the proposed DPA architecture with a high dynamic range is shown in Fig. 4. The DPA is composed of a unit amplifier cell array and digital control circuitry that controls the cell array for amplitude modulation and the Tx power. Amplifier cells are connected in parallel to combine the RF output current of each cell. The digital control circuitry consists of binary-to-thermometer decoders and a digitally controlled bias generator. In order to achieve the desired amplitude modulation of the RF signal, the ACW determines the number of activated amplifier cells to amplify the input phase modulated LO signal with the binary-to-thermometer decoders. The output power of each unit amplifier cell is determined by the BCW for Tx power control. This is done by the digitally controlled bias generator, of which the output voltage is applied to the CG gate of each PA cell.

The amplitude resolution of the DPA is determined by considering the targeted application. As reported with system-level simulations in previous works [13], [15], for WCDMA amplitude, resolution of at least 6 bits is required so as not to violate the ACLR specifications with a 10-dB margin. With an additional 4 bits, the DPA is designed to have a 10-bit amplitude resolution on account of nonidealities such as an effectively reduced resolution caused by the ACW-AM distortion [11]–[13], [15], [20]–[22], unit amplifier cell mismatch [22],

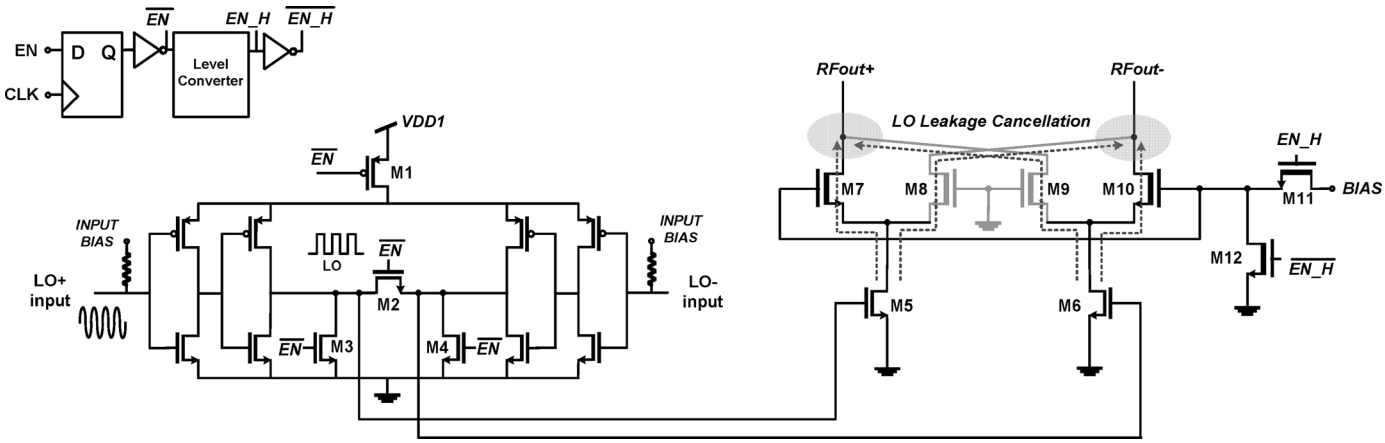

Fig. 5. Schematic of the unit PA cell.

spectral degradation from AM–PM time misalignment [13], [23], and spectral regrowth due to an insufficient oversampling rate [10], [11].

Unary-weighted and binary-weighted approaches have their own advantages in the current mismatches of the amplifier cells and the chip size, respectively. To compromise between these two factors, segmentation architecture is adopted [22]. The 10-bit resolution of the DPA is implemented with 127 unary amplifier cells for seven most significant bits (MSBs) and seven 1/8-sized unary amplifier cells for three least significant bits (LSBs). Moreover, to alleviate the nonlinearity effect caused by the threshold voltage gradients in the array, the cell selection order is pseudorandomized [24].

A. Circuit Details

A schematic of the unit PA cell is depicted in Fig. 5. The cell includes a driver stage and a power stage to amplify the LO signal, as well as a D-F/F register and a level converter for cell selection. In the driver stage, one pair of an inverter chain is designed to make the sinusoidal LO signal a square wave signal. This allows the following power stages to be switched perfectly and allows the power stage to have high efficiency. When the enable signal from the thermometer decoder is applied to a cell through the D-F/F for clock synchronization, transistor M1 is turned on to connect the supply voltage, while M2 through M4 are turned off to operate the drive stage. M2, which is connected to the differential output nodes of the driver stage, and M3–M4, which are connected to the output nodes to the ground, are employed in order to increase the isolation between the driver stage and the power stage when the power cell is turned off.

When the enable signal is high and the driver stage is on, the power stage designed as Class-E for high efficiency is also simultaneously turned on through the gate bias of the cascode transistors, M7 and M10. These are connected to the output node of the bias generator through M11. When the enable signal is low, the gate is grounded through M12. The enable signal for thick gate–oxide transistors, M11 and M12, is level converted to handle bias voltage from 2 to 0.47 V.

As illustrated in Fig. 5, the power stage has two additional cascode transistors, M8 and M9, which are connected as a double-balanced mixer structure to reduce the LO leakage. These additional transistors are always turned off. Thus, when the power stage is turned off, the LO leakage from the parasitic capacitors $C_{dg}s$ of the switching transistors (M5 and, M6) and the leakage of the cascode transistors (M7 and M10) are cancelled out at each RF output node of the power stage. This occurs due to the same amount of oppositely signed LO leakage from the additional leakage path through the cascode transistors (M8 and M9). To ensure this LO leakage cancellation, the sizes of the additional transistors (M8 and M9) should be equal to those of the cascode transistors (M7 and M10). Since the additional transistors are always turned off, these do not contribute to power amplification. Thick gate–oxide transistors with a gate length of 0.40 μm are utilized for the cascode transistors (M7–M10) to ensure the ruggedness of the PA. Although the two additional cascode transistors are employed solely to cancel the LO leakage, the total area of the power cell in the layout is increased by less than 20% compared to a conventional amplifier cell. RF transistors are separated from digital circuits for cell selection, such as the D-F/F register and a level converter using a triple-well structure to reduce the digital noise disturbance.

An accurate and stable bias control scheme for the CG gate of the power stage in each unit amplifier cell is essential to control the Tx power level precisely. The digitally controlled bias generator is based on the $V_{\rm th}$ reference current source [25]. A schematic of the digitally controlled bias generator is shown in Fig. 6. While the drain current of M3 is mirrored in the drain of M7, the voltage of the bias node connected to the gates of the common source (CS) transistors is determined by tailoring the width of the binary-weighted CS transistors, which are controlled by an 8-bit BCW to control the Tx power, as described by

$$V_{\rm BIAS} = \sqrt{\left(\frac{2I_D}{k_n{}'}\right) \cdot \left(\frac{L}{W_{\rm bias\_state}}\right)} + V_{\rm th} \qquad (6)$$

where I_D is the mirrored drain current, k_n' is the process transconductance parameter, L is the channel width, $W_{\rm bias\_state}$ is the effective width of the CS array, and $V_{\rm th}$ is the threshold voltage. As the effective width of the CS array is digitally increased by the BCW, the bias voltage gradually approaches $V_{\rm th}$, as shown in Fig. 7. The bias voltage is designed to make the 6-dB-step output power control of the DPA per 1 bit of

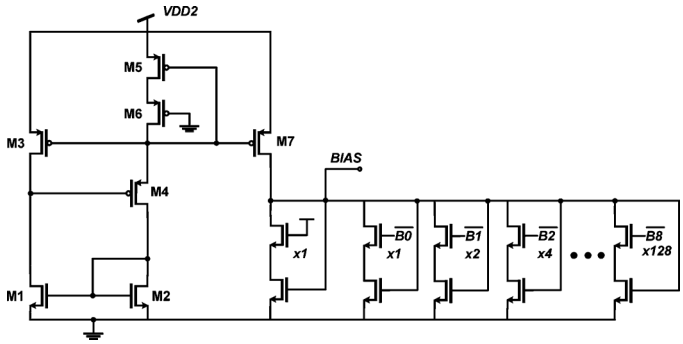

Fig. 6. Schematic of a digitally controlled bias generator.

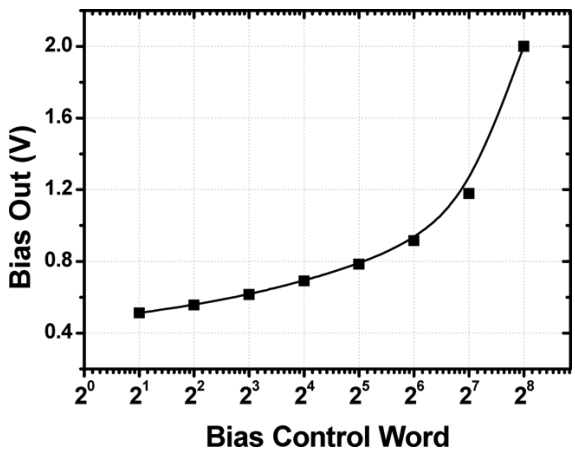

Fig. 7. Simulated bias output voltage of a digitally controlled bias generator.

the BCW. Moreover, in order to express the modulated RF signal, the minimum instantaneous output power of a DPA, which is generated by one unit cell, should be much lower than the minimum Tx output power for WCDMA. Assuming the amplitude resolution of 5 bit for WCDMA is used, it is needed to have the minimum output power with approximately -80 dBm with the lowest BCW state. Therefore, the 8-bit resolution of the bias generator is determined to reach the minimum output power. As previously stated, the bias voltage can be reduced to around $V_{\rm th}$ without concern over the linearity degradation of the amplitude modulation. Thus, in addition to a simple Tx power control scheme, the drain current of the DPA can be significantly reduced at a low output power using a bias generator.

B. Layout Scheme

To achieve a high dynamic range using a digital bias control scheme, it is necessary to ensure sufficiently lower LO leakage than the minimum output power from the unit amplifier with the lowest bias state. Otherwise, the minimum output power of the DPA is limited by the LO leakage. Unfortunately, although a sufficiently low amount of LO leakage is accomplished at the circuit level by means of a balanced mixer-type LO cancellation structure, the LO leakage through the capacitive coupling between the LO input paths and the RF output paths can become more serious due to the long and complicated RF-combining network of the DPA.

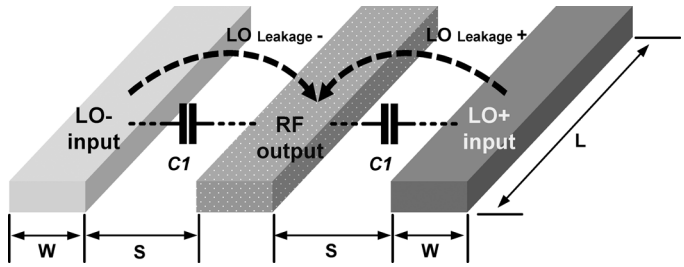

Fig. 8. Virtual ground of the capacitive coupled signals.

To reduce the LO leakage caused by the signal paths, a leakage virtual ground concept is explained in differential LO paths and in a single-ended output path, as illustrated in Fig. 8. When the output path is located between differential input signal paths with the same spacing, the same amount, but oppositely signed signals are coupled to the output path from each LO path. In this way, very low leakage signal coupling at the output path is realized.

However, in the practical layout of the cell array, the output RF path must be differential. Therefore, this LO leakage virtual ground is tailored to appear at the combining junctions of the output path. When both the left- and right-hand-side LO input differential paths are positioned with the same polarity in a cell array of the DPA, as shown in Fig. 9(a), the leakage currents through parasitic capacitors at the combining junction of the RF output paths can be represented as follows:

$$\begin{aligned} i^{+}_{\rm out,leakage} &= j\omega(C_1 {v_{\rm in}}^{+} + C_2 {v_{\rm in}}^{-}) + j\omega(C_1 {v_{\rm in}}^{+} + C_2 {v_{\rm in}}^{-}) \\ &= 2j\omega(C_1 {v_{\rm in}}^{+} + C_2 {v_{\rm in}}^{-}) \qquad (7) \\ i^{-}_{\rm out,leakage} &= j\omega(C_3 {v_{\rm in}}^{+} + C_4 {v_{\rm in}}^{-}) + j\omega(C_3 {v_{\rm in}}^{+} + C_4 {v_{\rm in}}^{-}) \\ &= 2j\omega(C_3 {v_{\rm in}}^{+} + C_4 {v_{\rm in}}^{-}) \qquad (8) \end{aligned}$$

where $i^{+}_{\rm out,leakage}$ and $i^{-}_{\rm out,leakage}$ denote the LO leakage currents at differential RF output paths; $v^{+}_{\rm in}$, $v^{-}_{\rm in}$ are the differential input LO signals of the LO input paths, respectively; and C_1–C_4 are the parasitic capacitors between the input and output paths. The LO leakage currents are added up without any cancellations when these are combined at the combining junction of the RF output path. On the other hand, when the polarity of the differential input paths at two equivalent branches changes, as shown Fig. 9(b), the leakage currents at the junction can be represented as follows:

$$\begin{aligned} i_{\rm out1,leakage} &= j\omega(C_1 {v_{\rm in}}^{+} + C_2 {v_{\rm in}}^{-}) + j\omega(C_1 {v_{\rm in}}^{-} + C_2 {v_{\rm in}}^{+}) \\ &= 0 \qquad (9) \\ i_{\rm out2,leakage} &= j\omega(C_3 {v_{\rm in}}^{+} + C_4 {v_{\rm in}}^{-}) + j\omega(C_3 {v_{\rm in}}^{-} + C_4 {v_{\rm in}}^{+}) \\ &= 0. \qquad (10) \end{aligned}$$

The LO leakage currents are cancelled out at the combining junction. The isolation between the input paths and the output paths is improved by 13–30 dB over a frequency range of 800 MHz–3 GHz with the alternating differential-path layout based on the leakage virtual ground concept, as shown in the electromagnetic (EM) simulation results in Fig. 10. Furthermore, the differential amplifier cells are placed with opposite polarity and connected to the RF output paths, as depicted

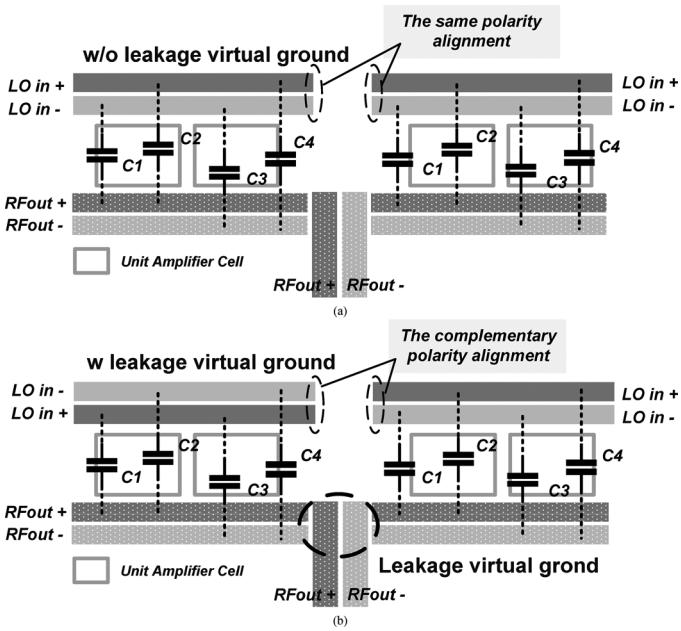

Fig. 9. Layout based on a: (a) conventional method and (b) leakage virtual ground.

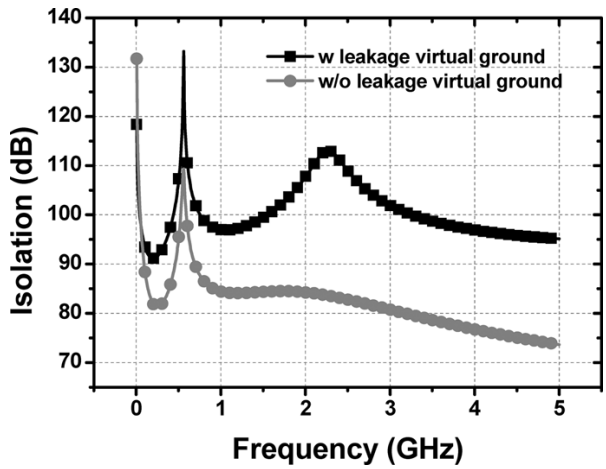

Fig. 10. Simulation results of the isolation between the input and output paths for a unit amplifier cell versus the frequency.

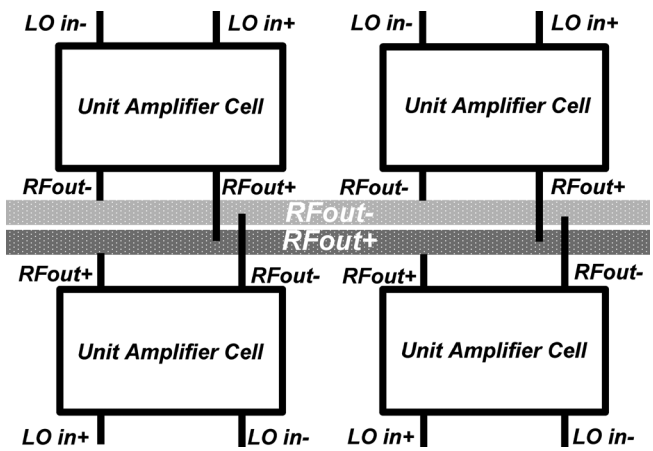

Fig. 11. Cell arrangement for leakage cancellation.

in Fig. 11. These two methods are also applied to the overall output path design to enhance the isolation. While the output

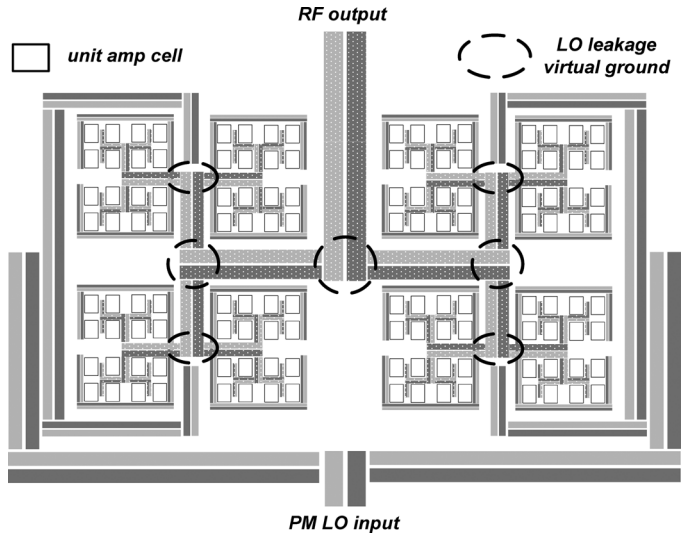

Fig. 12. Overall input and output paths in the amplifier cell array of the DPA.

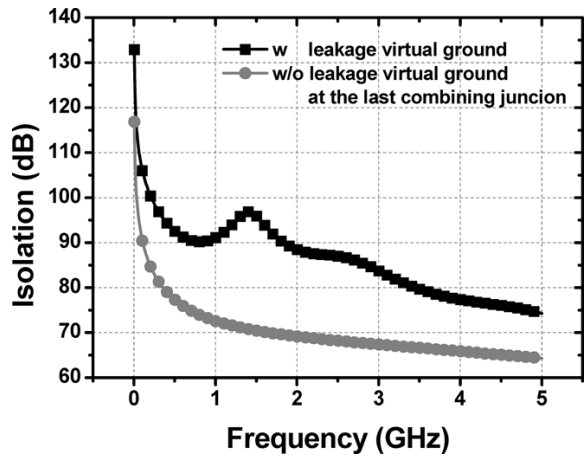

Fig. 13. Simulation results of the isolation between the overall input and output paths versus the frequency.

powers are combined along the H-tree output paths, the leakage virtual grounds are laid at the combining junctions for leakage current cancellation, as shown in Fig. 12. In order to ensure that the leakage virtual grounds along the output path, the polarities of the differential input and output paths are such that they have complementary characteristics in the entire cell array. An EM simulation of the full input and output paths was conducted to calculate the complicated parasitic signal couplings. Fig. 13 shows the simulation results of all path layouts with the leakage virtual grounds and without the leakage virtual ground only at the last output port for comparison. This is the most critical instance among the leakage virtual grounds. The isolation is improved by 16–26 dB over a frequency range of 800 MHz–3 GHz.

IV. Measurement Results

The chip was fabricated in a 65-nm RF CMOS process. A photograph of the chip is shown in Fig. 14. Its area is 1.7 mm $\times$ 1.3 mm including all of the pads. The output-matching network with the *LC* balun depicted in Fig. 4 is implemented on an FR-4 printed circuit board. The

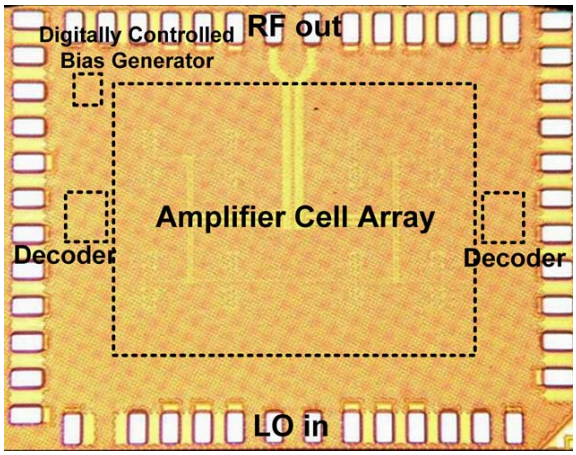

Fig. 14. Chip photograph.

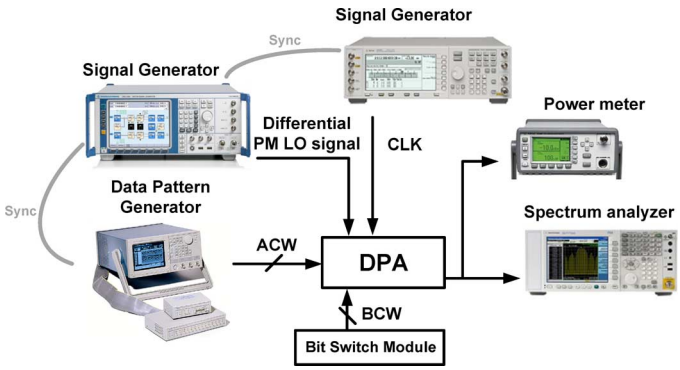

Fig. 15. Measurement setup.

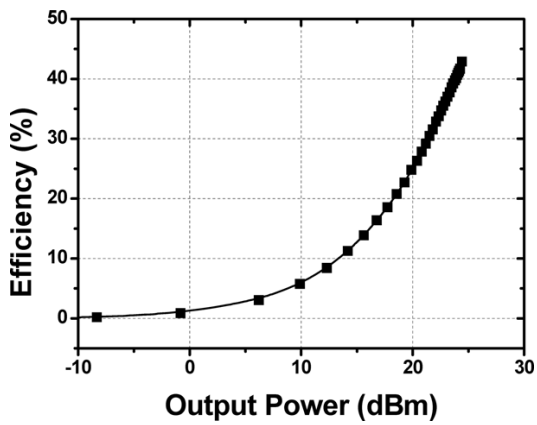

Fig. 16. Measured overall efficiency versus the output power (single-tone input $f_{\mathrm{RF}} = 800$ MHz).

measurement setup is shown in Fig. 15. The ACW and the differential phase modulated LO signals are generated using a Tektronix DG2020A digital pattern generator and an R&S SMU200A signal generator, respectively. The supply voltages are 2.5 V for the RF circuitry and 1.2 V for the digital circuitry.

The measured overall efficiency versus the output power with respect to the ACW at a single-tone LO input at 800 MHz is shown in Fig. 16. The LO input power is 6 dBm. The peak power including the loss of the off-chip *LC* balun output matching- network is 24.4 dBm with 42.5% peak efficiency at 800 MHz. As expected, the back-off efficiency characteristic curve resembles a Class-B curve [12], [13], [15], [20]. Fig. 17 shows the measured peak output power and the overall efficiency of the DPA throughout the frequency with maximum values of the ACW

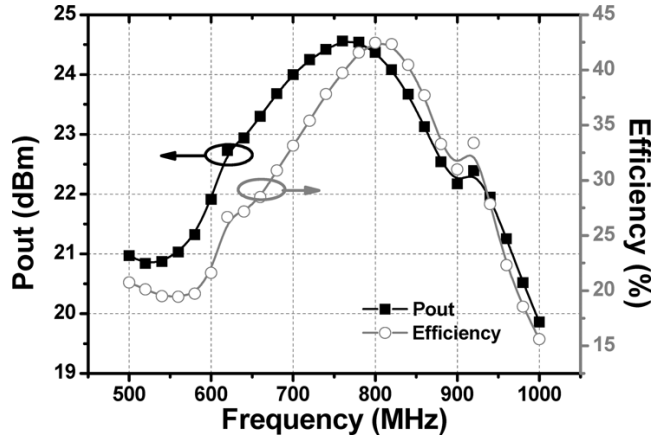

Fig. 17. Measured peak output power and overall efficiency versus the carrier frequency.

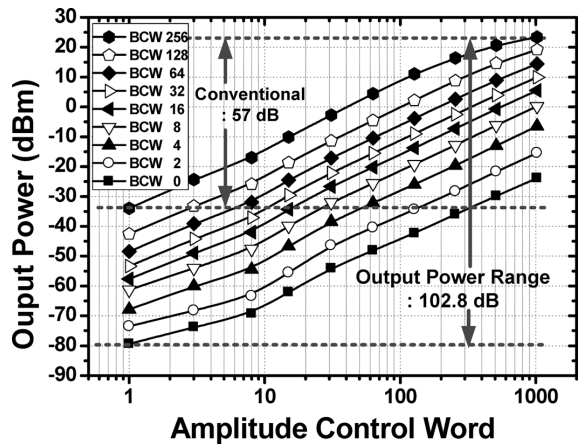

Fig. 18. Measured output power versus ACW with the BCW parameter (single-tone input $f_{\mathrm{RF}} = 800$ MHz).

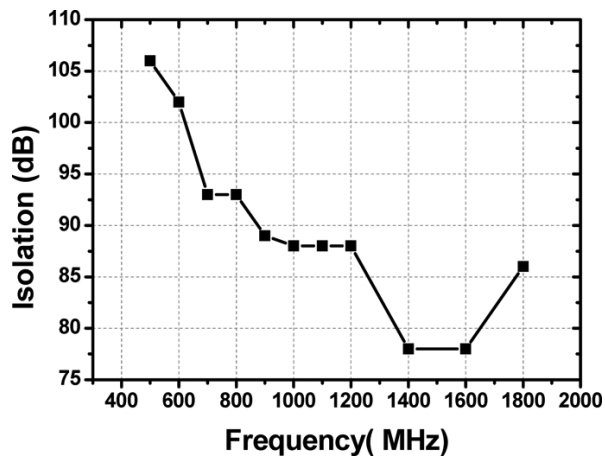

Fig. 19. Measured isolation between the input and the output over the frequency.

and BCW. The output power 3-dB BW is 350 MHz ranged from 600 to 950 MHz. While the conventional DPA with the fixed CG gate bias of the power stage has only one output power curve according to the ACW sweep at a constant level of LO input power, the output power range is 57 dB in this design. The proposed DPA has many output-power-ACW curves according to the BCW states, which allows the expansion of the TPC range with a constant LO input power. As a result, the proposed DPA shows a power dynamic range of 102.8 dB, as plotted in Fig. 18. In this figure, 8-bit control of the BCW is applied as an example.

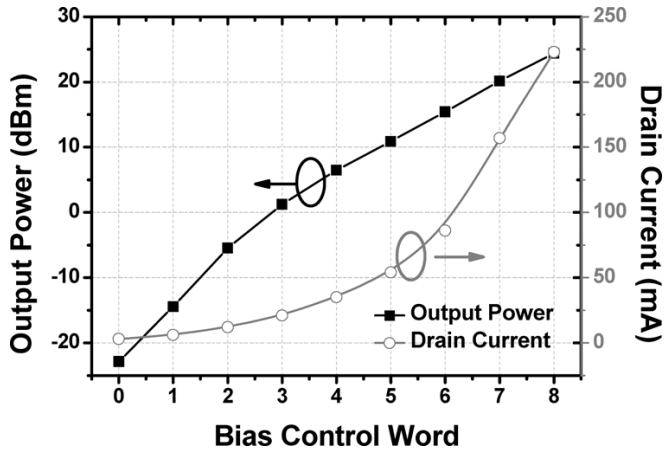

Fig. 20. Measured output power and drain current of the DPA with respect to the BCW at 800 MHz.

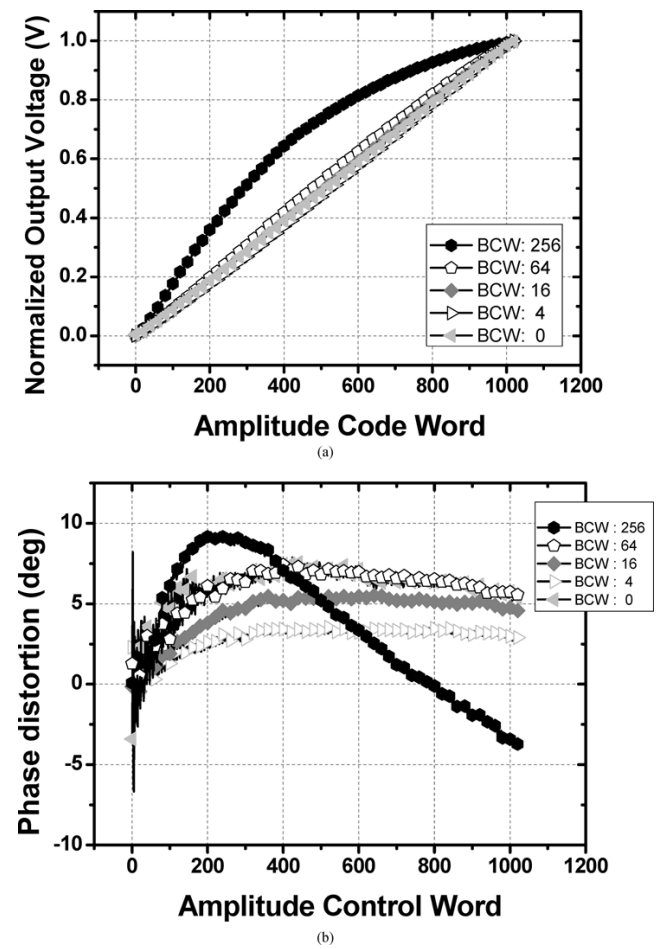

Fig. 21. Measured: (a) ACW-AM and (b) ACW-PM characteristics with respect to the BCW at 800 MHz.

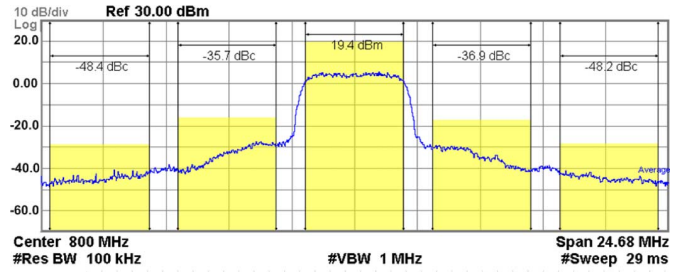

Fig. 22. Output spectrum for a WCDMA signal at 800 MHz.

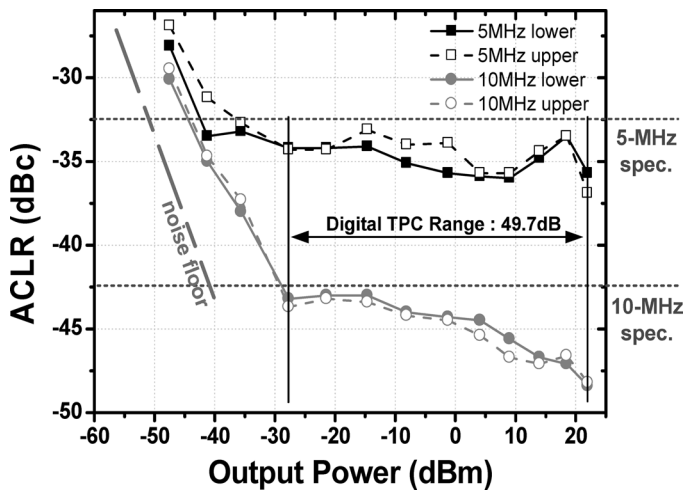

Fig. 23. Measured ACLR versus the output power with digital bias control at 800 MHz.

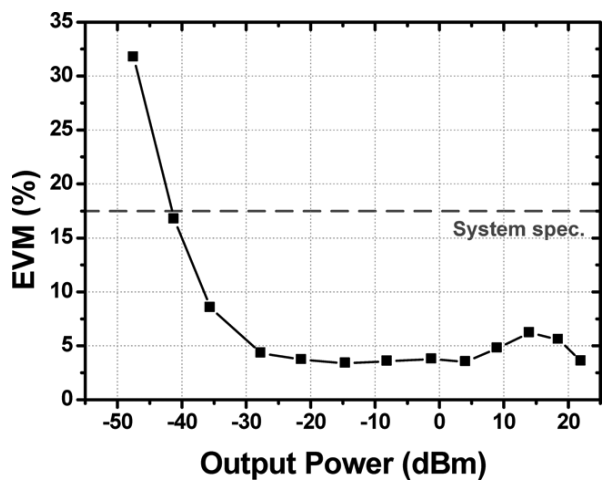

Fig. 24. Measured EVM versus the output power with digital bias control at 800 MHz.

It is also possible to have 1-dB-step gain control with the ACW and BCW TPC methods simultaneously. It is important to note that by employing a BCW in this structure, the output power range is increased by about 45 dB. Furthermore, the designed resolution implemented as the amplifier cell array is fully used in each BCW state.

Fig. 19 shows the measured LO signal isolation between the input and the output over the frequency. Isolation of more than 88 dB is maintained up to 1.2 GHz. This indicates that the PA works very well below 1.2 GHz.

The output power of the DPA with the maximum value of the ACW is controlled by the BCW in steps of $\sim$ 6 dB/bit, as if the unit amplifier cell is effectively re-sized according to the BCW, as shown in Fig. 20. Since the CG bias of the power stage is controlled by the BCW, the total drain current is drastically reduced at a low value of the BCW for a low output power. Therefore,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF DIGITAL POLAR PAs

Reference	[10]	[20]	[13]	[12]	This work
Frequency [GHz]	0.75	0.9	0.8-2	2.25	0.8
Resolution	6 bits	10 bits	10 bits	8 bits	10 bit
Peak P_{out} / Efficiency [dBm / %]	30 / 40.6	24.9 / 62.7	23.5-25.2 / 40-47	22 / 44	24.4 / 43
Supply voltage	3.3	1.2 / 2.5	1.2 / 2.1	1.0	1.2 / 2.5
Average P_{out} / Efficiency [dBm / %]	24 / 26.5	-	21.7 / 38.2	14 / 18	22 / 35
Modulation Format	WCDMA	-	EDGE / WCDMA / WiMAX OFDM	802.11g WLAN	WCDMA
EVM	-	-	1.5% (64-QAM)	4% (64-QAM)	3.6%
Output power range [dB]	43	43.9**	48	42	102.8
Tx Power Control [dB]	8*	-	> 70***	-	49.7
Matching Network	External	External	External	Integrated	External
Technology	0.15-μm CMOS	0.13-μm SOI-CMOS	0.13-μm SOI-CMOS	65-nm CMOS	65-nm CMOS

*without DPD
**input attenuator / Supply variation technique
***with a variable-gain-amplifier

only 3 mA of dc current is consumed with the maximum value of the ACW at the lowest bias state.

The measured ACW-AM and ACW-PM characteristics with respect to the BCW are plotted in Fig. 21. The ACW-AM distortion and ACW-PM distortion are alleviated as the bias state is decreased for a lower Tx power. As reported in previous works [13], [20], [26], DPA distortion is mainly due to the finite output impedance and the active load–pull effect. The mitigated distortion in the low bias state can also be explained in terms of these two factors. First, the output impedance of the DPA is much larger than the load impedance in the lower bias state; secondly, the drain voltage swing at the output of the power stage is small such that the operation region of the cascode transistor can remain in the saturation region without entering the triode region due to the active load–pull effect. These distortion characteristics are considered to make a LUT for the digital pre-distortion at each BCW state.

The DPA is tested with a 3GPP WCDMA hybrid quadrature phase-shift keying (HQPSK) signal with 3.4-dB peak-to-average power ratio (PAPR) to verify its dynamic behavior. The sampling frequency of the AM and PM signals is 76.8 MHz and the clock frequency is 153.6 MHz. AM–PM time alignment, which has a critical effect on the purity of the spectrum [13], [23], is achieved using baseband sample delays in the digital domain. The output spectrum with the highest BCW state at 800 MHz is shown in Fig. 22. The measured ACLR versus the output power with BCW control is shown in Fig. 23. The BCW was swept with a simple static digital pre-distortion for each BCW state, while the ACW is fully used. Moreover, in order to reduce the transmit output power below −30-dBm output power, the ACW scaling scheme was additionally used with the lowest BCW state. The digitally controlled TPC range is 49.7 dB without any analog TPC techniques using additional components such as a VGA or a VATT for LO input power control or RF output power control. Although the results do not meet the specifications of the WCDMA TPC range, they can be improved with more precise time alignment between the AM and PM signals [13], [23] using the fine-step sample delay. The results exhibit a maximum linear power of 22 dBm with an overall efficiency of 35%, including the dc power consumption of all of the circuitry considering off-chip matching network loss. The measured root mean square (rms) error vector magnitude (EVM) versus the output power with the BCW control scheme is plotted in Fig. 24. The measured EVM meets the system specifications in a range that exceeds 60 dB. The rms EVM is 3.59% at the peak linear power. The measured performances of the DPA are summarized and are compared to those of several recent DPAs in Table I. This DPA has the wide dynamic range and Tx power control range using a simple digital bias control scheme to reduce the complexity and power consumption of the entire Tx system.

V. CONCLUSION

A DPA has been presented. The DPA has a wide power dynamic range without external analog components such as a VGA, VATT, or supply modulator. The novel DPA simply uses a digitally controlled bias generator to have a wide dynamic range. A very low level of LO leakage is achieved by employing a balanced mixer-type LO leakage canceller in a unit amplifier cell of the DPA and LO leakage virtual ground concept in the input and output path layout. This allows the minimum output power of the DPA to be sufficiently reduced also for a wide output power dynamic range. Moreover, this architecture enables low dc power consumption at the low Tx power level without degrading the linearity. The peak output power is 24.4 dBm with an overall efficiency of 43% at 800 MHz. The output power range is 102.8 dB. The DPA has linear output power of 22 dBm with an average efficiency of 35% for WCDMA using a simple static pre-distortion scheme. The Tx power control range is 49.7 dB with only digital TPC methods.

ACKNOWLEDGMENT

The authors would like to thank J. Paek and H. Lee, both with Samsung Electronics, Yongin, Korea, for their helpful advice and discussions, and System LSI Business, Samsung Electronics Company Ltd., Yongin, Korea, for the fabrication of the chip.

REFERENCES

[1] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[2] M. R. Elliott, T. Montalvo, B. P. Jeffries, F. Murden, J. Strange, A. Hill, S. Nandipaku, and J. Harrebek, "A polar modulator transmitter for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2190–2199, Dec. 2004.

[3] T. Sowlati, D. Rozenblit, R. Pullela, M. Damgaard, E. McCarthy, D. Koh, D. Ripley, F. Balteanu, and I. Gheorghe, "Quad-band GSM/GPRS/EDGE polar loop transmitter," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2179–2189, Dec. 2004.

[4] A. A. Abidi, "RF CMOS comes of age," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 549–561, Apr. 2004.

[5] T.-W. Kwak *et al.*, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2666–2676, Dec. 2007.

[6] P. Nagle, P. Burton, E. Heaney, and F. McGrath, "A wideband linear amplitude modulator for polar transmitters based on the concept of interleaving delta modulator," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1748–1756, Dec. 2002.

[7] J. H. Chen, P. Fedorenko, and J. S. Kenney, "A low voltage WCDMA polar transmitter with digital envelope path gain compensation," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 7, pp. 428–430, Jul. 2006.

[8] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "A two-point modulation technique for CMOS power amplifier in polar transmitter architecture," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 1, pp. 31–38, Jan. 2008.

[9] P. Cruise *et al.*, "A digital-to-RF- amplitude converter for GSM/GPRS/EDGE in 90-nm digital CMOS," in *Proc. IEEE RF Integrated Circuits Symp. Dig.*, Jun. 2005, pp. 2179–2189.

[10] T. Nakatani *et al.*, "Digital-controlled polar transmitter using a watt class current-mode class-D CMOS power amplifier and Guanella reverse balun for handset applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1104–1112, May 2012.

[11] A. Kavousian, D. K. Su, M. Hekmat, A. Shirvani, and B. A. Wooley, "A digitally modulated polar CMOS power amplifier with a 20 MHz channel bandwidth," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2251–2258, Oct. 2008.

[12] D. Chowdhury, L. Ye, E. Alon, and A. Niknejad, "An efficient mixed signal 2.4-GHz polar power amplifier in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1796–1809, Aug. 2011.

[13] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25 dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.

[14] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.

[15] Y. Lee and S. Hong, "A dual-power-mode output matching network for digitally modulated CMOS power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1570–1579, Apr. 2013.

[16] T. Johnson and S. P. Stapleton, "RF class-D amplification with bandpass sigma-delta modulator drive signals," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 12, pp. 2507–2520, Dec. 2006.

[17] T.-P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "Design of H-bridge class-D power amplifiers for digital pulse modulation transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2845–2855, Dec. 2007.

[18] J. Mehta *et al.*, "A 0.8 mm all-digital SAW-less polar transmitter in 65 nm EDGE SoC," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2010, pp. 58–59.

[19] J. Paek, H. Lee, and S. Hong, "Analysis and design of CMOS amplitude modulator with digitally controlled variable attenuator," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 3, pp. 727–740, Mar. 2011.

[20] S. Pornpromlikit *et al.*, "A 25-dBm high-efficiency digitally modulated SOI CMOS power amplifier for multi-standard RF polar transmitters," in *Proc. IEEE RF Integr. Circuits Symp. Dig.*, Jun. 2009, pp. 157–160.

[21] K. Waheed and R. B. Staszewski, "Mitigation of CMOS device variability in the transmitter amplitude path using Digital RF Processing," in *IEEE Int. Circuits Syst. Symp.*, pp. 568–571.

[22] K. Waheed and R. B. Staszewski, "Digital RF processing techniques for device mismatch tolerant transmitters in nanometer-scale CMOS," in *IEEE Int. Circuits Syst. Symp.*, May 2007, pp. 1253–1256.

[23] K. Waheed, R. Staszewski, and S. Rezeq, "Curse of digital polar transmission: Precise delay alignment in amplitude and phase modulation paths," in *IEEE Int. Circuits Syst. Symp.*, May 2008, pp. 3142–3145.

[24] C.-H. Lin and K. Bult, "A 10 b 500 Msamples/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, Dec. 1998.

[25] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits (A Design Perspective)*. Englewood Cliffs, NJ: Prentice-Hall, 2003.

[26] P. T. M. van Zeijl and M. Collados, "A digital envelope modulator for a WLANOFDMpolar transmitter in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2204–2211, Oct. 2007.

Hyunseok Choi (S'08) received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 2008, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at KAIST.

His research interests include CMOS PAs and highly efficient RF transmitters for wireless communication systems.

Yumi Lee (S'06) received the B.S. degree in electrical engineering from Kyungpook National University (KNU), Daegu, Korea, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2008, and 2013, respectively.

In 2013, she joined the Modem and Connectivity Design Team, Samsung Semiconductor Inc., Yongin, Kyoungki-Do, Korea. She is currently involved with development of transceivers for mobile communications.

Songcheol Hong (S'87–M'88) received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, Ann Arbor, MI, USA, in 1989.

In May 1989, he joined the faculty of the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. In 1997, he held short visiting professorships with Stanford University, Palo Alto, CA, USA, and Samsung Microwave Semiconductor, Suwon, Korea. His research interests are microwave integrated circuits and systems including PAs for mobile communications, miniaturized radar, millimeter-wave frequency synthesizers, and novel semiconductor devices.