A Fully Integrated Watt-Level Linear 900-MHz CMOS RF Power Amplifier for LTE-Applications

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***Abstract*—There is a growing demand for the implementation of the RF power amplifier (PA) in CMOS technologies, due to its cost and integration benefits. Most of the already reported CMOS PAs do not have sufficient output power nor linearity to cope with the long term evolution (LTE) requirements. In this paper, the linearity requirements for power amplifiers targeting LTE-applications are investigated. Based on this system level analysis, a single-chip fully integrated CMOS power amplifier with sufficient power and linearity for emerging E-UTRA/LTE- applications is designed. This 90-nm LTE-band VIII CMOS linear power amplifier uses a distributed active transformer (DAT) as power combiner and delivers an output power up to 29.4 dBm with 25.8% power-added efficiency (PAE) and has 28-dB small-signal gain. The choice of optimal biasing ensures a very flat gain and small AM-PM distortion up to high output power. While applying an uplink LTE signal, the PA produces 25 dBm of average output power with 15% PAE while obeying the stringent EVM-specifications.**

***Index Terms*—CMOS RF power amplifier (PA), distributed active transformer (DAT), linearity optimization, long term evolution (LTE) , power combiner.**

I. Introduction

THERE is a tremendous interest from industry in completely integrated radio solutions in CMOS technology. CMOS offers a powerful platform for realizing a fully integrated radio system-on-chip (SoC) with its unparalleled integration level and extensive digital processing capability. CMOS PAs have demonstrated their suitability for advanced wireless communication standards, such as LTE/LTE-advanced and WiMAX, with good performance in output power, efficiency, and linearity performances.

Long term evolution (LTE) is the next step forward in cellular 3G services towards the 4G cellular services. LTE is a 3GPP standard that provides an uplink speed of up to 50 Megabits per second (MB/s) and a downlink speed of up to 100 Mbps [1]. LTE will bring many technical benefits to cellular networks. The bandwidth needs to be scalable from 1.25 to 20 MHz [1]. This will accommodate the needs of different network operators that have different bandwidth allocations, and also allow operators to provide different services based on the spectrum. LTE is also expected to improve spectral efficiency in 3G networks, allowing carriers to provide more data and voice services over a given bandwidth. Going to larger bandwidths requires high-linearity performance for the complete band, while not sacrificing in efficiency.

Many commercially available power amplifiers (PAs) based on a III-V compound semiconductor can produce a saturated output power much over 30 dBm with peak power-added efficiency (PAEs) greater than 45%, but they need 3–4 dB-backoff from the $P_{1\mathrm{dB}}$ compression point to meet the 3GPP LTE linearity requirements, resulting in lower overall PAE [2], [3]. Recently, a state-of-the-art linear SiGe dual-standard LTE/WiMAX PA has been reported with a saturated power of 30 dBm and a peak PAE of 30%, but its PAE is less than 20% once backed off around 6 dB to satisfy the WiMAX linearity requirements [4]. Newly, CMOS PAs with on-chip transformers have successfully delivered over 30-dBm saturated output power with the best PAE value around 50% [5], [6], but they need a large back-off to meet the linearity specifications of LTE signals. Nevertheless, standard CMOS is rapidly catching up.

Standard CMOS is the desired technology for the implementation of low-cost high-volume products. However, the use of a CMOS technology for a PA design introduces some challenges. Nanoscale CMOS technologies offer the advantage of realizing a design at high frequency, but unfortunately this also implies much lower breakdown voltages. This explains why the PA has been the last subblock to be integrated entirely in a standard CMOS technology. Delivering RF power in excess of 1 W to a 50-Ω load at high operation frequencies in CMOS has been the bottleneck for many years, because it requires a peak-to-peak voltage of at least 20 V [7].

To achieve a large output power in a standard CMOS technology despite the low transistor breakdown voltage, an impedance transformation is required to transform the 50-Ω load to a lower impedance [8]. Unfortunately, the low quality passives in CMOS, such as *L–C* networks or spiral transformers, fundamentally limit the designer to achieve a high output power when a high transformation ratio is necessary [9]. The distributed active transformer (DAT) allows alleviating the effect of the low-Q passive elements integrated in the output matching network of a standard CMOS process [5], [9], [10] and simultaneously makes it viable to realize a fully-integrated watt-level PAs by using low-breakdown voltage transistors. However, most of the already reported Watt-level CMOS PAs, [5], [7]–[9], [11], [12], do not have sufficient linearity to cope with the LTE linearity requirements so far.

This paper presents one of the first implementations of a fully integrated CMOS PA that has both high output power and lin-

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TABLE I
EVM REQUIREMENTS FOR THE E-UTRA/LTE-UPLINK SIGNALS FOR DIFFERENT CONSTELLATIONS

Constellation	QPSK	16-QAM	64-QAM
EVM-requirement (3GPP v8.3)	17.5%	12.5% (5.6%)	-

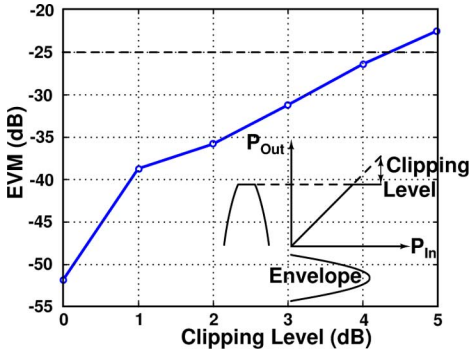

Fig. 1. Simulated EVM with respect to clipping level of an ideal linear amplifier while applying an LTE-signal (16-QAM) with 10-MHz bandwidth and 6.92-dB PAPR.

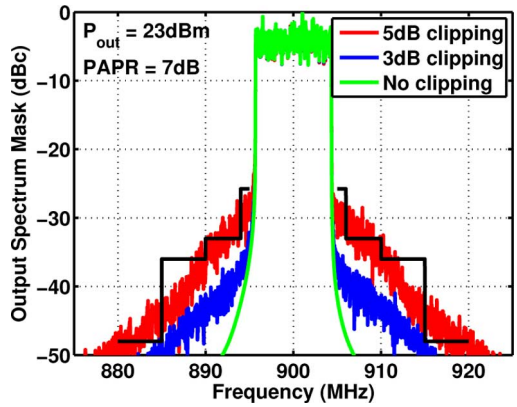

Fig. 2. Simulated output spectrum of an ideal linear amplifier for different clipping levels while applying an LTE-signal (16-QAM) with 10-MHz bandwidth and 6.92-dB PAPR.

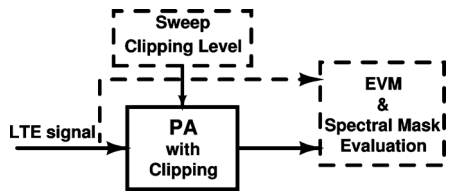

Fig. 3. Flowchart of the system evaluation of the PA with varying the clipping level for LTE applications.

earity required for LTE-applications. The paper is organized as follows: Section II will outline the targeted specifications of the PA based on spectral mask and EVM requirements. Based on these requirements a system analysis is performed. Section III presents a distributed active transformer based RF PA architecture that can allow generation of high output power on-chip while using low-voltage standard CMOS process. Section V explains the details on the PA implementation. The measurement results of the two-stage PA with clover-shaped DAT will be summarized in Section VI with special attention to the linearity requirements. Finally, Section VII concludes this paper.

II. LTE SPECIFICATIONS FOR THE RF PA AND SYSTEM LEVEL EVALUATION

In this section, the required linear peak output power, $P_{\mathrm{peak\_lin}}$, for an LTE PA is investigated. First, the important LTE requirements are discussed.

As mentioned in the introduction, the required average output power from the PA for LTE-applications is 23 dBm, while complying with the LTE 3GPP standard Release 8 EVM and Mask requirements [1]. But the total antenna port average output power may never exceed 23 dBm due to SAR regulations, i.e., class 3 power requirements. Taking into account a 2-dB front-end insertion loss (IL) (switches), a 25-dBm average output power must be feasible at the PA output.

In LTE, the uplink transmission scheme is based on single-carrier FDMA, more specifically DFTS-OFDM, and depending on channel quality, the data is mapped onto a QPSK, 16-QAM, or 64-QAM signal constellation. For signals of this kind, the transmitter must provide large reserves for the peak power to prevent signal compression and thus an increase of the bit error rate at the receiver. The peak power or the peak-to-average ratio (PAPR) of a signal is therefore an important transmitter design criterion. While applying a 16-QAM signal with 10-MHz bandwidth, the PAPR is around 7 dB. For this modulated output signal, the PA must be able to amplify linearly up to 32 dBm output power. However in practice, a certain degradation of the signal is allowed. Therefore PAs having less peak output power can be used to deliver 25-dBm average output power. In this condition, the output of the amplifier is clipped due to saturation.

For each constellation, different EVM limits apply, as shown in Table I. Unlike the QPSK and the 16-QAM modulation, it is still premature to specify the 64-QAM EVM-limit for uplink. In the 3GPP standard, the EVM limit for the 16-QAM modulated signal is defined as 12.5%, but the industry tends to target a much more stringent EVM-limit of 5.6% (-25 dB), as shown in Fig. 1. The other most important linearity constraint for an LTE PA is the spectrum emission mask, as shown in Fig. 2 for a signal with 10-MHz bandwidth. Notice that the power values for the out-of-band emissions vary, depending on the resolution bandwidth (30 kHz and 1 MHz), as is common also in the spectrum emission mask for WCDMA and HSPA. The first 1-MHz band adjacent to the occupied channel has a limit of -18 dBm with a resolution bandwidth of 30 kHz, but this is transformed in the figure to -2.77 dBm/MHz. More details on the spectrum emission mask can be found in [1] (see Table 6.2.4-1).

To investigate the effect of clipping at the output due to saturation of the amplifier, a system level simulation is performed. A PA with hard clipping behavior is simulated to verify the effect of clipping on EVM and output spectrum, as shown in Fig. 3. The constellation of the applied modulated signal is 16-QAM with a bandwidth of 10 MHz. Fig. 1 shows the degradation in EVM with respect to the clipping level of the modulated LTE-signal. Clipping level is defined as shown in Fig. 1. The amplifier still meets the -25 dB EVM limit while the output signal is clipped 4.3 dB.

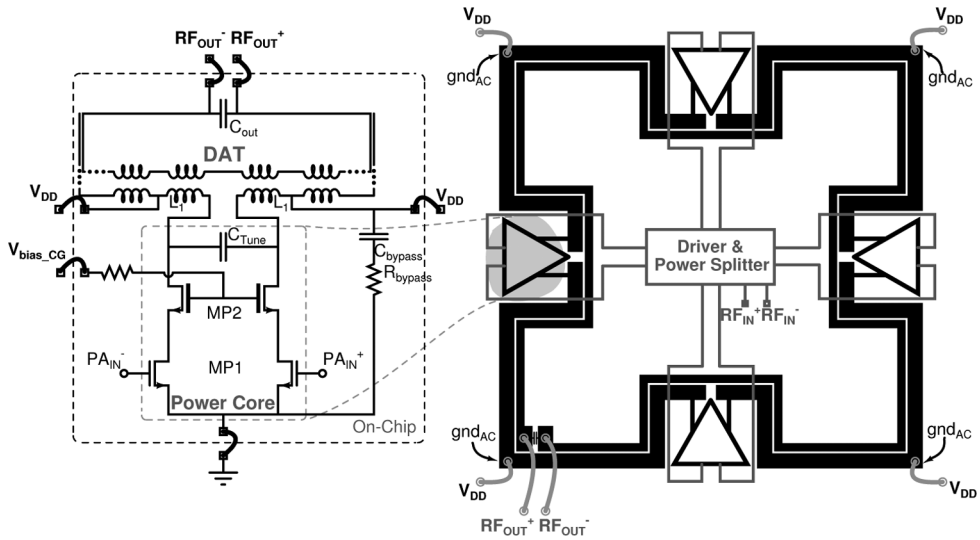

Fig. 4. Schematic of the designed DAT and the circuit design of the main amplifier.

On the other hand, the effect of clipping is more severe for the spectral mask requirements. As shown in Fig. 2, an ideal amplifier meets the spectral mask easily. While clipping the modulated signal 3 dB, the amplifier barely meets the stringent spectrum emission mask.

Finally, to meet the output power requirements while obeying the linearity requirements, the linear peak output power of the amplifier is calculated in (1), where IL represents the front-end insertion loss (switches) and ACL represents the allowable clipping level

$$P_{\text{peak\_lin}} = P_{\text{out\_AVG}} + \text{IL} + \text{PAPR} - \text{ACL}. \tag{1}$$

To achieve the required 23-dBm average output power for LTE-applications, the PA should be able to linearly amplify up to 29 dBm, since the ACL is 3 dB. The efficiency of linear PAs degrades significantly at power back-off. To improve the average efficiency, the PA should satisfy the LTE specifications close to its peak output power level. Thus, in this work, a highly linear PA is designed to obey the LTE-linearity requirements with high average efficiency.

III. DAT-Based PA Design

Section III-A describes the implementation of distributed active transformer. Section III-B explains the design details for the main and driving stage.

A. Distributed Active Transformer

The DAT was first introduced by Aoki in 2002 [9] and the designed clover shaped DAT is shown in Fig. 4. Its primary side consists of four independent unity transformers that are driven by independent differential amplifiers. The RF power is magnetically coupled from the four primary slabs to the secondary winding. At the secondary side of the DAT power combiner, the voltages add up in the voltage domain to achieve the high voltage levels necessary for a watt-level output into the 50-Ω load. The DAT is not only combining the power of the four differential amplifiers, it also transforms the impedance seen by each amplifier [8], [9] and the large voltage swing on the secondary loop does not pose any reliability issue since no transistor electrically connected to the large output swing. More information on reliability of the design PA is given in Section IV.

The distributed active transformer was implemented in the thick top metal (3.2 μM) to maximize the quality factor of both primary and secondary windings. Primary and secondary slabs are separated with the minimal spacing to increase the coupling factor. In other words, the effective resistance loss of the DAT is minimized.

The DAT was optimized for the optimal load using the passive power transfer efficiency. The passive power transfer efficiency was both calculated and simulated using a 2.5-D electromagnetic simulator. The calculation was based on the analysis given in [9]. This efficiency calculation is only depending on the quality factors of both windings and on the coupling factor. This optimization resulted in an optimal width for the inner slab of 32 μm and the outer slab of 52 μm and their quality factors are 21.2 and 14.8, respectively. This resulted in a theoretical maximum efficiency of 77.6%.

The passive power transfer efficiency of a matching network, η, can be calculated as the ratio of the power delivered to the load to the power delivered into the network [13]. In terms of scattering parameters, the efficiency expression becomes

$$\eta = \frac{S12^2}{1 - S11^2}. \tag{2}$$

The simulated passive power transfer efficiency of the DAT, is shown in Fig. 5. The peak passive power transfer efficiency is achieved at the desired operation frequency band, which is close to the calculated efficiency.

Due to the huge voltage swing in the secondary winding of the power combiner, the unwanted coupling from output-to-input is significant and becomes even more important when the driver and driving splitting network are realized inside the DAT-transformer, as shown in Fig. 4. To reduce this coupling, the DAT is slightly dented in the middle into a clover shape in order to minimize the length of the driver lines. In addition, the driver lines

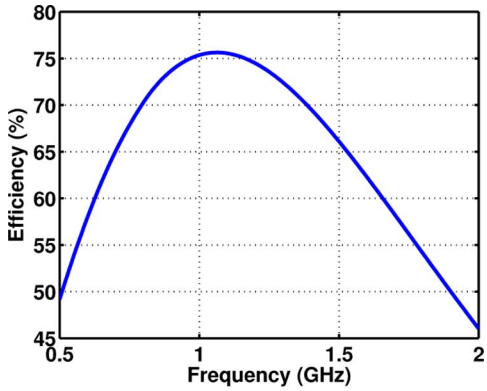

Fig. 5. Passive power transfer efficiency of the DAT versus frequency.

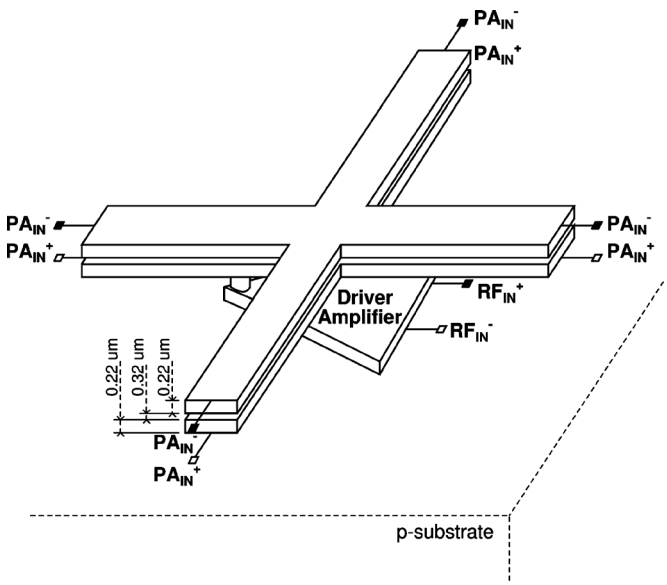

Fig. 6. Driver amplifier and power splitting network.

are realized on top of each other with a spacing of only 0.32 μm, to increase the coupling factor between the driving lines and decrease the coupling from other close by components, as shown in Fig. 6. This resulted in the very high 0.96 driver line coupling factor. Furthermore, considering a cross sectional view of the chip, the driver lines were realized in the middle metals with 2.39 μm separation from the thick top metal, used for the DAT combiner, to reduce the coupling slightly further. Moreover, the driver lines are exactly passing in the middle of each differential amplifier and taken into account the symmetry of both the power splitting network and the clover shaped DAT, the magnetic coupling is minimized. Finally, this resulted in the clover shaped DAT and since not only the main amplifiers but also the driver amplifier are inside the DAT, this design proves to be very area efficient.

B. Main and Driver Amplifier

The clover-shaped magnetically coupled power combiner shown in Fig. 4 is used as the output power combiner. Each main amplifier consists of a push–pull amplifier. The power stage was designed as a Class AB for both good efficiency and linearity.

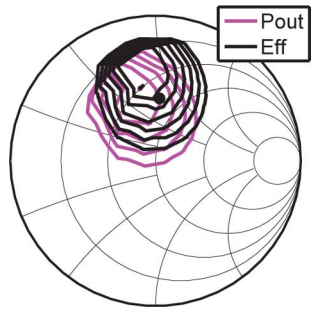

Fig. 7. PAE- and the $P_{\rm out}$-circles of load–pull simulations of the extracted transistors. The "fat" dot represents the transformed impedance seen at the drain of each side of the differential amplifier. The Smith Chart has a normalized impedance of 5 Ω. The step used for PAE- and the $P_{\rm out}$-circles are 4% and 0.5 dB, respectively.

Since the drain of a power core transistor can experience a signal swing at its drain larger than two-times the nominal supply voltage, a cascode structure in the power cell is used so the voltage is divided over both the common source and common gate transistor. The common source transistor has a gate length of 90 nm while the common gate transistor is a 250-nm-thick oxide transistor device. To maximize the efficiency of the amplifier, the 50 Ω load should be transformed in the desired impedance for the optimal operation of the active devices. As already explained, the DAT allows impedance transformation and power combining simultaneously. Additional capacitors $C_{\rm out}$ at the output and $C_{\rm tune}$ at the primary loop and the parasitic capacitors of the transistors itself, fulfill part of the matching network. The gate widths of the transistors are determined by load–pull simulation to achieve the optimum efficiency and output power. This resulted in optimal gate widths of the common source power transistors, MP1, and the common gate transistors, MP2, of 4.6 and 8.6 mm, respectively. Fig. 7 shows the results for both the PAE- and $P_{\rm out}$-circles of the load–pull simulations of the extracted transistors on the Smith Chart. The "fat" dot in Fig. 7 represents the simulated transformed impedance, $(3.6 + j3.8)\Omega$, seen at the drain by the transistors. The main stage achieves a simulated drain efficiency of 54%.

The advantage of differential driving each primary inductor of the DAT, as presented in Fig. 4, is a virtual ground created in the middle of each primary inductor [9]. Consequently, the parasitic leakage inductance of the power combiner is used as the dc feed inductor for the main amplifier.

Another advantage of this differential push–pull technique is the reduced coupling of the second harmonics. First of all, the differential pair substantially rejects the even harmonics. Second, since the corners of the clover shaped DAT are virtual grounds, bypass capacitors, $C_{\rm bypass}$, are used to short the impedance at the second harmonic to the AC ground at two common source transistors from the differential power cell. Every bypass capacitor has a certain quality factor, which is proportional to the ratio of the capacitance by the resistance of the capacitor. Since this bypass capacitor is part of the common mode impedance, lowering the quality factor of the capacitor will reduce the impedance over a wide frequency range and minimize the coupling to the substrate, which helps to stabilize

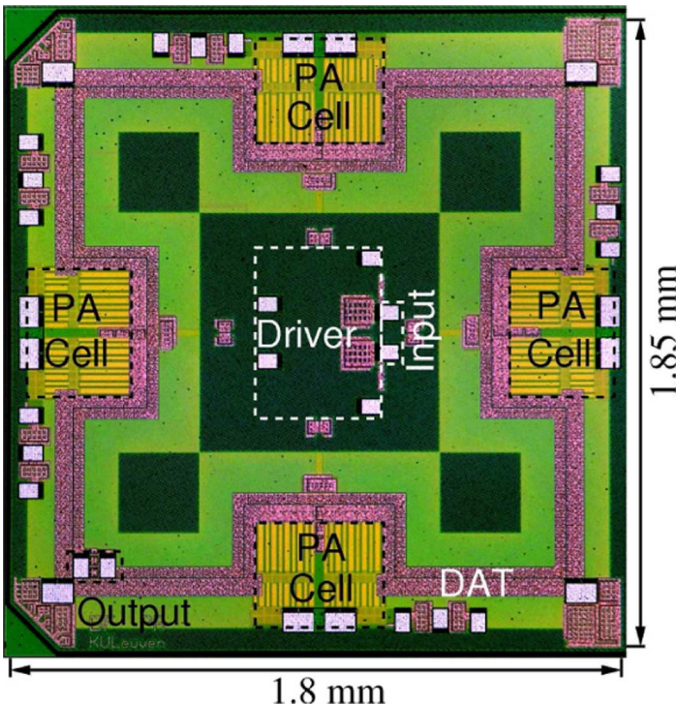

Fig. 8. Die photograph of the quad-core fully integrated CMOS PA.

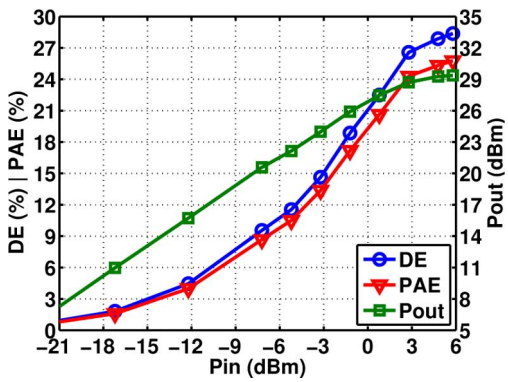

Fig. 9. Measured drain efficiency (DE) (%), PAE (%), and gain (dB) versus input power (dBm).

the RF PA [14]. In order to reduce the third harmonic distortion, the common source transistors are biased slightly below the threshold voltage [15].

Similar to the main stage, the driver amplifiers are designed as Class AB amplifiers to obtain good linearity and efficiency. Again, load–pull simulations were performed in order to guarantee an optimal efficiency performance. In this Class AB driver, the bondwire serves as the RF choke. The input of the PA is fully differential, $\mathrm{RF_{IN+}}$ and $\mathrm{RF_{IN-}}$, as shown in Fig. 4. Matching at the input of the driver stage, to 50 Ω is achieved by tuning the parasitic capacitances of the transistors with the bondwire and together with the stabilizing resistor at the gate, the reflection coefficient is minimized.

IV. Reliability

Reliability is important for the lifetime of the product. The maximum gate-drain voltage stress ($V_{\mathrm{gd\_MAX}}$) on the 1.2-V 90-nm common source transistor is 1.45 V while the 2.5-V-thick

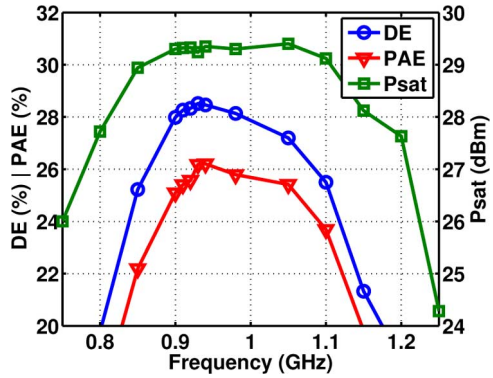

Fig. 10. Measurement results for PAE (%) and DE (%) when the PA reaches its peak output power, P_{sat}, for different operation frequencies.

oxide transistor handles a peak of 2.8-V $V_{\mathrm{gd\_MAX}}$. Therefore, the supply voltage is chosen as 2 V to ensure reliability.

In addition, the metal widths of both the DAT-combiner (32 and 52 μm for the inner and outer slab respectively) and the transistors interconnects and routing are selected and verified to satisfy the electromigration rules at the peak output power. Furthermore, to cope with the high current densities inside the transistors, each interconnect of the transistor subblocks of each PA is constructed using multiple metal layers.

V. Silicon Implementation

Fig. 8 shows a die micrograph of the chip. The fully integrated quad-core CMOS RF PA is implemented in a standard 90-nm CMOS process. The die size is 1.8 mm × 1.85 mm. The PA is designed for the extended GSM-band and for band VIII of the LTE standards.

VI. Measurement Results

A. Measurement Setup

During measurements, the chip is glued on an alumina substrate that is connected to a brass heat sink using thermal conductive glue to allow sufficient thermal dissipation during measurements and to minimize the effects of the thermal variations.

All the pins, including the input and output, are wire bonded on the alumina substrate. All output powers are measured using a power meter.

B. Experimental Results

1) Single-Tone Characterization: To characterize the gain, power and efficiency of the PA, continuous wave signals are applied to the designed PA at 930 MHz. The measurement results, shown in Fig. 9, illustrate that the PA delivers an output power up to 29.4 dBm with a small-signal gain of 28 dB using a 2-V supply voltage. A power added efficiency (PAE) of 25.8% with 28.4% drain efficiency (DE) is achieved.

Fig. 10 shows the performance of the PA across the frequency band. By considering the peak output power, P_{sat}, the 3-dB bandwidth is around 450 MHz. The designed PA still operates at a PAE which is above 24% in the frequency band between 880 MHz–1.09 GHz while achieving an output power of more than 29 dBm and only varying 0.4 dB. In this frequency band, the PAE only varies maximally 2%.

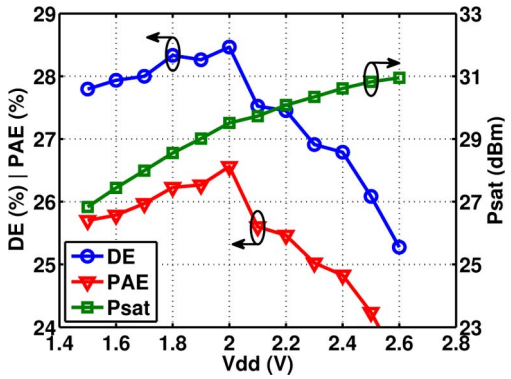

Fig. 11. Measurement results for DE (%), PAE (%) and peak output power (dBm), $P_{\rm sat}$, for different supply voltages, Vdd (V), at 930 MHz.

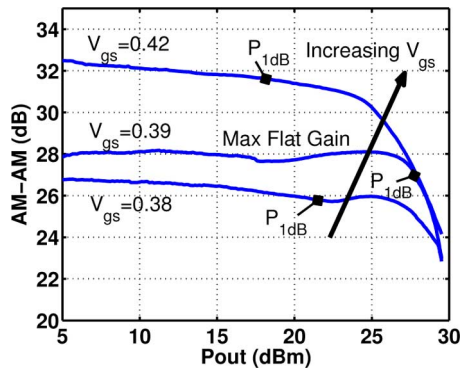

Fig. 12. Measured AM-AM response for different gate bias voltages ($V_{\rm gs} = 0.38$ V, $V_{\rm gs} = 0.39$ V, and $V_{\rm gs} = 0.42$ V) at 930 MHz.

In Fig. 11, the PAE, the drain efficiency and the peak output power, $P_{\rm sat}$, are investigated as a function of the dc supply voltage. The peak PAE is reached at a supply voltage of 2 V, but with a supply voltage of 2.6 V, the PA is able to deliver an output power up to 31 dBm or 1.26 W with a drain efficiency of 25.3% and 23.4%.

2) AM-AM and AM-PM Distortion: Fig. 12 shows the measured AM-AM response for different gate bias voltage at 930 MHz. Class AB amplifiers suffer both from gain expansion and compression. Gain expansion is known as the effect that the gain slightly increases when the input power is increasing. On the contrary, gain compression happens in the transistors because the transistors' change in gate voltage doesn't result in a related change in drain-source voltage. As depicted in Fig. 12, increasing the gate bias voltage, $V_{\rm gs}$, induces some "early" compression, while decreasing the gate bias, causes gain expansion before the gain compression. Both effects should be minimized in order to optimize EVM for both the driver and main amplifier. Hence, the transistors operating in class AB behavior were biased to achieve maximally flat gain and this is illustrated by the mid-curve in Fig. 12. Fig. 12 shows the AM–AM response for different gate bias voltages ($V_{\rm gs} = 0.38$ V, $V_{\rm gs} = 0.39$ V and $V_{gs} = 0.42$ V) which results in 30.97-, 36.28-, and 45.2-mA quiescent current for each transistor respectively. Additionally, the gate bias is slightly adjusted to be as close as possible to the point where the small-signal gain is null, $g_{\rm m3}$, or in other words to minimize the third order intermodulation products [15]. As retrievable

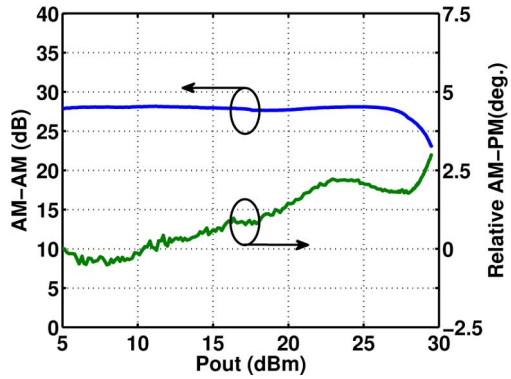

Fig. 13. Measured AM-AM and AM-PM response for the optimal gate bias.

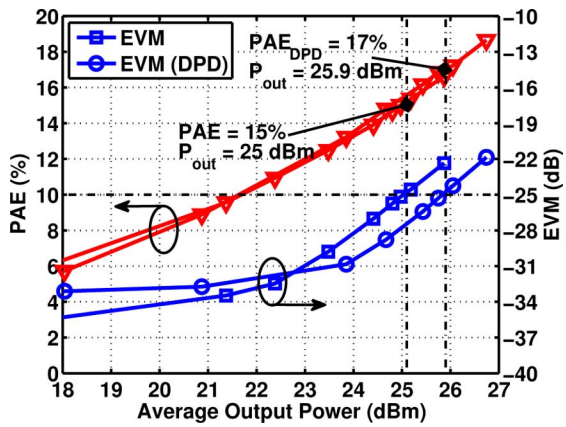

Fig. 14. Measurement results for the PAE (%) and the EVM (dB) with and without predistortion versus average output power (dBm) for the applied uplink 10 MHz LTE-signal at 930 MHz.

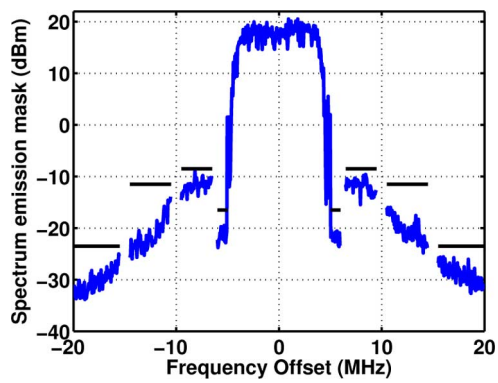

Fig. 15. Measured output spectrum for the applied 10 MHz uplink LTE-signal at 21.6 dBm average output power at 930 MHz.

from Fig. 12, the $P_{\rm 1dB}$ point is at 27.7 dBm, which is only 1.7 dB less than the peak output power.

Simultaneously with the AM–AM distortion, the AM–PM distortion is measured. The effect of the AM-PM distortion is as important as the AM–AM distortion on the EVM. Just as the measurement for the AM-AM distortion, this measurement was realized by applying an unmodulated carrier to the RF PA while increasing the envelope of the applied signal, based on a pulse profile measurement to avoid the impact of the thermal effects on the AM–AM- or AM–PM-curve profile. This measurement was done with the R&S ZVA-40 Network Analyzer. Fig. 13

TABLE II
PERFORMANCE COMPARISON OF WATT-LEVEL LINEAR CMOS RF PAS

Ref.	[14] ISSCC 2009	[16] ISSCC 2010	[17] CICC 2010	[18] ESSCIRC 2011	[19] RFIC 2006	[3] Commercial PA Skyworks	**This Work**
Freq. [GHz]	2.4	2.35	2.4	1.85	0.92	0.85	0.93
Psat [dBm]	30.1	31.5	33.5	32	-	-	29.4
P_{1dB} [dBm]	27.7	27.5	31	-	27	32.5	27.7
Peak PAE [%]	33	25	37.6	15.3	28	29	25.8
Application	WiMAX	WLAN	WLAN	LTE	RFID	WCDMA/LTE	LTE
Modulation	16-QAM 10 MHz	64-QAM -	64-QAM -	16-QAM 20 MHz	- -	- -	16-QAM 10 MHz
Pout@-25dB EVM [dBm]	22.7	21.5|25.5†	23.9|26.4†	24.9	-	-	25.1|26†
PAE@-25dB EVM [dBm]	12.4	9|16†	14|22†	4	-	-	15|17†
Supply [V]	3.3	3.3	3.3	5.5	2.5	5	2
Area [mm^2]	4.32	2.7	6	6	4.8*	-	3.3
Technology	90 nm	65 nm	65 nm	130 nm	250 nm	GaAs	90 nm

* graphically estimated † with DPD

shows the AM–AM and the AM–PM distortion of the designed PA with the optimal bias to achieve maximally flat gain. As seen in the graph, when using the bias on the decision criteria explained above, the phase is only distorted by three degrees over the full operation range up to 29.4 dBm.

3) Measurements With Modulated Signals: The EVM and PAE of the PA for LTE-signals as a function of the desired output power are investigated. The EVM was measured to determine the linearity of the designed PA with the 16-QAM modulated E-UTRA/LTE-signal with a PAPR of 6.92 dB. Fig. 14 shows the EVM and the PAE versus the average output power. The PA satisfies the industry based EVM LTE specifications (5.6%) with 16.5% drain efficiency and 15% PAE while delivering 25 dBm average output power. This is the required output power for LTE taking into account the switch losses at the output, referring to the system analysis in Section II. Thus, the measurement result with the optimal biasing to achieve a flat gain curve, shown by the dotted lines in Fig. 14, already demonstrates that with a peak output power of 29.4 dBm an average output power of 25 dBm is delivered to the load while meeting the stringent industry based EVM-specifications.

With the use of a simple look-up based digital predistortion algorithm (DPD), based on the AM-AM and AM-PM distortion measurements from Fig. 13, and with 1 dB hard clipping, the average output power can be further increased from 25 to 25.9 dBm, while obeying the EVM-specifications. This also increases the PAE from 15% to 17% with a drain efficiency of 18.6%, as shown in Fig. 14. This is a relative increase of 13% in efficiency and almost 1 dB more output power is pushed by the amplifier. With this simple DPD, the output power only increases 1 dB. This again proves the already high inherent linear behavior of this PA.

The PA still satisfies the LTE spectral mask requirements at 21.6-dBm-average output power. The measured spectrum and mask are shown in Fig. 15. The corresponding ACLR1 is -33.4 and -34.2 dB. As proven in the system level LTE analysis in Section II, the spectral mask requirements are more difficult to obey than the EVM requirements and due to noise pickup in the measurement setup at 1–5-MHz-offset from the channel bandwidth, the RF PA delivers slightly less output power while obeying the spectral mask specifications than while obeying the EVM requirements.

To conclude, the performance of designed PA is summarized and compared to state-of-the-art linear CMOS and commercial PAs in Table II. Unlike all PAs mentioned in this table, the commercial PA is designed in GaAs-technology. Unfortunately, this is one of the first measured LTE PAs for the LTE band VIII while most of the PAs are designed for higher operation frequencies and make use of a higher supply voltage to reach the watt-level output power. In this table, the performance of the designed PA is summarized and shows that the PA delivers higher output power and achieves higher efficiency without any predistortion technique while obeying the EVM-linearity requirements (@-25-dB EVM or 5.6% EVM) for the LTE communication standard. And all this in a very limited area.

VII. CONCLUSION

In this paper, the linearity requirements for PAs targeting the LTE-performance are investigated. A two-stage watt-level fully integrated RF PA in 90-nm CMOS technology competent of achieving the LTE-performance requirements, is demonstrated. To achieve the watt-level output power, a clover shape DAT combiner is presented. And the driver stage and power splitting network are completely constructed inside the DAT. The PA delivers 29.4-dBm saturated output power with 25.8% PAE using 2-V supply. While applying an uplink LTE signal, the PA produces 25 dBm of average output power with 15% PAE while obeying the stringent EVM-specifications.

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