Wideband and Efficient Watt-level SiGe BiCMOS Switching Mode Power Amplifier Using Continuous Class-E Modes Theory

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***Abstract* — In this paper, a generic, wide-band switch mode power amplifier (SMPA) design approach is developed based on the continuous class-E modes theory. A watt level, 1.3-2.2 GHz SiGe BiCMOS class-E SMPA is realized for experimental verification. The prototype provides collector efficiencies higher than 70% and output power levels higher than 29 dBm across 1.3-2.2 GHz band, fully confirming the validity of the proposed design approach.**

***Index Terms* — CMOS, class-e, efficiency, SiGe, wide-band**

I. Introduction

In recent years switch mode power amplifier (SMPA) based digital/polar radio transmitter architectures have shown great potential for energy efficient amplification of amplitude modulated realistic communication signals [1]–[3]. RF bandwidth of such transmitters are typically determined by the bandwidth of the final output SMPA stage. Wide-band SMPAs are therefore necessary components for realization of multi-band, highly efficient digital transmitters for the emerging/future communication standards.

Class-E is the best known/used SMPA due to its well proven high efficiency and simple realization. Wide-band class-E PA design requires the necessary load impedances to be provided versus frequency to satisfy the switching conditions. The optimal impedances are found via well established design equations, where the fundamental and the second harmonic impedances have the highest impact on the efficiency and output power [4]. Wide-band RF class-E PA design therefore boils down maintaining fixed fundamental and second harmonic impedances over the band.

In wide-band class-E PA designs, the fundamental tone impedance may be kept fixed over wide bandwidths by incorporating multi-section low pass filters in the load networks [5], [6]. However, this kind of filters typically exhibit very sharp out of band frequency response, making it very difficult to provide a fixed second harmonic impedance [5], and therefore limiting the achievable bandwidth.

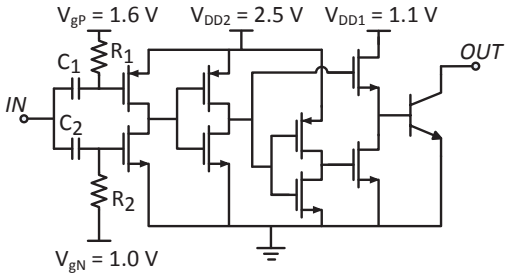

Fig. 1. Schematic of the active power switch. On-chip decoupling capacitors are not shown for the sake of simplicity.

Recently, the authors have theoretically proven that the class-E switching conditions can actually be satisfied for different continuous combinations of the fundamental tone and second harmonic switch impedances [7]. The extended impedance design space hence allows some variation for the fundamental and second harmonic impedances versus frequency creating a very important possibility for design and realization of wide-band class-E PAs.

In this paper, a novel wide-band class-E design approach is developed utilizing the extended design space provided by the continuous class-E modes theory. The technique is demonstrated by design of a watt-level, 1.3-2.2 GHz continuous class-E modes PA, covering several LTE bands. The active switching device for the class-E is realized in NXP's QUBIC4X SiGe BiCMOS process, while the load network is realized off-chip on a teflon substrate. First the BiCMOS chip design is treated.

II. Active switch design in BiCMOS Technology

In Fig. 1 the chip schematic is shown. The output power switch for the class-E is implemented using a SiGe HBT with 13 V collector-base breakdown voltage (BV_{CBo}). The total emitter length of the power bar is 4.96 mm, where the emitter width is 0.4 μm. It is also important to mention that 50 mΩ of emitter ballasting resistance is used to improve the thermal stability. The power bar provides

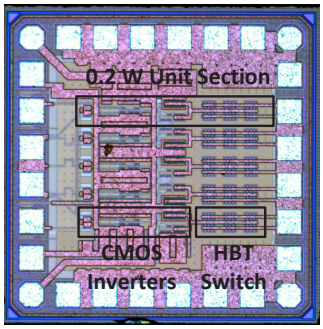

Fig. 2. Chip photo, the dimensions are 1040x1040 μm.

a maximum current level (I_{max}) of 1.2 A and has a total output capacitance (C_{out}) of 4.5 pF, which is considered as part of the continuum class-E load network in the next section.

Three stages of inverters are implemented as drivers using 0.25 μm 2.5 V CMOS transistors, see Fig. 1. The inverter drivers ensures switching the HBT on and off with short transition times. Due to high power consumption/low speed of the the PMOS devices, the last inverter stage is implement using two NMOS devices and a conventional inverter. The delay of the inverter driving the bottom NMOS device is then compensated in the layout to prevent crossbar currents. The last NMOS-only stage is operated at a drain-source bias of 1.1 V, which is sufficient to turn the HBT switch on and off and hence no extra power is wasted for switching. The preceding inverter stages are biased with nominal 2.5 V bias.

A large chip area is needed to achieve a watt-level output power. The layout should therefore be made carefully avoiding large interconnect parasitics. For instance, the harmonics in the square shaped inverter output signals may easily be filtered-out by large interconnect parasitics. The HBT power bar is therefore divided into five equal-sized sections and separate pre-drivers are implemented for each, ensuring small interconnect parasitics, see Fig. 2.

III. Load network design for continuous class-E modes PA

The load networks of conventional RF class-E PAs, see Fig. 3, are designed to provide the optimal fundamental and second harmonic switch impedances calculated via well-established design equations [8]:

$$Z_1^S = (1.52 + j1.11)R \quad (1)$$

$$Z_2^S = -j5.45R/2 \quad (2)$$

where $R = 0.5768V_{CC}^2/P_{out}$. On the other hand, in [7], it is analytically shown that the class-E switching conditions can be satisfied for different continuous combinations of

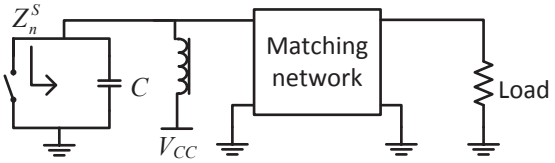

Fig. 3. Generic single ended switch mode power amplifier schematic. Symbol Z_n^S denotes the impedance provided by the load network at $n\omega_o$, where n is the harmonic index. The unavoidable output capacitance of the switching transistor is represented by C.

$\{Z_1^S, Z_2^S\}$, revealing an additional degree of freedom for the design. A wide-band load network design approach, which utilizes the extended design space, is thus developed in this section.

A. High-efficiency impedance trajectories

High-efficiency $\{Z_1^S, Z_2^S\}$ trajectories that satisfies the class-E switching conditions have been derived in [7]:

$$Z_1^S(\phi_1) = R\frac{(1+jx_1)\pi}{\pi + j2(1+jx_1)\cos^2\phi_1} \quad (3)$$

$$Z_2^S(\phi_1) = j\pi x_2 R/(\pi - 4x_2\cos^2\phi_1) \quad (4)$$

where $R = 8\sin^2\phi_1 V_{CC}^2/(\pi^2 P_{out})$ and

$$x_1 = \frac{16\pi\cos^2\phi_1\cot\phi_1 + 2\pi\sin 2\phi_1 + 3\pi^2 - 32}{12\pi\cos^2\phi_1}$$

$$x_2 = \frac{\pi\sec^2\phi_1}{24(\pi - 2\tan\phi_1)}\Big[4\sin\left(2\tan^{-1}(2\cot\phi_1)\right) + 3\pi + 2\Big(\cos\left(2\tan^{-1}(2\cot\phi_1)\right) - 2\Big)\tan\phi_1\Big]$$

The parameter ϕ_1 is a new design variable that denotes the phase of the fundamental tone load current. In principle, ϕ_1 can take any value in $[0, 180^o]$, however, only for the range $\phi_1 \in [43^o, 78^o]$ the maximum values of the switch waveforms are comparable to those of the conventional class-E mode waveforms [7].

The supply voltage V_{CC} should also be determined for calculation of the impedance trajectories. The maximum switch voltage is well approximated by $3.6V_{CC}$ for relevant $\phi_1 \in [43^o, 78^o]$ range. The V_{CC} is thus set to 3.7 V for a reliable operation ($BV_{CBo} = 13$ V). The output power, P_{out}, is set to 1 W and kept constant for all ϕ_1 values. With these settings, the resulting maximum switch current is below 1 A, which can easily be provided by the HBT power bar ($I_{max} = 1.2$ A). It is also relevant to mention that the conventional class-E mode, i.e. $\phi = 57.5^o$, requires a maximum switch current of around 0.85 A for the same power level. The calculated optimal impedance trajectories are plotted in Fig. 4.

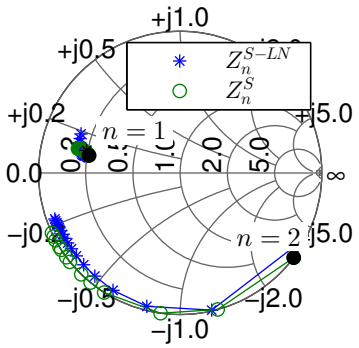

Fig. 4. Calculated and synthesized switch impedances, $Z_n^S(\phi)$ $Z_n^{S-LN}(f)$ respectively, where term n denotes the harmonic index. The black markers denotes the impedance points at the lowest ϕ and f, where $\phi \in [43^o, 78^o]$ and $f \in [1.4, 2.2]$ GHz.

B. Load network synthesis

The $\{Z_1^S, Z_2^S\}$ impedance trajectories that provide high efficiency and constant output power are now known. A different combination of $\{Z_1^S, Z_2^S\}$ may then be provided by the load network at each frequency point. The following error function is thus defined for optimization of the load network parameters:

$$\alpha = \sum_{n=1}^{2} \frac{1}{\max|Z_n^S(\phi_{1i})|} \sum_{i=1}^{N} |Z_n^{S-LN}(f_i) - Z_n^S(\phi_{1i})| \tag{5}$$

where ϕ_{1i} values are also considered as optimization variables since Z_n^S are frequency independent. The symbol Z_n^{S-LN} denotes the frequency dependent impedance provided by the load network, see Fig. 5. For our case, $f \in [1.4, 2.2]$ GHz and the number frequency points used for the optimization is $N = 17$.

To find a proper load network topology that yields a low α, one may start with a highly complex topology and reduce the number of elements gradually until a suitable complexity/performance trade-off is obtained. A load network consisting of several cascaded stages of transmission lines and shunt stubs is therefore selected to start with. After a few trials, the topology in Fig. 5 is found, which yields a very good fit between the synthesized and calculated switch impedances, see Fig. 4. It is also important to stress that, only small signal linear circuit simulations are required for design of the load network, enabling a fast and robust design cycle.

IV. Experimental Results

The load network shown in Fig. 5 is implemented off-chip on Duroid 5870 substrate that has a relative dielectric constant of 2.3 and thickness of 5 mil. Electromagnetic simulations of the transmission lines and the bond wires

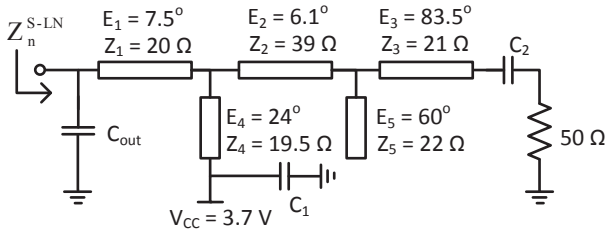

Fig. 5. Schematic of continuum Class-E load network, where C_{out} represents the output capacitance of the HBT.

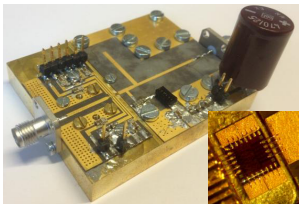

Fig. 6. Fabricated continuous class-E modes PA prototype.

are also performed using Agilent's Momentum and FEM simulators, respectively, to guarantee good agreement between measurements and simulations across the band.

For construction of the PA, the die and the load network are soldered on a brass fixture. Also, using Au plated alumina bars, the ground plane is brought to the chip height to ensure low emitter and source bond-wire inductances. The final constructed PA is shown in Fig. 6.

The bias settings used for the measurements were $V_{CC} = 3.7$ V, $V_{DD1} = 1.0$ V, $V_{DD2} = 2.5$ V, $V_{gN} = 1$ V, $V_{gP} = 1.6$ V. Sinusoidal input signals were used for the characterization, where a fixed available power level of $P_{av} = 6$ dBm was used for all of the measurements.

The efficiency results are shown in Fig. 7, where a very good agreement is achieved between simulations and measurements. The prototype provides a virtually flat efficiency profile across 1.3 GHz and 2.2 GHz band. The measured collector efficiency is better than 70% and the total line-up efficiency, which also includes the DC and RF input powers consumed by the CMOS drivers, $\eta_{tot} = (P_{out} - P_{av})/P_{DC-tot}$, is higher than 50%.

The output power results are shown in Fig. 8, where the measured output power is higher than 29 dBm across 1.3-2.2 GHz. It is also important to mention that output variation is less than 1.5 dB across the band. As seen from the figure, the discrepancy between the simulated and measured power is larger for the higher frequencies. Post simulations indicated that this is mainly due to underestimation of the collector bond-wire lengths. The gain curve is not presented since it resembles the output power curve with a 6 dB offset.

TABLE I
COMPARISON WITH STATE-OF-THE-ART CLASS-E PAS

	Technology	Load Network	f (GHz)	Num. of stages	Gain (dB)	P_{out} (dBm)	η (%)	η_{tot} (%)
2005, [9]	130 nm CMOS	On-chip	1.4-2	2	n/a	> 23	> 62	> 59
2006, [10]	IBM 6HB SiGe BiCMOS	On-chip	0.5-1.2	1	> 7.2	> 17.2	n/a	> 50
2012, [11]	65 nm CMOS	Off-chip	0.55-1.05	2	> 16	> 30	> 67	> 52
This work	NXP 0.25 μm SiGe BiCMOS	Off-chip	1.3-2.2	4	> 23	> 29	> 70	> 50

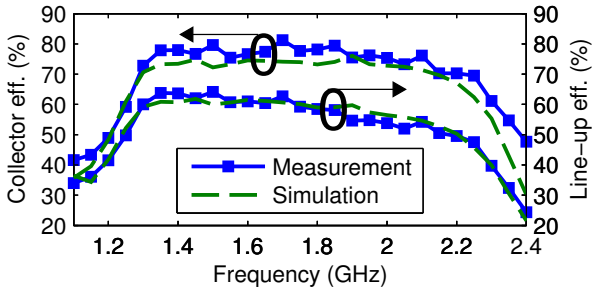

Fig. 7. Efficiency versus frequency.

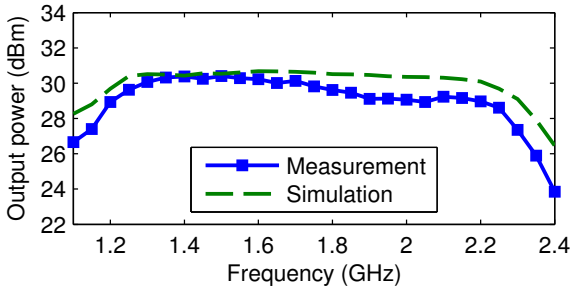

Fig. 8. Output power and gain versus frequency.

In Table I, the measurement results are summarized and compared with state-of-the-art CMOS/BiCMOS based wide-band class-E PAs. As seen from the table, even considering that the center frequency is the highest for the prototype, the efficiency-bandwidth performance stands out. This indicates that the proposed design technique may provide a very useful toolbox for practical realization of wide-band highly efficient class-E PAs in diverse applications.

V. CONCLUSIONS

Class-E operation can be maintained over a wide frequency range by mapping the inherent variation of the load impedances to optimal impedance trajectories calculated via continuous class-E theory. A generic, wide-band class-E design methodology is developed based on this principle. The proposed design technique and careful implementation enabled a watt level SiGe class-E PA with excellent efficiency-bandwidth performance.

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