A Highly Linear and Efficient 28 GHz Stacked Power Amplifier for 5G using Analog Predistortion in a 130 nm BiCMOS Process

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***Abstract*—In this paper a highly linear, analog predistorted 28 GHz stacked power amplifier (PA) for 5G is presented. A 130 nm BiCMOS process is used for the circuit realization. The usage of a diode predistorter for analog predistortion is investigated for the stacked PA design and compared to a circuit without predistortion. It is shown, that the linearity of the stacked PA is significantly improved compared to a conventional biasing topology at almost no additional layout size. The measurement shows an overall large signal gain of 14.6 dB and the simulated power added efficiency (PAE) reaches 26 %. The circuit yields a measured input-referred 1 dB compression point (P_{1dB}) of 1.5 dBm. Hence, the amplifier is able to provide 16 dBm output power at P_{DC}=40 mW. The simulated circuit performance fits well with the measured results.**

***Index Terms*—Analog Predistortion, Power Amplifier, 5G**

I. Introduction

Recent innovations of the 5th generation of mobile communication have shown the need for highly linear and efficient PAs in order to achieve a high IP3 and P_{1dB} [3]. New semiconductor technologies yield lower breakdown voltages due to the trend of downsizing the transistor size, consequently [4]. As the output power mainly relies on the current and voltage drop across the circuit, it is either possible to massively interconnect several transistors in order not to exceed the breakdown voltage and to draw the current which is needed to achieve the desired output power of a single stage. The other way round there is the possibility to stack *n* transistors in order to achieve the desired output power by using a *n* times higher voltage drop across the transistor stack [1], [4]. Besides reaching the necessary output power, there are high requirements on the circuit linearity [3]. In this work a stacked transistor topology is examined for a 28 GHz PA. The usage of a diode predistorter is investigated for analog predistortion in order to improve the linearity of the stacked circuit topology. A comparison between the diode predistorter and an alternative biasing scheme is carried out for the stacked PA.

II. Technology

A 130 nm BiCMOS process is used for the circuit realization. The process is characterized by a ft/fmax=250/370 GHz. For all transistors a double base configuration is used in order to reduce the ohmic input resistance. The supply voltage of the circuit is set to 4 V and the transistors are biased in a way not to exceed the maximum collector-emitter breakdown voltage. The circuit yields a measured DC power consumption of 40 mW (36 mW simulated).

III. Stacked PA Design

Fig. 1 shows the three transistor stacked architecture which is used for the realization of the PA. The common emitter stage

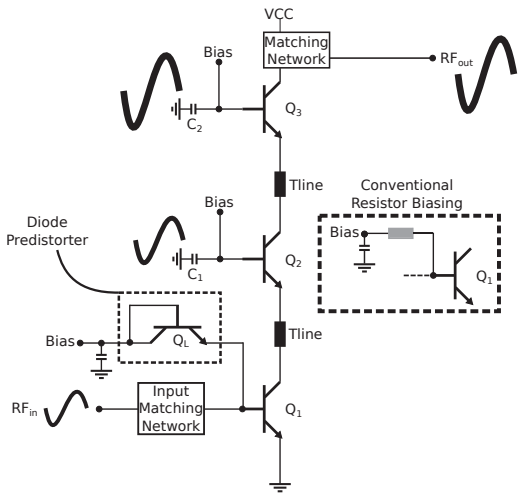

Fig. 1. Simplified schematic, showing the design of the stacked PA.

Q_1 constitutes the input of the PA while Q_2 and Q_3 represent non classical base-circuits. For a classical base circuit Q_2 and Q_3 would be tied to perfect RF ground by using large

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capacitances. In case of a stacked PA architecture this is no longer the case. A voltage swing at the base is desired. Hence, the base of Q_2 and Q_3 are tied to finite impedances by using the capacitances C_1 and C_2 [4], [5]. Q_L is diode connected and acts as a rectifying element in the biasing circuit for analog predistortion [2]. In order to maximize the output power and the efficiency of the amplifier it is necessary to use an interstack matching. This is realized with series and shunt inductances as well as capacitances.

IV. Gain and Phase Compression in Analog Circuits

Fig. 2 shows the basic scheme of gain and phase compression. In the middle, gain and phase compression can be observed at a high input power level. This is the usual case for a PA. To improve this behavior, a topology which offers gain and phase expansion is necessary in front of the amplifier. In case of this paper, a diode predistorter is used as an analog predistortion element. The summation of both, the input signal and the predistorted signal yields an improved large signal linearity [1].

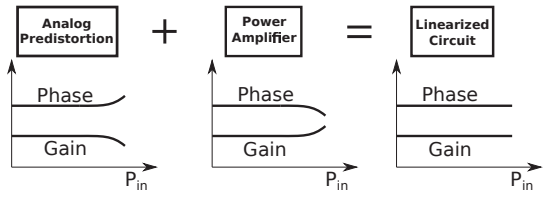

Fig. 2. Schematic, showing the basics of gain and phase compression [1].

V. Analog Predistortion Using a Diode Predistorter

Compared to CMOS, bipolar transistors require an appropriate biasing current at the base in order to keep the transistor in the desired operational point. According to Fig. 1, two possible biasing schemes are investigated:

First, it is possible to use a resistor in the biasing path right in front of the base in order to supply the bipolar transistor with a certain base current and to set the base potential. As the input power increases, the rectified current of Q_1 leads to a higher base current. Hence, the voltage drop across the biasing resistor will be higher. In this way, the base-emitter voltage of Q_1 drops as the input power increases: the PA drives into compression [2].

Second, a diode is used in the biasing network for analog predistortion in order to improve the limiting compression behavior by using a resistor. As the input power increases, the rectified dc current of the diode predistorter (base-emitter diode) Q_L in Fig. 1 increases. Hence, the bias point of the diode is shifted and the voltage drop across the diode decreases [7]. In this way, the diode compensates the compression characteristic of Q_1 as the base-emitter voltage across Q_1 stays almost constant at higher power levels. Therefore, the large signal linearity shows an improved behavior. Besides, the phase distortion of the circuit is improved, too. The diode predistorter yields a positive phase distortion with increasing input power. In this way, the predistorter counteracts to the negative phase distortion of Q_1. Hence, the diode predistorter acts as an analog predistortion circuit which improves both, gain-compression and phase distortion [2], [6], [7]. In Fig. 3 the change in the base-emitter voltage of Q_1 is simulated for increasing input power levels. The dashed curve shows the result with a resistor in the biasing network and the solid curve the result by using the diode predistorter. It can be seen that the base-emitter voltage of Q_1 decreases rapidly for higher input power levels when using the classical resistor biasing scheme. In comparison, the same circuit with the diode predistorter yields a higher base-emitter voltage for higher input power levels and therefore a better large signal linearity.

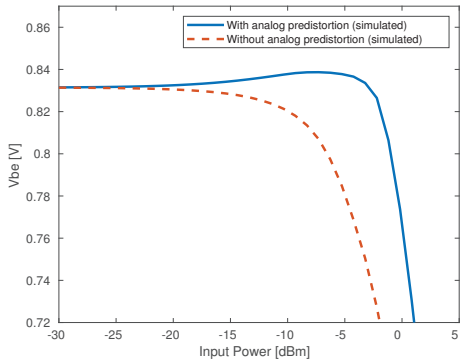

Fig. 3. Simulation, showing the comparison between the change in vbe of Q_1 for increasing input power levels by using the diode predistorter (solid line) and a resistor in the biasing network (dashed line).

The simulation in Fig. 4 shows a comparison of the resulting power gain and input-referred P_{1dB}. By using a resistor instead of the diode predistorter the circuit yields an input-referred P_{1dB} of −9.51 dBm. With diode predistorter, the circuit yields an input-referred P_{1dB} of −3.12 dBm. Hence, the linearity is significantly improved by 6.39 dB.

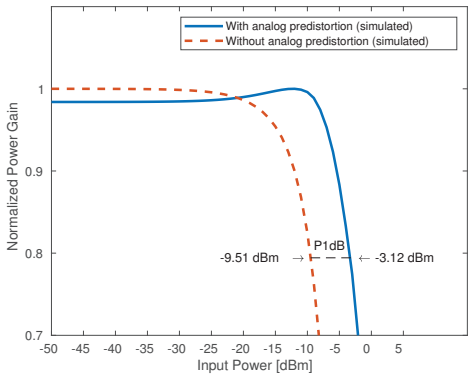

Fig. 4. A comparison of the input-referred P_{1dB} is shown. The blue curve (solid line) shows the input-referred P_{1dB} by using the diode predistorter and the red curve (dashed line) the input-referred P_{1dB} of the stacked PA with a resistor in the biasing network. The simulation frequency is 28 GHz.

A comparison of the simulated and measured power gain at 28 GHz is shown in Fig. 5. Compared to the simulation (power gain 15.2 dB, input P_{1dB} −3.12 dBm), the measured gain is lower (14.6 dB) and the input-referred P_{1dB} is slightly higher (1.5 dBm). The power added efficiency (PAE) is defined as [1]:

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{DC}}} \tag{1}$$

The maximum PAE is usually reached close to the P_{1dB}. In case of this work, the simulated maximum PAE yields 26 % at an input power level of −1 dBm.

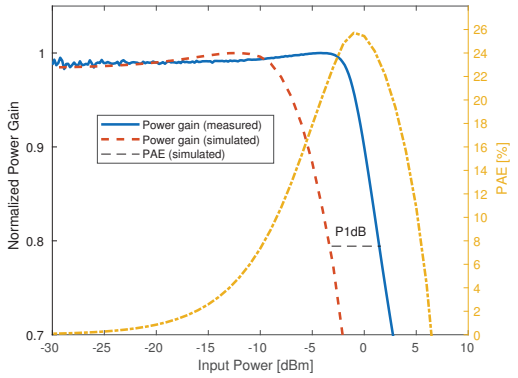

Fig. 5. Simulated and measured power gain and simulated PAE. The simulated input-referred P_{1dB} is −3.12 dBm. Compared to the simulation, the measured input-referred P_{1dB} is 1.5 dBm. The simulated PAE reaches 26 %.

Fig. 6 shows the comparison of the simulated and measured S-parameters. The circuit achieves a measured power gain of 14.6 dB (s_{21}) and the in- and output matching (s_{11}, s_{22}) yields an adaption better than −12 dB in the desired frequency range. Compared to the simulation, the measured S-parameters are slightly shifted towards higher frequencies. This behavior can be attributed to parasitic inductances and capacitances in the chip layout. In total, the simulated and measured parameters are in good agreement.

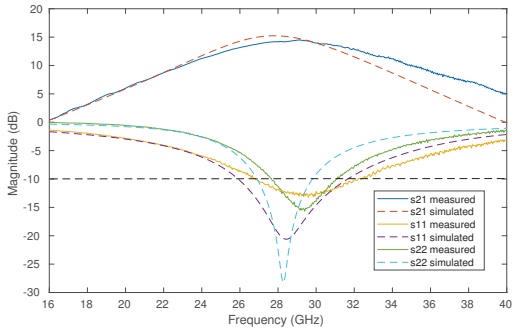

Fig. 6. Simulated and measured S-parameters of the designed PA. The simulation results are in good agreement with the measurement results.

Fig. 7 shows a micrograph of the designed IC. The picture shows the dc supply pads as well as the GSG (Ground Source Ground) pads at the in- and output of the PA. Further, the inductances for in- and output matching can be seen. The complete chip size is 930 µm×930 µm and the PA itself has a size of 220 µm×400 µm.

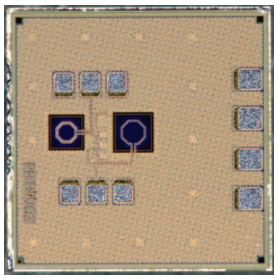

Fig. 7. Micrograph, showing a picture of the designed PA. The PA has a size of 220 µm×400 µm.

VI. Conclusion

In this paper a 28 GHz predistorted stacked PA is presented. The chip was fabricated and evaluated. The PA is linearized by using a diode in the biasing network. A comparison between different biasing schemes is carried out. The input-referred P_{1dB} is significantly improved by 6.39 dB compared to the case with a conventional resistor biasing while the additional layout effort is insignificant. Hence, this work opens up a multitude of new design approaches for the 5G PA design.

Acknowledgment

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References

[1] Andrei Grebennikov, 'RF and Microwave Power Amplifier Design - Second Edition', in Mc Graw Hill, pp. 509-512, 2015.

[2] Bo Shi, 'Mixer Linearization Using Dynamic Bias Circuit with an Integrated Diode predistorter', in IEEE Region 10 conference, 2016.

[3] D.Y.C. Lie, J. C. Mayeda and J. Lopez, 'Highly Efficient 5G Linear Power Amplifiers (PA) Design Challenges', in IEEE international Symposium on VLSI Design, 2017.

[4] Michele Squartecchia, Tom K. Johansen, Virginio Midili, 'Design Procedure for Millimeter-wave InP DHBT Stacked Power Amplifiers', in IEEE Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop, 2015.

[5] Thomas J. Farmer, Ali Darwish, and Mona E. Zaghloul, 'A 2.4 GHz SiGe HBT High Voltage/High Power Amplifier', in IEEE Microwave and Wireless Components Letters, vol. 20, no. 5, pp. 286-288, May 2010.

[6] Toshihiko Yoshimasu, MasanoriAkagi, Noriyuki Tanbe and Shinji Hara, 'An HBT MMIC Power Amplifier with an Integrated Diode predistorter for Low-Voltage Portable Phone Applications', IEEE Journal OF SOLID-STATE CIRCUITS, vol. 33, no. 9, pp. 1290-1296, 1998.

[7] Kazuhisa Yamauchi, Kazutomi Mori, Masatoshi Nakayama, Yasuo Mitsui, and Tadashi Takagi, 'A Microwave Miniaturized Linearizer Using a Parallel Diode', IEEE MTT-S International Microwave Symposium Digest, pp. 1199-1202 ,1997.