A 3.4 GHz to 4.3 GHz Frequency-Reconfigurable Class E Power Amplifier with an Integrated CMOS-MEMS LC Balun

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***Abstract* — A monolithically integrated differential class E power amplifier capable of dynamically switching between 3.4 GHz and 4.3 GHz operation has been designed and fabricated in a 0.35 µm BiCMOS process; this power amplifier also includes an integrated CMOS-MEMS variable capacitor enabled LC balun for differential to single-ended conversion. The power amplifier achieves a maximum output power of 19.1 dBm and a maximum power added efficiency of 15.1% with a supply voltage of 3.3 V.**

***Index Terms* — Power amplifiers, power combiners, microelectromechanical devices.**

I. Introduction

With the abundance of wireless standards, there is a desire to make RF front-ends frequency-reconfigurable. Of particular importance is the power amplifier which typically dominates the power consumption of the RF front end and frequency-reconfigurability is needed to maximize output power and efficiency at frequency extremes. Frequency-reconfigurable power amplifiers reported in the past [1]-[2] are not monolithically integrated although the tunable element itself in [2] is integrated and the entire power amplifier holds promise for future integration. This paper presents a frequency-reconfigurable power amplifier that is monolithically integrated.

With monolithic integration comes the strong motivation to use power combining techniques in order to deliver high power from low-breakdown voltage devices [3]-[4]. It is logical that a frequency-reconfigurable power combiner would be needed. Of the several power combining techniques, the LC balun (see Fig. 1) is best suited to be made frequency-reconfigurable with a monolithically integrated CMOS-MEMS variable capacitor. Not only is an LC balun useful for differential to single-ended conversion, but it also has a higher power enhancement ratio than an L-match for achieving high output power with low transformation loss [5]. With the LC balun, this new power amplifier is able to outperform a previously designed monolithically integrated frequency-reconfigurable power amplifier [6].

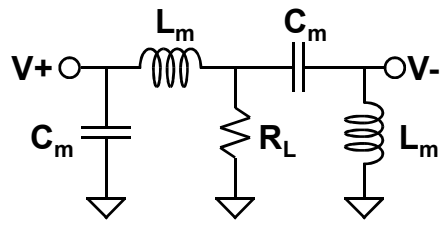

Fig. 1. Lattice-Type LC Balun.

II. Tunable Elements

A. CMOS-MEMS Variable Capacitor

The CMOS-MEMS variable capacitor (see Fig. 2) is fabricated in a 0.35 µm BiCMOS process along with CMOS circuitry, and the CMOS-MEMS post-process [7] releases the MEMS structures without any additional masks. This CMOS-MEMS post-processing uses the existing metal as a mask by removing any oxide and 50 µm of the silicon substrate that is not covered by metal. In this way, the MEMS variable capacitor is monolithically integrated with CMOS. The CMOS-MEMS variable capacitor has interdigitated capacitance beams consisting of the back-end-of-line metal dielectric stack that form the basis of the variable capacitance. Because these capacitance beams are released by the CMOS-MEMS

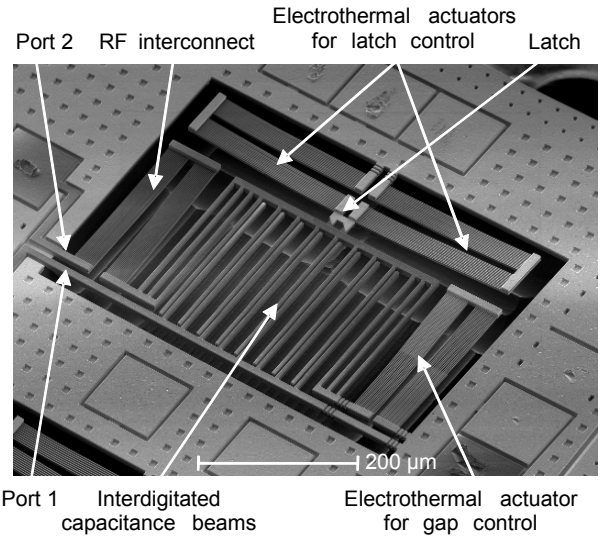

Fig. 2. CMOS-MEMS Variable Capacitor.

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post-process, the gap between the beams, and hence the capacitance of the device, can be varied by electrothermal actuators that use embedded polysilicon resistors. A mechanical latch can maintain the capacitance position so that the device does not burn static power. This CMOS-MEMS variable capacitor has a tuning ratio of 6.9:1, a quality factor of 28 at 3 GHz [8].

B. Switched Capacitors

A switched capacitor is simply a capacitor in series with a switch. The main drawback of a switched capacitor is that there is an unfavorable tradeoff between its quality factor and tuning range. The switch would be implemented as a transistor and a large transistor is desired for a high quality factor when the switch is ON. However, when the switch is OFF, the capacitance consists of the series combination of the fixed capacitance and the parasitic capacitance of the transistor, and therefore a small transistor is desired for a large tuning range (see Fig. 3).

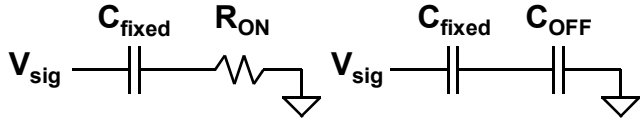

Fig. 3. Simplified model of a switched capacitor when ON (left) and OFF (right).

A differential switched capacitor can win back a factor of two in either tuning range or quality factor by taking advantage of the fact that the switch can be shared and that a differential ground exists in the middle of the switch (see Fig. 4). For the same sized switch and capacitor (but with two capacitors), the OFF capacitance of the switch is the same as before, but the ON resistance of the switch is half of what it was before because the ground is now half a channel length closer than before, resulting in a doubling of the quality factor (see Fig. 5). Tiny grounding transistors ensure that the source of the switch is grounded so that a maximum gate overdrive voltage can be applied to the gate of the switch to minimize the ON resistance of the switch.

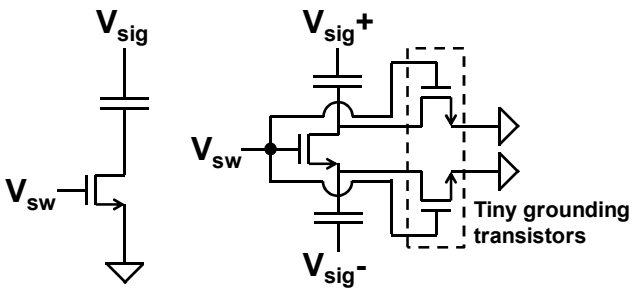

Fig. 4. Single-ended switched capacitor (left) vs. differential switched capacitor (right).

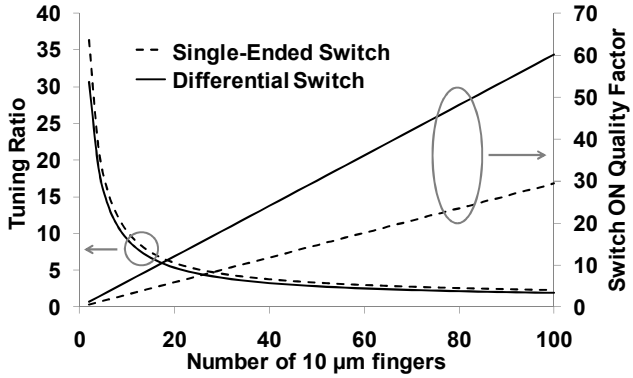

Fig. 5. Simulated quality factor and tuning ratio of a switched capacitor as a function of switch size: single ended vs. differential. Capacitor value = 1 pF. Frequency = 3 GHz.

C. Use of Tunable Elements

Although the CMOS-MEMS variable capacitor has a quality factor of 28 at 3 GHz and a tuning range of 6.9:1, a single device measures roughly 400 μm by 500 μm but only has a variable capacitance of 54 fF to 372 fF and should only be used where the benefits justify the added area such as in an LC balun. If the LC balun requires a series capacitance of 400 fF at 4 GHz, the impedance of the capacitor is –j*100 Ω, and if an optimistic quality factor of 10 is assumed for a switched capacitor, then there are 10 Ω of series resistance in the capacitive branch of the LC balun. Such a large series resistance would severely degrade the power amplifier's overall efficiency and therefore a CMOS-MEMS variable capacitor is used in the LC balun. The CMOS-MEMS variable capacitor also has the added benefit of having a low parasitic shunt capacitance. The area-efficient switched capacitor is used for all other variable capacitors in the power amplifier.

The use of MOS or diode varactors was considered but switched capacitors were ultimately chosen because of the varactors' signal dependent capacitance. For the tuning ratios that were chosen, the two have similar quality factors so quality factor was not the deciding factor. If varactors must be used, the distortion can be reduced with stacking, and higher quality factor varactors can be fabricated in a silicon-on-glass process [2].

III. Power Amplifier Design

The output stage with the LC balun is preceded by a pre-amplifier in order to form the input match and to reduce the power amplifier's drive requirement. Since CMOS transistors in a 0.35 μm BiCMOS process are too slow to create a good CMOS inverter above 3.4 GHz, a simple inverter chain as the pre-amplifier was ruled out. Even if the transistors were fast enough, the $f_0 C_{gate} V_{DD}^2$ power would be significant above 3.4 GHz and the gate

capacitance of the output stage clearly needs to be resonated with an inductor. A variable capacitor C_1 was added in parallel with this gate capacitance to enable frequency-reconfigurability (see Fig. 6). This frequency-reconfigurable LC tank is driven by a pre-amplifier with an input match that simply consists of a 50 Ω resistor to a differential ground, in parallel with the input transistor (see Fig. 6). This input match works well from DC until slightly beyond the frequencies of interest as long as the input capacitance of the transistor is small enough. To get the most transconductance out of the input transistor for a given input capacitance, a BJT was used instead of a MOS device because of the BJT's higher cutoff frequency. Such a simple input match is appropriate for an already complex power amplifier with many tunable elements.

To save area, several things were done. First, L_1 and L_2 are both differential inductors rather than two single ended inductors (see Fig. 6). Second, C_1 and C_2 are both arrays of 15 identically sized switched capacitors that are controlled by low power 4-bit flash ADCs for testing purposes. As discussed in section II-C, switched capacitors are area-efficient and therefore they are suitable for nodes with a large fixed capacitance. C_1 is in parallel with a large gate capacitance that together resonates with L_1, and C_2 is in parallel with a large drain capacitance that is a part of the output network. Third, the shunt C_m and shunt L_m in the LC balun (see Fig. 1) were omitted in the design. An L_m of 3.5 nH including wire parasitics is large compared to 1.03 nH on one half of L_2, and the two in parallel is still relatively close to L_2; therefore the shunt L_m was omitted. A C_m of 590 fF is also small compared to the single-sided capacitance C_2 of 1.4 pF in the high capacitor setting; therefore the shunt C_m was also omitted.

The chip was tested using a probe station and due to the limited number of probe tips and the abundance of control signals, a low inductance path to ground was provided via bondwires (see Fig. 7). Although only one probe tip is used for the supply in each stage, 60 pF and 140 pF of on-chip decoupling capacitance are provided for the first and second stages respectively. An off-chip DC blocking capacitor was used during testing.

TABLE I
COMPONENT VALUES

Component	Value
Half of L_1	496 pH
Half of L_2	1.03 nH
Half of C_1	1.23 pF - 3.98 pF
Half of C_2	923 fF - 1.84 pF
L_m	2.05 nH
C_m	162 fF - 1.12 pF

IV. MEASUREMENT RESULTS

In Fig. 9 and Table II, the drain efficiency (DE) only includes the power consumption of the output stage while the global efficiency (GE) includes the whole amplifier. Looking at Table II, the power amplifier's performance is comparable to [5] which is another power amplifier with an integrated LC balun. The lower drain efficiency compared to [5] is the result of a higher operating frequency with slower transistors and the fact that the LC balun is missing the shunt L_m and C_m to save area. These high frequencies were chosen for the appropriateness of inductor and CMOS-MEMS variable capacitor values. While a more advanced CMOS process may have been more appropriate for these frequencies, the CMOS-MEMS variable capacitor exists at the 0.35 μm process node. The distortion components (HD_2 and HD_3) are slightly high also because the LC balun is missing the shunt L_m and C_m. Although this work uses a higher supply voltage than [5], the output powers are similar because of the higher loss in

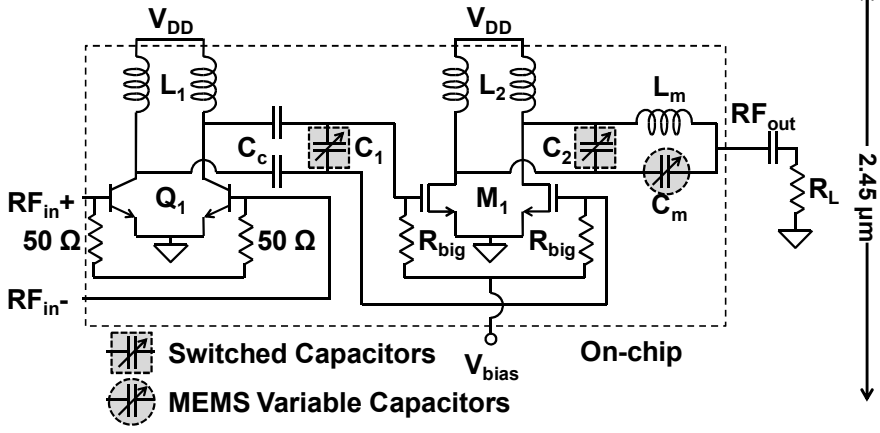

Fig. 6. Complete power amplifier schematic.

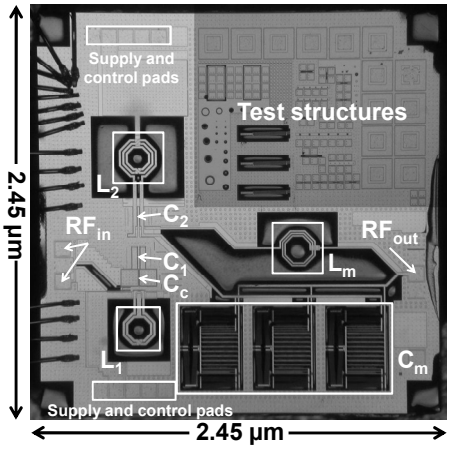

Fig. 7. Power amplifier die photo.

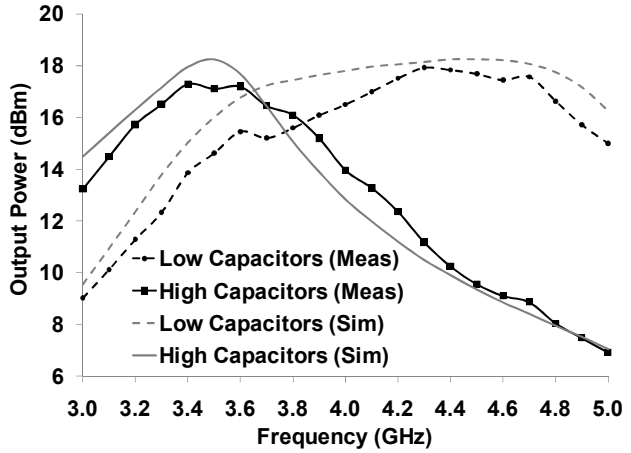

Fig. 8. Output power versus frequency. Input power = 4 dBm.

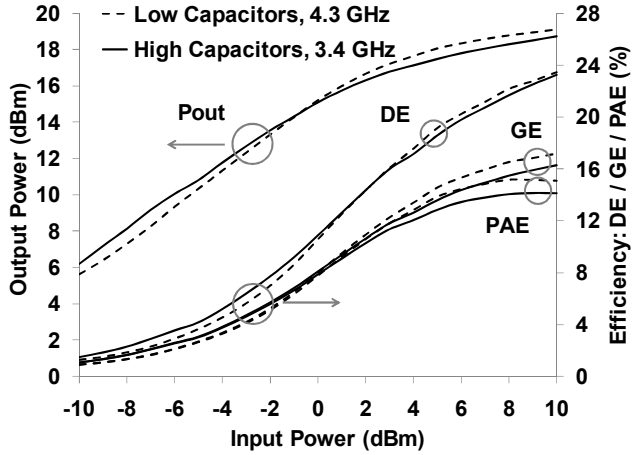

Fig. 9. Measured output power/efficiency versus input power.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work		[5]
Process	0.35 µm BiCMOS		0.13 µm CMOS
V_{DD}	3.3 V		1.5 V
Setting	High Caps	Low Caps	1 section–2 PAs
Frequency	3.4 GHz	4.3 GHz	2.45 GHz
Max P_{out}	18.7 dBm	19.1 dBm	18 dBm
Max DE	23.6%	23.5%	32%
Max GE	16.3%	17.2%	21%
Max PAE	14.1%	15.1%	21%
HD_2*	-16.6 dBc	-19.9 dBc	-
HD_3*	-25.3 dBc	-29.6 dBc	-

*At P_{in} = 10 dBm

the passive components at higher frequencies and because [5] uses a higher transformation ratio in the LC balun; this work opted for a lower transformation ratio in order to obtain a lower C_m that is appropriate for the CMOS-MEMS variable capacitor. Although the tuning range of this amplifier is from 3.4 GHz to 4.3 GHz determined by the output power peaks in Fig. 8, the output power at 4.7 GHz is higher than the peak at 3.4 GHz.

V. CONCLUSION

To the authors' best knowledge, this power amplifier is the first frequency-reconfigurable power amplifier with a power combiner that is monolithically integrated; [1]-[2] are frequency-reconfigurable but not monolithic and [3]-[4] are monolithic and use power combining but are not frequency-reconfigurable. Although the CMOS-MEMS variable capacitor simultaneously has a high quality factor and a wide 6.9:1 tuning ratio, the tuning range of the power amplifier is limited by the weakest link: the area-efficient switched capacitors. Future linearization can be achieved by adding parallel LC balun sections and turning each section on or off as appropriate as discussed in [5].

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