A Feedback Technique to Compensate for AM-PM Distortion in Linear CMOS Class-F Power Amplifier

Joon Hyung Kim, *Senior Member, IEEE*, and Chul Soon Park, *Senior Member, IEEE*

***Abstract*—An amplitude-phase (AM-PM) linearization technique using a direct drain-gate feedback method in a cascode CMOS amplifier is proposed. This technique consists of a series-connected capacitor and an inductor coupling the residue of the RF signal drain. The coupled RF ac signal to gate node of the common gate stage (CG) prevents the CG stage from entering the triode region at a high output power region. In this respect, the parasitic gate-drain capacitance sustains a constant value, achieving an enhancement in linearity. To verify the superior performance of the proposed technique, a CMOS PA was fabricated using a commercial 0.18 μm process. The experimental results show that the implemented PA delivers a PAE of 34.2% at an output power of 26.7 dBm for a 10 MHz 3G LTE signal at Band 5/8 (824–915 MHz), and has an improved spectral performance of over 5 dBc.**

***Index Terms*—Cascode amplifier, CMOS, linearization, power amplifier (PA).**

I. Introduction

IMPLEMENTING a watt-level power amplifier (PA) using CMOS for a wider-band communication system is a challenging task owing to the lower breakdown voltage and poor linearity. While a stacked cascode structure has contributed to resolving the low breakdown voltage issue [1], [2], the linearity problem still remains a more critical factor in a high data rate system with a high peak-to-average power ratio (PAPR), such as in third-generation long-term evolution (3G-LTE). In a mobile PA, the nonlinearity mainly originates in the amplitude-amplitude (AM-AM) and amplitude-phase (AM-PM) distortion. Although AM-AM distortion is relatively well treated through inter-stage matching and an inverse biasing technique for the driver and power stage, an additional linearized function is required to deal with AM-PM distortion. In particular, control of the gate-drain parasitic capacitance of the common-gate (CG) stage in a cascode amplifier has been highlighted to compensate for AM-PM distortion [3], [4].

A feedback bias technique for the cascade stage [3], and an AM-PM linearizer implemented in a matching network [4], have both been introduced. However, the former technique scarifies the gain and efficiency, whereas the later solution requires an additional active canceller with a specific bias. In this paper, a partial coupling method using a feedback network through a gate-drain of the CG stage is introduced to avoid entering the triode region. In this way, the variation in gate-drain parasitic capacitance with respect to the output power is reduced, guaranteeing a linear operation.

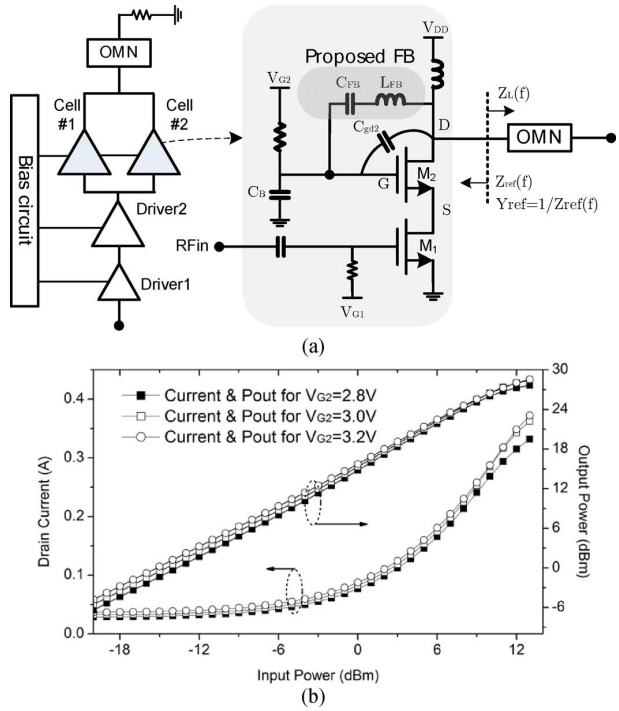

Fig. 1. Simplified Class-F cascode amplifier (a), and output power and drain current as a function of input power for different v_{G2} (b).

II. Gate-Drain Feedback Technique (FB) for Class-F Load

Fig. 1(a) shows two cascode cells terminated as a Class-F harmonic termination [5]. In a conventional case, each cell consists of a CS as a transconductance stage and CG with a fixed bias gate voltage. To combine both cells, the current combining method with high pass filter has been used. For an optimized amplification of Class-F, in which the voltage and current waveform at a drain node form a square and one-half sinusoidal, $Z_L(2f)$ and $Z_L(3f)$ are short and open conditions, respectively, whereas $Z_L(f)$ is tuned as an optimum resistance.

In tandem with the harmonic loading condition, the gate voltage of M_2 is critical design parameter directly affecting an output power and current driving capability as shown Fig. 1(a).

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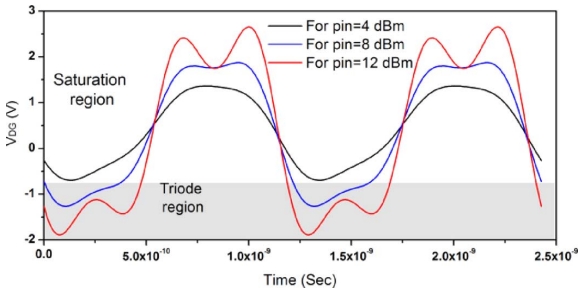

Fig. 2. Drain-gate voltage waveform of M_2 for different input powers.

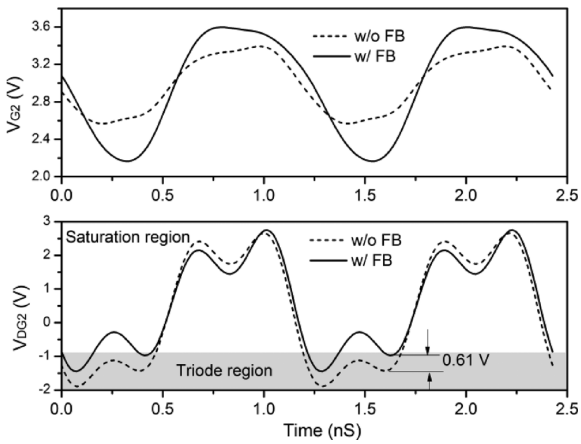

Fig. 3. Simulated drain-gate and gate voltage of CG stage with and without the proposed technique.

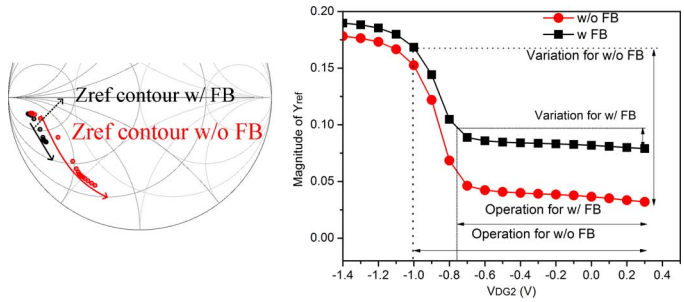

Fig. 4. Simulated admittance seen at the drain of M_2 as a function of drain-gate voltage ($F = 824$ MHz).

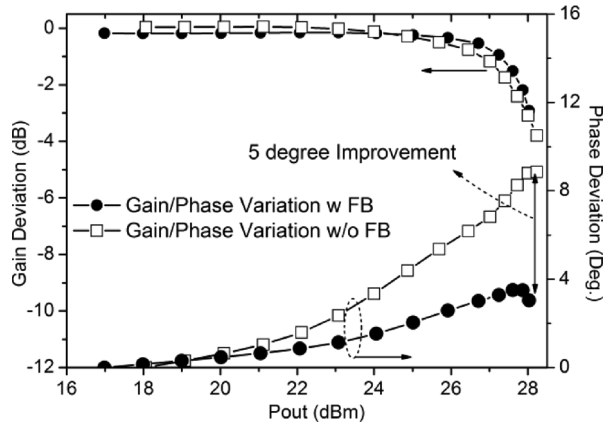

Fig. 5. Simulated AM-AM and AM-PM response with and without the proposed technique.

To deliver sufficient output power and good efficiency simultaneously for average output power of 27 dBm of LTE signal, a gate voltage of higher than 2.8 V should be considered and 3.0 V has been used in this letter. For this condition, when the input power is small, the drain voltage is high enough that M_2 is always saturated, satisfying the condition of $v_{DG2} > V_{th2}$, where V_{th2} is the turn-on voltage of M_2. However, as the input voltage further increases, since the drain voltage of M_2 is decreased, M_2 then enters the triode region due to a fixed gate bias voltage, as shown Fig. 2. This change in operation mode causes a variation of the gate-drain capacitance of M_2, resulting in severe AM-PM distortion. To resolve this problem, an effective method for exploiting the synchronized residue of the drain voltage signal is proposed to establish a partial coupling path in the gate node of the CG stage, as shown Fig. 1(a). The proposed gate-drain FB network consisting of an inductor L_{FB} and capacitor C_{FB} allows a partial output signal to be inserted into the gate node of M_2. The compensated gate voltage is correspondingly decreased as the drain voltage is decreased. Thus, M_2 is guaranteed to operate in a saturation region even at a high power level. The optimum value for L_{FB} and C_{FB} should be chosen carefully, not only to compensate v_{G2} but also to minimize the insertion loss through the FB path. In our work, L_{FB} of 2.2 nH and C_{FB} of 5.6 pF are used. With these values, the impedance seen in the FB path is over $j \times 30\Omega$ across 824 to 915 MHz, which is sufficient when considering a $Z_L(f)$ of 5.4 Ω. The simulated insertion loss is around 0.21 dB causing a PAE degradation of 2.18%. Fig. 3 shows the compensated v_{DG2} and v_{G2} compared with a conventional case. By adopting the FB technique, the increase of v_{DG2} minimizes the triode operation of M_2 at a high power level, and keeps C_{gd2} as a constant value. This effect can be verified by the admittance contour seen toward the drain node described as $Y_{ref}(f)$ in Fig. 1(a). As shown in Fig. 4, the variation of $Y_{ref}(f)$ related with C_{gd2} is reduced by more than half compared with that of a conventional case, inferring that AM-PM distortion is compensated. Fig. 5 shows the AM-AM and AM-PM responses as a function of the output power. While a slight degradation in signal gain is observed, as previously expected, owing to the proposed negative effect, 5° of the AM-PM is compensated, inferring an improvement in the linearity with respect to a non-constant envelope signal.

III. Implementation and Measurement

A prototype three-stage CMOS cascode PA was fabricated using a commercial 0.18 μm process. Fig. 6 shows a detailed schematic and photograph of the proposed CMOS PA. For proper harmonic termination of Class-F, the second harmonic impedance is shorted by an MIM cap in the die and wire bonding, while the third harmonic impedance is adjusted to have high impedance using the internal parasitic capacitance. To minimize the source degeneration through the ground, an eight-wire bond is used for a ground connection. For feasibility and easy optimization, an FB LC series network is used as an SMD, and implemented values of 2.2 nH and 5.6 pF were chosen. The die size is 1.36 m × 1.1 m including all current mirror bias circuitry, the inter-stage matching inductor, and the bonding pads, as shown in Fig. 6. Fig. 7 shows the measured output power, gain, and PAE for a supply voltage of 3.3 V and a gate voltage of 3.0 V. In this condition, the quiescent current of 2-drivers and final stage is 16 mA and 54 mA respectively. The CMOS PA delivers a power gain of 31.2 dB and a PAE of 53.4% at a saturated output power of 31.3 dBm. Compared with the results without compensation, 0.3 dB, 0.2 dB, and 2.8% degradations in the gain, output

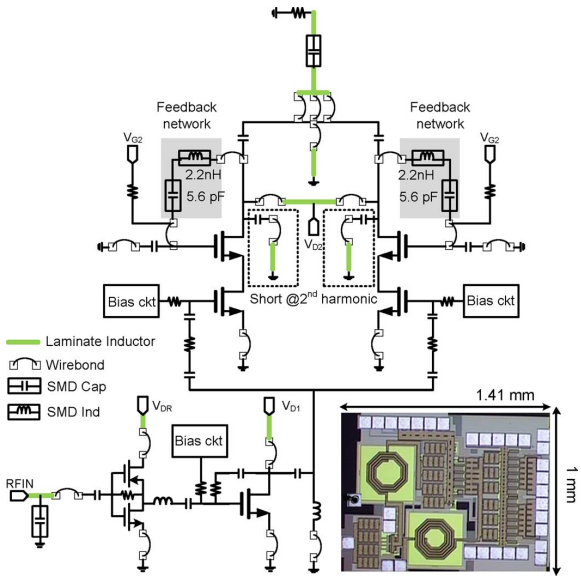

Fig. 6. Schematic and photograph of the proposed CMOS PA.

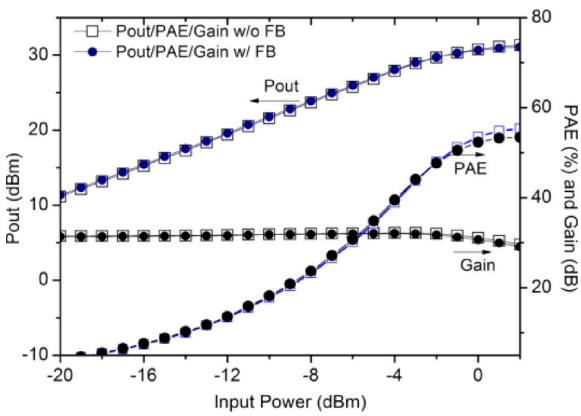

Fig. 7. Measured output power, gain, and PAE of CMOS PA with and without FB.

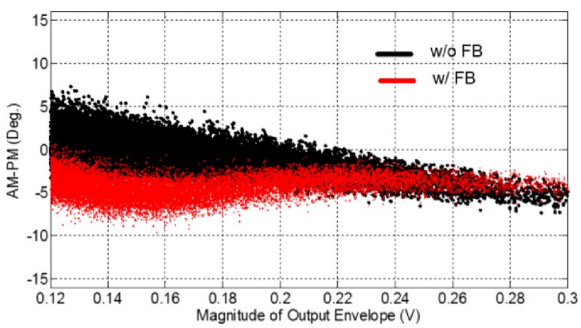

Fig. 8. Measured phase deviation at an average output power of 26.7 dBm.

power, and PAE are observed, respectively. Fig. 8 compares the results of the phase response with and without the FB for a 3G LTE, 10 MHz, 50 resource-block (RB) signal at an average output power of 26.7 dBm. The phase deviation with the FB is observed to be within 4.3°, which is approximately a 5.2° smaller value compared with that of no FB. A comparison between the adjacent/alternative channel leakage power ratio (ACLR1/ACLR2) and the error vector magnitude (EVM) is shown in Fig. 9. The proposed PA delivers an ACLR1/ACLR2 of $-35.2/-48.2$ dBc and an EVM of 2.9% at an average output power of 26.7 dBm, which is $-4.7/-2.8$ dBc, and 1.7% lower than in a conventional PA over the frequency range

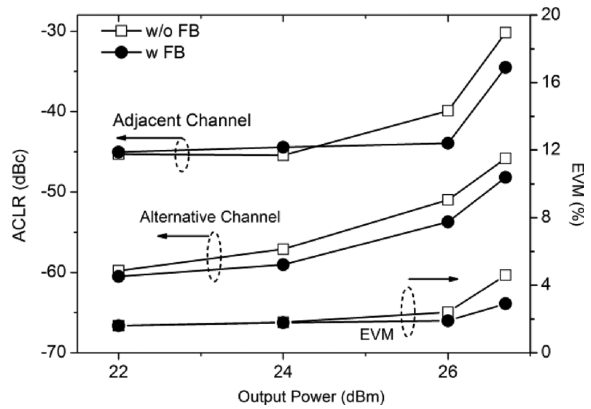

Fig. 9. Measured ACLR1/2 and EVM as a function of output power.

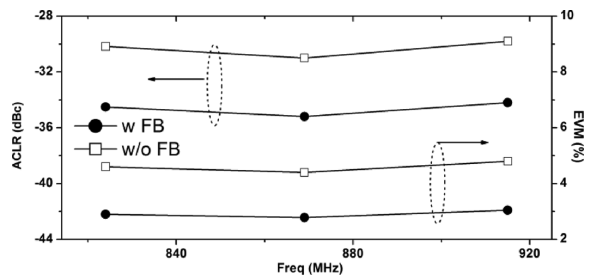

Fig. 10. Measured ACLR and EVM as a function of frequency (F $=$ 824/849/915 MHz, Pout $=$ 26.7 dBm).

TABLE I
PERFORMANCE COMPARISONS

Ref.	f.(GHz) Applic.	Pavg (dBm)	PAE @Pavg(%)	EVM (%)	ACLR (dBc)
[3]	1.95 WCDMA	23.5	40	-	-33.2
[4]	1.95 WCDMA	28	-	2.8	-35.9
[6]	1.88 WCDMA	27.1	28	-	-40
This Work	0.824 3G LTE	27 (w/o) 26.7 (w/)	34.8 (w/o) 34.2 (w/)	4.6 % (w/o) 2.9 % (w/)	-30.3 (w/o) -35 (w/)

shown in Fig. 10. Under such a condition, PA delivers a PAE of 34.2%. A performance comparison of the proposed CMOS amplifier and previous works is summarized in Table I.

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