Design of High Efficiency Monolithic Power Amplifier With Envelope-Tracking and Transistor Resizing for Broadband Wireless Applications

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***Abstract*—This paper presents the design insights for the implementation of a fully monolithic radio frequency (RF) power amplifier (PA) using both envelope-tracking (ET) and transistor resizing techniques for long-term evolution (LTE) applications. At the low output power region, some of the power cells in the PA can be disabled to further save power consumption, thus enhancing the efficiency from a traditional ET-PA. Our ET-PA system is first realized with a two-chip solution, consisting of a high voltage envelope modulator fabricated in a 0.35 μm Bipolar-CMOS-DMOS (BCD) technology, and a differential cascode PA in a 0.35 μm SiGe BiCMOS technology. This two-chip solution of the ET-PA is to showcase the effective efficiency enhancement of using the transistor resizing method. In the second design, a CMOS envelope modulator is integrated with the cascode PA on the same die in the 0.35 μm SiGe BiCMOS technology. Some insights are demonstrated regarding the optimization of the envelope modulator specific to our cascode PA for LTE broadband signals, where the finite bandwidth and the switching frequency of the envelope modulator are considered for achieving the minimal error-vector magnitude (EVM) and spurious noise. The fully monolithic BiCMOS ET-PA reaches the maximum linear output power ($\mathrm{P_{out}}$) of 24 dBm and 23.4 dBm with overall power-added-efficiency (PAE) of 41% and 38% for the LTE 16QAM 5 MHz and 10 MHz signals at 1.9 GHz, respectively, without needing predistortion. At the low power mode of our ET-PA, an additional PAE enhancement of 4% is obtained at $\mathrm{P_{out}}$ of 16–20 dBm by disabling some of the PA power cells. Our fully monolithic ET-PA satisfies the LTE 16QAM linearity specs with high efficiency.**

***Index Terms*—Bipolar-CMOS-DMOS (BCD), cascode power amplifier (PA), envelope modulator, envelope-tracking (ET), long-term evolution (LTE), low power mode, SiGe BiCMOS, transistor resizing.**

I. Introduction

BROADBAND 3G/4G/WLAN wireless standards utilize highly spectral-efficient modulation schemes with inherent non-constant-envelope signals having high peak-to-average power ratios (PARs) and wide bandwidths. Even though saturated PAs can work efficiently with constant envelope signals for the case of the Global System for Mobile Communications (GSM) standard, the non-constant envelope signals with high PARs require the PAs to be backed off from their saturation power ($\mathrm{P_{sat}}$) to satisfy the stringent linearity specs. This is a major bottleneck for realizing highly efficient mobile 3G/4G transmitters (TXs). Moreover, the average power efficiency of the PA is dominated by the efficiency at its most probable output power ($\mathrm{P_{out}}$) levels, which can be lower than its maximum $\mathrm{P_{out}}$ by an order of magnitude. For example, in some power control schemes for the Long Term Evolution (LTE) standard, $\mathrm{P_{out}}$ of $\leq$15 dBm presents a probability over 70% [1], [2]. Therefore, a highly linear PA achieving high efficiency over a wide dynamic range (i.e., at the maximum $\mathrm{P_{out}}$ and the more probable low $\mathrm{P_{out}}$ levels) would be desired for 3G/4G handset applications.

The dynamic power-supply modulation schemes (e.g., the envelope-elimination-and-restoration (EER) and the envelope-tracking (ET) techniques) are among the most effective approaches for the PA efficiency enhancement. Recent literature has demonstrated excellent overall efficiency using either EER [3]–[5] or ET [6]–[15]. In addition, several envelope shaping methods are proposed to improve the efficiency and linearity for ET-PAs, such as the sweet spot tracking reported in [8]. However, there are several practical challenges for designing the EER/ET systems, such as the bandwidth limitation of the envelope modulator, and the precise timing alignment between the envelope and the RF paths. In [3], [5], a low dropout (LDO) is used in EER-PAs for good spurious emission, but at the cost of low efficiency. A switching modulator can be combined with the linear stage (i.e., a linear-assisted switching modulator) to improve the overall efficiency [4], [30], but the linear stage must have large bandwidth to suppress the switching ripples. For example, in [4] a linear-assisted switching modulator with a large bandwidth of 285 MHz was proposed to work satisfactorily in an EER-PA for a 20 MHz signal. The bandwidth requirement is relatively relaxed for the ET-PA system [7], [12], [15], but it is still crucial to perform careful system analysis and optimization for the best overall efficiency and linearity, such as a judicial selection of the average switching frequency, applying necessary envelope shaping, and delivering the current handling capability to drive a small PA load for high $\mathrm{P_{out}}$. As different from previous publications in [4], [11], [15], this work emphasizes the impacts on the linearity of our cascode SiGe PA, when selecting the average switching frequency and the optimal envelope shaping.

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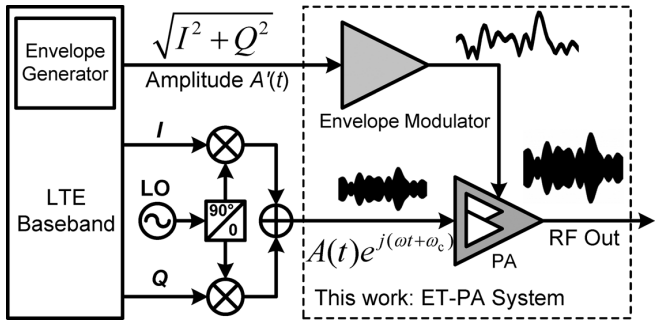

Fig. 1. Simplified block diagram of the ET-PA system reported in this work.

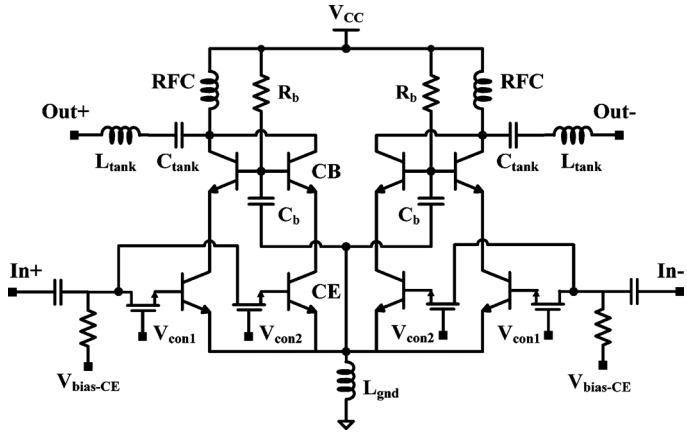

Fig. 2. Schematic of the cascode differential SiGe PA using the proposed transistor resizing technique.

As reported in the literature, a highly-efficient and linear envelope modulator design is a key to achieve the best performances for an overall EER/ET PA system. A comprehensive system-efficiency analysis is given in [16], which compares different supply tracking schemes for mobile TXs. Due to the inevitable power consumption of the envelope modulator, there is a crossover point at back-off where the efficiency enhancement of using the EER/ET techniques at the low power region becomes limited [16]. Therefore, further improvements of the PA efficiency at the low average power levels are desired to extend the battery lifetime of mobile devices. Besides using the dynamic power-supply tracking/modulation techniques, several methods have been reported to reduce the PA current consumption at the low power mode, such as device size switching [17]–[20], [23], parallel amplification [21]–[23], switchable power combiner [24], Doherty PA [9], etc. In the recent literature, combinations of different techniques have also been reported. For example, in [9] the ET technique was combined with a Doherty GaAs PA, achieving an efficiency enhancement over the extended output dynamic range. In [23] a discrete device resizing technique is proposed in combination with a parallel-combining transformer for efficiency improvement at the low power mode.

Using different sizes of power cells for the low power and high power modes of the PA is a simple solution with low cost for the enhancement of low-power efficiency [17]–[20]. In this work, we will adopt the combination of the ET and transistor resizing techniques to a cascode SiGe PA [27], [31], as shown in Fig. 1. Section II presents the cascode SiGe PA using the transistor resizing. A high voltage envelope modulator designed in a Bipolar-CMOS-DMOS (BCD) technology will be reported in Section III. The overall performance of the ET-PA provided by the two-chip solution (i.e., a BCD envelope modulator and a SiGe BiCMOS PA) will also be demonstrated in Section III. In Section IV, a fully monolithic ET-PA designed and fabricated in a 0.35 μm SiGe BiCMOS technology will be presented. This technology provides CMOS devices for the design of the envelope modulator and switches, and also the bipolar devices for the robust PA design. The integrated envelope modulator is carefully optimized specific to our cascode SiGe PA for the LTE broadband signals. The LTE 16QAM signal having a PAR of $\sim$7.5 dB and bandwidth of 5 MHz and 10 MHz will be used to evaluate our monolithic ET-PA systems.

II. SiGe Power Amplifier Design

A. Cascode PA With Transistor Resizing Technique

In our differential cascode PA design, a high-$f_{\rm T}$ low-$\rm BV_{CEO}$ bipolar device ($\rm BV_{CEO} = 3.8$ V) is utilized as the common-emitter (CE) stage and a high-$\rm BV_{CEO}$ low-$f_{\rm T}$ bipolar device ($\rm BV_{CEO} = 6$ V) is used as the common-base (CB) stage. The size of the CB transistor needs to be carefully considered. For example, making the CB transistor larger can reduce the power loss due to its smaller collector-to-emitter resistance (i.e., "$r_{\rm on}$") [27]. However, this inevitably introduces larger shunt capacitance on the collector, leading to the efficiency drop due to non-optimized switching [27]. In this design, the emitter area of CE transistor is first set as 290 μm^2, while the optimal ratio of emitter area of the CB/CE transistors was found to be around 2:1 via SPICE simulations.

Fig. 2 shows the schematic of our proposed differential cascode PA using the transistor resizing technique. Due to the linearity concerns and the designed capability to perform dynamic power supply modulation, the CB transistor is self-biased [6]. The base of the CB transistor is connected to $\rm V_{CC}$ through $\rm R_b$-$\rm C_b$ and the DC voltage applied to the base is close to $\rm V_{CC}$ [37], [38]. At the low power mode, half of the power cells will be switched off, which is implemented by adding two pairs of MOSFET switches at the base of the CE transistors (see Fig. 2). These MOSFET switches are biased at the triode region. Only two modes of operation are chosen, because adding more resizing steps will inevitably increase the additional loss due to the inactive power cells and make the output matching design more challenging. The trade-off between the power isolation and power loss was considered for the optimal size of each MOSFET switch. In this case, the MOSFET size of 240 μm $\times$ 0.35 μm was chosen. The simulated insertion loss is 0.7 dB. The output L-C resonator needs to be carefully designed to enhance the power-added efficiency (PAE) of the PA at the low power mode, while only costing very little PAE degradation at the peak $\rm P_{out}$. The PA has been tested under an elevated $\rm V_{CC}$ of up to 5 V. No reliability or stability issue has been found for both the high power mode and the low power mode.

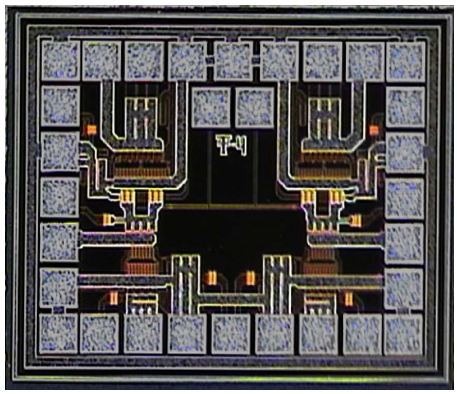

Fig. 3. Die picture of the cascode PA, fabricated in the TSMC 0.35 μm SiGe BiCMOS technology.

The PA shown in Fig. 2 was fabricated in the TSMC 0.35 μm SiGe BiCMOS process. Its die picture is shown in Fig. 3. The die area is 1.2×1.1 mm^2 including the bondpads, and 0.85×0.6 mm^2 excluding the bondpads. Bondwires were used for the RF chokes (RFC) and the output tank inductors, thus reducing the amount of external components needed. This PA requires two off-chip baluns to convert the differential signal into a single-ended signal and vice versa. The balun losses were de-embedded from the measurement results. No extra off-chip input/output matching networks are used in this design.

Fig. 4 shows the measured PAE against P_{out} of the cascode SiGe PA at the high power mode (A) and the low power mode (B) at different V_{CC} for continuous wave (CW). The PAE trajectory on the PAE clusters (i.e., the red curve in the color version) represents the real-time operation of the ET-PA. As shown in Fig. 4, the ET-PA provides high average efficiency values over a wide range of P_{out}. The PAE trajectory in Fig. 4 is obtained by holding the PA at its 1-dB compression ($P_{1\,dB}$) for $V_{CC} \geq 1.2$ V. Driving the PA into deeper compression can get higher efficiency and average P_{out}, but results in degraded linearity performance. It is worthwhile to note that the PAE is improved by 3–6% at the low power mode using the transistor sizing technique, as shown in Fig. 4(b). In addition, an important parameter given by Fig. 4 is the R_{load} seen by the envelope modulator. The R_{load} vs. P_{out} curve is also obtained at each $P_{1\,dB}$ point of a different V_{CC}. At V_{CC} of 1.8 V and above, the R_{load} stays relatively constant for both the high and low power modes, and becomes larger at V_{CC} of 1.2 $\sim$1.4 V. The trend of R_{load} vs. P_{out} is dependent on the distinct characteristics of PAs and also different envelope shaping methods. In our cascode SiGe PA design, the collector-emitter resistance of the CB transistor increases at a V_{CC} of 1.4 V and below, resulting in larger R_{load} seen by the envelope modulator [6], [37]. Since the R_{load} affects the efficiency of the envelope modulator, one needs to pay special attentions to the value of R_{load} when optimizing the envelope modulator for a specific PA.

B. Envelope Shifting for the Cascode ET-PA

Before applying the ET technique to the proposed cascode PA, the overall system needs to be carefully investigated for good linearity and efficiency. As opposed to EER, it is feasible

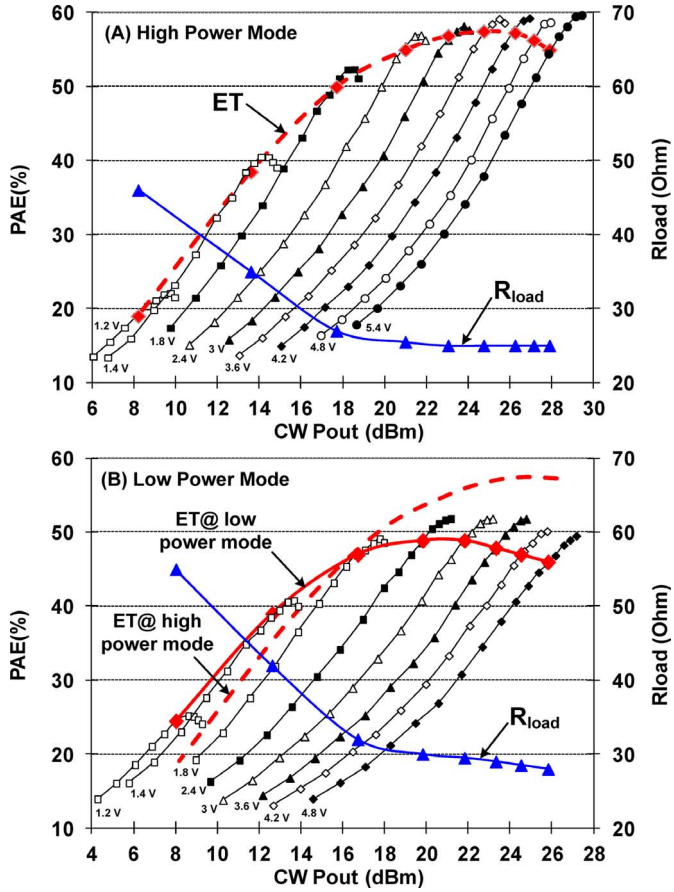

Fig. 4. The PAE vs. P_{out} curves of the proposed self-biased cascode SiGe PA (measured at different V_{CC} in the CW mode) and the R_{load} seen by the envelope modulator: (A) the high power mode; (B) the low power mode.

to shape the envelope signal in the ET system, so that the linearity and efficiency can be enhanced simultaneously. There have been various envelope shaping methods reported in the literature, focusing on different aspects such as bandwidth relaxation [25], sweet spot tracking for intermodulation distortion (IMD) [8], and linearity enhancement for the cascode PAs [6]. The envelope shifting proposed by [6] will also be applied to the self-biased cascode PA designed in this work. As briefly mentioned, the envelope signal fed into the envelope modulator is first shifted to a predetermined minimal level, while the AC magnitude of the envelope is reduced to avoid possible clipping. Currently, the envelope shifting is implemented with the Agilent vector signal generator (E4438C). The minimum envelope level is manually adjusted for the minimum EVM of the PAs. The envelope shifting method not only improves the output power and linearity of the proposed cascode PA, but also has effects to the efficiency of the envelope modulator, as will be demonstrated in Section IV.

III. High Voltage Envelope Modulator Design

We will then turn to implementing the envelope modulator monolithically. The envelope modulator must be designed for high efficiency, wide bandwidth, and with the capability of driving a varying PA load. Compared with the discrete solutions in [7], [11], the monolithic implementation of the

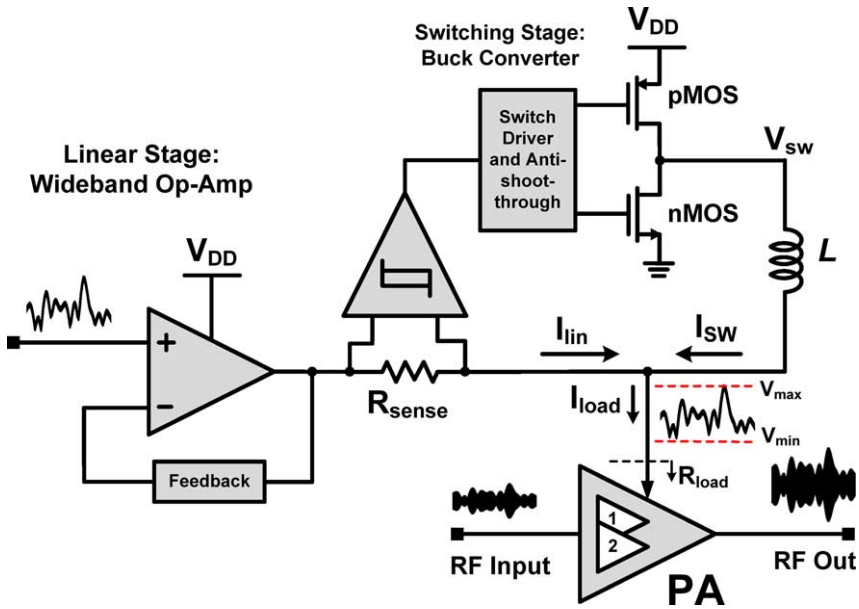

Fig. 5. Simplified block diagram of the envelope modulator connected to the cascode SiGe PA using the transistor resizing technique.

envelope modulator has several benefits: 1) it can reduce cost; 2) it can have an integrated signal path providing better signal integrity, and 3) the transistors can be optimized more freely according to different power levels for better performances [15]. In this section, a monolithic envelope modulator will be reported, designed in a 0.35 μm proprietary 40 V BCD technology developed by Texas Instruments (TI).

A. Design of the BCD Envelope Modulator

Fig. 5 shows the simplified block diagram of the BCD envelope modulator connected to the cascode SiGe PA using transistor resizing technique as presented in Section II. The monolithic envelope modulator utilizes a hybrid configuration consisting of a linear stage (i.e., Op-Amp) and a switching stage (i.e., buck converter) [12]. The high efficiency switching stage mainly supplies the low-frequency contents of the envelope signal, while the linear stage tracks the rest of the high frequency contents. The output current of the linear stage is sensed and compared with the threshold level of a hysteresis comparator to control the switching stage. The efficiency of the entire envelope modulator ($\eta_{\mathrm{env.-mod.}}$) is a combination of the switching stage efficiency (η_{SW}) and the linear stage efficiency (η_{lin}), as expressed by

$$\frac{1}{\eta_{\mathrm{env.-mod.}}} = \frac{\alpha}{\eta_{\mathrm{SW}}} + \frac{1-\alpha}{\eta_{\mathrm{lin}}} \tag{1}$$

where α is the ratio of the DC content to the total envelope power [6]. Since more than 85% of the envelope signal power resides between DC to several kHz, this configuration is suitable for high efficiency broadband envelope tracking [4], [10], [12].

The simplified circuit schematic of the linear stage is shown in Fig. 6. This design is based on a constant-g_m input stage with a wide-swing folded cascode configuration [32]. The biasing circuitry of this configuration is designed to avoid large open-loop gain variation by ensuring M9-M16 not entering into the triode region. The input stage is followed by a class-AB output stage with optimized biasing. The output stage utilizes 7 V high breakdown MOS devices available from the 0.35 μm BCD technology used. These 7 V devices were chosen over higher breakdown devices, since they give better headroom performance while allowing the necessary frequency response for high-PAR broadband signals. The linear stage in this design achieves the maximum output voltage above 6.5 V at the supply voltage ($\mathrm{V_{DD}}$) of 7 V for $\mathrm{R_{load}}$ beyond 10 Ω. The hysteresis comparator has the similar circuitry schematic as reported by [6] but with a basic current sink. To provide most of the current to the load through the buck converter, its off-chip inductor is chosen as 6.8 μH. This design presents an opportunity to assemble an integrated watt-level ET-PA system where the PA with small collector/drain impedance ($\mathrm{R_{load}}$) presents a big challenge for the modulator to drive effectively.

B. Evaluation of the BCD Envelope Modulator With SiGe PA

The die of the envelope modulator fabricated in the 0.35 μm BCD technology is shown in Fig. 7. The total chip size is 1.5×1.5 mm^2. To test the performance of the envelope modulator by itself, we first used a resistive load to mimic the real PA. The $\mathrm{R_{load}}$ represents the behavior of a PA at various $\mathrm{P_{out}}$ levels. For example, when an average modulated envelope of 5.5 V is fed into the PA's collector, the $\mathrm{R_{load}}$ is $\sim$10 Ω presented by a PA of 60% efficiency and 33 dBm $\mathrm{P_{out}}$. Fig. 8 shows the efficiency of the envelope modulator for the LTE 5 MHz 16QAM signal by sweeping $\mathrm{V_{DD}}$ up to 7 V at different $\mathrm{R_{load}}$. When the $\mathrm{V_{DD}}$ is increased from 3.5 V to 7 V, the envelope waveform is kept with the same clipping ratio (CR) during testing. The clipping ratio in this work is defined as

$$CR = 20 \cdot \log\left(\frac{E_{\mathrm{peak}}}{E_{\mathrm{clip}}}\right) \tag{2}$$

where E_{peak} denotes the peak of the ideal output envelope, and E_{clip} is the clipping level due to the rail-to-rail limitation of the

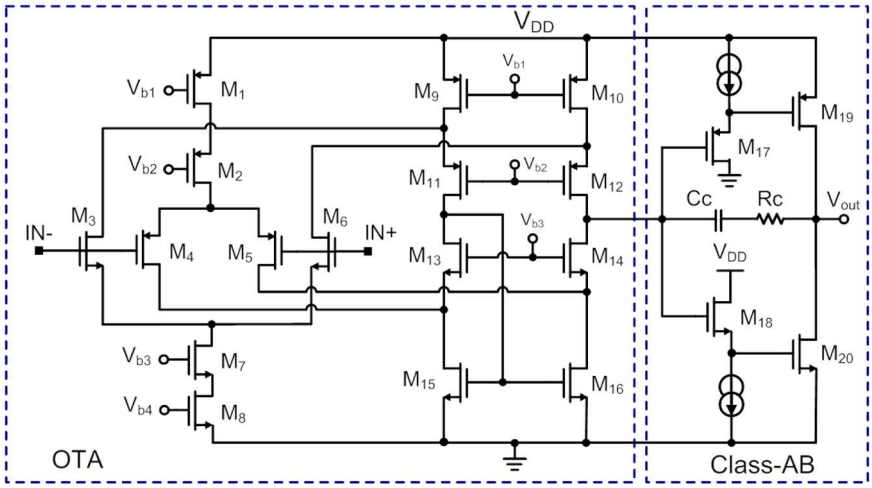

Fig. 6. Simplified circuit schematic of the linear stage used in the proposed BCD envelope modulator.

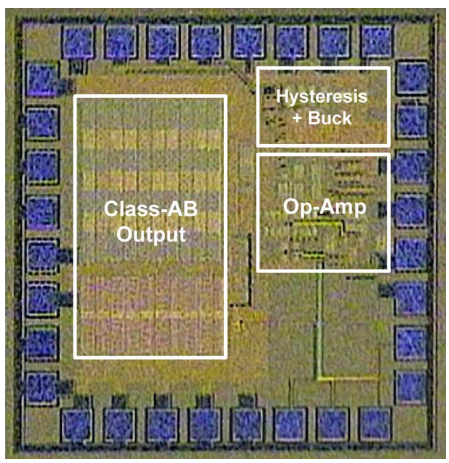

Fig. 7. Die picture of the envelope modulator fabricated in the 0.35 μm BCD technology.

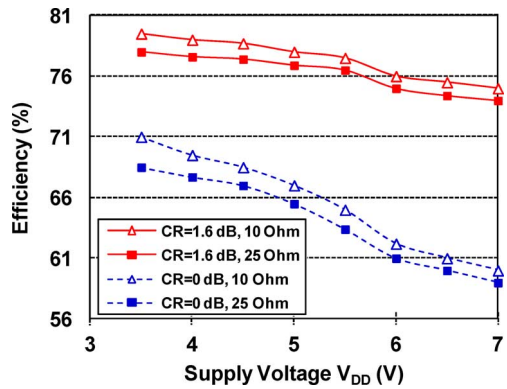

Fig. 8. Measured efficiency of the envelope modulator for the LTE 16QAM 5 MHz signal by sweeping $\mathrm{V_{DD}}$ at different $\mathrm{R_{load}}$ with and without envelope clipping.

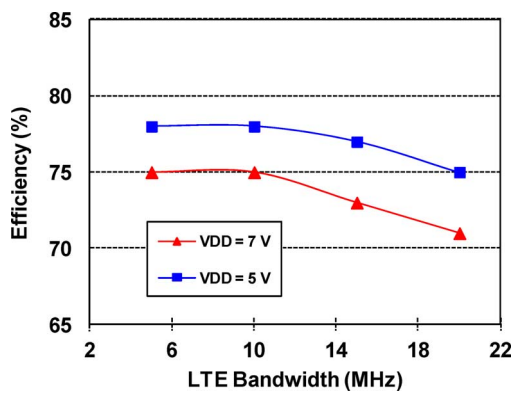

Fig. 9. Measured efficiency of the envelope modulator with various bandwidth of LTE 16QAM signals; $\mathrm{R_{load}} = 10\ \Omega$.

envelope modulator [8], [29]. As shown in Fig. 8, the efficiency of the envelope modulator is increased by clipping the envelope signal. In addition, the efficiency variation becomes less dependent on the $\mathrm{V_{DD}}$ once the envelope clipping is applied. A CR of 1.6 dB for the LTE signal is experimentally determined for best efficiency with very little linearity degradation [8], [29]. Fig. 8 also shows that the efficiency of the envelope modulator slightly reduces with larger $\mathrm{R_{load}}$, since the envelope modulator supplies less output power at larger $\mathrm{R_{load}}$. Fig. 9 shows the efficiency of the envelope modulator at $\mathrm{R_{load}}$ of 10 Ω for different bandwidths of the 16QAM LTE signals. The efficiency only drops by 3–4% when the bandwidth is increased from 10 MHz to 20 MHz. This can be mainly attributed to higher switching loss for wider bandwidth signals.

The BCD envelope modulator is then used to drive the SiGe PA described in Section II. This two-chip solution of the ET-PA is used mainly to showcase the efficiency enhancement of using the transistor resizing technique. Fig. 10 shows the measured overall PAE and EVM of the ET-PA at its high power mode ($\mathrm{N} = 2$) and low power mode ($\mathrm{N} = 1$), respectively, for the LTE 16QAM 5 MHz signal under $\mathrm{V_{DD}}$ of 4.2 V. The maximum linear $\mathrm{P_{out}}$ is 23.1 dBm with an EVM of 4.9% and PAE of 37%. At the low power mode, an efficiency enhancement is clearly observed at $\mathrm{P_{out}}$ of 13–19 dBm by using the transistor resizing technique. The low power mode also achieves good linearity (i.e., low EVM) at $\mathrm{P_{out}}$ of 19 dBm and below. Fig. 11 shows the $\mathrm{P_{1dB}}$, EVM and overall PAE of the ET-PA by sweeping $\mathrm{V_{DD}}$ up to 5.5 V. The $\mathrm{V_{DD}}$ did not exceed 5.5 V during testing due to the

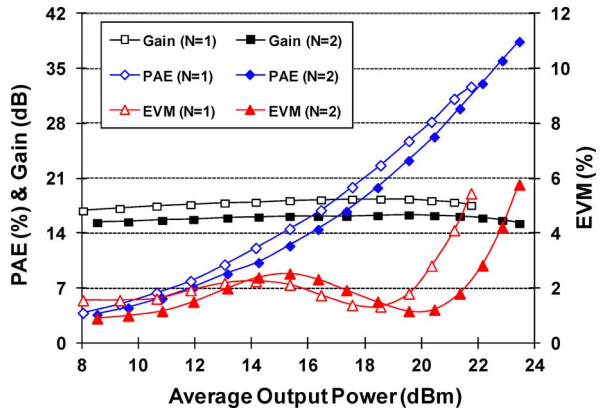

Fig. 10. Measured EVM, overall PAE and gain of the ET-PA using the BCD envelope modulator for LTE 16QAM 5 MHz at 1.9 GHz ($V_{DD} = 4.2$ V).

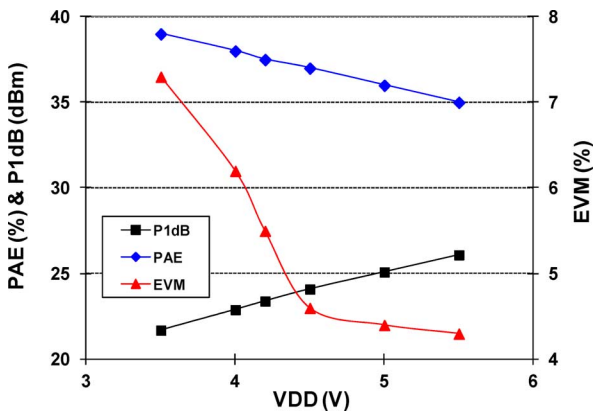

Fig. 11. Overall PAE, EVM and $P_{1\,dB}$ of the ET-PA using BCD envelope modulator and the cascode SiGe PA for LTE 5 MHz 16QAM at 1.9 GHz, measured under different levels of V_{DD}.

reliability concern of the SiGe PA. At V_{DD} of 5.5 V, the P_{1dB} of the ET-PA reaches 26.1 dBm with an overall PAE of 35% and an EVM of 4.3%. In order to obtain good linearity at P_{1dB}, the V_{DD} should be kept above 4.5 V. The class-AB stage of the BCD envelope modulator will deviate from its optimal biasing condition at lower V_{DD}, resulting in distorted output envelope. As seen from Fig. 11, the EVM at P_{1dB} degrades rapidly at V_{DD} below 4.5 V.

IV. Optimization of Envelope Modulator for Cascode SiGe PA

We have so far demonstrated a 7-V BCD envelope modulator that can provide the current handling capability required for driving a small resistive load of 10 Ω with high efficiency. It is worth noting that the performance of the BCD envelope modulator is somewhat compromised by the need of driving a PA load smaller than 15 Ω with an average output envelope higher than 5 V. Since our cascode SiGe PA does not need to deliver P_{out} of 1 W for LTE applications, it presents higher R_{load} that is easier to drive and thus, a monolithic envelope modulator designed at lower V_{DD} for this SiGe PA should achieve better overall performances in a highly-integrated one-chip solution. The better overall linearity, for example, would allow the PA to be driven into deeper compression, resulting in higher efficiency. In this section, a CMOS envelope modulator will be integrated with the SiGe PA on the same die to form a fully monolithic ET-PA system. The entire ET-PA is fabricated in TSMC 0.35 μm SiGe BiCMOS technology, and only the inductor in the buck converter is implemented off-chip with some off-chip bypass capacitors. The CMOS envelop modulator operates at V_{DD} of 4.2 V. The circuitry topology of this CMOS envelope modulator was first reported in [6]. In this work, we will demonstrate how to optimize the envelope modulator specific to our cascode SiGe PA for the LTE broadband applications. The optimization in this work considers the efficiency and linearity at the same time.

A. Linear Stage Design

The linear stage uses a folded cascode amplifier with gain-boosting to meet the slew-rate requirement of the LTE 16QAM envelope signal [6]. Its simplified schematic is shown in Fig. 12. The output stage has a common source structure biased as class-AB for a good compromise between distortion and quiescent dissipation. At R_{load} of 25 Ω, the 1-dB bandwidth and the 3-dB bandwidth of the linear stage are 12 MHz and 17 MHz, respectively.

The efficiency of the class-AB stage is the key for achieving high efficiency of the linear stage. Since all the DC current is supplied by the switching stage, the loss of the class-AB stage is minimal at the DC level of the output signal. When the output transistors (M16 and M17) begin to source or sink current, the voltage across them will cause power loss, expressed as:

$$P_{\mathrm{nMOS}} = (I_{\mathrm{sw}} - I_{\mathrm{load}}) \cdot V_{\mathrm{out}} \tag{3a}$$

$$P_{\mathrm{pMOS}} = (I_{\mathrm{load}} - I_{\mathrm{sw}}) \cdot (V_{\mathrm{DD}} - V_{\mathrm{out}}). \tag{3b}$$

For our shifted LTE envelope signal, as shown in Fig. 13, the switching current (I_{SW}) has slowly varying amplitudes with the low switching frequency, performing nearly as a constant current source. Meanwhile, the linear stage sources the AC current more often than sinking the current, since most of the time $I_{load} > I_{SW}$. This helps to remain the power loss of the nMOS device (M17) roughly same as the case without envelope shifting. In addition, the envelope-shifting pushes the output voltage (V_{out}) closer to V_{DD}, reducing the power loss of the pMOS device (M16). As indicated by SPICE simulation shown in Fig. 14, the reduction of power loss for the class-AB stage is clearly presented after applying the envelope-shifting. Another important point in Fig. 14 is that the average V_{out} is increased after envelope-shifting, improving the PA output power and efficiency.

B. Switching Stage Design

In our ET-PA system, the envelope shifting method reduces the power of high frequency contents with a lower PAR, while increasing the DC content [6]. Therefore, the efficiency of the switching stage has become more dominant to the overall system efficiency. There are at least two main sources of power loss in the switching stage: 1) conduction loss; and 2) switching loss. The switching loss is caused from the simultaneous current

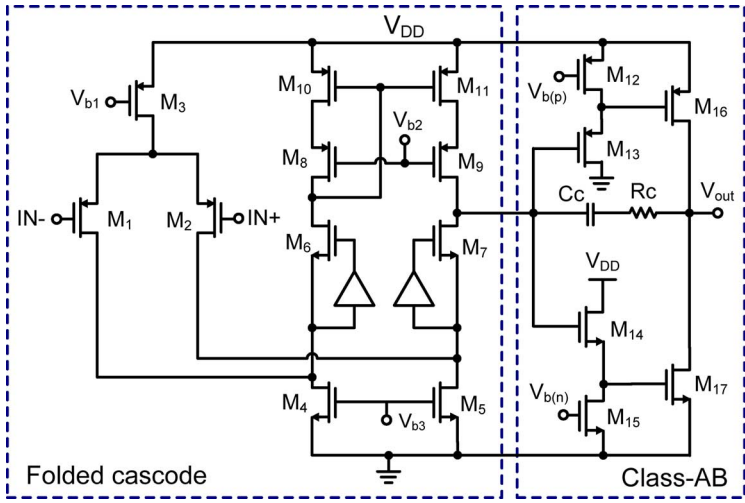

Fig. 12. Simplified schematic of the linear stage in the proposed CMOS envelope modulator.

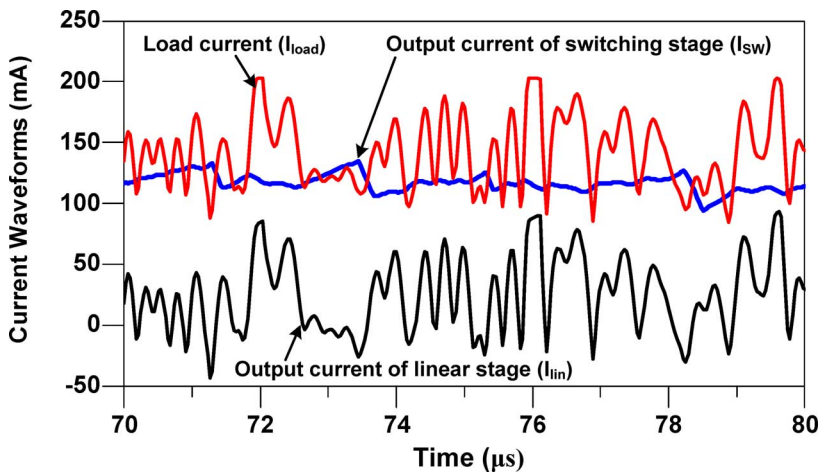

Fig. 13. Simulated current waveforms from the proposed CMOS envelope modulator for the shifted LTE 16QAM envelope.

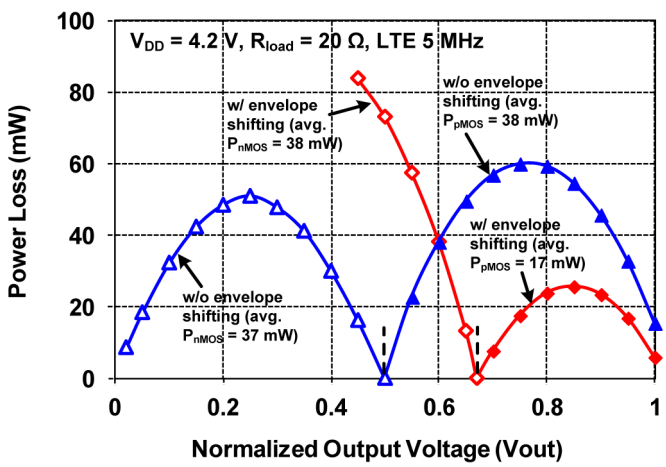

Fig. 14. Simulated power loss of the output transistor (M16 and M17) in the linear stage of the proposed CMOS envelope modulator.

and voltage overlap during the turn on/off time, as well as the loss due to the input/output capacitances during switching. The conduction loss is not dependent on the switching frequency and is inversely proportional to the device width. The MOSFET switches need to be sized for the minimal total power loss (i.e., conduction loss plus switching loss). Generally, a wider FET width results in larger gate and drain capacitances but smaller "*on*" resistance, leading to higher switching loss but lower conduction loss. An excellent analysis is reported in [15] for minimizing the power losses of the switching stage. With a rather low switching frequency, the conduction loss would be dominant [15]. In our design, the sizes of pMOS and nMOS are chosen as 20 mm $\times$ 0.4 μm and 7 mm $\times$ 0.4 μm, respectively.

Switching ripples generated by the switching stage will be mixed with the modulated carrier in PAs, causing large spurious noise at the RF output. This situation is especially critical for stand-alone switching modulator controlled by the conventional pulse-width modulation (PWM) scheme with a constant switching frequency. To mitigate the impact of the spurious noise of the stand-alone DC-DC converters, several techniques of altering the switching behaviors of DC-DC converters have been reported, such as the frequency hopping/stepping/dithering in [33]–[36]. In our linear-assisted switching modulator, however, the switching ripples can be suppressed by the

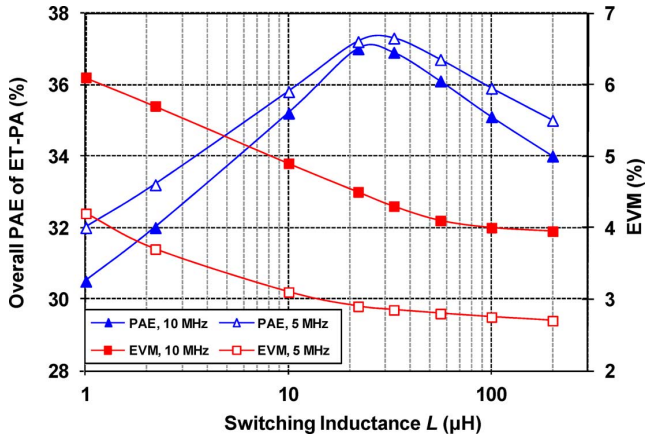

Fig. 15. Measured EVM and overall PAE of the ET-PA against different switching inductance L (in logarithmic scale) for both LTE 16QAM 5 MHz and 10 MHz signals.

linear stage. Moreover, the switching frequency of our linear-assisted switching modulator is time-varying with respect to the instantaneous envelope, and therefore the spurious noise is spread over a wider frequency range, reducing the peak magnitude of the spurs.

The choice of the inductor (L) has a major influence to the efficiency of the switching stage, since the switching frequency is inversely proportional to the inductance L [12]. In the earlier works reported in the literature [4], [11], [15], the switching frequency is optimized for the best efficiency so that the switching stage supplies not only the DC current but also some partial AC current. The drawback of such higher switching frequency is that it usually requires the linear stage to have wider bandwidth to suppress the switching ripples. Switching noise above the bandwidth of the linear stage may not only distort the envelope signal but also transfer to the PA output, potentially degrading the system linearity (e.g., EVM) and/or the spurious emission. In this work, therefore, the switching frequency is selected by considering its effects to the overall system linearity and bandwidth.

Fig. 15 plots the measured EVM and overall PAE of the entire ET-PA using different off-chip inductors for both LTE 16QAM 5 MHz and 10 MHz signals. The $\mathrm{P_{out}}$ of the ET-PA was kept at 23 dBm for all cases here. The EVM increases with smaller L and is more sensitive to L for the 10 MHz LTE signal than the 5 MHz LTE signal. On the other hand, from the efficiency point of view, the best efficiency is achieved by L of 22 μH for the LTE 10 MHz signal, but the efficiency reduction is only 0.7% as L changes from 22 μH to 56 μH. Such negligible efficiency improvement is not worthy to obtain at the cost of higher EVM. To obtain good linearity for the system, the L is chosen at the higher value side (i.e., 56 μH instead of 22 μH). The average switching frequency is 0.9 MHz according to the SPICE simulation. Such low switching frequency significantly relaxed the bandwidth requirement of the linear stage design. Please note that the switching frequency in this work is generally lower than those reported in other works such as [4], [10], [12], [15], but the efficiency of the envelope modulator is maintained at $\sim$78%, thanks to the envelope-shifting method we used.

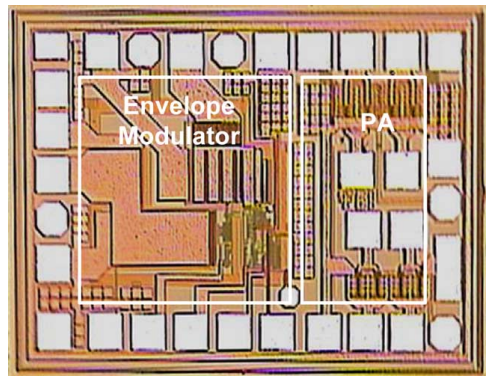

Fig. 16. Die picture of the proposed fully monolithic ET-PA with transistor resizing fabricated in the TSMC 0.35 μm SiGe BiCMOS technology.

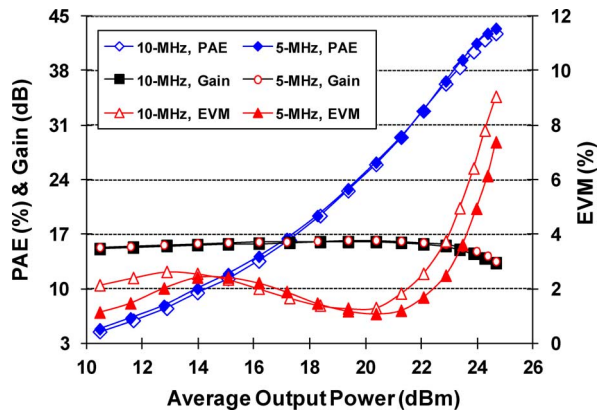

Fig. 17. Measured gain, EVM and overall PAE of the ET-PA (at high power mode) for the LTE 16QAM 5 MHz and 10 MHz signals, $\mathrm{V_{DD}} = 4.2$ V.

V. Measurement of the Monolithic BiCMOS ET-PA

A. Efficiency and Linearity for LTE Signals

Once the envelope modulator is optimized for our cascode PA, the entire ET-PA is evaluated for the LTE 16QAM signals. It operates at $\mathrm{V_{DD}}$ of 4.2 V. The die picture of the fully monolithic ET-PA is shown in Fig. 16, fabricated in the TSMC 0.35 μm SiGe BiCMOS technology. The total chip size is 1.5×1.1 mm^2. No predistortion algorithm was used in this system. Fig. 17 shows the measured EVM, gain and overall PAE of the ET-PA for the LTE 16QAM 5 MHz and 10 MHz signals at 1.9 GHz (high power mode). The quiescent current of the ET-PA is 17 mA. For keeping the EVM below 5%, the maximum linear $\mathrm{P_{out}}$ is 24 dBm with an overall PAE of 41% for the LTE 5 MHz signal. In order to achieve the same EVM for the LTE 10 MHz, the maximum linear $\mathrm{P_{out}}$ needs to be 0.6 dB lower than the case of LTE 5 MHz, resulting in an overall PAE of 38% at $\mathrm{P_{out}}$ of 23.4 dBm. When this ET-PA is backed off 0.5 dB from the maximum linear $\mathrm{P_{out}}$ levels, better EVM values of 3.6% and 3.7% can be achieved with overall PAE of 39% and 37% for the LTE 16QAM 5 MHz and 10 MHz signals, respectively.

The output spectra of the ET-PA and the stand-alone PA ($\mathrm{V_{CC}} = 4.2$ V) are plotted in Fig. 18. The ET-PA successfully passes the LTE spectral mask at $\mathrm{P_{out}}$ of 24 dBm. However, at the same $\mathrm{P_{out}}$ of 24 dBm, the output of the stand-alone PA

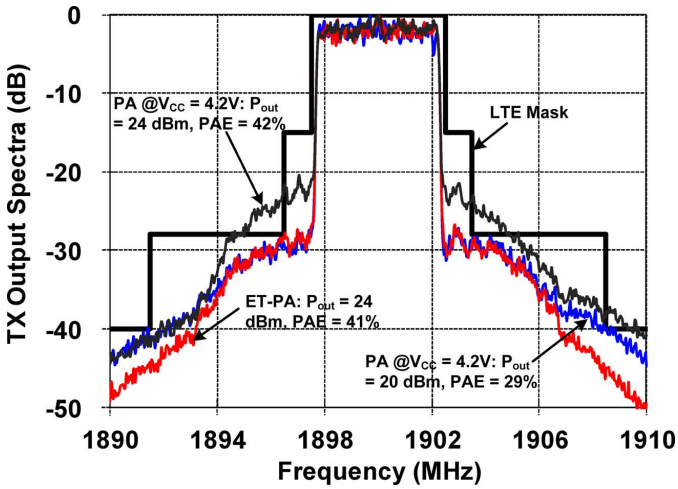

Fig. 18. Measured output spectra of the ET-PA and the stand-alone PA for the LTE 16QAM 5 MHz signal.

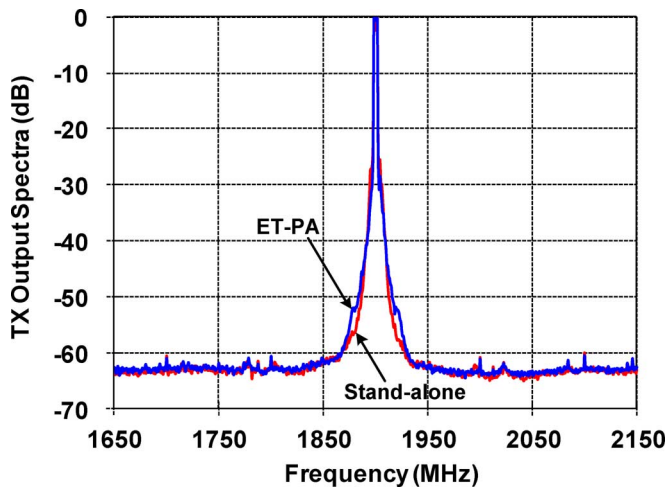

Fig. 20. Measured far-out output spectra of the ET-PA and stand-alone PA for the LTE 16QAM 5 MHz signal, both at P_{out} of 24 dBm.

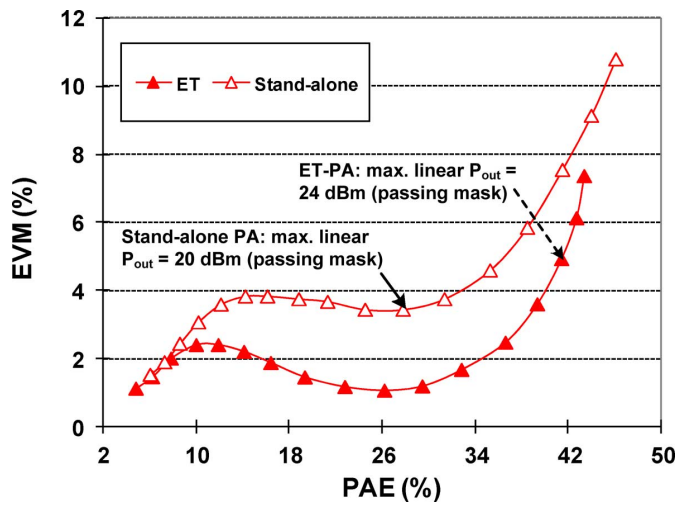

Fig. 19. Efficiency-linearity comparison for the ET-PA vs. stand-alone PA with the LTE 16QAM 5 MHz signal.

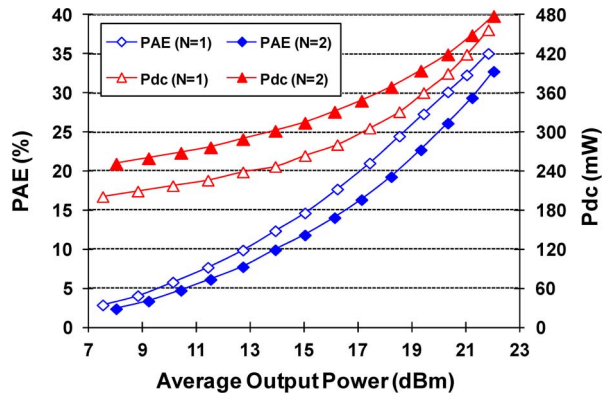

Fig. 21. Overall PAE and DC power dissipation (P_{dc}) of the proposed monolithic ET-PA for the LTE 16QAM 5 MHz signal at the high power mode ($N = 2$) vs. the low power ($N = 1$) mode, $V_{DD} = 4.2$ V.

fails the LTE spectral mask, forcing it to be backed off by at least 4 dB. The maximum linear P_{out} of the stand-alone PA is only 20 dBm at best, with a PAE of 29%. The linear P_{out} and PAE are, therefore, 4 dB and 12% lower than the ones achieved by the ET-PA system. To further demonstrate the advantages of ET-PA, Fig. 19 compares the PAE of the ET-PA and the stand-alone PA in terms of EVM. It clearly shows that at the same PAE, the ET-PA presents a better EVM. The ET technique improves the linearity of the PA, because the dynamic PA supply can reduce the intermodulation distortions (IMDs) by using certain envelope shaping method [6], [8], [10].

The measured far-out output spectra of the ET-PA and the stand-alone PA are plotted in Fig. 20 without any external filtering. Compared with the stand-alone PA, the ET-PA has little spectral regrowth at the offset of 20–30 MHz from the center frequency, but no strong spur appears at the offset frequency above 50 MHz. Such reasonable spurious emission was achieved by the envelope modulator with the low average switching frequency and the linear class-AB stage. The emission noise can be further suppressed by adding extra filtering or duplexer isolation. We also expect that, by using the silicon-on-insulator (SOI) technology or technology with high-resistivity silicon substrate, the noise coupled from the buck converter to the PA can be effectively reduced [33]. We would like to point out again that the switching ripples of the envelope modulator would be more critical in EER-PA systems, requiring the linear stage of much wider bandwidth (e.g., in the work of [4]), or even a plain linear regulator (e.g., in the work of [3]) in the system, which will inevitably lower the overall system efficiency.

B. Efficiency Enhancement at Low Power Mode

The power saving of the monolithic ET-PA by using the transistor resizing method is demonstrated by measuring the overall PAE and DC power dissipation at the high power mode and low power mode, respectively, as shown in Fig. 21. Fig. 22 shows the measured EVM performances of the ET-PA at both high/low power modes. To maintain a good EVM below 3% at the low power mode, the switching point is selected at P_{out} of 20 dBm. At P_{out} of 20 dBm and below, it is beneficial to switch off half of the transistor cells. At P_{out} of ~16–20 dBm, the PAE enhancement is ~4%, as shown in Fig. 21. The DC power consumption is also reduced once the ET-PA is switched to the low power

TABLE I
SUMMARY AND COMPARISON OF OUR MONOLITHIC ET-PAS WITH STATE-OF-THE-ART ET/EER PA AND/OR TX DESIGNS.

	Freq. (GHz)	V_{DD} (V)	Avg. P_{out} (dBm)	[1]Overall PAE	EVM	Signal BW (MHz)	Modulation	PD	Technology
[5]	2.0	3.3	19.6	22.6%	2.5%	20	WLAN 64QAM	No	0.13 μm CMOS
[6]	1.75	4.2	24.2	43%	4.8%	5	LTE 16QAM	No	0.35 μm SiGe BiCMOS
[8]	1.85	5	28.9	42.2%	2.69%	10	LTE 16QAM	No	PA: 2 μm InGaP/GaAs [2]EM: 0.18 μm CMOS
[9]	1.88	3	24.22	38.6%	3.64%	5	WiBro 16QAM	No	PA: 2 μm InGaP/GaAs EM: 0.13 μm CMOS
[10]	1.88	3.3	29	46%	---	3.84	WCDMA	No	PA: 2 μm InGaP/GaAs
	1.88	3.3	23.9	34.3%	2.98%	5	WiMAX 64QAM	No	EM: 0.13 μm CMOS
[12]	2.4	3.3	20	28%	5%	20	WLAN 64QAM	Yes	0.18 μm SiGe BiCMOS
[13]	2.535	3.3	25.8	32.3%	3%	10	LTE 16QAM	No	PA: 2 μm InGaP/GaAs EM: 0.35 μm CMOS
[14]	2.535	6	30	45%	---	20	LTE 16QAM	Yes	PA: GaAs HBT EM: 0.15 μm CMOS
[28]	1.92	2.1	15.3	22%	1.5%	5	WiMAX 64QAM	Yes	0.13 μm SOI-CMOS
This work	1.9	5.5	26.1	35%	4.2%	5	LTE 16QAM	No	PA: 0.35 μm SiGe BiCMOS EM: 0.35 μm BCD
		4.2	23.1	37%	4.9%				
This work	1.9	4.2	24	41%	4.9%	5	LTE 16QAM	No	0.35 μm SiGe BiCMOS
			[3]18	22%	1.1%				
	1.9	4.2	23.4	38%	4.9%	10	LTE 16QAM	No	

Note:
1. The overall PAE includes the efficiency of the envelope modulator
2. EM: envelope modulator
3. 6 dB back-off from the maximum linear P_{out} of 24 dBm

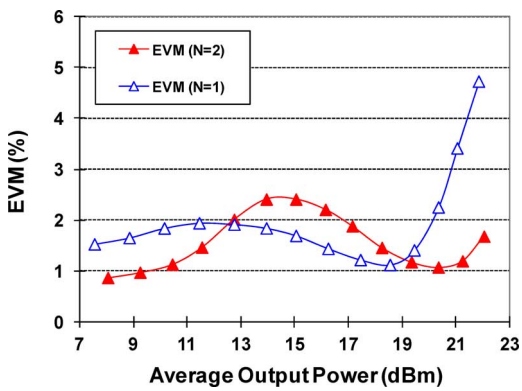

Fig. 22. Measured EVM of the ET-PA at high/low power modes for LTE 16QAM 5 MHz at 1.9 GHz; $V_{DD} = 4.2$ V.

mode. This efficiency enhancement was obtained without any off-chip output matching. Please note that instead of using the bulky on-chip LC balun [21], transmission line [22] or switchable transformer [24], our simple transistor resizing technique achieves similar efficiency enhancement with only a negligible increase of the chip area.

C. Performance Summary

Table I summarizes the performance of our ET-PA systems reported in this work (i.e., 1) the cascode SiGe PA with a separate BCD envelope modulator in a two-chip solution; and 2) the cascode SiGe PA integrated with the CMOS envelope modulator in a 0.35 μm SiGe BiCMOS technology) against other state-of-the-art ET/EER PA/TX designs in the literature. The integrated CMOS envelope modulator has better linearity than the BCD envelope modulator under the same V_{DD} of 4.2 V, because its class-AB stage is optimized for less distortion at V_{DD} of 4.2 V and its switching frequency is lower. With an EVM of 4.9%, the fully monolithic solution provides the linear P_{out} 0.9 dB higher than the two-chip solution under the same V_{DD} of 4.2 V, leading to a 4% higher PAE as well. Additionally, the active chip size (excluding bonding pads) of the CMOS envelope modulator is more compact than the BCD envelope modulator (i.e., 0.75×0.7 mm^2 vs. 1.1×1.1 mm^2). However, the supply voltage of the integrated envelope modulator is limited below 4.5 V, due to the low breakdown voltage of the CMOS transistors in the 0.35 μm SiGe BiCMOS technology. On the other hand, without any reliability issues, the ET-PA of the two-chip solution achieves the maximum linear P_{out} of 26.1 dBm with an overall PAE of 35% at V_{DD} of 5.5 V. For other high voltage applications, the BCD envelope modulator is a good candidate to drive a PA for high P_{out} under V_{DD} of 7 V, where the high power PA presents a small load to the envelope modulator.

Both of our designs are shown to be among the highest performances achieved by Si-based ET/EER PA and TX systems. Compared to the works in [8]–[10], [13], [14] using the III-V semiconductor technologies, our Si-based ET-PAs present very competitive overall efficiencies. In addition to the high efficiency achieved in the peak output power region, our ET-PA has achieved an additional efficiency enhancement of 4% at 4–8 dB back-off compared to the conventional ET-PA, saving the power consumption at the low power mode as well. If we further adopt the memoryless digital predistortion (PD) techniques (e.g., similar to the work in [14]), the EVM and ACPR can possibly be further improved, thus allowing deeper compression with higher P_{out} and overall PAE.

VI. Conclusion

We have presented two designs of Si-based ET-PA systems for LTE broadband applications. Both designs used a cascode SiGe PA with the transistor resizing technique. The first design provided a separate high voltage envelope modulator designed in a 0.35 μm BCD technology, capable of driving a small resistive load with high efficiency. When the SiGe PA is modulated by the BCD envelope modulator for the LTE 16QAM 5 MHz signal at 1.9 GHz, a maximum linear $\mathrm{P_{out}}$ of 26.1 dBm with overall PAE of 35% was achieved at $\mathrm{V_{DD}}$ of 5.5 V. The second design provided a CMOS envelope modulator, integrated with the PA in a 0.35 μm SiGe BiCMOS technology. The integrated envelope modulator was optimized for better linearity and spurious noise with a relaxed bandwidth requirement. The fully monolithic ET-PA system reached the maximum linear $\mathrm{P_{out}}$ of 24 dBm and 23.4 dBm with overall PAE of 41% and 38% for the LTE 16QAM 5 MHz and 10 MHz signals, respectively. At the same $\mathrm{V_{DD}}$ of 4.2 V, due to lower distortion of the integrated envelope modulator, the maximum linear $\mathrm{P_{out}}$ was extended by 0.9 dB with the same EVM compared to the two-chip solution, leading to higher PAE as well. Compared with conventional ET-PAs, the transistor resizing technique further enhanced the efficiency of our ET-PAs at the average low power region, which has been demonstrated by both designs.

Acknowledgment

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References

[1] C. U. Castellanos, D. L. Villa, C. Rosa, K. I. Pedersen, F. D. Calabrese, P.-H. Michaelsen, and J. Michel, "Performance of uplink fractional power control in UTRAN LTE," in *Vehicular Tech. Conf.*, 2008, pp. 2517–2521.

[2] N. J. Quintero, "Advanced Power Control for UTRAN LTE Uplink," Master, Aalborg University, , 2008.

[3] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.

[4] R. Shrestha, R. v. d. Zee, A. d. Graauw, and B. Nauta, "A wideband supply modulator for 20 MHz RF bandwidth polar PAs in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1272–1280, Apr. 2009.

[5] J. S. Walling, S. S. Taylor, and D. J. Allstot, "A class-G supply modulator and class-E PA in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2239–2347, Sep. 2009.

[6] Y. Li, J. Lopez, P.-H. Wu, W. Hu, R. Wu, and D. Y. C. Lie, "A SiGe envelope-tracking power amplifier with an integrated CMOS envelope modulator for mobile WiMAX/3GPP LTE transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2525–2536, Oct. 2011.

[7] J. Lopez, Y. Li, J. D. Popp, D. Y. C. Lie, C.-C. Chuang, K. Chen, S. Wu, T.-Y. Ying, and G.-K. Ma, "Design of highly efficient wideband RF polar transmitter using the envelope-tracking technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2276–2294, Sep. 2009.

[8] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho, and B. Kim, "Optimization for envelope shaped operation of envelope tracking power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 7, pp. 1787–1795, Jul. 2011.

[9] J. Choi, D. Kang, D. Kim, and K. Kim, "Optimized envelope tracking operation of Doherty power amplifier for high efficiency over an extended dynamic range," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 6, pp. 1508–1515, Jun. 2009.

[10] J. Choi, D. Kim, D. Kang, and B. Kim, "A polar transmitter with CMOS programmable hysteretic-controlled hybrid switching supply modulator for multistandard applications," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 7, pp. 1675–1686, Jul. 2009.

[11] F. Wang, D. F. Kimball, J. D. Popp, A. H. Yang, D. Y. C. Lie, P. M. Asbeck, and L. E. Larson, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN application," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4086–4099, Dec. 2006.

[12] F. Wang, D. F. Kimball, D. Y. C. Lie, P. M. Asbeck, and L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.

[13] J. Choi, D. Kim, D. Kang, and K. Kim, "A new power management IC architecture for envelope tracking power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 7, pp. 1796–1802, Jul. 2011.

[14] M. Hassan, M. Kwak, V. W. Leung, C. Hsia, J. J. Yan, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "High efficiency envelope tracking power amplifier with very low quiescent power for 20 MHz LTE," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2011, pp. 1–4.

[15] M. Kwak, D. F. Kimball, C. D. Presti, A. Scuderi, C. Santagati, J. J. Yan, P. M. Asbeck, and L. E. Larson, "Design of a wideband high-voltage high-efficiency BiCMOS envelope amplifier for micro-base-station RF power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1850–1861, Jun. 2012.

[16] B. J. Minnis, P. A. Moore, P. N. Whatmough, P. G. Blanken, and M. P. van der Heijden, "System-efficiency analysis of power amplifier supply-tracking regimes in mobile transmitters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 1, pp. 268–279, Jan. 2009.

[17] J. Deng, P. S. Gudem, L. E. Larson, and P. M. Asbeck, "A high average-efficiency SiGe HBT power amplifier for WCDMA handset applications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 529–537, Feb. 2005.

[18] J. Deng, P. S. Guden, L. E. Larson, D. F. Kimball, and P. M. Asbeck, "A SiGe PA with dual dynamic bias control and memoryless digital predistortion for WCDMA handset applications," *IEEE J. Solid-State Circuits.*, vol. 41, no. 5, pp. 1210–1221, May 2006.

[19] K. Han and B. Kim, "A parallel power amplifier with a novel mode switching control," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 3, pp. 200–202, Mar. 2008.

[20] G. Hau, S. Caron, J. Turpel, and B. MacDonald, "A 20 mA quiescent current 40% PAEWCDMAHBT power amplifier module with reduced current consumption under backoff power operation," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2005, pp. 243–246.

[21] P. Reynaert and M. S. J. Steyaert, "A 2.45-GHz 0.35-μm CMOS PA with parallel amplification," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 551–562, Mar. 2007.

[22] A. Shirvani, D. K. Su, and B. A. Wooley, "A CMOS RF power amplifier with parallel amplification for efficient power control," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 684–693, Jun. 2002.

[23] J. Kim, Y. Yoon, H. Kim, K. H. An, W. Kim, H.-W. Kim, C.-H. Lee, and K. T. Kornegay, "A linear multi-mode CMOS power amplifier with discrete resizing and concurrent power combining structure," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1034–1048, May 2011.

[24] D. Chowdhury, C. D. Hull, O. B. Degani, Y. Wang, and A. M. Niknejad, "A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4G WiMAX applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393–3401, Dec. 2009.

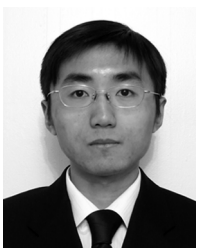
[25] J. Jeong, D. F. Kimball, M. Kwak, C. Hsia, P. Draxler, and P. M. Asbeck, "Wideband envelope tracking power amplifier with reduced bandwidth power supply waveform," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 1381–1384.

[26] M. Kwak, D. Kimball, C. Presti, A. Scuderi, C. Santagati, J. Yan, P. Asbeck, and L. Larson, "Wideband high efficiency envelope tracking integrated circuit for micro-base station power amplifiers," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2011, pp. 1–4.

[27] Y. Li, R. Wu, J. Lopez, and D. Y. C. Lie, "A highly-efficient BiCMOS cascode class-E power amplifier using both envelope-tracking and transistor resizing for LTE-like applications," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Oct. 2011, pp. 142–145.

[28] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25 dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.

[29] Y. Li, J. Lopez, D. Y. C. Lie, K. Chen, S. Wu, T.-Y. Yang, and G.-K. Ma, "Circuits and system design of RF polar transmitters using envelope-tracking and SiGe power amplifiers for mobile WiMAX," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 893–901, May 2011.
[30] J. N. Kitchen, C. Chu, S. Kiaei, and B. Bakkaloglu, "Combined linear and Δ-modulated switch-mode PA supply modulator for polar transmitters," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 404–413, Feb. 2009.
[31] Y. Li, J. Lopez, D. Y. C. Lie, K. Chen, S. Wu, and T.-Y. Yang, "Efficiency enhancement and linearity trade-offs for cascode vs. common-emitter SiGe power amplifiers in WiMAX polar transmitters," in *Proc. IEEE Int. Circuits Syst. Symp.*, May 2010, pp. 1915–1918.
[32] R. J. Baker, H. W. Li, and D. E. Boyee*, CMOS Circuit Design, Layout, and Simulations*, 1st ed. : Wiley-IEEE Press, 1997, pp. 657–658.
[33] A. Tombak, R. J. Baeten, J. D. Jorgenson, and D. C. Dening, "Ingeration of a cellular handset power amplifier and a DC/DC converter in a silicon-on-insulator (SOI) technology," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2008, pp. 413–416.
[34] E. J. Kim, C.-H. Cho, W. Kim, C.-H. Lee, and J. Laskar, "Spurious noise reduction by modulating switching frequency in DC-to-DC converter for RF power amplifier," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, May 2010, pp. 43–46.
[35] J.-H. Chen, P.-J. Liu, and Y.-J. E. Chen, "A spurious emission reduction technique for power amplifiers using frequency hopping DC-DC converters," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Jun. 2009, pp. 145–418.
[36] C. Tao and A. A. Fayed, "A GSM power amplifier directly-powered from a DC-DC power converter," *IEEE Microw. Wireles Compon. Lett.*, vol. 22, no. 1, pp. 38–40, Jan. 2012.
[37] C. Park, Y. Kim, Y. Kim, H. Kim, and S. Hong, "A 1.9-GHz CMOS power amplifier using three-port asymmetric transmission line transformer for a polar transmitter," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 2, pp. 230–238, Feb. 2007.
[38] T. Sowlati and D. M. W. Leenaerts, "A 2.4-GHz 0.18-μm CMOS self-biased cascode power amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1318–1324, Aug. 2003.



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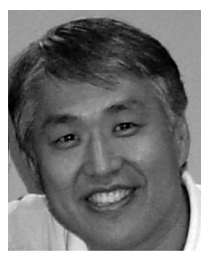

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