A 19 dBm 0.13µm CMOS Parallel Class-E Switching PA with Minimal Efficiency Degradation under 6 dB Back-off

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Abstract — **This paper implements a digital Zero Voltage Switching (ZVS) Contour based power amplifier previously proposed by the authors in [1]. The proposed PA implemented in 0.13µm digital CMOS technology, achieves a peak power of 19dBm at a peak drain efficiency of 23% and peak power added efficiency (PAE) of 18% at a center frequency of 800MHz from a 1.2V supply. The PA can maintain its peak efficiency over a 6dB dynamic range of output power by a simultaneous load and duty cycle modulation of a parallel class E PA. The PA achieves an average drain efficiency of 20% and an average PAE of 15% while generating 6dB peak to minimum ratio (PMR) OQPSK signal with bandwidths up to 20Mbps.**

Index Terms — **PA, PMR, PAR, PAE.**

I. Introduction

Power amplifier design presents the twin, and often contradictory, challenges of achieving linearity and efficiency. Advances in switching and/or digital PA architectures [2–6] have improved both linearity and the efficiency achieved at peak output power. However, invariably, efficiency still degrades rapidly with output power back-off resulting in low average efficiency particularly while generating non-constant envelope modulated signals with a large peak-to-average power ratio (PAR).

In architectures based on a class-E switching PA [2-3], the efficiency degradation at backed-off power levels is primarily due to so-called Zero Voltage Switching (ZVS) conditions being violated. This paper presents a digital *ZVS Contour PA* proposed by the authors in [1] that employs a combination of duty cycle and load modulation to satisfy ZVS conditions and thereby maintains a nearly constant efficiency for a 6dB back-off in output power. Measurement results on an 800MHz PA built in 0.13µm digital CMOS technology show that the proposed PA can maintain a peak drain efficiency of 23% over a 6dB range of output power. Furthermore dynamic testing of the PA with a 6dB PMR OQPSK modulated signal with bandwidths up to 20Mbps show that the PA achieves an average drain efficiency of 20%, suggesting that the dynamic losses associated with the PA are also minimal.

The paper is divided into 3 sections. In section II, we first briefly summarize and intuitively explain the concept behind the *ZVS Contour PA,* proposed by the authors in [1]. Section III, and IV extend the previous work in [1] by implementing a prototype PA in 0.13µm digital CMOS technology. In Section III we briefly discuss the practical IC implementation of the proposed PA. Measurement results showing that the PA not only achieves a peak power of 19dBm from a 1.2V supply at 23% drain efficiency but also maintains this efficiency for a 6dB range of output power are presented in section IV. Measurements from dynamic testing of the PA with 6dB PMR OQPSK signals with bandwidths up-to 20Mbps are also discussed in Section IV.

II. ZVS Contour PA: Concept

Conventionally a class E PA is deigned to meet the so called ZVS conditions at 50% duty cycle and a particular output power level from a fixed supply voltage [2]. ZVS conditions ensure that just when the transistor turns ON during each carrier period, the drain voltage is at zero thereby avoiding any wasted power in discharging the drain capacitance. Power back-off in such schemes with a fixed supply voltage is commonly realized by either reducing the duty cycle, D, of the drive waveform or increasing the load, R_{eq} seen by the PA (Fig. 1(a)). However increasing R_{eq}, decreases the rate of discharge of the drain capacitor C through the load when the switch is turned OFF. Similarly decreasing the duty cycle D, gives the drain capacitor C more time to discharge, allowing it to discharge fully and then charge up again through the load during the time when the switch is OFF. Thus in both the cases, the drain voltage is non-zero at the switch turn-on instance, leading to a violation of ZVS conditions and thus lower efficiency under power back-off conditions.

The proposed PA is based on the fact that it is possible to meet ZVS conditions and thus ideally 100% efficiency in a parallel class E PA, not only at a particular power level but also at backed-off power levels by a simultaneous modulation of the duty cycle D, drain capacitance $C(D)$ and the load seen by the PA, $R_{eq}(D)$ (Fig 1(a)). For example if at increased load conditions, the drain capacitor C is given more time to discharge, i.e. if

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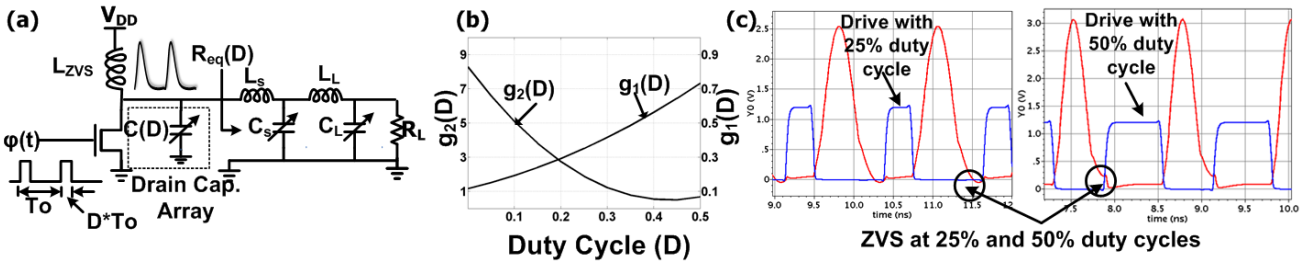

Fig. 1. (a) A schematic for the proposed *ZVS Contour PA*, (b) the variation of $g_1(D) = L_{zvs}\omega_0/R_{eq}(D)$ and $g_2(D) = C(D)\,\omega_0 R_{eq}(D)$ with duty cycle D, (c) the simulated drain waveforms at 25% and 50% duty cycle..

we allow the duty cycle D to be simultaneously reduced, then the drain capacitor can still discharge to zero when the switch turns ON. Specifically, if D, C, and R_{eq} are chosen such that,

$$\omega_0 L_{ZVS} / R_{eq}(D) = g_1(D),\ \omega_0 C(D) R_{eq}(D) = g_2(D) \quad (1)$$

then ZVS conditions are satisfied at the output power level,

$$P_{out}(D) = g_3(D) V_{DD}^2 / R_{eq}(D), \quad (2)$$

where g_1, g_2 are functions of D plotted in Fig. 1(b), derived using numerical techniques, omitted here for the sake of brevity. Fig. 1(c) shows the simulated drain waveforms of the implemented PA clearly showing that the PA achieves ZVS at 25% and 50% duty cycles.

III. Practical IC Implementation

As mentioned before the duty cycle, D, the drain capacitance, $C(D)$ and the load presented to the PA, $R_{eq}(D)$ need to be simultaneously modulated to realize a *ZVS Contour PA*. Fig. 2 shows the detailed circuit schematic of the prototype IC built in 0.13µm CMOS which implements the proposed *ZVS Contour PA*. A LC-LC tunable transformation network is used to vary $R_{eq}(D)$. The duty cycle modulation is performed by digitally controlling a cascade of inverters while the drain capacitance variation is achieved by using a bank of capacitors, each connected in series with a digitally controlled NMOS switch.

A. Tunable Drain Network

The drain network consists of a tunable drain capacitance bank and a tunable impedance transformation network (Fig. 2). The requirements on the tunable transformation network are two-fold. Firstly, as the duty cycle, D is changed from 50% to 15%, the network should be able to vary $R_{eq}(D)$ by 4x (from 5Ω to 20Ω), corresponding to 4x change in the function $g_1(D)$. Secondly, this required variation in $R_{eq}(D)$ should be achieved without much degradation in the network efficiency and only by changing a few capacitances connected from particular nodes to the electrical ground node of the network. A cascade of two low pass LC networks was used to achieve the desired transformation in $R_{eq}(D)$. Note that the inductors L_s (1nH) and L_L (1.5nH) are fixed and only the capacitances $C_s(D)$ and $C_L(D)$ are varied along with the duty cycle, D to realize $R_{eq}(D)$ (Fig. 2). The capacitances $C_s(D)$ and $C_L(D)$ as well as the drain capacitor bank $C(D)$ were implemented using binary weighted capacitance banks with a 6 bits precision. To increase or decrease the capacitance, appropriate amount of capacitance is switched in/out by turning ON/OFF one or more branches in the banks. In particular $C_s(D)$ needs to be varied from 12pF to 48pF while the $C_L(D)$ was varied from 10pF to 20pF for a 4x change in $R_{eq}(D)$. The drain capacitance $C(D)$ was varied from 10pF to 20pF corresponding to an 8x change in the function $g_2(D)$. Simulations show that with a quality factor of 15, the efficiency of the network increases from 70% to 90% as $R_{eq}(D)$ is increased from 5• to 20• by changing the capacitances $C_s(D)$ and $C_L(D)$. With no ultra-thick-metals (UTM) available in the digital CMOS technology in which the IC was designed and fabricated, the inductors L_s (1nH) and L_L (1.5nH) were realized using off-chip components which were tested separately and found to have a Q of 15 at 800MHz.

B. Duty Cycle Modulation

Duty cycle modulation is performed by changing the fall-time of a phase modulated waveform with nominally 50% duty cycle. This is achieved by increasing or decreasing the resistance in the pull down path of a CMOS inverter. Appropriate amount of resistance is switched in/out to increase/decrease the duty cycle. A cascade of three such binary weighted inverters with a two-bit binary

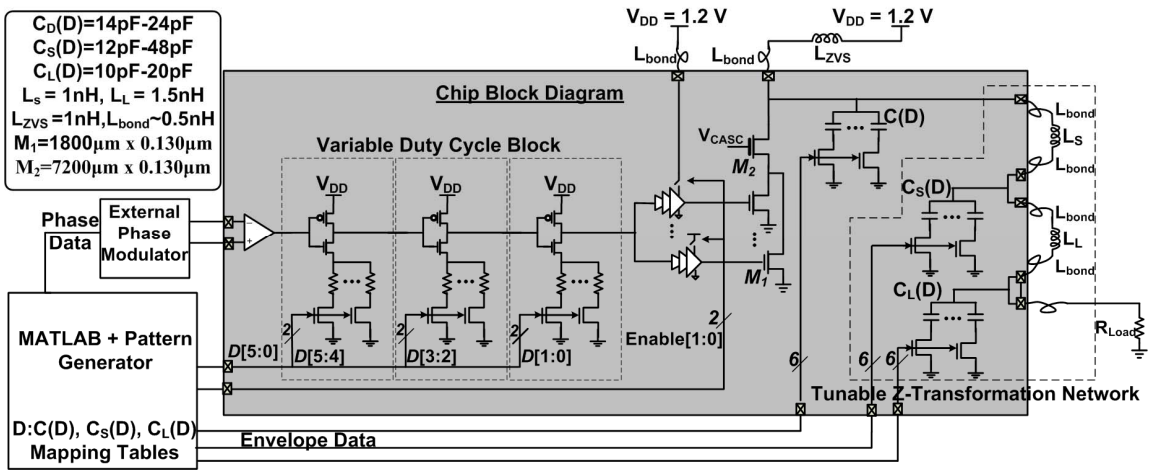

Fig. 2. A schematic of the proposed *ZVS Contour PA* implemented in 0.13µm digital CMOS technology.

weighted control in each inverter (Fig. 2) varies the duty cycle with a 6bit precision from 15% to 50% The first inverter is controlled by two most significant bits of the duty cycle control word, thus providing a coarse control of the duty cycle while the subsequent stages provide for a finer control. Simulations suggest that a resolution of 6 bits is enough to calibrate for variations in duty cycle due to 10-15% component mismatch. As the duty cycle modulation is performed before the main PA drivers, the implementation is low power and also wide-bandwidth. However the main PA drivers limit the smallest pulse which can pass without any distortion, limiting the lowest duty cycle to about 15%.

C. Parallel Class E PA and Split PA Drivers

A parallel class E PA is designed to operate in a push-pull fashion (Fig. 2 shows only single ended operations). The differential outputs were combined on board using an external transformer. To improve the peak output power and to reduce device stress common in class-E PAs, a cascode device is used (Fig. 2). The cascode switch size, (7200µm x 0.13µm) along with the off-capacitance of the drain capacitor bank and the fixed drain inductance L_{zvs} (1nH) are chosen so as to satisfy ZVS conditions at 50% duty cycle. The fixed drain inductance L_{zvs} is realized using off-chip components for the lack of any ultra thick metals. The LC-LC network is designed so as to transform 25Ω to R_{eq} of 5Ω at 50% duty cycle. The PA's switching device is broken up into four nominally identical parts (4 x 1800µm x 0.13µm) with independent drivers. The PA drivers are inverter based with a fan-out of about 2.5 so as to provide sufficient buffering of the phase and duty cycle modulated drive waveform. Each PA switch segment and the corresponding driver can be individually turned ON or OFF using a two bit 'Enable' control as shown in Fig. 2. At low output powers, some of these PA segments and drivers are turned OFF to reduce driver power. Consequently, not only is the drain efficiency of the *ZVS Contour PA* maintained relatively constant, the overall efficiency also suffers minimal degradation.

IV. Measurement Results

A prototype PA occupying an area of 1.6mmx1.9mm (Fig. 3(a)) was built in 0.13µm digital CMOS technology. Measurements show that the PA achieves 23% drain efficiency and a PAE of 18% at peak output power of 19 dBm from a 1.2V supply at 800MHz. Note that though off-chip inductors have been used, the measured quality factor of these inductors was only 15, fairly comparable to that offered by on-chip inductors built with ultra thick metals in RF CMOS technologies. Simulations show that a higher peak power (21.5 dBm), higher drain efficiency (40%) and wider dynamic range (~8.5dB) were possible if not for an unanticipated 2Ω resistance in the ground path due to a layout mistake. Fig. 3(c) shows both the measured drain efficiency and the measured PAE plotted as a function of the output power. Note that the efficiency of the *ZVS Contour PA* degrades by only 20% for a 6 dB output power back-off. In contrast most prevalent state-of-the art PA architectures have about 40% to 50% degradation in efficiency for the same back-off (Table I).

The *ZVS Contour PA* was also tested under dynamic conditions with a 6dB PMR OQPSK signals. To do this, first 64 distinct codes, where the PA satisfies ZVS conditions by design, are chosen within the output voltage dynamic range of 6dB by sweeping through the 26 bit codes (6 bits for the duty cycle and 18 bits for the capacitor arrays, 2 bits for the enable control). A mapping from the 64 code values to the output voltage and output phase is thus obtained. Next the inverse of this mapping is used to pre-distort the envelope and the phase signal. The pre-distorted envelope and the phase signal are then over-

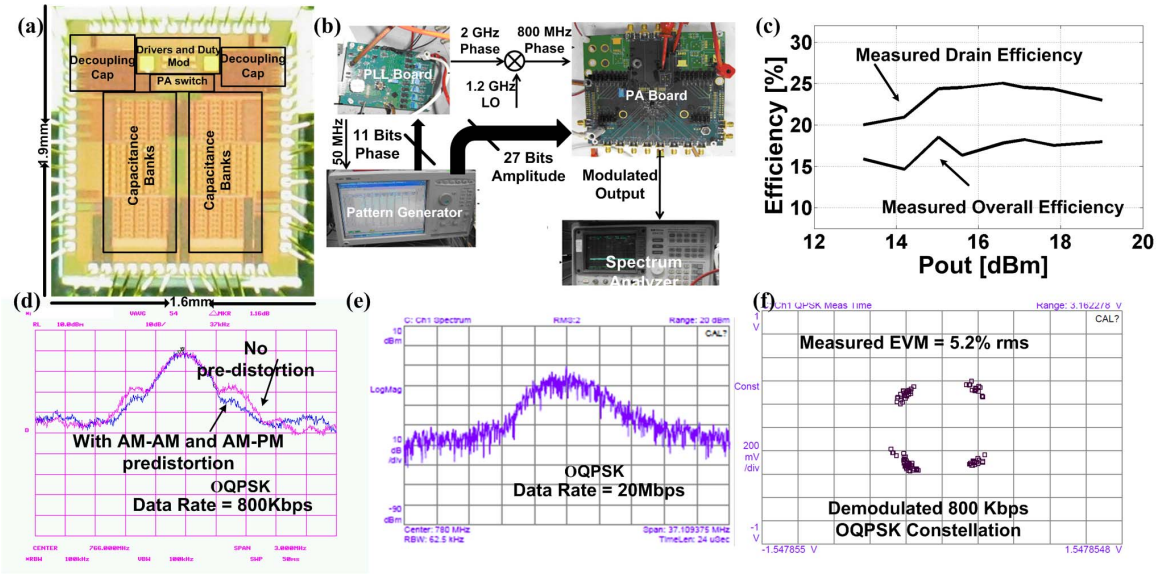

Fig. 3. (a) Die Photograph (b) Measurement set-up, (c) Measured Drain Efficiency and PAE vs. Output Power, (d) Output spectrum with 800Kbps OQPSK signal, (e) Output spectrum with 20Mbps OQPSK signal, (f) Demodulated 800Kbps OQPSK signal.

TABLE I
PERFORMACE COMPARISON OF THE ZVS CONTOUR PA WITH STATE-OF-THE ART

Reference	Process [nm]	Supply Voltage [V]	Peak Power [dBm]	Peak PAE [%]	[%] Efficiency Degradation at 6dB back-off
[2]	65	2.5	28.6	28	40
[4]	180	1.7	22.6	NA	50
[5]	65	1.0	21.8	38	50
This Work	130	1.2	19	18	20

sampled at 50MHz and quantized to 6bits. The pre-distorted, over-sampled and quantized envelope is then utilized to dynamically change the duty cycle, capacitor arrays $C_s(D)$, $C_L(D)$, $C(D)$ and Enable bits settings (Fig. 3(b)), thus generating the instantaneous envelope. The phase bits are passed on to a PLL [6] which generates the phase modulated 50% duty cycle carrier, which is applied to the digital PA (Fig. 3(b)).

The *ZVS Contour PA* was able to reliably generate 6dB PMR 800Kbps OQPSK modulated signal with an average drain efficiency of 20%. Note that the average efficiency is only 3% below the peak efficiency. Further testing with bandwidths up to 20Mbps shows no degradation in the average efficiency, clearly suggesting that the loss incurred in dynamically switching the PA is extremely small. Fig. 3(d) and 3(e) show the measured power spectral density of the PA output when tested with 800Kbp/s and 20Mbps OQPSK signals. Fig. 3(f) shows the demodulated output while using 800Kbps OQPSK signal with the measured EVM performance being -26dBc. The ACPR measured at an offset of 1MHz and 5MHz while generating the 800Kbps OPSK signal was found to be less than -40dBr and -50dBr respectively.

V. Conclusion

In conclusion, a *ZVS Contour PA* which can maintain its peak efficiency for a 6dB back-off in output power has been described. The PA can reliably generate 6dB PMR OQPSK signal with bandwidths up-to 20Mbps with an average drain efficiency of 20%.

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