A 900-MHz 29.5-dBm 0.13-μm CMOS HiVP Power Amplifier

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***Abstract*—Using ST 0.13-μm CMOS technology, a class A power amplifier has been developed for the global system for mobile communication in Europe. To solve the problem of low breakdown voltage in deep-submicrometer CMOS technology, the high-voltage/high-power (HiVP) device configuration is used. With the HiVP configuration, a large voltage can be divided by several devices so that the voltage drop on each device can be limited under the breakdown voltage. The measurement results show that the output power of 29.5 dBm has been achieved at the frequency of 900 MHz. The linear power gain reaches 11.5 dB and the maximum power-added efficiency is as high as 34.5%.**

***Index Terms*—CMOS, global system for mobile communication (GSM), high voltage/high power (HiVP), power amplifier.**

I. Introduction

TODAY, the evolution of CMOS technologies and the high level of integration are also attractive for RF and microwave applications. Many ongoing efforts are focused on the integration of RF circuits in standard CMOS technologies, in order to allow the implementation of RF front-ends with digital signal processors, and enable low-cost single-chip fully integrated solutions. The power amplifiers are indispensable components in the cellular phones of the mobile communication systems. Recent years have seen a worldwide effort to develop power amplifiers in deep-submicrometer CMOS processes [1]–[4]. Still, the power amplifier circuits are a design bottleneck in the deep-submicrometer CMOS processes. Usually, a large RF output voltage is required to achieve a large output power. However, the maximum allowable voltage of a MOSFET in the deep-submicrometer CMOS processes is well limited. For instance, the supply voltage of a conventional 0.13-μm CMOS transistor is only 1.5 V and the breakdown voltage is close to 2.5 V. The gate–drain–voltage $V_{\rm gd}$ of a MOS transistor is especially critical due to the field distribution along the channel and the extreme thin gate oxide. To overcome this problem, the high-voltage/high-power (HiVP) structure [5], [6] is employed in this study in which several transistor devices are connected dc and RF in series. Therefore, the large drain voltage can be divided by all the cascaded devices. In this paper, methods for achieving equal voltage division and compact layout for the large MOSFETs are introduced. Simulation and measurements results are also presented.

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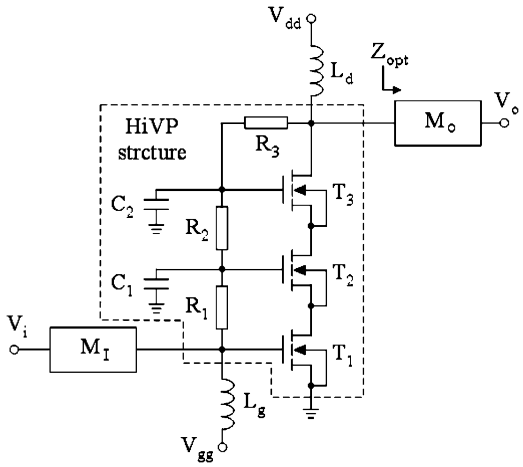

Fig. 1. Schematic of the HiVP power amplifier.

II. Design Process of the HiVP Power Amplifier

In this section, the functional principle of the proposed HiVP power amplifier is described in detail and further illustrated with simulation results. Finally, the design process of a compact layout is introduced.

A. Functional Principle of the HiVP Power Amplifier

Fig. 1 shows the schematic of the proposed power amplifier circuit. In order to achieve a relatively high output power, the maximum available supply voltage in a cellular phone $V_{\rm dd}$ of 3.6 V should fully be applied. However, since the breakdown voltage of the transistor is only close to 2.5 V, even the supply voltage itself is already overstrained for a single transistor. Therefore, the HiVP configuration is adopted here as the active device. As shown in Fig. 1, several identical transistor devices are connected in series by which the large drain voltage of the top device required for the high output power can be shared. On the other hand, the transistors used in the HiVP configuration should have identical operating points since the same current flows through them. Therefore, the numbers of the transistors used in the HiVP structure must be limited due to the limited supply voltage. In this study, three transistor devices T_1–T_3 are used, as shown in Fig. 1.

To ensure equal drain–source–voltages $V_{\rm ds}$ at all transistors, the voltage divider formed by resistors R_1–R_3 is adopted. The gate–source–voltage $V_{\rm gs}$ of the transistors are also identical since they are determined by the voltage source $V_{\rm gg}$. The

resistor R_3 also serves as a feedback to allow the gate voltages of T_1–T_3 to swing with the RF output signal. In this manner, $V_{\rm gd}$ of each transistor can remain smaller than the maximum allowable voltage for the transistors.

Besides the HiVP structure, the two inductors $L_{\rm d}$ and $L_{\rm g}$, shown in Fig. 1, serve as RF chokes of the amplifier circuit, which feed dc power to the gate and drain, respectively. Additionally, the input and the output matching networks (M_I and M_O) are employed. The output matching network is especially important. Due to the low dc supply voltage, high output power can only be obtained in case that the 50-Ω load is transformed to a much smaller resistance, the so-called optimum output impedance $Z_{\rm opt}$, which can be calculated as follows:

$$Z_{\rm opt} = \frac{V_{\rm dd}^2}{2P_{\rm out}} \tag{1}$$

where $P_{\rm out}$ is the expected output power. With this impedance, the peak RF current will not exceed $V_{\rm dd}/Z_{\rm opt}$, and the dc drain current bias must approximately be set to this value. Since the peak drain current is the sum of the bias and peak RF current, the transistor must be dimensioned to supply approximately $2V_{\rm dd}/Z_{\rm opt}$ with minimum voltage drop. However, the peak value of the drain voltage of the top device can even be higher than $2V_{\rm dd}$, depending on the resonance circle used in the output matching network. This value can be overstrained for the three transistors used in the HiVP structure. Therefore, the drain voltage of the top device (e.g., T_3 in Fig. 1) must be reduced. That means the large output power should be obtained more by an even larger current rather than by a higher voltage. Two modifications must be implemented. The first one is further reducing $Z_{\rm opt}$. The ratio of the impedance transformation from the load resistance of 50 Ω to the optimum output impedance is enhanced. Therefore, the ratio of the voltage transformation through the output matching network is also increased. In this case, only a lower drain voltage of T_3 is necessary for the required large voltage swing on the load resistance of 50 Ω. The other modification is to increase the gatewidth of the transistors in order to allow an even larger current to flow through the HiVP structure. Finally, transistors having a gatewidth of 4.5 mm are selected in this study.

The drain impedance of T_3 is mainly determined by $Z_{\rm opt}$, which is obtained from the impedance transformation at the output, as shown in Fig. 1. On the other hand, the impedance seen at the drains of T_2 and T_1 can separately be adjusted by the shunt capacitors C_2 and C_1, which are connected between the floating gates of the MOS transistors and ground. The relationship between the drain impedance $Z_{d,i}$ of the transistor T_i and the shunt capacitance C_i can be described as follows [7]:

$$Z_{d,i} \approx \frac{1}{g_m} \cdot \left(1 + \frac{C_{\rm gs}}{C_i}\right) \tag{2}$$

where i is an integer between 1 and 2. Clearly, a higher drain impedance level requires a smaller shunt capacitance. By tuning the shunt capacitance, a gradually reduced drain impedance can be obtained from the top transistor T_3 to the bottom one T_1. Since the transistors are connected in series, and hence, the same current flows through all the transistors, gradually reduced drain voltage is realized from T_3 to T_1. In other words, the drain voltage of T_3 is divided by all three transistors used in the HiVP configuration. Additionally, an equal voltage division can even be achieved by using several methods. One of the methods is optimizing the values of the resistors used in the voltage divider [7].

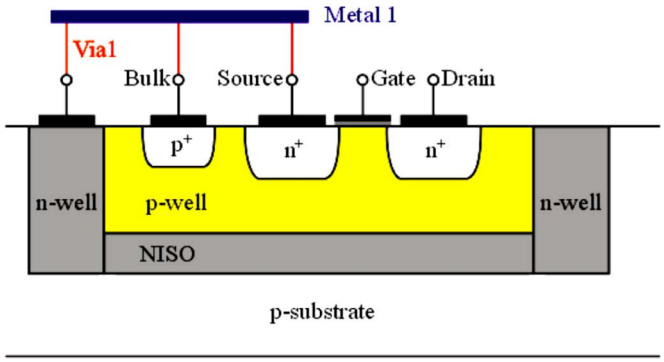

Fig. 2. Cross section of the isolated NMOS transistors.

In order to realize that the voltage difference between every two terminals of the transistor is smaller than the maximum allowable voltage, the bulk voltage of the transistors must also swing with the RF voltages of the other transistor terminals. In this study, the bulk of every transistor is, therefore, connected to the source, as shown in Fig. 1. For this reason, p-well is required to isolate the NMOS transistors from the substrate, as illustrated in Fig. 2. Furthermore, the p-well is separated by the NISO layer from the p-substrate in the vertical direction and it is embraced by the n-well layers laterally. In this manner, a NMOS transistor is totally isolated from the substrate; hence, the bulk of it can be connected with the source using metal layers. However, a p-n junction is generated due to the direct contact of the n- and the p-well, which causes additional power loss. To avoid this secondary effect, the n-well layer must be connected to a higher positive voltage level than the p-well. Another possibility to avoid the power loss is to directly short the n- and p-well, also using the metal layers, as shown in Fig. 2.

B. Simulation

The dc behavior of the HiVP structure has first been simulated. The simulated output characteristic is presented in Fig. 3 in comparison with that of a single transistor, which has the same dimensions as the transistors used in the HiVP structure.

Similar dc behaviors are obtained from both configurations. Therefore, the HiVP configuration can approximately be regarded as a single transistor device. The gate of the bottom transistor T_1 can be considered as the input, and the drain of the top transistor T_3 can be considered as the output of this device, respectively. The difference between the HiVP structure and a conventional single transistor is that the former has a much higher ability to carry the voltage. However, compared to a single transistor, the output characteristic lines of the HiVP structure are shifted to the right since the supply voltage $V_{\rm dd}$ is divided by all the three transistors. According to the load-line matching theory [8], the maximum range of the voltage swing

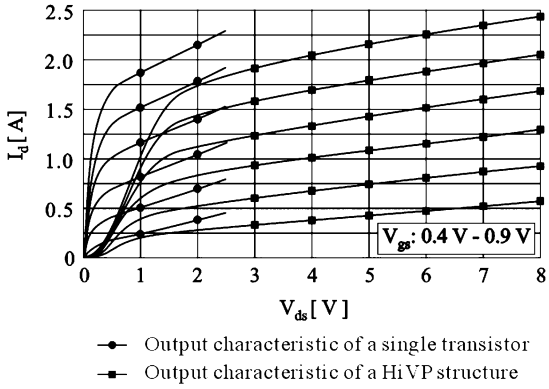

Fig. 3. Output characteristic of the HiVP structure and of a single transistor.

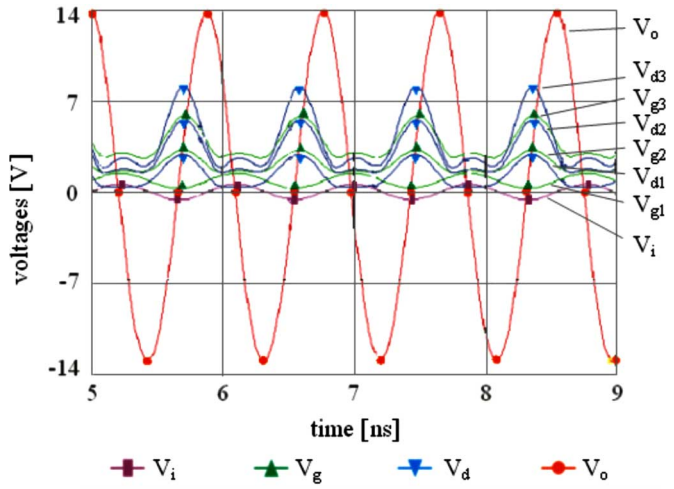

Fig. 4. Simulated waveforms for the RF voltages.

is required for the maximum achievable output power. Since the supply voltage of a cellular phone is fixed and the output characteristic lines are shifted to the right, the maximum swing range for the output voltage is reduced. The more transistors used in the HiVP structure, the more critical this problem becomes. Therefore, the minimum number of the transistors that are able to sustain the required output voltage has to be chosen.

A class A power amplifier is proposed in this study. The voltage $V_{\rm gg}$ of 0.8 V is selected, while the supply voltage $V_{\rm dd}$ is 3.6 V, as mentioned above. The input and output matching networks are designed in order to obtain a complex conjugate matching at the input and a power matching at the output of the amplifier circuit. A sinusoidal signal V_i having the magnitude of 0.5 V is fed into the input of the HiVP power amplifier. This signal has the frequency of 900 MHz, which is approximately the center frequency of the global system for mobile communication (GSM) uplink band in Europe. The simulated waveforms in the time domain for the output voltage V_o on the load of 50 Ω, as well as for the gate voltages $V_{\rm g}$ and for the drain voltages $V_{\rm d}$ of all the three transistors, are presented in Fig. 4.

The RF output voltage on the load resistance of 50 Ω has a positive amplitude of 14 V and a negative amplitude of -13 V, which generate a distortion. The accomplished output power is approximately 32 dBm, which is also proven by the power-transfer $(P_{\rm out} - P_{\rm in})$ simulation. The lowest value of the $V_{\rm g1}$ is

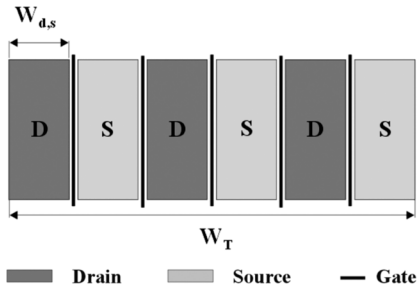

Fig. 5. Conventional layout concept for a single MOSFET.

0.3 V. On the other hand, the peak voltage achieved at the drain of the top device T_3 is approximately 7.8 V. Obviously, $V_{\rm d3}$ is equally divided by the three transistors used in the HiVP structure so that gate–drain–voltage of all the three transistors remain in range of 2.5 V. All transistors operate in a safe operating area.

C. Layout Design

As mentioned above, transistors with a gatewidth of 4.5 mm are employed in the proposed HiVP power amplifier. Therefore, a compact layout for such large transistors is required. On the other hand, the metal lines used in the transistors must be wide enough to sustain the large current. In the ST 0.13-μm CMOS technology, six metal layers are available. To obtain a compact layout for the large transistors, and hence, for the entire HiVP structure, all these metal layers must be used. The lowest metal layer (metal 1) is reserved to connect the ground areas in the layout. Metal 2 is used for the routing of the gates of the transistors. Furthermore, both the drain and source of the transistors are constructed using from metal 3 to metal 6.

The in-practice mostly used layout concept of a MOSFET is shown in Fig. 5. Obviously, the long poly-gate is divided into several fingers; in this manner, significant voltage attenuation on a single long poly-Si line is avoided. Most of the chip area is occupied by the metal lines of the drain and source terminals, which are equally allocated on both sides of the gate fingers. Assuming the transistor has n ($n = 3$ in Fig. 5) pieces of metal lines for the drain and source, respectively, the width of each piece $W_{\rm d,s}$ can be determined by

$$W_{\rm d,s} = \frac{I_{\rm ds}}{n \cdot I'} \tag{3}$$

where $I_{\rm ds}$ is the drain–source current of the transistor and I' (with a unit of microamperes/micrometer) is the current-carrying ability of the metal lines used in the drain and source. The total width of the transistor layout W_T is approximately equal to $2nW_{\rm d,s}$. However, as seen from (3), only $nW_{\rm d,s}$ is actually the effective width, which must be large enough to sustain the current flowing from the drain to the source.

A new layout concept is introduced in Fig. 6 for a single transistor, where the transistor having a gatewidth of 4.5 mm is presented as an example. In this layout, 496 transistor cells are connected in parallel, each of which has a gatewidth of 9.07 μm. They are equally distributed in a 16×31 matrix. Observing the layout, the drain is arranged above and the source is located below. The drain current flows downward to the source and is allocated by all the transistor cells. Therefore, the current flowing

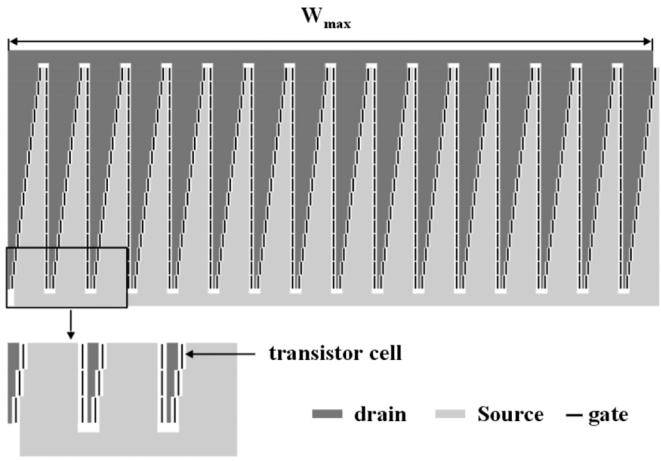

Fig. 6. Novel layout concept for the NMOS transistors.

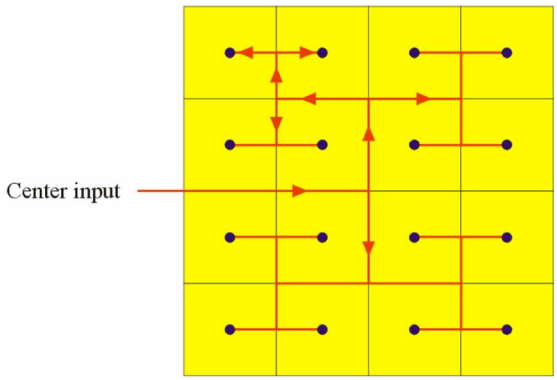

Fig. 7. H-structure.

in the metal line of the drain has the largest value only at the top of the layout and decreases on the way. Oppositely, the source current flowing in the metal line of the source is still relatively small on top, but it increases downwards. The largest value of it exists at the bottom of the layout. Therefore, the largest width of the metal line $W_{\max}$ for the drain is only necessary on the top of the transistor layout, which is reduced top down. On the other side, the linewidth for the source can start at the top with a very small value; however, it increases top down up to the largest width $W_{\max}$ at the bottom of the transistor layout. Obviously, by using such a staggered form, the layout area occupied by the transistor can approximately be reduced by a factor of 2 compared with the layout concept given in Fig. 5.

Another emphasis of the layout design concerns the gate distribution. Assuming the input signal comes from the left of the layout and runs to the right, there is a long distance between the left-most transistor cells and the right-most transistor cells due to the large dimension of the transistor layout. This results in a significant phase difference between the input signals of the transistor cells on the left side and the input signals of the transistor cells on the right side. Therefore, the amplified output signals of these transistor cells partly compensate each other; a degradation of the output power is generated. In order to minimize the phase difference, the so-called H-structure is used, which is illustrated in Fig. 7.

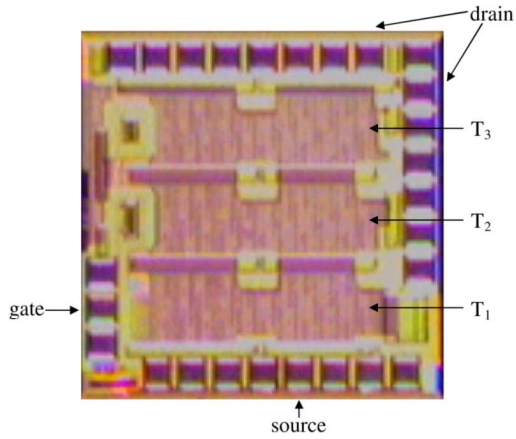

Fig. 8. Micrograph of the fabricated HiVP structure.

In this figure, a chip area is assumed to be divided into 16 parts, which are arranged in a 4×4 square matrix. The small circles in the figure indicate the inputs of every part. Apparently, the center input signal is first fed to the middle of the chip area. It is then routed equally into all the directions. The time delay from the center input to all the part inputs is identical so that no phase difference exits between the input signals of all 16 parts. The decisive factor of using the H-structure is that the entire chip area can be divided into an $n \times n$ square matrix. Since the transistor cells used in Fig. 6 are distributed in a 16×31 matrix (not square matrix), the phase difference between the input signals of the transistor cells cannot totally be deleted. However, using the H-structure, the maximum route difference of the input signals among all the transistor cells is significantly reduced. The degradation of the output power due to the phase difference is negligible.

III. Experiment

The HiVP test chip has been fabricated with ST 0.13-μm CMOS technology. The micrograph of the HiVP chip is shown in Fig. 8. The chip area is 1 mm^2, including the pads.

The HiVP chip has been mounted on a printed circuit board (PCB) on which the input and output matching networks of the HiVP power amplifier are built. The layout of the PCB is shown in Fig. 9. The passive components to be mounted are also indicated in the layout. The inductor L_1 and capacitor C_1 construct the input matching network, while L_2 and C_2 define the output matching network. Several parallel decoupling capacitors C_{b1}–C_{bn} in range of 1 and 100 nF are applied to couple the RF signal of different frequencies to the ground. A large inductor L_d is used as the RF choke at the drain of the HiVP device, and a large capacitor C_3 operates as a coupling capacitor at the output. All these passive components are in the form of surface mount device (SMD) and are soldered on the metal lines. The RF choke for the gate of the HiVP device and the coupling capacitor at the input of the amplifier circuit are included by the bias tee.

Using the bias voltages $V_{\rm gg} = 0.8$ V and the supply voltage of $V_{\rm dd} = 3.6$ V, the output power, power gain, and power-added efficiency (PAE) of the HiVP power amplifier are measured at 900 MHz. The measurement results are illustrated in Fig. 10.

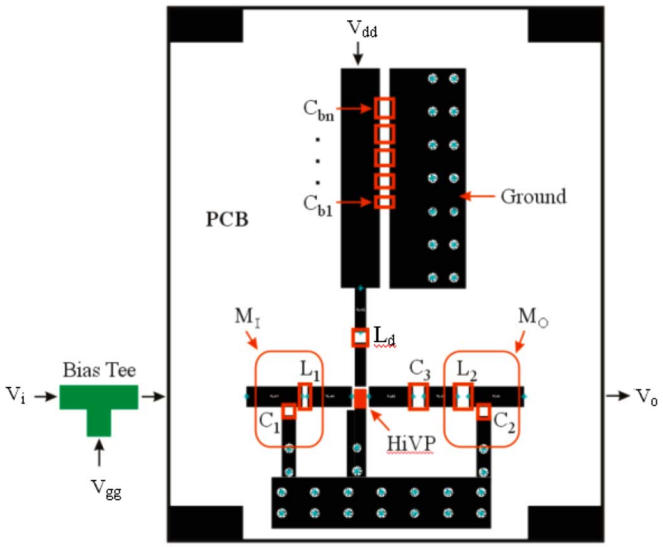

Fig. 9. Layout of the PCB.

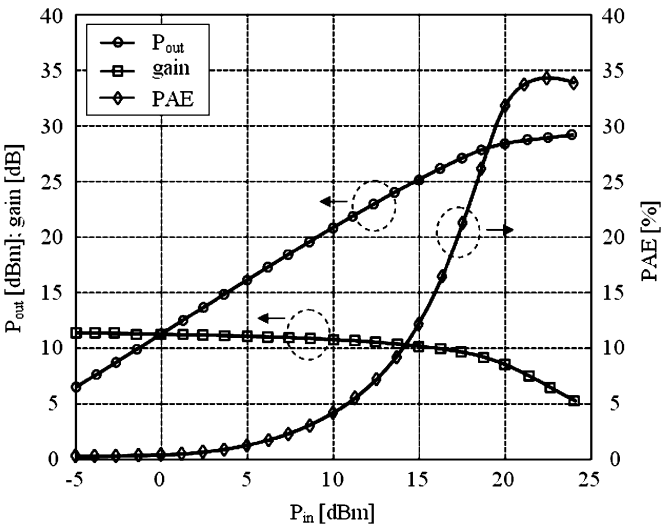

Fig. 10. Measurement results of the HiVP power amplifier.

It can be seen that the maximum output power reaches 29.5 dBm, while the 1-dB compression point is located at 27 dBm. The small-signal gain is approximately 11.5 dB, which is degraded with the increased input power. The maximum PAE of approximately 34.5% has been achieved in the high-output power range.

Obviously, the measured output power is 2.5 dB lower than the simulated result. Larger output power can only be obtained by using even higher supply voltage. In case $V_{\rm dd}$ is equal to 4.9 V, the maximum output power can reach 33 dBm. A comparison has been done between these measurement results and those of other recent studies. The measurement results are listed in Table I. Our results with an advanced CMOS technology fit well into the state-of-the-art.

One of the causes for the power degradation arises from the loss of supply voltage on the parasitic series resistance of $L_{\rm d}$. As the current flowing through the HiVP structure is very large, the power loss in $L_{\rm d}$ can no longer be neglected. The lumped electrical model of an inductor is shown in Fig. 11. It consists of

TABLE I
COMPARISONS OF CMOS POWER AMPLIFIER

Author	Technology [CMOS]	Frequency [GHz]	P_{out} [dBm]	PAE [%]	V_{dd} [V]
Aoki et al. [4]	0.35-µm	2.4	36	41	2
Reyneart et al. [2]	0.18-µm	1.75	27	34	3.3
Sowlati et al. [1]	0.18-µm	2.4	23	42	2.4
Knopik et al. [3]	0.13-µm	2	21	18	2.8
This work	0.13-µm	0.9	29.5	34.5	3.6

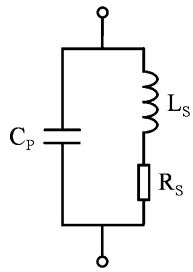

Fig. 11. Lumped electrical model of an inductor.

an inductance L_s with a series resistance R_s and a parasitic capacitance C_p. The series resistance R_s causes the loss of supply voltage leading to reduced output power. It increases with the increased inductance L_s and is approximately proportional to the square root of the frequency [9]. On the other hand, the self-resonance occurs due to the parasitic capacitance C_p. At the resonance frequency, the quality factor of the inductor becomes zero.

In future study, attention must also be paid to the parasitic resistance on the source of the HiVP structure. During the measurement, it is remarkable that the dc current flowing through the HiVP structure is only one-half of the simulated value. It directly causes the degraded output power obtained by the measurement. According to the results of the re-simulations, the reduction of the current mainly arises from the parasitic resistance occurring at the source of the HiVP structure, namely, at the source of T_1. This source resistance comes from the bonding wires, which connect the source pads to the conductor lines of the PCB, and also from the PCB conductor lines themselves. Though several bonding wires are placed in parallel, the parasitic resistance and inductance on them are not significantly reduced due to the proximity effect [9]. Since large current flows through the HiVP structure, and hence, through the source resistor, significant reduction for $V_{\rm gs}$ of all the three transistors can be generated even by a very small value of the source resistance (e.g., 0.4 Ω), resulting in the significant degradation of the output power. Naturally, $V_{\rm gs}$ can again be increased by increasing $V_{\rm gg}$. However, as seen from Fig. 4, larger $V_{\rm gg}$ lowers the maximum swing of V_{d3}; hence, the voltage swing on the load of 50 Ω is also reduced. Furthermore, increased $V_{\rm gs}$ again causes increased current, and hence, increased voltage drop on the source resistance. A balance for the biasing and voltage drop should be found during the measurements.

IV. Conclusion

Using an HiVP configuration, a 0.13-μm CMOS class A power amplifier has been developed with an output power of 29.5 dBm and a maximum PAE of 34.5%. The most important advantage of the HiVP configuration is the subdivision of high output voltage, which solves the problem of low breakdown voltage of the transistors in deep-submicrometer CMOS technologies. It has been shown that with the deep-submicrometer CMOS technologies, power amplifiers for cellular phones can be designed. A monolithic integration of such transceiver systems in a deep-submicrometer CMOS technology is an attractive option to reduce fabrication costs.

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Ingo Dettmann, (S'99–M'07) photograph and biography not available at time of publication.

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