A Single-Chain Multiband Reconfigurable Linear Power Amplifier in SOI CMOS

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Abstract — A multiband linear CMOS power amplifier (PA) is developed to cover multiple LTE bands from 800 to 2000 MHz using a single PA core. The single-chain PA is based on a two-stage design using stacked-FET cells, and is designed to support any combinations of low/high dual bands out of five popular 3G/4G bands (Band 1/2/4/5/8). To avoid the performance degradation by covering such a wide bandwidth using a single PA-core, the frequency reconfigurability has been applied to the stacked-FET cells, interstage matching as well as the output matching. To further enhance the linearity and efficiency, a phase-based linearizer is employed and reconfigured according to the operating frequencies. W-CDMA test on the fabricated PA shows adjacent channel leakage ratios (ACLRs) better than –39 dBc up to the rated linear power of 28.5 dBm and power-added efficiencies (PAEs) higher than 40.7% and 46% for high- and low- frequency band groups, respectively. Compared with the dedicated PAs using the same process, PAE degradation is limited to 1.6 ~ 3.3%. To our knowledge, this work is among the best results from the single-chain PAs for 3G/4G mobile applications.

Index Terms — CMOS, envelope injection, linearization, LTE, multiband, power amplifier (PA), reconfigurable, SOI, stacked-FET, W-CDMA.

I. Introduction

Multiband (MB) power amplifier (PA) is a key component to support the ever-increasing number of 3G/4G frequency bands for global roaming in mobile handsets. Contrary to the dedicated single-band PA for each band, a converged MB PA using either broadband or reconfigurable networks shares a PA-core to reduce the overall size and cost [1]-[6]. Due to the practical bandwidth limit, however, most of the MB converged PAs for the handset applications employ two PA-cores to cover the 3G/4G bands from 800 MHz to 2000 MHz [3]-[6]. A single-chain PA was tried in [2]. However, the PAE was compromised too much (25 ~ 31%) to be used for the power-hungry handset applications. Recently, the reconfigurable matching has been introduced to minimize the efficiency degradation. However, its operating bandwidth has been limited to 0.65 to 1 GHz [7]. In terms of the process technology, there have been continuous studies to improve the linearity and efficiency of watt-level CMOS PAs to take advantage of CMOS process in terms of cost and size [8]-[11].

In this work, a highly efficient single-core CMOS PA has been developed using the reconfigurable circuits not only for the output matching network (OMN) but also for the interstage matching network. The single-chain PA supports any combination of two bands, one from the low-band (LB: 0.8 ~ 0.9 GHz) group and the other from the high-band (HB: 1.7 ~ 2.0 GHz) group. The fabricated PA shows minimal PAE degradation (< 3.3%) compared with the dedicated PA with W-CDMA PAEs in excess of 46% for LB and 40.7% for HB.

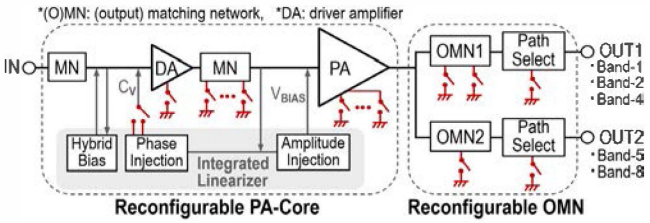

Fig. 1. Block diagram of the proposed multiband reconfigurable linear CMOS PA.

II. Circuit Description

Fig. 1 shows a block diagram of the proposed PA. It consists of a reconfigurable single-chain PA core and a reconfigurable OMN. The PA has two outputs and is designed to support any combinations of one low band and one high band out of five popular 3G/4G bands (Band 1/2/4/5/8), covering uplink UMTS/LTE frequency range of 824 ~ 1980 MHz [1]. Circuit reconfiguration has been achieved by using the silicon-on-insulator (SOI) CMOS switches made out of the same process as the PA core. Also, to improve the linear output power (P_{out}) and PAE, a phase-based linearizer [11] is employed and reconfigured according to the operating frequencies.

The detailed schematic of the proposed PA is shown in Fig. 2. The PA core is based on a two-stage stacked-FET amplifier [8]. The HB output path supports Band-1 as a natural band and can be reconfigured to support Band-2 and Band-4. The LB output path supports Band-8 as a natural band and Band-5 as a reconfigured band. Since only one output port is used at a time, the unused output is deactivated in OMN using the path-selection networks and frequency reconfigurable networks [4].

RF switches are implemented using 0.32-μm 2.5-V NFETs, which show an on-state resistance (R_S) of 0.8 Ω•mm and an off-state capacitance (C_{off}) of 310 fF/mm. The switch design is aimed to minimize the loss due to the reconfiguration. As shown in [4], the loss of the path-selection network is a strong function of R_S and thus large switches (6-stacked NFETs with a 5 mm gate-width; $R_S \approx 1$ Ω) are used for S3 and S4. On the other hand, the frequency reconfiguration switches (S1, S2

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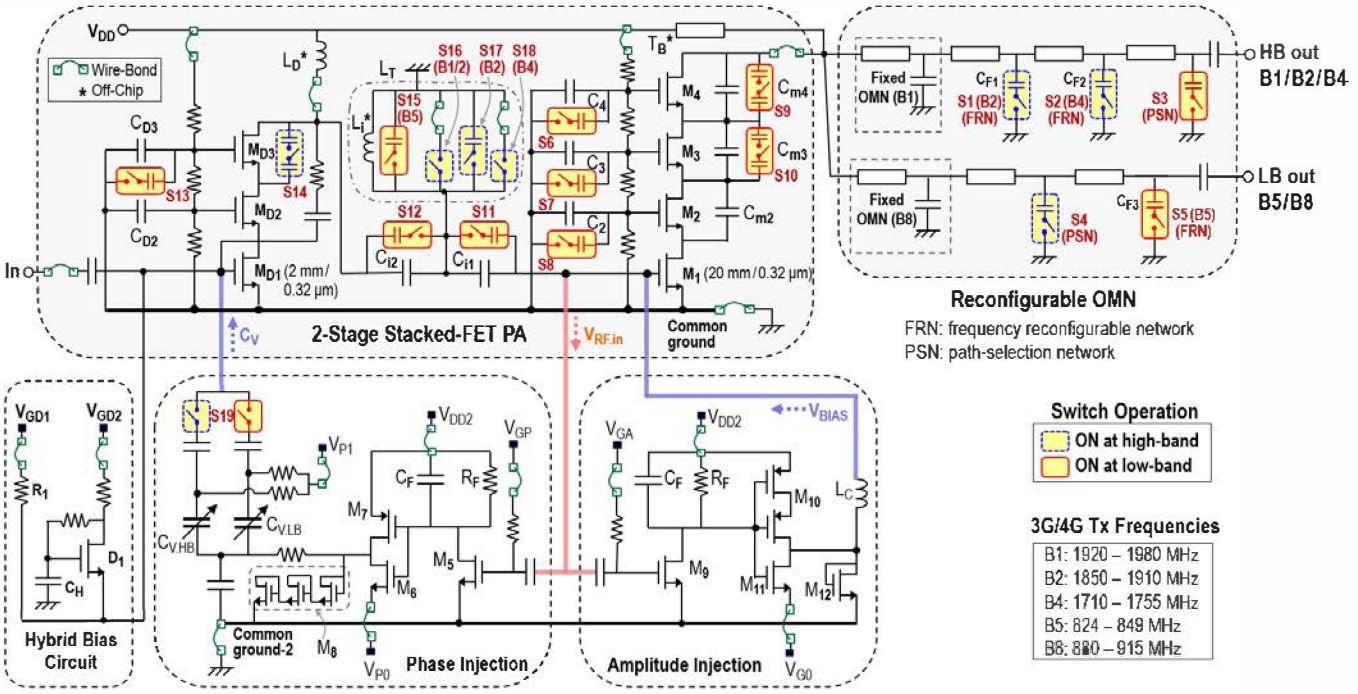

Fig. 2. Detailed schematic of the proposed multiband reconfigurable PA.

and S5 in Fig. 2) have smaller size (6-stacked NFETs with 1 ~ 1.5 mm; $R_S \approx 3.2 \sim 4.8\ \Omega$) since the reactances for frequency reconfigurations (C_{F1}, C_{F2}, and C_{F3} in Fig. 2) are far greater (>90 Ω) than R_S. A single-stack FET can handle a maximum RF voltage swing of 3.3 V and thus a switch cell composed of six FET-stacks shows $P_{0.1dB}$ more than 35 dBm, which is sufficient for 3G/4G handset applications.

In the PA-core, circuit reconfiguration is applied to the interstage network as well as the internal FETs in the stack. The interstage matching is based on a high-pass network consisting of two series capacitors and a shunt inductor. The values of the two series capacitors, C_{i1} and C_{i2} in Fig. 2, are designed for HB operation, and the capacitances are reconfigured by closing S11 and S12 during LB operation. The composite inductance of the shunt inductor, L_T, is reconfigured according to the frequency band of operation. For example, L_T becomes L_i at Band-8 (f_0 = 897.5 MHz) and is reconfigured for Band-5 (836.5 MHz) by turning S15 on. Likewise, S16 is closed during Band-1/2 operation and S17 and S18 are turned on for Band-2 (1880 MHz) and Band-4 (1732.5 MHz) operation, respectively.

To operate the stacked-FET cells at optimum PAE and power points, the individual FETs in the stack need to present the optimum load to the preceding FETs. For this purpose, the external drain-source Miller capacitors (C_{m3} and C_{m4}) and the gate capacitors (C_2, C_3, and C_4) have been reconfigured according to the frequency. Simple stacked-FET theory assumes that constant gate capacitances ($C_2 \sim C_4$) can be used irrespective of the frequency [8]. However, this assumption is no longer valid if the parasitic capacitances cannot be neglected [12]. Since the output-stage FETs ($M_1 \sim M_4$) with a 20 mm gate-width have large parasitic capacitances and the common node of $C_2 \sim C_4$ is RF grounded through a wire-bond, the optimum load impedances of internal FETs change as a function of frequency. To compensate for this, the capacitances in the power-stage stacked-FET cells are increased during LB operation by closing the switches, S6 ~ S10. Similar reconfiguration is also applied to the driver-stage using S13 and S14.

As demonstrated in [11], the linearizer circuits are instrumental in achieving the required W-CDMA/LTE linearity while not compromising the PAE for CMOS PAs. The detailed circuit schematic of the linearizers is shown in Fig. 2. The phase injection circuit provides the envelope-reshaped capacitance (C_V) to the stacked-FET cells to recover the dynamic AM-PM distortion. Since the amount of the required capacitance injection for phase correction is different between HB and LB modes, the switches, S19, select one of the two varactors according to the operating frequency band groups ($C_{V.HB}$: HB, $C_{V.LB}$: LB). On top of the phase injection, the amplitude injection and hybrid bias are also activated during HB operation to further enhance the PA linearity.

III. Fabrication and Measurement

The designed PA was fabricated using an SOI CMOS process and all the MOSFETs have 0.32-μm gate length with an oxide thickness of 5.2 nm. Fig. 3 shows a photograph of the

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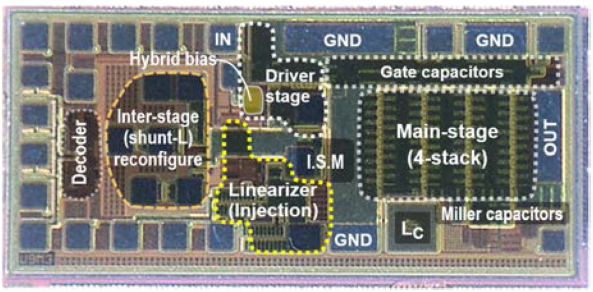
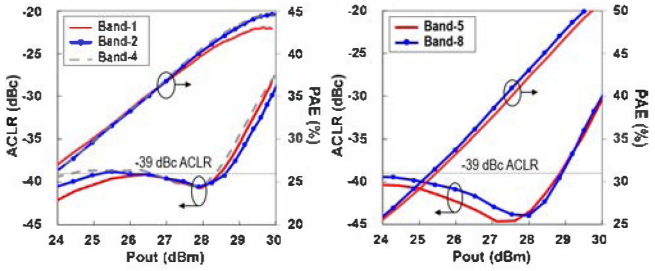
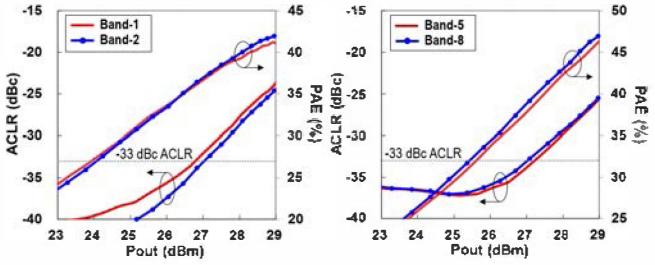


Fig. 3. Photo of the SOI CMOS IC (size = 1.54 mm × 0.68 mm).



(a) (b)

Fig. 4. Measured ACLR and PAE results using a W-CDMA signal: (a) High-band operation. (b) Low-band operation.



(a) (b)

Fig. 5. Measured $ACLR_{E\text{-}UTRA}$ and PAE results using a LTE signal: (a) High-band operation. (b) Low-band operation.

SOI CMOS PA IC. It was mounted on a 400-μm-thick FR4 substrate, where the reconfigurable OMN was realized using the off-chip capacitors and discrete SOI switches for the proof-of-concept experiment. The switches in the PA-core (S6 ~ S19) are controlled by the integrated 3-bit logic decoder.

The PA works with V_{DD} = 4 V and idle current of 92 / 106 mA for HB / LB modes, and 3GPP uplink W-CDMA (Rel'99) signal was used for the initial testing. The measured results are plotted in Fig. 4. In the case of HB operation shown in Fig. 4(a), the PA showed gains higher than 23 dB and adjacent channel leakage ratios (ACLRs) better than –39 dBc up to the rated linear P_{out}'s (~28.5 dBm). The measured PAEs at the maximum linear P_{out}'s (meeting –39 dBc ACLR) were higher than 40.7% for all high bands. In the case of LB shown in Fig. 4(b), the PA showed gains higher than 28 dB and ACLRs of better than –39 dBc up to the rated linear P_{out}'s (~28.8 dBm). PAEs of higher than 46% were measured for all the low bands while meeting –39 dBc ACLR. A separate test turning on and off the linearizer showed that the linear P_{out}'s and PAEs were improved by more than 0.8 dB and 3.5%, respectively, through the use of the linearizer.

LTE performance test was also performed using 10 MHz-bandwidth 16-QAM signal with a peak-to-average power ratio (PAPR) of 7.5 dB, and the results are shown in Fig. 5. The measured PAEs at the rated linear P_{out}'s (~27 dBm) meeting $ACLR_{E\text{-}UTRA}$ = –33 dBc were higher than 35.7% for all the high bands and 38.6% for the low bands. The measured PAEs for each band combination are summarized in Table I.

To estimate the reconfiguration loss of the PA, a single-band reference PA was also fabricated on the same chip using the fixed OMN. The reference PAs for HB / LB showed PAEs of 44 / 48.3% at the rated linear P_{out}'s (meeting W-CDMA ACLRs of –39 dBc). Thus, the PAE degradation due to multi-banding in our work are estimated to be of 1.6 ~ 3.3%, which is attributed to the losses of the switches and output matching.

TABLE I

PAE SUMMARY FOR EACH BAND COMBINATION

Band	PAE (%) at W-CDMA –39 dBc	PAE (%) at LTE –33 dBc
B1 / B5	40.7 / 46.0	35.7 / 38.6
B1 / B8	40.7 / 46.7	35.7 / 38.7
B2 / B5	41.7 / 46.0	36.8 / 38.6
B2 / B8	41.7 / 46.7	36.8 / 38.7
B4 / B5	41.2 / 46.0	36.2 / 38.6
B4 / B8	41.2 / 46.7	36.2 / 38.7

TABLE II

PERFORMANCE COMPARISON OF THE REPORTED MB W-CDMA PAS

Ref	PA (switch) technology	N.out / core[1]	PAE (%)					ACLR (dBc)	OMN
			B1	B2	B4	B5	B8		
[2]	GaAs HBT (FET)	1 / 1	31	26	28	26.5	24.5	–37	Reco-nfig.
[3][2]	pHEMT	8 / 2	40	40.5	40	44	42	–38	Broad band
[4]	GaAs HBT (PIN diode)	2 / 2	39.1	40.7	38.7	43	43.3	–39	Reco-nfig.
[5]	GaAs HBT (0.32 μm SOI)	5 / 2	38	39	37.5	41	41.1	–39	Reco-nfig
[6][3]	CMOS+HBT (HEMT)	4 / 2	35.1	34.5	-	38.5	40.1	–38 ~ –39	Broad band
This work	0.32 μm SOI [W-CDMA]	2 / 1	40.7	41.7	41.2	46.0	46.7	–39	Reco-nfig.
This work	0.32 μm SOI [LTE[4]]	2 / 1	35.7	36.8	36.2	38.6	38.7	–33	Reco-nfig.

[1] Number of the reconfigurable outputs / PA-cores.
[2] It is based on triple stacked-FET structure with separated V_{DD} for each FET, resulting in large load impedance (R_{opt} = 25 ~ 30 Ω).
[3] CMOS and InGaP HBT processes are employed for driver-stage and main-stage amplifiers, respectively.
[4] LTE 10-MHz bandwidth 16-QAM signal with PAPR = 7.5 dB.

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The PAE degradation is much smaller than that from the previous single-chain PA [2]. The performance of recently reported MB linear PAs is compared in Table II. To the best of our knowledge, this is the first demonstration of 3G/4G MB reconfigurable CMOS PA using a single PA-core showing above 40% W-CDMA efficiency while meeting the 3GPP linearity requirements with margin. The performance is comparable or better than GaAs-based counterparts.

IV. Conclusion

A single-chain multiband PA has been developed using the SOI CMOS process to cover multiple LTE bands from 800 MHz to 2000 MHz. To avoid the performance degradation by covering too wide bandwidth using a single PA-core, SOI CMOS switch-based reconfiguration is applied to the stacked transistor cells, interstage matching as well as output matching. As a result, the PAE degradation due to multi-banding is limited to 1.6 ~ 3.3% compared with the dedicated PAs for any dual-band combinations between low- and high- LTE band groups. The proposed PA design can offer significant advantages in terms of the PA module size and cost for 3G/4G mobile applications requiring global roaming.

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