A High-Gain, Two-Stage, X-Band SiGe Power Amplifier

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***Abstract*— SiGe technology is becoming well-known for its capabilities as a high-speed IC design platform, and is being increasingly employed to address a wide variety of communications circuit applications. Unfortunately, the ever-increasing speed of the requisite SiGe transistors comes at a cost that significantly constrains their use in power amplifier design: available breakdown voltage. We demonstrate here that by using an optimized cascode amplifier architecture employing both the high speed (low breakdown voltage) and high breakdown voltage (low speed) SiGe transistors, one can relax these design constraints considerably. Using this approach, a two stage, X-Band amplifier has been fabricated exhibiting maximums of more than 40 dB of stable gain, an output power greater than 20 dBm, and a power-added efficiency of 25% over the X-band operating frequency of 8.5 to 10.5 GHz, and is suitable for emerging X-band phased array radar applications.**

***Index Terms*— SiGe, power amplifiers.**

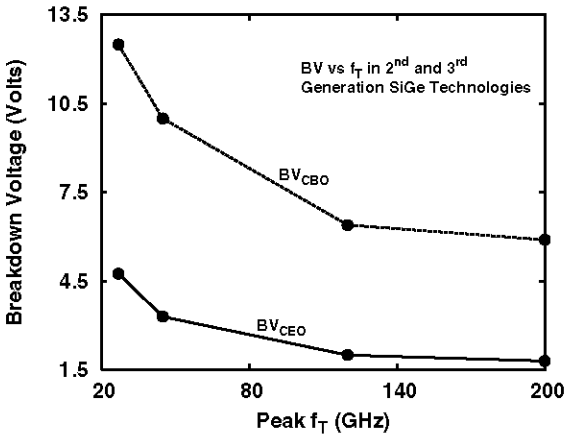

Fig. 1. Collector-Emitter breakdown voltage BV_{CEO} and Collector-Base breakdown voltage BV_{CBO} vs. peak f_T in 2^{nd} and 3^{rd} generation SiGe technologies.

I. Introduction

The performance of SiGe transistors continue rise to impressive levels while maintaining strict compatibility with silicon IC manufacturing, with reported peak cutoff frequencies (f_T) above 350 GHz [1]. This increase in speed comes, however, at the cost of decreasing breakdown voltage, as can be seen in Figure 1. While this contraction in breakdown voltage with scaling does not present a large problem for small-signal circuits such as Low Noise Amplifiers (LNAs), it represents a fundamental design constraint for Power Amplifiers (PAs), ubiquitous in all wireless transceiver systems, regardless of the operating frequency.

Increased voltage swing in SiGe amplifiers has been demonstrated by using Common-Base (CB) rather than Common-Emitter (CE) topologies [2]. Combining these two amplifier types in a cascode amplifier configuration allows for separation of the gain and output drive between the two transistors used in the amplifier. It has been shown [3] that a hybrid use of a High-Speed (HS) (high f_T, low BV_{CEO}) and High-Breakdown (HB) (low f_T, high BV_{CEO}) SiGe transistors in the cascode topology allows for optimal design for both gain and voltage swing in SiGe PAs.

In the present work, such a HB/HS cascode is used to demonstrate a high gain, two stage power amplifier in a third-generation SiGe technology. Through the use of on chip biasing and matching, the amplifier is well-matched to 50 Ω input and output impedances, exhibits greater than 20 dBm of output power, 25% power-added efficiency (PAE) and 40 dB of stable power gain from 8.5 to 10.5 GHz (X-Band).

II. Breakdown Voltage in SiGe Devices

It is commonly accepted that low breakdown voltage transistor technologies are incompatible with efficient power amplifier design. Power amplifiers, unlike small-signal amplifiers such as LNAs, are not conjugately matched on their outputs, but instead are intentionally mismatched to drive a given output power. The optimal output power for a given power amplifier is derived from its maximum deliverable voltage and current, which also sets the load for the amplifier [4]. Consequently, the output load resistance of a power amplifier is related to the maximum breakdown voltage of its requisite transistors and the desired deliverable power by the well-known relation, $R = V^2/P$. Thus, the load line value for an amplifier increases as the square of the available breakdown voltage of the requisite transistors. The increased load match allows for decreased losses in the matching circuitry, improving gain, output power, and importantly, efficiency [5].

While a common-emitter configured high-breakdown SiGe transistor in a 200 GHz technology exhibits a breakdown voltage of a little over 3 Volts, as seen in Figure 2, the same transistor, when configured in a common-base configuration, exhibits a breakdown voltage of nearly 8 Volts, as shown in Figure 3. This phenomenon is achieved through the physical mechanism of base current reversal [6]. As opposed to current flowing into the base of the common-base transistor, as is generally the case, at higher collector voltages, current actually flows out of the base, since it looks like a low impedance at DC. The base current reversal is explicitly shown in Figure

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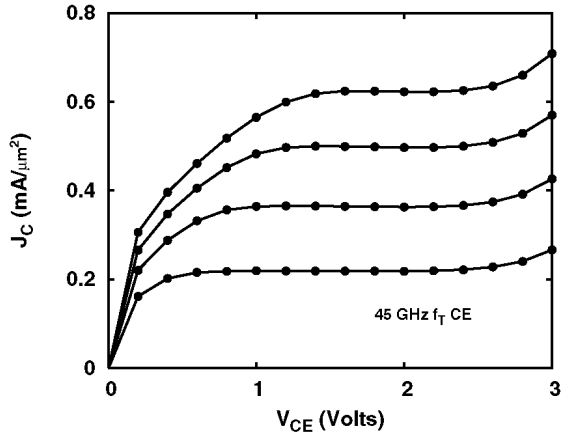

Fig. 2. Output characteristics for a 45 GHz peak f_T high-breakdown device in a common-emitter bias configuration.

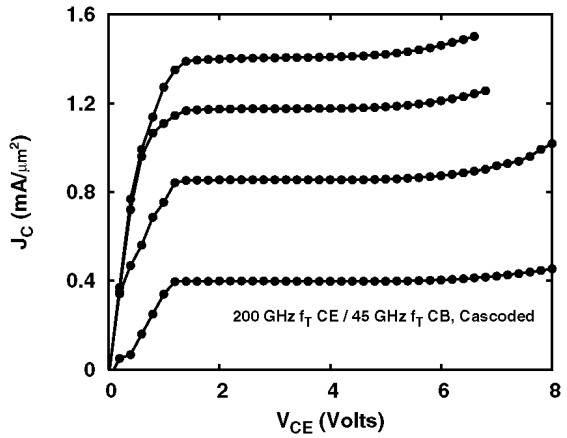

Fig. 3. Output characteristics of a 200 GHz peak f_T high-speed device cascoded with a 45 GHz peak f_T high-breakdown device, showing the increased breakdown voltage achievable in the cascode configuration.

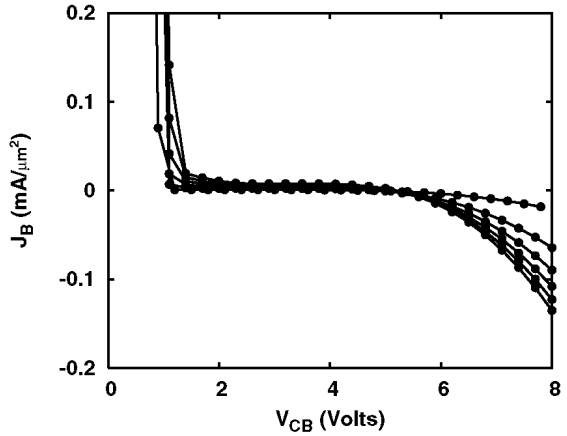

Fig. 4. Base current flow in the high-breakdown, common base configured transistor of a cascode configuration, as a function of collector voltage.

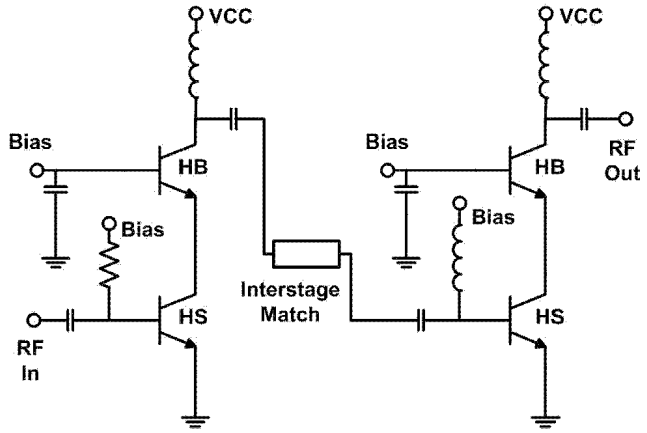

Fig. 5. Schematic of the two-stage hybrid cascode power amplifier showing use of high-breakdown (HB) and high-speed (HS) SiGe transistors.

4. It is serendipitous that the bias point for the amplifier configuration occurs at a collector voltage below where the current reversal occurs. Thus, the bias circuitry need not sink any current, simplifying its design. It is necessary, however, that ample capacitance be placed on the base of the high-breakdown device to provide the necessary current under RF drive conditions. This also coincides with the condition that the base look like an RF ground, which is necessary to achieve the desired power gain and remain stable during operation.

III. The Hybrid Cascode Topology

The cascode architecture incorporates the use of two transistors in two different modes of operation (one in common-emitter mode and one in common-base mode) to exploit certain desirable characteristics of each respective amplifier topology. As can be seen in Figure 5, the lower device, labeled HS, operates in a common-emitter configuration, while the upper device, labeled HB, operates in a common-base configuration. It is well-known that the cascode architecture acts to mitigate the Miller effect, and in doing so, acts to increase the bandwidth of operation of the common-base configured device [7]. In addition, this architecture also allows for an effective separation of gain and output drive voltage, which can be particularly exploited to our advantage in SiGe technology. The common-base configuration allows for an increase in the available breakdown voltage of the device through base current reversal. The gain for the configuration is derived from the lower device. Thus, the use of a high-speed device for the gain stage and a high-breakdown device for the output stage, can be exploited to optimize SiGe PAs across a wide range of operating frequencies [3].

IV. Power Amplifier Design

The power amplifier was implemented in a commercially-available 200 GHz SiGe process technology. The first stage is made up of a single HS/HB pair of devices that are available in the design kit. The devices were sized such that, at optimal bias, each device operates near its peak f_T current. The ratio of peak f_T on J_C in this technology between the available high-speed and high-breakdown devices is nearly 8-to-1, making the emitter area of the HB device 8 times that of the HS device.

Using the maximum emitter geometry available of this particular SiGe technology would have required nearly 40

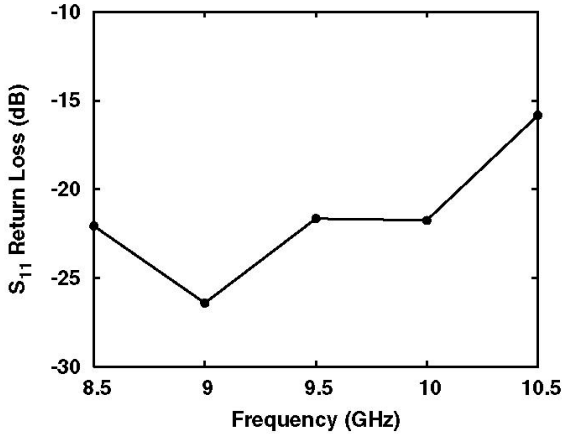

Fig. 6. Measured S_{11} performance of the two-stage SiGe amplifier.

HB devices hooked in parallel to meet the targeted output power for the second stage amplifier. This was deemed an unattractive choice from a real estate perspective, as well as adding unwanted interconnection parasitics. Consequently, a larger device with 5 times the area of the largest available HB device was designed and modeled for use in the second stage. Eight HS/HB pairs were then used to achieve the desired output power.

To match to the relatively small input impedance of the second stage, on-chip microstrip transmission lines fabricated in the top two thick (Al) metals available in the technology were employed. This was done out of necessity of a series inductive element for the match of this PA. Space requirements prohibited the use of available on-chip spiral inductors. The incorporation of both foundry provided models and EM modeling of corner joints and T-junctions was used to obtain the series contribution of the meandered transmission line for fine-tuning the interstage match.

Large banks of lumped, on-chip MIM (metal-insulator-metal) capacitors, on the order of 10 pF, were used at the base of the common-base transistor in each stage. Connections between the transistors and the capacitors were kept as short as possible to minimize series resistance and inductance.

The designed operational frequency of the amplifier was 8.5 to 10.5 GHz to support the intended X-band radar application. Both input and output ports were matched to 50 Ω using available on-chip passives. An input bias resistor was used on the first stage to save space over the use of an inductor and to also improve the broadband S_{11} performance. Post-extraction simulation results showed a worst case 41 dB of gain with an output power of 20.4 dBm across band, with a PAE of 31%.

V. Measured Results

The fabricated amplifier exhibited excellent input matching to 50 Ω across the entire operating frequency, as can be seen in Figure 6. The output power match for the second stage was also well-matched across the band to the 50 Ω system impedance, as shown by the 1 dB power contours in Figure 7 and the 3% PAE contours of Figure 8.

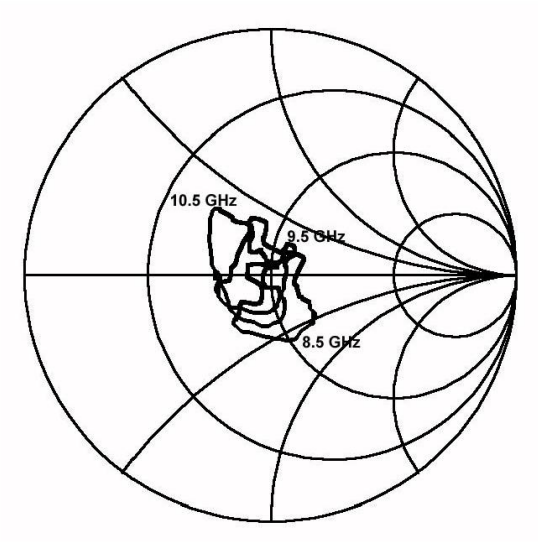

Fig. 7. 1 dB power contours at low, mid, and high frequency points showing excellent match to 50 Ω.

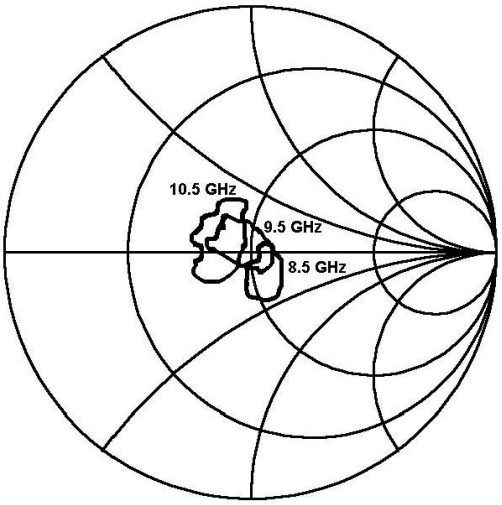

Fig. 8. 3% PAE contours at low, mid, and high frequency points.

TABLE I
X-Band Multi-Stage Amplifiers

Substrate	Stages	Gain (dB)	PAE (%)	Pout (dBm)	Reference
GaAs	2	17	-	17	[8]
GaAs	3	16	-	26	[9]
GaAs	2	18	25	36	[10]
GaAs	2	19	40	37	[8]
GaAs	2	16	40	37	[11]
SiGe	2	21	40	25	[12]
SiGe	2	41	26	21.4	This Work

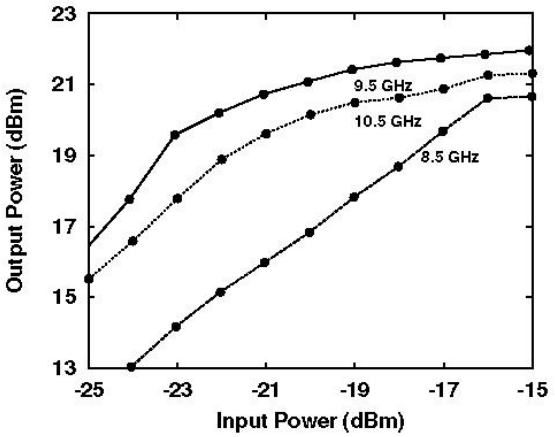

Fig. 9. Output power as a function of input power.

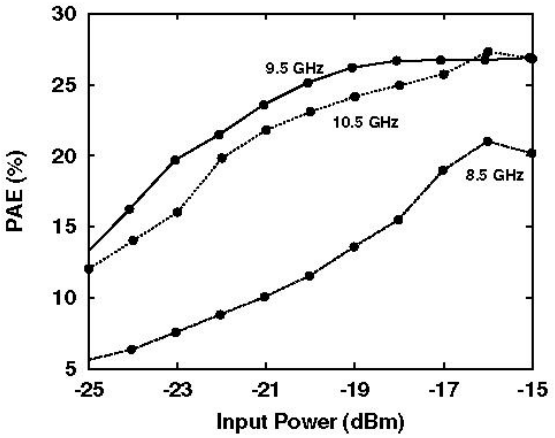

Fig. 10. Power Added Efficiency as a function of input power at low, mid, and high frequencies.

The input and output matching contribute directly to the measured output power meeting (and exceeding) the simulated performance at mid and high frequencies in the band of operation, as shown in Figure 9. The interstage match was slightly off in frequency, which accounts for a lack of drive power to the second stage at lower output power and PAE at the low end of the band, but this can be easily adjusted.

A summary of X-Band multistage amplifiers is shown in Table I. To achieve similar gain to this work, all of the other amplifiers would require at least two more stages. These would be significantly more difficult to design, take more die space, and be more susceptible to instability and loss of efficiency, which often result when using more interstage matches.

VI. Summary

SiGe continues to show that it is a viable contender for many microwave circuit applications. An optimal use of hybrid high-breakdown and high-speed devices available in SiGe technologies, when combined in the cascode topology, can provide excellent gain and high voltage swing (efficiency) for SiGe power amplifiers. A fabricated two-stage SiGe power amplifier exhibits greater than 40 dB of gain with an output

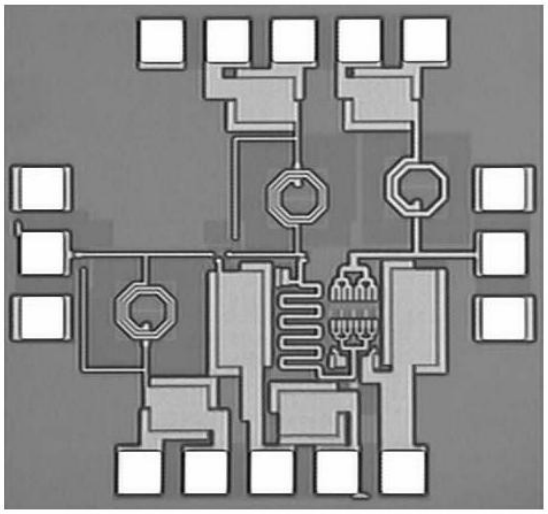

Fig. 11. Die photo of the two-stage SiGe amplifier, measuring 1.1 mm x 1.2 mm in area, including pads. Some of the discernible features include the on-chip spiral inductor feeds, large banks of MIM capacitors, and microstrip transmission line matching elements.

power of greater than 20 dBm and a PAE of greater than 25% at X-Band. Use of the hybrid breakdown cascode topology in SiGe is demonstrated to be a powerful technique for reducing the number of amplifier stages needed to obtain the desired overall gain, while simultaneously improving matching through increased breakdown voltage.

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