A Wideband Envelope-Tracking CMOS Linear Transmitter without Digital Predistortion

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***Abstract*— In this work, an effective linearization technique to linearize both AM-PM and AM-AM distortions in CMOS envelope tracking (ET) transmitter is developed using dual shaping tables. AM-AM response is linearized using iso-gain shaping table. A variable phase shifter is integrated with the RF power amplifier (RF PA), which linearizes AM-PM response of CMOS ET PA in conjunction with the iso-gain shaping table. In this way, no additional digital predistortion (DPD) is required to linearize the CMOS ET PA. The 2-stage RF PA with the integrated phase compensation circuit is fabricated in 0.28-µm SOI CMOS process. The ET transmitter system demonstrated using the CMOS envelope amplifier (EA) shows an overall system PAE of 42.2% with –34.5 dBc E-UTRA ACLR with 40 MHz BW LTE signal centered at 0.837 GHz. The proposed method overcomes the bandwidth limitation of the conventional methods relying on DPD and/or feedback loops, and can be applied to wide bandwidth LTE signals.**

***Index Terms* — AM-PM, CMOS, DPD, envelope tracking (ET), linearity, LTE, power amplifier (PA), wideband.**

I. Introduction

Envelope tracking (ET) is a very effective method to enhance the overall efficiency of the linear transmitter handling LTE signals with a large peak-to-average power ratio (PAPR) ([1]-[6]). GaAs HBT ET PAs driven by the CMOS envelope amplifier (EA) have demonstrated high system PAEs with good linearity ([1]-[2]). Even though CMOS RF PAs have also been developed for ET operation, showing comparable efficiency to the GaAs counterparts, the linearity is often compromised ([3]-[4]). This is mainly attributed to the relatively large knee voltage of the CMOS device; large phase distortion occurs when the dynamic drain bias enters the knee region during ET operation. The FET stacking, often employed in CMOS PAs to overcome the low breakdown limit, aggravates the phase distortion problems due to the contracted headroom.

Digital predistortion (DPD) is widely used to linearize ET-based transmitter system. However, DPD poses several system-level issues when the signal bandwidth increases above 20 MHz. First of all, high-speed DPD is required to handle wideband signals, which increases the power consumption due to high-speed signal processing. The other issue is the excessive signal spreading after DPD. For example, Fig. 1 (a) shows the simulated

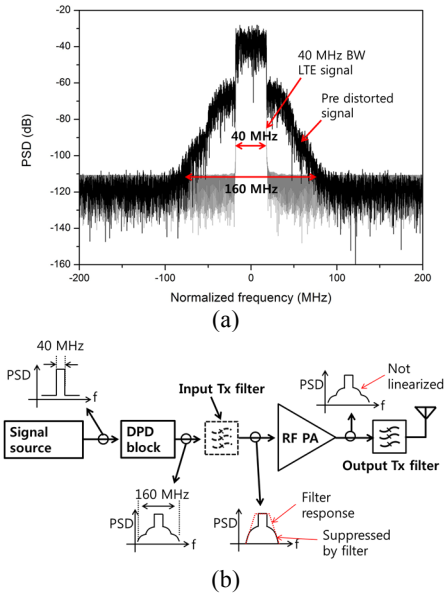

Fig. 1. (a) Simulated spectrum of the predistorted input signal when the original input signal has 40 MHz BW. (b) Simplified block diagram of the transmitter, showing the issues with DPD.

frequency spectrum of 40 MHz BW LTE signal before and after DPD. The bandwidth expands to as much as 160 MHz, 4 times the original signal bandwidth. The subsequent PA should have flat gain response across the entire spreading bandwidth to recover the linearity. Also, the signal spreading prevents the use of the Tx filters in front of the PAs as shown in the Fig. 1 (b), which may be required for a certain LTE bands to solve the out-of-band emission issues. Furthermore, unwanted Rx sensitivity degradation can occur if the spectrum spreading extends into the Rx-band and the spread Tx signal couples to the signal receive path. To avoid the potential issues due to wideband DPD, it will be beneficial to develop a linear ET transmitter without relying on DPD for linearization.

In this work, a self-linearizing CMOS ET PA is developed to demonstrate a 40 MHz LTE transmitter without DPD-based linearization. Many linearization techniques have been investigated for CMOS ET PA, including dynamic gate bias control [5] and dynamic feedback [6]. However, most of these works have focused on gain flattening rather than phase linearization, and the signal bandwidth for linearization has been limited to 10

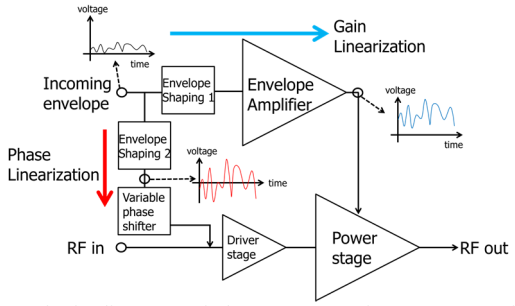

Fig. 2. Block diagram of the ET transmitter system with the proposed phase linearizer.

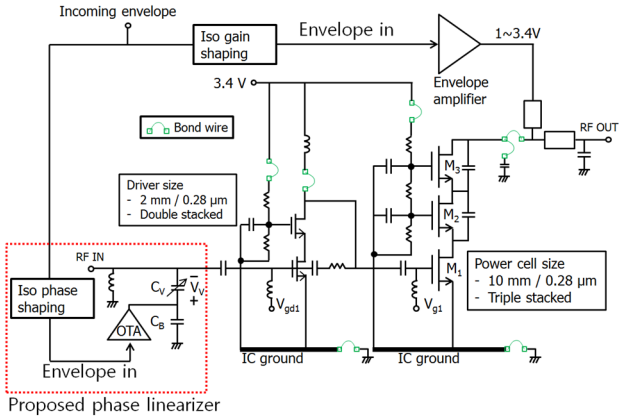

Fig. 3. Detailed circuit schematic of the 2-stage CMOS RF PA with the proposed phase linearizer.

MHz. In this work, dual shaping tables are employed during ET operation to linearize both gain and phase response of the CMOS ET PA. Since the proposed linearization method does not rely on the band-limited feedback loop, it can be applied to wideband signals with minimal degradation in the linearity.

II. Circuit Design

The block diagram of the proposed ET transmitter system is shown in Fig. 2. It consists of a 2-stage RF PA with a center frequency of 0.837 GHz, an envelope amplifier (EA), two shaping table blocks and a variable phase shifter. RF PA and a variable phase shifter are fabricated using 0.28-μm SOI CMOS process and integrated on a single chip with a size of 1.27 mm × 0.64 mm. The EA used in this work is the same one developed in our previous works ([3]-[4]), which is fabricated with 0.32-μm SOI CMOS in a separate chip. The envelope information is fed to the "Envelope Shaping 1" block to flatten the dynamic ET gain. For this purpose, iso-gain calibration is performed to find the optimum gain shaping table between the envelope voltage and the input voltage to the envelope amplifier. The same envelope information is fed to the second block called "Envelope Shaping 2" block, which generates the controlled input voltage to the

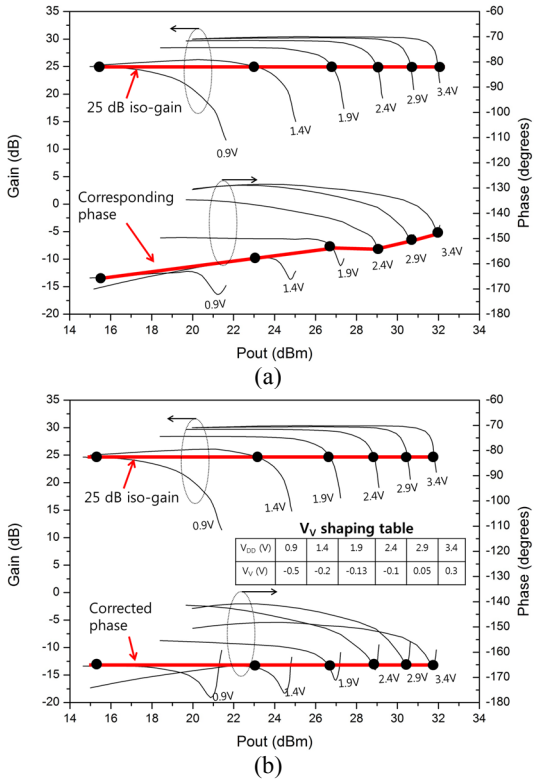

Fig. 4. Simulated gain and phase of the 2-stage RF PA when the drain bias of the power stage is swept from 3.4 V to 0.9 V with 0.5 V steps. (a) before phase compensation, (b) after phase compensation.

variable phase shifter so that the overall phase response of the ET PA can be linear. For this, another calibration step is performed before PA operation to find the optimum phase shaping table between the envelope voltage and the input voltage to the phase shifter.

The detailed circuit schematic of the 2-stage RF PA with the phase linearizer is shown in the Fig. 3. The power cell is a triple-stack FET with a unit transistor size of 10 mm while the driver stage is a double-stack FET with a size of 2 mm. The drain bias of the driver stage is connected to a fixed bias of 3.4 V while that of the power stage is supplied by the EA. Output matching is realized off chip on a 400-μm-thick 2-layer FR4 PCB (ε_r=4.6, tanδ=0.025).

The phase linearizer is added at the input of the RF PA for on-chip AM-PM correction. The phase linearizer consists of an iso-phase shaping block, a varactor (C_V), a RF bypass capacitor (C_B), and an operational trans-conductance amplifier (OTA). The OTA design is based on the folded cascode input stage to extend the input common range, and the push-pull common-source output stage to drive highly capacitive load, a parallel combination of C_B and C_V, without distortion. The output voltage from the OTA (V_V) controls the capacitance of the

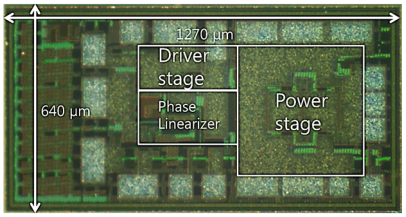

Fig. 5. Chip photograph of the 2-stage RF PA.

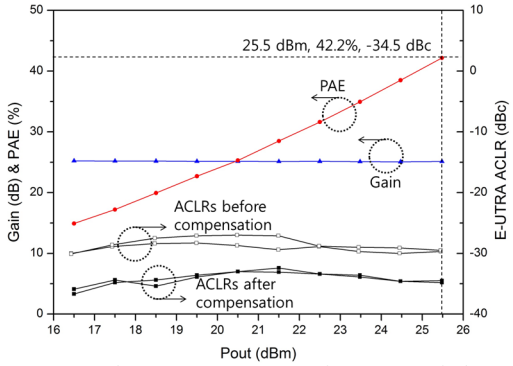

Fig. 6. Measured 40 MHz LTE performance of the ET PA system with the proposed phase linearizer.

varactor (C_V) so that the phase predistortion can be introduced to the RF signal path across the PA. During the iso-phase calibration, the voltage shaping table is generated to map the envelope voltage to the phase shifter input voltage so that the overall AM-PM characteristics of the RF PA can be made linear.

Fig. 4 shows the simulated gain and phase of the 2-stage RF PA when the drain bias of the power stage is swept from 0.9 to 3.4 V in 0.5 V steps. During the iso-gain calibration, the envelope voltage is mapped to the dynamic V_{DD} to achieve flat gain response. In our work, a flat gain of 25 dB is chosen considering V_{DD} range and system gain requirement. However, as shown in Fig. 4 (a), iso-gain V_{DD} mapping results in large distortion in AM-PM response (~20°). This is recovered by applying the additional mapping between V_{DD} and V_V, as shown in Fig. 4 (b). The applied V_V boosts the phase delay at high V_{DD}'s to achieve flat AM-PM response. In summary, both gain and phase distortions in CMOS ET PAs are fully recovered through two layers of voltage mapping using dual shaping tables.

III. Measurement Results

Fig. 5 shows the photograph of the fabricated RF PA chip with the on-chip phase linearizer. CW testing shows that the 2-stage RF PA delivers a maximum PAE of 63% at 30.5 dBm output power at a drain bias of 3.4 V. Wideband LTE test is performed at 837 MHz using 40 MHz BW QPSK LTE signal with a PAPR of 6.7 dB. Since the LTE signals wider than 20 MHz were not

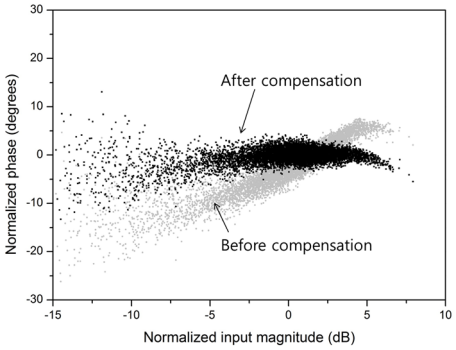

Fig. 7. Measured dynamic AM-PM of the ET PA at 25.5 dBm with 40 MHz BW LTE signal.

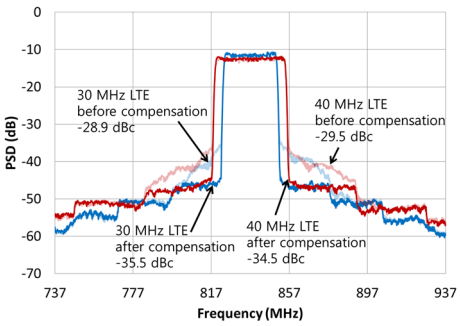

Fig. 8. Measured output spectrum of the ET PA using 30/40 MHz BW LTE signals with and without phase compensation (P_{out}=25.5 dBm).

readily available in our lab, 40 MHz BW compatible LTE signals was constructed by increasing the sampling rate of the fully loaded 20 MHz LTE signal [2]. Timing alignment between the two envelope paths and the RF path is adjusted using Keysight 33622A arbitrary waveform generator. After the delay alignment, two shaping tables are constructed through iso-gain and iso-phase calibration steps.

Fig. 6 shows the measured gain, PAE and ACLR of the CMOS ET PA with 40 MHz BW LTE signal. The linear output power reaches 25.5 dBm with a flat gain of 25.1 dB. The overall system PAE is 42.2% at 25.5 dBm, which includes the efficiency of the EA (~75% for 40 MHz operation) and the current consumption in the phase linearizer (~ 2 mA). Without ET operation, the same RF PA showed a PAE of 33.3% with a fixed drain bias of 3.4 V. So, the PAE boost by ET operation is as much as 8.9%. Fig. 6 also compares ACLR before and after phase linearization. Without phase linearization, the measured E-UTRA ACLR is only –29.5 dBc at 25.5 dBm even if iso-gain shaping is applied. E-UTRA ACLR is restored to –34.5 dBc by turning on the proposed phase compensation circuit.

To clearly show the effect of the proposed linearizer, we have measured the dynamic AM-PM with 40 MHz

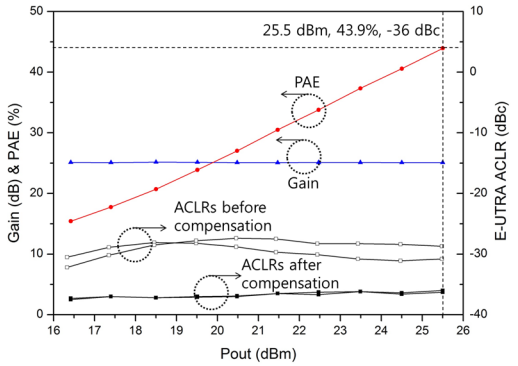

Fig. 9. Measured 20 MHz LTE performance of the ET PA system with the proposed phase linearizer.

BW LTE signal with and without phase linearization. As shown in Fig. 7, large phase distortion up to 25° has been corrected to less than 4° by applying phase compensation. The measured output spectrum of the CMOS ET PA is also compared in Fig. 8 with and without phase compensation for 30 MHz and 40 MHz BW LTE signals. The proposed linearizer improves ACLR by 6.6, and 5 dB for 30, and 40 MHz BW LTE signals respectively.

To benchmark the ET PA performance, 20 MHz LTE test is also performed, and the results are shown in Fig. 9. The overall system PAE reaches 43.9% at 25.5 dBm output power. With the phase compensation, the measured E-UTRA ACLR is –36 dBc while EVM is 2.32%. Slightly better linearity for 20 MHz operation is attributed to the reduced memory effect in the EA.

Table I summarizes the measured results of our work for 10/20/30/40 MHz BW signals and compares them with the state-of-the-art ET PAs published to date. To the best of our knowledge, this is the first demonstration of a linear CMOS ET PA to cover 40 MHz LTE bandwidth. Compared with other works for 10/20/30 MHz LTE, our CMOS ET PA without DPD shows ACLRs and PAEs comparable to GaAs HBT ET PAs.

IV. Conclusion

In this work, a linear CMOS ET transmitter is demonstrated to cover 40 MHz LTE signals without relying on digital predistortion. The 2-stage RF PA includes the variable phase shifter at the input, which linearizes AM-PM response in conjunction with the iso-phase shaping table. Together with iso-gain shaping table, the transmitter shows E-UTRA ACLRs better than –34.5 dBc for LTE signal bandwidths up to 40 MHz. Overall system PAEs higher than 42% is achieved up to 40 MHz bandwidth. This work presents a dual-shaping-table-based linearization method that overcomes the bandwidth limitation of the conventional methods relying on DPD and/or feedback loops. Hence, the proposed method has the potential to cover even wider bandwidth LTE signals.

TABLE I

Comparison of the ET PA systems for Mobile LTE Terminals

Ref.	PA Tech.	Freq. (GHz)	BW (MHz)	PAPR (dB)	P_{out} (dBm)	PAE (%)	ACLR (dBc)	Gain (dB)	Output matching
[1]	GaAs HBT	2.535	20	6.6	29	43	1.9%[1]	28.5	Off chip
[2]	GaAs HBT	1.74	10	6.9	27	40	–34.4	30.1	Off chip
			20	6.9	27	39.4	–33.9	29.9	
			30	6.9	27	38.5	–33.4	29.8	
[5]	0.18-µm CMOS	1.9	5	7.5	23.5	28	–32.5	N/A	On chip
[6]	0.18-µm CMOS	1.85	10	7.5	26.5	37.6	–36.8	~13	On chip
This work	0.28-µm SOI CMOS	0.837	10	6.7	25.5	44.7	–36.9 1.94%[1]	25.1	Off chip
			20	6.7	25.5	43.9	–36 2.32%[1]	25.1	
			30	6.7	25.5	43.2	–35.5	25.1	
			40	6.7	25.5	42.2	–34.5	25.1	

[1]: EVM

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