Quasi Inverse Class-F X-Band Highly Efficient Power Amplifier with 51.8% Peak PAE in SiGe

S. Redois[1,2], E. Kerhervé[1], A. Ghiotto[1], B. Louis[2], V. Petit[2], Y. Mancuso[2]

[1] IMS Lab, University of Bordeaux, France

[2] Thales DMS, Elancourt, France

samuel.redois@ims-bordeaux.fr

***Abstract* — This paper presents a compact quasi inverse class-F highly efficient power amplifier (PA) based on the 130 nm SiGe technology. The purpose is to drive high output power with high power added efficiency (PAE) over the X-band, while ensuring a good amplitude and phase linearity. To do that, a differential cascode topology with low base impedance has been used. Measured results exhibit 51.8% peak PAE with 25.7 dBm output power at 9 GHz. To our knowledge, this PA demonstrates the highest efficiency with linear behaviour among Si-based X-band power amplifiers found in literature.**

***Keywords* —BV_{CB0}, BV_{CE0}, high efficiency, inverse class-F, linearity, power amplifier.**

I. Introduction

In recent years, the rapid scaling in Si-based transistors have allowed to develop fully integrated SiGe BiCMOS transceiver RADAR modules [1]. Their low cost, high integration and high transition frequency *ft,* make them an alternative to higher cost III-V components.

However, in Si-based PAs, it is difficult to drive high RF power with high efficiency due to the low breakdown voltages. In a T/R RADAR module, an output power over one Watt is generally required.

In order to achieve the Watt level output power, several techniques have been explored. First of all, harmonic tuned PAs like inverse class-F based on 2nd / 3rd harmonic matching network have been proposed [2], [3]. They can achieve sub-watt level output power with high efficiency. However, multi-harmonic resonant filters are needed, ensuring a low compactness. Moreover, these PAs show a low linearity.

Then, stacking transistors in series has been proposed [4]. The output power is combined thanks to a Wilkinson power combiner. However, the efficiency is low, leading to high heat dissipation. In addition, the X-band Wilkinson power combiner has very low capability of integration, which implies large silicon area.

Finally, class-J PAs have been designed to reduce AM-PM distortion [5] with Bessel bandpass filter implemented to reduce sensitivity to the transistor input capacitance. This topology shows a good AM-PM linearity but is not able to achieve high RF output power together with high efficiency.

The proposed paper presents a linear highly efficient quasi inverse class-F power amplifier. The main challenge is to drive high output power with high efficiency, while maintaining the linear behaviour. The PA is based on parallel cascode topology shown in Fig. 1. Common base stage uses a low base impedance termination to overcome the breakdown voltage limitations. The PA is implemented in the low cost BiCMOS9MW technology from STMicroelectronics. The measured results show 51.8% peak PAE with 25.7 dBm output power at 9 GHz. The measured 1 dB power gain bandwidth (BW) extends from 7.7 GHz to 10.4 GHz. The measured AM-PM distortion is lower than 5° and 10° below 22 dBm and 24 dBm output power, respectively. To the authors' best knowledge, the proposed PA provides the highest efficiency with high output power and a linear behaviour in SiGe-based PAs.

II. Quasi Inverse Class-F Power Amplifier

The proposed X-band power amplifier schematic is given in Fig. 1. The structure is based on a differential cascode topology.

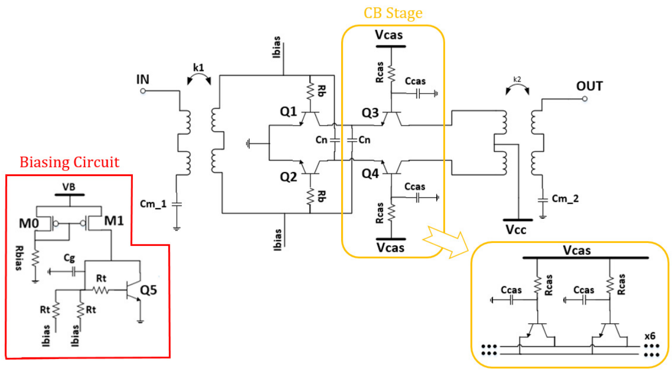

Fig. 1. Schematic of the quasi inverse class-F power amplifier.

Two baluns are used to present the optimum input and output impedances to common emitter (CE) and common base (CB) stage, respectively. The optimum impedance seen at collectors of CB stage is equal to 18Ω+j28 Ω at 9.5GHz. *Cm_1* and *Cm_2* capacitances allow to balance the transformers asymmetry [6]. Therefore, the common mode rejection ration (CMRR) of the PA is improved.

Q1 and Q2 common-emitter transistors are made from 2 parallel HBTs. Each HBT has 5 emitter fingers with length of 10.5 µm. The *Rb* resistor of 5 Ω is used to stabilize the PA.

The CE stage is biased in AB-class thanks to an integrated active bias which provides a collector current equal to 6.5 mA. Two current mirrors have been used to ensure a good reliability in case of high output power. The first current mirror stage is based on the PMOS mirror composed of M0 and M1:

- M0 consists of 2 fingers of 30 µm width,
- M1 is built with 28 fingers of 420 µm width.

Therefore, the PMOS mirror ratio is equal to 24. The bias current is adjusted thanks to the *Rbias* resistor. The second mirror stage is composed of the Q5 HBT transistor with a current ratio equal to 1. Therefore, the quiescent DC current of the CE biasing is set to 13 mA. The *Rt* base resistors are 200 Ω. The *Cg* capacitor is used to filter the RF leakage. The bias voltage *Vb* is set to 1.2 V.

Two neutrodyne MIM capacitances, *Cn*, have been used to stabilize the PA. Indeed, a large base-collector capacitance, *Cbc*, reduces the PA isolation and could lead to a potential instability. The *Cn* capacitances allow to minimize *Cbc* by introducing a parallel 180° phase shifted capacitance. Therefore, isolation, gain and stability are increased.

The common base stage (CB) consisting of the Q3 and Q4 transistors, is composed of 6 parallel HBTs. Each HBT is built with 3 emitter fingers with 15 µm width. The CB base impedance termination is crucial for PA reliability. According to [2], the CB electrical schematic is exhibited in Fig. 1. *Ccas* are 1pF MIM capacitances. These low resistance capacitances allow to bypass excessive holes generated by impact ionization. The cascode voltage *Vcas* is set to 1.8 V.

III. Breakdown Voltages Overcome

The BiCMOS9MW design kit provides three types of NPN HBTs transistors (HS: high speed, MV: medium voltage, and HV: high voltage) which electrical parameters are summarized in Table 1. In the proposed power amplifier, HS transistors are used as they provide the highest current density to achieve high output power.

Table 1. Electrical parameters of NPN BiCMOS9MW HBTs.

Ref.	Jc@ft (mA/µm²)	BV_{CE0} (V)	BV_{CB0} (V)	ft (GHz)	fmax (GHz)
HS	7.5	1.6	5.5	220	280
MV	1.5	2	7.5	145	300
HV	0.5	3.5	13.5	60	210

A. Beyond the BV_{CE0}

Typically, the common-emitter breakdown voltage with open-base, BV_{CE0}, is given for a zero current base. However, this case is not encountered in this circuit. Considering the CB stage voltage swings and to operate beyond the BV_{CE0}, the voltage-current overlap has to be reduced. Indeed, in case of large V_{CE} swing, BV_{CE0} may exceed the open-emitter breakdown, BV_{CB0} [7]. The BV_{CE0} can be expressed as follows:

$$BV_{CE0} = 3.6281x^{-0.209}, \quad (1)$$

With

$$x = \frac{I_e}{0.0126LWnbe}, \quad (2)$$

Where *Ie* is the current emitter, *L* the emitter length, *W* the emitter width and *nbe* is the number of emitter fingers.

According to (1) and (2), the V_{CE} voltage swing is compared to the BV_{CE0} in Fig. 2.

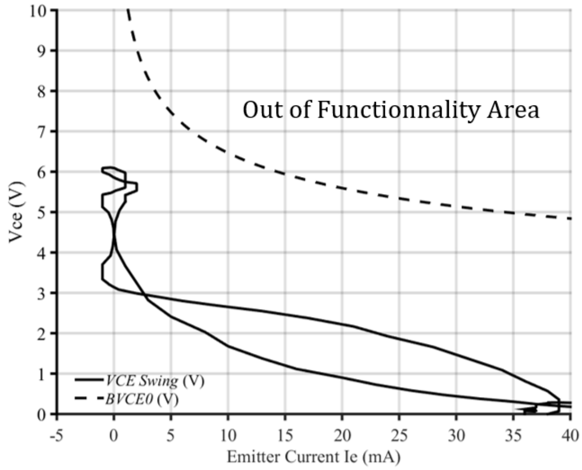

Fig. 2. Simulated V_{CE} voltage swing vs. CB emitter current (Pin = 12 dBm @9.5 GHz).

The current-voltage overlap has to be minimized in order to achieve high V_{CE} voltage swing. Quasi inverse class-F allows a good current-voltage overlap reduction due to harmonic tuning.

Indeed, by producing high impedance and low impedance at 2nd and 3rd harmonics respectively, a half-sine waveform voltage and a quasi-square current waveform are generated (Fig. 3).

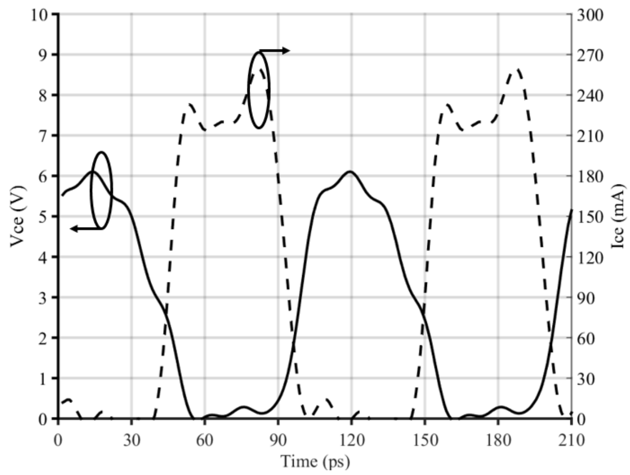

Fig. 3. Simulated waveforms of collector-emitter voltage and current emitter of the CB stage (Pin = 12 dBm @9.5 GHz).

B. Up to the BV_{CB0}

At high collector-base voltage swing, the base resistance of the CB stage has to be considered. Indeed, the series base resistance limits the breakdown voltage. The safe-operating voltage decreases with increasing base termination impedance.

To minimize the CB base resistance, the transistor is fragmented in 6 parts has shown in Fig. 4. Therefore, the collector-base voltage swing can be extended up to the BV_{CB0}.

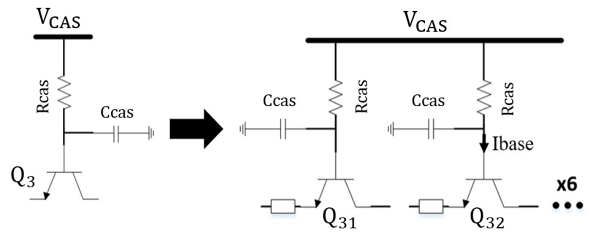

Fig. 4. Schematic of the CB stage topology.

Moreover, the *Ccas* capacitors have a double role. First, the high quality factor MIM capacitors allow to reduce the base current at the compression point. Therefore, the collector-base voltage swing can be also extended. The *Ccas* value has to be carefully chosen because a too large capacitance may induce an avalanche breakdown ($I_{base} < 0$) and a too small value will decrease the PAE

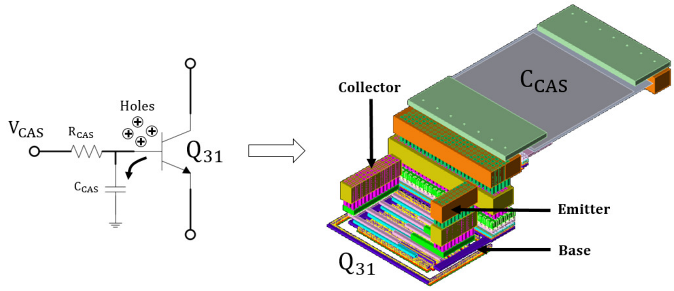

Fig. 5. An isometric 3D view of the CB transistor.

Second, the *Ccas* capacitors are also used to bypass excessive holes generated by impact ionization. Indeed, at high voltage swing, electrons have enough kinetic energy to create electron-hole pairs [8]. Holes flow into the base which cause negative base current. The base impedance has to be minimize to optimize holes evacuation and to reach high V_{CB} swings. Figure 5 shows the associated layout used to minimize the base impedance termination. Therefore, the PA reliability is improved at high compression point.

IV. Measurement Results

The compact quasi inverse class-F PA was manufactured with the SiGe 130 nm BiCMOS9MW from STMicroelectronics. The chip micro-graph of the PA is shown in Fig. 6. The chip die size is equal to 0.56 mm² including pads. The active core size is 0.17 mm², reflecting an excellent compactness.

Measurements are performed on chip with a 3.6 V supply voltage. Total quiescent DC current is 45 mA.

Measured S-parameters are shown in Fig. 7. Small-signal gain exhibits a relative bandwidth equal to 29.8% and 52.4% at -1 dB and -3 dB, respectively.

The large signal performances are obtained with a Keysight N5242A PNA-X. Due to instrument output power limitations, an AML0518P1606 driver was added to reach the required input power. The large signal performances at 9 GHz are shown in Fig. 8.

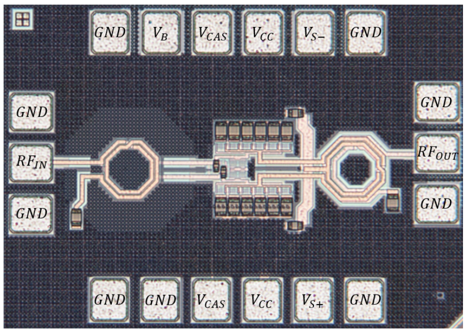

Fig. 6. Chip micro-graph of the quasi inverse class-F power amplifier.

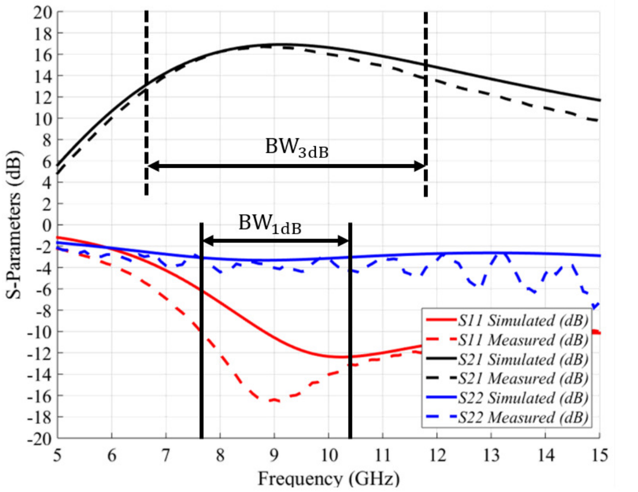

Fig. 7. Measured (dotted line) and simulated (solid line) S-parameters of the quasi F^{-1} PA.

The peak PAE is 51.8% with an output power of 25.7 dBm. At 1 dB compressed output power (P_{1dB}), the PAE is equal to 50.2% with 25.2 dBm output power. Therefore, the PA is able to operate with a high efficiency and good AM-AM linearity.

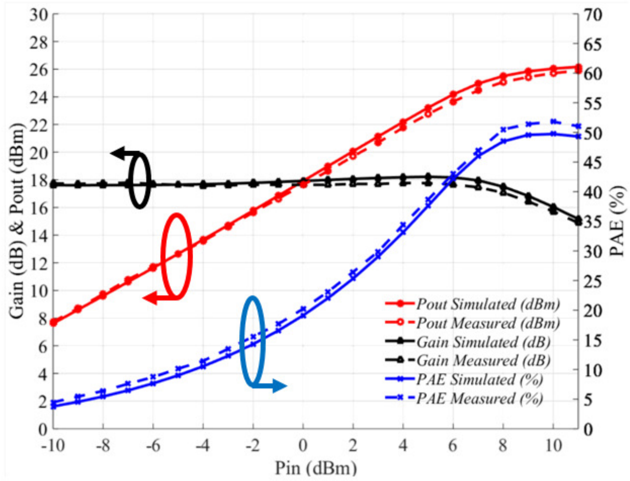

Fig. 8. Measured (dotted line) and simulated (solid line) Gain, PAE and Pout at 9 GHz of the quasi F^{-1} PA.

The measured output power and PAE over the X-band are shown in Fig. 9. From 8 to 10.5 GHz, the output power and PAE are higher than 25.3 dBm and 44.6% respectively.

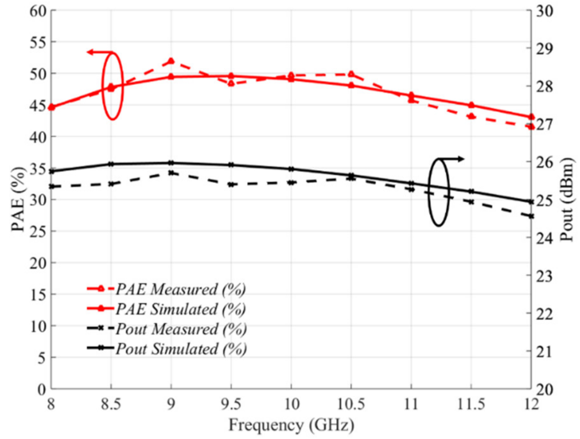

Fig. 9. Comparison between measured (dotted line) and simulated (solid line) CW large-signal performances versus frequency at *Pin* = 10 dBm.

Finally, linearity measurements have been performed at 9.5 GHz (Fig. 10). The gain expansion is lower than 0.86 dB. Moreover, the circuit shows a phase linearity smaller than 5° below 22 dBm.

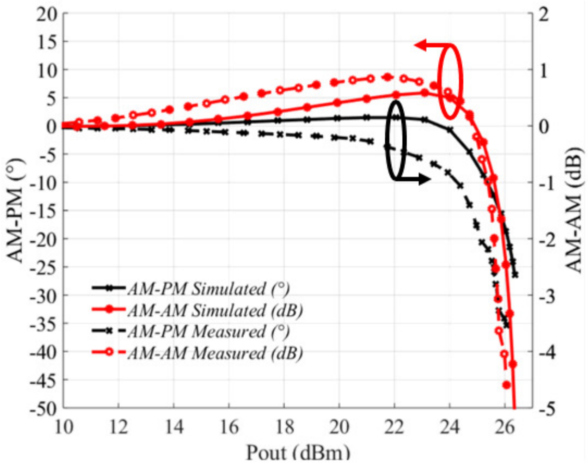

Fig. 10. Measured (dotted line) and Simulated (solid line) AM-AM and AM-PM versus *Pout* at 9.5 GHz

V. Comparison with the State-of-the-Art

Table 2. State-of-the-art comparison of X-band SiGe-based power amplifiers.

Ref.	[9]	[4]	[3]	[2]	**This work**
Tech. [nm]	250 nm GaAs	130 nm SiGe	130 nm SiGe	130 nm SiGe	**130 nm SiGe**
Gain [dB]	33	27.7	16.1	15.8	**17.3**
Psat [dBm]	35	29.5	26.5	26.3	**26.2**
PAE_{max} [%]	45	17.8	53.4	51.1	**51.8**
BW* [GHz]	8.25-9	8.0-12.0	8.6-11.2	8.0-11.5	**7.7-10.4**
Area [mm²]	5.4	2.66	0.81	0.90	**0.54**

*BW defined at 1 dB lower than maximum Gain.

The state-of-the-art performances of X-band SiGe-based power amplifiers are summarized in Table 2. In [9], [4], [3] and [2], suitable PAs for RADAR applications are presented. The PA proposed in this work exhibits an excellent compactness, compared with GaAs technology. Moreover, in comparison with [2] and [3], the structure ensures a linear behaviour with good AM-AM distortion. Finally, compared to [4], this structure drives high output power with high efficiency.

VI. Conclusion

A X-band compact quasi inverse class-F power amplifier was designed using the 130nm BiCMOS technology. It is based on the cascode topology using low impedance base termination. Thanks to a low base impedance termination, the proposed PA allows to achieve high efficiency with high output power while ensuring a linear behaviour. Large signal measurements at 9 GHz show a 51.8% peak PAE with 25.7 dBm output power. No harmonic filter has been used in this topology, resulting in an active core size as small as 0.17mm². To the authors' best knowledge, this solution is the highest efficient linear power amplifier

Acknowledgement

The authors wish to thank the STMicroelectronics foundry, together with Magali de Matos and Manuel Potéreau from the IMS Research Center for their technical support during measurements.

References

[1] T. Dinc, E. Özeren, C. Çalışkan, H. Kayahan, and Y. Gurbuz, "X-band SiGe bi-complementary metal–oxide semiconductor transmit/receive module core chip for phased array RADAR applications," *Antennas Propagation IET Microwaves*, vol. 9, nº 9, pp. 948-956, 2015.

[2] I. Ju and J. D. Cressler, "An X-band inverse class-F SiGe HBT cascode power amplifier With harmonic-tuned output transformer," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 390-393.

[3] I. Ju and J. D. Cressler, "A highly efficient X-band inverse class-F SiGe HBT cascode power amplifier with harmonic-tuned Wilkinson power combiner," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, nº 11, pp. 1609-1613, nov. 2018.

[4] C. Liu, Q. Li, Y. Li, X. Li, H. Liu, and Y.-Z. Xiong, "An 890 mW stacked power amplifier using SiGe HBTs for X-band multifunctional chips," in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, Graz, Austria, 2015, pp. 68-71.

[5] P. Scaramuzza, C. Rubino, M. Caruso, M. Tiebout, A. Bevilacqua, and A. Neviani, "Class-J SiGe X-band power amplifier using a ladder filter-based AM–PM distortion reduction technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, nº 11, pp. 3780-3789, nov. 2018.

[6] E. Kerherve *et al.*, "A broadband 4.5–15.5-GHz SiGe power amplifier with 25.5-dBm peak saturated output power and 28.7% maximum PAE," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, nº 5, pp. 1621-1632, mai 2015.

[7] M. Rickelt, H.- Rein, and E. Rose, "Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 48, nº 4, pp. 774-783, avr. 2001.

[8] M. Jaoul, D. Céli, C. Maneux, M. Schröter, and A. Pawlak, "Avalanche compact model featuring SiGe HBTs characteristics up to BVcbo," in *2017 47th European Solid-State Device Research Conference (ESSDERC)*, 2017, pp. 70-73.

[9] Y. Hua, H. Wu, X. Liao, C. Liao, . Hu, and J. Lv, "A high-efficiency 3-watt GaAs pHEMT X-band MMIC power amplifier," in 2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT), 2018, p. 1-2.