A CMOS RF Power Amplifier Using an Off-Chip Transmision Line Transformer With 62% PAE

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***Abstract*—In this letter, a two-stage 900-MHz CMOS differential power amplifier (PA) is designed and implemented in a 0.18-μm radio frequency CMOS process. A transmission line transformer on a printed circuit board is used as an output power combiner and matching circuits of a class-E power stage. To drive the power stage effectively, cascaded class-D amplifiers are used as driver amplifiers. The PA delivers an output power of 31.7 dBm and a power-added efficiency of 62.4% with a power gain of 30.3 dB, including the losses of the bond-wires and the output transformer.**

***Index Terms*—Class-D, class-E, CMOS power amplifier (PA), driver amplifier, power added efficiency (PAE), transformer.**

I. Introduction

IT IS beneficial that a CMOS power amplifier (PA) can be readily integrated with various digital control circuits in many mobile communication transmitters. Recently, due to the development of a CMOS process, it was found that the performance of a CMOS active device by itself is comparable to that of GaAs in terms of output power and efficiency [1]. The possibility of CMOS technology for nonlinear PAs has been verified in previous work [1]. However, it is difficult to realize a passive device with a high quality factor due to the lossy silicon substrate of a CMOS process. To overcome the lossy characteristics of a silicon substrate, which is the main reason for the degradation of efficiency in PAs, a transmission line transformer (TLT) on a printed circuit board (PCB) is used as an output power combiner and a matching circuit. This study demonstrates the performance limit of a CMOS PA as compared to GaAs PAs [2]. Additionally, driver circuits with cascaded class-D amplifiers are proposed to drive a power stage effectively while operating as class-E.

II. Transmission Line Transformer on PCB

The output power, $P_{\rm OUT}$, of a class-E amplifier is determined by the output load impedance, $R_{\rm LOAD}$, and the supply voltage, $V_{\rm DD}$, as in

$$P_{\rm OUT} \propto \frac{V_{\rm DD}^2}{R_{\rm LOAD}}. \tag{1}$$

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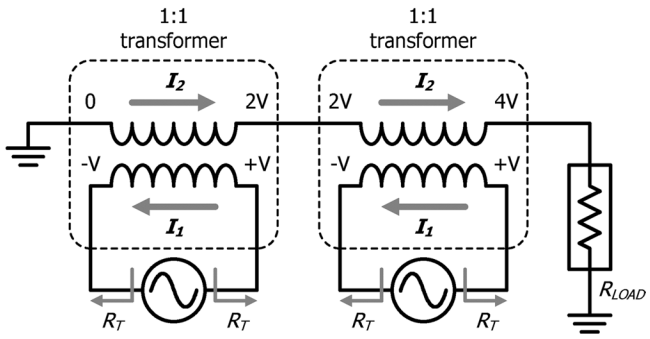

Fig. 1. Voltage combining scheme using a transmission line transformer as an output power combiner and a matching circuit to follow [1].

Transforming a load impedance to an impedance lower than 50 Ω is necessary for the maximum power transfer. Fig. 1 shows a simplified structure of a PA using a TLT as a power combiner. Ideally, the magnetically-induced current of the secondary component of the transformer would be identical to that of the primary component of the transformer. The ac voltages between the two terminals of each primary component are added at the secondary component. A 50-Ω output load, $R_{\rm LOAD}$, is therefore transformed into four equal loads of 12.5 Ω, R_T, at each output of the power transistor [3], as shown in

$$I_1 = I_2 = \frac{4V}{R_{\rm LOAD}} = \frac{V}{R_T} \tag{2}$$

$$R_{\rm LOAD} : R_T = 4 : 1. \tag{3}$$

However, with the parasitic inductance and capacitance of the transformer, and additional shunt capacitors, the load impedance of each power transistor can be tailored. The length and width of the transformer in addition to the shunt capacitance were determined in order to generate the desired output power.

In spite of the merits of the TLT, which can effectively combine output power, an on-chip TLT has several problems. Efficiency degradation of a PA using the on-chip TLT is mainly caused by the parasitic resistance of the transformer. In particular, because the length of the transformer is longer in a 900-MHz frequency band than in a higher frequency band [1], [3], [4], the substrate coupling loss as well as the parasitic resistance loss become more serious. Thus, a more efficient off-chip TLT over an on-chip TLT was studied, and the transformer structure was created on a PCB, which has a metal thickness of several tens of μm and small substrate-related losses. The loss of the transformer on the PCB is 0.238 dB in electromagnetic (EM) simulation, which is much less than the

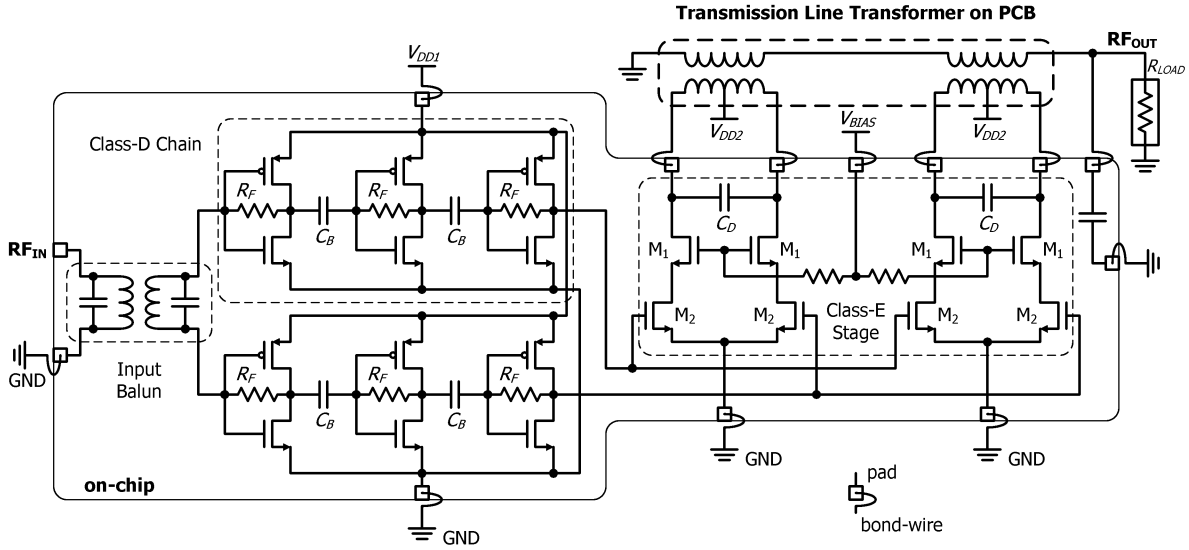

Fig. 2. Schematic of the designed PA.

loss of approximately 1.5 dB for an on-chip transformer with a metal thickness of 2–3 μm.

III. Circuit Design

A. Cascaded Class-D Driver Stage

A schematic of the designed PA is shown in Fig. 2. A transformer balun is used at the input port for differential signals. Higher efficiency can be achieved by using the power transistor (M_2) as an on/off switch instead of a high-impedance current source [5]. The driver stage consists of class-D amplifier chains in order to deliver a square wave signal to the power stage. The gain of a class-D amplifier is highest when the biases of the input and output are set to the mid-point between V_{DD1} and the ground. The input and the output of each class-D amplifier are connected through a feedback resistor (R_F) in order to equalize the bias of the output to the bias of the input. To separate the bias of each class-D amplifier, class-D amplifiers are cascaded through dc blocking capacitors (C_B). By doing this, the gain degradation of each amplifier is prevented. As the output bias of the last class-D amplifier is used for the input bias of the power stage, no additional gate bias of the power transistors is needed. When power in excess of -3 dBm is provided to the input port, the driver stage is designed to generate square wave signals. The transistor of each class-D amplifier is two times larger than that of the previous class-D amplifier.

B. Class-E Power Stage

The PA is designed with a differential structure to avoid the gain reduction due to the ground metal line and bond-wire. A cascode configuration is used in the power stage to prevent the transistor from breakdown of drain-source. The gate lengths are 0.35 μm for the common-gate transistors (M_1) and 0.18 μm for the common-source transistors (M_2). The total gate width of each power transistor (M_1, M_2) is 4096 μm. The supply voltage of the power stage is provided through the center of the primary component of the transformer, which is a virtual ground [1]. The transformer functions, therefore, as a matching network as well as an radio frequency (RF) chock. The output matching network of the power stage is designed to operate as class-E and the integrated metal–insulator–metal (MIM) capacitors (C_D) are connected between the drains of the differential power transistors (M_1).

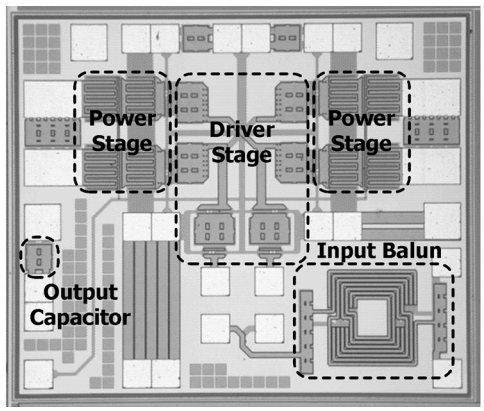

Fig. 3. Chip photograph of the PA (1.2 mm × 1.0 mm).

IV. Measurement Results

A chip photograph of the PA using a 0.18-μm RF CMOS process is shown in Fig. 3. The chip area is 1.2 mm × 1.0 mm including the input transformer and the bonding pads. Fig. 4 shows the implemented transformer on a PCB. FR4, which has a substrate thickness of 1000 μm and a metal thickness of 35 μm, was used for the PCB material. The transformer is wire-bonded to the drain terminals of the common gate transistors (M_1) on the chip. There is no additional off-chip matching component, with the exception of the transformer.

The losses of the bond-wires, the input balun, and the output transformer are included in the measurement results. The input power is fixed at 1.4 dBm in all measurements, since the amplifier operates in switching mode class-E. Fig. 5(a) shows the frequency responses of the amplifier, for which the supply voltages are 3.3 V for the power stage and 1.8 V for the driver

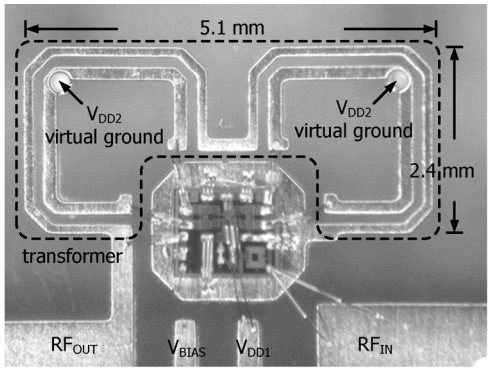

Fig. 4. Implemented transmission line transformer on PCB (5.1 mm × 2.4 mm).

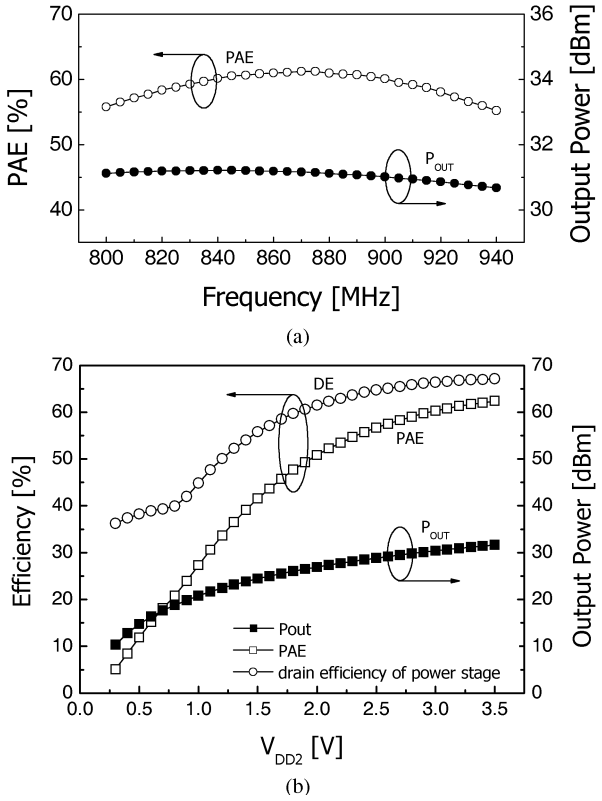

Fig. 5. (a) Measured output power and efficiency versus frequency. (b) Measured output power and efficiency versus V_{DD2}.

stages. The amplifier has an output power of approximately 31 dBm and a flatness of 0.45 dB in a frequency band from 800 to 940 MHz. The power-added efficiency (PAE) is always higher than 55% in the same frequency band and the maximum PAE is achieved at 875 MHz. Fig. 5(b) shows the efficiency and the output power while the supply voltage of the power stage varies from 0.3 to 3.5 V. The PAE is 62.4% at a maximum output power of 31.7 dBm, and the drain efficiency of the power stage is 67.2% at the same output power. The power stage and the driver stage consume dc currents of 625 mA and 91 mA, respectively. The second harmonic is −33.9 dBc and the third harmonic is −62.5 dBc. The PAE has a variation of 1.7% and the output power has a flatness of 0.14 dB while the supply voltage of the driver stage is varied from 1.7 V to 1.9 V. This amplifier maintains very stable operation under variations of the driver supply voltage. The output power remains unchanged by input power variations from −4 dBm to 14 dBm. This result shows that the driver stage successfully delivers square wave signals to the power stage. This amplifier shows the best PAE for watt-level CMOS PAs published thus far [1], [6]–[8] (see Table I). It demonstrates that the power and efficiency of a CMOS PA are comparable to those of GaAs HBT-based PAs [2].

TABLE I
COMPARISONS OF CMOS PAS

Design	Frequency (MHz)	Pout (W)	PAE (%)	Gain (dB)
I. Aoki et. al. [1]	2440	1.9	41	8.7
K.L.R. Mertens et. al [6] *	700	1.04	62	18
C. Yoo et. al. [7]	900	0.9	41	**
C. Fallesen et. al. [8]	1750	1.09	55	**
This work	875	1.48	62	30.3

* de-embedded the loss of the output balun [6].

** not indicated in the papers [7], [8].

V. CONCLUSION

In this work, the demonstration of a high efficient watt-level CMOS PA is presented. A more efficient transformer over an on-chip transformer is implemented on a PCB. A class-E power stage uses the transformer as an output power combiner and as a matching circuit. The measured PAE is 62.4% at a maximum output power of 31.7 dBm including the losses of the bond-wire and transformers. To drive the class-E power stage effectively, a cascaded class-D amplifier is also designed.

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