A Fully Integrated Flip-Chip SiGe BiCMOS Power Amplifier for 802.11ac Applications

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***Abstract*— A fully integrated flip-chip SiGe BiCMOS power amplifier for wireless local area network (WLAN) applications in the 2 GHz band is presented. In a front-end module (FEM) configuration and under 802.11ac signal excitation, the PA delivers 29 dB small-signal gain and -30.4 dB dynamic error vector magnitude (EVM) at 20.6 dBm, at nominal operating conditions (3.3 V, 25 °C). The PA tightly controls detector voltage and corrects the dynamic EVM over supply voltage, temperature, orthogonal frequency division multiplexing (OFDM) burst length and duty cycle variations.**

***Index Terms*—Front-end modules, flip chip, power amplifiers, WLAN, 802.11ac, dynamic EVM.**

I. Introduction

Exchanging large data volumes over WLAN interfaces necessitates the use of higher order modulation schemes, such as those implemented in the emerging 802.11ac standard, as well as flexible burst schemes. Varying the burst length and duty cycle may, however, place more exacting requirements on the performance of the wireless device.

The power amplifier (PA) at the end of the transmit path is responding to the WLAN bursts following its electro-thermal transient response. To accommodate the high power levels required for the transmission of information contained in short OFDM bursts, the PA will usually employ large device peripheries. This results in high power dissipation and slow electro-thermal transients which depend on the duration of the OFDM burst and the inter-frame spacing (IFS).

The information needed for signal detection, frequency synchronization and channel estimation is retrieved from the short and long training symbols transmitted during the preamble of the 802.11 frame. As the PA is turned on a few μs before the burst and its thermal turn-on transient does not settle until several hundreds of μs later, it will not reach steady state upon the arrival of the OFDM burst. Thus, the gain of the symbols relative to the preamble will vary during the thermal turn-on transient causing erroneous detection at the receiver. To avoid impairment of the dynamic error vector magnitude (DEVM), either the gain variations must be tracked and corrected at the receiver, or the PA gain turn-on transient must be controlled so that it reaches steady state to within a few tenths of a dB from the gain set in the OFDM preamble [1]-[4]. Previous publications have discussed means to correct the gain transients in the transmit side using external circuits [5] or more advanced bias circuitry [6],[7]. Work by the authors in [8] investigated the dependence of DEVM on supply voltage, temperature, modulation scheme, and burst length and addressed DEVM correction through the use of programmable bias pulse shaping techniques.

This work extends the work in [8] by presenting a SiGe BiCMOS PA for the 2 GHz WLAN band which corrects DEVM over supply voltage, temperature, burst length and duty cycle variations. Combined with a CMOS switch, it complies with the linearity requirements of the 802.11 family of standards. Unlike the circuit in [8], which was designed for wire bond based assembly, the present PA was designed for flip-chip assembly ensuring a minimum form factor and package height. In addition, power detection was compensated over supply voltage and temperature variations. Moreover, PA bias pulsing was dynamically adjusted in order to optimally correct EVM degradation due to supply voltage, burst length and duty cycle variations.

II. Flip-Chip Power Amplifier Design

Flip-chip assemblies pose various challenges to electrical design. Unlike conventional packaging techniques, flip-chip assemblies do not allow circuit tuning through modifications of wire bond lengths or laser trimming metal traces at the surface of the integrated circuit (IC). Since wire bonds cannot be used as high quality inductors, on-chip matching networks in flip-chip ICs are more integrated but less efficient compared to off-chip networks. In addition, all heat generated in the PA stages must be removed through the emitter ground bumps rather than the through-silicon vias of conventional ICs. This further deteriorates the thermal behavior of the IC and also adds additional parasitic ground inductances which reduce the gain of the last stage and increase the RF power drive, dissipation and nonlinearity of the preceding stages. Moreover, since the IC is not assembled to a PCB at shipment, it is not only the input/output pins (I/O) that need to be protected from electro-static discharge (ESD): all pins must be protected against ESD in order to minimize the risks during assembly, test and tape and reel.

Despite these disadvantages, flip-chip ICs not only save space and cost, but their RF performance is more tolerant

to process variations compared to conventionally assembled RFICs. This results in more repeatable performance trends during the evaluation and debugging procedures. In addition, use of detailed EM and thermal analysis facilitates the design task and improves the chances for first-pass design success.

At the system level, the IC must comply with the linearity requirements of the 802.11 standards over voltage, temperature and OFDM burst length and duty cycle. This includes a low 802.11ac DEVM floor of -35 dB and a tightly controlled detector accuracy requirement.

The block diagram of the PA and a die photograph are shown in Figures 1 and 2 respectively. The three stage PA operates in the 2.4–2.5 GHz band. Assembled with two external decoupling components, it fits in less than 2 mm^2 circuit board space. The IC assembly employs copper pillars for bumping as they offer better thermal conduction and tighter bump to bump pitch than traditional solder bumps.

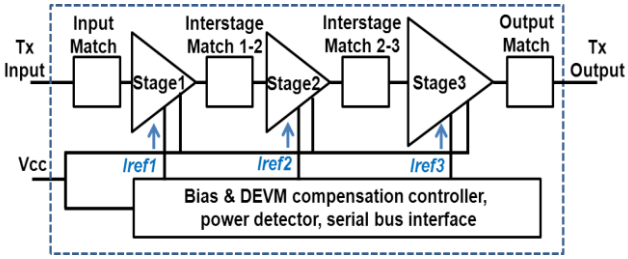

Fig. 1. Block diagram of the 2.4 GHz flip-chip WLAN amplifier.

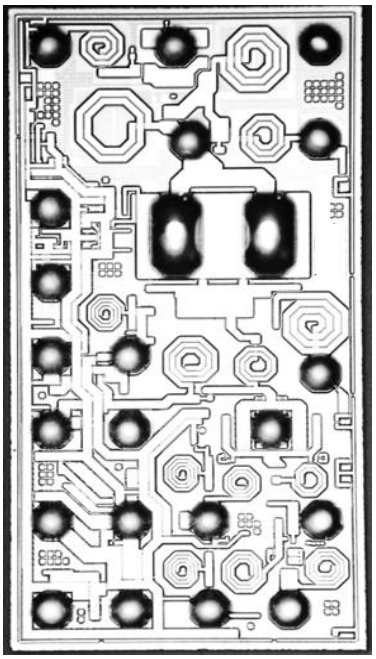

Fig. 2. Die photograph of the 2.4 GHz flip-chip WLAN amplifier.

To improve DEVM, layout was carefully planned and was supported by thermal simulations to ensure adequate heat sinking. Figure 3 shows the simulated temperature profile across the die at an output power level of 22 dBm and 3 V supply voltage. Such images are helpful when optimizing the floorplan of the PA, since they help designers identify hot spots and modify the layout ensuring that the temperature rise between junction and base plate does not exceed a maximum level beyond which the long term reliability of the IC could be compromised. Thermal imaging confirmed the simulated temperature profiles under worst case conditions and validated that transistors were operating within rated junction temperatures.

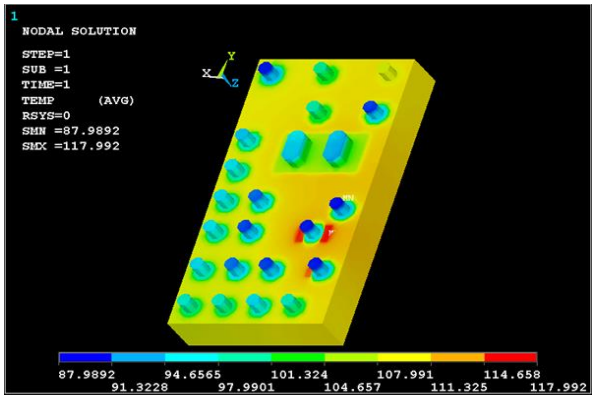

Fig. 3. Thermal simulation image of the WLAN amplifier at 22 dBm, 3 V. Base plate temperature is 85 °C.

Proper RF transistor sizing and use of temperature-compensated bias circuits can further improve the temperature uniformity across the die. Moreover, fast current sourcing techniques were employed to help the PA gain transient settle quickly into steady state as discussed earlier.

Finally, specially designed control circuitry was employed to optimize DEVM correction over battery voltage, temperature, burst length and duty cycle variations.

III. Performance

For testing purposes, the PA was cascaded with a flip-chip CMOS switch/LNA in an FEM configuration. The CSOI switch/LNA IC consists of a single-pole three-throw CMOS switch enabling WLAN Tx/Rx and Bluetooth® functionality. The low-parasitic high-speed switch employs a series-shunt configuration of multi-gate FETs with low insertion loss (in Rx mode) and maximum isolation (in Tx mode). The IC also employs a switch implementing a low power Rx bypass mode [9]. The LNA consists of a cascode transistor with emitter degeneration and was optimized to provide high linearity with simultaneous low current consumption.

In the transmit mode (Tx) of operation, the switch has an insertion loss of 0.6 dB. A model of the RF chain was developed using a mix of EM and compact models for active and passive elements, and interconnects. Figure 4 shows the measured and simulated small-signal gain of the FEM in the Tx mode at 3.3 V, 25 °C.

Discrepancies between measured and modeled data can be attributed to the lack of a complete electro-thermal model that reflects the actual temperature profile across the die, process variations and assembly tolerances that could not be represented accurately in the FEM model.

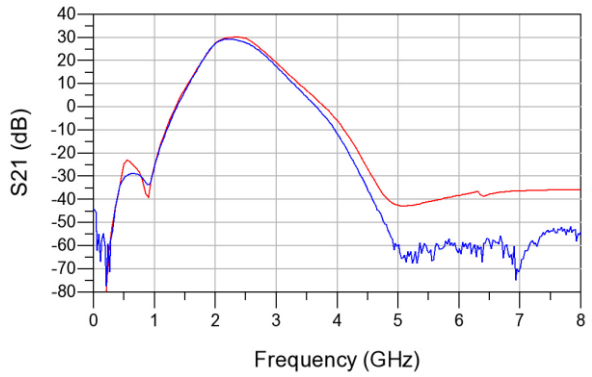

Fig. 4. Measured (blue) and simulated (red) S21 of the flip-chip FEM at 3.3 V, 25 °C.

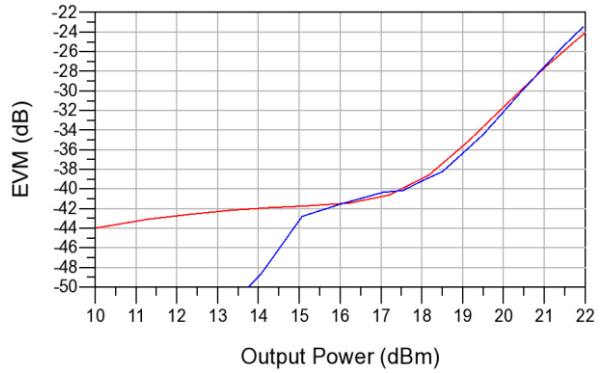

Fig. 5. Measured (blue) and simulated (red) static EVM (802.11g 54 Mb/s) of the flip-chip FEM (2.45 GHz, 3.3 V, 25 °C).

The FEM delivers a small-signal gain of 29 dB at 2.45 GHz range for a quiescent current of 116 mA. Figure 5 shows the measured and simulated static EVM at 2.45 GHz under 802.11g 54 Mb/s modulation, as a function of output power. At 3.3 V, 25 °C, the FEM achieves a -30.4 dB EVM at 20.3 dBm. Under 802.11ac modulation, it delivers 20.6 dBm for the same operating conditions.

Extended tests were carried out under different modulation schemes, duty cycles, temperatures and supply voltages.

As discussed in [8], for a given burst length the optimum DEVM correction setting (e.g. bias pulse amplitude) decreases as off time (duty cycle) decreases (increases) and approaches zero (e.g. no bias pulse shaping is applied) as off time approaches zero. This is expected since off time = 0 corresponds to the static EVM case. Secondly, for a given off time, the DEVM correction setting decreases as burst length (duty cycle) increases. Since the PA does not completely cool off when pulsed with a high duty cycle burst, its turn-on transient will have a memory of previous on-state temperature. Higher duty cycles have successively more correction memory. Similar observations were made with respect to supply voltage, where it was found that the optimum correction setting decreases with supply voltage.

In addition to the work in [8], the DEVM compensation scheme implemented in this work dynamically adjusts the DEVM correction settings according to the supply voltage and the off time in order to generate the appropriate bias pulse shape, ensuring a fast settling of the gain transient. As a result, the output power meeting a certain linearity requirement (e.g. -30.4 dB) for a given supply voltage and temperature does not vary by more than 0.29 dB, as a function of duty cycle. This is illustrated in Figure 6, for the case of 176 µs long 802.11n bursts at 2442 MHz, at the extreme operating condition 3.6 V, 85 °C.

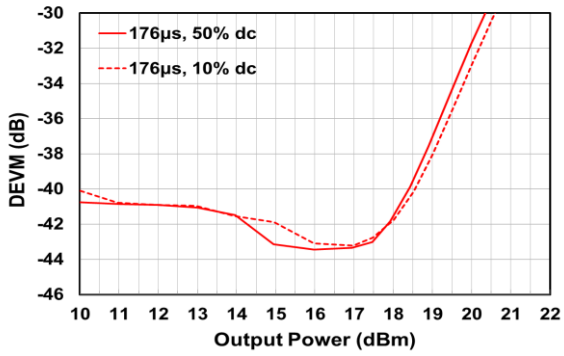

Fig. 6. Measured DEVM vs. output power for a 176 µs 802.11n burst as a function of duty cycle (2.45 GHz, 3.6 V, 85 °C).

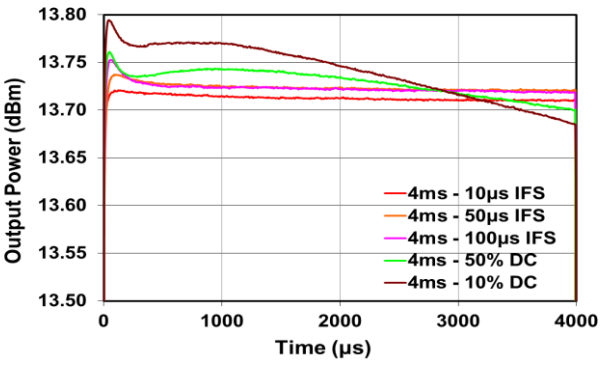

Figure 7. Measured transient output power response under pulsed DC, continuous CW excitations (2.45GHz, 3.3V, 25°C).

To further validate the functionality of the IC, tests were carried under longer burst conditions. Figure 7 shows the output power transient under continuous CW excitation at 2.45 GHz and bias pulsing conditions using 4 ms long bursts and varying the interframe space (IFS) and duty cycle. As one observes, the PA power remains within 0.1 dB from its steady state for the duration of burst even for the lowest duty cycle (10%), where it completely cools during the inter-frame OFF period.

Consequently, the DEVM shown in Figure 8 for 802.11ac bursts shows very little degradation as a function of output power for the various long word burst schemes. Comparing Figures 7 and 8 one observes the relation between the DEVM at backed-off power levels and the power transient characteristic: a transient settling faster to the steady state results in low DEVM levels at backed-off power levels.

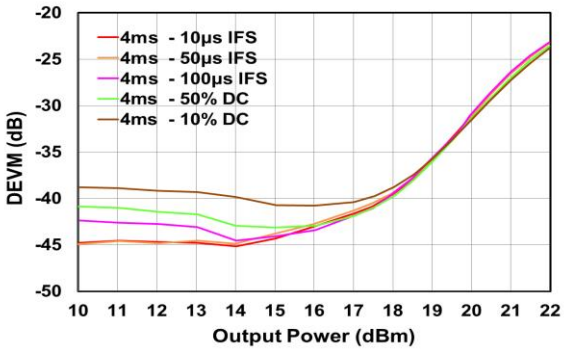

Figure 8. Measured DEVM vs. output power under pulsed 4 ms 802.11ac bursts and varying IFS and duty cycle (3.3V, 25°C).

Figure 9 shows the detector voltage CW response in the 2.4–2.5 GHz range as a function of output power, for supply voltages between 3.0 V and 3.6 V and temperatures in the -20 °C to 85 °C range.

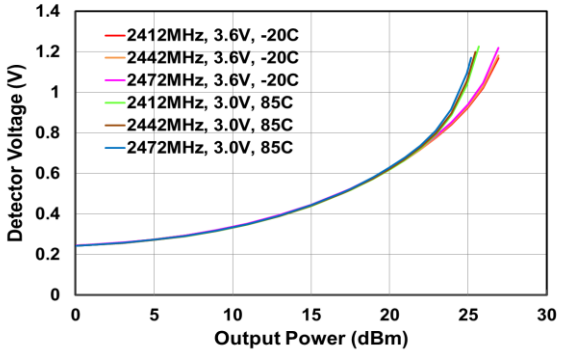

Figure 9. Measured CW response of power detector in the 2.4–2.5 GHz band over supply voltage and temperature variations.

As one observes, the detector voltage does not vary over supply voltage and temperature variations up to a power level of 22 dBm. This allows the transceiver to accurately control the output power thereby ensuring maximum data transmission under all operating conditions. For power levels larger than 22 dBm, the detector voltage is limited by gain compression and increases faster with power for lower supply voltages.

IV. Conclusion

A WLAN flip-chip PA operating in the 2 GHz band has been developed. In an FEM configuration, it delivers 29.5 dB small-signal gain and -30.4 dB EVM at 20.6 dBm at 3.3 V, 25 °C. The PA demonstrates robust DEVM and power detector control under variable supply voltage, temperature, duty cycle, and burst length.

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