A Broadband Linear Millimeter-Wave Power Amplifier With an Adaptive Bias Circuit

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***Abstract*—A broadband linear millimeter-wave power amplifier (PA) with an adaptive bias circuit implemented in 0.25 um SiGe BiCMOS for 5G millimeter-wave phased arrays is presented in this paper. The PA demonstrates a measured 21.7-dB small signal gain, 17.1-dBm saturated output power and 26.5% peak power added efficiency (PAE) at 27 GHz and the peak PAE maintains over 20% from 25 GHz to 32 GHz. At 27.5 GHz, the proposed PA is tested with an 800 MHz bandwidth 64-QAM signal without digital predistortion, which achieves a PAE of 11.56%, error vector magnitude (EVM) of −29.7 dB, and adjacent channel leakage ratio (ACLR) of −28.01 dBc at an average output power of 8.77 dBm.**

***Index Terms*—5G mobile communication, SiGe, mm-wave, power amplifiers(PAs), broadband, linearity.**

I. Introduction

The 5th generation (5G) mm-wave systems are expected to provide extremely high communication rate and spectral efficiency in order to face more complex application scenarios. To fulfill the increasing demand for high data rates, new broadband spectra and complex modulations need to be adopted to improve spectrum efficiency. Multiple mm-wave frequency bands around 28 GHz have been proposed for 5G communication in different countries and areas, including 27.5-28.35 GHz for the US, 24.25-27.5 GHz for Europe and China, 26.5-29.5 GHz for Korea, 27.5-29.5 GHz for Japan [1]. In order to achieve international roaming, the power amplifiers(PA) are required to cover these bands while maintaining high efficiency. In addition, complex modulation with high peak to average power ratios (PAPRs) and large RF bandwidths will require higher performance of PA especially the linearity [2]. Due to the digital predistortion technology limited in the millimeter-wave band, the linearization problem needs to be solved from the perspective of circuit design.

In this paper, we propose a broadband linear mm-wave PA with an adaptive bias circuit as shown in Fig. 1. The PA achieves a power added efficiency (PAE) of 11.56%, error vector magnitude (EVM) of −29.7 dB, and adjacent channel leakage rate (ACLR) of −28.01 dBc at an average output power of 8.77 dBm for a 64-QAM signal with 800 MHz bandwidth. Also, it maintains over 20% peak PAE from 25 GHz to 32 GHz.

II. Circuit Design

A. Adaptive Bias Circuit

The nonlinearity of power amplifier based on heterojunction bipolar transistor (HBT) is mainly caused by the nonlinearity of base-emitter diode of the input amplification transistor. The PA adopts an adaptive bias circuit to solve this problem which consists of a resistor, a bypass capacitor, two diodes, and a compensation transistor. The bypass capacitor C3 and C5 provide the function of shorting the inserted RF signal. The resistance R and the two diodes can provide a constant voltage for the base of the compensation transistor. When the input power increases, the dc current after rectification by the base-collector diode of compensation transistor Q2 and Q5 increases, and the dc voltage across the junction decreases, thereby compensating the base-emitter voltage of the input amplification transistor. Therefore, the transconductance under the large signal of the transistor can be kept consistent with the small signal to improve the linearity.

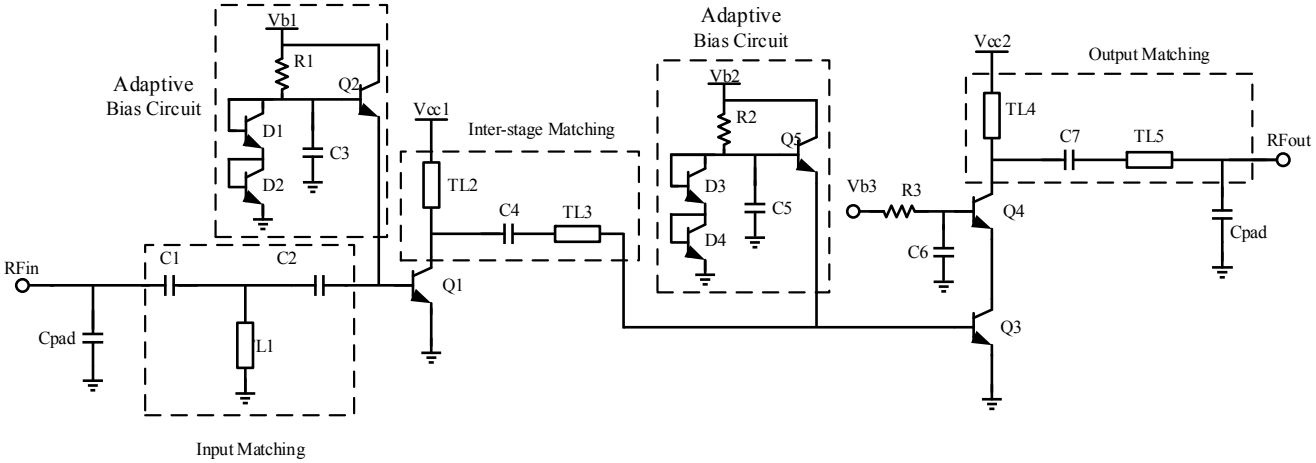

Fig. 1. Schematic of the designed PA with an adaptive bias circuit.

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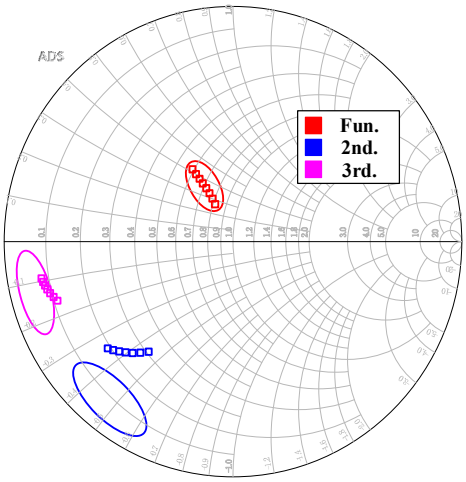

Fig. 2. The optimum impedances of fundamental, second and third harmonic by multi-harmonic load-pull.

B. Matching Network Design

The output matching network is designed with a multi-harmonic load-pull simulation for high efficiency and broadband operation. The areas covered by the circles represent the optimal impedances of fundamental, second and third harmonic respectively as shown in Fig. 2. In our design, the output matching network was designed to provide the near optimum impedance at both the fundamental frequency, 2nd and 3rd harmonic.

The input match was conjugately matched to 50Ω using a π-network of a shunt microstrip line and series MIM capacitors. The inter-stage matching adopts power matching for the front stage and conjugate matching for the latter stage. It can simultaneously improve the power efficiency of the front stage and the gain of the latter stage by adopting this matching method.

III. Measurement Results

The designed PA is implemented in IHP 0.25 um SiGe BiCMOS process with a chip size of 0.66×0.55 mm^2, as shown in Fig. 3. S-parameter simulation and measurement results of the PA are illustrated in Fig. 4. The forward gain S_{21} achieves 21.7 dB gain at 27 GHz.

The measured large-signal performances at 27 GHz are depicted in Fig. 5. The saturated output power is 17.1 dBm, oP1dB is 15.7 dBm, peak PAE is 26.5%, PAE at 1-dB compression is 24.9% and PAE at 7-dB back-off is 14% at 27 GHz. The measured continuous-wave large-signal performance versus frequency is shown in Fig. 6. The peak PAE maintains over 20% from 25 GHz to 32 GHz, which addresses the efficiency-bandwidth challenge of mm-wave PAs.

Fig. 7 and Fig. 8 shows the measured ACLR and EVM at 27.5 GHz. The PA achieves PAE of 11.56%, EVM of −29.7 dB, and ACLR (upper band) of −28.01 dBc at an average output power of 8.77dBm for a 64-QAM signal with 800 MHz bandwidth.

The results are summarized and compared with reported silicon-based PAs around Ka-band frequencies in Table I. Considering bandwidth and linearity, the proposed PA achieves good performance.

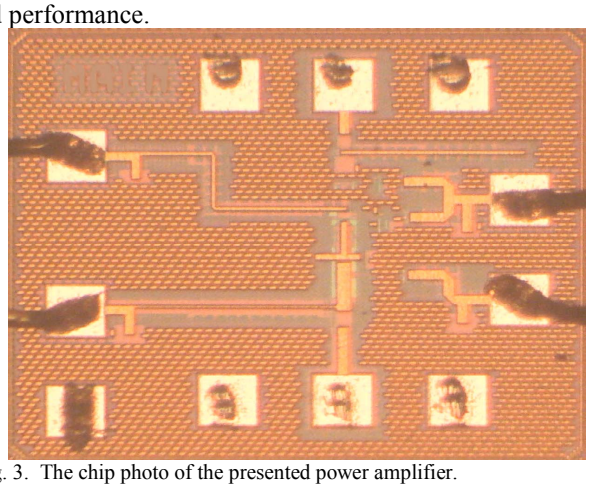

Fig. 3. The chip photo of the presented power amplifier.

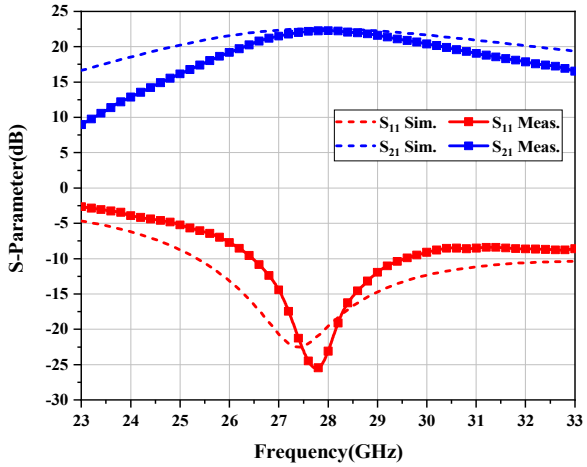

Fig.4. Measured and simulated S-parameters.

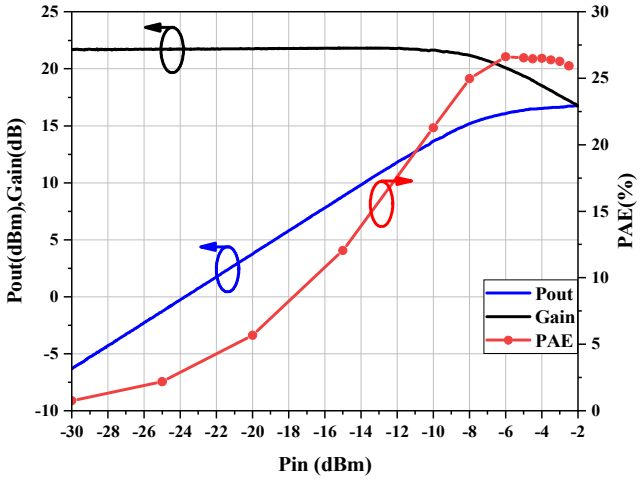

Fig.5. Measured Gain, Pout, and PAE against input power at 27 GHz.

Table 1. Comparison with silicon-based mm-wave PAs.

Reference	Freq. (GHz)	Gain (dB)	Po.1dB (dBm)	Po.sat (dBm)	PAE 1dB (%)	PAE sat (%)	BW (GHz)	Modulated Signal	RF BW (MHz)	Data rate (Gb/s)	ACLR (dBc)	EVM (dBc)	Po@ EVM (dBm)	PAE@ EVM (%)	Active Area (mm2)	Topology	Tech.
This work	**27.5**	**21.7**	**15.7**	**17.1**	**24.9**	**26.5**	**7**	**64-QAM**	**800**	**3.6**	**-28.01**	**-29.7**	**8.77**	**11.56**	**0.36**	**2-Stage Cascode**	**0.25um SiGe**
[2] JSSC 16	30	15.7	13.2	14	34.3	35.5	4	64-QAM	250	-	-	-25	4.2	9	0.16	2-Stage Diff.	28nm CMOS
[3] MTT 17	28	15.3	15.5	18.6	31.5	35.3	2	16-QAM	800	-	-	-22	10.6	-	0.45	1-Stage Cascode	0.13um SiGe
[4] MTT 18	28	8.9	13.6	14.4	37.2	40.1	6	64-QAM	250	-	-	-26.6	7	14.1	0.11	1-Stage CS	65nm CMOS
[5] ESSCIRC 18	28	19	17.4	18	26.5	26.7	7.5	64-QAM	200	1.2	-	-27	10.5	17.8	0.16	2-Stage Diff.	65nm CMOS

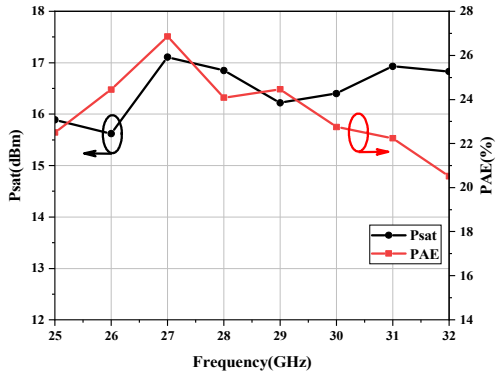

Fig. 6. Measured continuous-wave large-signal performance versus carrier frequency.

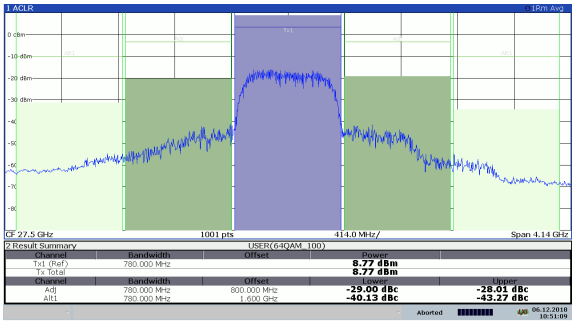

Fig. 7. Measured ACLR waveforms at 27.5 GHz for 64-QAM, 800-MHz signals.

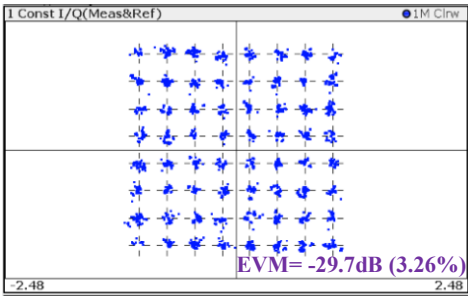

Fig. 8. Measured constellation and EVM at 27.5 GHz for 64-QAM, 800-MHz signals.

IV. Conclusion

This paper presents a broadband mm-wave PA with an adaptive bias circuit using a 0.25 um SiGe BiCMOS process. By controlling the optimization of harmonic impedance, the PA achieves good results in both efficiency and bandwidth. At 27 GHz, the PA achieves 21.7 dB small signal gain, 17.1-dBm saturated output power and 26.5% peak PAE, and the peak PAE maintains over 20% from 25 GHz to 32 GHz. By applying the adaptive bias circuit, the PA achieves PAE of 11.56%, EVM of −29.7 dB at an average output power of 8.77 dBm with an 800 MHz bandwidth 64-QAM signal.

Acknowledgment

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