A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier

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***Abstract*—A monolithic SiGe BiCMOS envelope-tracking power amplifier (PA) is demonstrated for 802.11g OFDM applications at 2.4 GHz. The 4-mm^2 die includes a high-efficiency high-precision envelope amplifier and a two-stage SiGe HBT PA for RF amplification. Off-chip digital predistortion is employed to improve EVM performance. The two-stage amplifier exhibits 12-dB gain, $<5\%$ EVM, 20-dBm OFDM output power, and an overall efficiency (including the envelope amplifier) of 28%.**

***Index Terms*—Envelope tracking, orthogonal frequency-division multiplexing (OFDM), power amplifier (PA), SiGe, wireless local-area network (WLAN).**

I. Introduction

HIGH-EFFICIENCY radio frequency (RF) power amplifiers (PAs) are critical in portable battery-operated wireless communication systems, because they can dominate the DC power consumption in the transmit mode [1], [2]. To maximize the efficiency of the PA, a constant envelope modulation scheme is often employed, since the PA can operate in the high-efficiency or switched mode of operation (such as Class D, E, or S) [3]–[5]. However, with modern wireless communication systems evolving to a higher data rate, non-constant-envelope modulation schemes are preferred. For example, the wireless local area network (WLAN) 802.11g standard employs 64 QAM modulation and 52 orthogonal frequency-division multiplexing (OFDM) carriers at a 54-Mb/s data rate centered near 2.4 GHz. This modulation format has a high-envelope peak-average ratio (PAR) of 12–14 dB [6], [7]. This nonconstant envelope modulation requires highly linear PAs to avoid distortion of the signal.

Traditionally, linear PAs are implemented by "backing off" the Class-A or Class-AB PA, so that their average output power is well below the amplifier saturated power. Unfortunately, this decreases the average efficiency, since the PA now operates in the low-efficiency region most of the time [8], [9]. The efficiency can be improved using gate/base modulation approaches [10], but the improvement in efficiency is relatively modest. In all of these cases, the average efficiency is much lower than the peak efficiency for a high PAR signal, demonstrating the well-known tradeoff between linearity and efficiency.

This tradeoff problem has been investigated for many years. Collector/drain modulation schemes offer the greatest potential for realization of high-average-efficiency/high-linearity operation for high PAR signals [11]–[13]. However, due to bandwidth limitations of the DC/DC converter, these traditional dynamic supply control schemes are typically limited to narrow-bandwidth applications like EDGE and CDMA [13], [14]. In addition, these power-supply modulation schemes are complicated and often require digital predistortion, precision time alignment, and a mix of video and RF design approaches to simultaneously realize high linearity and high efficiency. As a result, most implementations of these techniques to date use hybrid rather than monolithic circuit techniques.

In this paper, we demonstrate a monolithic 2.4-GHz envelope-tracking OFDM PA implemented in a SiGe BiCMOS technology. Section II reviews collector/drain modulation approaches for high-linearity/high-efficiency amplification. Section III discusses the design tradeoffs for a wideband high-efficiency envelope amplifier design. Section IV presents the experimental measurements of the wideband envelope amplifier and the complete PA designed for WLAN 802.11g applications.

II. Wideband Collector/Drain Modulation PA Approaches

Dynamic power-supply schemes are usually separated into two types: envelope elimination and restoration (EER) and envelope tracking (ET). Fig. 1 shows the principles of traditional EER and ET systems. EER uses a combination of a high-efficiency switched-mode PA with an envelope remodulation circuit [10]–[14]; ET utilizes a linear PA and a controlled supply voltage, which closely tracks the output envelope. When the supply voltage tracks the *instantaneous* output envelope, it is known as wide-bandwidth ET (WBET) [9], [15]–[17]; when the supply voltage tracks the *long-term* average of the output envelope, it is known as average ET (AET) [18], [19]. AET techniques are especially useful for power control schemes, such as the reverse link in CDMA, where the long-term variation in average power is much greater than 20 dB [8]. However, they improve the efficiency only modestly for high-PAR signals such as

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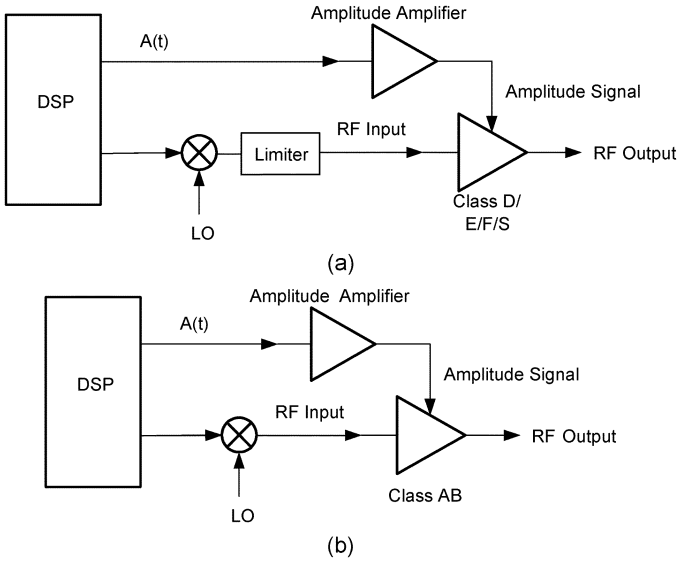

Fig. 1. Block diagram of (a) EER PA and (b) ET PA.

OFDM. For OFDM, wideband ET is preferred. Gate/base modulation approaches have also been explored, but they are also less effective for OFDM signals [20], [21].

In both EER and wideband ET systems, the collector/drain supply of the RF power transistor dynamically changes with the output envelope, so the RF transistor operates with higher efficiency over a wide dynamic range of output power. Theoretically, EER is more efficient than ET, since the RF transistor is always operating in a switching mode. In the traditional EER system, the input RF signal is applied to a limiter (as shown in Fig. 1); this is a problem for some wide dynamic range OFDM signals, where the peak-to-minimum ratio is essentially infinite [22]. By contrast, ET systems are better positioned to accommodate high peak-to-minimum signals because the amplifiers operate in a linear (if slightly compressed) mode at all output power levels, so the gain variation is manageable.

In modern EER systems, the amplitude and phase component signals are generated directly in the baseband domain and upconverted to RF. For the complex modulated signal, the complex baseband signal $s_{\rm BB}(t)$ can be expressed with Cartesian coordinate components $I(t)$ and $Q(t)$ or the polar phasor components $A(t)$ and $\Phi(t)$ as

$$s_{\rm BB}(t) = I(t) + jQ(t) = A(t)\phi(t) \tag{1}$$

where the magnitude of the complex envelope is

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2}$$

and the phase signal of the complex envelope—with appropriate mapping to the entire complex plane—is

$$\phi(t) = e^{j\arctan(Q(t)/I(t))}. \tag{3}$$

Due to the nonlinear operations of (2) and (3), the bandwidths of the amplitude signal $A(t)$ and the phase signal $\Phi(t)$ are much wider than that of baseband signal $s_{\rm BB}(t)$ [23]. This imposes practical challenges to the traditional EER transmitter and typically limits it to narrow-bandwidth applications [24], [25]. By contrast, the ET system requires a lower envelope amplifier bandwidth and less precise time-alignment between the envelope and RF paths [17]. Therefore, it is more easily applied to applications requiring a wide signal bandwidth such as OFDM. For these reasons, we choose a wideband ET amplifier for this investigation.

III. High-Efficiency Wideband Envelope Amplifier Design

The use of wideband ET techniques can boost the RF PA drain/collector average efficiency, but the total system efficiency is determined by the product of the envelope amplifier efficiency and the RF transistor drain/collector efficiency [26]–[28]. Thus, a high-efficiency envelope amplifier design is critical to the EER/ET system. This design is itself quite challenging, since the amplifier needs to provide a 3-V peak amplitude signal to a load (the PA collector) of just a few ohms, at a frequency of well over 20 MHz. The load impedance presented to the envelope amplifier by the collector can be estimated from

$$P_{\rm RF} \approx \frac{\eta_{\rm RF} A_{\rm rms}^2}{R_{\rm load}} \tag{4}$$

, where $\eta_{\rm RF}$ is the collector efficiency and $P_{\rm RF}$ is the rms output power. For example, for a 3.3-V supply voltage and 9-dB PAR signal, the equivalent $R_{\rm load}$ is approximately 5 Ω for a 40% efficiency PA when the output power is 19 dBm.

The high-efficiency envelope amplifier is usually realized by a DC/DC converter whose switching frequency is several times the signal bandwidth [2], [29]. For narrow-bandwidth applications, most high-efficiency switching-mode DC/DC converters for PA applications are realized by traditional delta-sigma [13], [27], [30], [31] or pulsewidth modulation (PWM) [9], [32], [33] modulators. However, the high switching frequency introduces a significant switching loss for a wideband signal. For example, a 20-MHz envelope bandwidth is required for an 802.11g OFDM signal for low EVM, so the switching frequency of the traditional DC/DC converter needs to be of the order of 100 MHz, which can introduce a significant switching loss [2] and out-of-band switching noise.

To overcome the tradeoff between efficiency and bandwidth of the traditional DC/DC converter, a combination of linear amplification and switching-mode converter may be used. To this end, a feed-forward topology is proposed in [34], [35]. For proper operation, time-alignment between the switching mode and linear portions of the circuit must be maintained, and a power combiner is required at the output. In this study, we utilize a different approach, based on a combination of linear stage and switching-mode stage in a feedback loop, which we term linear control of Delta modulation (LCDM). A similar topology was originally proposed to improve the fidelity of the Class-D audio amplifier [36]–[44]. A block diagram of this approach is shown in Fig. 2. The nonlinear transformation from I(t) and Q(t) to the envelope signal A(t) will greatly expand the envelope signal bandwidth. However, most of the energy is concentrated from DC to 20 kHz (e.g., more than 85% for an OFDM waveform), and 99% of the energy is concentrated

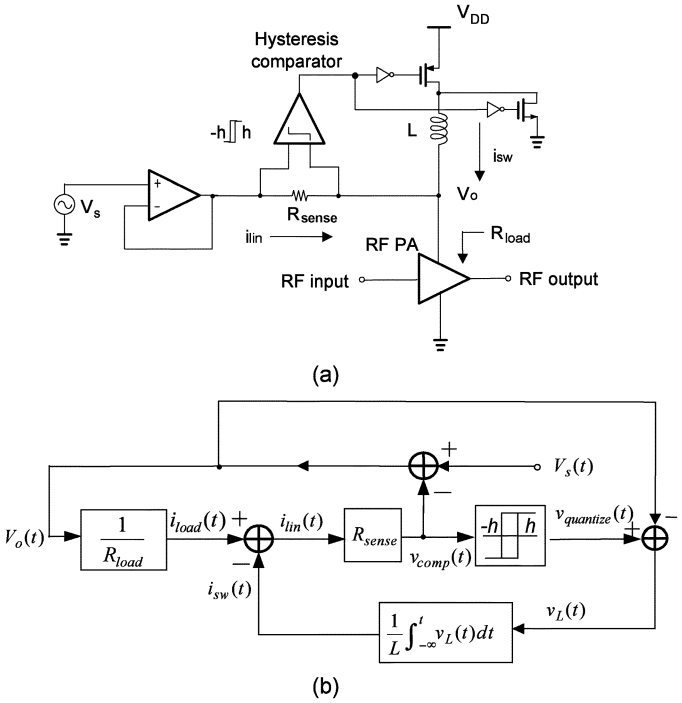

Fig. 2. (a) Simplified block diagram of the WLAN wideband ET PA with envelope amplifier. (b) Simplified block diagram of an envelope amplifier.

below the signal RF bandwidth of 20 MHz [26]. This characteristic of the signal energy implies that a "split-band" envelope amplifier using LCDM can achieve a high efficiency over a wide bandwidth.

This split-band envelope amplifier is composed of a wideband (but rather low-efficiency) linear stage and a high-efficiency narrowband switching stage, where the overall efficiency is a combination of the two efficiencies. In this case, a high-efficiency switching amplifier operates in parallel with a linear op-amp-based amplifier. The linear amplifier supplies the current to the RF PA when the switching stage cannot respond quickly enough, and the switch stage operates by sensing the current supplied by the linear stage. The optimization of this topology for OFDM applications was extensively reviewed in [45]. The result of this analysis is that an optimized switching stage operated at a frequency of roughly one-third the envelope signal bandwidth.

A hysteretic current feedback control is used to realize the smooth power split between the switch-stage and linear-stage amplification, as shown in Fig. 2(a). Fig. 2(a) shows the circuit implementation of the envelope amplifier using an op-amp as the linear voltage source and a buck converter as the current source (switch stage). The current feedback control is composed of a current sense resistor $R_{\rm sense}$, which senses the current direction, and a hysteretic comparator to control the single-pole-double-throw switch, consisting of a pMOS and nMOS transistor. The inductor L is alternately switched between $\rm V_{DD}$ and ground under control of the comparator, whose output is controlled by current supplied by the linear stage. The gain of the comparator operates to set the current supplied by the linear stage to zero, but—as shown in Fig. 2(b)—the integration function performed by the inductor limits the bandwidth of the loop response. The current flowing through the linear stage is minimized with respect to an error signal in the current feedback.

The block diagram of the circuit is shown in Fig. 2(b), which is extensively analyzed in [45]. The switching frequency of this stage is determined by the hysteresis of the comparator, and an increase in hysteresis causes an increase in the time required for the comparator output to change states, lowering the frequency. For low-envelope modulation signal frequencies and for small amplitudes, the *average* switching frequency of the switch stage is approximately

$$f_{\rm sw} \approx \frac{R_{\rm sense}}{L}\frac{A_{\rm DC}}{2h}\left(1-\frac{A_{\rm rms}}{V_{\rm DD}}\right) \tag{5}$$

where A is the envelope modulation signal consisting of a DC portion $A_{\rm DC}$ and an rms portion $A_{\rm rms}$, L is the switch-stage inductance, and h is the hysteresis of the comparator. In this case, (5) applies at envelope modulation signal frequencies and amplitudes where the *slew rate* of the envelope modulation current is less than the $V_{\rm DD}/L$. In this case, most of the PA current is supplied by the inductor. Note that the average switching frequency is a function of both the DC and AC components of the envelope signal. Also, here, the average switching frequency is less than the envelope modulation frequency, which is beneficial for minimizing the switching loss and the out-of-band switching emissions. When the average slew rate required by the load current *exceeds* the average slew rate that the switch stage can provide, the input AC signal exceeds the slew rate limitation of the switch stage. In this case, the switching frequency becomes equal to the envelope modulation frequency, and the linear stage provides a large portion of the load current. There is a delay of approximately 15 ns along the control loop, from the comparator to the switcher. The effect of this delay on the average switching frequency can be included in (5) by adjusting the hysteresis value, so that the effective hysteresis value is the weighted combination of the comparator hysteresis value and the hysteresis induced by the delay itself (which is approximately $\tau_{\rm delay}R_{\rm sense}\partial i_{\rm lin}/\partial t$).

For the envelope amplifier designer, the goal is to maximize the circuit efficiency and at the same time to maintain the high fidelity of the signal. Among the five circuit parameters (L, h, $R_{\rm sense}$, $R_{\rm load}$, $V_{\rm DD}$), L and the hysteresis h are under complete control of the circuit designer. The current sense resistor $R_{\rm sense}$ is chosen to be much smaller than $R_{\rm load}$ for low loss. The determination of h is a tradeoff issue between the signal fidelity and the average switching frequency; a smaller h will lead to a smaller error in the switcher output, but a larger switching frequency, from (5). From simulations and (5), a 7-mV hysteresis value provides an optimized switching frequency with respect to efficiency for this application, as well as a low EVM for the 802.11g signal [45]. The comparator is based on a standard CMOS design, as described in [46].

The operational amplifier is designed for a wide gain-bandwidth product and a low DC power consumption, so a traditional folded-cascode topology with a rail-to-rail Class-AB output stage is employed as shown in Fig. 3 [47]. In order to minimize the DC power consumption, a low-quiescent current rail-to-rail Class-AB output buffer is employed to provide the output linear supply current to the PA. The current in source followers

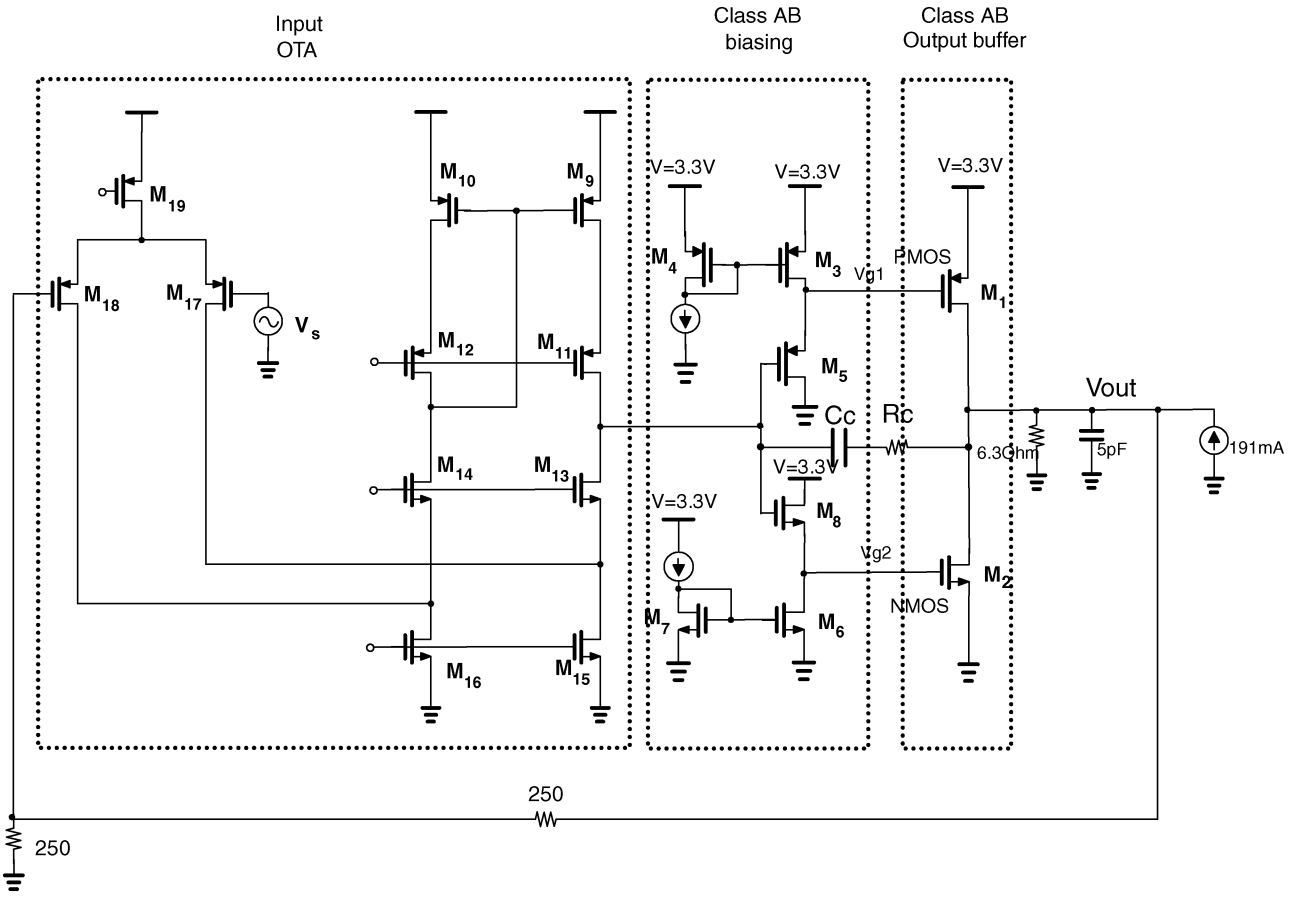

Fig. 3. Simplified schematic of Class-AB rail-to-rail op-amp (the load and the switch stage are respectively simplified as a resistor and a DC current source). Op-amp quiescent current is 3 mA. Closed-loop gain is 3 dB. Maximum output voltage is 3 V. Closed-loop bandwidth at 3-dB gain is 20 MHz.

M3–M8 is set to keep the Class-AB output devices M1–M2 operating at low quiescent currents. This approach will exhibit high sensitivity of the quiescent current to process and power supply variations, since a variation in a threshold voltage of M3–M8 with respect to M1–M2 will result in a change in the effective gate-to-source voltage. If desired, this sensitivity can be reduced through the use of more elaborate Class-AB biasng schemes [48]. Since the linear current supplied by the Class-AB output can be as high as 300 mA, as shown in the next section, the pMOS and nMOS devices must be sized to supply the necessary current; in this case, the nMOS device (M2) is $2\ \text{mm} \times 0.4\ \mu\text{m}$ and the pMOS device (M1) is $8\ \text{mm} \times 0.4\ \mu\text{m}$. The operational amplifier/Class-AB output buffer has a quiescent DC current consumption of 3 mA and, when operated in the closed-loop mode, has a simulated gain of 3 dB and a bandwidth of 20 MHz when driving a load of 5 Ω [from (4)] in parallel with 5 pF (which is the approximate reactance of the parallel combination of the power transistor and the inductor).

Maximizing the efficiency of the class-AB stage is a key to maximizing the overall linear amplifier efficiency. The fundamental power losses from the class-AB output stage are due to the finite voltage across the output transistors when they are sourcing or sinking current and are approximately

$$P_{\text{NMOS}} \approx \left(I_{\text{sw}} - \frac{V_{\text{out}}}{R_{\text{load}}}\right) \cdot V_{\text{out}} \tag{6a}$$

$$P_{\text{PMOS}} \approx \left(\frac{V_{\text{out}}}{R_{\text{load}}} - I_{\text{sw}}\right) \cdot (V_{\text{DD}} - V_{\text{out}}). \tag{6b}$$

These losses limit the overall efficiency of the linear amplifier to a maximum of approximately 30% for a typical OFDM waveform [45].

The switch stage is realized by a buck converter, as shown in Fig. 2, and requires an off-chip inductor ($L = 10\ \mu\text{H}$). Along with the linear stage, the efficiency of the buck-converter stage is critical for achieving a high overall efficiency. The power loss of the switch stage is dominated by *three* factors: conduction loss (Ron loss) when the switcher pMOS or nMOS transistor is on, commutation loss due to the pMOS nonzero turn-on and turn-off time, and, finally, the power consumption of the switch drivers. The conduction loss due to the MOS transistors is approximately

$$\text{P}_{\text{lossMOS}} \approx D\overline{I_{\text{sw}}}^2 R_{\text{PMOS}} + (1-D)\overline{I_{\text{sw}}}^2 R_{\text{NMOS}}. \tag{7}$$

This illustrates the importance of low-series resistance in the pMOS and nMOS devices; in fact, the pMOS device is sized to be $2\ \text{cm} \times 0.4\ \mu\text{m}$ and the nMOS device is $0.7\ \text{cm} \times 0.4\ \mu\text{m}$ in order to keep the loss minimal with an average switching current of up to 0.5 A.

The commutation loss due to the pMOS and nMOS nonzero turn-on and turn-off time is

$$P_{\text{comm\_loss}} = I_{\text{on}} \cdot V_{\text{off}} \cdot (t_{\text{on}} + t_{\text{off}}) \cdot f_{\text{sw\_ave}}/\alpha \tag{8}$$

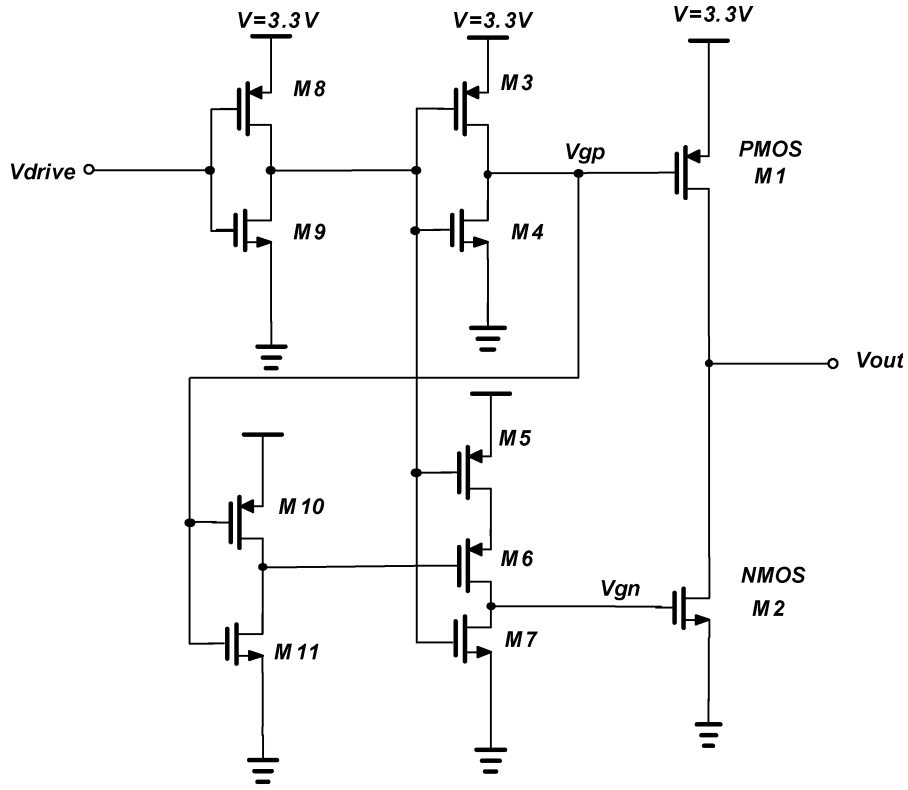

Fig. 4. Simplified schematic of the switch stage and switch driver. Since M1 is much larger than M2, M2 turns on much faster than M1 turns off. To prevent the shoot-through current, a delay is introduced by inverters M10–M11 and a NAND M5–M7. The NAND gate prevents the shoot-through current when M2 turns off and M1 turns on [49].

where $f_{\mathrm{sw\_ave}}$ is the average switching frequency, t_{on} and t_{off} are the switcher turn-on and turn-off times, and α is the commutation parameter (assuming $\alpha = 2$ for the worst case [49]). Note that the power loss in the output capacitor C_{ds} is included in the commutation loss. The "shoot-through" loss due to the nMOS and pMOS devices being "on" simultaneously is minimized with the circuit shown in Fig. 4 [49].

The driver loss caused by charging and discharging the input capacitor C_{gs} and the Miller capacitor C_{gd} of the MOSFET switching devices is approximately

$$P_{\mathrm{drive\_loss}} = Q_g \cdot V_{\mathrm{gs}} \cdot f_{\mathrm{sw\_ave}} \tag{9}$$

where Q_g is the MOSFET input charge of approximately 100 pC. This expression also highlights another advantage of the relatively low switching frequency employed by this approach. With a total input capacitance of M1 and M2 of approximately 30 pF, the power loss due to this effect is close to 2 mW. The overall efficiency of the switcher stage was simulated to be 75% with a 100-mW 802.11g OFDM waveform.

IV. Measured Results

A high-efficiency common-emitter SiGe HBT two-stage PA is designed for operation on the same die as the envelope amplifier, and its schematic is shown in Fig. 5. The total emitter area of the driver stage is 400 μm^2, and the emitter area of the final stage is 1500 μm^2. Special care is taken to achieve isolation between the envelope amplifier and the PA to reduce the coupling of the envelope amplifier switching noise to the RF amplifier output, and so the two circuits are placed on separate ends of the die, with separate substrate contacts and dedicated substrate rings surrounding each circuit. If the coupling between the two amplifiers is large, the switching signal (5) can be modulated onto the output waveform, which will increase the EVM and increase the out-of-band spectrum. The input match and interstage matching circuits are implemented on-chip, but the output match is implemented off-chip using high-Q surface-mount components. The PA is implemented in 0.18-μm SiGe BiCMOS technology [51], and the HBT devices have a simulated peak f_T of 25 GHz and a $\mathrm{BV_{CEO}}$ of 6 V. The 1×4 mm^2 die is packaged in an MLF44 package as shown in Fig. 6. The measured and simulated results for the PA operated at a constant V_{cc} of 3.3 V in CW mode are shown in Fig. 7. The peak power-added efficiency (PAE) is approximately 40% at an output power of 29 dBm at 2.4 GHz. The small-signal gain is 13.8 dB.

Since the wideband ET system has a significant nonlinearity associated with the collector modulation, as well as the intrinsic nonlinearity of the amplifier, off-chip baseband digital predistortion is implemented to improve the system linearity, using a previously published approach [52]. This predistortion algorithm was implemented on a Xilinx Vertex field-programmable gate array (FPGA), and the sample rate of the modulation DAC was 250 MHz. The predistortion itself is implemented with a table-lookup (LUT) scheme, where the AM–AM and AM–PM correction coefficients are stored at output power increments of 1.0 dB. The coefficients are calculated after an initial PA training sequence. Since this digital correction was not implemented

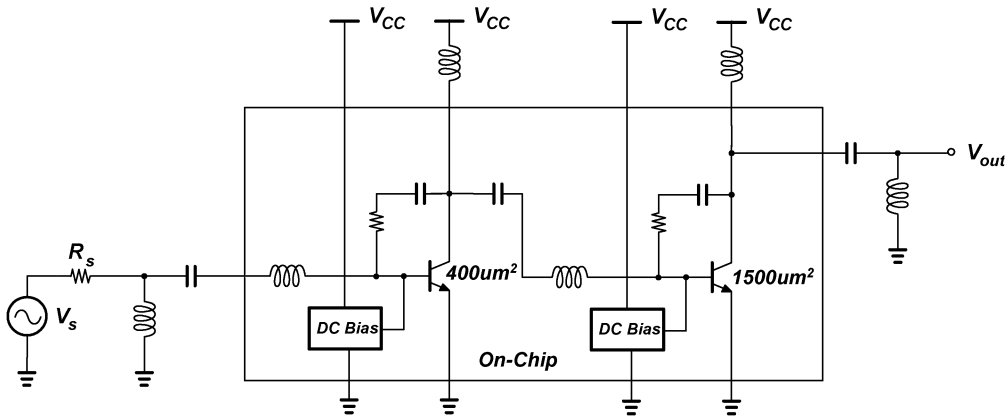

Fig. 5. Schematic of SiGe HBT 2.4-GHz PA. $\mathrm{Vcc} = 3.3$ V.

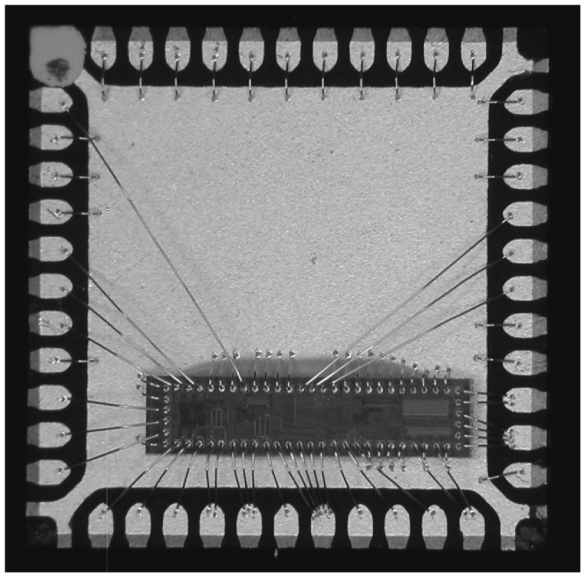

Fig. 6. Die and package photograph of SiGe BiCMOS ET PA. Chip size 1 mm $\times$ 4 mm^2.

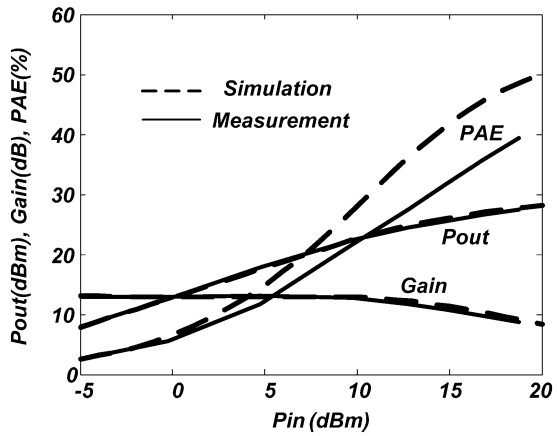

Fig. 7. Measured gain, output power, and PAE of the SiGe PA when operated in CW mode at 2.4 GHz, $\mathrm{Vcc} = 3.3$ V.

on-chip, it is difficult to estimate the additional complexity of the digital predistortion if it were implemented on-chip. As a result, we have not included the overhead associated with implementation of the digital predistortion in our efficiency calculations. However, we believe the additional complexity is relatively modest, since roughly 25 pairs of complex correction coefficients are required to perform a complete digital predistortion at a unique temperature and center frequency. Digital predistortion techniques also place a greater burden on the DAC sampling rate of the upconverter, since the upconverted signal now has to include at least three times the original signal bandwidth [52].

Fig. 8 shows a comparison of the measured AM-to-AM and AM-to-PM distortion before and after digital predistortion, clearly demonstrating the improvement in linearity that can be achieved with this technique. Note that this predistortion is implemented digitally in baseband prior to complex upconversion. The measured spectrum with and without predistortion is shown in Fig. 9, and the output signal meets the spectral regrowth mask associated with the 802.11g standard in both cases, although the predistorted case meets the mask with an improved margin.

The output of the envelope amplifier has to be "time-aligned" to the output of the RF amplifier, so that extra distortion is not created by the resulting time mismatch between the two paths. The effect of this misalignment was investigated in [17] and an alignment algorithm was proposed, which is used here. Fortunately, the wideband ET system is less sensitive to this misalignment effect than the traditional EER amplifier, and so the effect of small misalignment on EVM is negligible. Fig. 10 shows the measured time-domain output of the envelope amplifier superimposed on the measured output of the RF amplifier, and the two signals are aligned. Fig. 11 shows the detailed operation of the switcher stage in conjunction with the input and output of the envelope amplifier.

The envelope amplifier, which consists of both the switching stage and the linear stage, has an output voltage that varied from 0.3 to 3 V, operating from a 3.3-V supply. The voltage limits of the envelope amplifier are primarily determined by the on resistance of transistors M1 and M2 from Fig. 3. The peak output current supplied to the RF amplifier is 330 mA, and the op-amp quiescent current is only 5 mA. Its measured

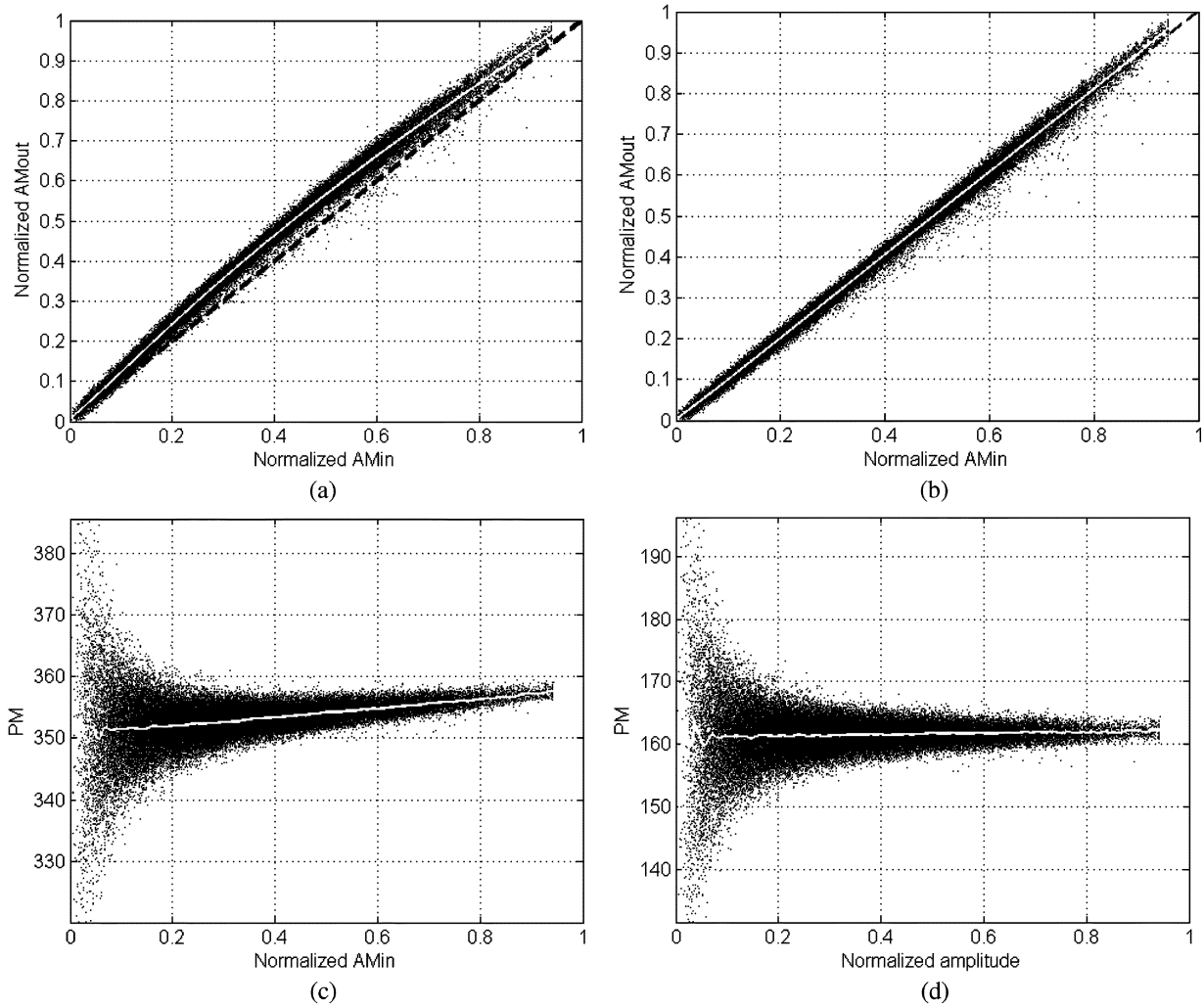

Fig. 8. (a) ET PA AM–AM before predistortion. (b) ET PA AM–AM after predistortion. (c) ET PA AM–PM before predistortion. (d) ET PA AM–PM after predistortion. Maximum PA output is 19 dBm.

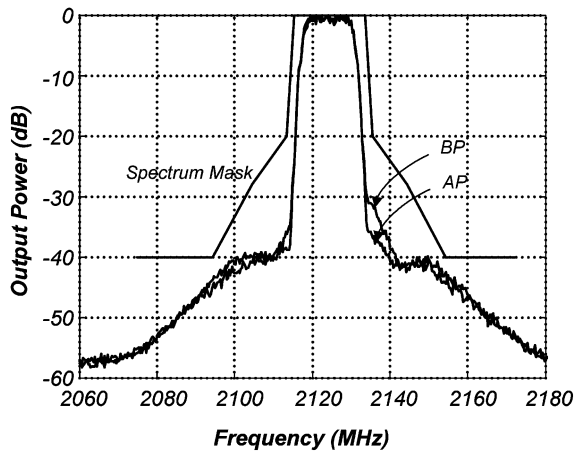

Fig. 9. Measured spectrum of output waveform before predistortion (BP) and after predistortion (AP). Both waveforms meet the spectral masks, although the predistorted waveform exhibits significantly improved EVM.

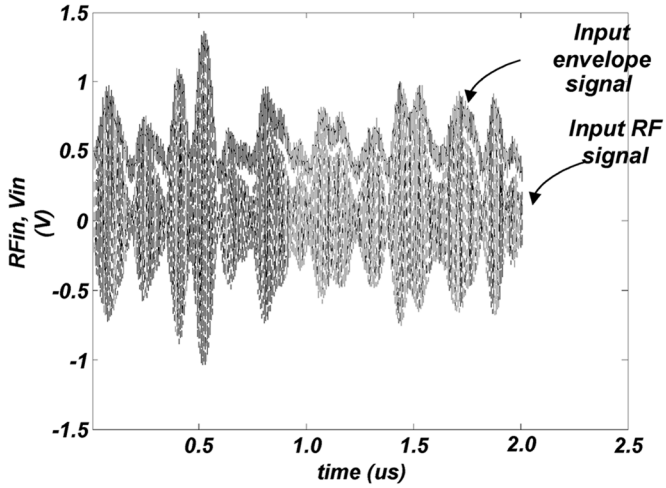

Fig. 10. Measured input RF signal and envelope signal under time-alignment condition when RF output power is 19 dBm.

bandwidth is 20 MHz, and it has an overall efficiency (envelope power out/DC power in) of 65%, at an average switching frequency of 5 MHz for a 20-dBm OFDM signal. The measured efficiency of the switch stage is 75%, and the linear stage

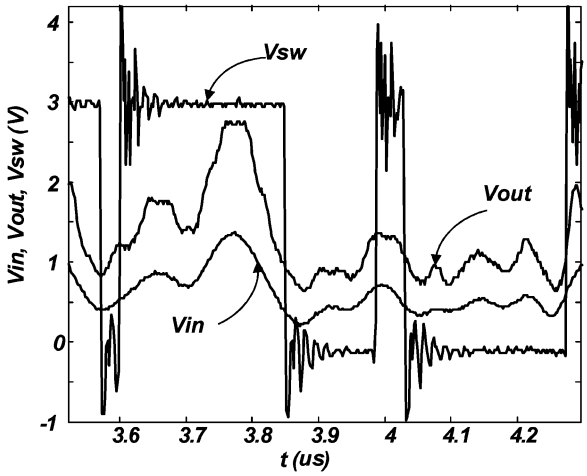

Fig. 11. Measured envelope amplifier, switch-stage control voltage, and input waveforms. The envelope signal is the amplitude of the OFDM signal. Average switching frequency is 5 MHz. Maximum Vout is 3 V.

TABLE I
ENVELOPE AMPLIFIER PERFORMANCE IN A WLAN ET SYSTEM

Supply Voltage	3.3V
Output voltage	0.3V to 3V
Current Supplied to Load	180 mA (rms) 330 mA (peak)
Quiescent Current	5mA
Output power	23.2 dBm (rms) 29.8 dBm (peak)
Bandwidth	20MHz
V_{dd} Amp efficiency	65%
Average switching frequency	5MHz
Normalized RMS error of envelope modulation voltage	3%

Note: The average switching frequency was determined by the peak of the measured spectrum of the comparator waveform.

has an efficiency of 24%. The normalized rms error of the envelope amplifier (which is determined by measuring the scaled difference between input and output with an OFDM waveform) is 3%. The rms error of the envelope amplifier increases the RF amplifier EVM, as shown in [45], but the effect is reduced in ET systems (compared with EER systems) due to the linear operation of the RF amplifier. These results are summarized in Table I.

The complete wideband ET system is measured for an 802.11g OFDM signal and a data rate of 52 Mb/s. The total PA overall efficiency (RF modulated output power/envelope amplifier DC power plus RF input power) is 28% with an EVM 5% at an output power of 20 dBm. The fully integrated version of the wideband ET system also has a thermal advantage compared with a traditional efficient linear amplifier, since the (lower) overall DC power dissipation is *split* between the envelope amplifier and the RF amplifier, reducing the temperature rise significantly. A plot of EVM as a function of output power

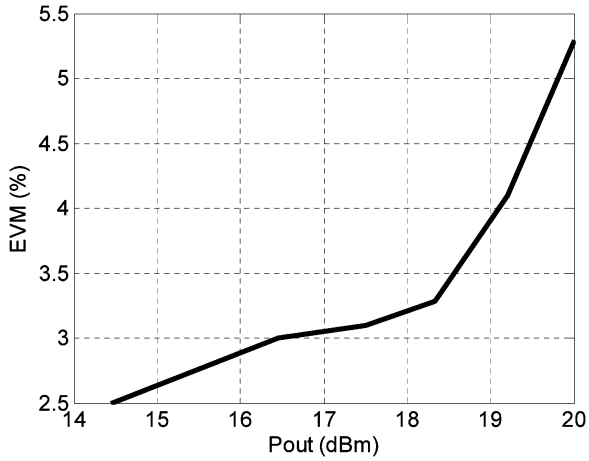

Fig. 12. Measured EVM as a function of output power for the wideband ET amplifier.

TABLE II
COMPARISON OF WIDEBAND ET PA AND CONSTANT BIAS PA WITH OFDM SIGNAL

	ET PA	3.3V PA
Pout	20dBm (100mW)	20dBm (100mW)
Gain	11dB	13.7dB
Overall efficiency	28%	19%
EVM	5%	5%

Note: The required EVM is 5% by 802.11 specifications.
Overall efficiency = RF modulated output power/final stage DC power + RF input power.
Digital predistortion is implemented to both an ET PA and a 3.3-V PA to achieve 5% EVM.

is shown in Fig. 12. Table II summarizes the performance of the wideband ET amplifier along with a comparison with the PA above operated with a *fixed* 3.3-V power supply. Note that the efficiency of the amplifier operated in this more traditional mode is also quite high (roughly 19%) thanks to the same digital predistortion system used in both cases. Note also that the gain of the fixed-supply amplifier is higher than that of the wideband ET amplifier (13.7 dB instead of 11 dB). This is a common feature of supply modulated amplifiers and is a result of the gain compression of the ET RF amplifier at low supply voltages. This particular implementation of the wideband ET system, with the modified LCDM envelope amplifier, generates negligible switching noise at the output of the RF amplifier, as shown in Fig. 9, since the switching noise is within the bandwidth of the linear amplifier and the RF amplifier does not enter saturation during normal operation. The measured PA efficiency was also enhanced by the use of a PAR "crest factor reduction" algorithm (see, for example, [53]), which reduced the PAR of the waveform from 12–14 dB to 8–10 dB. This crest factor reduction is a common feature in OFDM baseband processing to reduce the PAR of the transmitted waveform without excessively increasing the EVM.

V. Conclusion

A monolithic wideband high-efficiency ET PA, employing a high-efficiency envelope amplifier, is designed and implemented for WLAN 802.11g applications in a SiGe BiCMOS technology. A highly efficient wideband envelope amplifier is designed for wideband ET applications. The measured efficiency of the wideband envelope amplifier is approximately 65% for a WLAN OFDM envelope signal. The overall PAE of the amplifier (including the envelope amplifier and the RF PA, but not including digital circuit power consumption relating to the baseband predistortion and time-alignment or the envelope amplifier DAC) is 28% at 20 dBm (100 mW) output power. Digital predistortion is implemented to reduce the EVM of the amplifier. The measured results demonstrate that high efficiencies can be obtained in a wideband OFDM amplifier implemented in monolithic silicon technology.

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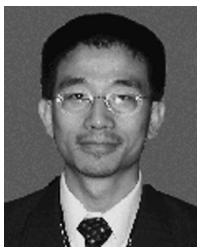

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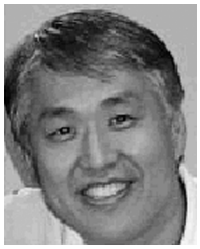

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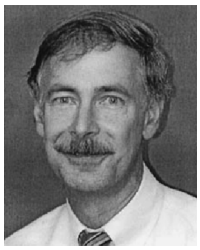

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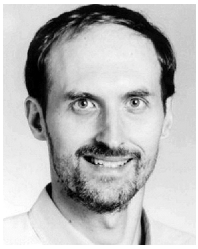

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