A Triple-Power-Mode Digital Polar CMOS RF Power Amplifier With LO Duty Cycle Control

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***Abstract*—A triple-power-mode digital polar CMOS power amplifier (DPA) with a high dynamic range is presented. The triple-power-mode to enhance the efficiency when operating under back-off power is facilitated by the combination of a switched output transformer to change the load impedance and a reduced duty cycle of the LO input signal of the DPA for additional back-off power. This static power-mode method for the low-power region can be used with a DPA which has a high dynamic range in conjunction with a digitally controlled bias generator. An improvement in the PAE from 14.5% to 28.7% is achieved at a back-off power of 6.5 dB from a peak output power of 21.54 dBm at 1.7 GHz. A digital transmit power control (TPC) range of 68.2 dB for WCDMA is realized without any external components.**

***Index Terms*—CMOS RF power amplifier, digital polar power amplifier, high dynamic range, LO duty cycle control, transmit power control, triple power mode.**

I. Introduction

WHILE modern telecommunication standards are required to transfer signals with a high peak-to-average ratio (PAPR) for high-speed data, CMOS PAs have been extensively researched in an effort to improve the back-off power efficiency and provide a high level of integration. As part of this trend, RF-DAC-type digital polar CMOS power amplifiers (DPAs) [1]–[5] have received attention as one of the most promising alternatives due to their higher efficiency and flexibility for multiple modes and multiple bands. DPAs, which have an array of switching-mode sub-amplifiers, utilize digital amplitude modulation for the RF envelope with a phase-modulated LO signal.

Load modulation method [1], [2] has been adapted for DPAs to enhance the back-off efficiency while using a part of the amplitude control bits in the low-power region. However, it is difficult to have a multiple efficiency boosting at low power with the method due to a high-order output-matching network. The limited amplitude resolution at a low power region can also directly affect the linearity of the digital amplitude modulation. Although a Class-G technique can be used for a greater improvement in the power efficiency, fully utilizing the amplitude resolution of DPAs [3], [4], this approach inevitably requires multiple supply voltages with a costly DC-DC converter.

In this letter, a static controlled triple-power-mode technique for DPAs is presented using a combination of load impedance transformation with a switched transformer [2] and a reduced duty cycle of a square-wave LO input signal without the assistance of additional components. Moreover, the proposed DPA allows the full utilization of the amplitude resolution regardless of the power mode by means of a DPA core with a high-dynamic-range [5].

II. Implementation

A schematic of the implemented DPA is shown in Fig. 1. The dual-mode switched output transformer [2] is integrated with the high-dynamic-range DPA core [5], previously proposed by the authors, for output load impedance transformation between the high-power mode (HPM) and the medium- and low-power mode (M/LPM). The DPA core has an input DC bias circuit which determines the duty cycle of the LO signal for the triple-power mode. The array of the RF-DAC-type DPA for the digital amplitude modulation has a segmented composition of 78 sub-amplifiers for a 10-bit amplitude resolution and a bias generator with an 8-bit bias control word (BCW) for digital transmit power control (TPC). LO leakage cancellation structures including a double-balanced LO leakage canceller and LO leakage virtual grounds, are introduced in each of the sub-amplifiers and in the output-power combining network to ensure very low LO leakage. The output voltage of the digitally controlled bias generator is used as the gate bias of each sub-amplifier to realize a 6 dB output power step per BCW bit.

Fig. 2(a) shows the results of a load pull analysis of the DPA for maximum output power and efficiency and the load impedance trajectories of a switched transformer for the HPM and the MPM/LPM. The optimal impedances of the peak output power and the PAE deviate from each other. Because larger series inductance for the matching network is required for the peak PAE as compared to that for the peak output power, it is possible to improve the efficiency under the back-off power by means of output load impedance transformation. In this way, the output impedance is initially optimized to ensure maximum peak output power in the high-power mode (HPM), and it is modified to have high peak efficiency at the 3 dB back-off output power using a switched transformer in the medium-power mode (MPM). Additionally, by moderately reducing the duty cycle of the LO input signal with a simple bias circuit, it becomes possible to lower the output power while also maintaining the efficiency by remaining close to a zero-voltage-switching (ZVS) condition [6], [7]. When an LO input signal with a 35% duty cycle is applied for the low-power mode (LPM), the optimal impedance rarely deviates from that of the MPM and the PAE is maintained while providing an additional output power reduction of 3 dB as shown in Fig. 2(b).

Manuscript received January 2, 2016; revised April 24, 2016; accepted June 7, 2016. Date of publication August 26, 2016; date of current version September 1, 2016. This work was supported by the National Research Foundation of Korea (NRF), by the Korea government Ministry of Education, Science and Technology (MEST) under Grant 2014R1A2A1A01004954, and by the IC Design Education Center (IDEC).

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Digital Object Identifier 10.1109/LMWC.2016.2597187

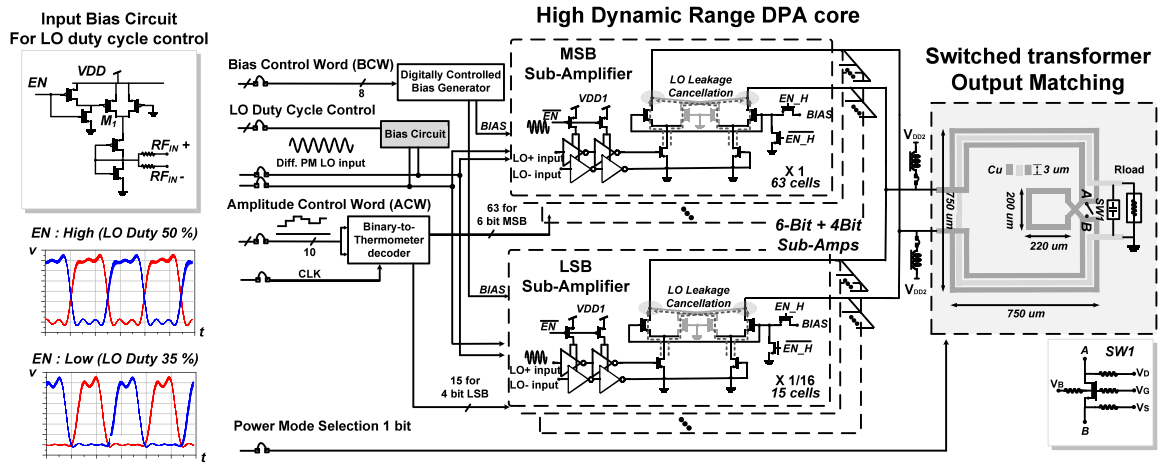

Fig. 1. Block diagram of the proposed triple-power-mode DPA with a high dynamic range. The three modes are implemented by introducing a LO-duty-cycle control circuit and a switched output transformer.

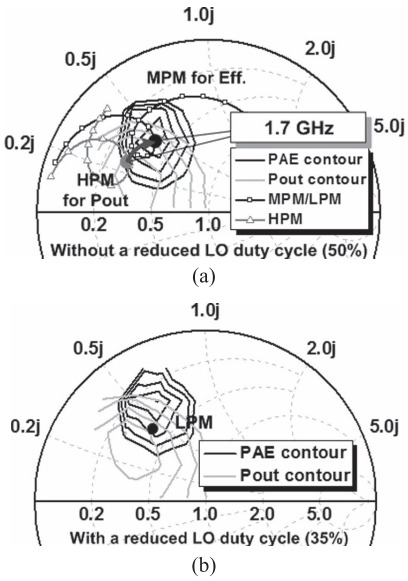

Fig. 2. Load pull analysis of the DPA for the triple power mode and load impedance trajectories of a switched transformer for the (a) HPM/MPM (b) LPM.

TABLE I
OPERATION OF THE SWITCHED TRANSFORMER AND LO BIAS CIRCUIT FOR TRIPLE-POWER MODE

Power Mode	*Switched TLT*	*EN for LO bias circuit*
HPM	HPM (ON)	High (50-% Duty cycle)
MPM	M/LPM (OFF)	High (50-% Duty cycle)
LPM	M/LPM (OFF)	Low (35-% Duty cycle)

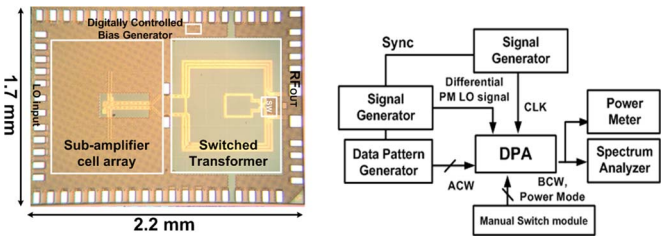

Fig. 3. Chip photograph and measurement setup.

If the duty cycle is narrower than 35%, an output-matching network is required for further impedance transformation. It should be noted that these power modes are statically switched

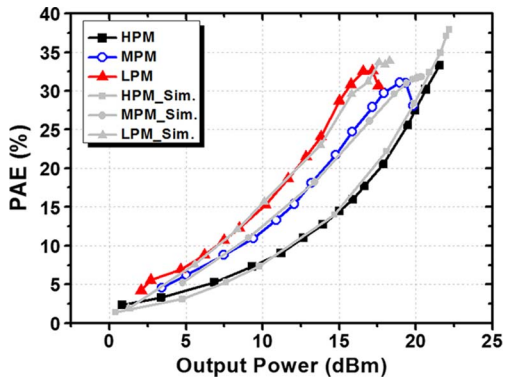

Fig. 4. Measured PAE versus output power with triple-power mode (single-tone input $f_{\mathrm{RF}} = 1.7$ GHz).

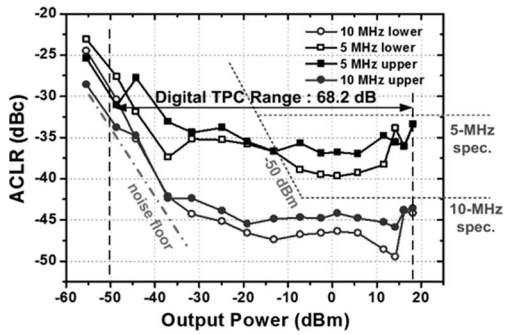

Fig. 5. Measured ACLR versus output power with bias control using the BCW at 1.7 GHz.

in this work. Mode switching can be dynamically applied considering the distortion from the transition time and the different amounts of AM/PM distortion among the modes. Since the amplitude linearity of a DPA is mainly affected by the amplitude resolution, it is advantageous to use this scheme regardless of the ACW (Amplitude Control Word) while fully utilizing the implemented 10-bit ACW resolution in the low-power region. This triple-power-mode scheme can also be widely applied in other switching PAs to improve the back-off efficiency without the requirement of multi-level supply voltages. The switched transformer [2], which serves to reconfigure the primary inductance, is implemented as shown in Fig. 1. The matching impedance is retransformed by the switch SW_1,

TABLE II
COMPARISON WITH OTHER PAS FOR EFFICIENCY ENHANCEMENT AT POWER BACK OFF

Ref.	Freq. [GHz]	Amp. Reso. [bit]	Supp. (V)	Peak P_{out}/Eff. [dBm/%]	η Improvement at -6 / -12 dB PBO	Avg. P_{out}/Eff. [dBm/%]	Mod.	Digital Tx Power Control [dB]	PA core Architect.	Method for Efficiency improvement at PBO	CMOS Tech.
[1]	2.2	8	1.2	23.3 / 43 (DE)	x 1.5 / 1.4	16.8 / 24.5 (DE)	802.11g WLAN	-	Digital	Transformer-based dynamic load modulation	65-nm
[8]	1.8	-	3.3	27.2/30 (PAE)	x 1.5 / 1.2	24.8 / 24 21.3 / 18	WCDMA/ LTE	-	Analog	Supply-path switching	65-nm
[3]	2.15	7	1.4 / 2.8	24.3/44 (PAE)	x 1.7 / 1.6	16.8/33	802.11g WLAN	-	Digital	Class-G Supply switching	65-nm
[4]	3.71	10	3 / 1.2	26.7/40.2 (DE)	x 1.8 / 2.6	20.8/28.8 (DE)	1 MSym/s 16-QAM	-	Digital	Digital Doherty + Class-G with a half supply voltage	65-nm
[9]	2.4	-	2.4	31.6/49.2 (DE)	x 1.8 / 1.8(9dB)	25.6/32.9 (DE)	LTE / 802.11g WLAN		Out-phasing	Multi-level Outphasing	45-nm
This work	1.7	10	1.2 / 2.5	21.5 / 33.3 (PAE)	x 2 / 1.8	18.2 / 21.2 (PAE)	WCDMA	68.2	Digital	Switched transformer + Reduced LO duty ratio	65-nm

located at the virtual ground of the primary side, as plotted on the Smith chart shown in Fig. 2(a). The switch is turned on and has a low inductance value on the primary side for the HPM, and the switch is turned off and has a high value for the M/LPM. The insertion losses are 1.76 dB and 1.87 dB for the HPM and M/LPM, respectively. The LO input bias circuit as shown in Fig. 1, can determine the LO duty cycle by means of bias voltage control with the transistor M_1 using the enable signal (EN). While converting the sinusoidal LO signal to the square waveform, the threshold level of the inverter of each sub-amplifier can be adjusted by the input bias voltage. The states of the switched transformer and the LO bias circuit for the triple-power mode are summarized for triple-power-mode in Table I.

III. MEASUREMENT RESULTS

This chip was fabricated in the 65-nm RF CMOS process, as shown Fig. 3. It occupies an area of 3.74 mm^2 including all of the pads. Supply voltages of 1.2 V and 2.5 V are used for the digital circuitry and RF circuitry, respectively. Fig. 4 shows the power-added efficiency (PAE) versus the output power of the DPA with the triple-power mode. LO input power of 8 dBm is applied. The peak output power, including all of the losses of the matching network, is 21.54 dBm with a PAE of 33.3% for the HPM. The PAEs of the MPM and LPM are maintained as they are for the HPM. The peak output powers of the MPM and LPM are 19.34 and 16.59 dBm with 2.2 and 4.59 dB of back-off power from the peak output power of the HPM with peak PAEs of 31.1% and 32.6%, respectively. Consequently, The LPM offers a relative PAE improvement of 97% at a back-off output power of 6.5 dB. The proposed DPA is tested with a 3GPP WCDMA signal to verify the dynamic digital modulation and its digital TPC range. The sampling frequency of AM and PM baseband signals is 92.16 MHz. Fig. 5 shows the measured ACLRs at 5 MHz and 10 MHz offsets with respect to the BCW. Static digital pre-distortion is adapted for each BCW state. Maximum linear output power levels of 18.2, 16.1, and 14.2 dBm are achieved with PAEs of 21.2, 21.4 and 22.7% for the HPM, MPM and LPM, respectively, with the maximum BCW state for WCDMA. For low power consumption, the LPM scheme is utilized with the BCW at an output power of less than 14.2 dBm. A digital TPC range of 68.2 dB from -50 dBm to 18.2 dBm is achieved using only digital controls while providing a root mean square (rms) error vector magnitude (EVM) of less than 5% throughout the range without any external components. The measured performance of the proposed DPA is summarized and compared to that of the other state-of-the-art CMOS PAs in Table II.

IV. CONCLUSION

This letter presents a triple-power-mode high-dynamic-range DPA to enhance the back-off efficiency without multi-level supply voltages. The amplitude resolution can be fully utilized in the low-power region. An improvement in the PAE from 14.5% to 28.7% is achieved at a back-off output power of 6.5 dB. A digital TPC range of 68.2 dB is achieved for WCDMA without any external components.

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