Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications

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***Abstract*—This paper discusses and illustrates the key device design issues for SiGe BiCMOS HBTs suitable for wireless power amplifier (PA) applications. Experimental results addressing ruggedness, ac performance, and safe operating area for high-breakdown SiGe HBTs built in several generations of BiCMOS technology are presented. Implications of recent high-performance SiGe HBT scaling achievements for BiCMOS technologies targeting wireless PA applications are considered. Circuit results for GSM, PCS, GPRS, and EDGE front-end modules have been obtained. A one-chip solution is demonstrated, including control circuitry and switching functionality, that supports all GPRS, PCS, and EDGE modes featuring output power at 33.8 dBm and overall power added efficiency of 37% withstanding voltage standing wave ratio conditions of 15:1.**

***Index Terms*—BiCMOS, HBTs, SiGe, silicon-germanium technology, wireless power amplifiers.**

I. Introduction

POWER AMPLIFIERs (PAs) are key components in the wireless communications industry, which is rapidly evolving in both architecture and communication protocols [1], [2]. The general PA design trend focuses on the whole system architecture and, by adopting the chip-partitioning strategy best suited for the particular radio architecture, realizes advantages in terms of performance, cost, and size. The requirements on the ability to integrate additional functional analog and digital blocks onto the same PA chip are becoming increasingly important.

Several device technologies have found use in the PA field. Historically, gated field-effect structures such as MOS and MESFET structures have found widespread use but, due to higher gain and current density at the frequencies employed, bipolar transistors have evolved as the preferred choice. GaAs HBTs have dominated such applications, however, bandgap-engineered SiGe heterostructure bipolar transistors (HBTs) are an emerging alternative due to their ability to provide high integration and to reduce cost. Further, SiGe has several advantages over GaAs for PA applications

1) Chip area is reduced and chip robustness is facilitated by the heat-conductive silicon substrate.
2) Circuit design issues arising from thermal runaway are minimized by the temperature-insensitive current–gain behavior of SiGe HBTs.
3) Well-characterized reliability at high current densities enables further reduction in device size.

The challenge faced by SiGe-based PA technologies is providing sufficient high-voltage immunity without compromising device performance. While less publicized than recent high-speed performance gains, advances have indeed been made in the design and characterization of SiGe HBTs with the requisite combination of performance and ruggedness required for wireless PA applications. Further, device-design experience indicates significant opportunity for continuous expansion of the SiGe HBT ruggedness–speed envelope through technology scaling. Technology scaling also provides opportunities to reduce process complexity while maintaining the required level of device performance.

II. SiGe HBT Device Design for PA Applications

A. Overview

Silicon-germanium technology development has pursued three directions with respect to HBT device design: 1) very high-speed low-power devices for wired and optical applications [3]; 2) relatively high-performance technologies with reduced process complexity [4]; 3) devices for wireless PA applications [5].

For wireless PA applications, SiGe HBT device design is constrained by the performance tradeoff defined by the well-known Johnson Limit, which states that, due to material limitations in carrier velocity and avalanche generation, the product of current–gain cutoff frequency f_T and open-base breakdown voltage $\mathrm{BV_{ceo}}$ should be relatively constant. While the Johnson Limit is a useful concept, it can be misleading in several respects [6]: Emitter-open breakdown $\mathrm{BV_{cbo}}$ and collector breakdown with the base grounded through a resistance $\mathrm{BV_{cer}}$ are becoming accepted as more useful indicators of device ruggedness than $\mathrm{BV_{ceo}}$ for PA applications, as it has been shown that SiGe HBTs can operate at collector voltages significantly above $\mathrm{BV_{ceo}}$ [5]–[7]. Indeed, as shown in Fig. 1, which plots the PA voltage standing wave ratio (VSWR) tolerance versus $\mathrm{BV_{cbo}}$ for a wide range of HBT process splits in a SiGe BiCMOS technology, $\mathrm{BV_{cbo}}$ can be directly related to standard PA robustness figures of merit. Further, power–gain cutoff frequency f_{MAX} is as useful a figure of merit of bandwidth as f_T for wireless PA application, and SiGe HBT device physics do not demand a rigid

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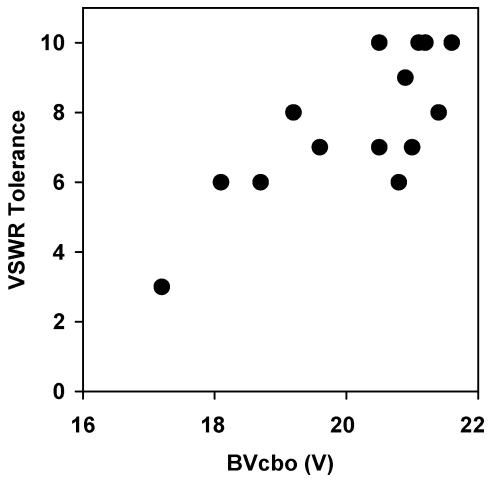

Fig. 1. PA VSWR tolerance at rated output power for process splits in a 0.5-μm SiGe HBT technology. Results show that the dc parameter $\mathrm{BV_{cbo}}$ is a useful metric for predicting device ruggedness in PA applications. PAs tested at $\mathrm{Vc} = 3.5$ V, $P_{\mathrm{out}} = 35$ dBm and $f = 900$ MHz.

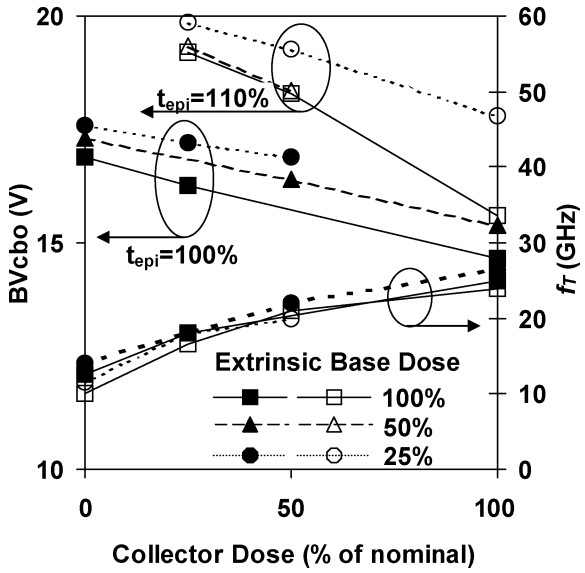

Fig. 2. Experimental results showing SiGe HBT device sensitivity in a 0.5-μm generation BiCMOS process. The experiment indicates that BVcbo, an important measure of device ruggedness, can be modified significantly without perturbing f_T.

tradeoff between $\mathrm{BV_{cbo}}$ or $\mathrm{BV_{cer}}$ and f_{MAX}, implying significant device optimization opportunities with respect to wireless PA applications. Thus, while $\mathrm{BV_{ceo}}$ and f_T provide a convenient metric to characterize SiGe HBT ruggedness and speed, they do not define the device performance boundaries for PA applications.

B. SiGe HBT Device Engineering for Ruggedness and Speed

The SiGe HBT performance–ruggedness tradeoff has been addressed primarily through collector engineering. Modern silicon process technology makes this a large design space. Collector design in state-of-the-art SiGe HBTs is characterized by: 1) a thickness composed of epitaxially grown silicon above; 2) a heavily doped subcollector with a doping profile defined by 3) one or more implants before, during, or after the growth of the SiGe epitaxial region.

The opportunities for HBT device optimization are illustrated in Fig. 2, which plots the experimental results from a 0.5-μm BiCMOS technology. In this experiment, a single collector implant prior to the collector and SiGe epitaxial layer growth was varied, along with the extrinsic base dose and collector epitaxial layer thickness. The $f_T * \mathrm{BV_{ceo}}$ product was observed to be essentially constant across all splits. f_T, dominated by base pushout in this device, is monotonic with respect to collector implant dose and relatively insensitive to collector epitaxial layer thickness or extrinsic base dose. However, $\mathrm{BV_{cbo}}$ is observed to be quite sensitive to both the collector epitaxial layer thickness and the extrinsic base dose, as well as the collector implant dose. Thus, Fig. 2 indicates that devices with a wide range of $\mathrm{BV_{cbo}}$ values can be specified for a given value of f_T. These results show that modern silicon process technology provides sufficient device engineering levers to allow that PA-relevant SiGe HBT performance to avoid being rigidly constrained to trading bandwidth for ruggedness.

The experimental results shown in Fig. 2 indicate that, in this device, the doping levels at the collector and extrinsic base junction determine device ruggedness, characterized by $\mathrm{BV_{cbo}}$. Additional collector dopant, added to raise f_T by delaying base push out, degraded $\mathrm{BV_{cbo}}$. Alternative collector implants in terms of dose, energy, and species were analyzed through process and device simulation [8], which indicated that a multiple collector-implant process could delay base push-out, the most important factor in setting the f_T of the device, without interacting strongly with the extrinsic base and thus degrading device breakdown. The results of an experiment based on this analysis are shown in Fig. 3. Over the range of collector implant dose analyzed, an implant dose window was identified over which this design goal could be achieved. Note that the experimental results plotted in Fig. 3 verify that the 25% implant dose achieved a 40% improvement in the $f_T * \mathrm{BV_{ceo}}$ product without degrading any measure of breakdown. However, further increases in collector dose degraded breakdown significantly and returned the $f_T * \mathrm{BV_{ceo}}$ product to the value of the single-implant device. Figs. 2 and 3 demonstrate the significant opportunity to engineer SiGe HBT performance that silicon process technology provides, despite the rigid ruggedness/performance tradeoff implied by the Johnson Limit.

III. SiGe HBT Device Operation

The breakdown voltages $f_T * \mathrm{BV_{cbo}}$ and $f_T * \mathrm{BV_{ceo}}$ are essentially off-state measurements. Characterizing device ruggedness for the hostile environments that characterize PA applications requires understanding the robustness of devices in their expected active operating regimes. Under such conditions, SiGe HBTs are found to show excellent thermal stability relative to GaAs HBTs. The safe operating area of these transistors is well defined and observed to provide large operating margins.

A. Thermal Stability

In Fig. 4, the desirable behavior of the current gain in the 0.5-μm SiGe BiCMOS technology is demonstrated by plotting device current gain over many decades of collector current and

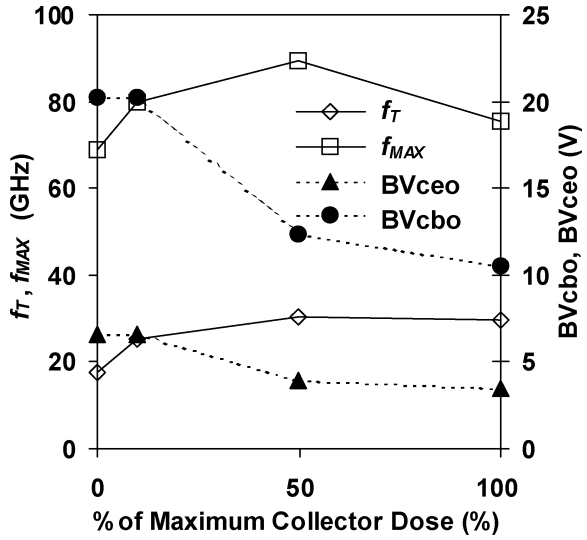

Fig. 3. Results from the experimental optimization of the ruggedness-speed tradeoff in a 0.5-μm technology generation SiGe BiCMOS HBT. The $f_T * \mathrm{BV_{ceo}}$ product of the HBT was increased by 40% without degradation in breakdown voltage by the optimal collector implant dose.

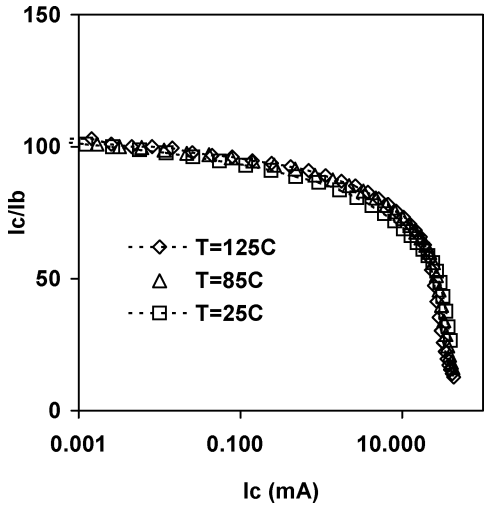

Fig. 4. Current gain versus temperature for a 0.5-μm SiGe HBT in a BiCMOS technology optimized for wireless PA applications.

over temperatures from 25 °C to 125 °C. The weak dependence of current gain with temperature at any bias indicates the stable thermal environment SiGe technology provides for PA circuit design. While temperature stable current gain is not the only thermal stability concern for PA applications, it has the important benefit of reducing or eliminating the requirement for emitter ballasting. Reduced emitter ballasting improves PA efficiency and allows reduction in the saturation voltage or the size of the output stage transistor. The thermal environment of SiGe HBTs is well understood and thus accurately incorporated into the design environment for SiGe technologies [9].

B. Safe Operating Area

The safe operation area (SOA) for SiGe HBTs will be constrained by junction breakdown at high voltages and low currents and by impact-ionization and self-heating thermal effects under high-current conditions.

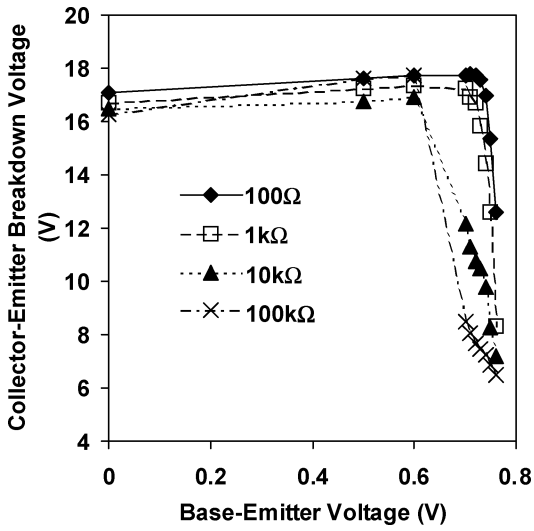

Fig. 5. Experimental breakdown characteristics of a $0.25\ \mu\mathrm{m} \times 5\ \mu\mathrm{m}$ 0.18-μm-generation BiCMOS SiGe HBT taken over a range of base-emitter bias and externally applied base resistance. The off-state breakdown voltage of the device is significantly higher than $\mathrm{BV_{ceo}} = 6$ V and close to $\mathrm{BV_{cbo}} = 18$ V over much of the V_{be} range tested.

In wireless PA applications, the relevant breakdown voltage for SiGe HBTs is $\mathrm{BV_{cer}}$, not the considerably lower $\mathrm{BV_{ceo}}$; an open circuit condition at the base is unlikely to be encountered in PA operation. SiGe HBTs show a robust tolerance for base resistance in supporting a high value of $\mathrm{BV_{cer}}$. This is demonstrated in Fig. 5, where the collector breakdown voltage of a high-breakdown SiGe HBT from a 0.18-μm technology is plotted against base-emitter voltage and with an externally applied base resistance. Collector breakdown remains close to $\mathrm{BV_{ccbo}}$ for large values of externally applied base resistance and for a wide region of V_{be} swing. The low values of intrinsic and extrinsic base resistance enable the devices to shunt large amounts of hole current, created by high values of reverse bias at the collector–base junction, away from the emitter–base junction, thus delaying the bipolar feedback mechanism that results in device breakdown.

The SOA collector voltage limit for SiGe HBTs is also a function of current drive. One approach to determining this current limit is shown in Fig. 6. The measurement consists of fixing V_{cb} and forcing emitter current until the slope of the I_e–V_{be} curve becomes infinite. This current value determines the emitter current below which the device is stable for the designated value of V_{cb}. This device instability point is driven both by self-heating and by impact ionization. The collection of these (V_{cb}, I_e) instability points defines the HBT SOA region. Fig. 7 plots this SOA region for a 0.5-μm technology SiGe HBT that has been optimized for wireless PA applications. Fig. 7 illustrates the relationship between the transistor SOA region and the expected operating conditions of the transistor by plotting the currents at which peak f_T occurs, for a range of values of V_{cb}. It is clear that the expected operating areas for the device, at or below the current at which peak f_T occurs, are well within the SOA boundary.

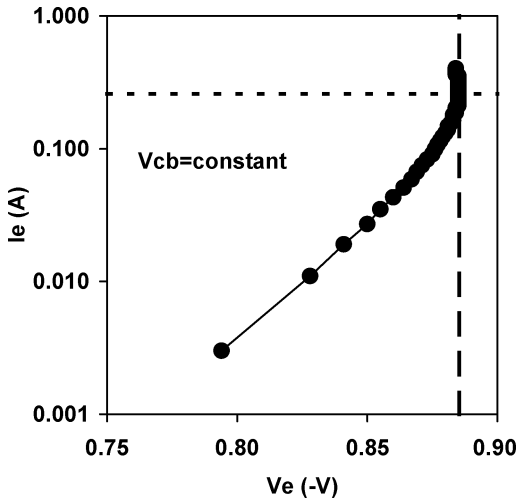

Fig. 6. Derivation of HBT instability points for determination of device SOA. The point at which the I_e–V_e curve attains a vertical slope for a fixed $V_{\rm cb}$ determines the maximum current at which the HBT can safely operate.

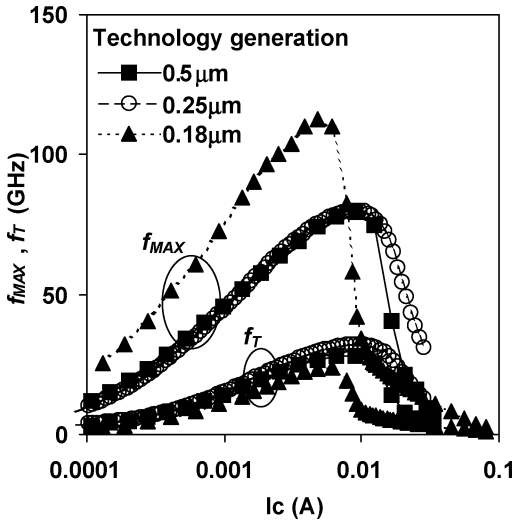

Fig. 8. AC characteristics of $2 \times 0.5\ \mu\text{m} \times 20\ \mu\text{m}$ high-breakdown SiGe HBTs at $V_{\rm cb} = 3$ V from three lithographic generations. The 0.5-, 0.25-, and 0.18-μm technology devices have a $\text{BV}_{\rm ceo}$ of 7, 5.7, and 6 V, respectively.

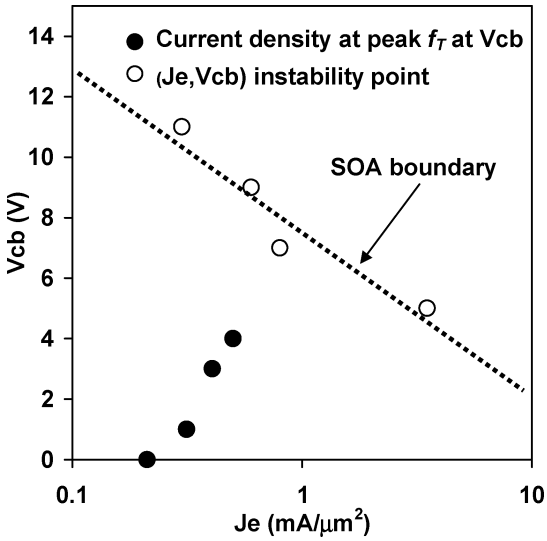

Fig. 7. On-wafer SOA analysis for a 0.5-μm technology SiGe BiCMOS HBT optimized for wireless PA application. "Device instability" indicates the operating limit due to device runaway, determined as in Fig. 6. The operating point for the device, at or below peak f_T, is well within the SOA. All operating regions of interest have collector voltage limits well above $\text{BV}_{\rm ceo} = 7$ V.

IV. Implications of SiGe HBT Device Scaling for PA Applications

SiGe HBT technology scaling progress is driven primarily by device engineering for low-power, high-speed performance [1], since the aggressive performance targets for such devices demand aggressive exploitation of both the vertical and lateral scaling capabilities of the target technology generation. f_T improvements observed in these devices arise primarily from decreased base transit time due to reduced base width and optimized Ge profiles. Full leverage of base width reduction requires both decreased collector thickness and an optimized extrinsic base process that minimizes extrinsic device parasitics. $f_{\rm MAX}$ improvements in high-speed devices arise from reduction in base resistance and base-collector capacitance. These $f_{\rm MAX}$ improvements are a result of improved lithographic tolerances, process optimization, and device architectural modifications [10].

Unfortunately, SiGe HBTs suitable for wireless PA applications do not fully benefit from high-performance HBT scaling trends because reduced intrinsic base width does not significantly improve f_T unless collector thickness is also scaled. However, Fig. 2 clearly showed that sufficient collector thickness is a critical lever in setting HBT ruggedness. This conflict implies that a very high-performance device in the same technology as an optimal device for PA applications, for which ruggedness is a critical consideration, is a problematic technology performance point, since the two device types demand the opposite trends in collector design. Therefore, SiGe BiCMOS technologies can be expected to diverge into two paths: a high-performance path with thinner collector thickness and reduced ruggedness, and a technology of the same lithographic generation containing HBTs possessing lower ac performance but higher breakdown voltages and thus ruggedness appropriate for wireless PA applications.

However, technology scaling does benefit SiGe HBTs appropriate for wireless PA applications through improved lithographic tolerances and optimized intrinsic and extrinsic base processes, both of which increase $f_{\rm MAX}$. Fig. 8 illustrates this by plotting f_T and $f_{\rm MAX}$ for high-breakdown transistors from three lithographic generations. While all three devices have approximately the same peak f_T, the 0.18-μm generation device shows a significantly higher $f_{\rm MAX}$ arising from: 1) reduced parasitic capacitances due to reduced lithographic overlay tolerances and 2) reduced base resistance due to an optimized extrinsic base process. Technology scaling has also benefited the 0.18-μm technology node shown in Fig. 8 through allowing reduced process complexity: this latest technology node requires significantly less raw process time than the 0.5-μm technology node.

Another view of this scaling trend is presented in Fig. 9, which plots the $f_T, *\text{BV}_{\rm ceo}$ and $f_{\rm MAX} * \text{BV}_{\rm ceo}$ products for

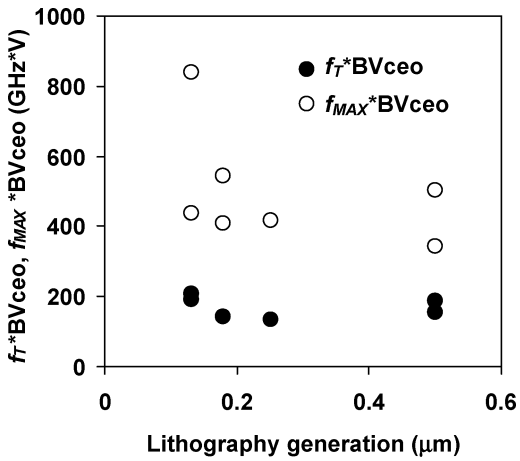

Fig. 9. Observed speed–ruggedness tradeoff for four lithographic generations of high-breakdown SiGe HBTs, from both production and experimental technologies. These results suggest that technology scaling will enhance PA device performance primarily through improvements in f_{MAX}, although improvements in the $f_{T,} * \mathrm{BV}_{\mathrm{ceo}}$ metric are observed at the 0.13-μm generation.

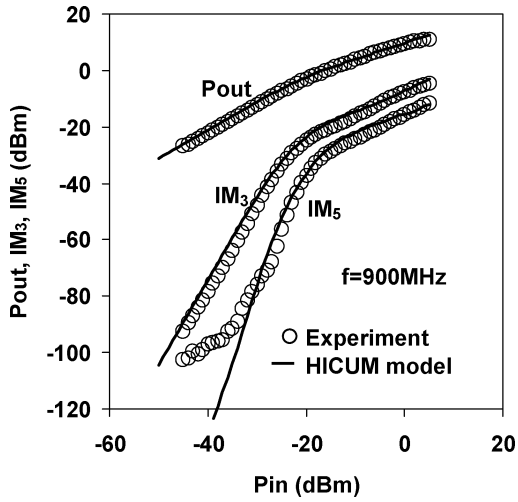

Fig. 10. Comparison between experimental PAE and intermodulation distortion characteristics for a 0.35-μm technology generation SiGe BiCMOS HBT and HICUM model extracted to fit the ac, dc, and large-signal characteristics of the device. Good correspondence between model and hardware can be observed.

high breakdown SiGe HBTs, from both high-performance and low-complexity process approaches and from lithographic generations from 0.5 to 0.13 μm. The data shown are derived from both manufactured and experimental technologies. SiGe HBT performance enhancement through technology scaling is observed primarily in power gain performance. Fully leveraging the process innovations available at the 0.13-μm technology node [10] shows significant advances in performance by both measures of the speed–ruggedness tradeoff.

V. SiGe BiCMOS Integration and Design Automation

As a CMOS derivative, SiGe BiCMOS technologies offer the advantage of high levels of integration, with a wide variety of on-chip active and passive device offerings [4], [11]. This allows the integration of bias and power control circuitry, voltage regulation, and temperature compensation to be integrated into the PA, making the PA module simpler and more cost-effective.

Because SiGe BiCMOS technologies consist of modular additions to a base CMOS technology, they inherit the design automation infrastructure required for large-scale integration [12]. Enhancements to the design infrastructure to address RF and analog circuit design issues provide the capability required to achieve first-pass success on silicon for highly integrated analog and mixed-signal designs [13]. Analog and mixed-signal integrated circuits containing millions of transistors are now commonly built in SiGe BiCMOS technology.

An important component of the SiGe BiCMOS design automation infrastructure is the HBT compact model. Significant effort over the last decade has been concentrated on the development of compact models that can accurately reproduce the range of small- and large-signal characteristics critical to successful design of complex, highly integrated analog and mixed-signal integrated circuits.

The MEXTRAM [14] and HICUM [15] models are two bipolar compact models that are finding increasing use in analog and mixed-signal circuit design environments. Fig. 10 shows the fit of the HICUM model and Fig. 11 the fit of the

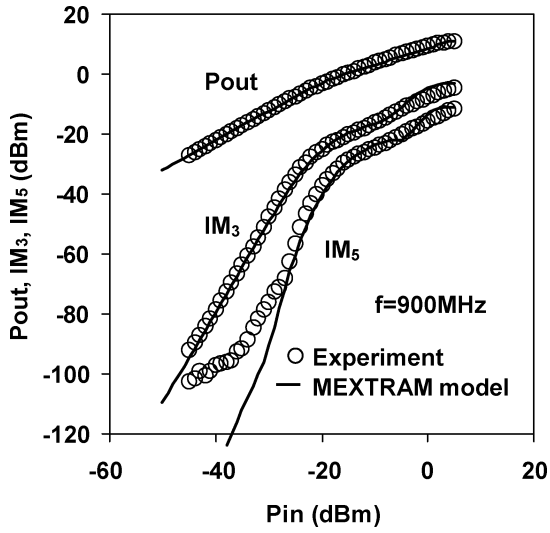

Fig. 11. Comparison between experimental PAE and intermodulation distortion characteristics for a 0.35-μm technology generation SiGe BiCMOS HBT and MEXTRAM model extracted to fit the ac, dc, and large-signal characteristics of the device. Good correspondence between model and hardware can be observed.

MEXTRAM model, to the large-signal power-added efficiency (PAE) and third-order intermodulation distortion (IM_3) and fifth-order intermodulation distortion (IM_5) of the same SiGe HBT. Excellent correspondence between model and hardware can be observed in all regions of operation. Such advanced compact models, accurately reproducing the dc, ac, and large-signal characteristics of HBTs operating in communications circuits, will significantly enhance the prospects for first-pass success on silicon for highly integrated analog and mixed-signal designs.

VI. Wireless PA Circuits in SiGe BiCMOS Technology

A. Technology Overview

The 0.5-μm SiGe BiCMOS technology discussed above supports circuit applications requiring both ruggedness and

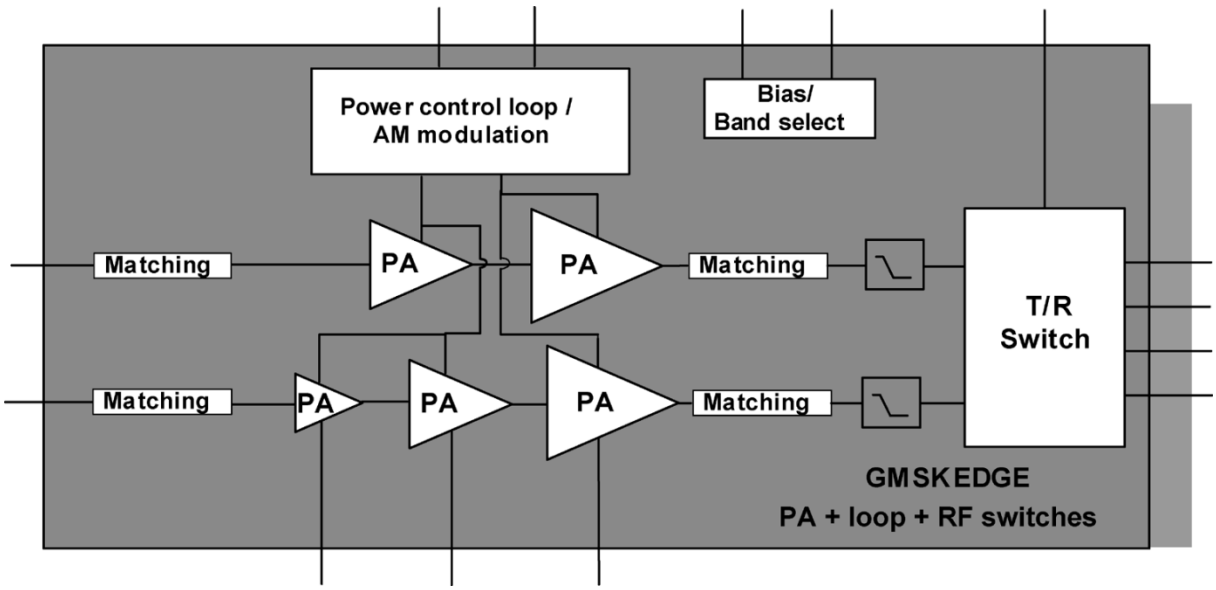

Fig. 12. Principle PA circuit schematic.

performance, achieving a $\mathrm{BV_{CBO}}$ greater than 20 V and minimum $\mathrm{BV_{CEO}}$ of 6.5 V. Fig. 8 indicates a peak $f_T/f_{\max}$ of 25 GHz/80 GHz at a collector–base voltage of 3 V. The high cutoff frequencies enable available power gain of 39 and 33 dB for the basic transistor cells at the operating frequencies around 900 and 1800 MHz, respectively.

B. Circuit Design

The output power requirements for GSM, GPRS, and EDGE are 33 dBm from the antenna. In order to provide sufficient margin for losses in antenna near components, the output from the PA should exceed 34.5 dBm. Such high output power imposes severe demands on both the voltage immunity of the output device and the thermal stability of the entire design. For the GPRS and EDGE standard, multiple-time-slot operation further increases the requirement on the thermal performance and robustness of the power amplifier. Thermal paths through standard C4-PAD:s and low-temperature-cured ceramic (LTCC) provide a very low thermal resistance. The current PA design has been demonstrated to operate at a 4× slot time-division scheme without performance degradation.

The circuit topology chosen is a single ended two- or three-stage solution with built-in biasing circuitry and power control. A principle functional description can be found in Fig. 12. Interstage matching is performed both on- and off-chip. The off-chip components are either designed directly into an LTCC substrate or mounted on top of the substrate surface. The die is mounted by means of C4 flip-chip technology onto the substrate surface, thereby providing extremely low parasitic inductance and good thermal conductivity together with a small footprint. No external components outside of the module are needed for matching or decoupling. The constant current gain as a function of temperature together with the high current density of the PA SiGe HBT technology makes it possible to make use of smaller output devices, thereby minimizing parasitic effects. The low parasitics increase the inherent gain of the devices, which together with an efficient adaptive biasing scheme can be utilized for achieving high efficiency at all output powers. The biasing scheme uses an external bias reference to set the bias (I_{cq}) in the PA to an optimum value, adapted to the power levels to minimize current consumption over the varying output power levels. A one-chip approach is adopted for a PA application addressing GPRS, PCS, and EDGE. Polar modulation is used for the EDGE mode in order to modulate both phase and amplitude with high efficiency and to obtain a direct adoption to varying output power requirements with maintained efficiency. The amplitude modulation is achieved by modulating the supply voltage of the PA kernel. The phase is modulated by the preceding TX circuitry and fed directly to the main amplifier.

The robustness requirements on the whole front-end module (FEM) can be expressed as a VSWR tolerance of 15:1 at the antenna output port. The VSWR at the PA output will be lower due to loss in the antenna switch of the FEM. VSWR at the PA in this FEM is reduced to below 5.5:1.

The FEM was tested with a VSWR of 15:1 without failure. The VSWR robustness test was performed for supply battery voltages of up to 5.5 V. During the VSWR test at high battery voltage, the reference, the power/amplitude input, to the regulator in the FEM was kept at the same value as when calibrated at a 3.6-V battery voltage, therefore the collector voltage at the PA was 3.5 V during the VSWR test. Excellent power control is achieved with on-chip PMOS, which regulates the PA collector voltage in the FEM.

For GMSK standards (e.g., GSM and GPRS), the signal envelope is constant and, as a consequence, linearity of the PA is not an issue, however, for the current polar EDGE implementation, AM(BB)-AM(RF) and AM(BB)-PM(RF) linearity is vital.

The 0.5-μm SiGe PA technology demonstrates high Early voltages even at lower collector-emitter voltages and pushes the onset of avalanche breakdown toward the higher voltage regime, thus increasing the linear region of operation for the output transistor.

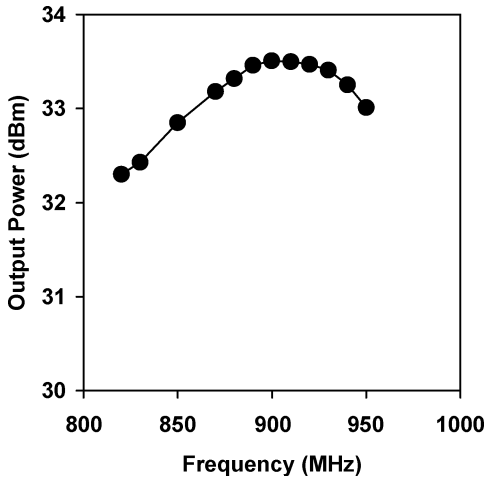

Fig. 13. Output power for the full PA module operated in the GPRS mode. The input power is 14 dBm.

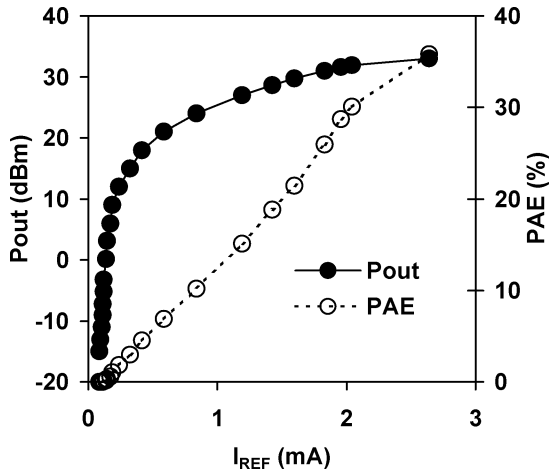

Fig. 14. GMSK PA characteristics showing output power ($P_{\rm out}$) and PAE at 900 MHz and $P_{\rm in} = 14$ dBm. High PAE is exhibited at high output power levels.

VII. Circuit and Module Performance

The circuit is built around a proven PA kernel [17], consisting of a quad-band power amplifier with two amplifier chains, depicted in Fig. 12.

One chain is designed for the frequency range 824–915 MHz, spanning output powers from 6.5 to 34.5 dBm, with an efficiency of 55% at a supply voltage of 3.5 V. The output characteristics versus frequency for the full PA module operated in low-band GPRS mode are shown in Fig. 13. The gain in each stage allows the use of only two stages for this low-band PA.

The second high-band amplifier chain consists of a three-stage PA intended for the DCS/PCS PCS frequency range 1710–1910 MHz. The output power spans from 1.5 to 31.5 dBm, showing a PAE of 45% at 31.5 dBm and a supply voltage of 3.5 V. The output power and efficiency characteristics of the PA in the GMSK mode at 900 MHz are shown in Fig. 14. Note the high PAE at higher output levels.

Concerns have been raised regarding using Si technologies in PA applications for wireless standards requiring high outputs at high efficiency and the changing load characteristic of the GSM/GPRS standards. The high breakdown voltage of the SiGe PA technology, $\rm BV_{CBO} >= 20$ V, constant current gain as a function of temperature, and Si substrate thermal conductivity significantly exceeding that of GaAs make this technology extremely well suited for applications requiring both ruggedness and high output power, such as the multiple-slot-operation GPRS standard. A fully functional test was performed into a load presenting a VSWR ratio of 15:1 at the E-GPRS module output through all phase angles at a 5.5-V supply voltage. The reference input was kept constant at a level that would give 33 dBm of output power in a 50-Ω load at 5.5-V supply voltage.

The output performance for the whole E-GPRS FEM reaches 27 dBm for EDGE-850 MHz and EDGE-900 MHz bands at a PAE of 20% including AM modulator and antenna switch losses. The lower saturation voltage in SiGe HBTs is attractive for open-loop modulation, providing increased dynamic range and efficiency at lower output levels. This design exploits the high levels of integration offered by SiGe BiCMOS technologies by incorporating both the regulator and the antenna switch on the same die as the PA engine.

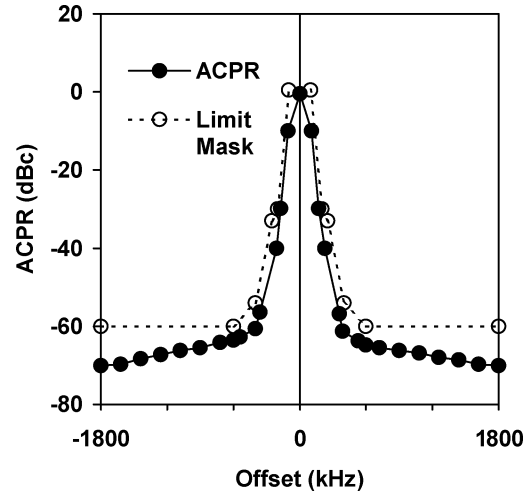

Fig. 15. Spectrum due to modulation at maximum specified output power $P_{\rm out} = 27$ dBm, $f = 910$ MHz. At this output power, the EVM is about 2.3%, indicating excellent modulation accuracy.

For the higher bands at 1710–1785 MHz and 1850–1910 MHz, respectively, output powers of 26 dBm have been demonstrated. Stability has been tested at up to VSWR 10:1 with no oscillations (< -36 dBm 3 MHz BW). Four-slot GPRS power ramping has been measured. Full ramp and spectrum mask compliance are demonstrated, indicating excellent thermal stability and signal controllability. Worst-case Rx noise performance of -87 dBm/100 kHz is demonstrated for GSM. The GSM system requirement is -79 dBm/100 kHz [16].

The linearity requirements for the EDGE mode is expressed in terms error vector magnitude (EVM), but even more stringently as a spectrum mask conformance [16]. An EVM of 2.3% has been demonstrated at the aforementioned specification compliant at maximum output powers, as shown in Figs. 15 and 16. At varying output power levels, EVM is kept at an excellent

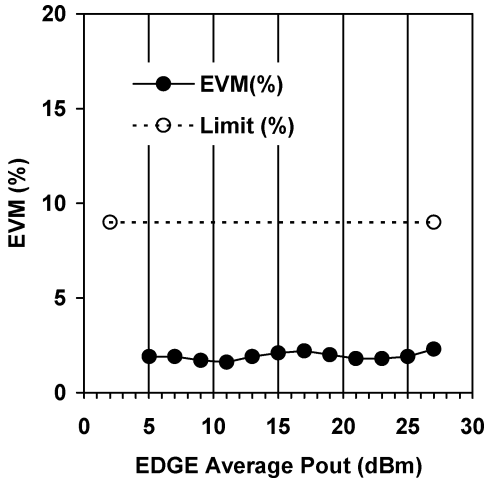

Fig. 16. Measured EVM at varying output power levels, $f = 900$ MHz.

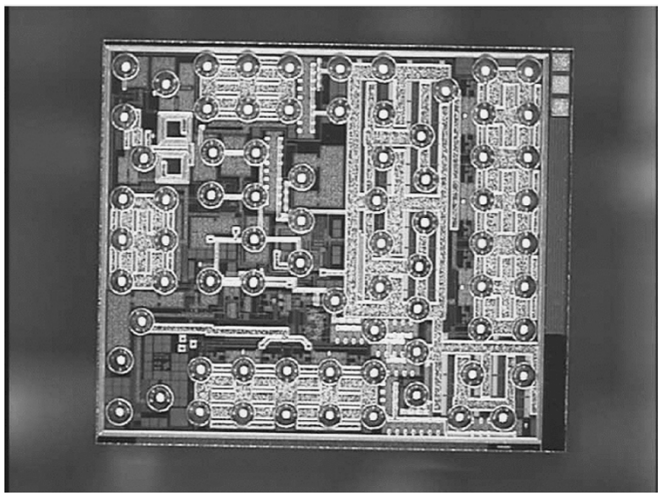

Fig. 17. EDGE FEM die, including two PAs, an antenna switch, and an AM modulator using PMOS.

margin to the limit [16] in Fig. 16. A photograph of the PA chip is shown in Fig. 17.

VIII. Conclusion

SiGe BiCMOS technology is finding increasing use in wireless PA applications. The favorable thermal properties, volume manufacturing capability, and design automation support of SiGe BiCMOS technology have long been recognized. Detailed investigation of the SOA analysis of SiGe HBTs reveals favorable device ruggedness for PA applications.

Device engineering with respect to SiGe HBT speed and ruggedness has been intensively studied. A roadmap of SiGe BiCMOS technologies targeting wireless PA applications will be constrained by the tradeoff between HBT ruggedness and speed discussed in this paper. SiGe HBTs that require high breakdown voltages will not strongly benefit from the vertical scaling trends that drive high-performance low-power HBT roadmaps due to the significant collector thickness required to support high levels of device ruggedness. Because of this, SiGe BiCMOS technologies targeting wireless PA applications will not be expected to show significant increases in f_T from generation to generation unless PA ruggedness requirements are relaxed. However, it has been shown that high-breakdown SiGe BiCMOS HBTs engineered for wireless PA applications should benefit significantly from advances in lateral scaling and new device architectures, without detriment to device ruggedness, and can therefore be expected to show a significant generational progression in performance metrics related to power gain.

PA designs have been demonstrated for GSM, GPRS, and EDGE wireless standards using a SiGe HBT technology specifically tailored to meet the divergent requirements of high VSWR robustness at high output power and high linearity. The GPRS/EDGE FEM shown here exceeds the 15:1 VSWR requirement at 33 dBm with an overall efficiency of 37%. The SiGe HBT was optimized to simultaneously provide ruggedness and speed and is compatible with the base 0.5 μm CMOS. The favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities demonstrated by these SiGe PAs make them a compelling choice for wireless applications. A SiGe BiCMOS flip-chip together with LTCC is a very strong path for PA modules. The combined module exhibits superior performance and stability together with a low component count for the entire front-end solution.

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