

Highly Linear High-Power 802.11ac/ax WLAN SiGe HBT Power Amplifiers With a Compact 2nd-Harmonic-Shorted Four-Way Transformer and a Thermally Compensating Dynamic Bias Circuit

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Abstract—This article presents the design of a highly linear high-power silicon–germanium (SiGe) heterojunction bipolar transistor (HBT) 802.11ac/ax wireless local area network (WLAN) power amplifiers (PAs). The challenges associated with electrothermal effects on the dynamic operation of WLAN PAs are first discussed. We then propose the design methods that take into account the electrothermal transient effect to improve linear output power (P_{OUT}) and dynamic error vector magnitude (DEVM). A compact four-way output transformer balun is proposed to achieve efficient power combining, and a built-in 2nd-harmonic short is demonstrated by using a novel multi-layered metallization scheme. A thermally compensating dynamic bias circuit that improves the DEVM and reduces memory effects is designed with an integrated temperature sensor. Different SiGe HBT array layouts, laterally and vertically arranged, of the output stage of the PA are also investigated. With the 802.11ac MCS9 VHT80 test signals, the DEVM of a PA with a laterally arranged output stage is lower than that of its vertical counterpart. This suggests the importance of the layout on the transistor electrothermal transient effect. The PA with the laterally arranged output stage shows a P_{OUT} of 22.5/23.6/23.2 dBm (DEVM = −35 dB) with 10.0/12.2/11.2% power-added efficiency (PAE) at 5210/5530/5855 MHz under an 802.11ac MCS9 VHT80 test signal at 50% duty cycle. Good DEVM performance was measured under the test signal with various duty cycles, indicating that the proposed PA is thermally robust. The design supports the 802.11ax MCS11 VHT80 signals with 19.4-dBm P_{OUT} , satisfying a DEVM of −40 dB.

Index Terms—802.11ac/ax, dynamic error vector magnitude (DEVM), electrothermal, error vector magnitude (EVM), heterojunction bipolar transistor (HBT), junction temperature, memory effect, power amplifier (PA), silicon–germanium (SiGe), thermal, transformer, wireless local area network (WLAN).

I. INTRODUCTION

WIRELESS local area network (WLAN) radio, supporting dense modulation schemes and massive

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multiple-input multiple-output (MIMO) techniques, is popular for high-speed spectrum-efficient mobile access. The 802.11ac WLAN standard [1] is widely deployed for indoor wireless communications due to its wide channel bandwidth of 80/160 MHz, 256 quadrature amplitude modulation (QAM), and massive MIMO capability of up to four spatial streams. All these features lead to increased data rates and expanded network capacity. As a result, the 802.11ac WLAN standard can support 780-Mbps data rates per stream.

With the advent of advanced applications, such as high-definition video streaming, Internet of Things (IoT), and augmented reality (AR)/virtual reality (VR), the demand for wireless connectivity solutions with significantly increased throughput ($\gg 1$ Gbps), higher spectral efficiency, and more network capacity is ever-growing. Efforts to deliver better designs compliant with the new 802.11ax WLAN standard, also known as sixth-generation Wi-Fi, are rapidly ramping up. The 802.11ax standard promises [2]:

- 1) 1024 QAM to increase data rates by 25% compared to 256 QAM in 802.11ac;
- 2) orthogonal frequency division multiple access (OFDMA) for a more efficient use of resources;
- 3) 8 × 8 multi-units MIMO in downlink and uplink for access points (APs) to increase network capacity; and
- 4) a longer OFDM symbol for extended coverage and increased efficiency.

These attractive features imply significant design challenges for power amplifier (PA) designers. Higher index modulation in the 802.11ax standard imposes stricter amplitude–amplitude (AM–AM) and amplitude–phase (AM–PM) distortion specifications for the 802.11ax WLAN PAs. The increased number of sub-carriers (from 234 in the 802.11ac to 980 in 802.11ax for 80 MHz channel) in OFDMA results in higher peak-to-average power ratio (PAPR), necessitating a larger power back-off (PBO) operation. The massive MIMO with multiple PAs increases the ambient temperature (T_{amb}) of a mobile unit or an AP. Moreover, the longer OFDM symbol induces error vector magnitude (EVM) degradation in the dynamic operation of WLAN PAs.

As such, the 802.11ac/ax WLAN standards require highly linear PAs that operate at a large PBO, with decreased power-added efficiency (PAE). As a result, most of the dc power will

be dissipated as heat, which leads to the junction temperature (T_J) rise in active devices that worsens several device metrics, including transconductance (g_m) and f_T/f_{MAX} of the transistor [3]. It also causes detrimental thermal memory effects and shortens the device lifetime under high-voltage stress [4].

Si-based PAs are attractive for their ease of integration with other functions and bias control compared with III-V technologies [5], [6], but their linearity can be a challenge. Several linearization schemes have been proposed by researchers: an 802.11ac/ax digitally assisted differential Doherty CMOS PA was presented in [7]; pseudo-differential 802.11ac CMOS PAs with an adaptive gate biasing were demonstrated in [8]–[10]; an 802.11n/ac inverse class-D CMOS PA with digital I/Q combining was proposed in [11]; and a 802.11ac spatially combined CMOS PA was showcased in [12]. However, the above-mentioned designs require digital pre-distortion (DPD) [13] for linear operation, which increases system-level complexity. The researchers also demonstrated a CMOS dual-band WLAN PA with wideband AM–AM envelope feedback [14] applied to the gate biasing in addition to DPD for AM–PM correction. An AM–PM compensation scheme with PMOS varactor was exploited [15] at the cost of a capacitive loading at the gate of an NMOS transistor. An 802.11ac CMOS PA with a reconfigurable inter-stage matching network [16] was demonstrated that covers the entire band from 4.9 to 5.9 GHz; however, it only supports up to 40-MHz channel bandwidth and the linear output power (P_{OUT}) of the PA is still limited. An asymmetrical parallel-combined transformer in a CMOS 802.11ac WLAN PA [17] was also proposed, but its linear P_{OUT} and PAE need improvement. Kang *et al.* [18] proposed a parallel-cascoded CMOS 802.11ac WLAN PA with an active feedback linearizer to improve AM–AM, but with a decreased power gain and PAE. To boost PAE at deep PBO, the envelope tracking [19] was adopted in external WLAN PAs. The limited bandwidth of the supply modulator, however, restricts its usage to a 40-MHz channel 802.11n MCS7 WLAN mode. Transformer-based CMOS Doherty PAs [20], [21] have been implemented for PAE enhancement at PBO, but they only support the 2.4-GHz 802.11g WLAN mode. A 5-GHz CMOS PA with a transformer-coupled envelope detector for DPD loopback and power control [22] has been realized for the 802.11ac WLAN application.

With increased complexity in DPD implementation for linear operation and inherent low breakdown voltage, CMOS would not be the ideal choice for highly linear high-power 802.11ac/ax WLAN PA designs. Silicon–germanium (SiGe) heterojunction bipolar transistors (HBTs) [23]–[25], on the other hand, are more suitable for WLAN PA development compared to CMOS, due to their higher power density, good ruggedness, better linearity, and reasonable integration capability, all with a reasonably low cost. An 802.11ac WLAN front-end IC using SiGe BiCMOS was successfully realized with full integration of a PA, an LNA, and a single-pole double-throw (switch) (SPDT) on a single Si die [26]. Another SiGe HBT PA [27] supporting both the 802.11ac/ax modes ($P_{OUT} \sim 20$ dBm) without any DPD requirement was demonstrated. A two-stage SiGe HBT PA [28] was proposed, achieving an EVM of -47 dB at 16.5-dBm P_{OUT} for the 802.11ax WLAN standard with a programmable temperature

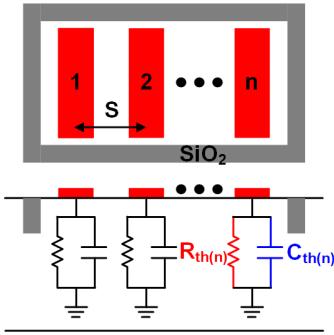


Fig. 1. Top view of a SiGe HBT array with n multi-emitter HBTs (red-colored rectangular bar) with a shared sub-collector surrounded by a SiO_2 deep trench isolation (top) and its corresponding cross section (bottom).

compensating bias circuit. The linear P_{OUT} of the state-of-the-art SiGe HBT WLAN PAs, however, is limited to 20 dBm and needs to be enhanced further to realize low-cost, high-performance 802.11ac/ax WLAN applications.

This article is an extension of our previous work [29]. More elaborate explanations of the WLAN PA design are given here, including the design of a four-way output transformer balun and a thermally compensating dynamic bias circuit with an integrated temperature sensor to improve linearity.

This article is organized as follows. Section II discusses the details of the electrothermal transient effect and its impact on the EVM of WLAN PAs. Section III describes the design details of the proposed PA with focus on the functionalities of each sub-block. Section IV explains the design procedure of passive networks, especially focused on a compact four-way 2nd-harmonic-shorted output transformer balun. Section V covers the design of a thermally compensating dynamic bias circuit and PA memory effects associated with its dynamic operation. In Section VI, the features of SiGe HBT BiCMOS technology utilized in the design are specified and the design of a multi-layered printed circuit board (PCB) for PA evaluation is explained. Section VII shows simulated and measured results of the two prototype PAs, and this article is concluded in Section VIII.

II. ELECTROTHERMAL TRANSIENTS IN WLAN PAs

The EVM is a key metric for WLAN PAs. Most publications have focused on improving the EVM in static conditions, where the PA operates in its thermal steady state. Actual WLAN transceiver operation, however, uses time-division duplexing (TDD), and the PA is turned off while receiving to reduce its current consumption. Thus, the PA must be turned on and off periodically with a certain duty cycle. An electrothermal transient effect associated with this dynamic PA operation which, if not properly accounted for, will cause EVM degradation [30].

In a Watt-level PA design, a SiGe HBT array of shared sub-collector HBTs with multiple emitter stripes is preferred over an array of individual single-emitter SiGe HBTs for smaller silicon real-estate and lower interconnect parasitics. The compactness of the multi-finger SiGe HBT array, however, also leads to increased mutual thermal coupling among devices, as well as self-heating of each SiGe HBT [31]. A simplified top view of a SiGe HBT array and its cross section is shown in Fig. 1. T_J of the i th npn SiGe HBT in the

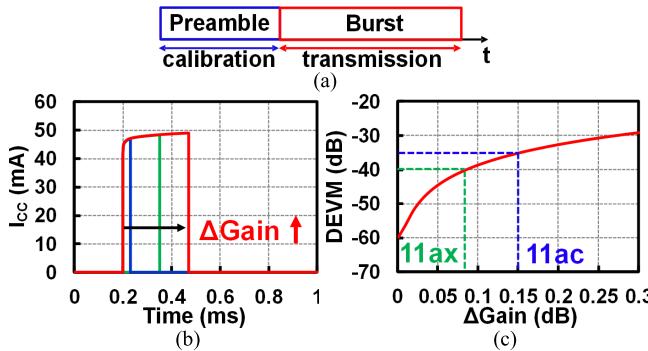


Fig. 2. (a) Simplified structure of a WLAN OFDM symbol, (b) pulsed collector current of a WLAN PA under variable burst length, and (c) minimum EVM floor determined by the gain error.

array can be expressed as follows:

$$T_{J(i)} = T_{\text{amb}} + R_{\text{th}(i,i)} P_{d(i)} + \sum_{j=1, j \neq i}^n R_{\text{th}(i,j)} P_{d(j)} \quad (1)$$

where T_{amb} is an ambient temperature of the SiGe HBT array, $R_{\text{th}(i,i)}$ is a thermal resistance of the i th SiGe HBT under self-heating, $R_{\text{th}(i,j)}$ is the mutual thermal resistance between the i th and j th SiGe HBTs, and $P_{d(i)}$ and $P_{d(j)}$ are powers dissipated as heat by the i th and j th HBTs, respectively. With a $T_{J(i)}$ increase, the current gain β and f_T/f_{MAX} of SiGe HBTs in the array will degrade accordingly. To mitigate these adverse effects, a variety of SiGe HBT array configurations have been proposed, such as the nonuniform spacing across emitter stripes [32], the nonuniform emitter ballasting resistors [33], and the nonuniform emitter stripe lengths [34] with increased model complexity.

Another important thermal effect to be considered in WLAN PAs is the electrothermal transient, i.e., the thermal response of the SiGe HBTs before they reach a thermal steady state. A thermal capacitance $C_{\text{th}(n)}$ is added in parallel with a thermal resistance $R_{\text{th}(n)}$ to model the electrothermal transient effects, as shown in Fig. 1. Each device can be represented by a heat source with a single-pole thermal network for simplicity, although a more realistic electrothermal model should include multi-poles for better accuracy [35]. A thermal time constant is defined as follows:

$$\tau_{\text{th}(n)} = R_{\text{th}(n)} C_{\text{th}(n)}. \quad (2)$$

$\tau_{\text{th}(n)}$ is the amount of time it takes to heat up a specified volume of a material to 63.2% of its thermal steady-state temperature. The large active area of a PA output stage increases $C_{\text{th}(n)}$ dramatically and its $\tau_{\text{th}(n)}$ can be a couple of milliseconds.

Fig. 2(a) shows a simplified WLAN symbol structure which consists of a preamble for gain calibration and a burst of data transmission. Fig. 2(b) shows the pulsed collector current of the PA with varied burst lengths and Fig. 2(c) shows the EVM versus the gain [36]. To meet the minimum EVM requirement of -35 and -40 dB, the gain error in a pulsed operation should be less than 150 and 80 m dB for the 802.11ac and 802.11ax standards, respectively. Thus, maintaining the power

gain constant in the dynamic operation of the WLAN PA is critical. For this reason, the notion of the dynamic EVM (DEVM) [30] is more relevant than the static EVM, when assessing the WLAN PA's linear performance.

III. CIRCUIT SCHEMATIC OF THE PROPOSED 802.11ac/ax WLAN PA

Fig. 3 shows a circuit schematic of the proposed SiGe HBT 802.11ac/11ax WLAN PA. It is a three-stage PA, and the total emitter areas of each stage (A_{E1} , A_{E2} , and A_{E3}) are ratioed as 1:4:18 to ensure driving capability from a previous stage to its next stage. The collector current densities of the input stage, the second stage, and the output stage are 0.160 , 0.081 , and $0.027 \text{ mA}/\mu\text{m}^2$, respectively. These bias current densities correspond to class-A, class-AB, and deep class-AB modes for the three stages to ensure good linearity while achieving high efficiency. All the SiGe HBT arrays, as shown in the top left image of Fig. 3, are composed of multiple SiGe HBTs with shared sub-collectors, each with three emitter stripes. As shown in the bottom-right table, only the output stage has an emitter width (W_E) of $1.2 \mu\text{m}$ to increase the power density of the SiGe HBT array. Through-wafer vias (TWVs) [37] with a low parasitic inductance are exploited for robust ground connections.

A thermally compensating dynamic bias circuit, consisting of a CMOS control logic, a SiGe HBT current mirror (Q_{M1} – Q_{M2}), and two diodes (Q_{REF} and Q_A), are included in the design, as shown in the bottom left inset of Fig. 3. Only the Q_{REF} , designated as S_1 , S_2 , and S_3 in the circuit schematic, is thermally coupled to the SiGe HBT arrays in their corresponding stages. These SiGe HBTs function as temperature sensors. An avalanche diode Q_A is included in the bias circuit to provide a low impedance path to bypass any avalanche current of the SiGe HBT arrays [38]. An enable pulse (EN) is applied to the PA to control the duty cycle under dynamic operation.

A compact input transformer balun is proposed for achieving equal power splitting with a 180° phase shift. An inter-stage four-way transformer was designed to generate two differential signals for driving the output stage [39]. A multi-section high-pass matching network was inserted between the second stage and the output stage to compensate for gain roll-off at the higher frequency band. Neutralization capacitors [40] C_{neu} of 0.73 pF are used at the output stage to mitigate the Miller effect. An output passive network is a parallel power combining the four-way transformer balun. The emitter ballasting resistors (R_E) and base ballasting resistors (R_B) [41] with a resistance-per-emitter area of $100 \pm 30 \Omega \cdot \mu\text{m}^2$ were inserted at the emitter and base nodes of each individual npn SiGe HBT in the arrays to prevent thermal runaway at elevated T_J . The series resistors R_{C1} and R_{C2} are utilized on supply rails of the input stage and the second stage to stabilize the PA. The staggered-RC bypass networks [42] are inserted in the supply lanes of the 2nd stage and the output stage to suppress even-mode oscillations. EMX was used for the full chip-scale 3-D EM simulation, including TWVs and bond wires.

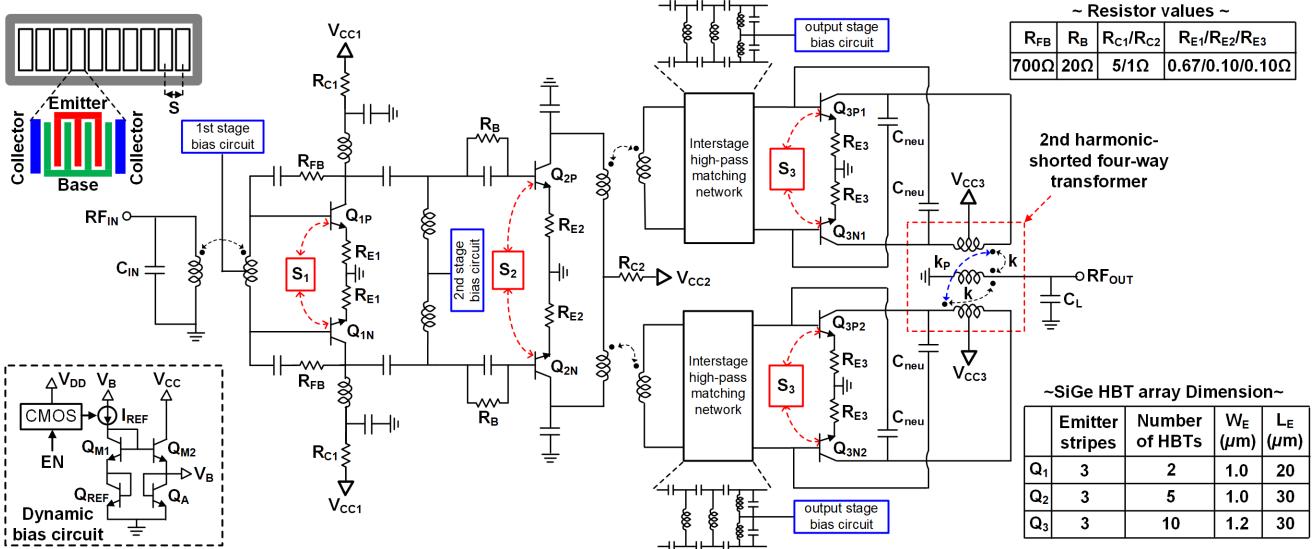


Fig. 3. Circuit schematic of a three-stage SiGe HBT PA with a compact 2nd-harmonic-shorted four-way output transformer balun (highlighted by the red dotted box). Schematic of a dynamic bias circuit with an embedded thermal sensor Q_{REF} (bottom left inset). Simplified top view of a SiGe HBT array with a magnified layout of a single SiGe HBT (top left image). Resistor values and dimension of SiGe HBT arrays, respectively (top and bottom right tables).

IV. DESIGN OF TRANSFORMERS

A. 2nd-Harmonic Tuning in Linear PA Design

Since the 2nd-harmonic current is the strongest among all harmonics for the deep class-AB mode PAs, its suppression, especially at the output stage of the PA, is crucial for the linear operation of WLAN PAs [43], [44]. Conventionally, a series LC tank is added at the drain or the collector of a transistor for the 2nd-harmonic current rejection at the cost of increased capacitive loading at the fundamental frequency, which lowers the required inductance and its quality (Q) factor for output matching. This leads to an increased insertion loss of the output matching network and reduced PA efficiency. Alternatively, for differential PAs, a two-way transformer with a 2nd-harmonic trap at its center tap was demonstrated in [45]. However, the use of a bulky series inductor on the supply lane consumes a significant Si area and causes large IR drops that degrade P_{OUT} and PAE. A wire-bond inductance was used for the 2nd-harmonic traps in a differential output stage in [46], but its reproducibility would limit its usage to low-frequency bands.

B. Four-Way 2nd-Harmonic-Shorted Output Transformer

The design of a compact 2nd-harmonic-tuned four-way output transformer balun is described in this section. The proposed four-way output transformer balun was constructed using two primary windings and a single secondary coil, as shown in Fig. 4, all within a single footprint, and its diameter is 280 μm. The metal line width was set to 16 μm for high current handling. A back-end-of-line (BEOL) process, as highlighted by a dotted box in Fig. 4, provides a 4-μm-thick aluminum layer (MA), a 3-μm-thick copper layer (E1), and a 3-μm-height continuous-run via (E2). The BEOL cross section of a quadrant in the output transformer balun

is shown in a solid inset of Fig. 4, where the solid and dotted arrows indicate the current directions in the primary windings and the secondary coil, respectively, at the fundamental frequency. The center and the innermost metal traces are multi-layered stacks connected through the continuous via E2. The proposed structure achieves both broadside and lateral magnetic coupling among the primary coils and the secondary winding, leading to a high magnetic coupling factor k of 0.82. The multi-layered configuration has two primary coils with just 4-μm spacing, which results in a high magnetic coupling factor k_P of 0.53 between the two primary coils. The equivalent turn ratio n is defined as follows:

$$n = \sqrt{\frac{L_S}{(1+k_P)L_P}} = 1.9. \quad (3)$$

This configuration also enables us to obtain a large primary inductance modulation factor depending on the mode of operations

$$M = \frac{1+k_P}{1-k_P} = 3.24. \quad (4)$$

Such a high inductive modulation factor enables a separate impedance matching at the fundamental and 2nd-harmonic frequencies. In an odd-mode, ac currents on the primary windings flow in the same direction, and the mutual inductance between the two windings effectively increases their primary inductance from L_P to $(1+k_P)L_P$ with a Q -factor enhancement. Fig. 5(a) shows a simulated passive efficiency and the primary inductance values of the output transformer balun. The peak passive efficiency is 87.2% at 5.5 GHz, which corresponds to the insertion loss of 0.6 dB. L_P is also increased to 388 pH, thanks to the strong positive magnetic coupling between the two primary windings. As shown in Fig. 5(b), the simulated unloaded Q -factors for the primary winding and the secondary

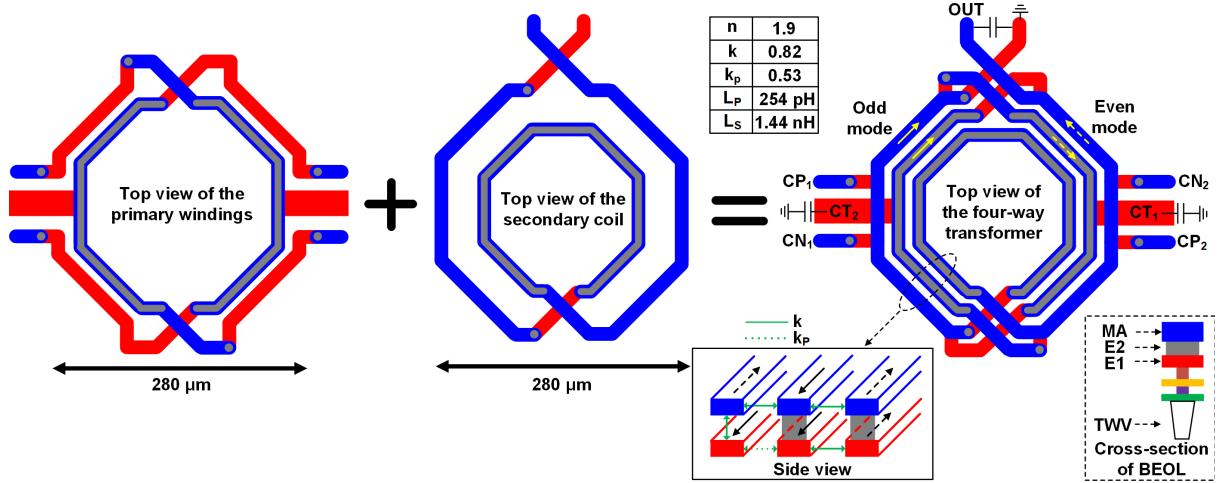


Fig. 4. Top view of the proposed compact 2nd-harmonic-shorting four-way output transformer balun. Cross section of the BEOL is highlighted in the bottom right dotted inset. The solid inset shows a side view of the novel multi-layered metallization with current directions labeled on the primary windings and the secondary coil at the fundamental frequency. Design parameters of the four-way output transformer balun at 5.5 GHz (top table).

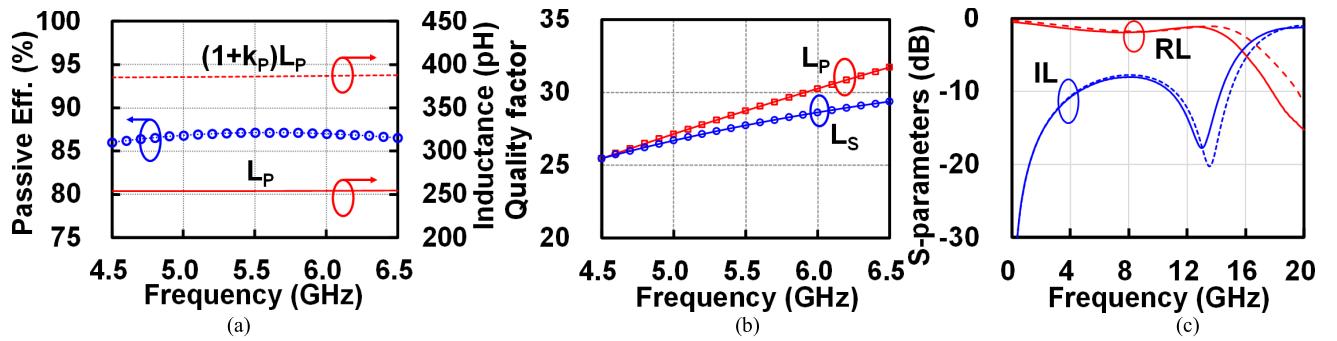


Fig. 5. Simulated (a) passive efficiency (blue circle) and primary inductances, (b) unloaded quality factors of the primary winding (red rectangular) and the secondary coil (blue circle), and (c) simulated (dotted) and measured (solid) back-to-back test structure of the four-way output transformer balun.

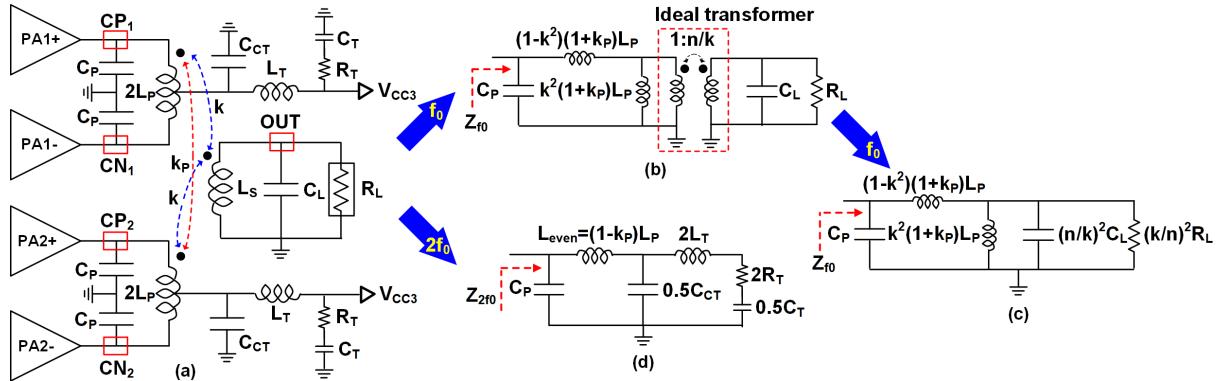


Fig. 6. (a) Simplified circuit schematic of the output stage, (b) single-ended odd-mode PA half-equivalent circuit, (c) single-ended odd-mode PA half-equivalent circuit with the load shifted to the primary side, and (d) single-ended even-mode PA half-equivalent circuit.

coil are 28.8 and 27.6 at 5.5 GHz, respectively, because of a low ohmic loss of the multi-layered BEOL.

Fig. 6(a) shows a simplified circuit schematic of the output stage, including the output transformer balun. An odd-mode PA half-equivalent circuit is shown in Fig. 6(b). It can be modeled by a leakage inductance of $(1-k^2)(1+k_p)L_p$, a magnetizing inductance of $k^2(1+k_p)L_p$, an ideal transformer with a turn ratio of $1: n/k$, a PA parasitic capacitance C_P of 1.9 pF,

and a 50Ω load R_L in parallel with a load capacitance C_L of 0.33 pF.

The half- equivalent circuit shown in Fig. 6(b) can be further simplified to a 4th-order passive network shown in Fig. 6(c), by transferring the load from the secondary to the primary side of the ideal transformer [47]. The R_L is transformed to the optimum impedance of 15Ω for a single-ended PA cell.

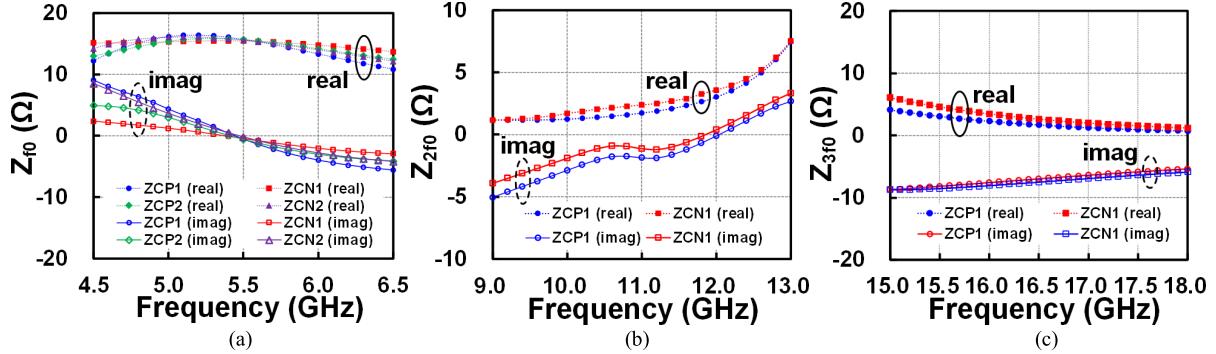


Fig. 7. Simulated (a) fundamental impedances (Z_{f0}), (b) 2nd-harmonic impedances (Z_{2f0}), and (c) 3rd-harmonic impedances (Z_{3f0}) of the output transformer balun.

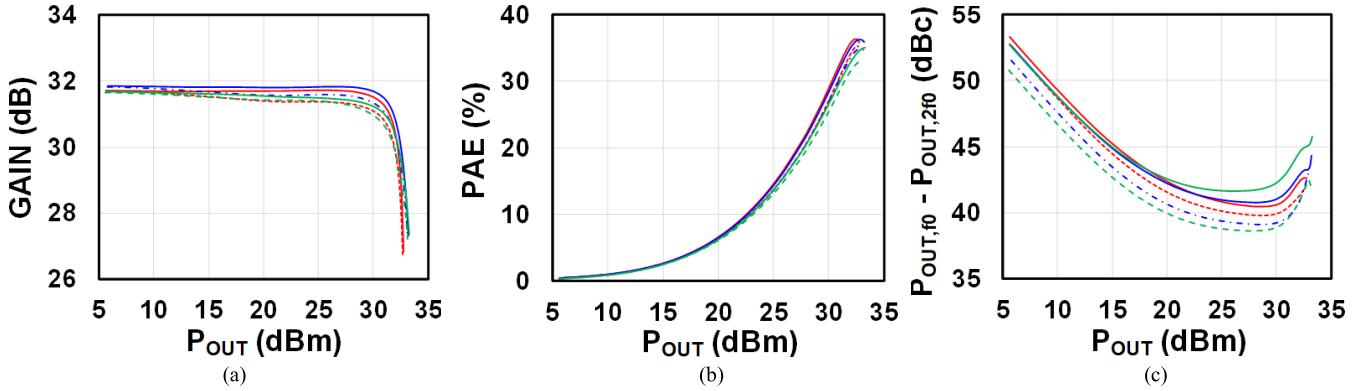


Fig. 8. Simulated (a) power gain, (b) PAE, and (c) 2nd-harmonic rejections of the PA both with C_{CT} (solid lines) and without C_{CT} (dotted line) at the center taps of the proposed four-way output transformer balun (red: $f_0 = 5.210$ GHz, blue: $f_0 = 5.530$ GHz, green: $f_0 = 5.855$ GHz).

Under the even-mode operation, the effective inductance of the primary windings is reduced to $(1 - k_P)L_P$ as currents flow in the opposite directions on the two primary windings. An even-mode PA half-equivalent circuit is shown in Fig. 6(d). Adding a bypass capacitor C_{CT} at each center tap (CT_1 and CT_2) of the output transformer balun synthesizes a highly capacitive π -network, resulting in very low 2nd-harmonic impedance. C_{CT} was tuned to 3.4 pF to account for the parasitic inductance of the TWVs used to ground the bottom plates of the capacitors. A trace inductance L_T of 0.2-nH functions as an RF choke and minimizes the influence of the $R_T C_{CT}$ bypass network on the 2nd-harmonic impedance of the highly capacitive π -network.

Simulated odd-mode (Z_{f0}) and even-mode (Z_{2f0}) impedances are shown in Fig. 7(a) and (b), respectively. Real and imaginary parts of Z_{f0} are 15.0 ± 1.5 and 0 ± 4.9 Ω, respectively, from 5 to 6 GHz, with a good balance. From 10 to 12 GHz, the real and imaginary parts of Z_{2f0} are 2.4 ± 1.1 and -1.5 ± 1.6 Ω, respectively. The odd-mode self-resonance frequency of the output transformer is 13 GHz, leading to a highly capacitive 3rd-harmonic impedance (Z_{3f0}), as shown in Fig. 7(c).

A back-to-back structure of the four-way output transformer was characterized to verify simulation fidelity. As shown in Fig. 5(c), the simulated and measured insertion losses of the back-to-back output transformer balun are 8.9 and 9.1 dB at 5.5 GHz, respectively, showing close match.

To demonstrate its built-in 2nd-harmonic short ability, large-signal performances of the proposed PA both with and without C_{CT} were simulated. As shown in Fig. 8(a), output P1dB decreased by 0.6 dBm without C_{CT} . This reduced output P1dB also leads to a peak PAE reduction of up to 2%, as shown in Fig. 8(b). Fig. 8(c) shows that 2nd-harmonic rejection without C_{CT} is degraded by 1/2/3 dBc at 5.210/5.530/5.855 GHz, respectively.

Comparisons between the PA with C_{CT} and that without C_{CT} , but with series LC traps at collectors (CP1/CN1/CP2/CN2) of SiGe HBT arrays in the output stage were simulated. An inductor with $Q = 15$ and a 0.5-pF process design kit (PDK) MIM capacitor were used for the LC traps. As shown in Fig. 9(a), the PA with C_{CT} has a higher power gain by 0.4/0.6/0.8 dB than that with the four LC traps at 5.210/5.530/5.855 GHz, respectively, due to smaller capacitive loadings at the collectors. As a result, higher peak PAEs by 0.6%/1.7%/2.7% are obtainable at 5.210/5.530/5.855 GHz, respectively, as shown in Fig. 9(b). Fig. 9(c) clearly shows the PA with C_{CT} is comparable to that with the four bulky LC traps in terms of 2nd-harmonic rejection capability.

The proposed four-way output transformer balun achieved simultaneous fundamental and 2nd-harmonic impedance matching without any harmonic trap and efficient parallel power combining. It attained an equivalent impedance transformation ratio higher than 13:1 using a single inductor footprint. Another unique advantage of this four-way output

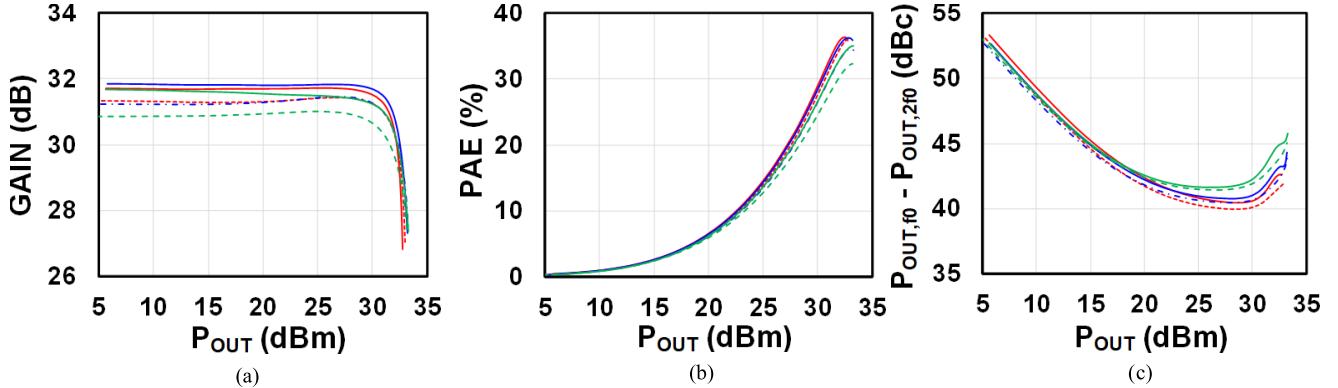


Fig. 9. Simulated (a) power gain, (b) PAE, and (c) 2nd-harmonic rejection of the PA both with C_{CT} (solid lines) and without C_{CT} but with a series LC 2nd-harmonic trap (dotted lines) at the collector of each SiGe HBT array in the output stage (red: $f_0 = 5.210$ GHz, blue: $f_0 = 5.530$ GHz, and green: $f_0 = 5.855$ GHz).

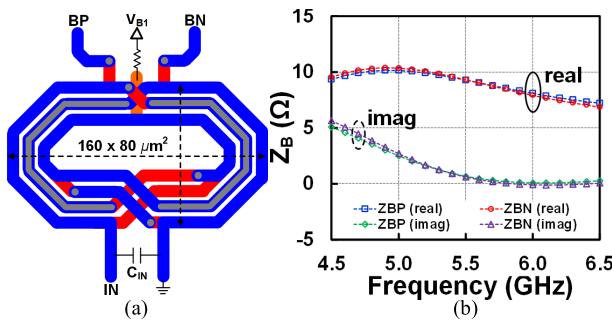


Fig. 10. (a) Top view of the proposed compact input transformer balun and (b) impedances looking into the secondary winding (Z_{BP} and Z_{BN}) of the balun.

transformer balun lies in the large physical separation ($440 \mu\text{m}$) of the two differential pairs in the output stage that minimizes the mutual thermal coupling between them, and thus, helping to keep T_J of SiGe HBT arrays in the output stage low.

C. Input Transformer and Inter-Stage Four-Way Transformer

For a fully single-ended PA operation, an ultra-compact two-way input transformer with a 3:2 turn ratio was designed, as shown in Fig. 10(a). A compact footprint of $160 \times 80 \mu\text{m}^2$ was achieved with both vertical and lateral magnetic couplings. An MIM shunt-capacitor C_{IN} of 0.8 pF was added in parallel with the 50Ω source impedance R_S for broadband matching. A 4Ω series resistor was inserted at a center tap of the input transformer balun to suppress an even-mode oscillation. The metal line width was chosen to be $7 \mu\text{m}$, in order to minimize a capacitive coupling between the primary winding and the secondary coil, which is the main cause of the signal imbalance.

Simulated impedances looking into two nodes BP and BN shown in Fig. 10(a) at the secondary side of the input transformer balun are shown in Fig. 10(b). Input impedances of the two SiGe HBT arrays are included in the simulation. The proposed ultra-compact input transformer balun transforms the R_S to the optimum impedance of $9 \pm 1 \Omega$ from 5 to 6 GHz.

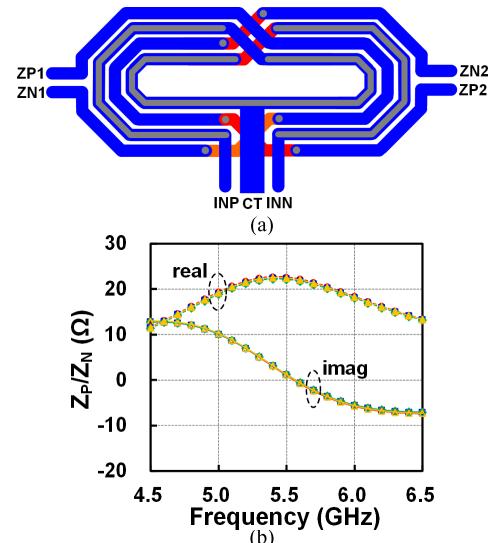


Fig. 11. (a) Top view of the inter-stage four-way transformer and (b) impedances looking into the secondary coil (Z_P and Z_N) of the transformer.

Fig. 11(a) shows a top view of a four-way inter-stage transformer with a 2:1 turn ratio. It converts an optimum differential impedance of 80Ω in the 2nd stage to two 40Ω differential impedances ($ZP1-ZN1$ and $ZP2-ZN2$). Unlike other transformers, it is laterally magnetic-coupled for reduced fringing capacitance. The 0.7-pF MIM capacitors were added at the output of the 2nd stage for the optimum matching. Due to its fully differential operation, the excellent balance can be maintained from 4.5 to 6.5 GHz, as shown in Fig. 11(b). The metal trace width and spacing are 10 and $4 \mu\text{m}$, respectively.

V. ELECTROTHERMAL DESIGN OF THE OUTPUT STAGE

In this section, the electrothermal behavior of the output stage in two PAs is described in detail. Fig. 12(a) shows a simplified circuit schematic of the differential pair in the output stage with a thermally compensating dynamic bias circuit. An off-chip resistor and CMOS current mirrors with enabled switches (not shown) are used to generate a constant reference current I_{REF} . Additional shunt CMOS switches were

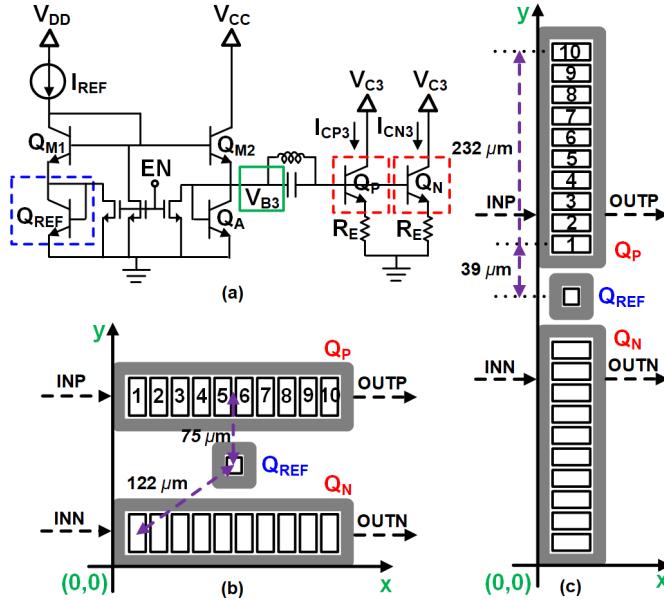


Fig. 12. (a) Circuit schematic of a differential pair in the output stage with a thermally compensating dynamic bias circuit, (b) LA of Q_P and Q_N with Q_{REF} , and (c) VA of Q_P and Q_N with Q_{REF} .

inserted into the SiGe HBT current mirror to enable a pulsed operation.

A lateral arrangement (LA) and a vertical arrangement (VA) output stages were configured as shown in Fig. 12(b) and (c), respectively. The two SiGe HBT arrays, Q_P and Q_N , are laid out symmetrically with respect to Q_{REF} , which acts as a temperature sensor that tracks the T_J variation of the output stage. Since the base-emitter voltage of Q_{REF} shows a strong complementary-to-absolute-temperature (CTAT) characteristic with a constant current bias, V_{B3} decreases with increased power dissipation in Q_P and Q_N . This CTAT characteristic of V_{B3} was leveraged to help maintain the collector current I_C of Q_P and Q_N and slowdown their β drop at high T_J . Without the proposed bias scheme, the collector current of the power cells will increase rapidly as T_J rises due to the positive electrothermal feedback [48]. Devices other than Q_{REF} in the bias circuit are kept far away from Q_P and Q_N to minimize an additional V_{B3} droop caused by Q_{M1} and to maintain the avalanche current-sinking capability of Q_A . An LC tank is used to present a high impedance at the fundamental frequency to the base node of the power cells in order to minimize signal leakage.

Electrothermal simulations were carried out by using the layout-based electrothermal model. The SiGe HBTs on the layout view are mapped with the corresponding device symbols in the schematic view. The $R-C$ thermal networks for modeling both self-heating and mutual thermal effects were extracted based on the locations and power dissipations of the Q_{REF} and the npn SiGe HBTs in the Q_P and Q_N arrays, as shown in Fig. 12(b) and (c).

The electrothermal behavior of the output stage in the dc domain was simulated. Fig. 13(a) shows V_{B3} and the sum of I_{CP3} and I_{CN3} in the differential pair with and without thermally coupled Q_{REF} for the two output stages. With thermally coupled Q_{REF} , both LA and VA configurations show

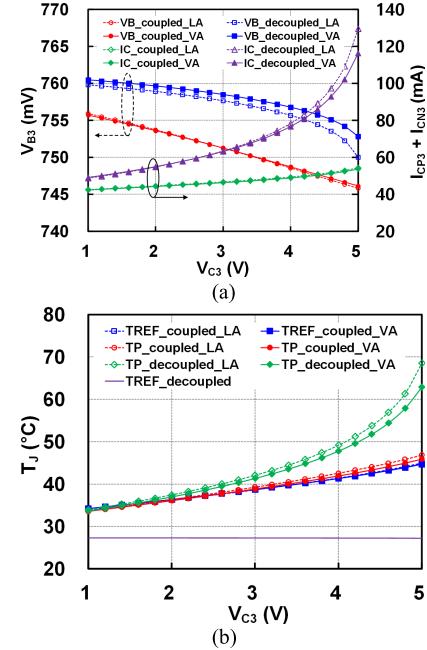


Fig. 13. Simulated (a) base voltage V_{B3} and collector current $I_{CP3} + I_{CN3}$ of the LA (empty symbol) output stage and the VA (solid symbol) output stage versus V_{C3} and (b) average T_J of Q_P and T_J of Q_{REF} versus V_{C3} . No RF signal is excited.

a linearly decreasing V_{B3} and relatively constant $I_{CP3} + I_{CN3}$ as V_{C3} increases. Fig. 13(b) shows the average T_J of Q_P versus V_{C3} for both LA and VA output stages. Due to symmetry, the average T_J of Q_N is omitted in this plot for simplicity. The T_J of thermally coupled Q_{REF} tracks that of Q_P , whereas the T_J of thermally decoupled Q_{REF} does not.

The electrothermal behavior of the PAs was simulated using the harmonic balance at 5.5 GHz. The average T_J of Q_P and T_J of Q_{REF} in the two arrangements are shown in Fig. 14(a) with respect to P_{OUT} . The T_J of Q_{REF} follows the average T_J of Q_P .

The AM-AM distortion characteristics of the two PAs were simulated at 5.5 GHz and they are shown in Fig. 14(b). With thermally coupled Q_{REF} , the output P_{1dB} for the lateral and vertical output stages is 31.7 and 31.6 dBm, respectively, which are 0.4 dB higher than those without thermal coupling, suggesting that the proposed bias circuit effectively prevents premature AM-AM compression at elevated T_J .

Memory effect [49], induced by a thermal effect and/or bias modulation, is another important phenomenon to be considered, as it is a source of DEVM degradation and asymmetry in the spectral mask. There are two types of memory effects: static and thermal. While the static memory effect is caused by the limited bandwidth of the bias circuit, the thermal memory effect results from the gain deviation in the dynamic operation of the PA due to a temperature mismatch between Q_{REF} and Q_P/Q_N [50].

Since the proposed bias circuit inherently has a closed-loop operation, its insufficient bandwidth will cause V_{B3} distortion, which in turn results in severe nonlinearity. The simulated gain of the bias circuit is normalized with respect to that

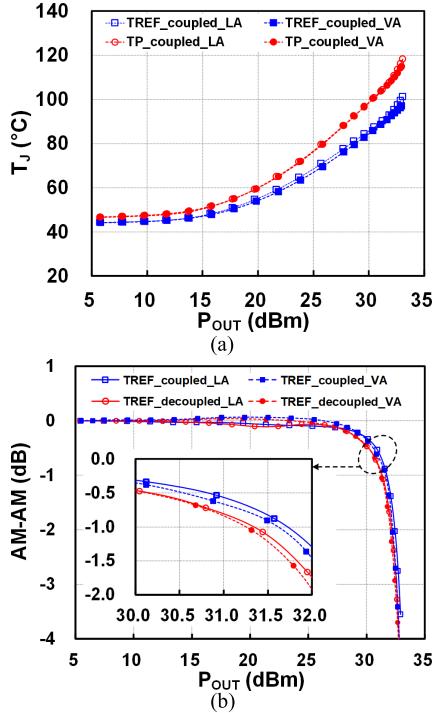


Fig. 14. Simulated (a) average T_J of Q_P and T_J of Q_{REF} with P_{OUT} sweep (LA: empty symbol and VA: solid symbol) and (b) AM-AM of PAs (LA: empty symbol and VA: solid symbol) with coupled (rectangular) and decoupled (circle) Q_P .

at 1 kHz, and its 1-dB gain bandwidth is 300 MHz. The emitter area of Q_A is set to $36 \mu\text{m}^2$ in order to provide low impedance at the input envelope frequency. If not suppressed, the low-frequency current is mixed with a fundamental frequency current, increasing the adjacent channel power ratio (ACPR) [49].

To address the dynamic memory effect, the electrothermal transient of the transistors during a pulsed operation needs to be considered. The thermally coupled network is particularly important in this case, as large gain hysteresis at the rising and falling edges in dynamic operation have been reported for the thermally decoupled case, which stems from I_C variation [50].

Fig. 15(a) shows a pulsed I_C of Q_P for the LA output stage with and without the thermally coupled Q_{REF} . The relatively constant I_C for the thermally coupled output stage leads to less gain variation in the pulsed operation. τ_{th} of the thermally coupled Q_P is shorter than that of the thermally decoupled case, suggesting that the proposed thermally compensating dynamic bias circuit is effective for thermal memory effect reduction. The pulsed I_C at various T_{amb} is shown in Fig. 15(b).

Also, a faster electrothermal transient would be expected for the PA with the LA output stage than its VA counterpart, due to a smaller distance between Q_{REF} and SiGe HBTs in Q_P , resulting in DEVM improvement of the lateral PA over the vertical one.

The impact of the electrothermal design on the SiGe HBT WLAN PA's linear performance is first analyzed by highlighting the interaction between the SiGe HBT arrays and the temperature sensor. The proposed thermally compensating

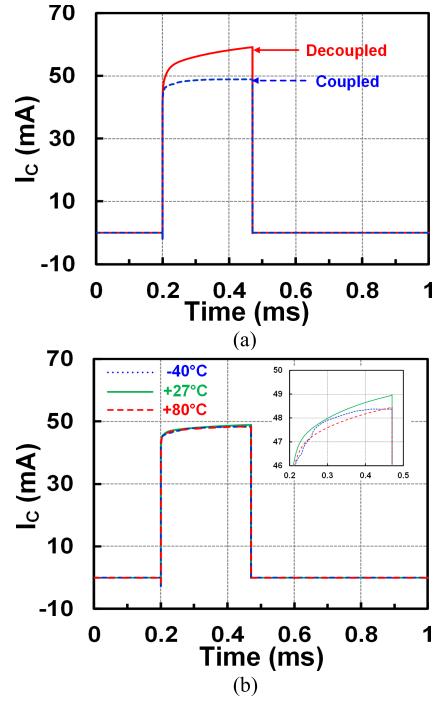


Fig. 15. Simulated pulsed I_C of Q_P for the LA output stage (a) with (dotted) and without (solid) thermal coupling at the ambient temperature of 27 °C and (b) with thermal coupling at various ambient temperatures. No RF signal is excited.

dynamic bias circuit not only prevents β drop as T_J rises, but reduces memory effects. The tight thermal coupling among SiGe HBT arrays and the temperature sensor would be key for enhancing DEVM. Further improvement will be expected if a more sophisticated bias circuit [51] was developed for the PA, which ramps up I_C such that the PA power gain is constant during a pulsed operation.

VI. FABRICATION AND EVALUATION BOARD DESIGN

A. Implementation of SiGe HBT PAs

Two PA prototypes, as shown in Fig. 16(a) and (b), were fabricated in GlobalFoundries 0.35- μm SiGe BiCMOS technology with emitter widths (W_E) ranging from 0.24 to 1.20 μm and emitter lengths (L_E) up to 40 μm . The peaks f_T and f_{MAX} of a SiGe HBT array with W_E/L_E of 1.2/30 μm , three emitter stripes, and two SiGe HBTs are 26.5 and 70.0 GHz, respectively.

Each PA chip occupies $1.45 \times 1.40 \text{ mm}^2$ active area with a substrate thickness of 100 μm . The solid red and green-colored boxes in Fig. 16(a) and (b) mark the locations of Q_{REF} and remaining elements in the dynamic bias circuit, respectively.

Several SiGe HBT model parameters used in the simulations were characterized by using test wafers instead of the nominal values given in the PDK documentation for better simulation accuracy. For example, measured β of the SiGe HBT array on the test wafer is 112, which is 7.5% lower than the nominal PDK value. BV_{CEO} and BV_{CBO} of the SiGe HBT are 6.1 and 17.7 V, respectively, and 3.3-/5.0-V CMOS devices are available for integrating analog bias circuits and digital control blocks.

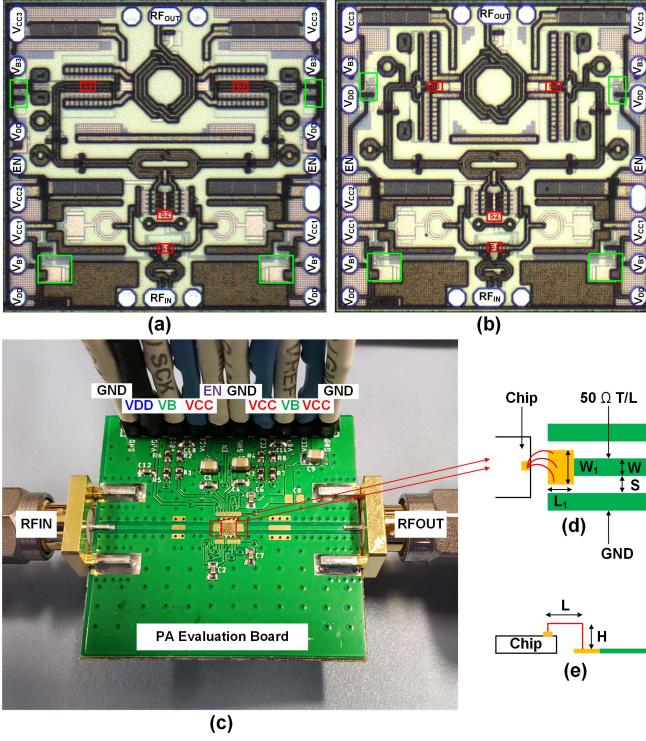


Fig. 16. Chip micrograph of (a) PA with LA output stage and (b) PA with VA configuration. (c) Top view of a PA evaluation board with (d) magnified view of RF input and output pads on the PCB, and (e) cross section of the RF pads.

The technology also provides an MIM capacitor and sili-cid ed polysilicon resistors for accurately valued resistors. The high-resistivity substrate is beneficial for realizing high Q passives.

B. Evaluation Board Design

Fig. 16(c) shows a top view of a PA evaluation board. The two PAs were mounted on a PCB using a thermally conductive epoxy EK2000, and all RF and dc pads on the PA semiconductor chips (DIEs) were wire-bonded to the PCB traces. The multi-layered PCB was made of a low-loss, thermally conductive RO4350B material as a top substrate and low-cost FR406B as a bottom substrate and an interposer for dc signal routings. No heat sink was put underneath the PCB in the measurements.

Grounded coplanar waveguide (GCPW) transmission lines (T-lines) were designed as shown in Fig. 16(d). The line width (W) and spacing (S) of a 50- Ω GCPW T-line are 0.6 and 0.5 mm, respectively. Bond-wire inductances were simulated using EMX. As shown in Fig. 16(e), all bond wires used a fixed length (L) and height (H) of 250 and 125 μm . The bond-wire inductance was tuned by varying the number of wires in parallel. Simulated bond-wire inductances up to three parallel wires are shown in Fig. 17(a). The effective inductance of the connection gradually decreases from 0.28 to 0.15 nH, as the number of parallel wires increases. This inductance reduction, however, saturates with an increasing number of parallel wires due to mutual inductance among bond wires.

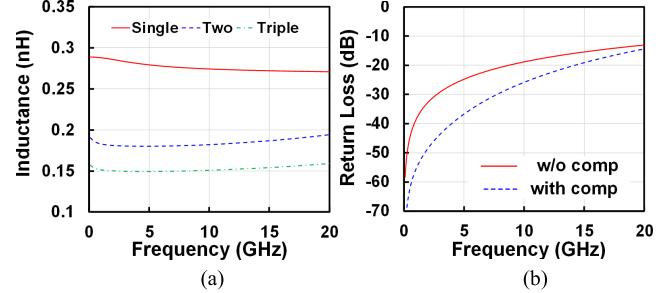


Fig. 17. Simulated (a) bond-wire inductances for a different number of parallel bond wires and (b) return losses of the triple bond-wire inductance in series with 50- Ω T-line without compensation (solid) and with compensation (dotted).

The inductance of three wire bonds was absorbed by a low characteristic impedance (Z_0) T-line section on PCB. The width (W_1) and length (L_1) of the low Z_0 T-line were set to 0.9 and 0.7 mm, respectively, to synthesize an artificial lumped-element 50- Ω T-line with the bond-wire inductance. Fig. 17(b) shows the comparison of the simulated return losses of the 50- Ω T-line with and without the wide metal trace.

Any series resistive and/or inductive parasitics on a supply lane can induce a supply voltage modulation [42], which results in an asymmetry in a modulated spectrum. To reduce the supply modulation, a metal trace width of 1 mm was used for the output stage supply for low ohmic loss and small parasitic inductance. Multiple bypass capacitors were placed along the PCB traces, such that the closest to the die can supply the current with the minimal ripple for the modulation bandwidth of 20 MHz.

VII. CHARACTERIZATION OF THE PROPOSED WLAN PAs

A. Small-Signal and Large-Signal Results

Simulated and measured S -parameters of the PA with LA and VA output stages are shown in Fig. 18(a) and (b), respectively. The quiescent current of both the PAs was set to 225 mA from 5.0-V supply. Peaks S21 for the PAs with LA and VA output stages are 31.6 and 31.8 dB at 5.5 GHz, respectively, with less than 1-dB gain variation from 5.0 to 5.9 GHz. The gain flatness for any 80-MHz bandwidth is ± 0.25 and ± 0.32 dB for LA and VA output stages, respectively. S11 lower than -10 dB is achieved from 4 to 8 GHz for both PAs due to the broadband matching of the compact input transformer balun. Good simulation and measurement agreement of the return losses of the two PAs suggests that the bond-wire effect is modeled well.

Large-signal characteristics of the two PAs were measured with a 300- μs burst length at 10% duty cycle. As shown in Fig. 19(a) and (b), the peak PAEs are $35.2\% \pm 1.0\%$ and $35.5\% \pm 0.7\%$ for the PAs with LA and VA output stages, respectively. Fig. 19(c) and (d) shows the measured AM-AM behavior of the LA and VA designs. $P_{1\text{dB}}$ and P_{SAT} are 32.0 ± 0.4 and 33.0 ± 0.5 dBm, respectively. AM-PM, shown in Fig. 19(e) and (f), are less than 2.5° at $P_{1\text{dB}}$. Measured

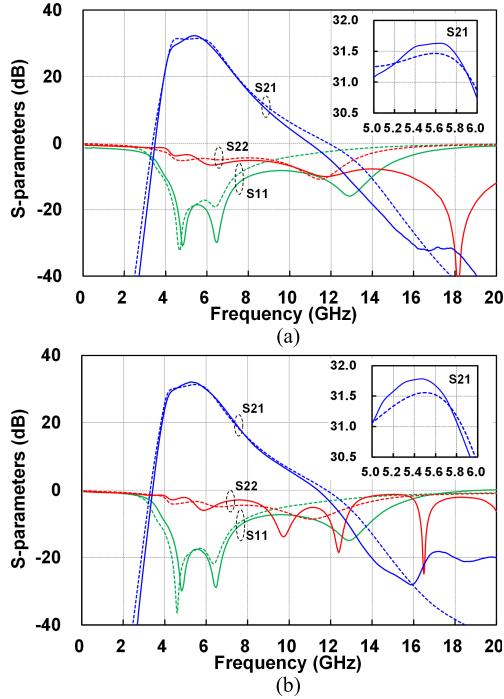


Fig. 18. Simulated (dotted) and measured (solid) S -parameters of (a) PA with LA output stage and (b) PA with VA output stage.

harmonic emissions were characterized at 5530 MHz for the 802.11ac MCS9 VHT80 signal. As shown in Fig. 20, 2nd- and 3rd-harmonic emissions are less than -45 and -67 dBm/MHz at P_{OUT} of 23 dBm, respectively, indicating the excellent spectral purity of the PAs without any harmonic rejection filter.

B. Linearity Measurement Results

A block diagram of the linearity measurement setup of WLAN PAs is shown in Fig. 21. A Keysight MXG vector signal generator synthesizes various WLAN test signals; and DEVM, I/Q constellation, and spectral masks of the PAs were measured using a Keysight PXA spectrum analyzer.

DEVM and PAE of the two PAs are shown in Fig. 22 for the 802.11ac MCS9 VHT80 test signals with $300\text{-}\mu\text{s}$ burst length at 50% duty cycle. The data were obtained at 5210, 5530, and 5855 MHz. The PA with LA output stage delivers $22.5/23.6/23.2$ dBm P_{OUT} ($\text{DEVM} = -35$ dB) with PAEs of $10.0\%/12.2\%/11.2\%$ at 5210/5530/5855 MHz, respectively. For the PA with VA configuration, linear P_{OUT} ($\text{DEVM} = -35$ dB) and PAE are $21.3/22.7/22.6$ dBm and $8.0\%/9.7\%/9.4\%$, respectively. The DEVM degradation at the lower frequency, compared to those measured at mid and high frequencies, is due to a smaller P_{SAT} and a larger gain expansion as shown in Fig. 19(c) and (d).

Fig. 23(a) and (b) shows the DEVM of the two PAs measured with the 802.11ac MCS9 VHT80 test signals at 5530 MHz under various duty cycles. The linear P_{OUT} ($\text{DEVM} = -35$ dB) is 23.4 and 22.4 dBm at 90% duty cycle for the PA with the LA output stage and its VA counterpart, respectively.

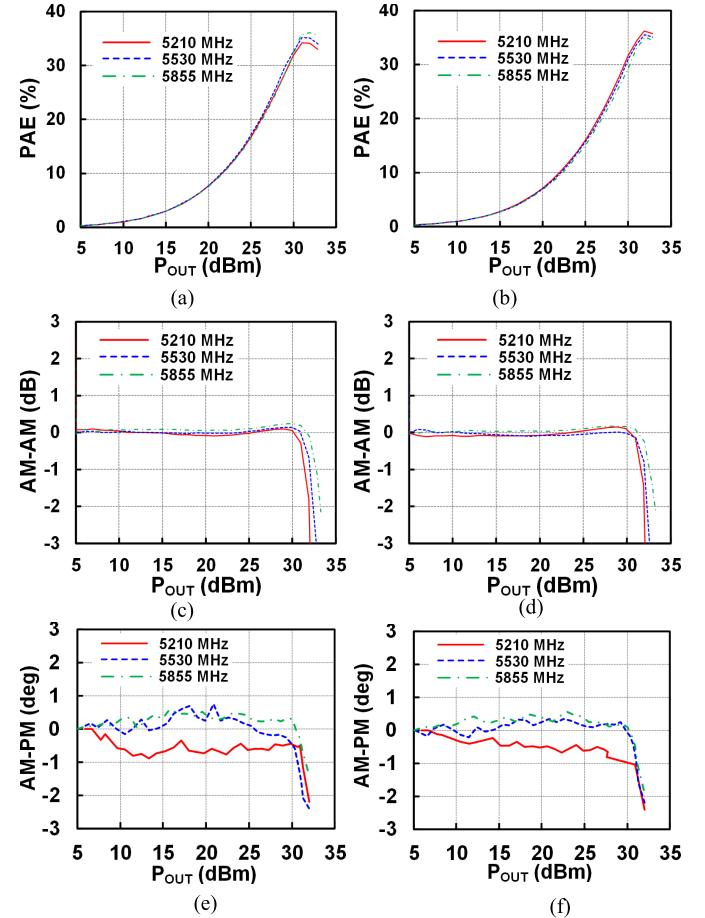


Fig. 19. Measured (a) PAE, (c) AM-AM, and (e) AM-PM of the PA with LA output stage and (b) PAE, (d) AM-AM, and (f) AM-PM of the PA with VA output stage. All measurements are carried out at 10% duty cycle with $300\text{-}\mu\text{s}$ pulsed signal.

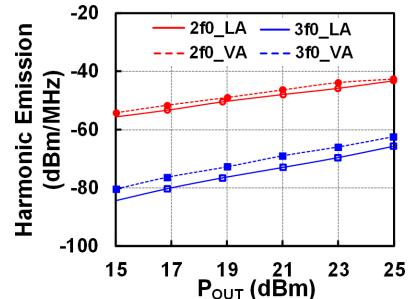


Fig. 20. Measured harmonic emission at $2f_0$ (circle) and $3f_0$ (rectangle) under the 802.11ac MCS9 VHT80 signal at 100% duty cycle. Solid and dotted lines are results for the PAs with LA output stage and VA output stage, respectively.

The higher P_{OUT} of the PA with LA output stage than its vertical counterpart would be due to its faster electrothermal transient response.

The WLAN PAs were tested under various standard signals at the mid-band and the measured DEVM is shown in Fig. 24(a) and (b). P_{OUT} of 25.9 and 25.5 dBm ($\text{DEVM} = -30$ dB) with PAE of 17.1% and 16.3% were measured for the

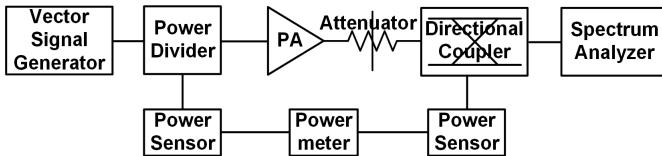
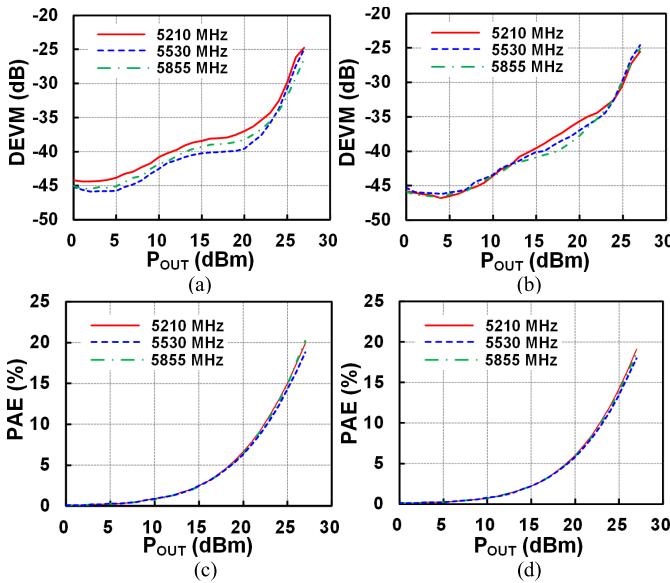
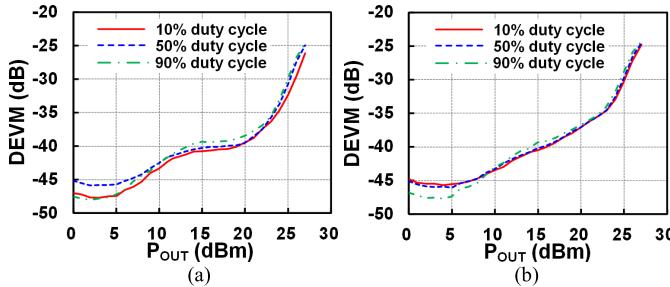
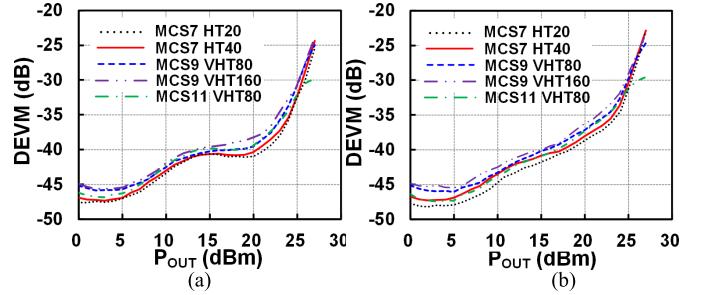
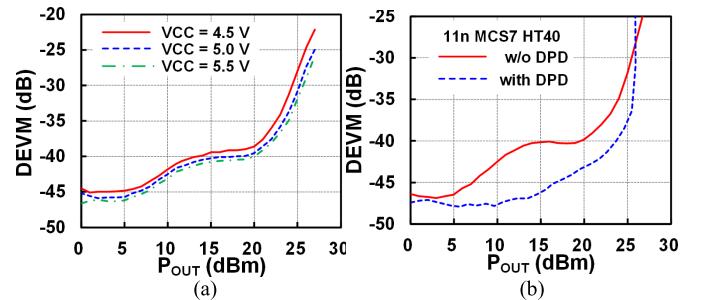


Fig. 21. Block diagram of linearity measurement setup of the WLAN PAs.

Fig. 22. Measured DEVM of the PAs with (a) LA and (b) VA output stages. Measured PAE of the PAs with (c) LA and (d) VA output stages. The 802.11ac MCS9 VHT80 test signal with 300- μ s burst length at 50% duty cycle is used.Fig. 23. Measured DEVM of the PAs with (a) LA and (b) VA output stages for the 802.11ac MCS9 VHT80 test signal with 300- μ s burst length at 10%/50%/90% duty cycles. The carrier frequency is 5530 MHz.

PA with LA output stage and its VA counterpart, respectively, using the 802.11n MCS7 HT20 signal. The PA with LA output stage supports the 802.11ax WLAN requirement of $DEVM = -38/-40$ dB at 21.4- and 19.4-dBm P_{OUT} with PAE of 8.5% and 6.1%, respectively. Higher PBO is required for the PA with the VA output stage to meet the 802.11ax DEVM specification. This difference is due to a larger gain error of the VA PA caused by its slower electrothermal transient. For the 802.11ac MCS9 VHT160 signal, 22.9- and 21.7-dBm P_{OUT} ($DEVM = -35$ dB) with 10.8% and 8.5% PAE were observed for the PA with LA output stage and its VA counterpart, respectively. The degradation in P_{OUT} compared with VHT80 is due to

Fig. 24. Measured DEVM of the PAs with (a) LA and (b) VA output stages for various WLAN signals (300- μ s burst length and 50% duty cycle at mid-band).Fig. 25. Measured DEVM of the PA with LA output stage (a) under supply variation (802.11ac MCS9 VHT80 with 300- μ s burst length under 50% duty cycle at 5530 MHz) and (b) the 802.11n MCS7 HT40 with (solid) and without (dotted) DPD (300- μ s burst length under 50% duty cycle at 5520 MHz).

a larger gain variation in a 160-MHz channel and a higher number of sub-carriers in the OFDM symbol.

The DEVM of the PA with LA output stage was measured over supply variation of 5.0 ± 0.5 V and the results are shown in Fig. 25(a). The linear P_{OUT} that satisfies the DEVM of -35 dB is 22.8/23.6/24.0 dBm at 4.5-/5.0-/5.5-V supplies and 5530 MHz, respectively.

The DEVM of the PA with LA output stage was also measured using memoryless DPD. As shown in Fig. 25(b), P_{OUT} meeting the DEVM of $-30/-35/-40$ dB were 26.2/25.6/23.7 dBm for the 802.11n MCS7 HT40 test signal at 5510 MHz, respectively, after DPD was applied. This large improvement in linear P_{OUT} indicates that the proposed 802.11ac/ax SiGe HBT WLAN PA still has more design margin to attain even better performance.

Clear I/Q constellations for various WLAN standard signals can be seen in Fig. 26(a)–(c). Fig. 26(d) shows that the PA follows the IEEE standard spectral mask at P_{OUT} of 25.7 dBm for an 802.11ax MCS11 VHT80 test signal.

Table I provides the performance comparison among the WLAN PAs. The proposed SiGe HBT PAs demonstrate the highest linear P_{OUT} and competitive PAE compared with all the Si-based WLAN PAs in the 802.11n/11ac standards. The SiGe HBT PAs also support the 802.11ax WLAN mode. Linear P_{OUT} of the SiGe HBT PA with LA output stage is comparable to its III-V counterpart, demonstrating that SiGe HBT BiCMOS platform is a good candidate to realize low-cost, high-performance WLAN PAs.

TABLE I
PERFORMANCE COMPARISON AMONG THE STATE-OF-THE-ART 802.11ac/ax WLAN PAs

Reference	[6]	[7]	[11]	[12]	[16]	[18]	[27]	[28]	This work	This work
Technology	GaAs HBT	55 nm CMOS	40 nm CMOS	40 nm CMOS	40 nm CMOS	130 nm CMOS	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS
PA Architecture	Class-AB	Class-AB Doherty	Digital PA IQ summing	Spatial combining	Class-AB	Class-AB	Class-AB	Class-AB	Class-AB LA output	Class-AB VA output
Frequency (GHz)	5.0	5.0	2.4/5.0	5.0	2.4/5.0	5.0	5.0	5.0	5.0	5.0
Supply (V)	5.0	3.3	3.3	-	3.3	3.6	5.0	3.85	5.0	5.0
Small signal gain (dB)	32.0	26.0	-	-	24.8/23.5	14.4	32.0	26.5	31.6	31.8
P _{SAT} (dBm)	34.0	29.0	27.0/25.5	27.0	27.9/27.1	26.0	30.5	-	33.0	33.0
2nd/3rd harmonic emissions (dBm/MHz)	-45/-45	-51/-51	-	-	-	-32/-60****	-/-	-/-	-46/-70	-44/-67
DPD requirement	No	Yes	Yes	Yes	No	No	No	No	No	No
Chip size (mm ²)	-	1.42***	0.70	-	0.49	0.62	0.95	-	2.03	2.03
802.11n	P _{OUT} (dBm)	27.0	-	18.1	19.7	19.5	19.0	23.0	-	25.9
MCS7	PAE (%)	16.7	-	14.1	-	-	14.7	13.0	-	17.1
802.11ac	DEVM (dB)	-30.0	-	-30.0*	-30.0	-30*	-30.0*	-31.0	-	-30.0
MCS0/8	BW (MHz)	20	-	20	20	20	20	-	20	20
802.11ac	P _{OUT} (dBm)	25.0	20.0	14.3	19.0	17.5	15.6	21.6	-	23.6/22.9
MCS9	PAE (%)	10.5	12.0**	-	-	10.0	7.5	10.2	-	12.2/10.8
802.11ac	DEVM (dB)	-35.0	-35.0	-32.0*	-35.0	-35.0*	-35.0*	-35.0	-	-35.0
MCS9	BW (MHz)	80	160	80	80+80	40	80	80	-	80/160
802.11ax	P _{OUT} (dBm)	-	18.0/15.0	-	-	-	-	20.3/19.8	16.5	21.4/19.4
MCS11	PAE (%)	-	10.0/7.0	-	-	-	-	8.4/7.8	4.6	8.5/6.1
802.11ax	DEVM (dB)	-	-38.0/-40.0	-	-	-	-	-38.0/-40.0	-47.0	-38.0/-40.0
MCS11	BW (MHz)	-	160	-	-	-	-	80	160	80

* EVM is not measured in dynamic environment. ** Memory polynomial DPD power consumption is not included in PAE calculation.

*** Area of a PA balun realized in 180 nm SOI CMOS is not included. **** Measured at a single-tone frequency.

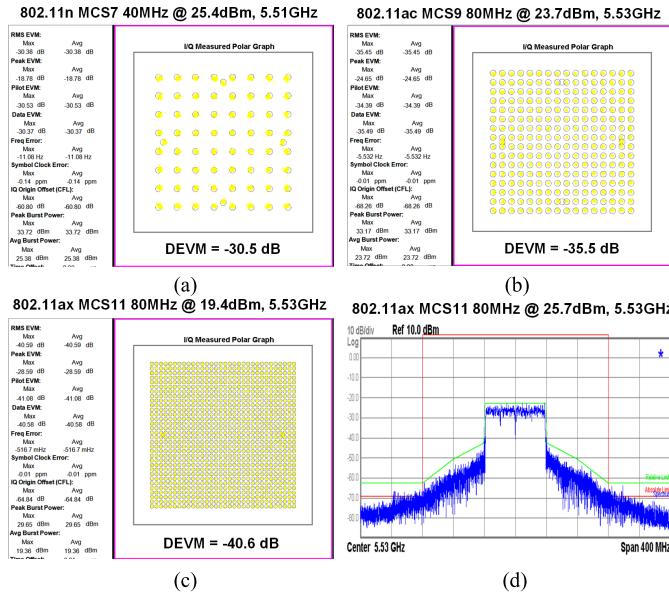


Fig. 26. Measured I/Q constellations for (a) 802.11n MCS7 HT40, (b) 802.11ac VHT80, and (c) 802.11ax MCS11 VHT80, and (d) measured spectral mask for 802.11ax MCS11 VHT80 test signal. The carrier frequency is 5530 MHz.

VIII. CONCLUSION

The design of highly linear high-power 802.11ac/ax WLAN SiGe HBT PAs has been presented. The compact four-way output transformer balun with the built-in 2nd-harmonic short

was realized with the novel multi-layered metal scheme with an embedded capacitor at its center tap. It achieved simultaneous impedance matching at the fundamental and 2nd-harmonic frequencies without any harmonic trap. The thermally compensating bias circuit with the integrated temperature sensor was designed to reduce the gain error under the dynamic operation and to minimize memory effects for linear operation. Two output-stage configurations (VA and LA) were compared and the results indicated the impact of the layout-dependent electrothermal transient on the DEVM of the WLAN PAs. The proposed 802.11ac/11ax WLAN SiGe HBT PA demonstrated record linear P_{OUT} and PAE among any Si-based WLAN PAs.

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