A 31-dBm, High Ruggedness Power Amplifier in 65-nm Standard CMOS with High-Efficiency Stacked-Cascode Stages

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***Abstract*—A novel, high ruggedness power amplifier topology in a 65-nm CMOS technology is proposed. The proposed stacked cascode topology uses only standard devices available in a modern triple-well CMOS process to achieve breakdown voltages of more than 18V. The power amplifier stage delivers 28 dBm output power at a power-added efficiency (PAE) of 69.9% from a 3.6V supply. The saturation gain is 18 dB. A watt-level power amplifier for GSM low-band operation with 31-dBm output power and 61% PAE is presented.**

***Index Terms*—Breakdown voltage, CMOS, high efficiency, HV device, power amplifier, RF, ruggedness.**

I. Introduction

The implementation of single-chip radios is the ultimate goal in RF CMOS design. This requires the full integration of power amplifiers (PA). The main obstacle is the ruggedness of standard devices (MOSFETs) available in modern CMOS processes. The low device breakdown voltages do not comply with the nominal battery voltage in a mobile handset of 3.6V (even up to 5.5V in the worst case) and the requirement to withstand load mismatch conditions, i.e. high VSWR up to 10:1 without harming the device. Thus, a much lower supply voltage would have to be generated efficiently (e.g. by means of a DC-DC converter) which leads to a reduction of the overall efficiency. Generating high RF power from low supply voltages poses also another problem: the optimum load impedance of the PA output stage transistors becomes very small. A matching network with a high transformation ratio is needed to transform the antenna impedance of 50 to the optimum load impedance. High transformation ratios usually result in small bandwidth and higher losses. Possible solutions are the use of either non-standard high power RF devices or special circuit topologies using only the available standard devices.

The development of non-standard devices (like LDMOS etc. [1], [2]) is expensive and increases technology costs due to additional masks and/or process modifications. Circuit topologies using only standard devices circumvent these additional costs and achieve the required ruggedness by stacking multiple transistors. Simple cascode structures in modern nm-CMOS technologies cannot withstand the high RF voltages of more than 15V occurring at the output of power devices in GSM PAs under load mismatch conditions. Therefore, more than two standard MOSFETs have to be stacked. This can be done in two ways: either by DC-only coupling of single FETs/cascode circuits [3] with RF power combining at the outputs or by the HiVP (High-Voltage/High-Power device) configuration [4], [5]. DC-only coupled devices require multiple matching networks while the HiVP and similar configurations suffer from reduced efficiency due to increased effective on-resistance because of the in-phase voltage swing at the gates of the stacked transistors.

In this paper, the novel stacked-cascode power amplifier topology is proposed. Section II summarizes the theory of circuit operation. Result from breakdown and load-pull measurements on single-stage test structures are discussed in Section III. Section IV presents a differential 31-dBm Class-AB power amplifier employing the novel stacked-cascode approach. Conclusions are given in Section V.

II. Stacked-cascode circuit

The efficiency is one of the most crucial performance parameters of a power amplifier. An important factor limiting the achievable efficiency is the on-resistance of the power amplifier output stage. From the load-line theory a simple expression for the efficiency can be derived taking the on-resistance into account (here for a class B amplifier):

$$\eta = \frac{\pi}{4}\frac{1}{1+\frac{2}{V_{max}/(R_{on}I_{max})-1}}.$$

When connecting N multiple MOSFETs in series V_{max} as well as R_{on} increase by a factor of N. Thus V_{max}/R_{on} stays constant and the efficiency will not be compromised by stacking multiple MOSFETs.

The novel stacked cascode structure proposed in this paper is shown in Fig. 1. It consists of two cascode circuits comprising the MOSFETs M1/M2 and M3/M4. The gates of the cascode transistors M2 and M4 are RF shorted by the blocking capacitors C_B to the source nodes of M1 and M3, respectively. This way the transistors M1 and M2

978-1-4244-6241-4/978-1-4244-6242-1/
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act as standard cascode circuit while M3 and M4 form a floating cascode circuit. The cascode behavior results in a lower on-resistance and therefore in a higher efficiency of the structure compared to the HiVP configuration. Proper choice of the tuning capacitor C_{Tune} sets the voltage swing for the top cascode circuit so that the total output voltage is uniformly distributed across all four MOSFETs. This allows the voltages seen by M1-M4 to remain below the oxide breakdown voltage and the maximum voltage ratings imposed by hot carrier effects.

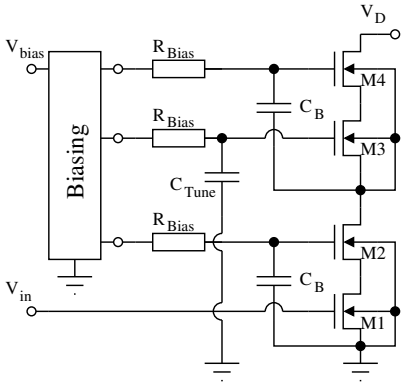

Fig. 1. Stacked cascode circuit comprising four MOSFETs, blocking/tuning capacitors and biasing

Another limiting factor is the breakdown of the drain diode of transistor M4 at high reverse voltages. High RF peak voltages (in the vicinity of the diode breakdown voltage) at the drain of M4 can lead to a current flow through the diode and to a clipping of the output voltage waveform. At higher RF peak voltages the drain diode will be destroyed. In order to avoid breakdown of the drain diode of M4 the cascode circuit formed by M3/M4 is realized in a p-well in n-well with the n-well biased to the supply voltage. The connection to the source of M3 forces the p-well to swing together with the top cascode circuit reducing the voltage across the drain diode of M4 by a factor of 2.

The circuit overall breakdown voltage is limited either by the gate oxide breakdown voltage ($4 \times V_{br,GOX}$) or by the diode and well breakdown voltages ($V_{br,diode} + V_{br,well}$). In the best case stacking of four MOSFETs leads to a four times higher overall breakdown voltage.

III. Measurement of load-pull test structures

A. DC and RF breakdown

To demonstrate the robustness of the stacked cascode topology DC breakdown measurements were performed, as well as RF measurements under optimum load conditions for increasing supply voltages.

The gate oxide of the thick oxide FET and diode/well breakdown voltages in the used technology are 7V and 10V, respectively. Thus, the circuit should be able to sustain a maximum output voltage of about 20V – limited by the breakdown of the N-well and the drain diode of transistor M4.

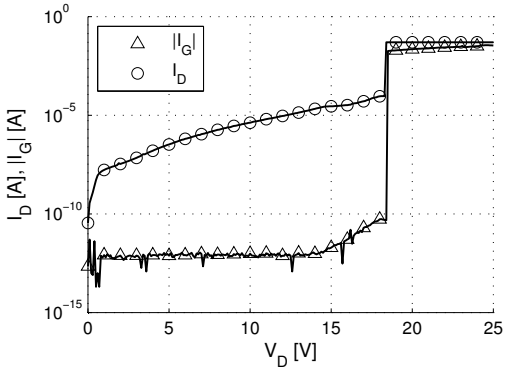

Fig. 2. Measured DC breakdown of the stacked cascode (gate-source voltage of transistor M1: $V_{gs,M1} = 0$V, bias voltage: $V_{bias} = 3/4 \times V_D$)

Fig. 2 shows the results of the DC breakdown measurement. To ensure proper distribution of the total drain voltage V_D across all devices, the bias voltage V_{bias} was swept during measurement along with V_D by setting $V_{bias} = 3/4 \times V_D$. The measured breakdown voltage of $V_{bd} = 18.4$V is slightly below the theoretical maximum.

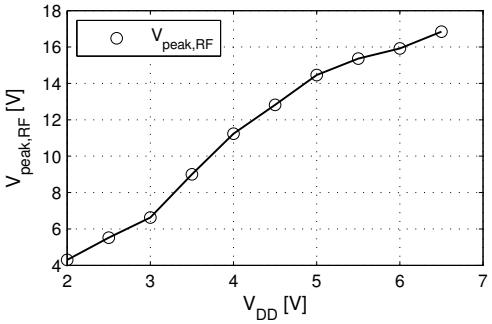

Fig. 3. RF peak voltage at increasing drain bias voltages

Using the possibilities of time-domain load-pull measurements, device breakdown under RF operation was evaluated. For each supply voltage level the amplifiers were operated in saturation at maximum output power. In Fig. 3 the reached peak RF voltage at the drain is plotted against the drain bias voltage V_{DD}. The circuit worked up to a drain bias voltage of 6.5V, which corresponds to a peak RF voltage of 17V; at $V_{DD} = 7$V degradation due to gate oxide breakdown of one of the four transistors was

observed. Extrapolating the measured curve the peak RF voltage reached levels of about 18V.

Under DC and RF stress the same breakdown voltages were measured. More importantly it is shown that circuits based on the stacked cascode approach can sustain the high peak voltages occurring in handset power amplifiers under load mismatch conditions.

B. RF performance

Fig. 4 and Table I compare the RF performance of three implemented PA stages. The measured PAE values for all the three PA stages are nearly the same. This result verifies the theoretical considerations in II. The output power increases by 6dB each time the number of FETs is doubled. This is because the drain bias voltage V_{DD} could also be doubled while keeping the stress on each single FET constant.

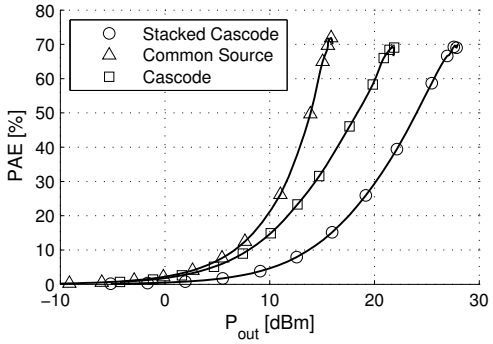

Fig. 4. Comparison of RF performance of a simple common-source stage, a cascode stage and the stacked cascode stage at $f = 900$MHz

TABLE I
MEASURED PERFORMANCE AT 900MHZ

	No. of stacked FETs à 7mm	V_{DD} [V]	P_{out} [dBm]	PAE [%]
Common-Source	1	0.9	15.9	71.9
Cascode	2	1.8	21.9	69.8
Stacked Cascode	4	3.6	28	69.9

The performance vs. frequency of the stacked cascode is plotted in Fig. 5. The circuit shows outstanding performance in the GSM low band at 900MHz and acceptable high efficiency in the GSM high band at 1.8GHz. At higher frequencies the PAE is limited due to the low unity-gain frequency ($\omega_u = 15$GHz) of the stacked-cascode using 230nm thick-oxide FETs. For higher frequency operation the gate length could be reduced or even thin oxide FETs could be used at the cost of circuit ruggedness.

Table II compares the measured performance of the presented stacked-cascode approach with the state-of-the-art. The circuit shows a performance in CMOS technologies

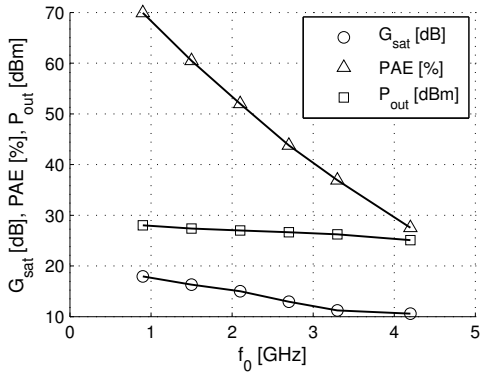

Fig. 5. PAE, gain and output power vs. frequency at $V_{DD} = 3.6$V for optimum load conditions for each frequency point

so far only reachable with special devices[1], [2]. Compared to other implementations using only standard devices [5] the efficiency of the stacked cascode is considerably higher.

TABLE II
COMPARISON WITH STATE OF THE ART

Reference	Technology	f [GHz]	P_{out} [dBm]	PAE [%]
[1]	Si-LDMOS	0.9	35	65
[2]	65nm CMOS using special EDMOS device	0.8	30	70
[5]	0.18μm CMOS	1	27.5	36.9
this work	**65nm CMOS, thick oxide FETs ($L_{Gate} = 230$nm)**	**0.9**	**28**	**69.9**

IV. A 31-DBM, CLASS-AB STACKED-CASCODE POWER AMPLIFIER

To show the feasibility of watt-level power amplifiers for GSM handset application, a differential power amplifier output stage including complete biasing, ESD protection and blocking capacitors in a flip-chip package was fabricated in a 65nm CMOS technology. A simplified block diagram of the chip and the test-board is shown in Fig. 6. The power amplifier occupies a total chip area of 0.6mm^2. The size of the output stage is 0.2mm^2.

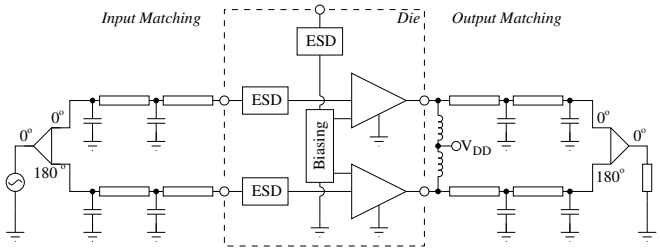

Fig. 6. Block diagram of chip and test-board

The matching at the amplifier input and output was realized on-board using grounded coplanar waveguides on a FR-4 substrate and SMD capacitors to form two-stage matching networks. The output matching was optimized for maximum PAE. Fig. 7 shows the complete test-board.

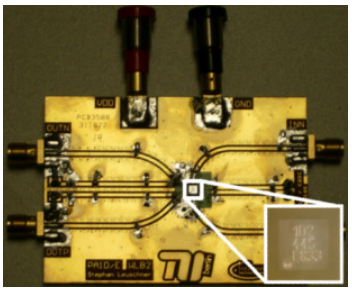

Fig. 7. Test-board and chip photograph

The power amplifier operates in classical class-AB mode. At 850MHz it delivers 31dBm output power at a power-added efficiency of 60.5% as shown in Fig. 8. The small-signal and saturation gain is 27dB and 16dB, respectively.

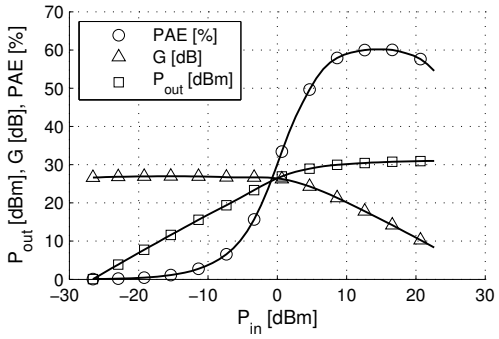

Fig. 8. Power amplifier performance at $f = 850$MHz

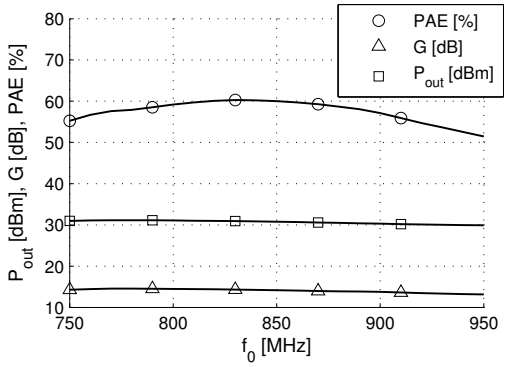

Fig. 9. Performance vs. frequency at $P_{in} = 14$dBm

The performance plotted versus frequency in Fig. 9 shows the maximum PAE of 61% at 830MHz. The PAE is always higher than 55% at frequencies ranging from 750MHz to 920MHz. In this range the output power is also equal or greater than 30dBm at a minimum saturation gain of 14dB.

The difference in maximum PAE compared to the load-pull measurements shown in Section III results from the losses in the on-board matching networks ($\Delta PAE \approx 5\%$) and a non-optimum ESD structure design ($\Delta PAE \approx 4\%$).

V. Conclusion

The presented stacked-cascode power amplifier topology uses only standard devices in a 65-nm CMOS process. The implemented stacked-cascode stage using 230nm thick-oxide MOSFETs has a breakdown voltage of 18.4V. The on-wafer load-pull measurements show a PAE of 69.9% at an output power of 28dBm at 900MHz. To the knowledge of the authors, this is the first CMOS power amplifier that is able to handle such high voltage levels using only standard devices with an efficiency so far only measured on special devices.

The GSM low-band power amplifier proves the feasibility of power amplifiers using the stacked-cascode topology. It delivers 31dBm output power at an efficiency of 61%.

Acknowledgements

The authors would like to thank Boris Kapfelsperger, Bernhard Sogl, Ronald Thueringer and Norman Wolf for constant support and their help during the measurements.

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