High-Efficiency LDMOS Power-Amplifier Design at 1 GHz Using an Optimized Transistor Model

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***Abstract*—A 10-W LDMOS harmonically tuned power amplifier at 1 GHz with state-of-the-art power-added efficiency of 80% is presented. The fundamental and second-harmonic load impedances are optimized for maximum efficiency while other harmonics are blocked by a low-pass load network. A simplified model of the transistor specialized for harmonically tuned and switched mode operations is proposed and used for the design. Good agreement between simulations and measurements is observed, indicating high accuracy of the model and design approach for these particular applications.**

***Index Terms*—Harmonically tuned, LDMOS, power amplifier (PA), switched mode.**

I. Introduction

A POWER amplifier (PA) is the most power-consuming block in any communication system and its efficiency is, therefore, very critical. High-efficiency PAs with a reasonable gain could be divided into two main categories. The first group consists of harmonically tuned versions of traditional class B and AB PAs, such as classes J or F [1]. In this group, the transistor is considered as a voltage-dependent current source. In the second group, however, the transistor is considered as a switch. Different switched mode PA classes have been defined, e.g., E, D, inverse-F, etc., which all have maximum theoretical efficiency of 100% [1], [2].

In practice, however, due to the nonideality of transistors, particularly the knee effect and large internal capacitances, achieving the theoretical efficiencies for high PAs at gigahertz frequencies is impossible. This fact is reflected in Table I, which shows the highest efficiency achieved in the low gigahertz frequency range with an output power of more than 5 W.

Table I also reflects the efficiency improvements in the later generation of LDMOS transistors. According to this table, PAs based on GaN HEMT transistors have not yet been able to demonstrate a power-added efficiency (PAE), which is significantly higher than LDMOS at about 1 GHz. At higher frequencies, the GaN devices outperform LDMOS because of the significantly lower capacitances. This is shown in Table I by the efficiency result achieved in [8] at 2 GHz.

TABLE I
HIGHEST PAE PUBLISHED AT $f \geq 1$ GHz WITH $P_{\rm out} \geq 5$ W

Device	Reference	PAE [%]	P_{out} [W]	f [GHz]
LDMOS	2003 [3] E	66	8	1
	2005 [4] inverse-F	74	12	1
	2006 [5] inverse-D	69	20	1
	2007 [6] F	78	5	1
	This work	80	10	1
GaN	2007 [6] inverse-F	79	9	1
	2007 [7] inverse-D	73	51	1.2
	2008 [6] inverse-F	83	6	1.2
	2007 [8] F	85	17	2

In this study, a harmonically tuned PA inspired by the class J concept [1] is presented. The class J PA topology presented in [1] is very useful for transistors with large output capacitance such as high-power LDMOS at gigahertz frequencies. In this approach, the second harmonic load impedance is tuned incorporating the device output capacitance. Other harmonics are left to be short circuited or capacitively loaded by the large-output capacitance of the device. The output network topology is a simple low-pass network with only the second harmonic and fundamental load impedance tuning. Hence, the name class J is only used to refer to the particular topology implemented rather than any specific harmonic terminations [1].

In order to design a high-power amplifier, an accurate transistor model specialized for the particular high-efficiency harmonically tuned PA application is needed. Negra *et al.* [9] recently presented a switch-based transistor model for a GaN HEMT. The model is based on a nonlinear representation of the drain–source resistance as a function of gate voltage with parasitics and linear capacitances added to represent the high-frequency effects. This allows an extraction, which is very simplified compared to models for linear amplifiers. However,

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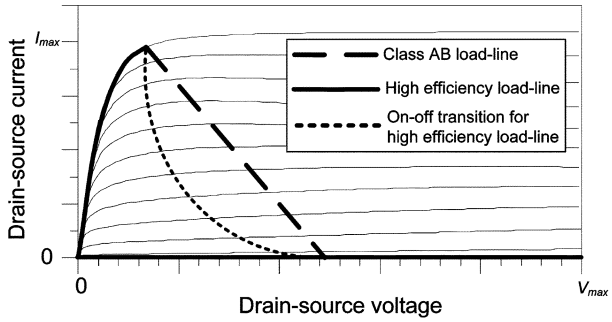


Fig. 1. Idealized transistor load-line trajectories illustrating the difference between traditional class AB and high-efficiency PAs. The dotted line represents the short transition time between on- and off-state in high-efficiency amplifiers.

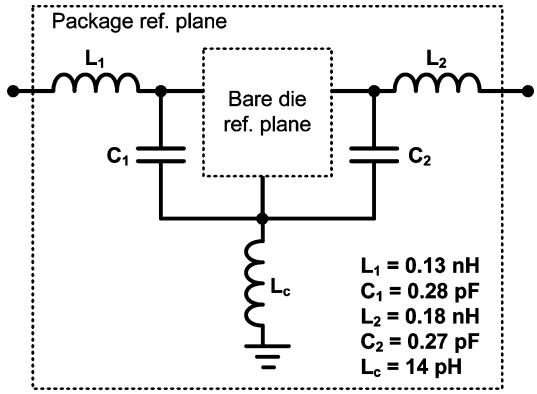


Fig. 2. Model for the package used for the transistor characterization.

due to the simplifications made, the model is not able to predict the high-frequency behavior in a PA very well, especially when the supply voltage and frequency are detuned from their original design values.

In this paper, a simplified transistor model optimized for harmonically tuned PAs such as F and J (first category), and switched-mode PAs (second category) is extracted and used in the design. The model is based on simplified expressions for the nonlinear currents and capacitances where the agreement in high-efficiency areas has been specifically stressed. The model allows the intrinsic waveforms to be studied in the PA design, and therefore, allows a careful investigation of the transistor operation.

II. Transistor Modeling for High Efficiency PAs

This section describes the transistor characterization and modeling procedure used for design of the high-efficiency PA presented.

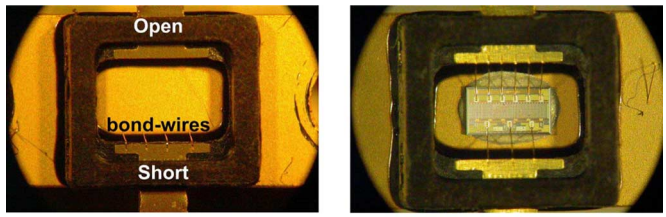
The need for a model specialized for high-efficiency harmonically tuned PA designs relates to the fact that the transistor mode of operation is fundamentally different compared to traditional linear class AB type of amplifiers. This is illustrated in Fig. 1, which compares the load line of a traditional class AB PA with the one in a high-efficiency PA.

Commercially available transistor models are normally optimized for class-AB operation, which means that the accuracy in the high-efficiency load-line region, shown in Fig. 1, is compromised. A consequence is also that commercially implemented models often suffer from convergence problems when used for switched-mode PA design [9].

Moreover, in order to eliminate the parasitics associated with packaged transistors, a bare-die approach is used in this study. This approach was also used in [8] where the transistor chip was wire bonded directly to the circuit. The reference plane of the transistor model is, therefore, set to the transistor chip surface. To facilitate a repeatable method for characterization of the bare-die devices to the chip surface reference plane, a package-based technique is developed.

A. Bare-Die Transistor Characterization Method

The bare-die characterization procedure may be summarized as follows. First, the transistor chip is mounted in a high-performance liquid-crystal polymer package (JT973C, RJR Polymers Inc., Oakland, CA). The package is then placed in a high-power test fixture (Inter-Continental Microwave, Chandler, AZ) during the characterization. The test fixture includes thru-reflect-line (TRL) calibration standards, which brings the reference plane to the tabs of the package. Finally, a model of the package is developed and used to deembed the influence of the package from the measurements. This finally brings the reference plane of the measurements to the bond wires of the transistor die. This procedure is similar to the one presented in [10], but uses measurements instead of 3-D electromagnetic simulations to find the package model parameters. Fig. 2 shows the topology used to model the package. The package model parameters are extracted with the help of three package standards: thru, short, and open. The thru and short standards are realized by adding bond wires between the package input–output and input–ground, respectively [see Fig. 3(a)].



(a) (b)

Fig. 3. (a) Short and open package standards. (b) Transistor die mounted in package during characterization.

Fig. 3(b) shows a 10-W NXP LDMOS transistor die mounted in the package. The product number for an unmatched packaged version of this transistor die is BLF6G21-10. This is also the same transistor used in the PA design. Once mounted according to the procedure above, dc and bias-dependent S-parameter measurements are used to characterize the bare-die device. Fig. 4 shows measured dc *I/V* characteristics. Square markers (□) are used to indicate the measurement points in the on- and off-states, which are considered most critical in terms of modeling for high-efficiency PAs according to Fig. 1. Note that the thermal effects are not dominant in these states, and therefore, static measurements are considered sufficient.

S-parameter measurements are performed at each of the points in Fig. 4 and forms the basis for the extraction of the new transistor model.

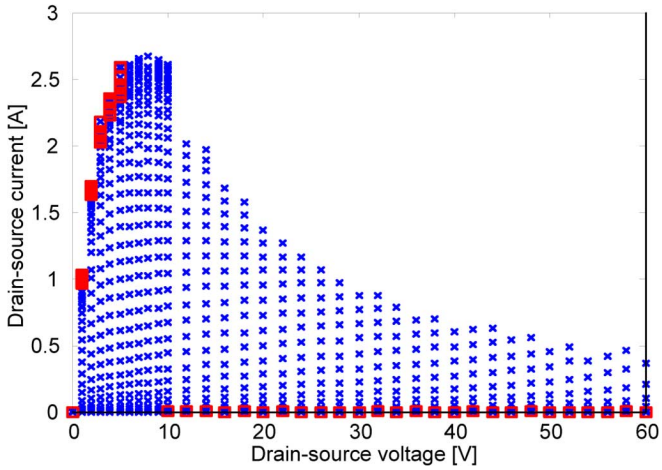


Fig. 4. Measured transistor dc characteristics (×). Points critical for high-efficiency PA operation are indicated with square markers (□).

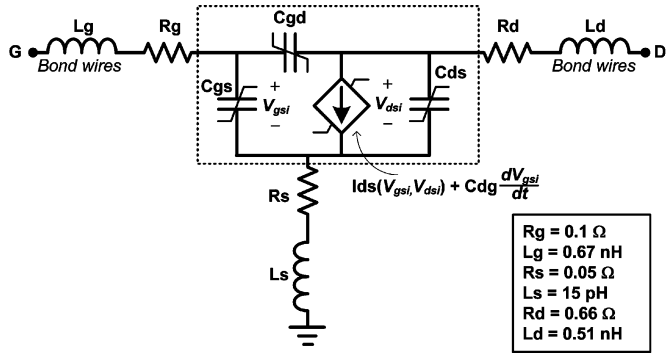


Fig. 5. Large-signal transistor model topology. The intrinsic bias-dependent part of the model is enclosed by the dashed rectangle.

B. Transistor Modeling

The model developed in this section is based on expressions that focus on accurately predicting the on and off areas of the transistor characteristics.

1) Model Topology: The model topology used is depicted in Fig. 5. Despite its relative simplicity, it has been found to accurately reproduce measured S-parameters to frequencies <6 GHz within all bias regions of interest.

A multibias optimizer-based extraction technique is then employed to extract the extrinsic parameters of the model [11]. This method has previously proven to give reliable and accurate results with LDMOS devices [12]. The resulting values of the extrinsic parameters are given in Fig. 5. Note that $R_s + R_d$ describes what is referred as the drain–source on-resistance $(R_{ds,on})$, which can also be identified from the slope of the *I/V* curve in Fig. 6.

The extrinsic parameters are then fixed and the intrinsic parameters are extracted versus bias using a similar optimization technique minimizing the difference between measured and modeled S-parameters. The results are used for the large-signal modeling.

2) Nonlinear Drain Current: The model equation used to approximate the intrinsic nonlinear current source in Fig. 5 has been developed having the high-efficiency load line of Fig. 1 in mind. This means that the model accuracy in the on region, i.e., where drain–source voltage is low and the drain current is high, is of main consideration. Nevertheless, since the transistor is operated part of the time in other regions, it is still important to base the model on equations that give physically reasonable results also in the intermediate transition regions. The model used in this work is, therefore, based on the $I_{\rm ds}$ model equations presented in [12]. This model has also been successfully used by others for LDMOS and GaN devices [13], [14] and is proven to predict practical device characteristics with a reasonable number of model parameters. The model equation in this model is in its basic form given by the following expression:

$$I_{\rm ds} = \frac{\beta V_{g,\rm eff}^2}{1 + V_{g,\rm eff}/VL}(1 + \lambda V_{\rm ds}) \tanh\left(\frac{\alpha V_{\rm ds}}{V_{g,\rm eff}}\right) \quad (1)$$

where $V_{g,\rm eff}$ is an effective gate–source voltage $(V_{\rm gs})$ used both to describe exponential characteristics in the sub-threshold region, and saturation of the drain current at high $V_{\rm gs}$ [12].

In terms of modeling the on region, the characteristics are mainly determined by the $\tanh$ function and the α parameter. The $V_{g,\rm eff}$ used in the denominator of the $\tanh$ function was introduced in [15] to model the relatively smooth resistive to saturation transition observed in LDMOS devices. In this study, we have found that the agreement in the on region can be further improved by replacing the tanh function with the following arctan-based model expression:

$$I_{\rm ds} = \frac{\beta V_{g,\rm eff}^2}{1 + V_{g,\rm eff}/VL}(1 + \lambda V_{\rm ds}) \frac{2}{\pi} \arctan\left(\frac{\pi \alpha V_{\rm ds}}{2V_{g,\rm eff}}\right) \quad (2)$$

where the scaling factor $2/\pi$ has been used for normalization purposes.

Fig. 6 shows measured and modeled dc $I_{\rm ds}/V_{\rm ds}$ characteristics in the knee region when the new model is used. As shown, the model gives a good agreement with the measurements. It should be noted that a simple electrothermal self-heating model has been used to take the thermal effects into consideration [12].

The nonlinear current model parameters, including the thermal effects, are extracted using a manual fitting procedure where static dc and small-signal parameters (g_m and $g_{\rm ds}$) are

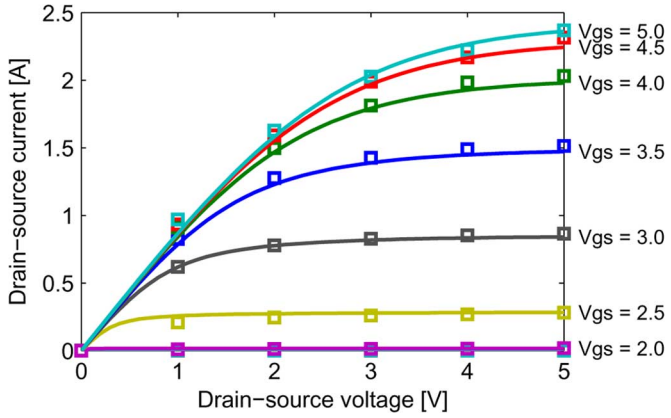
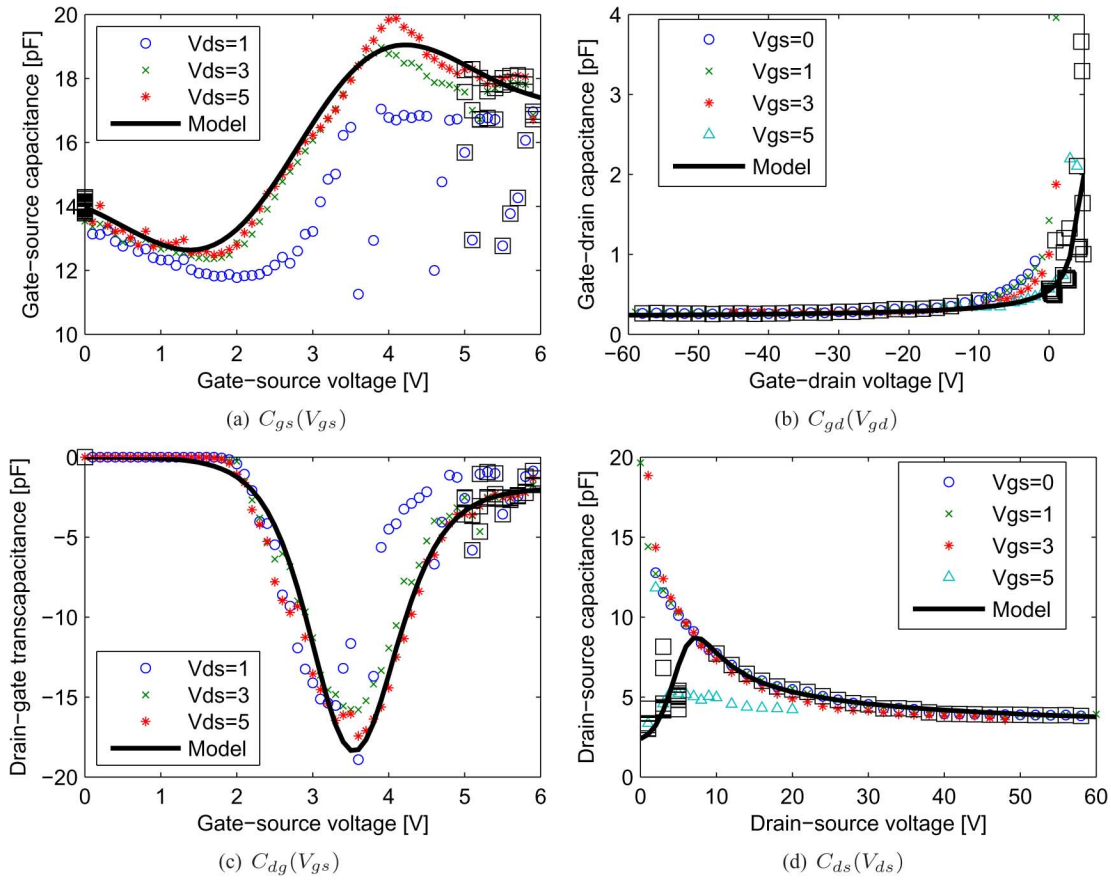


Fig. 6. Comparison between measured (markers) and modeled (lines) drain–source current in the on-state region.

TABLE II
EXTRACTED $I_{\rm ds}$ CURRENT SOURCE MODEL PARAMETERS CORRESPONDING TO THE MODEL IN (2)

β	V_{t0}	VST	λ	α	VL	$VK0$	Δ	$plin$	$psat$	γ	γ_{sat}	R_{th}	C_{th}	β_1
2.61	2.0	0.15	2E-3	1.85	1.7	1.9	0.65	0.8	1.3	-1E-3	8E-3	1.8	1E-4	4.5E-3



(a) $C_{gs}(V_{gs})$ (b) $C_{gd}(V_{gd})$ (c) $C_{dg}(V_{gs})$ (d) $C_{ds}(V_{ds})$

Fig. 7. Comparison between measured (markers) and modeled (lines) capacitance values versus bias. Thin square markers (□) are inserted in the plots to indicate operating voltages corresponding to the transistor on and off regions.

fitted to measurements in the on region. The complete set of model parameters are summarized in Table II.

3) Nonlinear Capacitances: Simplified models are derived for the nonlinear capacitances following the same procedure as for the current source above, meaning that only bias points in the on and off regions are considered. Separate models are derived to fit the bias-dependent small-signal capacitances $C_{\rm gs}$, C_{gd}, and $C_{\rm ds}$. As a simplification, each of the corresponding nonlinear capacitance models are set to depend only on the voltage across them. The small signal trans-capacitance $C_{\rm dg}$, which is needed for charge conservation [16], is also extracted and modeled using a function that depends only on $V_{\rm gs}$. As a consequence, the complete nonlinear transistor model, shown in Fig. 5, is also charge conservative [16].

Fig. 7 shows the extracted and modeled small-signal capacitances versus bias. For $C_{gd}(V_{gd})$ and $C_{\rm ds}(V_{\rm ds})$, the depletion capacitance model in [17] is adopted. The empirical models used for $C_{\rm gs}$ and the trans-capacitance $C_{\rm dg}$ are given as follows:

$$C_{\rm gs}(V_{\rm gs}) = a_0 + a_1 V_{\rm gs} + a_2 (V_{\rm gs} - a_3)\, e^{-a_4 (V_{\rm gs} - a_3)^2} \tag{3}$$

$$C_{\rm dg}(V_{\rm gs}) = \frac{b_0 - b_1 V_{\rm gs}}{\cosh^2 [b_2 (V_{\rm gs} - b_3)]} - b_1 \frac{1 + \tanh [b_2 (V_{\rm gs} - b_3)]}{b_2} \tag{4}$$

where the a and b parameters are extracted by manual fitting.

C. Model Verification

The accuracy of the implemented model is evaluated by comparing simulated and measured S-parameters versus bias. A normalized error metric, ϵ, is thereby defined as

$$\epsilon = \sqrt{\sum_{j,k \in \{1,2\}} \frac{1}{\alpha_{jk}} \sum_{i \in F} \left| S_{jk}^{\rm meas}[i] - S_{jk}^{\rm mod}[i] \right|^2} \tag{5}$$

$$\alpha_{jk} = 4N \max \left\{ \max \left| S_{jk}^{\rm meas} \right|^2, 0.01^2 \right\} \tag{6}$$

where F represents the measurement frequency range (in this case, 50 MHz–5 GHz). The factor 0.01 used with α_{jk} is included to minimize the effects of measurements error when $|S_{jk}| < -40$ dB.

The S-parameter modeling error is displayed versus bias in Fig. 8. This figure clearly shows that there is a good agreement

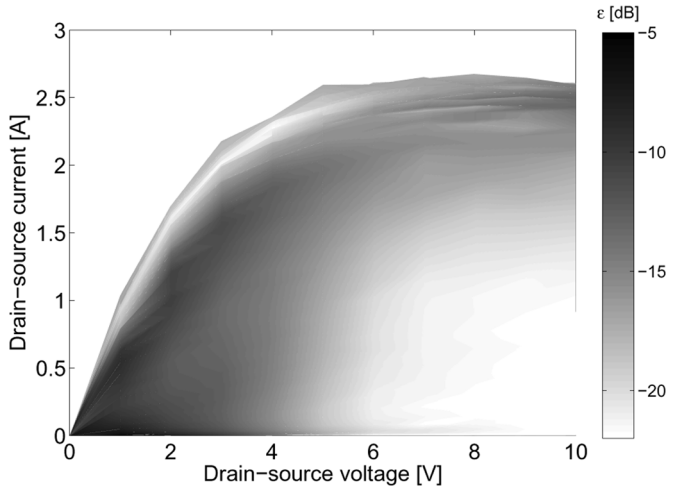


Fig. 8. Evaluation of normalized error ϵ between measured and modeled S-parameters versus bias. Brighter areas represent better agreement.

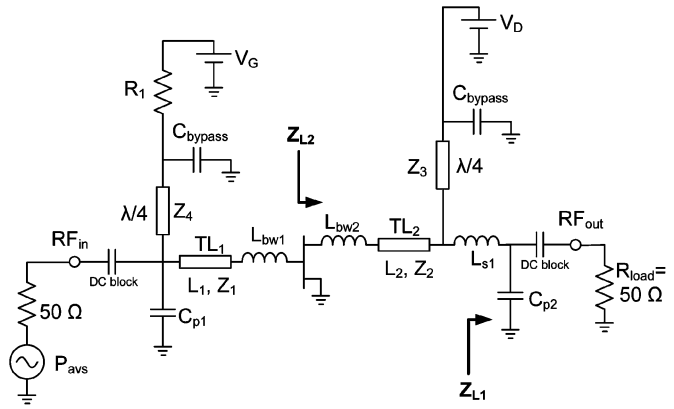


Fig. 9. Topology of the PA.

between modeled and measured S-parameters, particularly in the regions close to the load-line for high-efficiency PAs.

III. PA Design With Second Harmonic Load Impedance Tuning

In this section, the PA design based on the extracted model is presented. As mentioned before, a bare die instead of a packaged transistor is used in order to reduce the parasitics as much as possible and facilitate harmonic impedance optimization at the transistor output reference plane.

The PA topology is shown in Fig. 9. $L_{\rm bw1}$ and $L_{\rm bw2}$ are the input and output bondwire inductances, respectively. In order to facilitate harmonic impedance optimization at 1 GHz, avoiding narrowband, and therefore, sensitive harmonic matching, these inductances should be lower than 0.2 nH. This is done by reducing the space between the bonding pads on the chip and the printed circuit board (PCB) lines as much as possible. The thickness of the metal carrier used is, therefore, carefully adjusted to align the surface of the chip to the PCB lines. The substrate is a Rogers Duroid 5870 and the PCB lines are gold plated to facilitate bonding directly to the transistor chip. A photograph of the constructed PA is shown in Fig. 10.

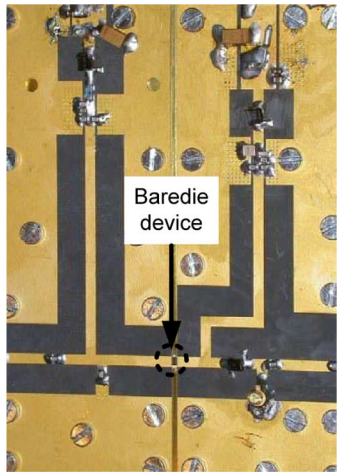


Fig. 10. Photograph of the implemented PA.

TABLE III
Normalized Optimum Load Impedances Realized by the Output Matching Network in Fig. 9

	f_0	$2f_0$	$3f_0$
$\frac{Z_{L2}}{50}$	0.18+j0.42	0.01+j0.49	0.14+j0.8

The input matching network consists of a parallel capacitor $C_{p1} = 8.2$ pF, and a 50-Ω transmission line (TL_1). The resistor R_1 is included to ensure stability at low frequencies.

The output matching network consists of a parallel capacitor $C_{p2} = 4.7$ pF, a series inductor $Ls1 = 2.5$ nH, and a transmission line (TL_2). C_{p2} transforms the 50-Ω load impedance to $Z_{L1} = 8.4 + j17.1\ \Omega$ at the fundamental frequency (f_0). $Ls1$ together with TL_2 then transform Z_{L1} to Z_{L2}. The optimum second harmonic load impedance is realized by the $\lambda/4$ stub and TL_2. Note that the stub is open at f_0, but short circuited at $2f_0$. The length and width of TL_2 decides the value for Z_{L2} at $2f_0$. Note that the circuit components on the right side of the $\lambda/4$ stub do not have any effect on the second harmonic load impedance. Therefore, C_{p2} and L_s can be varied to find an optimum Z_{L2} at f_0 without affecting the second harmonic termination. The other harmonic impedances are not optimized and are left to be short circuited by the transistor output capacitance. This approach is particularly useful for realizing high-efficiency PAs with high-power LDMOS devices, which have a large output capacitance.

The optimum load impedance (Z_{L2}) realized by the output matching network is normalized to 50 Ω and summarized in Table III for frequencies f_0, $2f_0$, and $3f_0$. Note that these values are provided by the external matching network. The intrinsic load impedance presented to the voltage-dependent current source of the transistor can, however, be completely different due to the large nonlinear output capacitance of this transistor. The ideal short, open, and other harmonic impedance conditions in literature are defined for the intrinsic current source of transistor, and therefore, cannot be compared with the values in Table III. The optimum values of Z_{L2} at f_0 and $2f_0$ in Table III were found by harmonic load–pull simulations

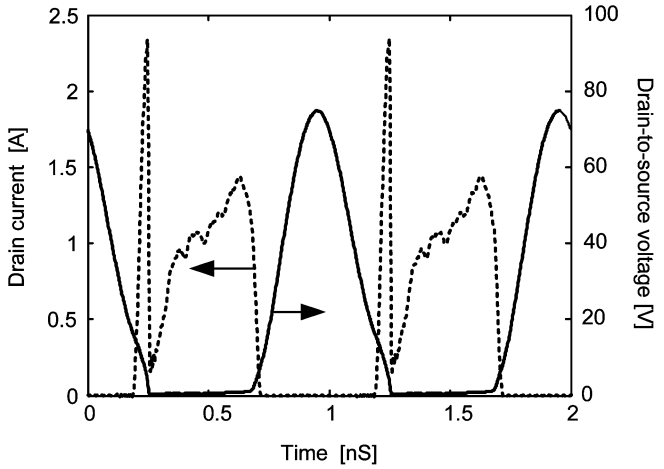


Fig. 11. Simulated intrinsic current and voltage waveforms of transistor resulting in 80% PAE at 1 GHz.

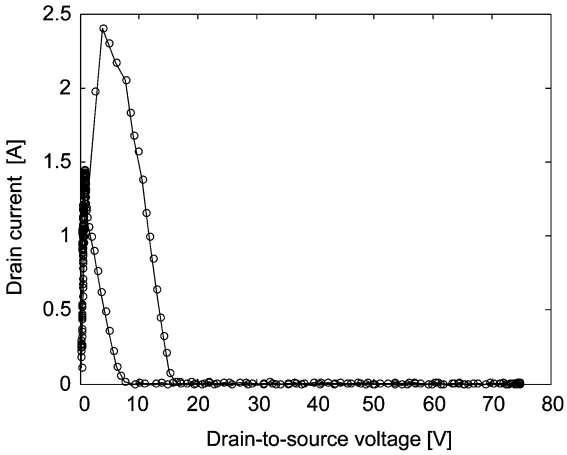


Fig. 12. Simulated dynamic load line of transistor at its intrinsic reference plane resulting in 80% PAE at 1 GHz.

at the transistor output reference plane to shape the intrinsic waveforms, provided by the developed model, for a class-J PA operation [1].

Fig. 11 shows the simulated intrinsic output voltage and current waveforms of the transistor, accessible by the internal nodes of the developed model, corresponding to 80% PAE. The voltage peak value in this figure is 75 V, which is equal to the typical breakdown voltage specified by the transistor manufacturer. The corresponding simulated dynamic load line of the device is shown in Fig. 12. The density of the circle markers indicates the relative amount of time the transistor is operated in different regions. Simulations show that very sharp, but narrow current peaks occur in transition between off- and on-states. However, they do not have any significant effect on PA performance due to their very short duration.

According to Fig. 12, the transistor is operated mostly in the switching region where the model is particularly optimized. Therefore, a good agreement between measurements and simulation is expected. Simulation results are presented in Section IV where they are compared with measurements.

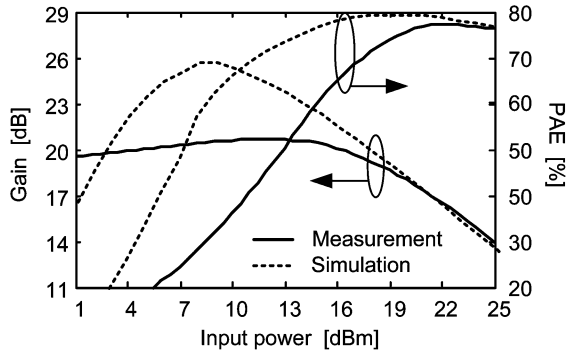


Fig. 13. Gain and PAE versus input power at 1 GHz. Drain and gate bias voltages are 20 and 2 V, respectively.

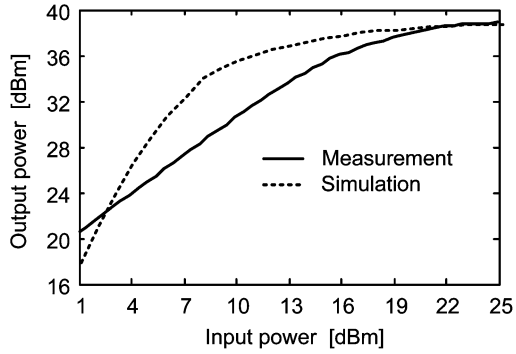


Fig. 14. Output power versus input power at 1 GHz. Drain and gate bias voltages are 20 and 2 V, respectively.

IV. Measurements Versus Simulations

Fig. 13 shows the simulated and measured gain and PAE versus input power at 1 GHz. There is a very good agreement between the simulated and measured results close to the peak efficiency operation.

The simulated and measured output power versus input power at 1 GHz are shown in Fig. 14. The agreement region is similar to that in Fig. 13.

As the input power is reduced and the device is less overdriven, the harmonic contents of its output waveforms are no longer strong enough to be able to form high-efficiency switching conditions. Therefore, the device operation extends outside of the region where the model is optimized and the simulation results start to deviate from measurements. This is a fact that the PA designer should be aware of. The model is mainly optimized for switched mode or harmonically tuned overdriven operations where conventional models lack accuracy and fail to provide convergence in simulations.

Fig. 15 shows the drain bias voltage sweep results for 23 dBm of input power. The measured results agree very well with simulations when the input drive level is high enough, as expected. As shown in Fig. 15, 80% PAE with 10-W output power is measured when the drain bias is 24 V. This presents a state-of-the-art result for LDMOS PAs at 1 GHz, which was accurately predicted by simulations.

Fig. 16 shows the frequency sweep results for a fixed input power level. The measured results are accurately predicted by simulations based on the model presented.

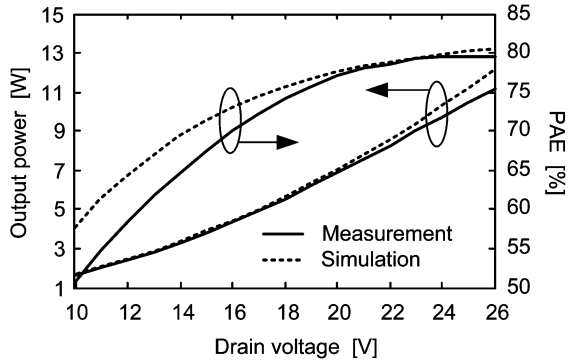


Fig. 15. Output power and PAE versus drain bias voltage at 1 GHz. Gate bias voltage and input power are 2 V and 23 dBm, respectively.

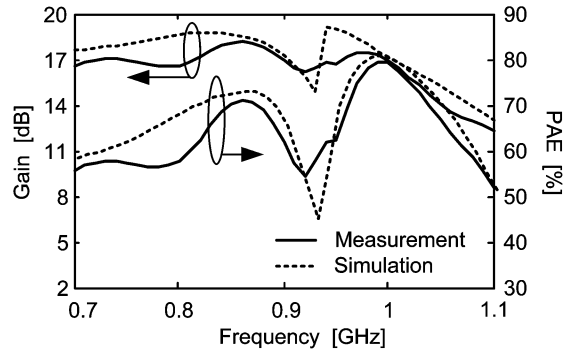


Fig. 16. Gain and PAE versus frequency. Drain and gate bias voltages, and input power are 24 V, 2 V, and 23 dBm, respectively.

V. Conclusions

An extensive design procedure for efficiency optimized harmonically tuned PAs has been presented. The procedure is based on a bare-die mounting technique that minimizes the influence of device parasitics, and therefore, takes full advantage of recent device technology improvements. A specialized transistor model was also developed and used for accurate prediction of measured results in high-efficiency PA applications.

The design procedure was demonstrated with a high-efficiency PA design using the LDMOS transistor die from NXP Semiconductors, Nijmegen, The Netherlands. The measured results, which demonstrate 80% PAE and 10-W output power at 1 GHz, represent state-of the-art and verifies the effectiveness and success of the design and modeling approach presented.

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