A 1.8-GHz CMOS Power Amplifier Using Stacked nMOS and pMOS Structures for High-Voltage Operation

Ki Yong Son, *Student Member, IEEE*, Changkun Park, *Member, IEEE*, and Songcheol Hong, *Member, IEEE*

***Abstract*—A class-E power amplifier is proposed in this study. It uses both nMOS and pMOS as switching devices to reduce the voltage stress of each transistor. A voltage-combining scheme with nMOS and pMOS is proposed, and a transformer is designed using this scheme. The power amplifier is implemented in a 0.18-μm RF CMOS process. Measurements show a maximum output power of 30.2 dBm with 36.8% power-added efficiency at a 3.3-V supply voltage. The power amplifier sustains a supply voltage of up to 3.9 V.**

***Index Terms*—Cascode amplifiers, CMOS, differential, power amplifiers, transformers.**

I. Introduction

RECENT progress toward single-chip radios has been made owing to the development of the CMOS process. For example, shortening the gate length leads to improvement in the MOSFET performance, as measured by the variables f_t and $f_{\max}$. While other small-signal RF blocks benefit from the development of CMOS technology, the lowered supply voltage makes it more difficult for RF power amplifiers to generate higher output power. In fact, the power amplifier is considered one of the bottlenecks in the performance of a true single-chip radio. A power amplifier in a CMOS process has weak points compared to its counterpart in compound processes due to such factors as the lossy substrate, low quality (Q) factor, and low breakdown voltage of active devices. Thus, designing a CMOS power amplifier remains a challenging task. Nevertheless, several studies have shown that voltage-combining methods provide a viable means of achieving watt-level output power in CMOS power amplifiers [1]–[6].

CMOS power amplifiers are associated with breakdowns of their active devices, especially in class-E amplifiers. Among switching mode power amplifiers, a class-E power amplifier is preferred due to its simple configuration and high efficiency. However, this type of amplifier requires a large drain voltage swing, which contributes to device stress. The amplitude of the drain voltage swing of a class-E power amplifier is approximately 3.6 times the supply voltage [7]; this degrades the performance of CMOS power amplifiers. Therefore, it is necessary to reduce the voltage swing of each active device for reliable operation.

CMOS power amplifiers that relax device stress have been reported in several studies. The self-biased cascode structure shows reduced voltage swings on each device without using thick-gate–oxide transistors [8]; these structures are used widely in linear power amplifiers [9], [10]. The stress becomes more severe in switching mode power amplifiers. A stacked class-D power amplifier under high supply voltage has also been reported [11]. The structure maintains the same amount of device stress, but allows higher supply voltage than that of an unstacked structure. However, with class-E power amplifiers, a large drain voltage swing requires a more reliable structure. A concentric distributed active transformer (DAT) structure is proposed for high voltage operation of class-E power amplifiers, which also minimizes substrate loss and gain reduction [3].

In this paper, both nMOS and pMOS devices are used to divide the voltage stress by sharing the voltage swing. It has been reported that pMOS devices can be used successfully as switching devices in a class-E power amplifier [12], [13]. The proposed power amplifier uses both nMOS and pMOS as switching devices, which are located in the current path from the supply voltage to the ground. The output voltage swing is divided into the drain voltage swing of the nMOS device and that of the pMOS device. Therefore, the drain–source voltage of each device can be reduced.

In Section II, the proposed structure is presented. It is then compared with a conventional class-E power amplifier that uses only one switching device in the current path. In Section III, the method of combining the voltage from each device is presented. The voltage-combining method in the proposed power amplifier is analyzed, and a transformer that combines the voltages between the nMOS and pMOS devices is proposed. The circuit configuration of the power amplifier is then explained in detail, and simulation results are presented in Section IV. Measurement results are presented in Section V, and conclusions are given in Section VI.

II. Principle of Operation

A. Conventional Class-E Amplifier

Fig. 1 shows a conventional class-E power amplifier that uses a transmission line transformer as an output matching network. The transmission line transformer is widely used in

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K. Y. Son and S. Hong are with the School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: kiyong.son@gmail.com; schong@ee.kaist.ac.kr).

C. Park is with the School of Electronic Engineering, Soongsil University, Seoul 156-743, Korea (e-mail: pck77@ssu.ac.kr).

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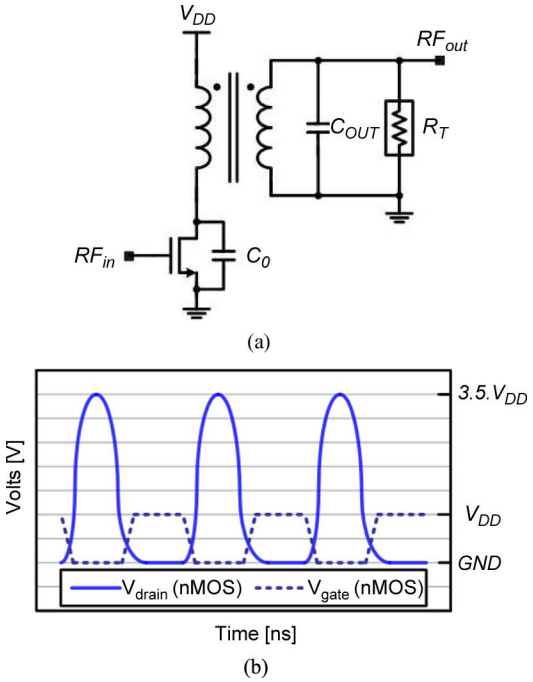

Fig. 1. (a) Schematic of a conventional class-E power amplifier that uses a transformer as an output network. (b) Ideal voltage waveforms at the gate and drain.

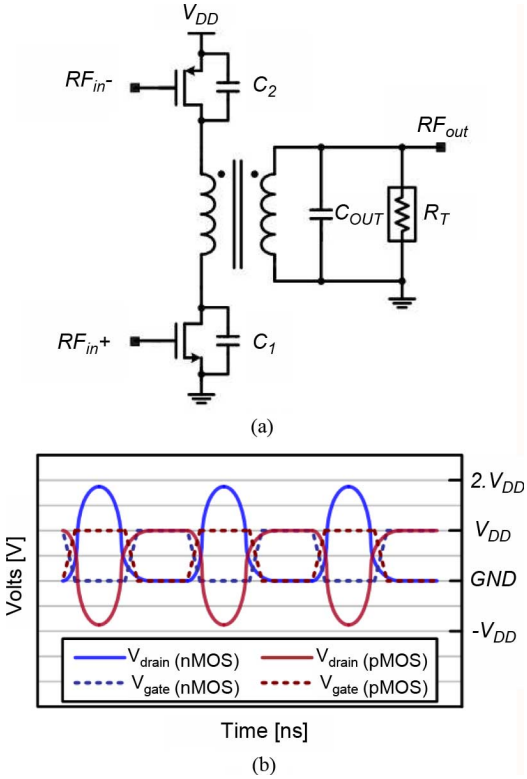

Fig. 2. (a) Schematic of the proposed class-E power amplifier. (b) Ideal voltage waveforms at the gate and drain.

CMOS power amplifier designs to combine the output powers from multiple pairs of amplifiers [1]–[3], [14]. In Fig. 1(a), the sum of the shunt capacitor and the transistor output capacitance is absorbed into C_0. These capacitances, $C_{\rm OUT}$, and the transmission line transformer constitute the load network of a class-E power amplifier. In Fig. 1(b), the operation of a class-E power amplifier is shown in terms of its gate and drain voltage waveforms. When the transistor is on, the drain voltage of nMOS is $V_{\rm DS(on)}$. Theoretically, this value should be close to zero so that its performance will remain efficient. When the transistor is off, the drain voltage increases to its maximum voltage and decreases to zero before the transistor is turned on again.

According to an early study [15], the peak drain–source voltage and the drain efficiency of a class-E amplifier can be estimated as follows:

$$\begin{aligned} V_{\rm DS,peak} &= V_{DD} + \left[2\pi \arcsin\left(\frac{\pi^2}{4}+1\right)^{-1/2} - 1\right] \\ &\quad \cdot \left[V_{DD} - V_{\rm DS(on)}\right] \\ &= 3.562 \cdot V_{DD} - 2.562 \cdot V_{\rm DS(on)} \end{aligned} \tag{1}$$

$$\eta_{\rm drain} = \frac{1 - \dfrac{(2\pi A)^2}{6} - \dfrac{V_{\rm DS(on)}}{V_{DD}}\left(1 + A - \dfrac{(2\pi A)^2}{6}\right)}{1 - \dfrac{(2\pi A)^2}{12}}. \tag{2}$$

Here, $A \equiv (1 + 0.82/Q_L) \cdot f \cdot t_f$, and Q_L is the network-loaded value of Q, f is the operating frequency, and t_f is the drain current fall time during transistor turnoff. V_{DD} is the supply voltage, and $V_{\rm DS(on)}$ is the drain–source voltage when the device is on.

According to (2), $V_{\rm DS(on)}$ should be minimized for high efficiency; however, this will increase the peak drain–source voltage, as shown in (1). In some designs, the peak drain–source voltage may exceed the breakdown voltage of CMOS transistors. In actuality, the supply voltage is set to be 3.3 V or higher in handset applications, which is not in the safe operating region of a submicrometer MOSFET. Therefore, a new configuration is required to reduce $V_{\rm DS,peak}$ without increasing $V_{\rm DS(on)}$.

B. Proposed Class-E Amplifier

Fig. 2 shows the proposed power amplifier with a transmission line transformer. The purpose of the structure is similar to the concentric DAT structure in [3]. Generally, a power amplifier uses one switching device. By adding another switching device in the path from the supply voltage to the ground, the generation of RF output power takes place at two nodes. In the proposed power amplifier, the additional switch is directly connected to the supply voltage so additional choke inductor is not required. The pMOS device is used for the pull-up device because it can avoid the voltage drop problem that the pull-up nMOS has. The output voltage swing in a conventional power amplifier is split into two voltage swings at the drain nodes of nMOS and pMOS in the proposed structure. A voltage-combining method between nMOS and pMOS simplifies the amplifier structure, and there is no V_{DD} port in the primary part of the transformer. The simplified layout is explained in Section III. Instead of lowering V_{DD}, the proposed class-E amplifier reduces the drain–source voltage of each active device compared to that of a conventional

class-E amplifier under the same supply voltage. In other words, a higher supply voltage can be applied to the proposed class-E amplifier if the drain–source voltage of the active device is equal to that of a conventional class-E amplifier.

In Fig. 2(a), the sums of shunt capacitors and the output capacitance of the nMOS and pMOS devices are absorbed into C_1 and C_2, respectively. These capacitances, C_{OUT}, and the transmission line transformer constitute the load network of the proposed class-E power amplifier. The operation is similar to that of a conventional structure. The voltage waveforms of the power amplifier are shown in Fig. 2(b). The active devices in this structure also follow the switching operation, as in other switching mode power amplifiers. When both transistors are on, the drain voltage of nMOS is $V_{\mathrm{DS(on,nmos)}}$ while that of pMOS is $V_{DD} - |V_{\mathrm{DS(on,pmos)}}|$. Here, V_{DD} is the supply voltage, and $V_{\mathrm{DS(on,nmos)}}$ and $V_{\mathrm{DS(on,pmos)}}$ are the turn-on drain–source voltages of nMOS and pMOS, respectively. These values should be close to zero and V_{DD}, respectively, to ensure good efficiency. When the transistors are off, the drain voltage of nMOS increases to its maximum voltage. It also decreases to zero before nMOS is turned on again. At the same time, the drain voltage of pMOS decreases to its minimum voltage and increases to V_{DD} before pMOS is turned on again.

As the supply voltage is fixed, the relationship between the peak drain–source voltages of nMOS and pMOS is complementary. If more output power is generated at the drain of nMOS, less output power is generated at the drain of pMOS. In such a case, the peak drain–source voltage of nMOS is larger than that of pMOS. By the proper selection of the capacitance values C_1 and C_2, the drain voltage waveforms of nMOS and pMOS can be symmetric; hence, equal amounts of voltage stress are applied to both nMOS and pMOS. The proposed class-E amplifier is similar to a class-D amplifier in that it uses both nMOS and pMOS as switching devices. A major difference with a class-D power amplifier is that both nMOS and pMOS are turned on and off simultaneously in the proposed structure. Moreover, the drain voltage waveforms of the proposed structure follow that of a class-E operation.

III. Voltage-Combining Method

The proposed amplifier is designed with a differential structure to create a virtual ground and to prevent gain reduction that can be caused by bonding wire connections to an external ground on a printed circuit board (PCB) [16]. In addition, to ensure a large output power, the voltages from two differential amplifiers are combined through the transmission line transformer. A 1 : 1 transmission line transformer is analyzed to explain the voltage-combining method in both a conventional and the proposed power amplifier. In the proposed power amplifier, the primary part of the transformer forms an inductor that connects the drains of nMOS and pMOS. Through the use of magnetic coupling, the voltages that arise in the primary parts of the transformer are delivered to the secondary part. The implemented structure of the power-combining transformer is then explained. A power-combining transformer is proposed to combine the voltages between nMOS and pMOS.

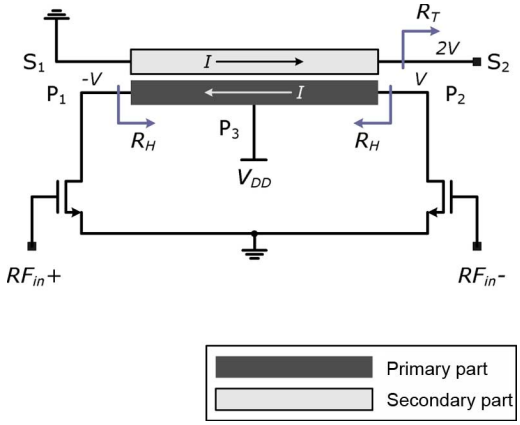

Fig. 3. Equivalent circuit of the 1 : 1 transmission line transformer for a conventional nMOS-based power amplifier.

A. Voltage-Combining Method in a Conventional Class-E Amplifier With Only nMOS Devices

To form a differential structure, one primary part is needed in the conventional nMOS-based power amplifier, as shown in Fig. 3. Two ports, P_1 and P_2, are connected to the drains of the nMOS devices that form a differential pair. The drain voltages of the differential pair are denoted as V and $-V$. The opposite signs indicate that they are out-of-phase signals. The supply voltage is applied to port P_3, the midpoint of the primary part. It is assumed that port S_1 is connected to the ground and that port S_2 is connected to a 50-Ω terminal. If the current flows from P_2 to P_1, the same amount of current flows through the secondary part in the opposite direction due to magnetic coupling. This coupling causes the voltage difference between P_1 and P_2 to between S_1 and S_2. The equivalent resistance R_H and R_T can be calculated by

$$R_H : R_T = \frac{V}{I} : \frac{2V}{I} = 1 : 2 = 25\,\Omega : 50\,\Omega \tag{3}$$

where R_H is the load impedance seen by one drain node in the nMOS-based power amplifier and R_T is the impedance of the terminal.

B. Voltage-Combining Method in the Proposed Class-E Amplifier With Both nMOS and pMOS Devices

1) Differential Structure: The relationship between the primary part and the secondary part of the transformer can be analyzed in the same manner. However, two primary parts are required in the differential structure of the proposed amplifier. One differential amplifier has differential pairs of both nMOS and pMOS; hence, there are four drain nodes. In Fig. 4, ports P_{1N} and P_{2N} are connected to two drains of the nMOS devices that form a differential pair. As the inputs of two devices in a differential pair are out of phase, the drain voltages appearing at P_{1N} and P_{2N} are also out of phase. Similarly, ports P_{1P} and P_{2P} are connected to two drains of the pMOS devices that also form a differential pair; the drain voltages appearing at P_{1P} and P_{2P} are also out of phase.

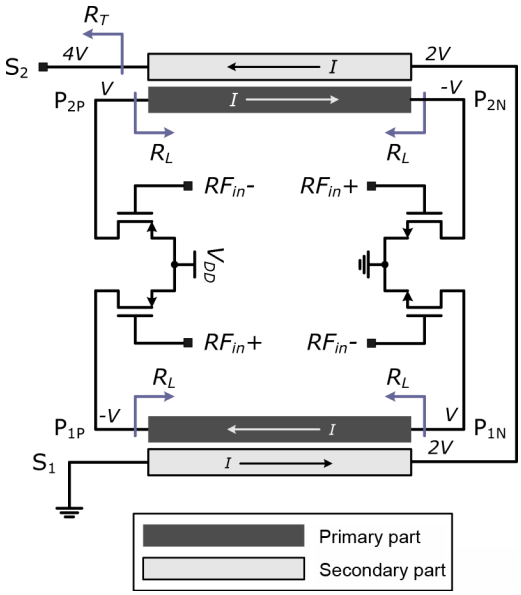

Fig. 4. Equivalent circuit of the 1 : 1 transmission line transformer for the proposed power amplifier.

Although two devices at P_{1N} and P_{2N} or at P_{1P} and P_{2P} form a differential pair, they cannot be connected through the transformer, unlike in a conventional nMOS-based power amplifier, because the two active devices connected through the transformer are the nMOS device and the pMOS device in the proposed structure. Instead, two types of devices at P_{1N} and P_{1P} or at P_{2N} and P_{2P} are connected through the primary part of the transformer, as shown in Fig. 4. The drain voltages at P_{1N} and P_{1P} or at P_{2N} and P_{2P} are also out of phase, as the out-of-phase signals should be applied to the gates of nMOS and pMOS to turn on and off both transistors simultaneously.

2) Node for the Power Supply: In addition, the transmission line transformer used in this work has no V_{DD} port, because the two ports of the primary part are connected to the drains of nMOS and pMOS, respectively. Instead, the supply voltage is connected to the source of pMOS, and dc power is supplied during the turn-on period of the transistors.

3) Operation of the Amplifier: If it is assumed that the output powers at the drains of nMOS and pMOS are identical, the two peak drain–source voltages of nMOS and pMOS would be equal and the operation of the transformer would be similar to that of a transmission line transformer in the conventional nMOS-based amplifier, where two voltages at two terminals have the same magnitude and are out of phase; i.e., they are inherently symmetric. Again, it is assumed that port S_1 is connected to the ground and that port S_2 is connected to a 50-Ω terminal. The equivalent resistance R_L and R_T can be calculated by

$$R_L : R_T = \frac{V}{I} : \frac{4V}{I} = 1 : 4 = 12.5\,\Omega : 50\,\Omega \tag{4}$$

where R_L is the load impedance seen by one drain node and R_T is the impedance of the terminal.

4) Peak Drain–Source Voltages: The equivalent supply voltages applied to one device can be calculated for both a conventional and the proposed amplifier. The voltage stress on each active device can then be compared. The output power generated by each amplifier can be calculated by

$$P_{\mathrm{OUT}} = k \cdot \frac{V_{DD}^2}{R_{\mathrm{LOAD}}} \tag{5}$$

where P_{OUT} is the output power of the amplifier, V_{DD} is the supply voltage, R_{LOAD} is the load impedance of the amplifier, and k is a constant that expresses a proportional relationship. The equivalent supply voltage can be calculated using the load resistance in (3) and (4) and their relationship in (5).

If $P_{\mathrm{OUT}<H}$ is the output power generated at each drain in a conventional nMOS-based power amplifier, the equivalent supply voltage on each device is calculated by

$$V_{\mathrm{EQUI,CONV}} = \sqrt{\frac{1}{k} \cdot P_{\mathrm{OUT}<H} \cdot R_H} \tag{6}$$

where R_H is the load impedance seen by one drain node in the nMOS-based power amplifier and k is the constant in (5). If $P_{\mathrm{OUT}<L}$ is the power generated at *each* drain in the proposed power amplifier, the equivalent supply voltage on each device is calculated by

$$V_{\mathrm{EQUI,PROP}} = \sqrt{\frac{1}{k} \cdot P_{\mathrm{OUT}<L} \cdot R_L} \tag{7}$$

where R_L is the load impedance seen by one drain node in the proposed power amplifier and k is the constant in (5). According to the assumption of an equal distribution of output power at two drain nodes, the following equation holds:

$$P_{\mathrm{OUT}<H} = 2 \cdot P_{\mathrm{OUT}<L}. \tag{8}$$

As noted in Section II, the appropriate selection of shunt capacitances makes this assumption valid.

Also, from (3) and (4),

$$R_H = 2 \cdot R_L. \tag{9}$$

Therefore, $V_{\mathrm{EQUI,PROP}}$ is expressed by

$$\begin{aligned} V_{\mathrm{EQUI,PROP}} &= \sqrt{\frac{1}{k} \cdot P_{\mathrm{OUT}<L} \cdot R_L} \\ &= \sqrt{\frac{1}{k} \cdot \frac{P_{\mathrm{OUT}<H}}{2} \cdot \frac{R_H}{2}} \\ &= \frac{1}{2} \cdot V_{\mathrm{EQUI,CONV}}. \end{aligned} \tag{10}$$

The equivalent supply voltage on a single device of the proposed amplifier is half that of a conventional nMOS-based amplifier. A switching device under half of the supply voltage will show a halved peak drain–source voltage during class-E operation because the peak drain–source voltage is approximately proportional to the supply voltage, as shown in (1). Therefore, the proposed amplifier can reduce the peak drain–source voltage under the same supply voltage.

5) Drain Efficiency: For simplicity of analysis, it is also assumed that the total output power of a conventional nMOS-

based amplifier is equal to that of the proposed amplifier, as expressed by (8). It is true that both the conventional and proposed power amplifiers are supplied by the same dc power under the same supply voltage. However, the amount of conversion from dc to RF in the conventional power amplifier differs from that of the proposed amplifier due to the difference between the drain efficiency of two structures. The drain efficiency can be calculated by

$$\eta_{\text{drain}} = l \cdot \frac{R_{\text{LOAD}}}{R_{\text{ON}} + R_{\text{LOAD}}} \tag{11}$$

where η_{drain} is the drain efficiency, R_{ON} is the on-resistance of the switching device, R_{LOAD} is the load impedance of the amplifier, and l is a constant that expresses a proportional relationship. Under the same supply voltage, the output power of the proposed amplifier is slightly less than that of the conventional nMOS-based amplifier due to the smaller load impedance.

In conclusion, if the peak drain–source voltages of nMOS and pMOS are identical in the proposed power amplifier, each device acts as though the applied supply voltage is approximately halved. This analysis shows good agreement with the qualitative prediction presented in Section II.

C. Implementation of the Power-Combining Transformer

To implement the transmission line transformer shown in Fig. 4, the two ports P_{1P} and P_{2P} should be physically close so as to create a connection between the two sources of the pMOS devices that form a differential pair. A short distance between the two transistors is required for a good virtual ground. Additionally, the two nMOS devices at P_{1N} and P_{2N} should be close for the same reason. In this work, the adjacent metal traces belong to different windings. One primary winding is not located next to another primary winding, nor is a secondary winding located next to another secondary winding. This is done to decrease self-inductance and increase mutual inductance [17]. Moreover, every primary winding port is designed to be located at one side to achieve separation of the transformer and the other circuit elements in the layout. In conventional nMOS-based power amplifiers, two devices in a differential pair are connected through one primary winding, and vice versa [16], [17].

In this study, however, two devices connected through the primary winding of the transformer cannot form a differential pair because one is an nMOS device and the other is a pMOS device. To establish a push–pull structure, they should be separated from each other in the layout. Therefore, the two devices that form a differential pair are not connected through the primary winding. This feature constitutes one difference from conventional power-combining schemes in CMOS power amplifiers.

Fig. 5(a) shows the proposed power-combining transformer connected to *two differential amplifiers* of the proposed structure. Four primary windings are used because there are four drain nodes of nMOS and four drain nodes of pMOS. One secondary winding combines the output voltages from the drain nodes. The direction of the current in the primary part must be matched in order to combine the power from each drain node. The connections of the transformer and the active devices were carefully selected so as to have the same current direction in the primary windings.

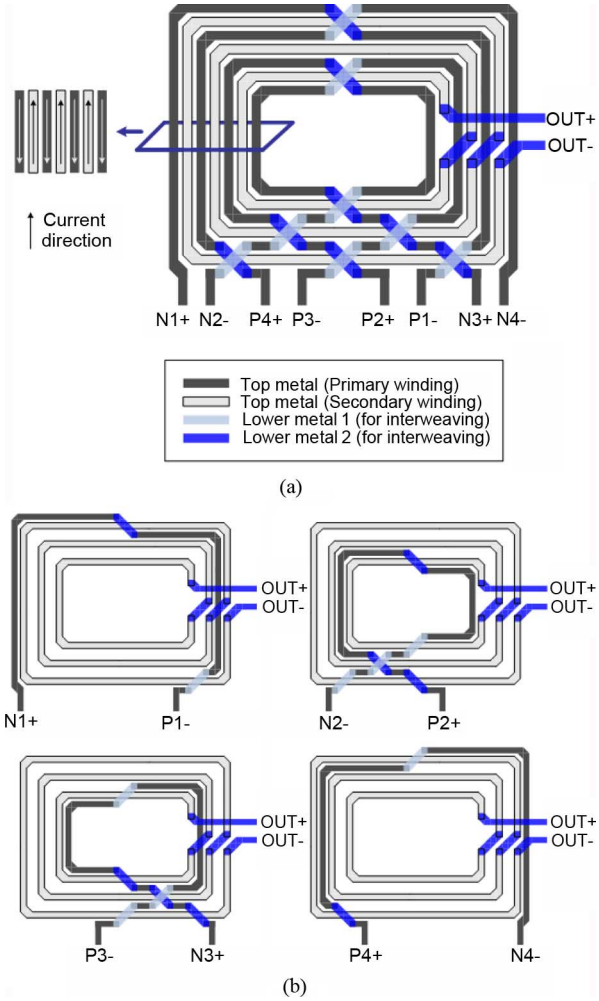

Fig. 5. (a) Diagram of the designed power-combining transformer. (b) Four primary windings that connect the drains of nMOS and pMOS. One secondary winding is also shown.

The connections between ports are defined as shown in Fig. 5(b). $N1+$ in the diagram indicates the port that is connected to the drain of nMOS, and $P1-$ indicates the port connected to the drain of pMOS. $+$ and $-$ denote the phase of the drain voltage. The drain node of nMOS is connected to the drain node of pMOS, whose gate input is out of phase with that of the nMOS device. For instance, port $N1+$ is connected to port $P1-$, and the gate inputs of nMOS at $N1+$ and that of pMOS at $P1-$ are out of phase. Therefore, pMOS at $P1-$, nMOS at $N1+$, and the primary winding comprise the basic structure, similar to that shown in Fig. 2(a). Similarly, port $N2-$ is connected to port $P2+$. $N1+$ and $N2-$ are not connected through the primary winding. Regardless of the connections with the primary winding, however, they form a differential pair and create a virtual ground. The lengths of the four primary windings are designed to be identical.

Table I shows the characteristics of various types of transformers. Only the proposed power-combining transformer can combine the voltages between the nMOS and pMOS devices in a configuration where the transformer is spatially separated

TABLE I
VARIOUS TRANSFORMERS FOR POWER-COMBINING STRUCTURES

Ref.	Structure	Two active devices connected through the primary part	Separation of transformer from active devices
[1]	DAT	*Not a differential pair*	Not achieved
[17]	PCT	a differential pair	*Achieved*
[18]	"Figure 8" Power Combiner	a differential pair	*Achieved*
This work	PCT (between nMOS and pMOS)	*Not a differential pair*	*Achieved*

TABLE II
COMPARISON OF THE SUPPLY VOLTAGE OF CASCODE POWER AMPLIFIERS THAT USE ONLY THIN-GATE–OXIDE TRANSISTORS

Ref.	Technology	Freq. [GHz]	V_{DD} [V]	P_{sat} [dBm]	Efficiency [%]
[8]	0.18-μm CMOS	2.4	2.4	23	42 (PAE)
[19]	0.13-μm CMOS	2.4	1.2	27	32 (drain effi.)

from the active devices. The connection shown in Fig. 5(b) can also be applied to conventional nMOS-based power amplifiers. The proposed transformer structure can be implemented with another chip because it is spatially separated from the active devices in the layout.

IV. DESIGN PROCEDURE

A power amplifier was designed using a 0.18-μm RF CMOS process. The proposed power amplifier is designed and optimized to have less drain–source voltage under a supply voltage. The designed power amplifier uses stacked structures of thin-gate–oxide nMOS and pMOS devices.

Table II shows the supply voltage of reported cascode power amplifiers that use only thin-gate–oxide nMOS devices. Compared with the common-source (CS) amplifier, the cascode amplifier enables higher supply voltage. In addition, according to the analysis in Section III, higher supply voltage can be applied to the proposed amplifier if a cascode structure of thin-gate–oxide pMOS devices is added. Therefore, cascode structures that use only thin-gate–oxide devices are used in both the nMOS and pMOS amplifiers in this study. The supply voltage is set to be 3.3 V, the conventional level in RF power amplifiers for handset applications. If the supply voltage is 3.3 V, the peak drain–source voltage can be estimated to be approximately 11 V, which is approximately 3.5 times the supply voltage. The voltage swing is divided at two drain nodes in the proposed amplifier. Each cascode structure experiences a voltage swing of approximately 5.5 V, an amount of voltage stress that is allowable for reliable operation, as will be explained later. The proposed configuration can be applied to any nMOS-based power amplifier, with increases of the supply voltage of the amplifier permitted. For instance, if this configuration is applied to nMOS-based cascode amplifiers that use both a 1.8- and 3.3-V device, a higher voltage will be allowed.

Fig. 6 shows the overall schematic of the designed power amplifier. An input passive balun and two stages of class-D driver amplifiers are followed by four differential pairs of transistors in the power stage. These components, together with feeding lines and interstage matching networks, are integrated within a CMOS chip. The second driver stage consists of four parallel amplifiers, each of which drives one differential pair in the power stage. Driver amplifiers also operate at a supply voltage of 3.3 V. The eight drain nodes in Fig. 6 are connected using the power-combining transformer described in Fig. 5(a). Each drain is connected to each port of the transformer, which uses the same note.

The transformer can be implemented either within a CMOS chip or with an off-chip component [20]. In this study, the power-combining transformer is implemented in an integrated passive device (IPD) process, which offers a higher quality factor than the CMOS process. The proposed transformer can also be integrated in a CMOS chip without modification of the structure. The transformer, with shunt capacitors and an output capacitor, is integrated within an IPD chip. The connections between the drain node in the CMOS chip and the port of the transformer in the IPD chip are made using bonding wires. This two-chip implementation does not require any off-chip discrete elements.

The size of the pMOS device in the CS amplifier is designed to be larger than that of the nMOS device in the CS amplifier in order to offset the mobility difference between the majority carriers of nMOS and pMOS devices. This will balance the on-resistances of nMOS and pMOS devices that operate as switching devices. The sizes of the devices in the common-gate (CG) amplifier are determined according to their on-resistance and output capacitance. Essentially, the output capacitance of the devices in the CG amplifier and additional metal–insulator–metal (MIM) capacitors (C_N, C_P) determine the division of voltage swings between the nMOS and pMOS devices. The load network is completed with these capacitances, as explained earlier.

Fig. 7 shows simulated drain voltage waveforms of the power amplifier. With the appropriate selection of the device size and the values of capacitors, symmetrical drain voltage waveforms of nMOS and pMOS can be obtained. $V_{\mathrm{DS}}(\mathrm{nMOS, CGCS})$ denotes the voltage between the drain of the CG device and the source of the CS device in the nMOS stacked structure. $V_{\mathrm{DS}}(\mathrm{pMOS, CGCS})$ denotes the voltage between the drain of the CG device and the source of the CS device in the pMOS stacked structure. The peak values of the two voltage waveforms are designed to have equal voltage stress on both the nMOS and pMOS stacks. Furthermore, by adjusting the gate bias of the CG device, it is possible to divide $V_{\mathrm{DS}}(\mathrm{pMOS, CGCS})$ equally between both the CG and CS devices. The gate bias of the CG device in the pMOS amplifier was designed to be 1.0 V. If it is set to be 0 V, most of the value of $V_{\mathrm{DS}}(\mathrm{pMOS, CGCS})$ arises across the CS device. However, by increasing the gate bias of the CG device in the pMOS stacked structure, the peak value of $V_{\mathrm{DS}}(\mathrm{pMOS, CS})$ is decreased and an equal voltage swing between the CS and CG devices is achieved. The gate

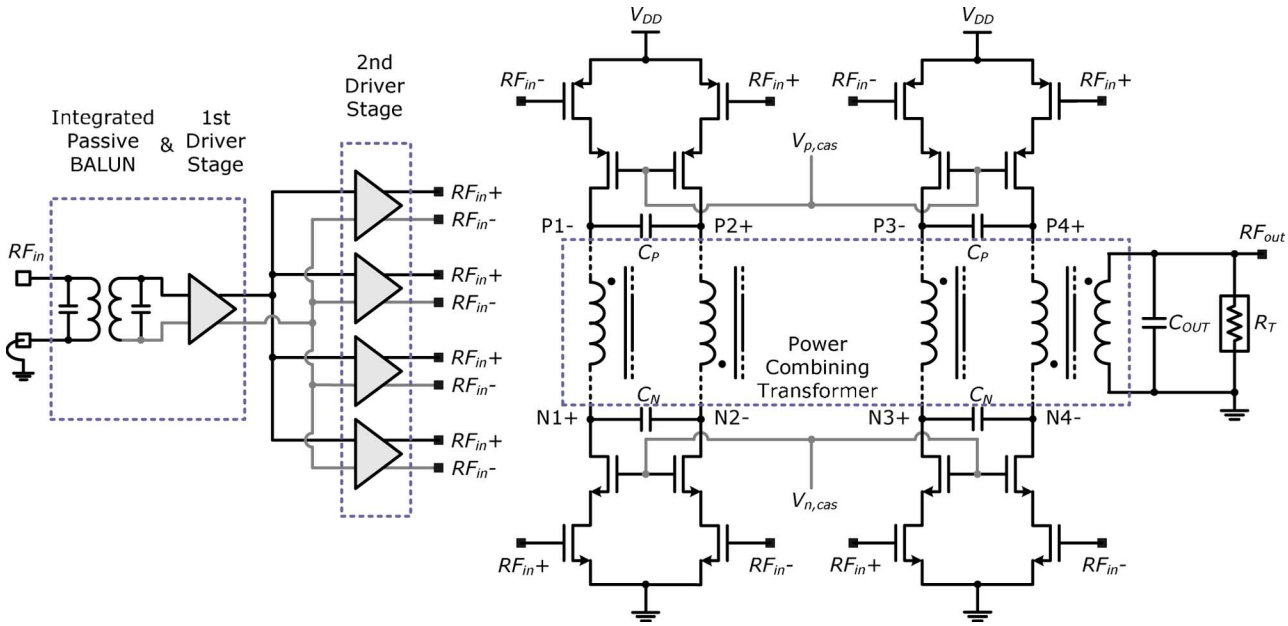

Fig. 6. Overall schematic of the power amplifier. Some bias circuits are omitted.

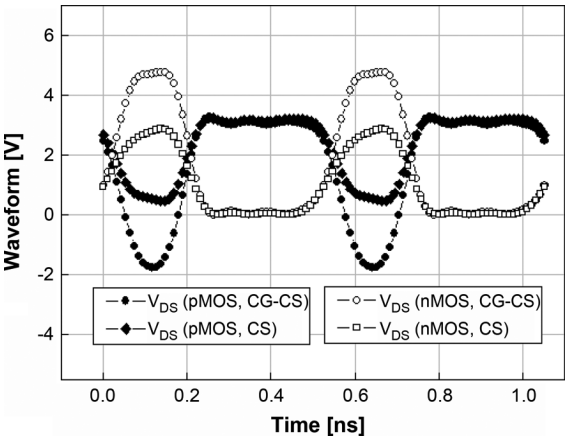

Fig. 7. Simulated drain voltage waveforms of power stage (P_{IN} of 10 dBm, $V_{\mathrm{DD}} = 3.3$ V).

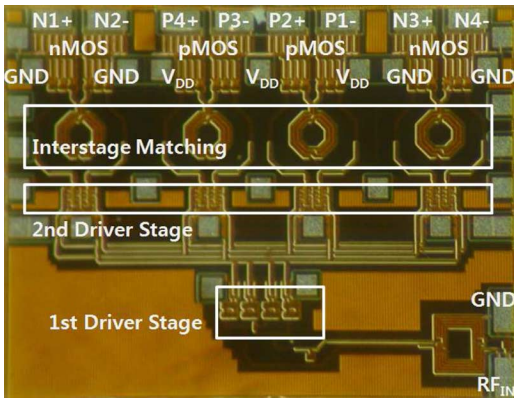

Fig. 8. Microphotograph of the CMOS power amplifier.

bias of the CG device in the nMOS stacked structure was designed to be 2.0 V for the same reason. The simulated voltage waveform confirms that equal amounts of voltage stress are applied to each thin-gate–oxide device for both the nMOS and pMOS stacked structures. It is known that a CMOS device can generally sustain only twice the nominal supply voltage [7]. As shown in Fig. 7, the drain–source voltage of each device in the proposed amplifier has a peak value between 2.5–3.0 V, which is less than twice the nominal supply voltage of 1.8 V. The proposed structure allows a higher supply voltage with reliable MOSFET operation, as opposed to the nMOS-based power amplifiers listed in Table II.

V. Measurement

The implemented chip was attached to the ground region of a PCB. The ground region acts as a heat sink, and the chip is glued using conductive adhesive so as to ensure good thermal dissipation. The ground pads and the signal pads in the CMOS chips were wire-bonded to the ground region and the gold-plated metal lines of the PCB, respectively. The input pad in the CMOS chip and the output pad in the IPD chip were wire-bonded to 50-Ω microstrip lines. Fig. 8 shows a microphotograph of the CMOS chip. The overall test sample including the IPD chip is shown in Fig. 9. As the performance is degraded with the inductance of bonding wires between the CMOS and IPD chips, multiple bonding wires were used for each connection.

All measurements were performed using one-tone continuous wave (CW) signals. The loss induced by the PCB and connectors is deembedded to calculate the efficiency of the designed power amplifier. Fig. 10 shows the measured output power and power-added efficiency (PAE) over a frequency band of 1500–1800 MHz at a supply voltage of 3.3 V. The chip is designed to cover the frequency band of 1700–1900 MHz, but a slight shift in the operating frequency occurred. The measured output power was flat over the frequency band and was found to exceed 1 W ($= 30$ dBm). The PAE was 36.81% at 1550 MHz and more than 35% in a range of 1500-1700 MHz.

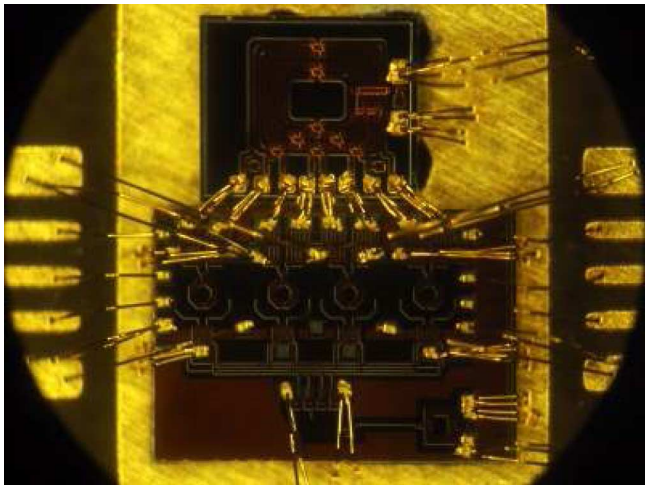

Fig. 9. Microphotograph of the CMOS power amplifier and IPD transformer after bonding-wire connections were made.

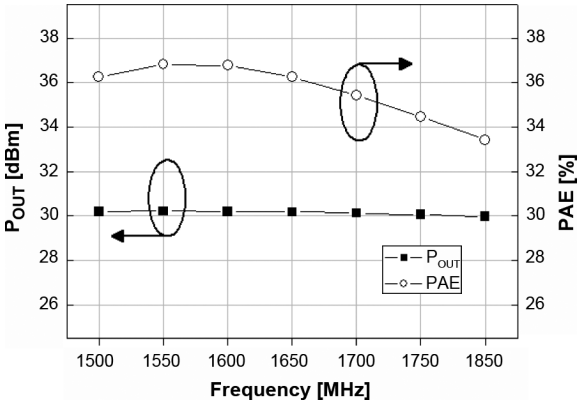

Fig. 10. Output power and PAE over a frequency band of 1500–1800 MHz ($P_{\rm IN}$ of 8.6 dBm, V_{DD} = 3.3 V).

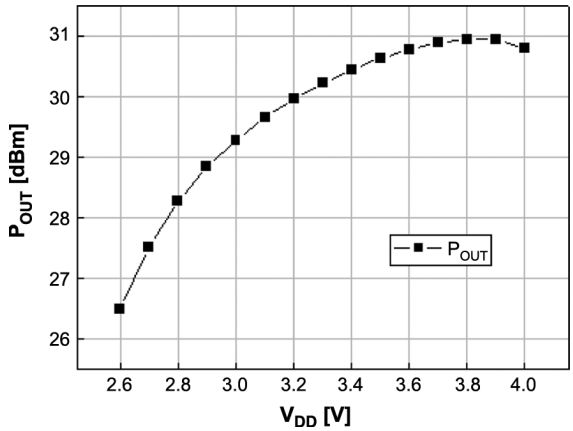

Fig. 11. $P_{\rm OUT}$ under V_{DD} variation ($P_{\rm IN}$ of 8.6 dBm, at 1600 MHz).

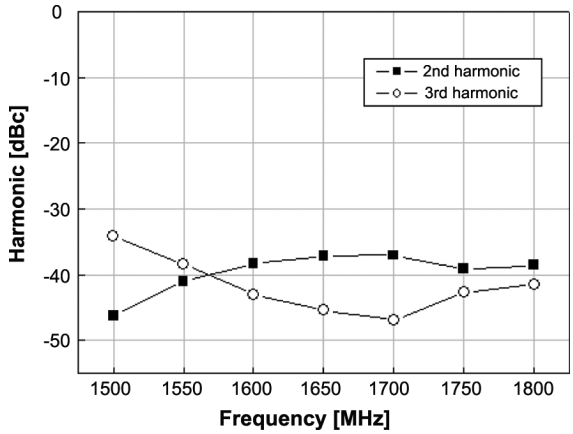

Fig. 12. Second and third harmonics over a frequency band of 1500–1800 MHz ($P_{\rm IN}$ of 8.6 dBm, V_{DD} = 3.3 V).

As shown in Fig. 7, the output voltage swing of the designed power amplifier is less than the maximum allowable swing. Therefore, the efficiency will be increased if the supply voltage is increased until the output voltage swing reaches its maximum allowable value. The load network also needs to be re-designed at the increased supply voltage.

Fig. 11 shows the measured output power with respect to the supply voltage. The other bias conditions are identical to the case of a supply voltage of 3.3 V. Given that the drain–source voltage of each active device is less than twice the nominal supply voltage of the device, as shown in Fig. 7, the supply voltage can exceed 3.3 V while maintaining reliable MOSFET operation. The measured results show that the designed power amplifier can sustain a supply voltage of up to 3.9 V. The output power at this voltage is 30.94 dBm. Compared with a conventional nMOS-based amplifier [8], this amplifier sustains a higher supply voltage using an additional pMOS stacked structure. Fig. 12 shows the measured second and third harmonics over a frequency band of 1500–1800 MHz at a supply voltage of 3.3 V. The measured second harmonics were below −37 dBc, and the measured third harmonics were below −41 dBc in a frequency band of 1600–1800 MHz. These results verify stable class-E operation of the proposed structure. The power amplifier can operate at a higher supply voltage compared to that of a conventional nMOS-based power amplifier.

VI. Conclusion

A class-E power amplifier that uses nMOS and pMOS transistors as complementary switching devices has been proposed and implemented in a 0.18-μm RF CMOS process. Additionally, a power-combining transformer has been proposed for combining voltages between nMOS and pMOS devices in which the connections are quite different from those of a conventional nMOS-based amplifier. The topology can also be applied to a conventional nMOS-based switching mode power amplifier in order to increase the supply voltage or to reduce the drain–source voltage stress.

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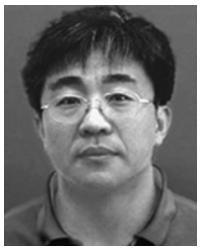
Ki Yong Son (S'06) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2005 and 2007, respectively, and is currently working toward the Ph.D. degree at KAIST.

His research interests include CMOS power amplifier design for mobile applications, RF power amplifier linearization, and digital/RF predistortion system.

Changkun Park (S'03–M'08) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2001, 2003, and 2007, respectively.

He was with the Advanced Design Team, Dynamic Random Access Memory (DRAM) Development Division, Hynix Semiconductor Inc., where he was involved with development of high-speed I/O interfaces of DRAMs. In 2009, he joined the School of Electronic Engineering, Soongsil University, Seoul, Korea, as a faculty member. His research interests are microwave integrated circuits and systems including power amplifiers for mobile communications.



Songcheol Hong (S'87–M'88) received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 1989.

In May 1989, he joined the faculty of the School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. In 1997, he held short visiting professorships with Stanford University, Palo Alto, CA, and Samsung Microwave Semiconductor. His research interests are microwave integrated circuits and systems including power amplifiers for mobile communications, miniaturized radar, and millimeter-wave frequency synthesizers, as well as novel semiconductor devices.