A 1.8-GHz 2-Watt Fully Integrated CMOS Push-Pull Parallel-Combined Power Amplifier Design

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***Abstract* — This paper newly presents a push-pull parallel-combined CMOS power amplifier (PA) and its analysis of operation. The proposed class-E CMOS PA incorporates the push-pull parallel-combined power devices with the 1:1:2 (two single-turn primary windings and a two-turn secondary winding) step-up on-chip transformer. The PA is fully integrated in a standard 0.18-μm CMOS technology without any external balun or matching networks. The operation of the PA with a multi-turn on-chip transformer is substantially analyzed in order to optimize the device size and its structure. Experimental data demonstrates the output power of 2-Watt and the power-added efficiency (PAE) of more than 30 % with a 3.3-V of power supply at 1.8 GHz. This is the new demonstration of the compact fully integrated CMOS PA with 2-Watt of output power with very stable operation at 1.8GHz range.**

***Index Terms* — CMOS PA, class-E, transformer, impedance transformation, parallel-combining, power amplifier.**

I. Introduction

The rapidly increasing interests in CMOS RF transceivers for various wireless communication applications have stimulated research on the design of a CMOS-based PA [1]. A CMOS PA provides the advantages of a higher level of integration, better thermal characteristics, and low cost advantages over a GaAs-based PA. Since a PA consumes a majority of DC power in the front-end side, a highly efficient PA with high output power is necessary for the longer battery life in wireless applications.

However, because of low breakdown voltage and lossy substrate of CMOS compared to III-V devices, the design of efficient high output power CMOS PA remains a challenging task. In prior art of the CMOS PA, the distributed active transformer (DAT)-based PA is the only one that is fully integrated for output power of greater than 1 Watt [2]. However, the DAT requires a relatively large die area, moreover, its circular structure may generate an instability issue due to the coupling of the input signal feeding line with the transformer [3].

In this paper, we propose a new push-pull parallel-combined class-E CMOS PA with a compact 1:1:2 step-up transformer to achieve high efficiency and high output power up to 2 Watts. In this structure, the coupling issue is minimized because of its local separation between the transformer and other components of the PA. To optimize device size for high-output power and efficiency, the parallel-combined class-E PA structure is incorporated with a step-up on-chip transformer. In addition, essential analysis of an ideal class-E PA with a 1:*N* transformer is presented.

II. Parallel-combined class-E Power Amplifier with a 1:N Transformer

For GSM-based wireless communication, a switching-mode PA is attractive due to its high DC-to-RF efficiency. Among the various classes of switching-mode PAs, a class-E PA is considered to be the most suitable solution because of its circuit simplicity and relatively high tolerance to circuit variation [4]. L-C-R lumped branch is necessary for the class-E switching conditions. Typically, the load resistance value of the switching network is quite small, so that additional lumped elements are required to transform this low impedance to a 50-ohm load.

Fig. 1(a) shows a schematic of the class-E CMOS PA with the 1:*N* transformer. In addition to the major role of impedance transforming, the transformer itself is a part of the L-C-R branch for the ideal class-E operation. Fig. 1(b) shows the equivalent circuit model of the class-E PA. The equivalent impedance of the transformer is used for the constitution of

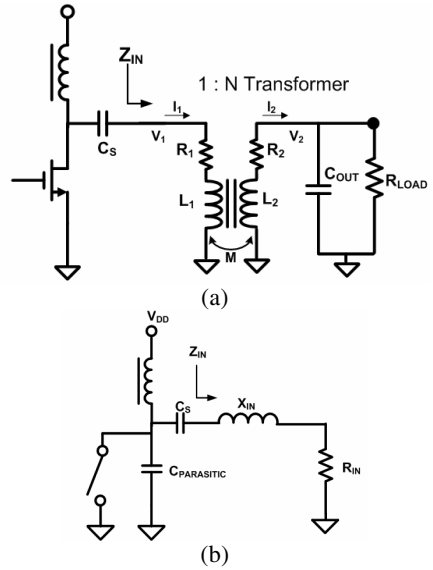

Fig. 1. (a) Schematic of the class-E PA with a 1:*N* transformer (b) Equivalent circuit model.

the L-C-R lumped branch required for the class-E operation. Hence, in the analysis of the class-E operation with the 1:*N* transformer, the number of necessary lumped elements can be

reduced while the class-E switching conditions are still satisfied. The magnetic-coupled transformer shown in Fig. 1(a) can be modeled with the equivalent series resistors, R_1 and R_2, and the equivalent net inductance, L_1 and L_2, from the primary and secondary winding. By taking into account the effect of the induced voltage through mutual coupling and neglecting the equivalent series resistance, one can write

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} j\omega L_1 & -j\omega M \\ j\omega M & -j\omega L_2 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (1)$$

$$V_1 = Z_{IN} I_1 = (R_{IN} + jX_{IN}) I_1 \quad (2)$$

$$V_2 = Z_{OUT} I_2 = 1/Y_{OUT} \cdot I_2 = I_2 / (G_{LOAD} + j\omega C_{OUT}) \quad (3)$$

where M is the mutual inductance between the primary and secondary winding. Z_{IN} is the input impedance and R_{LOAD} is the output resistance, which is typically 50 ohm. The output capacitor, C_{OUT}, locates in parallels to the load. From (2) and (3), the input impedance of the transformer is given by

$$Z_{IN} = \frac{V_1}{I_1} = R_{IN} + jX_{IN} = j\omega L_1 + \frac{\omega^2 M^2}{Z_{OUT}(1 + \frac{j\omega L_2}{Z_{OUT}})} \quad (4)$$

To minimize passive losses in the above equations, C_{OUT} tunes out $j\omega L_2$ at the designed frequency.

$$Z_{IN\,opt} = j\omega L_1 (1 - k^2) + \frac{k^2}{N^2} \cdot R_{LOAD} \quad (5)$$

Following the calculation methods in [5], the optimized values of the equivalent circuit for the class-E PA are calculated as follows:

$$R_{IN\,opt} = 0.577 \frac{{V_{DD}}^2}{P_{OUT}} = \frac{k^2}{N^2} \cdot R_{LOAD} \quad (6)$$

$$X_{IN\,opt} = QR = \omega L_1 (1 - k^2) \quad (7)$$

$$C_{PARASITIC} = 0.183 \frac{1}{\omega R} \quad (8)$$

$$Cs \approx C_{PARASITIC} (\frac{5.477}{Q})(1 + \frac{1.42}{Q - 2.08}) \quad (9)$$

where $R_{IN\,opt}$ is the optimum load resistance of the switching network for the required output power at a given supply voltage, and Q is the quality factor of the output network of the class-E PA. In this structure, in order to satisfy the above equations as well as the required impedance transforming, only the series capacitor, C_S, is necessary for the equivalent L-C-R branch of the class-E PA because the parasitic capacitance of the transistor output, $C_{PARASITIC}$, can be incorporated into the circuit with the required parallel capacitance. Therefore, this structure can reduce the size and number of the elements, resulting in a more simplified circuit.

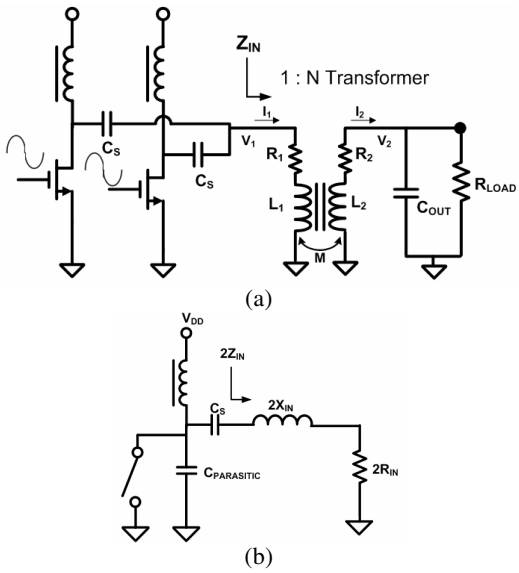

Fig. 2. (a) Schematic of the parallel-combined class-E PA with a 1:N transformer (b) Equivalent circuit model at each transistor.

According to (6), the optimum load resistance, $R_{IN\,opt}$, is determined by the desired output power and supply voltage to the device. To achieve a higher output power, a smaller load resistance of the switching network is required. The turn ratio of the transformer, N, enables the necessary impedance transformation from the optimum low impedance of the transformer input to the 50-ohm load. As the turn ratio increases, it can generate higher output power with large enough transistor device to handle the sufficient DC current. Since the switching efficiency of class-E PA is inversely proportional to the on-resistance, r_{on}, of the switch device, the transistor size should be also large enough to significantly reduce r_{on}. However, increasing the device size also increases the input gate capacitance that is driven by the driver amplifier stage. Although the gate capacitance can be tuned with an inductor, large input capacitance can degrade the power-efficiency performance [6], [7]. Furthermore, the large capacitance between the gate and drain, C_{gd}, may cause instability due to the presence of a feedback path [8]. Therefore, the size of a transistor should be carefully chosen for high-power and high-efficiency operation with stability.

Fig. 2 illustrates the proposed parallel-combined class-E PA with device size optimization for a given output power. In Fig. 2(a), the 1:N transformer is incorporated to transfer the output power of each transistor to the output load. By having two devices instead of one large device, currents from each transistor are summed in the same phase at the transformer input. As a result, the equivalent impedance is doubled at each of the transistors, as shown in Fig. 2(b). Therefore, it is possible to use half size of a power device optimized for high efficiency with stable operation. The $C_{PARASITIC}$ of a device output can be used as the parallel capacitor required in the class-E operation, which results in no need for additional parallel capacitors.

III. Design and Implementation

The PA, shown in Fig. 3, is composed of two-stage drive amplifiers and a power stage amplifier with a 1:1:2 step-up transformer.

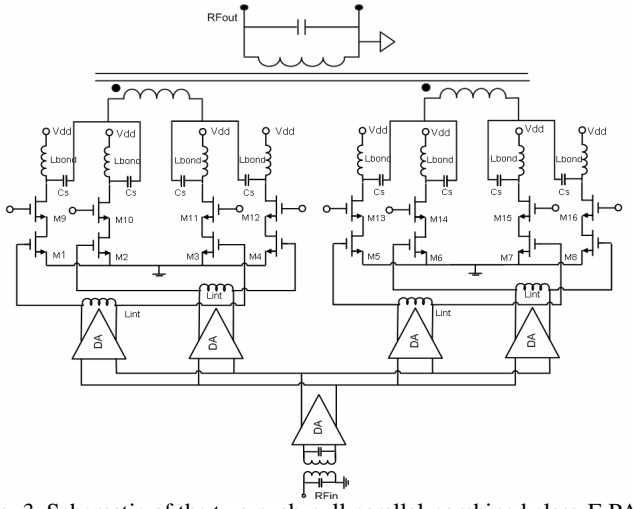

Fig. 3. Schematic of the two push-pull parallel-combined class-E PA with a 1:1:2 step-up transformer.

As mentioned in section II, the turn ratio of the transformer enables a necessary impedance transformation from the optimum low impedance of the transformer input to the load impedance. To obtain the target output power of 33 dBm, the turn ratio of the transformer needs to be increased until the small impedance of the transformer input transforms to the output 50-ohm load. Because of the increment of the turn ratio, the size of the overall transformer is increased. Also, the number of inter-weaved sections increases as well. This leads to the degradation of the passive performance of the transformer because of increased crossover points in the lateral structure. However, the push-pull power-combining configuration has its own 1:2 impedance transformation without increasing the turn ratio. Therefore, it lessens the burden of a large turn-ratio that is required for the impedance transformation. The parallel-combined class-E power amplifier uses the 1:1:2 step-up transformer for impedance transformation. As shown in Fig. 3, the transformer consists of double-lateral primary windings and one two-turn secondary winding. The induced currents from each primary winding are summed at the secondary winding in the same phase with same direction. Two individual push-pull class-E PAs are combined with each of the double primary windings.

To optimize the performance of the transformer, both 2-D Agilent ADS Momentum and 3-D Ansoft HFSS were used for an iterative optimum process. To consider layout effects of interconnection between the series capacitors, C_S, and the transformer, an EM simulation was performed including capacitors and interconnections. The metal widths of the primary windings and the secondary winding as well as the metal spacing were fully optimized. The physical metal thickness is 2.34 μm. The compact on-chip transformer size is 0.85 mm × 0.7 mm, as shown in Fig. 4.

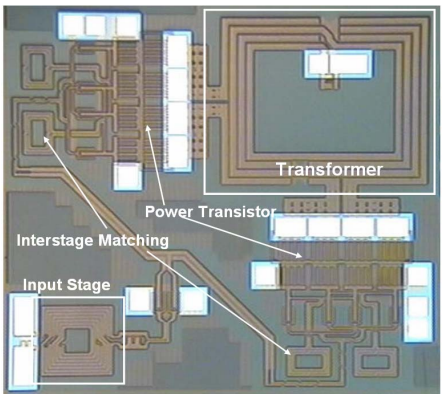

Fig. 4. Microphotographs of the PA (Chip size: 1.8 mm × 1.65 mm).

The input on-chip balun was designed to support differential operation of the driver amplifier and power amplifier. For the two-stage drive amplifier, a square-wave generating amplifier topology was used. For the power stage, a cascode topology was used to reduce the voltage stress of each power device [9]. The maximum AC voltage drop across the devices at any node should be below twice the nominal supply voltage in order to guarantee safe operation of the devices and circuits [7]. The devices in the common-source stage, M1-M8, and cascode stage, M9-M16, have gate lengths of 0.18-μm and 0.35-μm, respectively. Since the size of the transistors is determined to be large enough such that r_{on} is properly reduced, V_{DS} is less than 0.3 V when the transistor is in on-state. Since the parasitic capacitors of the transistor output are incorporated into the circuit, no additional parallel capacitor is needed for class-E operation. A parallel inductor located in the interstage between the driver and the power stage was used to tune out input capacitance of the power transistor. To minimize DC loss, the high-Q wire-bonding inductor is used for the DC feeding line. Finite DC-feed inductance was used to increase the output power capability of the class-E PA [9]. A 3.3-V supply voltage was fed into the drain of the PA through the finite wire-bonding inductor. The total simulation of the PA with the transformer was performed using ADS.

IV. Measurement Results

The proposed fully integrated PA was fabricated in a commercial 0.18-μm CMOS technology. Fig. 4 shows microphotograph of the fabricated CMOS PA. The chip size is 1.8 mm × 1.65 mm including the pads for the chip-on-board testing. The die was mounted on the ground heat sink of the printed circuit board (PCB) using electrically and thermally conductive adhesive. The input and output pads were wire-bonded to 50 ohm microstrip lines on PCB. The connector and PCB loss was calibrated out in the measurement procedure. Fig. 5 shows the measured output power (P_{OUT}) and PAE along with the input frequency. Measured P_{OUT} was 33 dBm (2 W) and PAE was 31 % with a single-ended 50-ohm input and output condition at 1.8 GHz. The performance of the

measured P_{OUT} and PAE was fairly constant over a frequency range of 300 MHz. Fig. 6 shows the measured P_{OUT} and PAE versus the input power in a 1.8 GHz operation. A compressed power gain was around 19.5 dB at the peak power. To verify its potential wireless communication application, the fabricated PA was tested with a Gaussian minimum shift keying (GMSK) modulated input signal. The product of the Gaussian filter bandwidth and the symbol duration (BT) was chosen to be 0.3. Fig. 7 shows the measured spectrum with the GSM mask in dBc with 33dBm of an output power. The output spectrum was well below the GSM spectral emission mask over the whole output power range. Also, there was no unstable tendency in the measurement due to the PA configuration of the separation between the transformer and input signal feeding-line.

V. Conclusion

The new push-pull parallel-combined class-E CMOS PA with a multi-secondary-turn transformer has been proposed in this paper. By carefully analyzing the push-pull parallel-combined device operation, the device size was optimized for high power and high efficiency with very stable operation. The size of the transformer was significantly reduced by incorporating the multi-turn on-chip structure. Since the transformer was substantially isolated from the input feeding line, there was no unstable tendency in any condition. Experimental data demonstrates the output power of 33 dBm, PAE of more than 30 % with a 3.3-V power supply at 1.8 GHz operation. This is the new approach for compact high power CMOS PA design that maintains very stable operation.

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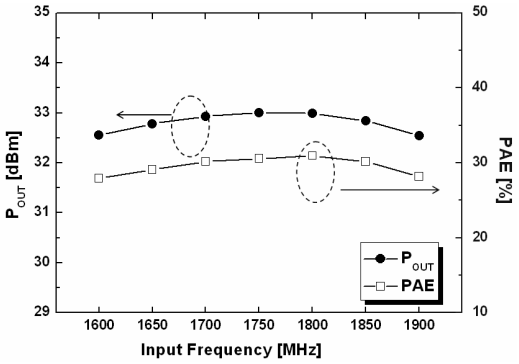

Fig. 5. Measured P_{OUT} and PAE versus frequency.

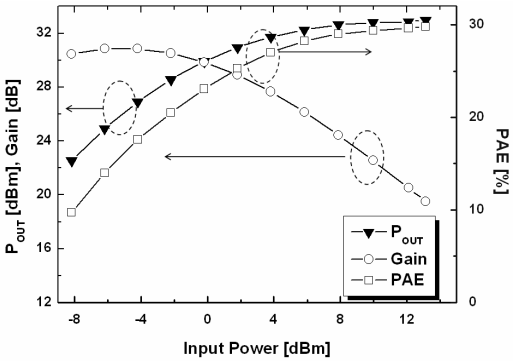

Fig. 6. Measured P_{OUT}, Gain and PAE versus input power at 1.8 GHz.

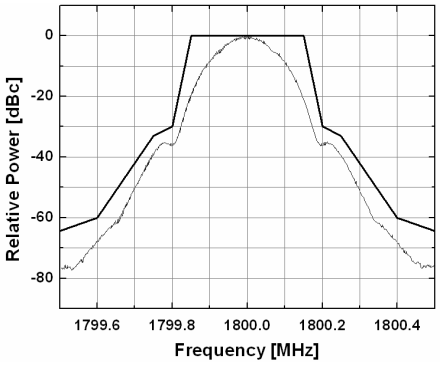

Fig. 7. Amplified GMSK modulated signal and the GSM spectrum emission mask.

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