Dynamic FET Stack Control for Enhanced Efficiency in Envelope Tracking Power Amplifiers

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Abstract — In this work, a dynamic FET stacking is proposed to implement an envelope tracking power amplifier (ET PA) to enhance the efficiency at low V_{DD} and backed-off power range. Quadruple-stacked CMOS power cell is reconfigured to operate as quasi-triple or quasi-double stacks according to the magnitude of the input envelope. The overall ET PA with the proposed RF power amplifier and envelope amplifier fabricated using 0.18-μm SOI CMOS shows an overall efficiency of 46% for 10 MHz LTE and 52% for WCDMA signal, which are 4.5% and 2.8% higher than the static stack ET PA. Adequate linearity has also been demonstrated using the gain and phase step compensation circuitry.

Index Terms — CMOS, dynamic stacking, envelope tracking (ET), power amplifier (PA).

I. Introduction

Modern multi-mode mobile phones require 4G-LTE coverage on top of the existing 3G-WCDMA. This presents special challenge to the design of high-efficiency power amplifiers (PA's) due to need to handle a wide range of peak-to-average-power ratio (PAPR) of the transmit signals. For example, a WCDMA voice signal has only 3.4 dB PAPR while a 10 MHz fully-loaded QPSK LTE signal has a PAPR as high as 6.7 dB. An RF PA with a fixed bias or average power tracking suffers from steep efficiency degradation at the backed-off power levels. Dynamic bias using envelope tracking (ET) has recently been employed to overcome this limit [1]-[5]. Many works have been focused on enhancing the efficiency of envelope amplifier (EA) through a dual-switcher [1], [2], a buck-boost converter [3] and so on. However, little attention was given to optimize the PA core to improve the efficiency for high PAPR signals such as LTE signals.

To overcome the low breakdown voltage problem of CMOS, multiple-FET stacking is often used for an RF PA. However, when the stacked FET cell is exposed to the low-voltage dynamic bias during ET operation, the drain-source voltage across each transistor falls below the knee-voltage, causing detrimental efficiency degradations. This problem is more pronounced for Si CMOS due to its "soft" knee characteristics. Also, the nonlinear drain-source capacitance tends to increase sharply as the transistor enters the triode region. This makes the optimum load impedance seen at drain node of each stacked-FET shifts to the undesirable region, resulting in severe efficiency degradation [6].

In this work, a dynamic FET-stacking design is proposed to realize an ET PA core showing near ideal efficiency characteristics, where the efficiency peak is maintained at optimum points across a wide V_{DD} range. This does not only improve the overall efficiencies for high PAPR signals such as LTE, but also allows low battery voltage operation.

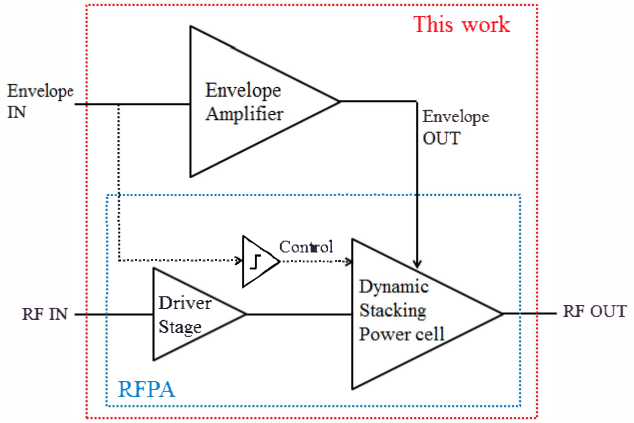

Fig. 1. Block diagram of the 2-stage ET PA system with dynamically controlled stacked power cell.

II. Dynamic Stack Control

The block diagram of an ET PA realized with 0.18-μm SOI CMOS is shown in Fig. 1. It consists of an EA and a 2-stage RF PA core with dynamic stack control, where the number of stacks in the power cell is controlled according to the magnitude of the input envelope signal.

Fig. 2 shows the detailed circuit schematic of the proposed RF PA core. The power cell is based on a quadruple-stacked FET PA. For dynamic stack control, two comparators are employed for generating on-off signals to 3rd and 4th common-gate (CG) FET's to dynamically control the number of active stacks in the power cell according to the input envelope.

When the magnitude of the input envelope (ENV_{in}) is in the highest state, namely, $ENV_{in} > ref_4 > ref_3$, the comparator A_4 turns on S_{41} and turns off S_{43} while the comparator A_3 turns on S_{42} and S_{31}, and turns off S_{33}, resulting in a quadruple-stacked mode. As ENV_{in} is decreased such that $ref_4 > ENV_{in} > ref_3$, A_4 turns off S_{41} and turns on S_{43} while A_3 maintains its previous state. Since the total capacitance at the gate of 4th-stack FET (M_4) is reduced from $C_{41}+C_{42}$ to C_{42}, the magnitude of the RF voltage swing at this node is increased, resulting in an additional DC offset. Therefore, the gate bias of M_4 is now much larger than V_{drain}, which effectively shorts out M_4 and

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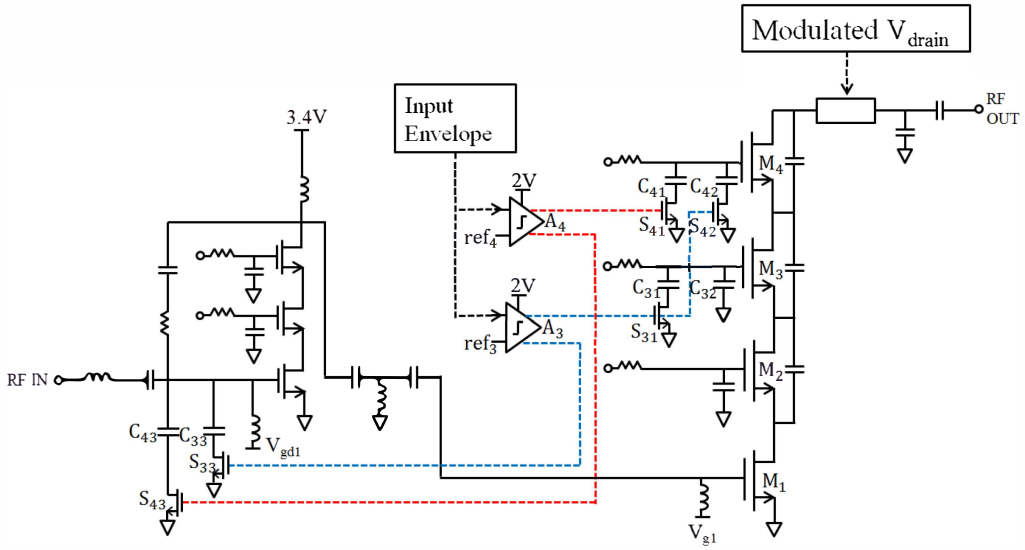


Fig. 2. Detailed schematic of the proposed 2-stage RF PA with dynamic stacking control circuits.

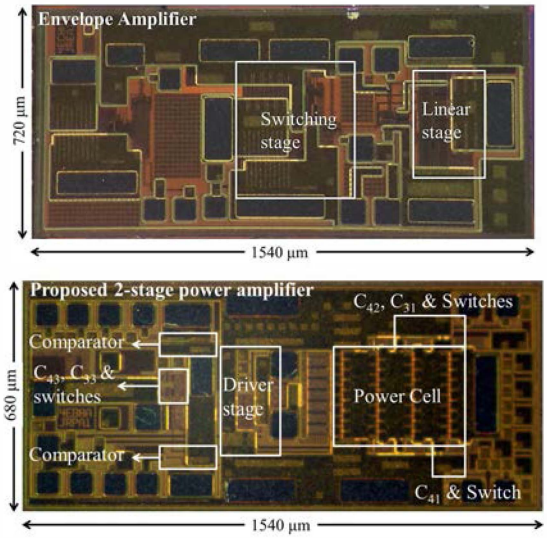
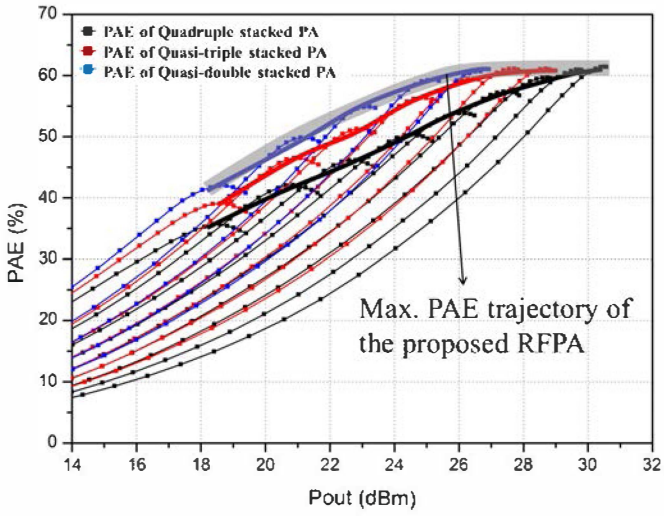


Fig. 3. Fabricated chip photographs of the EA and proposed RF PA.

reconfigures the main cell to a quasi-triple stack with hanging capacitors, a series combination of the $C_{M4,gs}$ (parasitic gate-source capacitor of M_4) and C_{42}. Finally, when ENV_{in} reduces below ref_3, the dynamic stack enters the lowest state. In this state, M_3 is also shorted out by the similar operation of A_3, resulting in a quasi-double stack. By reducing the number of active stacks according to ENV_{in} at low envelope levels, one can avoid operation into the knee region and subsequent efficiency degradation.

When transistors are switched in and out dynamically, there can be distortions due to the gain and phase discontinuities. Because step discontinuities in gain and phase cannot be compensated by digital pre-distortion, these distortions should be compensated for in the analog domain. To avoid step gain discontinuity during ET operation, the gain and output power at the switching point should be the same regardless of the number of active stacks. Because the output power of stacked



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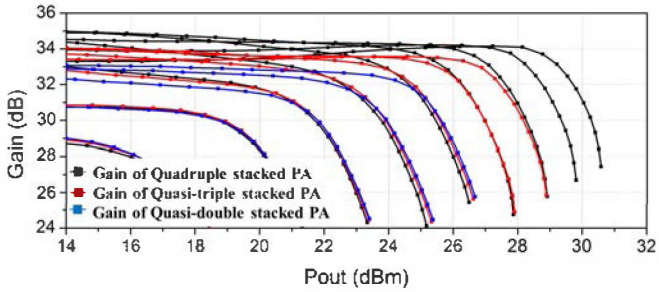

(b)

Fig. 4. Measured 837 MHz CW performance of the proposed RF PA, by sweeping power stage drain bias from 1 V to 3.4 V. (a) PAE, (b) gain.

PA is determined by the load impedance seen at each drain node of stacked FET, continuous ET gain trajectory can be achieved in the stacked FET by selecting appropriate switching capacitance ratio (C_{41}:C_{42} and C_{31}:C_{32}) at the gate of the upper FETs. Also, step phase discontinuity can be compensated by simultaneously switched input matching

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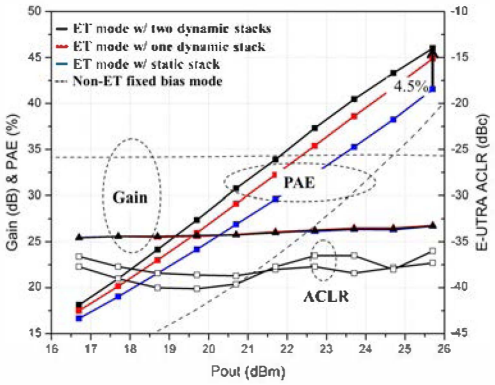

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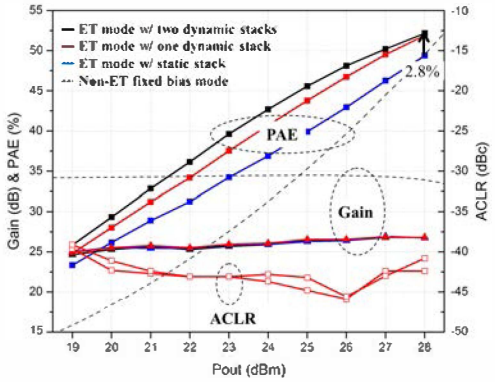
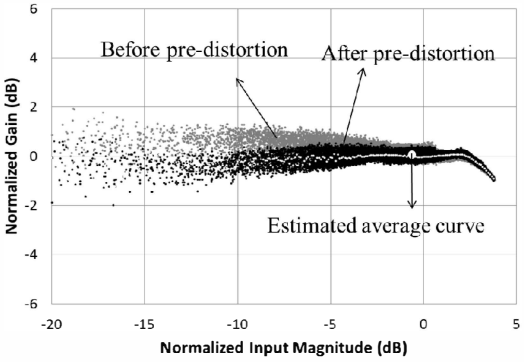
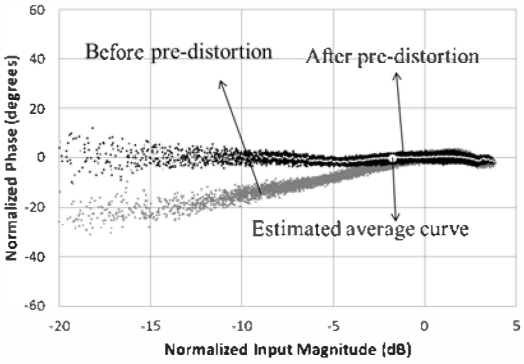


(b)

Fig. 5. Measured performance of the ET PA system with (a) 10MHz LTE, and (b) WCDMA signal.



(a)



(b)

Fig. 6. Measured dynamic characteristics of the ET PA system with WCDMA at 28 dBm output power. (a) dynamic AM-AM, (b) dynamic AM-PM. Input magnitudes are normalized to the 0 dB.

capacitors (C_{43} and C_{33}). The ratio of switching capacitances and magnitude of input matching capacitances are carefully chosen by the envelope simulation to achieve sufficient continuity in gain and phase.

III. Measurement Results

Both EA and RF PA are fabricated in 0.18-μm SOI CMOS process. Fig. 3 is die photographs of an EA and a proposed RF PA.

Fig. 4 is the measured 837 MHz CW performance of proposed 2-stage RF PA as the power stage drain bias is swept from 1 V to 3.4 V with 0.3 V step. The maximum PAE reaches 61% at 30.5 dBm with a 3.4V drain bias. By shorting upper transistors, the peak PAE remains over 60% even down to 5 dB back-off region (~25 dBm), which is 7% improvement over static quadruple stack. Total current consumption in the two comparators is only 1 mA with 2 V supply.

EA was characterized all by itself to estimate the efficiency in the EA. The efficiency peaks around 96.5% at 3.3 V (maximum voltage rail of the EA) and reduces to 45% at 1 V. The average efficiency for LTE signals (PAPR = 6.7 dB) is measured to be 77%, which is 6% lower than the state-of-the-art EA results (83%) [1], and the measured average efficiency for WCDMA signals (PAPR = 3.4 dB) is 88%.

Fig. 5 shows the measured performance of the overall ET PA system using 10 MHz BW, 6.7 dB PAPR, QPSK, LTE signal and 3.84 MHz BW, 3.4 dB PAPR, WCDMA signal with 837 MHz carrier frequency respectively. The PA meets the output power requirement of typical handset PA's with a WCDMA power of 28 dBm and battery voltage requirement of 3.4 V. To investigate the effect of dynamic stacking for each signal, four different cases are compared: ET mode with two dynamic stacks (M_3 and M_4), ET mode with only one dynamic stack (M_4), ET mode with static stack and non-ET fixed bias mode. In WCDMA test, two-stack dynamic control allows efficiency enhancement of 2.8% over the static-stack ET PA at 28 dBm, showing 52% PAE with 26.8 dB gain. The efficiency enhancement reaches up to 6% when the output power is backed off to middle power range (~24 dBm). As expected, larger improvement in the efficiency is observed for LTE tests. Two-stack dynamic control provides the efficiency boost of 4.5% at the max power of 25.7 dBm, resulting in an overall PAE of 46% with 26.7 dB gain.

In order to investigate the linearity impact of the dynamic stack control, LTE E-UTRA ACLR from two-stack dynamic control PA and WCDMA ACLR1 of one-stack dynamic control ET PA are plotted after applying a simple memoryless digital pre-distortion (DPD). The measured ACLR meets the system requirement with 6 dB margin in both LTE (–36 dBc) and WCDMA (–40.8 dBc) cases. The measured EVM after DPD is 3.7% and 2.2% for LTE and WCDMA respectively,

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TABLE I
PERFORMANCE COMPARISON OF ET PA SYSTEMS

Ref.	Freq (GHz)	BW (MHz)	PAPR (dB)	PA Technology	PAE (%)	Pout (dBm)	ACLR (dBc)	V_{DD} (V)
[1]	2.535	20	6.7	GaAs HBT	48	28.3	−41.4	5.5
[2]	0.782	10	6.6	0.35-μm SOS CMOS	50.1	29.3	−46.5	-
[3]	1.74	10	6.44	GaAs HBT	39.8	27	−35.7	3.4
[4]	1.85	10	7.5	0.18-μm CMOS	34.1	26	−34.2	5
[5]	0.7	10	7.5	0.35-μm SiGe BiCMOS	41.1	28.1	-	5
This work	0.837	WCDMA		0.18-μm SOI CMOS	52	28	−40.8	3.4
This work	0.837	10	6.7	0.18-μm SOI CMOS	46	25.7	−36	3.4

much lower than the system spec limits.

To further investigate the gain and phase discontinuity compensation, the measured dynamic characteristics of the one-stack dynamic control PA for WCDMA at 28 dBm are plotted with and without DPD in Fig. 6. The estimated average curves are overlapped with white dots on linearized gain and phase scatters to evaluate the step discontinuities. However, no step gain, and phase discontinuities are found, validating the step compensation circuitry. Table I compares the performance of LTE ET PA of this work with the published state-of-the art results using different technologies. Even with the compromised efficiency from the EA, this work is among the highest PAE results for 3.4 V battery operations.

IV. CONCLUSION

In this work, we have developed a dynamically controlled stacked RF PA core for ET operation in 0.18-μm SOI CMOS process. Dynamic stack control boosts up the efficiencies at the reduced V_{DD} and backed-off power range, and thus allows low voltage operation and provides higher efficiencies for high PAPR signals such as LTE. Compared with static stack ET PA, dynamically stacked PA offers 4.5%, and 2.8% efficiency enhancement for LTE and WCDMA, respectively. Potential degradation in the linearity due to gain and phase step discontinuity has also been avoided through compensation circuitry, showing ACLR' s 6 dB better than the system specs.

ACKNOWLEDGEMENT

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