1W 900MHz Direct Conversion CMOS Transmitter for Paging Applications

Danilo Gerna[1], Alexandre Giry[1], Danilo Manstretta[2], Didier Belot[1] and Denis Pache[1]
[1]STMicroelectronics, Central R&D, Crolles, France
[2]University of Pavia, Pavia, Italy

Abstract - This paper presents a 900MHz transmitter for FSK applications. A Power Amplifier, an Upconverter Mixer and a phase shifter have been integrated together on the same substrate in 0.35μm RF 3Volts CMOS technology. The power amplifier has been designed to transmit more than 30dBm@900MHz with an associated efficiency of more than 50% at the maximum power.

I. INTRODUCTION

RF integrated circuits has had, in the last few years, one of the greatest improvements in IC marketing. The use of CMOS technology has also become more and more important for RF applications and its feasibility for receivers has been already demonstrated[1].

CMOS becomes important from a commercial point of view when different blocks are integrated on the same substrate; insulations issues, together with the need to avoid using external components like high Q inductors or SAW filters, introduce new constraints in the design.

The trend is to use as much as possible a fully differential approach to design RF parts[2]; the intrinsic higher CMRR increases the decoupling from substrate noise as well as the supply rejection. This paper presents how a RF transmitter for 2 way Reflex 25 pager application at 900MHz has been integrated in one chip on a CMOS high resistivity substrate technology. The architecture will be briefly presented and the design of the PA and the up-converter mixer will be presented in detail.

II. ARCHITECTURE

The design of a fully integrated transmitter presents several challenges starting from the architecture choice and finishing with the design of each single device. Reflex25 specifications requires 30dBm output power at 900MHz[3]; the modulation used is a 4FSK, the fact that a constant envelope modulation is used is a key factor in this design. The choice of integrating everything on the same silicon together with the need to avoid using external components reduces the degrees of freedom. The direct conversion is one of the topologies which could better match all these requirements; its simplicity makes it also very attractive for high level of integration[4]. Fig. 1 shows a simplified scheme of the transmitter where the blocks integrated together are pointed out.

The fact that different components are integrated on the same substrate makes the isolation among them an important issue. In particular the presence of a 30dBm Power Amplifier injects a large amount of noise in the substrate; its isolation from other analog circuits becomes quite critical whenever there is, in the same chip, another device which works at the same frequency but has to deal with much smaller signal level. This work approach consists in using balanced topologies design; its great advantage is that the PA perturbs the substrate mainly at twice its signal frequency[2]; the noise injected at the operating frequency is a 2nd order effect. Simulations have shown 20dB better isolation using a differential structure rather than a single ended one.

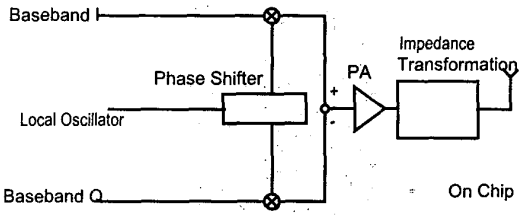

Fig. 1 Direct Conversion Transmitter

Particular attention must be paid also to the impedance matching between two RF components: in the classical microwave approach two blocks are matched at the same impedance of the strip line (50Ω) to obtain a maximum power transfer. On IC that is not necessary because the line length is usually much smaller than a wavelength but the conjugated impedance matching can guarantee the maximum power transfer. The main problem on IC is that the natural real conductance of a generic device is often very low, in the order of $1/1000\Omega^{-1}$ for balanced topologies. Achieving impedance matching on silicon would need high Q high value reactive components, a typical useful value for this purpose is 1000Ω which means 160nH at 900MHz. These passives are not feasible on IC, especially if a high Q is needed.

In this work the power amplifier and the upconverter mixer have been designed in such a way that the real conductance of the PA input is equal to the mixer output one. The impedance matching is achieved by tuning, in one of the two ports, the reactive conductance until the conjugate matching is achieved.

III. UPCONVERTER MIXER

The up-converter mixer presents several difficulties since its design cannot be separated from the PA one: the main reason for that is the time and voltage dependency of PA input impedance.

The basic approach was to estimate approximately the load in order to start designing, and to optimize the design by simulating the mixer together with the PA. The upconverter mixer must be able to provide an output power of 0dBm in order to drive the PA at the right power[3]. These specifications left us only with the active mixer choice; the Gilbert cell[5] (see Fig. 2), which can fairly match the fully differential approach and the linearity requirement.

Fig. 2 shows the Gilbert Cell Basic structure. It consists of

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two different input ports: the first one is very linear (M_5 and M_6) and it is driven by the input signal; the second one is used as a switch (M_1 to M_4) and it is driven by a large signal LO.

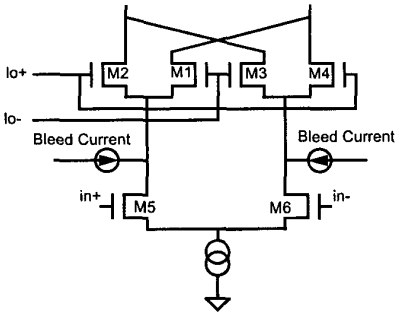

Fig. 2 Generic Mixer based on Gilbert Cell

The direct conversion topology needs two mixers to up-convert the I/Q signal from base-band to RF, their output signals must be added at the output for image rejecting[4]. This operation is obtained by injecting their currents to a common L/C resonating load (see Fig. 3).

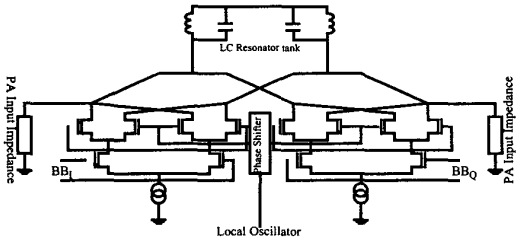

Fig. 3 0dBm Image Rejection Up Converter Mixer

Each mixer consumes 8mA, a bleed current technique is used to reduce the current that flows through the switches but not in the input pair (see Fig. 2), in order to optimize the linearity performances.

A poly-phase filter has been used to generate the quadrature signals, a differential pair buffer with L/C tank is used to drive the mixer. The entire phase shifter consumes 30mA and it allows the transmitter to achieve more than 30dB of image rejection.

IV. Power Amplifier

Reflex25 specifications require an output power greater than 1W@900MHz[3]; the low voltage supply makes the PA design very challenging because of the low impedance level.

The constant envelope modulation used in the Reflex25 (4-FSK) protocol allows to use high class switched mode PA. This kind of Amplifiers has an intrinsic high efficiency and its non-linear behavior does not constitute a drawback when using this kind of modulation[4].

As it has been already mentioned we decided to use a differential topology, the better isolation among different blocks not being the only advantage. Each branch of the PA has to deliver half of the power compared to a single-ended solution where, to obtain 1W over a 3Volts power supply, a 2Ω output impedance would be required. Using a balanced solution each branch delivers the power over a 4Ω impedance (8Ω differential) producing several advantages for the impedance transformation.

As we said before the constant envelope modulation allows to use a switched amplifier as final stage. Class E scheme could guarantee the same maximum theoretical efficiency[2]-[4] as the class F one, but the difficulty to generate an on-chip squarewave with sharp edges [6] has led us to choose the second solution.

The power gain specification has been estimated considering the stability limitations and the output power available from the mixer. A two gain stages PA is able to provide 30dB of power gain.

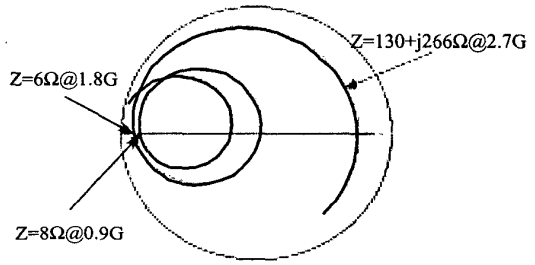

Fig. 4 Smith Chart Load Impedance

The first step is to design the output transistor and to determine its optimum load. An estimation of the 0.35μm MOS power density under 3V power supply gives us a 5000μm wide transistor in order to get the required output power (1W differential). The corresponding optimal load at the fundamental frequency is about 4Ω single ended and 8Ω differential.

The idea of class F amplifier is to create a squarewave at the drain of the device exploiting the harmonic generation. The spectral density of an ideal squarewave has contribution only from odd harmonics so the goal is to present high impedance for these and a low impedance for the even ones. Fig. 4 shows on the Smith diagram the values of the impedances for the fundamental, the 2nd and 3rd harmonic. Combined with the quasi semi-sinusoidal waveform of the drain current this kind of load allows to form a quasi squarewave drain voltage, giving an estimated efficiency of 75%.

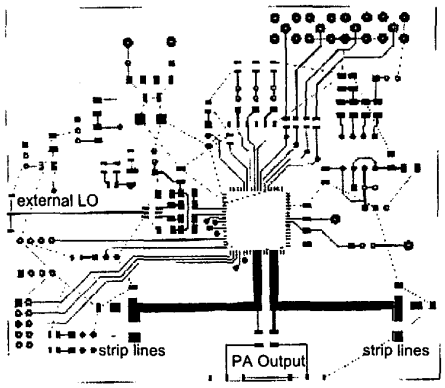

Fig. 5 Testing Board Layout

Given its high transformation ratio, the class F network has been realized by using external very low cost on board strip lines[7]. Fig. 5 shows the board layout where the large width strip-line represents the Class F impedance matching network.

The output stage power gain (transistor M_1 in Fig. 6) sets the first stage transistor width to 1000μm (M_2). For efficiency and gain considerations the driver is class AB biased and a L/C impedance matching network is placed between the two stages. This integrated matching network uses a DC block metal1/metal2 capacitor (C_1=18pF) and a metal 4 inductor (L_1=3.1nH) which, associated with the bonding, provides the adequate load at the driver output to optimize the power transfer.

Fig. 6 shows the simplified circuit scheme of the power amplifier (single-ended representation) where the on Chip components are pointed out.

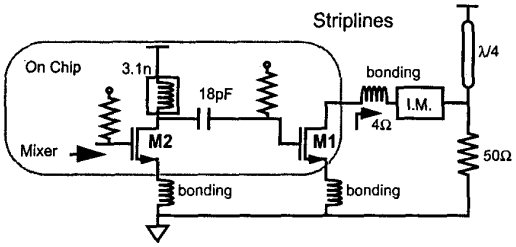

Fig. 6 Single Branch Power Amplifier Scheme. M_2=1000/0.35μm, M_1=5000/0.35μm

All the blocks have been packaged into a TQFP80 slug down; the advantage of this solution is that the metallic die pad is connected directly to the ground of the board. In this case the VSS of the chip is bonded directly to the die pad through multi bonding with a consequent reduction of the parasitic inductance. This approach decreases the power gain loss of the PA and improves its stability.

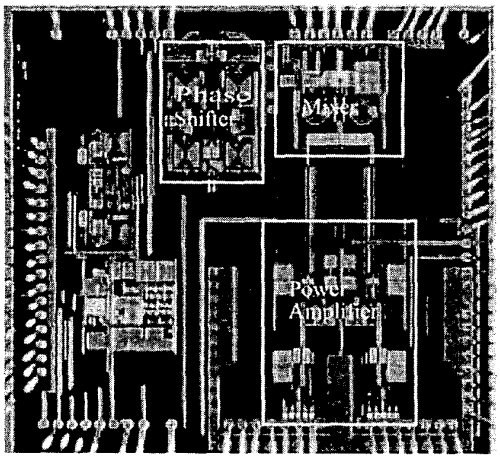

Fig. 7 Chip Picture

Multiple bonding has been also used to transfer the power outside the chip. It is important to point out how the package and the bondwire parasites have a very critical influence on the impedance matching. The spread out of their typical values modifies the impedance seen by each harmonic. Under these conditions the voltage waveform at the drain of the PA is not a quasi-squarewave anymore and output power and efficiency decrease.

Fig. 7 shows a picture of the chip with bond-wire.

V. Experimental Results

All the test has been made at room temperature, an external LO has been utilized to generate the phase shifter driving signal. Fig. 8 shows the board used to characterize the transmitter, the measurements reported in this work do not include the de-embedding of the losses in the board.

The efficiency shown in the measurement must not be intended as the power added one since there is no possibility of measuring the power at the input of the power amplifier. The efficiency η is expressed as:

$$\eta = \text{Output Power/Power Consumption.}$$

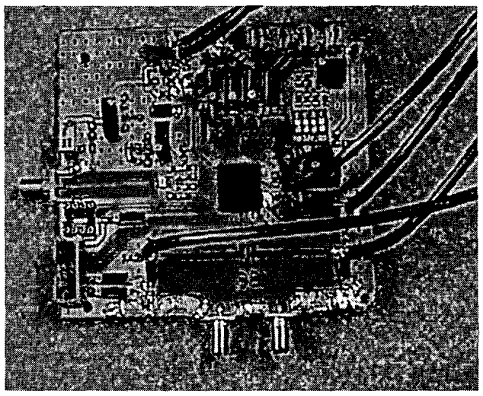

Fig. 8 Board Picture. It has been realized using FR4 for RF performances optimization.

Compression point measurement over the entire transmitter has been done.

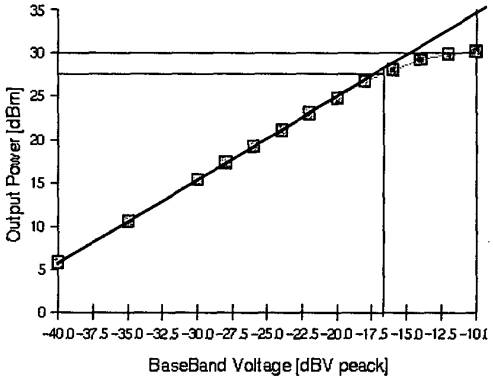

Fig. 9 Output Power Vs. Input Baseband Signal Amplitude.

An I/Q voltage sinusoidal waveform at the frequency of 20Khz is swept from -40 to -10 dBV peak. Fig. 9 and Fig. 10 show output power of more than 30dBm and an Efficiency of

more than 50% at its maximum power. The Transmitter presents a compression point at 27.25dBm. Nevertheless the Power Amplifier can be used at higher output power to transmit a constant envelope modulation signal.

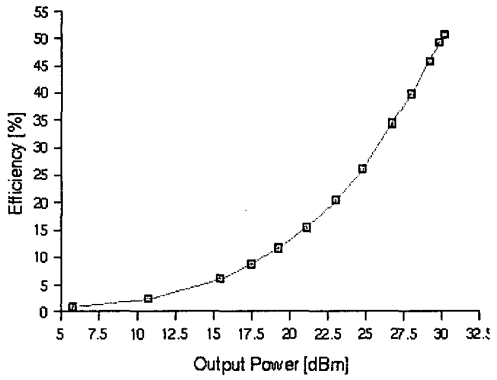

Fig. 10 Efficiency Vs. Output Power

The Power amplifier has been characterized at different supply voltages; Fig. 11 shows how the PA maintains a quite constant efficiency for different supply voltages.

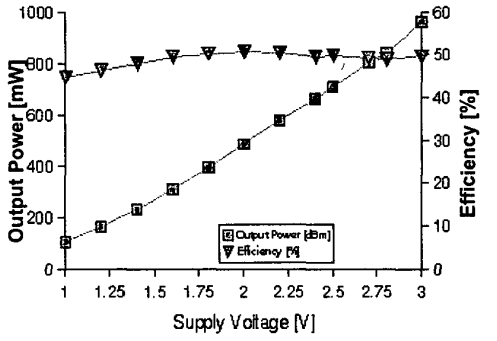

Fig. 11 Efficiency and Output Power Vs. Supply Voltage

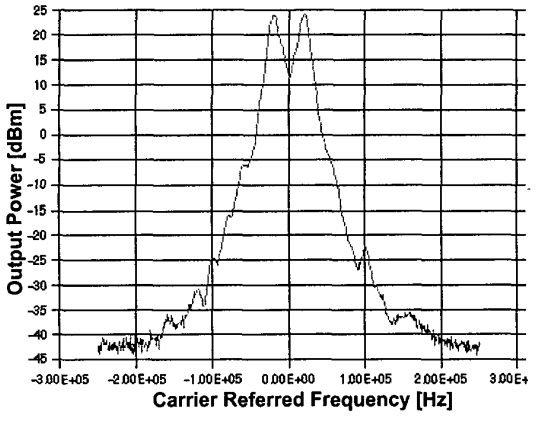

Fig. 12 Modulated Signal Output Spectrum for a FSK Signal. The Spectrum Analyser bandwidth is 10KHz.

The transmitter has also been tested with a modulated signal in the following conditions: a I/Q 2GFSK signal with gaussian filter coefficient=1, frequency deviation=20KHz and bit-rate=20Kbit/sec. has been injected at the baseband. Single-ended signal has been transformed to a differential one through a transformer with high pass corner frequency=10KHz, the power supply has been set to 2 Volts. Fig. 12 shows the spectrum analyzer output in the condition described above.

Table 1 shows the main measured results.

Operating Frequency	900MHz
Technology	0.35µm RFCMOS
Supply Voltage	3V
Output Power	30dBm
PA Efficiency	50%
Overall Efficiency	46.7%
Harmonics @ Maximum power	> 35dBc
Image Rejection	> 30dB
Mixers consumption	16mA
Phase-Shifter consumption	30mA

Tab. 1 Summary of the main testing results

VI. Conclusions

We have presented a RF part of a transmitter able to transmit more than 1W@900MHz, it has been integrated in a 0.35µm RF STMicroelectronics CMOS technology. The impedance matching has been done with very low cost components and the chip has been packaged on a TQFP80 slug down package. The testing results have shown the capability to transmit 30dBm with an overall efficiency of 46,7%, more than 50% including only the PA.

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VII. References

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