A High Efficiency WCDMA RF Power Amplifier With Adaptive, Dual-Mode Buck-Boost Supply and Bias-Current Control

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***Abstract*—Radio-frequency (RF) power amplifiers (PAs) are often the most power-consuming blocks in portable wireless systems, and maintaining high PA efficiency at heavy and light loads is therefore critical for extended battery life. This letter presents how a 0.5-μm CMOS dynamically adaptive, dual-mode buck-boost power supply and bias-current control circuit improves PA efficiency. The proposed system is validated with a 1.96-GHz, 25-dBm SiGe heterojunction bipolar transistor (HBT) wideband code division multiple access RF PA, where its supply voltage and bias current are dynamically adjusted from 0.4 to 4.5 V and 25 to 220 mA, respectively, over an output power range of −50 to 25 dBm. The prototype system is functional for a 1.8–4.2 V input supply range, meeting adjacent- and alternate-channel leakage ratio specifications with less than 10% of error vector magnitude across the entire power range. The average efficiency of the dynamically adaptive system (13.67%) was 7× better than the corresponding fixed-supplied, fixed-biased scheme (1.95%), with the same HBT PA.**

***Index Terms*—Adaptive bias, adaptive supply, battery life, dynamic bias, dynamic supply, power amplifier (PA), stand-by performance, wideband code-division-multiple-access (WCDMA).**

I. Introduction

HIGH efficiency during both heavy and light-to-moderate loads in portable battery-powered systems is critical for extended battery life, which is why custom high efficiency point-of-load power supplies are gaining popularity in next generation wireless systems [1]. In a state-of-the-art code-division-multiple-access (CDMA) system, for example, as many as eleven different power supplies are used [2]. Consequently, for a power-hungry application like a radio frequency (RF) power amplifier (PA), incorporating additional intelligence into already existing dedicated power supplies is logical and appealing. Although RF PA systems with boost [3], buck [4], and buck–boost [5] power supplies are published in literature, little effort has gone into optimizing these supplies to maintain high efficiency during light and moderate loads, which is the subject of this letter.

Light-load efficiency and low quiescent current are critical in portable wireless applications where battery life is important because mobile devices tend to mostly idle [6]. Unfortunately, conventional fixed-frequency pulse-width modulated (PWM) power supplies [3]–[5] incur relatively high switching power losses when lightly loaded. The situation is exacerbated by the stand-by quiescent current demands of the complex electronics used to regulate and control it. An adaptive dual-mode buck–boost power supply approach is therefore proposed whereby switching losses and quiescent current requirements are reduced during light loading conditions.

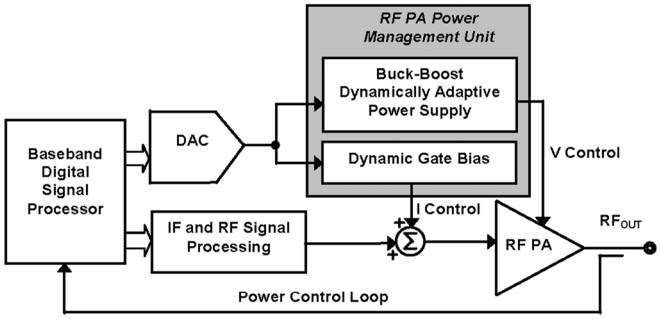

Fig. 1. Proposed dynamically adaptive RF PA power management system.

The proposed dual-mode supply operates in PWM control in moderate-to-high load levels and in pulse-frequency modulation (PFM) during light loads. Since the PFM mode supply runs at lower switching frequencies and demands less quiescent current (simpler circuit), system efficiency is improved during stand-by and idle modes, the result of which is higher average power efficiency and therefore extended battery life. As in [5], the bias current of the PA is also dynamically adjusted to further decrease the power losses in the PA itself, maintaining high system efficiency over a wide output power range. In addition to "continuously" adapting the biasing point of the PA, discrete two- and three-step adaptive schemes [7] are also presented, tested, and compared.

II. Proposed System

The biasing conditions of the proposed PA track the average power demands of the system, which are in turn set by an outer power control loop through a digital-signal processor (DSP), as shown in Fig. 1. The output of the DSP is decoded into an analog signal by a digital-to-analog converter (DAC) and fed into the power management unit. The supply and bias current of the proposed PA dynamically increase (decrease) with rising (falling) output power levels, but only as much as linearity performance specifications will allow.

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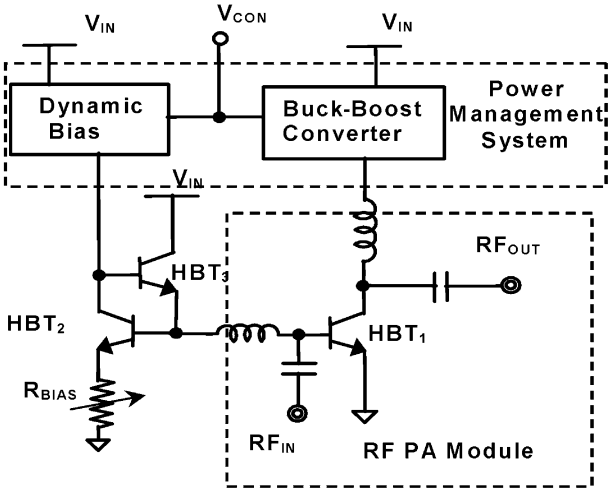

Fig. 2. Proposed embodiment of the dynamically adaptive voltage- and current-biased PA system.

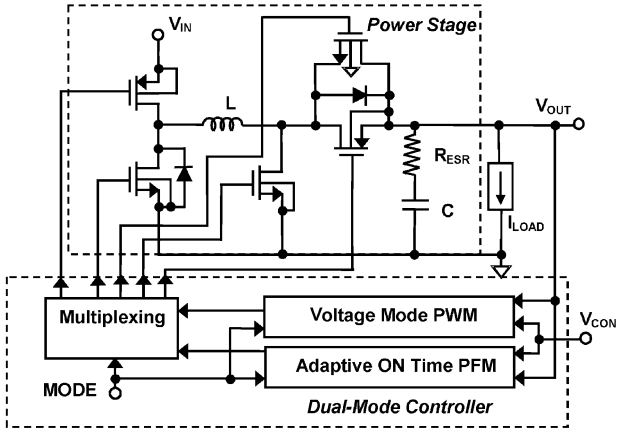

Fig. 3. Dual-mode buck-boost switching power supply prototype.

The proposed system proportionately decreases the PA's biasing supply voltage and current from 4.5 V and 220 mA to 0.5 V and 25 mA with decreasing output power levels, where output power is expressed as the ratio of the square of peak output voltage and PA load resistance. A 25 to 5 dBm output power variation yields a power-control range of 20 dB, below which the PA supply voltage and bias current remain at their lowest values. The power range is therefore partitioned in two, the dynamically adaptive high power region, where a fast high power PWM dc–dc supply circuit is quick enough to track the 1-dB power step changes demanded by the base station's control signal, and the constant low power region, where a slow responding low power PFM dc–dc converter circuit supplies a fixed 0.5 V supply. To generate a 0.5 to 4.5 V supply for the PA from a 1.8–4.2 V source, a noninverting buck–boost converter is used. The buck–boost circuit has three regions of operation: PFM buck (step-down), PWM buck, and PWM boost (step-up) for low, moderate, and high power levels, respectively.

III. Hardware Implementation

The proposed power supply and bias control circuits were designed and fabricated using AMI's 0.5-μm CMOS process and then applied to a 1.96-GHz silicon-germanium (SiGe) hetero-junction bipolar transistor (HBT) WCDMA RF PA from Sirenza Microdevices, as shown in Fig. 2. HBT_1 is the RF PA and HBT_2-HBT_3-R_{BIAS} combination comprise a β-helped Widlar current mirror, in other words, the dynamic current-driven bias-current generator circuit. The dynamic bias block is a transconductor whose input control signal V_{CON} and therefore output current are proportional to the output power of the PA, as discussed in Section II.

The dual-mode PWM–PFM controlled buck–boost switching supply circuit is shown in Fig. 3 [8]. The power stage is comprised of a 1-μH power inductor, 20-μF output capacitor with an equivalent series resistance (ESR) of 10 mΩ, a 47 μF input capacitor with an ESR of 5 mΩ, and five integrated 0.5-μm power field-effect transistors (FETs) with their respective body diodes. The feedback loop is closed through a PWM or a PFM control path, depending on the output power level of the PA (i.e., MODE), via a multiplexing control-signal generator that introduces dead-time between switching transitions to prevent short-circuit conditions from occurring. A two-zero/three-pole, type III external filter network is used to ensure the feedback control loop is stable across all possible operating conditions in PWM control. The measured quiescent currents of the power supply circuit in PWM and PFM modes were 800 and 140 μA, respectively, the latter represents an 82% reduction in quiescent power, which is especially significant in idle and stand-by operation.

IV. Experimental Results and Discussion

The prototype PA was tested with a 1.96-GHz, 3.84-MHz bandwidth, hybrid phase-shift keying (HPSK) modulated, WCDMA signal. The measured adjacent- and alternate-channel leakage ratios (ACLRs) of the PA over its full output power range of -50 to 25 dBm were less than -35 and -58 dBc, respectively, satisfying WCDMA requirements. The power gain of the PA had a 4–10 dB variation across the entire output power range, when the bias supply voltage and currents were changed from 4.5 V and 220 mA to 0.4 V and 25 mA. The measured error vector magnitude (EVM), which denotes the phase performance of the digital-modulation scheme (WCDMA PA in this case), was 2%–10%, indicating an acceptable bit-error rate (BER) performance.

The efficiency performance of interest for a PA with wide output power range is average power efficiency [5], which is the ratio of average output-to-input power. The average input power of the proposed PA system is the area under the weighted input supply power trace shown in Fig. 4(a), which is shown to be significantly lower than its fixed supply counterpart. As a result, the average power efficiency of the dynamically biased PA with the dual-mode (PWM–PFM) dc–dc switching supply outperformed the fixed-supply scheme by a factor of seven, which directly translates to extended battery life.

To evaluate the performance of the proposed dual-mode power supply scheme, a battery capacity of 1200 mWh (e.g., 1.5 V and 800 mAh) is assumed. Consequently, taking into account power supply stand-by (quiescent) current and assuming the system is active 5% of the time and idling for the remainder,

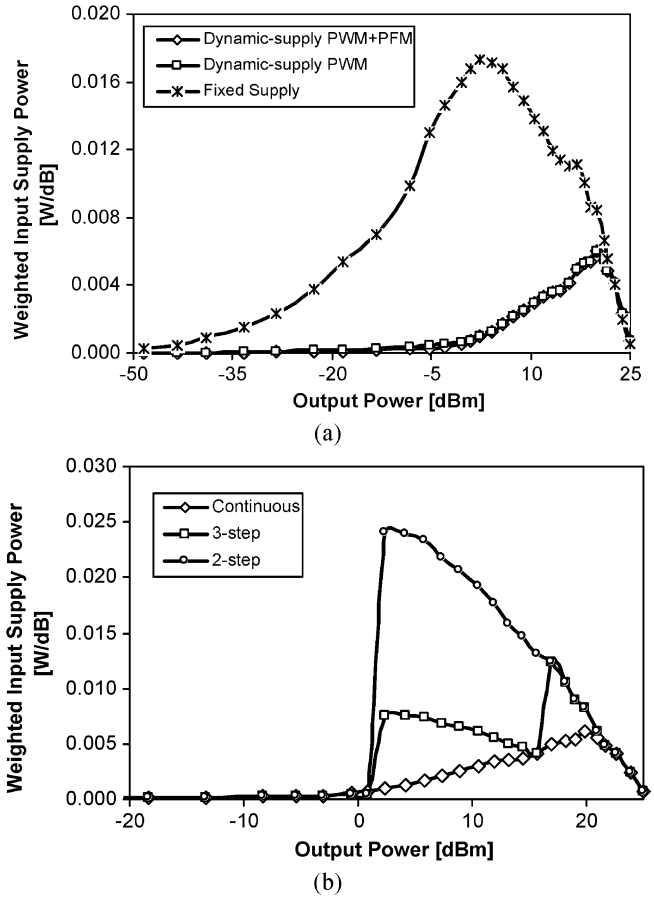

Fig. 4. Experimental weighted supply power profile performance as a function of output power for the proposed (a) continuous and (b) two- and three-step versions of the dynamically adaptive biasing scheme.

a PA with the proposed dual-mode supply has twice the battery life of a PWM-only scheme. The battery life improvement of the proposed approach is attributed to the lower power losses (i.e., switching and quiescent current) of the PFM circuit, which translates to higher efficiency at lower levels of transmitted output power.

In addition to continuously adapting the biasing point of the PA, a discrete two- or there-step approach [7] can be adopted for simplicity. For example, the entire output power range can be divided in two or three, each having a fixed predetermined supply voltage, as shown in Fig. 4(b). Decreasing the resolution like this, however, degrades overall PA efficiency, but decreases circuit complexity.

As shown in Table I, the overall PA efficiency of the proposed HBT PA system outperforms state-of-the-art solutions, when assuming the urban output transmitted power probability distribution of [5]. As mentioned earlier, the key feature of the proposed dual-mode control scheme is its ability to maintain high efficiency over a wide power range, especially during light-to-moderate output power conditions, where probability of occurrence is highest. The two- and three-step control alternatives, although simpler to implement, are not nearly as power efficient as the continuous version. Even though a buck–boost converter is necessarily less efficient than a buck converter, because of higher circuit complexity, the proposed buck–boost supply outperforms the best reported buck-only approach.

TABLE I
COMPARISON BETWEEN THE PROPOSED ADAPTIVE PA SUPPLY AND BIAS SCHEME WITH STATE-OF-THE-ART SOLUTIONS

	PA Scheme	Maximum Output Power	Fixed-Supplied Efficiency	Dynamic-Supply Efficiency
Reported work	Buck converter supplied AlGaAs/InGaAs MESFET PA [4]	28 dBm	2.2%	11.2%
	Boost converter supplied GaAs MESFET PA [3]*	26 dBm	3.89%	6.38%
	Buck-boost converter supplied LDMOS PA [5]	27 dBm	1.53%	6.78%
This work	V-I Controlled, buck-boost converter supplied HBT PA (Continuous)	25 dBm	1.95%	13.67%
	V-I Controlled, buck-boost converter supplied HBT PA (3-step)	25 dBm	1.95%	7.87%
	V-I Controlled, buck-boost converter supplied HBT PA (2-step)	25 dBm	1.95%	3.24%

* Output power probability distribution profile used in [3] is different.

V. CONCLUSION

This letter presented how a 0.5-μm CMOS dual-mode power supply and bias current control circuit improved the light-to-moderate power efficiency performance of a 1.96-GHz, 3.84-MHz baseband bandwidth, 25-dBm WCDMA RF PA. High efficiency (i.e., battery life) in this region is crucial in battery-powered systems because they tend to idle most of the time. The prototyped PA met all WCDMA requirements while yielding 7$\times$ higher average efficiency, when compared to conventional fixed-bias systems. In fact, the light load efficiency improvement that the proposed dual-mode power supply approach extended the battery life of the system 100% (i.e., 2$\times$) over the dynamically biased PWM-only mode supply.

REFERENCES

[1] D. Maksimović, "Power management model and implementation of power management ICs for next generation wireless applications," presented at the International Conference on Circuits and Systems (ISCAS) 2002, [CD ROM].

[2] G. Hurtz and D. Sugasawara, "CDMA handset design challenge: 11 separate power supplies," *Commun. Design—EE Times Publ.* 2003 [Online]. Available: http://www.commsdesign.com/design_corner/showArticle.jhtml?articleID=12804119

[3] G. Hanington, P. Chen, P. M. Ashbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.

[4] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA power amplifier using dynamic envelope tracking technique," in *IEEE MTT-S Dig.*, 2000, pp. 873–876.

[5] B. Sahu and G. A. Rincón-Mora, "A high-efficiency, linear RF power amplifier with a dynamically adaptive buck-boost supply," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 1, pp. 112–120, Jan. 2004.

[6] G. Hau, T. B. Nishimura, and N. Iwata, "A highly efficient linearized wideband CDMA handset power amplifier based on predistortion under various bias conditions," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1194–1201, Jun. 2001.

[7] T. Fowler, K. Burger, N. Cheng, A. Samelis, E. Enobakhare, and S. Rohlfing, "Efficiency improvement techniques for linear CDMA and WCDMA power amplifiers," in *Proc. Radio Freq. Integr. Circuits Symp.*, 2002, pp. 41–44.

[8] B. Sahu and G. A. Rincón-Mora, "A low voltage, high-efficiency, dual-mode, dynamically adaptive CMOS buck-boost power supply circuit," *J. Solid-State Circuits*, to be published.