A Digitally Modulated Polar CMOS Power Amplifier With a 20-MHz Channel Bandwidth

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Abstract—This paper presents a CMOS RF power amplifier that employs a digital polar architecture to improve the overall power efficiency when amplifying signals with high linearity requirements. The power amplifier comprises 64 parallel RF amplifiers that are driven by a constant envelope RF phase-modulated signal. The unit amplifiers are digitally activated by a 6-bit envelope code to construct a non-constant envelope RF output, thereby performing a digital-to-RF conversion. In order to suppress the spectral images resulting from the discrete-time to continuous-time conversion of the envelope, the use of oversampling and four-fold linear interpolation is explored. An experimental prototype of the polar amplifier has been integrated in a 0.18-μm CMOS technology, occupies a total die area of 1.8 mm^2, operates at a 1.6-GHz carrier frequency with a channel bandwidth of 20 MHz. For an OFDM signal, it achieves a power-added efficiency of 6.7% with an EVM of -26.8 dB while delivering 13.6 dBm of linear output power and drawing 145 mA from a 1.7-V supply.

Index Terms—CMOS RF, IEEE 802.11g, L-fold linear interpolation, polar transmitter, power amplifier.

I. INTRODUCTION

THE increasing demand for high data-rate wireless communications has driven the development of wide bandwidth, high data-rate wireless protocols such as Wireless LAN IEEE 802.11g [1]. In order to efficiently use the limited available frequency spectrum, these wireless systems employ spectrally efficient modulation, such as orthogonal frequency division multiplexing (OFDM). IEEE 802.11g systems, for example, are capable of transmitting data at the rate of 54 Mb/s while occupying a channel bandwidth of only 20 MHz. This bandwidth efficiency in the frequency domain comes at the expense of an increased peak-to-average-power ratio (PAPR) in the time domain. For example, IEEE 802.11g OFDM signals theoretically have a PAPR of 17 dB. In contrast to constant-envelope modulation, such as Gaussian Minimum Shift Keying (GMSK), amplifying signals with such a high PAPR requires

highly linear amplification, which is typically achieved by employing a linear class-A power amplifier with a large power back-off from its saturated output power. Due to the reduced power efficiency that accompanies this large back-off, the average power efficiency and battery lifetime are severely compromised.

The tradeoff between linearity and power efficiency in power amplifiers has been investigated extensively [2], [3]. Numerous methods have been proposed to either improve the efficiency of linear amplifiers or linearize the more efficient nonlinear amplifiers without significantly degrading their efficiency. Envelope-elimination and restoration (EER) is a technique based on performing efficient constant-envelope amplification of the phase-modulated portion of the input signal and then restoring the envelope by amplitude modulation at the output [4]. In effect, an EER system is a polar transmitter in which the signal is decomposed into a constant-envelope RF phase-modulated signal and an envelope component. Several papers have demonstrated the suitability of such architectures for CMOS implementation [5]–[7], and polar transmitters that take advantage of the digital signal processing to ease the generation of phase and amplitude signals have been successfully implemented [8], [9]. However, implementation of the amplitude modulation has typically limited the signal bandwidth of polar architectures to the vicinity of 1 MHz.

This paper describes a digitally modulated polar power amplifier with a 20-MHz channel bandwidth and the linearity required for IEEE 802.11g systems [10]. The amplifier employs an array of 64 constant-envelope transconductance "unit" amplifiers that are digitally activated by a 6-bit envelope code. By adapting the number of active amplifiers, and thus the dc current, to the envelope, the amplifier achieves a significant improvement in efficiency at back-off power levels when compared to a conventional class-A linear amplifier, thereby improving the average efficiency. An experimental prototype of the proposed amplifier, integrated in a 0.18-μm CMOS technology, meets the linearity requirements of the IEEE 802.11g standard and provides more than a factor of two improvement in average power efficiency compared to operating the same circuit as a linear class-A amplifier. L-fold linear interpolation [12] and oversampling are shown to be a means of suppressing the spectral images that result from the discrete-time to continuous-time conversion of the envelope.

Section II begins with an overview of class-A and polar amplifiers before introducing the proposed polar amplifier architecture. Section III describes details of the circuit design for a CMOS implementation of the proposed architecture. Measured results obtained for the experimental prototype are then presented in Section IV, and the work is summarized in Section V.
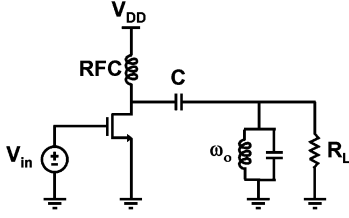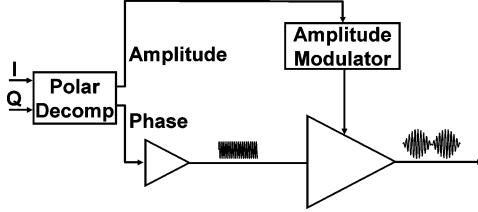
Fig. 1. Class-A power amplifier.

Fig. 2. Polar transmitter architecture.

II. ARCHITECTURE

A. Class-A Power Amplifiers

Fig. 1 shows the schematic of a conventional class-A power amplifier. The amplifying transistor is biased so that it conducts for the entire range of the input swing [13]. The power efficiency of this amplifier is given by

$$\eta = \frac{P_{\text{out}}}{P_{\text{supply}}} = \frac{\frac{I_{\text{RF}}V_{\text{RF}}}{2}}{I_{\text{DC}}V_{\text{DD}}} \tag{1}$$

where I_{RF}, V_{RF}, I_{DC}, and V_{DD} are the amplitudes of the drain current and voltage swings, the dc bias current and the supply voltage, respectively. Since I_{RF} and V_{RF} are smaller than I_{DC} and V_{DD}, respectively, the maximum possible efficiency is 50%. In practice various loss mechanisms and nonidealities often degrade this number to the range of 25–35%.

Since, for the amplifier in Fig. 1, I_{DC} and V_{DD} do not adapt to variations in the amplitude of the input, it can be seen from (1) that the efficiency degrades linearly as the output power is reduced. The average efficiency depends on the statistical characteristics of the envelope (or the instantaneous power), and can be computed as

$$\langle \eta \rangle = \int_{0}^{\text{max power}} \eta\,(p)\,f\,(p)dp \tag{2}$$

where $f(\cdot)$ is the probability distribution function of the instantaneous power. For example, for an ideal class-A power amplifier (assuming 50% efficiency at the peak power) with a 10-dB power back-off, the average efficiency is only 5%.

B. Polar Transmitters

Several approaches have been proposed to achieve more efficient linear power amplification [2]. Polar amplification provides the opportunity to take advantage of constant-envelope amplifiers, which are inherently more efficient than linear amplifiers. Polar transmitters have also received increased attention due to advantages over conventional I/Q modulation in certain applications [7], [14].
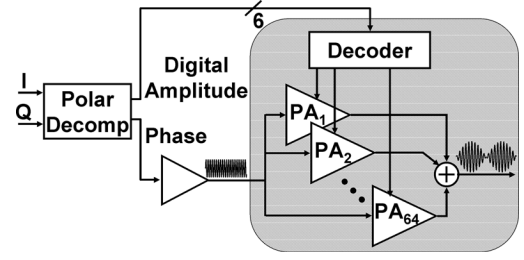

Fig. 3. Proposed polar power amplifier architecture.

Fig. 2 illustrates the operation of a polar transmitter. At the baseband, the Cartesian coordinates (I and Q) of an RF signal are converted to polar coordinates according to

$$A = \sqrt{I^2 + Q^2} \tag{3}$$

$$\varphi = \tan^{-1}\left(\frac{Q}{I}\right). \tag{4}$$

Instead of using an I/Q modulator, in a polar transmitter the amplitude and phase of the carrier are modulated separately according to (3) and (4). Several techniques have been proposed for the amplitude modulation of a phase-modulated signal, including modulating the supply voltage [9], modulating the amplifier current [14], and digitally mixing the input signal to a bank of switch-mode amplifiers [8]. These techniques have been all successfully implemented for Enhanced Data Rates for GSM Evolution (EDGE) applications. However, the much higher PAPR and bandwidth of wireless LAN applications such as IEEE 802.11g pose extraordinary challenges for the amplitude modulation. Since the linearity of the amplifier is determined by the linearity of the amplitude modulation, the modulator must provide high linearity. In the case of an IEEE 802.11g channel the occupied bandwidth is 16.6 MHz, but the nonlinear operation of (3) increases the bandwidth of the envelope to almost 40 MHz. In this work, we have adopted an open loop architecture to meet this bandwidth demand.

C. Proposed Polar Power Amplifier

Fig. 3 illustrates the proposed polar power amplifier architecture. At the input, baseband in-phase (I) and quadrature (Q) signals are digitally converted into envelope and phase components. The phase component is then converted into a constant-envelope RF signal that drives an array of parallel unit amplifiers. These unit amplifiers are digitally activated by the envelope code, and their outputs are combined to shape the RF output signal. In effect, this system provides a digital-to-analog conversion of the envelope, while performing efficient constant-envelope amplification in the RF phase domain. The focus of this work is on the shaded area of Fig. 3. In the experimental prototype reported herein, the envelope and RF phase signals are generated off-chip.

System simulations indicate that the error-vector-magnitude (EVM) and spectral mask specifications for a 64QAM OFDM IEEE 802.11g signal require at least 6-bit digital encoding of the envelope. Thus, the polar power amplifier in this work comprises 64 nominally identical unit amplifiers. Compared to a binary-weighted approach, the use of equal-weighted amplifiers offers better matching and DNL performance because only one
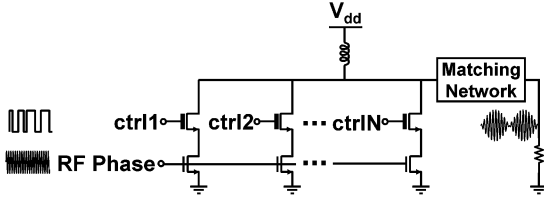
Fig. 4. Polar transmitter output stage.

TABLE I
AVERAGE EFFICIENCIES FOR CLASS-A AND THE
PROPOSED POLAR ARCHITECTURE

Power Backoff	Efficiency with ideal class-A PA	Efficiency with the proposed architecture
6dB	14.2%	23.2%
10dB	5.0%	14.0%
12dB	3.1%	11.1%

unit is switched as the digital input is changed by one LSB. This approach also reduces glitches at the switching instances and improves the dynamic performance [15]. Digital predistortion [2] and/or tapering the weight of the units might be used to improve the INL and DNL performance of the digital-to-analog conversion. However, these techniques were not explored in this work.

This design could be extended to support transmit output power control. The average output power of the amplifier can be varied digitally by changing the average amplitude of the envelope signal. However, providing output power control without degrading the EVM requires increasing the number of quantization levels for the envelope and the number of unit amplifiers.

Equal-weighted amplifiers require thermometer decoding, which has the drawback of an increased area. However, this increase is not significant when compared to the size of the unit amplifiers themselves. The major challenge is to provide a means for combining the output power of multiple amplifiers.

Conventional methods for power combining utilize transmission lines, transformers, or their lumped element approximations, which would occupy a large area at low gigahertz frequencies. In addition, their on-chip implementation in a CMOS technology results in large power losses [18]–[20]. In this work, current-summing power combination is employed, which can easily be extended to a large number of unit amplifiers. The unit amplifiers are current-source transconductance amplifiers that are wired in parallel at their drains. This architecture can be implemented with a compact layout, much like current-steering digital-to-analog converters (DACs) [15] and RF DACs [16]; however, the current sources are driven by a phase-modulated RF signal.

Fig. 4 is a simplified single-ended illustration of the amplifier circuit topology. The unit amplifiers comprise two transistors in series. The bottom transistors are driven by the RF phase signal. The cascode transistors act as switches and are controlled by the switching logic. The switches are implemented with thick-oxide I/O transistors to enable the use of a higher supply voltage and output voltage swing. As the cascode transistors of the unit amplifiers are switched on and off, the capacitance seen at the gate inputs of common-source transistors changes by about 10%, a variation that is easily tolerated in the design of the driver.

Although transconductance amplifiers with reduced conduction angles (such as class-C amplifiers) could be used as the unit amplifiers in this architecture to further improve the efficiency, class-A stages have been employed in this work so that the polar amplifier can be easily transformed into a class-A amplifier in order to compare the efficiency of the two configurations. This

transformation is accomplished by setting all of the envelope bits to one and driving the input with a linear OFDM signal.

Additional efficiency improvement is also possible by adapting the supply voltage as in envelope tracking systems [17]. However, this technique was not explored in this work.

D. Power Efficiency Improvement

In contrast to class-A amplifiers, the dc current in the proposed polar amplifier adapts as the envelope of the signal varies. Consequently,

$$\eta = \frac{\frac{I_{\text{RF}}V_{\text{RF}}}{2}}{I_{\text{DC}}V_{\text{DD}}} = \frac{\frac{V_{\text{RF}}}{2}}{V_{\text{DD}}} \propto \sqrt{P_{\text{out}}} \tag{5}$$

where I_{RF} and V_{RF} are the current and voltage amplitudes, respectively, and infinite resolution is assumed for the digitization of the envelope (so that $I_{\text{DC}} = I_{\text{RF}}$). Although the maximum efficiency is same as for class-A amplifiers, because of the higher efficiency at back-off power levels the average efficiency is significantly improved. Table I compares the average efficiency of this architecture, based on (5), to that of an ideal class-A amplifier, based on (1), for various power back-offs. The average efficiency values are obtained using (2) with a Rayleigh distribution assumed for the probability distribution of the envelope of the signal. It can be seen that the polar architecture offers significant power savings when linearly amplifying signals at a large back-off from the saturated output power.

E. Spectral Images

The digitally-modulated polar RF amplifier is essentially a digital-to-RF power converter. The energy in the resulting spectral images can be quite high and can violate the spectral mask and the constraints on out-of-band emissions. Since some of these images are close to the carrier frequency, using conventional filters to remove them is not feasible. The images can, however, be suppressed by increasing the sampling frequency and interpolating the input signal. Fig. 5 shows the result of oversampling the input in the digital domain at 4 and 8 times the Nyquist rate. It can be seen that even with 8x oversampling, the power in the images is still too high.

If, in addition to oversampling the input signal, linear interpolation is used at the output, it is possible to significantly increase the suppression of the images. However, the implementation of such interpolation faces severe technical challenges. L-fold linear interpolation is a staircase approximation to linear interpolation that can be more easily implemented [12]. In this work we have used four-fold linear interpolation as illustrated in Fig. 6, effectively further increasing the sampling rate at the output. Instead of a large step change at the sampling instances,
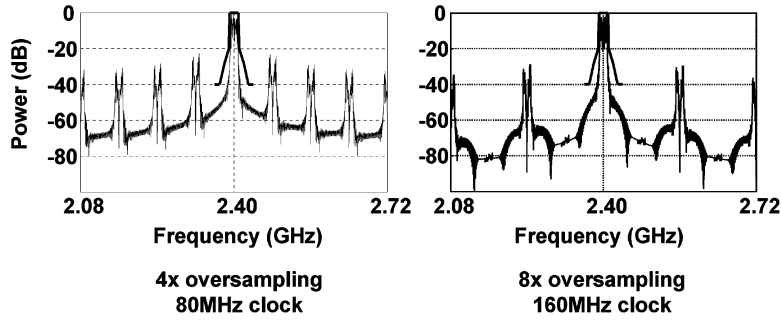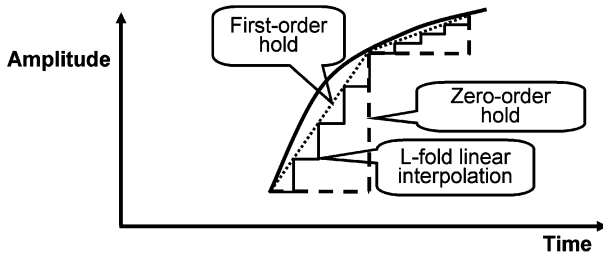
Fig. 5. Output spectra with oversampling.

Fig. 6. Illustration of four-fold linear interpolation.

Fig. 7. Simulation results for four-fold interpolation with oversampling.

four smaller steps are used to approximate linear interpolation. In order to implement the four-fold interpolation, the unit amplifiers are each divided into four sub-amplifiers that are activated sequentially using four quadrature-phased clocks.

Four-fold linear interpolation is essentially a combination of linear interpolation (with 4 times oversampling) followed by a zero-order hold [11]. The linear interpolation suppresses the spectral images at $\pm f_S$, $\pm 2f_S$, and $\pm 3f_S$ frequency offset by the sinc^2 function, where f_S is the sampling rate of the digital baseband envelope signal after oversampling. The images at offsets of $\pm 4f_S$ and above are far enough from the center frequency to be sufficiently suppressed by the zero-order hold (sinc function) and the RF bandpass output matching network.

As a consequence of only interpolating the envelope of the RF signal, the amplifier output differs slightly from the output that would be obtained by interpolating the output signal itself. This deviation translates into spectral regrowth and EVM degradation in the output. Compensation of the phase signal can be used to resolve this issue at the expense of an increased clock rate for the phase signal. Alternatively, the errors can be suppressed by increasing the oversampling ratio.

Fig. 7 shows the simulation results obtained with four-fold interpolation when applied to the envelope of an oversampled IEEE 802.11g signal. In this simulation, an IEEE 802.11g signal is upsampled to 80 MHz [Fig. 7(a)] and 160 MHz [Fig. 7(b)] in the digital domain and decomposed into envelope and phase components. The phase component is further low-pass filtered to suppress its spectral images. As can be seen, the use of four-fold linear interpolation eases the need for high oversampling ratios. With 4x oversampling, the spectral mask and EVM requirement for IEEE 802.11g signals can be met, albeit with little margin. The margin is much improved if the oversampling is increased to 8x.
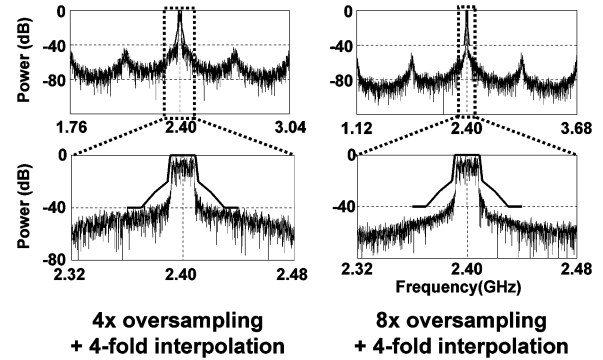
III. IMPLEMENTATION

A. Circuit Schematic

Fig. 8 shows a simplified circuit schematic for the polar amplifier. A single driver stage provides sufficient voltage drive to all of the output amplifiers. The driver employs the same cascode architecture as the output stage, but with the gate of the cascode transistor biased at a fixed voltage. This allows a higher supply voltage, and thus a larger voltage swing, at the output of the driver. Although the driver could be biased as a class-C amplifier, as in the output stage a class-A amplifier is used so as to allow easy transformation to class-A operation of the overall amplifier. The matching network between the driver and the output stages is implemented with on-chip spiral inductors and bond wires. Parts of both the RF input and output matching networks are realized using bond wires and off-chip components to allow more flexibility in tuning. In the actual implementation, the unit amplifiers and the driver stage are fully differential. The differential architecture relaxes the stringent demand for low-inductance ground bond wires while doubling the output voltage swing and lowering the current density in output devices, thus reducing the associated power loss. The drawback of using a differential architecture is the need for baluns at the RF input and output, which are lossy and add to the component count if implemented off-chip. In this work, off-chip baluns are used at both the RF input and output, and their losses were characterized with a test structure comprising two back-to-back baluns.

B. Layout

Fig. 9 illustrates the layout of the output stage. As noted previously, the output stage comprises 64 unit amplifiers that are
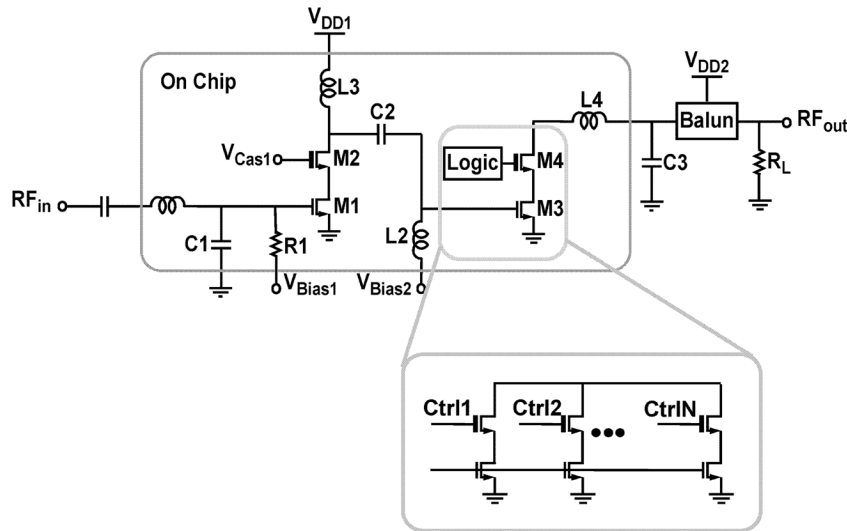
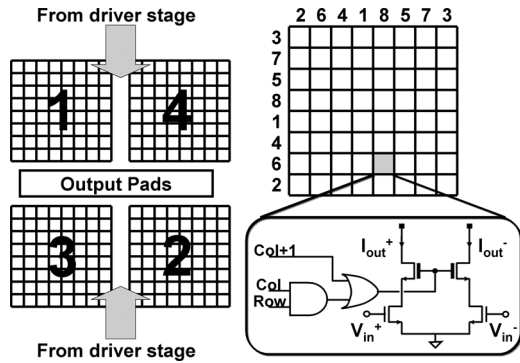Fig. 8.   Simplified schematic of the polar power amplifier.
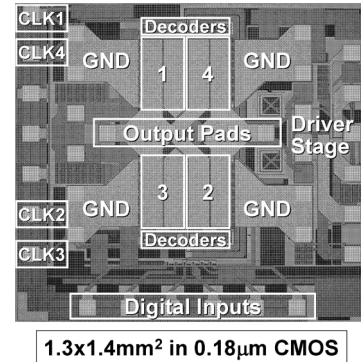

Fig. 9.   Layout of the output stage.

Fig. 10.   Die photomicrograph of the polar power amplifier.

Fig. 11.   Test board.

each divided into four sections. Sections with the same clock phase are grouped together, and thus four large quadrants are formed. In Fig. 9 the number identifying each quadrant corresponds to the number of the clock phase used to activate that quadrant. The clocks are offset from each other in the time domain by $T/4$, where $T = 1/f_S$. The three most significant bits of the digital envelope activate a row of unit amplifiers in each quadrant, while the three least significant bits activate the unit amplifiers within the selected row. The row and column placement is disordered, as shown in Fig. 9, in order to reduce the effect of thermal and process gradients. Many substrate contacts are placed around the output transistors, and care has been taken in the wiring to comply with the electromigration rules. The output pads are placed in the center to minimize resistive losses. The output nodes of the unit cells are wired together and their currents are summed at the output.

To reduce undesired feedback from the output stage into the driver, a separate ground pad is used for the driver stage. Also, an N-well guard ring is used to separate the driver and output stages. Placing the output bond wires orthogonal to the ground and input bond wires reduces magnetic coupling and the associated undesired feedback. An $N+$ diffusion shield layer is placed underneath the sign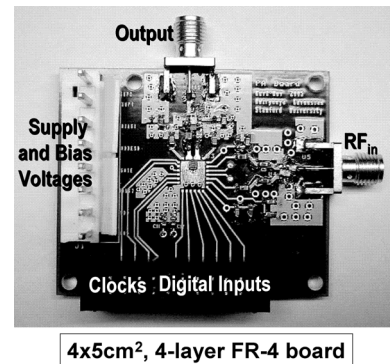al routing to reduce substrate loss. The spiral on-chip inductors were designed and analyzed using software introduced in [21] and [22]. Patterned ground shields are placed underneath the spiral inductors to reduce the loss due to substrate coupling [23].

Fig. 10 is a photomicrograph of the polar power amplifier die, which was fabricated in a 0.18-μm two-poly five-metal (2P5M) CMOS technology. The total chip area measures 1.8 mm^2. The output stage is in the center of the die, and multiple ground pads are positioned symmetrically around the output stage to provide
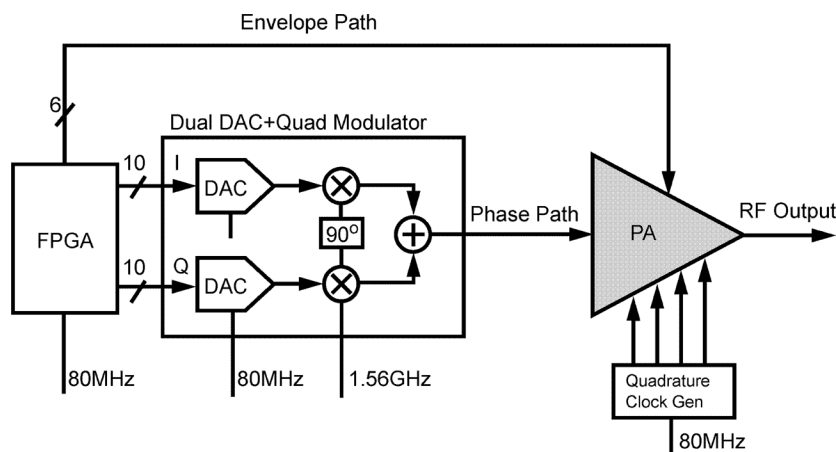
Fig. 12.   Demonstration system.

a low impedance path to ground. The RF phase input and the driver stage are on the right in Fig. 10, and the digital envelope input pads are located at the bottom.

Fig. 11 shows the test board used to measure the performance of the power amplifier. The chip is directly mounted on the board in center and bonded to gold-plated pads on the PCB. The board has four layers and is built of FR4 material. The board area measures 20 cm^2.

IV. MEASUREMENT RESULTS

Fig. 12 shows the demonstration system used to evaluate the performance of the polar power amplifier. An IEEE 802.11g 64QAM baseband signal sampled at 80 MHz is digitally decomposed into its phase and envelope and loaded into an FPGA. A dual-channel DAC with internal 8x upsampling and a quadrature RF modulator convert the FPGA output into the analog domain and transform the digital phase to the desired RF phase signal. The FGPA also directly drives the digital envelope input of the prototype power amplifier. Delay mismatch between the envelope and phase paths is compensated for by delaying the envelope signal digitally and by adjusting the delay between the FPGA and amplifier clocks. The RF center frequency is 1.6 GHz instead of the targeted 2.4 GHz because of errors in modeling the passive components.

Fig. 13 shows the measured output spectrum, which meets the spectral mask for the IEEE 802.11g protocol. Due to the clock rate limitations of the FPGAs used in the measurement setup, it was not possible to test 8x oversampling at 160-MHz clock rate. Therefore, a single 80-MHz clock was used to control the four amplifier quadrants in this experiment in order to avoid the nonlinearities introduced by four-fold interpolation at 80 MHz. The output constellation for a 64QAM signal is also shown in Fig. 13. The measured EVM of this 64QAM OFDM signal is -26.8 dB, which is better than the standard specification of -25 dB.

The measured output spectrum with four-fold interpolation is shown in Fig. 14. Spectral components beyond the shown frequency range were attenuated by the output matching network, which has a bandwidth on the order of 40 MHz. Table II summarizes the performance achieved. The 64QAM OFDM output
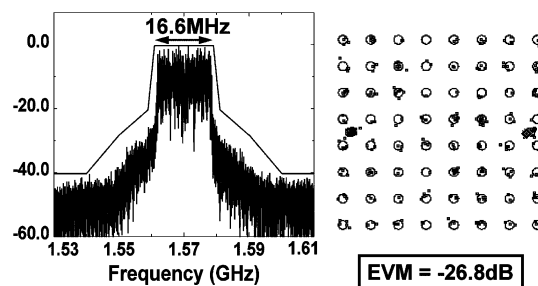

Fig. 13.   Measured output spectrum and constellation.
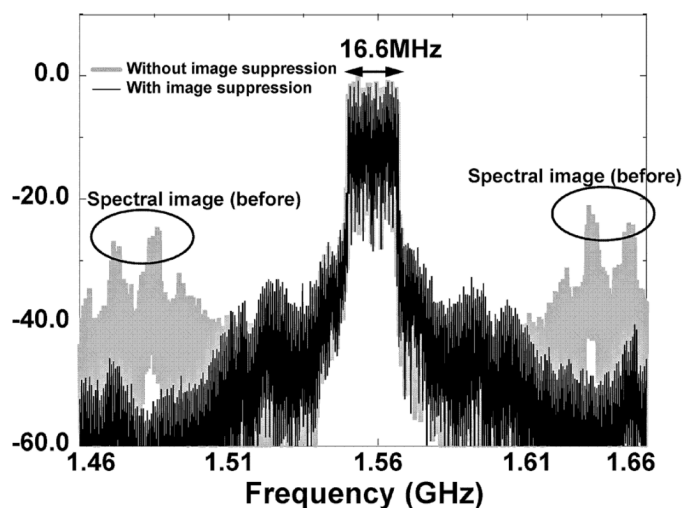
Fig. 14.   Measured output spectrum with four-fold linear interpolation.

power (including 1.1 dB loss in the output balun) is 13.6 dBm with an average power-added efficiency (PAE) of 6.7%. The measured input power is 2 dBm. The prototype power amplifier can be converted into a linear amplifier by setting all the envelope bits to one and driving the RF phase input of the power amplifier with a linear RF OFDM signal. The measured PAE of the amplifier in this linear mode is 3.1%, confirming that the digital modulation architecture more than doubles the measured power efficiency.

TABLE II
PERFORMANCE SUMMARY

Technology	0.18μm CMOS, 2P5M
Supply Voltage Digital Hardware Driver Stage Output Stage	 1.8 V 2.2 V 1.7 V
Linear 64 QAM OFDM Output Power	14.7 dBm 13.6 dBm (balun included)
EVM for 64 QAM OFDM	−26.8 dB
Dissipated Power Output Stage Driver Stage Digital	 247 mW 66 mW 3.4 mW
PAE (for 64QAM OFDM)	8.9% 6.7% (baluns included)
Center Frequency	1.56 GHz
Total Chip Area	1.8 mm^2

V. CONCLUSION

This research has demonstrated a polar power amplifier with a 20-MHz bandwidth and the linearity required for 64QAM IEEE 802.11g signals. The polar amplifier comprises parallel equal-weighted unit amplifiers that are driven by a constant-envelope phase-modulated signal and are digitally activated by the envelope code. Using transconductance amplifiers allows the use of simple and efficient current summation power combination method. Oversampling and L-fold linear interpolation were shown to suppress the spectral images resulting from the digital-to-RF power conversion. The polar amplifier was converted to a linear class-A amplifier by setting the envelope bits to one and driving the amplifier with a linear RF signal. Measurements confirm that the efficiency achieved in the polar mode is more than twice that in the class-A mode.

ACKNOWLEDGMENT

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