31.7 A Fully Integrated Quad-Band GSM/GPRS CMOS Power Amplifier

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There is a strong drive toward handheld communication devices with building blocks that are fully integrated in standard CMOS technologies. Although there are obvious cost, size, and repeatability advantages, it is particularly challenging to implement fully integrated power amplifiers with no external matching in standard CMOS under the large supply variations and harsh load mismatches present in handheld devices.

Distributed active transformers (DATs) have been shown as the way to solve this problem in a fully integrated fashion [1]. The DAT also alleviates the effect of the low quality factor passives used to integrate the output matching network. Although the DAT can be used to produce watt-level output powers at low GHz frequency range with good efficiency, its original implementation is more conducive to low supply voltages that is very useful for a low-battery-voltage solution. However, it is not compatible with the higher voltages presented by the Li-ion batteries which under charging situations can present supply voltages up to 5.5V to the PA.

Another challenge for a fully integrated commercial GSM/GPRS CMOS power amplifier is the potential load mismatch presented to the output of the PA mainly due to the changes in the relative position of conductive objects with respect to the antenna. The PA has to keep meeting its specifications for relatively large voltage standing-wave ratios (VSWRs) (8:1 at the PA output) for all potential phase angles. It also has to remain operational and should not be permanently damaged or degraded under an even greater VSWR (15:1 at the PA output). Additionally, it must not oscillate and its supply current has to be kept below a predetermined maximum under any of these conditions, with the output power tightly controlled over a broad range of power levels.

Figure 31.7.1 shows the block diagram of the presented quad-band fully integrated CMOS PA. It comprises two separate PAs on the same die, one for the two lower frequency bands (GSM at 850MHz and E-GSM at 900MHz) and another for the high bands (DCS at 1.75GHz and PCS at 1.9GHz). Both the low- and the high-band PAs are matched to 50Ω on-chip at their single-ended input and output terminals. The low-band (LB) PA is implemented using a double-concentric quad-core DAT, while the high-band (HB) PA is realized as a double-concentric triple-core DAT. A sophisticated on-chip power control monitors the output power and supply current of the PA and adjusts its operating point to a tight control of the output power level and supply current.

A single-concentric quad-core DAT is shown in Fig. 31.7.2. It consists of four differential cores that drive the four corners of the structure differentially. Thus, each primary slab is driven differentially creating a virtual ground in the middle of the slab where the power supply is applied. The RF power is then magnetically coupled to the secondary loop that consists of the secondaries of four 1:1 transformers in series. This allows the secondary voltages to add up in-phase to achieve the high voltage levels necessary for a watt level output into the load (roughly $36V_{pp}$ for +35dBm into a 50Ω load). The large voltage swing on the secondary loop does not pose a reliability issue since no transistor is connected electrically to the output to experience it.

In Fig. 31.7.2, the DC supply voltage is provided to the amplifier via the mid-point of the primary slab inductors (a virtual ground). Since this DC voltage appears directly at the drain of the drive transistors, it is limited by their breakdown voltage. A cascode topology structure can be used to increase the supply voltages that can be tolerated by the transistors. Although the cascode helps by allowing a larger voltage to appear on the drain of the top transistor without degrading the device performance, it is not sufficient for a power amplifier that must withstand a supply voltage of up to 5.5V (e.g., Li-ion battery on the charger) under large VSWR without any long-term performance degradation.

This problem can be solved by noticing that the mid-points of the slab inductors are at virtual grounds and can also serve as the ground connection of another DAT, concentric with the original one, thus forming the double-concentric DAT, as shown in double-concentric quad-core DAT example of Fig. 31.7.3. This arrangement allows for the same DC current to be shared by the inner and the outer DATs. This way each DAT experiences roughly half of the supply voltage while each contributes to the total output RF power coupled to the secondary loop. It is obvious that this procedure can be repeated multiple times if necessary.

The fully integrated quad-band CMOS PA is implemented in a standard 0.13µm CMOS process and runs off a nominal supply of 3.5V. It is housed in a 5mm×5mm×0.9mm MLF package. In the E-GSM band it produces a maximum RF power of +35dBm (3.2W) with a PAE of 51% that includes all the on-chip losses of the PA, the power control, and other supporting circuitry and package losses. It operates reliably with input power levels ranging from –2dBm to +8dBm. The HB power amplifier in the PCS band (1850MHz to 1910MHz) produces up to 33dBm (2W) of power at an overall efficiency of 45%.

The PA is fully compliant with the FCC and GSM requirements, has passed GSM/GPRS full-type-approval (FTA) certification for use in phones, and is in high volume production. The switching transient spectrum and the time masks are shown in Fig. 31.7.4. The power control accuracy and performance under supply voltage variations is shown in Fig. 31.7.5. Its transmit noise in the receive band (at 20MHz offset) varies between –102dBm to –84dBm for output power levels ranging from 0dBm to +35dBm, which meets the GSM requirements with a margin, as seen in Fig. 31.7.6.

The PA operates for any supply voltage between 2.9V and 5.5V, and can withstand a supply of up to 6V indefinitely under VSWR of greater than 15:1 for all phase angles with no oscillation, breakdown, or degradation. This has been demonstrated by more than 2,000 hours of failure free operation for hundreds of units at 87.5% duty-cycle under these conditions. The PA has also been tested for more than 1.5×10^6 device-hours (with ongoing reliability monitoring) without a single failure under nominal operation conditions. Its instantaneous supply breakdown voltage is greater than 9V. A die micrograph of the chip is shown in Fig. 31.7.7.

The presented PA proves the viability of CMOS technology for watt-level fully integrated power generation for wireless applications and serves as another step toward a single-chip cell-phone.

Acknowledgments:
We would like to thank M. Johnson, V. Boyapati, C. Huynh, J. Kim, F. Carr, F. Jarrar, A. Kral, A. Mellati, J. Mehta, S. Martin, H. Wu, T. Wisler, S. Mezouari, D. Kang, T. Trinh, K. Kong, J. Huynh, D. Qiao, D. Hartman, and M. Damgaard.

Reference:
[1] I. Aoki, S.D. Kee, D. Rutledge and A. Hajimiri, "A Fully 2.4-GHz, 2.2-W, 2-V Fully-Integrated CMOS Circular-Geometry Active-Transformer Power Amplifier," *Proc. IEEE CICC*, pp. 57-60, May 2001.

 978-1-4244-2011-7/08/$25.00

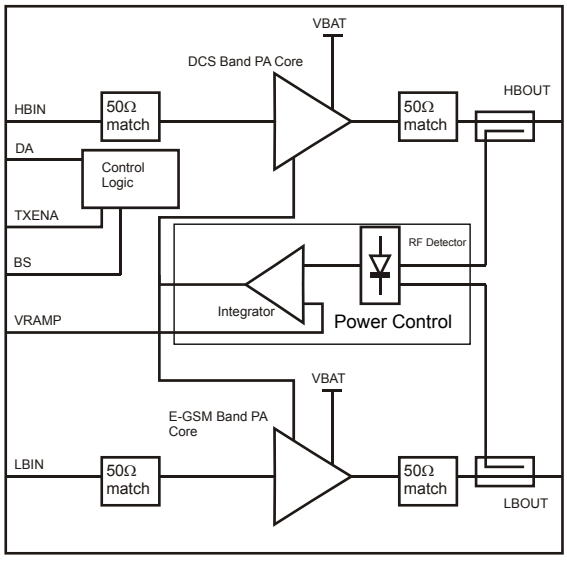

Figure 31.7.1: Functional block diagram of the fully integrated quad-band CMOS.

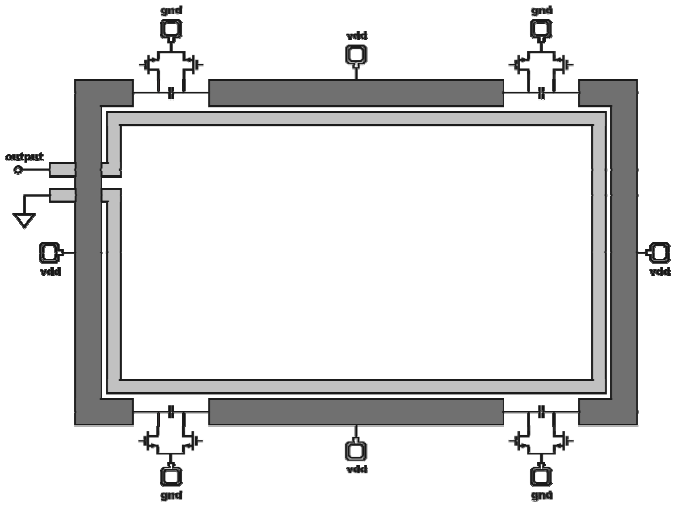

Figure 31.7.2: Single quad-core distributed active transformer [1].

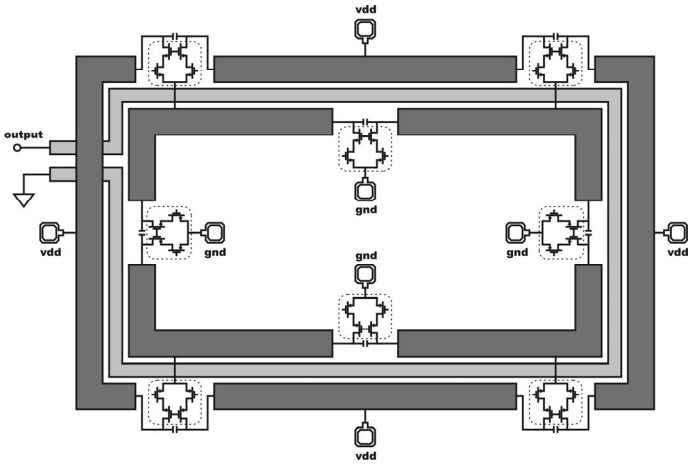

Figure 31.7.3: Double-concentric quad-core DAT with cascode drivers.

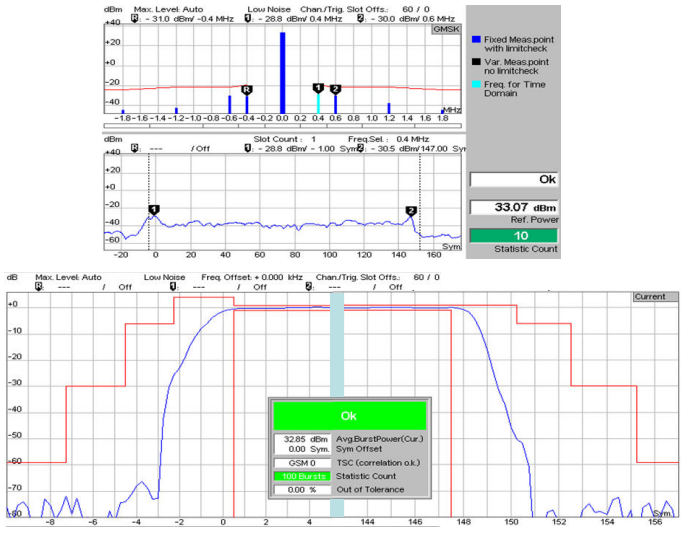

Figure 31.7.4: Switching transient and the time masks.

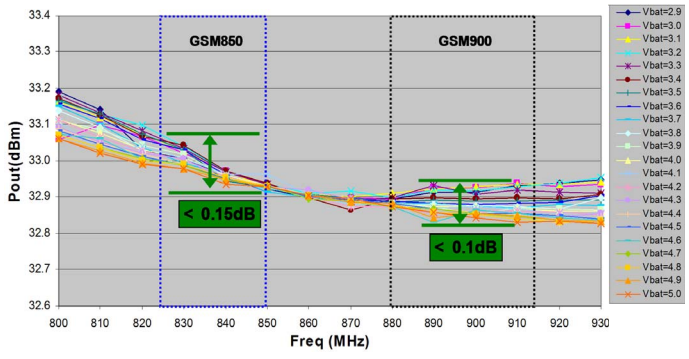

Figure 31.7.5: Power control accuracy and performance under supply voltage variations.

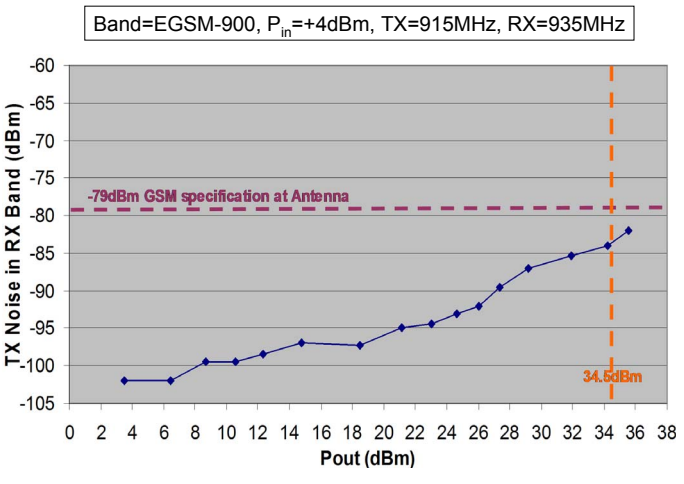

Figure 31.7.6: Transmit noise in the receive band (20MHz offset).

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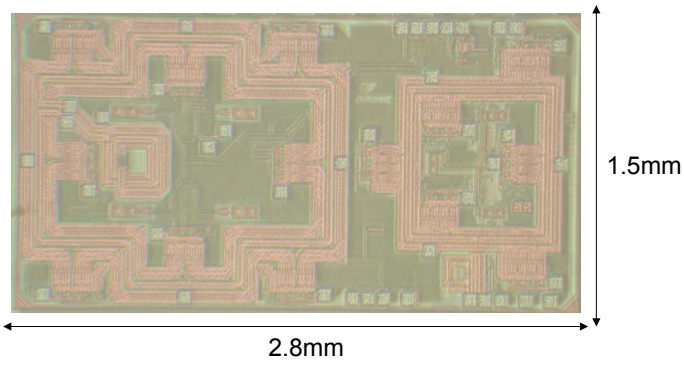

Figure 31.7.7: Die micrograph of the quad-band fully integrated CMOS PA.

 978-1-4244-2011-7/08/$25.00