A 30.5 dBm 48% PAE CMOS Class-E PA With Integrated Balun for RF Applications

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***Abstract*—Integration of the power amplifier together with signal processing in a transmitter is still missing in demanding RF commercial products. Issues preventing PA integration include LO pulling phenomena, thermal dissipation, and power efficiency. In this work we investigate high efficiency watt range Class-E PAs and integrated baluns. In particular, insights in the design of a fully differential cascode topology for high efficiency and reliable operation are provided and a narrowband lumped element balun, employing minimum number of integrated inductors for minimum power loss, is introduced. Two versions have been manufactured using a 0.13 μm CMOS technology. The first comprises the driver, and a differential PA connected to an external low-loss commercial balun. Experiments prove 31 dBm delivered output power, with 58% PAE and 67% drain efficiency, at 1.7 GHz. The second version adopts the same driver and PA and also integrates the balun. Experiments prove 30.5 dBm delivered output power, with 48% PAE and 55% drain efficiency, at 1.6 GHz.**

***Index Terms*—Baluns, class-E, CMOS power amplifiers, radio-frequency (RF) circuits, switching amplifiers, wireless communications.**

I. Introduction

WIRELESS connectivity in portable applications demands highly integrated transceivers to reduce costs and increase functionality. Systems on a chip (SOCs) for wireless local area networks (WLANs), global positioning systems (GPS) and personal area networks (Bluetooth) are available today in CMOS technology, after years of intense research [1]–[3]. Despite significant advances in integration level, more demanding applications, such as cell-phones, still rely on several off-chip components and functions. In particular, the Power Amplifier (PA), a key block of the RF transmitter, consuming the largest portion of DC power, and generating spurious and thermal interference, is off-chip and realized using compound semiconductor technologies. The path toward fully integrated transmitters in CMOS entails further investigation. The research is focused on: 1) techniques to alleviate coupling between PA and other analog circuits on the same die [4], and PA-induced heating [5]; 2) solutions to achieve high power PAs, with long and reliable life-time, and showing in the meantime, efficiencies comparable with those achievable using alternative and more expensive technologies.

This work is focused on the design of reliable, high efficiency 1-Watt range CMOS PAs. A cascode switched mode Class-E topology, very promising for integrated solutions, is investigated to maximize PA efficiency without compromising device reliability [6]–[10]. Integrated circuits usually adopt differential topologies mainly to get rid of spurious injection from other blocks, by virtue of the intrinsically improved common mode rejection. In the framework of power amplifiers, there is also another advantage coming from a differential choice. In fact, when targeted output powers are extremely high, a differential topology contributes a significant 3 dB power increase, for the same supply voltage, load resistance and efficiency [11]. Since the components driven by the PA are usually single-ended, an efficient integrated balun is a key component. In this work, we introduce an *LC* lumped balun [12] performing on-chip signal recombination and impedance matching simultaneously, and embedding also the Class-E PA output network. In addition, spiral inductors are reduced to a minimum number in order to reduce silicon area and, foremost, maximize power efficiency.

Two versions have been manufactured using a 0.13 μm CMOS technology, which also provides thick 0.28 μm devices we used in the design. The first comprises the driver and a differential PA connected to an external low-loss commercial balun. Experiments prove 31 dBm delivered output power, with 58% PAE and 67% drain efficiency. The second version adopts the same driver and PA and also integrates the balun. Experiments prove 30.5 dBm delivered output power, with 48% PAE and 55% drain efficiency.

The paper is organized as follows: Section II discusses our proposed strategy for maximum efficiency in reliable Watt range PAs. Section III introduces the design of two PA versions: the first comprising driver, differential PA and external balun, the second including driver, differential PA and the newly introduced balun. Section IV presents measurements and Section V draws the conclusions.

II. Strategy for High Efficiency High Power Fully Integrated Class-E PAs

Fig. 1 shows the schematic of a cascode single-ended Class-E PA, where parasitic resistors of inductors, responsible for efficiency degradation are highlighted. Nominal components values are set by operating frequency (f_0), output power (P_{OUT}), supply voltage (V_{DD}), and output network quality factor $(Q_{\mathrm{OUT}} = \omega_0 L_2/R_L)$ [10]. As known from the pioneering work of its inventor [13], Class-E topology exploits

Manuscript received December 21, 2007; revised March 17, 2008. Published July 23, 2008 (projected).

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Digital Object Identifier 10.1109/JSSC.2008.925605

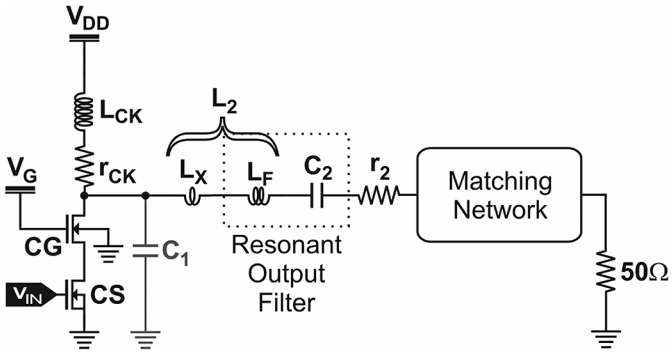

Fig. 1. Schematic of a cascode Class-E PA with an *LC* match, highlighting parasitic resistance of inductors.

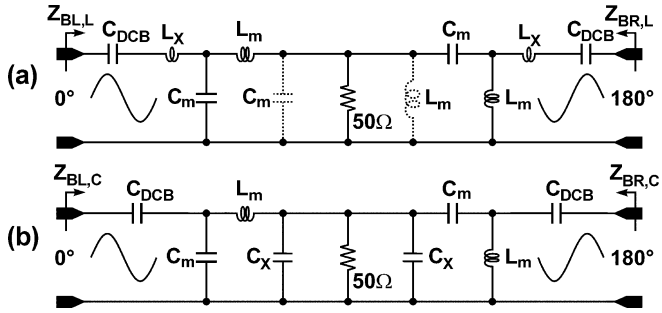

Fig. 2. Schematic of the CLC-LCL balun along with the Class-E output network (L_2 and C_2).

an ideally lossless charge/discharge mechanism onto a capacitance, C_1, shunt connected to the load through a selective filter, to shape the switch voltage for zero drop together with zero slope at turn on, thus minimizing device power losses caused by component spreading. The role played by the series inductor L_2 is twofold: a fraction L_X shapes the shunt capacitor voltage V_C, while $L_{\rm F}$, together with C_2 forms a series resonator, tuned at the operating frequency, to filter out higher harmonics of the load current. The matching network down-transforms the 50 Ω antenna resistance to a lower value (R_L), necessary to deliver the required amount of power. For a specified output power level, its value scales down as the square of supply voltage. The main drawback of the Class-E amplifier is the high peak value reached by the drain voltage, more than three times the adopted supply.

For this reason, to assure reliable operation, a supply lower than the nominal value is usually selected in a conventional common source Class-E topology, leading to extremely low R_L values when delivering high output powers. The effect is a reduction of efficiency, primarily due to ohmic losses of the matching network that rise up quickly reducing R_L.

On the contrary, in a cascode implementation each device sustains roughly half the voltage drop, thus allowing doubling the supply voltage, while still assuring reliable operation. The power loss penalty due to the on-resistance of the CG transistor is negligible since a large aspect ratio device can be selected to absorb the large shunt capacitor C_1 in the device drain capacitance. The ultimate efficiency of a cascode topology is higher than a CS solution, provided the parasitic capacitance between CG and CS devices is resonated out, as discussed in [8].

The Class-E, as originally introduced by Sokal, assumes a broadband matching network to down-transform antenna resistance, and relies on the series $L_{\rm F}$–C_2 network in order to suppress output harmonics. To down-transform antenna resistance, we adopted an integrated narrowband resonant match, which has also a filtering action. Its quality factor increases with reducing R_L [15], i.e., when delivering high power levels. A minimum inductance L_X corresponding to excess reactance required for proper Class-E operation should be left, whereas C_2 becomes a DC blocking capacitor.

Exploiting a CMOS PA, for future integration with the signal section of the transmitter, suggests a fully differential implementation to limit spurious emissions. A further aspect of this work is the analysis and design of a balun solution integrated on the same silicon substrate. This approach is very desirable in order to reduce external components and transceiver costs, but efficiency penalties due to low Q of on-chip inductors need careful inspection of balun related power losses. In order to address this issue our approach is twofold: 1) signal recombination and resistance down-transformation functions are lumped. A simple LC–CL network is adopted allowing minimum number of inductors; 2) inductor quality factor is maximized at the expense of self-resonance frequency, by designing ad hoc spirals whose track width is enlarged to diminish their series resistance, i.e., their losses.

The balun concept is based on the lumped implementation of a $\lambda/4$ and a $3\lambda/4$ branches into a single network [12]. As shown in Fig. 2(a), the two branches are realized by $C_{\rm m}$–$L_{\rm m}$–$C_{\rm m}$ and $L_{\rm m}$–$C_{\rm m}-L_{\rm m}$ that can be considered as separately connected to a 100 Ω load, i.e., two times the one of a standard 50 Ω antenna. When ideal $L_{\rm m}$ and $C_{\rm m}$ passives are considered, $L_{\rm m}$–$C_{\rm m}$–$L_{\rm m}$ and $C_{\rm m}$–$L_{\rm m}$–$C_{\rm m}$ provide $+90°$ and $-90°$ phase displacements at the fundamental frequency, respectively. Therefore, a differential signal at the two input branches results to be exactly in-phase on the two shunt 100 Ω loads, guaranteeing complete isolation between PA differential branches. $L_{\rm m}$ and $C_{\rm m}$ in parallel to the 50 Ω load (drawn in dotted line) resonate out at the fundamental frequency, hence they can be eliminated saving chip area. The characteristic impedance and resonance frequency of $\lambda/4$ and $3\lambda/4$ networks are given by [16]

$$\begin{cases} Z_0 = \sqrt{\frac{L_{\rm M}}{C_{\rm M}}} = \sqrt{100 R_L} \\ f_0 = \frac{1}{2\pi\sqrt{C_{\rm M} L_{\rm M}}}. \end{cases} \tag{1}$$

R_L is the matched resistance, while $L_{\rm M} = Z_0/\omega_0$ and $C_{\rm M} = 1/Z_0\omega_0$.

Reducing the number of inductors is crucial to improve efficiency. For this reason, displacement inductor L_X is synthesized by means of capacitor C_X, as shown in Fig. 2(b), in parallel to the resistive load exploiting impedance transformation properties of $\lambda/4$ and $3\lambda/4$ networks:

$$j\omega L_X = \frac{Z_0^2}{\frac{1}{j\omega C_X}} \Rightarrow C_X = \frac{L_X}{Z_0^2} \tag{2}$$

The elimination of L_X is also beneficial for area saving. The proposed balun combines the power from the two differential branches and increases the impedance at second and higher

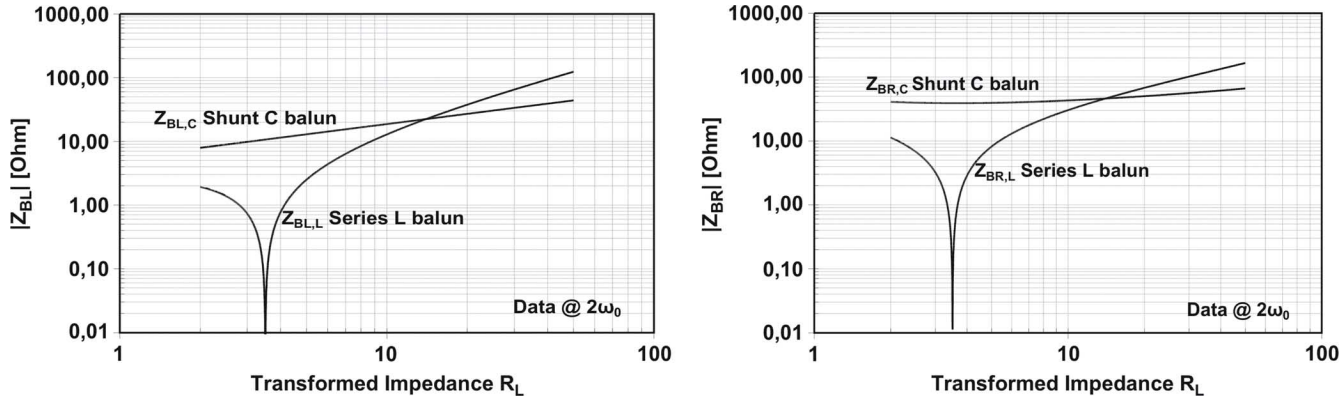

Fig. 3. Impedances at $2\omega_0$ calculated considering a series-L and a shunt-C balun solution.

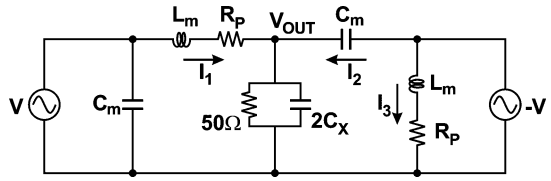

Fig. 4. Balun schematic for loss analysis.

harmonics. This is essential to assure proper Class-E PA operations [13], preventing excessive harmonic dispersion due to the high harmonic content of the drain voltage [17], [18]. As shown in Fig. 3, magnitudes of impedances realized by the two balun branches at second harmonic, $|Z_{\mathrm{BL},C}|$ and $|Z_{\mathrm{BR},C}|$, are relatively high for a wide range of down-transformed resistances R_L, i.e., for a wide range of delivered output powers. Thus, the introduced solution allows getting rid of the displacement inductor. This is actually not the case when the displacement inductor L_X is in series; see Fig. 2(a). In this case, Fig. 3 shows that balun impedances, i.e., $|Z_{\mathrm{BL},C}|$ and $|Z_{\mathrm{BR},C}|$ are always much lower with a deep minimum for $R_L \approx 3.5\ \Omega$, i.e., the typical value for ~30 dBm power delivery. Notice that these impedances are much lower than the down-transformed impedance, resulting in a dominant second order content in the output current.

A key aspect toward fully integrated CMOS PAs, i.e., the balun efficiency, can be analyzed assuming integrated inductors are the only source of losses, due to their much lower quality factor with respect to integrated capacitors [19], [20]. In Fig. 4, $R_P = Z_0/Q_L$ is the parasitic resistor and Q_L is the inductor quality factor. Circuit inspection results in the following equation:

$$\begin{cases} I_1 = \frac{V - V_{\mathrm{OUT}}}{jZ_0 + R_P} \\ I_2 = \frac{V + V_{\mathrm{OUT}}}{jZ_0} \\ I_3 = \frac{-V}{jZ_0 + R_P} \\ V_{\mathrm{OUT}} = (I_1 + I_2)\left(50 \left\| \frac{1}{j\omega 2C_X}\right.\right) \end{cases} \tag{3}$$

Once I_1, I_2, I_3, and V_{OUT} have been determined, the power loss due to two parasitic resistors can be computed. With some mathematical manipulation, we derived the following simplified

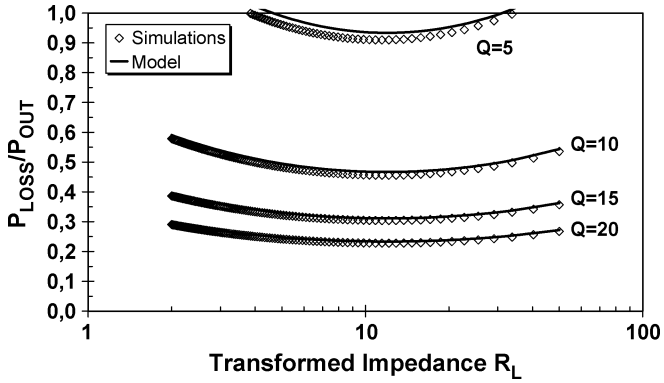

Fig. 5. Proposed balun related $P_{\mathrm{LOSS}}/P_{\mathrm{OUT}}$ ratio versus transformed impedance R_L.

expression for the balun power losses normalized to the output power:

$$\left.\frac{P_{\mathrm{LOSS}}}{P_{\mathrm{OUT}}}\right|_{\mathrm{BALUN}} = \frac{\frac{1}{2}R_P\left(|I_1|^2 + |I_3|^2\right)}{\frac{1}{2}R_L|V_{\mathrm{OUT}}|^2} \approx \frac{5 + 1.78\sqrt{R_L} + 0.417R_L}{\sqrt{R_L}Q_L}. \tag{4}$$

Equation (4) is plotted in Fig. 5 versus R_L together with values simulated by means of SPECTRE RF, showing a very good agreement. As intuitive, the inductor Q is crucial not to degrade PA efficiency. As an example, if we assume $R_L = 3.75\ \Omega$ and $Q_L \approx 10$ for on-chip inductors, the normalized power loss is ~0.52. To gain insight, we can compare this result with the power loss of a partially integrated PA, i.e., employing an external balun, a matching network realized by means of high quality bondwire inductors ($Q_L = 20$) and off-chip capacitors [21]. In this case, the power loss due to the matching network only [8] is given by

$$\left.\frac{P_{\mathrm{LOSS}}}{P_{\mathrm{OUT}}}\right|_{\mathrm{MATCH}} = \frac{Q_{\mathrm{OUT}}}{Q_L}. \tag{5}$$

Assuming $Q_{\mathrm{OUT}} = 5$, $P_{\mathrm{LOSS}}/P_{\mathrm{OUT}}|_{\mathrm{MATCH}} \sim 0.25$. Moreover, the insertion loss (IL) of the external balun has to be considered for a fair comparison with the fully integrated solution.

External balun IL leads to further efficiency degradation, given by the following:

$$\left.\frac{P_{\mathrm{LOSS}}}{P_{\mathrm{OUT}}}\right|_{\mathrm{EXT,BALUN}} = 10^{\mathrm{IL}/10} - 1. \tag{6}$$

The latter largely varies and trades off with component size and cost.

Assuming a design for a ~30 dBm power delivery, and choosing a standard SMD balun (IL ≈ 1 dB) the normalized power loss is also in the order of 0.3. The total normalized power loss is thus 0.55, indicating that the PA and the proposed balun lead roughly to the same degradation in power efficiency.

III. Design of the Differential and Integrated Balun Class-E PAs

A differential cascode Class-E PA and an integrated balun have been designed in a 0.13 μm CMOS technology from STMicroelectronics, targeting 31 dBm delivered output power at 1.7 GHz operating frequency. Two different chips have been realized for characterization. The first comprises the differential power amplifier and a locked oscillator driver. Output matching and power combiner are realized with bondwires inductors, off-chip passives and balun. In the second test chip a fully integrated lumped-element balun, introduced in the former section, follows the driver and the differential power amplifier stage.

The circuit schematic of the first test chip is shown in Fig. 6. Due to the differential topology, each branch is sized to deliver 28 dBm. 0.28-μm-thick oxide MOSFET devices are used to allow higher supply voltage, $V_{\mathrm{DD}} = 2.5$ V. The common-gate (CG) device in the power stage completely absorbs the shunt capacitance to minimize its on state dissipation. Choice of the common source (CS) width involves a trade-off between on-state resistance and power dissipated by the driver stage [8]. A width of 7000 μm has been selected as optimum compromise. A 1 nH spiral is inserted to resonate out the parasitic capacitor between CG and CS MOSFETs in each differential branch according to [8].

Both DC feed and output network inductors are implemented with bondwires. The matching network is implemented as a *LC* low-pass filter made of a fraction of the two output bondwire inductances (1.8 nH) and off chip SMD capacitors. To deliver the target power with 2.5 V supply, a matched load resistance (R_L) of 3.75 Ω is required. The quality factor of the matching network is high enough (~3.5 for each differential branch) to limit higher harmonics in the output current. The series resonator can be therefore eliminated. Thus, the output 40 pF acts as DC blocking capacitor.

A differential on-chip inductor resonates out the gate capacitance of each CS devices of the power stage. The resonator quality factor is set to 5 to accommodate the same bandwidth as the output stage. Voltage swing to drive the common source device is a compromise between required source power and dissipation on CS on-resistance: the larger the driving voltage, the lower the on-resistance but the larger the source power. Selecting an optimum voltage swing of 2 V would require an input power of 22 dBm, leading to a very limited power gain of 9 dB

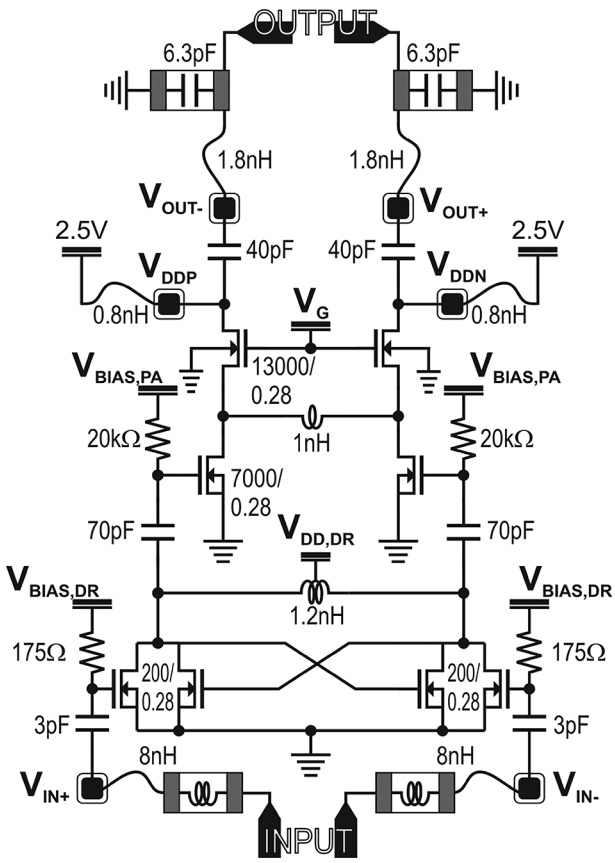

Fig. 6. Schematic of the differential power stage, including a locked oscillator driver and a cascode Class-E amplifier, realized in a 0.13 μm CMOS technology.

only. A driver stage has therefore been included. Because the Class-E PA operates as a switching-mode amplifier, the driver stage is not required to be linear and, for maximum gain, can be implemented as a locked oscillator. In order to guarantee a signal swing very close to the driver supply, set to 2 V, the total width of the switching devices in the driver stage is set to 400 μm. Choice of the relative size of cross-coupled and input devices in Fig. 6 trades locking bandwidth for power gain: the larger the input transistors, the larger the locking bandwidth of the oscillator but the higher the input capacitance to be driven, penalizing power gain. Equal devices of 200 μm have been selected providing an input-output power gain of 25 dB and a locking bandwidth >400 MHz. Off-chip SMD inductors are added to properly match input impedance.

The complete schematic of the second test chip is shown in Fig. 7. Size of active devices has been modified in order to absorb the balun input parasitic capacitance due to the wide metal lines. DC-feed inductors are still realized by means of bondwires. Note that excess inductor L_X is now implemented by means of capacitor C_X, as discussed in the previous section. The series resonator is again omitted in order to optimize efficiency.

The balun capacitors are implemented as high quality factor/high linearity MIM capacitors. Inductors have been customized for two main reasons: 1) their quality factor must be maximized for minimum power loss; 2) the large current flow mandates the use of wide metal lines to prevent electro-migration. Inductors are realized shunting together the three topmost metal

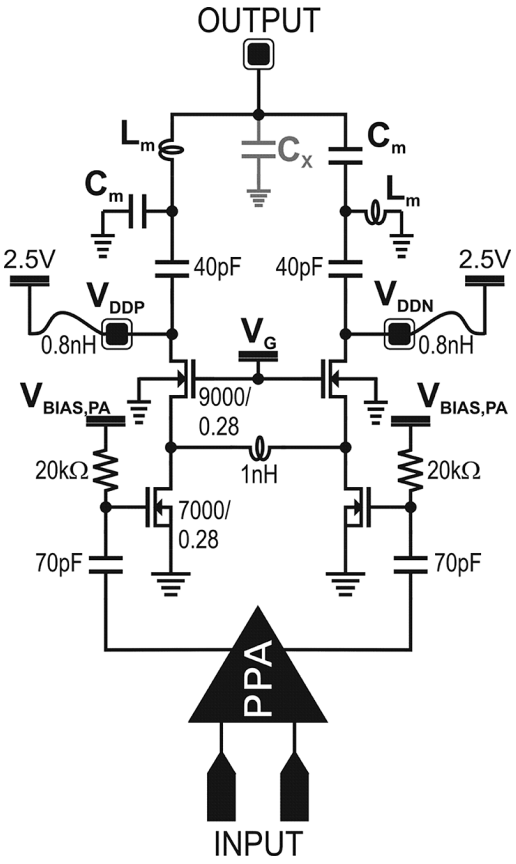

Fig. 7. Simplified schematic of the proposed single-ended output PA with on-chip embedded balun. C_X is realized by means of output metal parasitic capacitor.

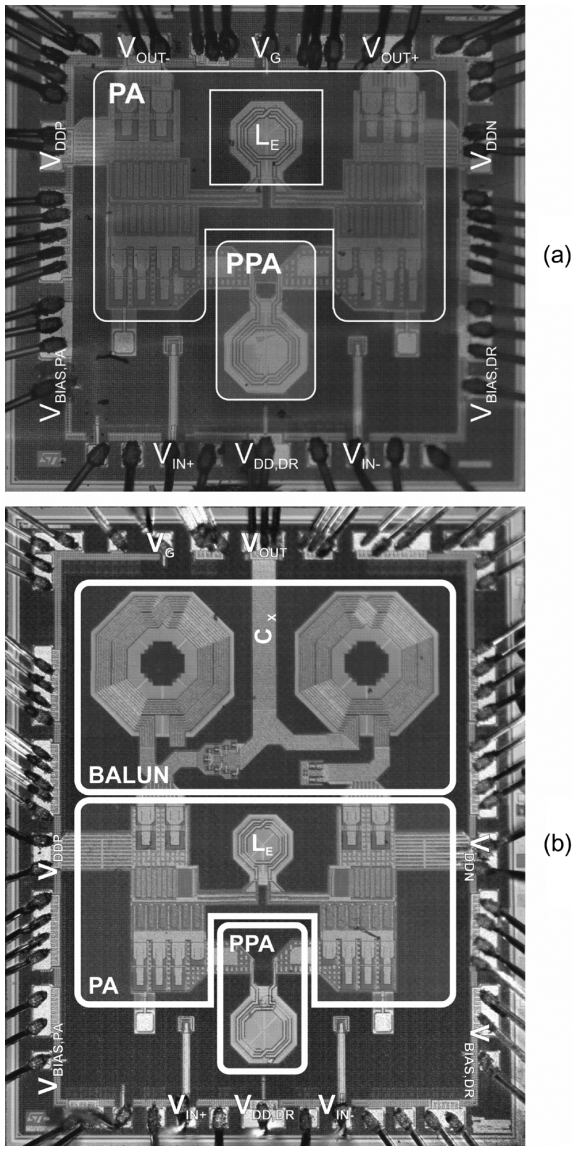

Fig. 8. Chip photomicrograph of (a) differential output realized PA, and (b) single-ended output PA with on-chip embedded balun.

layers. Metal width has been set equal to 60 μm to comply with electromigration requirements and the performance verified by means of exhaustive electro-magnetic simulation. The achieved quality factor at 1.7 GHz is ~ 10 while self resonance frequency is 4 GHz. A larger metal width would reduce further the self-resonance frequency without significant increase in the quality factor.

Particular care has been devoted to the layout of the two test chip in order to reduce parasitic resistors. Switching CS MOSFETs have been designed so that every transistor elementary cell can be grounded on both sides. This allows optimizing source grounding, i.e., minimizing switch on-state resistance. On the other hand, cascode MOSFETs are designed to minimize their gate resistance. V_G filters are purposely localized near every gate to provide optimum signal grounding. Particular care has been taken to provide thermal dissipation via both the grounding plane and the outputs. Wide area custom ground pads allow successful heat dissipation through ground bondwires.

IV. Measured Results

The chip photomicrograph of the two test chips is shown in Fig. 8. The die area, including bonding pads, of the power amplifier with off-chip balun is 2.7 mm^2. The on-chip lumped-element balun embedded in the second test chip occupies additional 2 mm^2. The wafer thickness is relatively large: 500 μm. For maximum thermal dissipation, dies were glued on a metal plane with conductive adhesive. Several ground bondings were also adopted to favour heat sink and, at the same time, assure low grounding resistance.

The first test chip has been characterized with an external hybrid balun whose power loss has been de-embedded from measured data. Fig. 9(a) shows output power $(P_{\rm OUT})$, drain efficiency (η) and power-added efficiency (PAE) versus supply voltage of the power stage $(V_{\rm DD})$ at 1.7 GHz operating frequency. At maximum supply voltage, measured output power is 31 dBm. Drain efficiency and PAE are maximum when $P_{\rm OUT} = 31$ dBm, reaching 67% and 58%, respectively. Input signal is set to 6 dBm in all measurements, so maximum power gain equals 25 dB. Fig. 9(b) shows output power and η versus operating frequency. Maximum $P_{\rm OUT}$ and efficiency are achieved at 1.7 GHz. $P_{\rm OUT}$ is however larger than 28 dBm, 3 dB lower than peak value, over a broad frequency range: from 1.5 GHz to 1.9 GHz. At band edges drain efficiency remains higher than 45%.

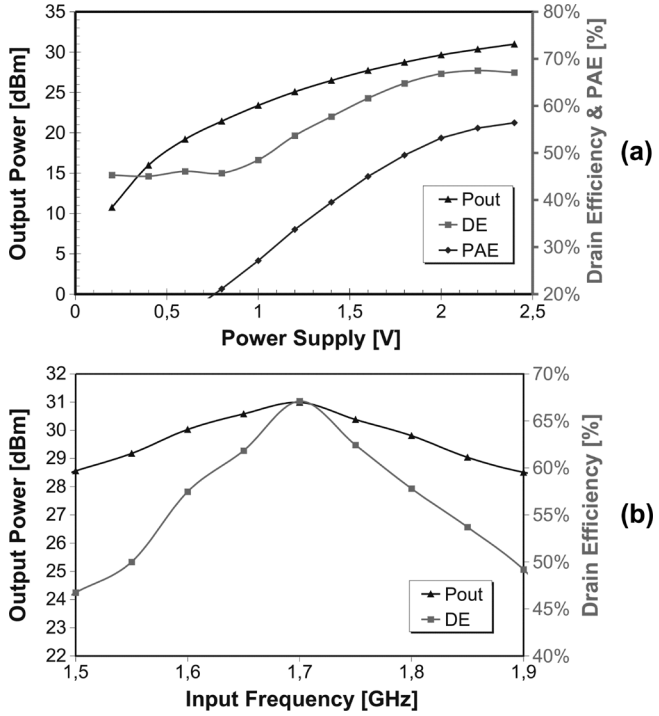

Fig. 9. Measurements performed on differential output PA. (a) Output power, drain efficiency and power added efficiency versus voltage supply. (b) Output power and drain efficiency versus input frequency.

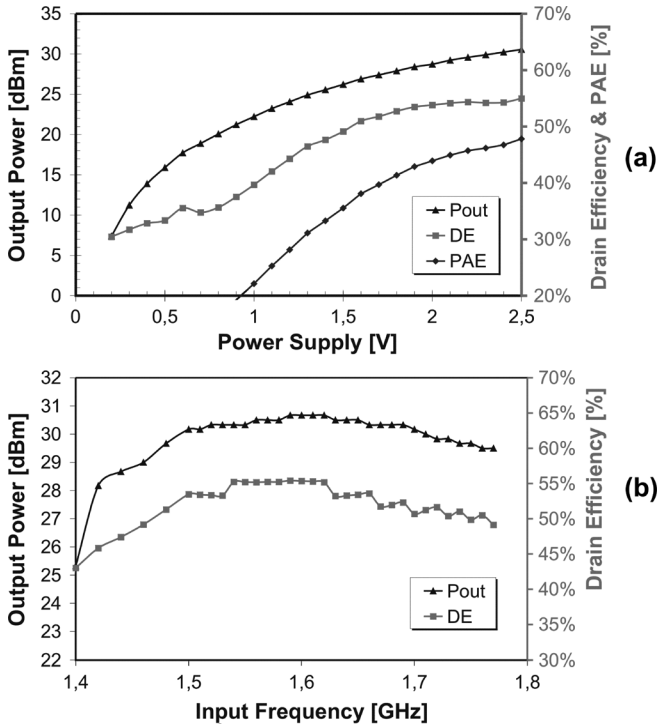

Fig. 10. Measurements performed on single-ended output PA with on-chip embedded balun. (a) Output power, drain efficiency and power added efficiency versus voltage supply. (b) Output power and drain efficiency versus input frequency.

The same measurements have been carried out on the power amplifier with on-chip balun and are shown in Fig. 9. In this case we do not make use of any off-chip component. Best performance is achieved at 1.6 GHz frequency. This is very likely due to a slight underestimation of parasitic capacitors in the routing of the on-chip balun. $P_{\rm OUT}$ and efficiencies versus $V_{\rm DD}$ are shown in Fig. 10(a). Maximum $P_{\rm OUT}$ is 30.5 dBm with a power gain of 24 dB. At maximum power, drain efficiency and PAE are 55% and 48%, respectively. Results confirm a normalized power loss from the on-chip balun of 52%, in good agreement with the theoretical value estimated from (4) assuming, for the inductors, a quality factor of $\sim$10. Fig. 10(b) shows output power and drain efficiency versus frequency. $P_{\rm OUT}$ is larger than 28 dBm over a bandwidth ranging from 1.42 to 1.74 GHz. At band edges drain efficiency is larger than 45%.

Fig. 11(a) and (b) displays the output spectrum for the two power amplifiers at maximum output power, from which the harmonic content can be evaluated. Second harmonic suppression for the power amplifier with an off-chip broadband balun is 52 dB. This is because with a fully differential circuit topology, even harmonics are in-phase and ideally rejected by a broadband balun. Measurements prove sufficient balancing between the two branches of the power amplifier. A rejection of 52 dB indicates phase and amplitude unbalances below 2° and 0.5 dB, respectively [11].

By contrast, second harmonic rejection is limited to 24.5 dB in the fully integrated solution. In fact, while the two branches of the lumped balun down-transform the same impedance (with opposite phase) at ω_0, they implement different impedances at higher harmonics, as shown in Fig. 3 for the second harmonic.

In order to test the PA reliability, we performed voltage accelerated stresses described in [9]. We supplied the PA at large

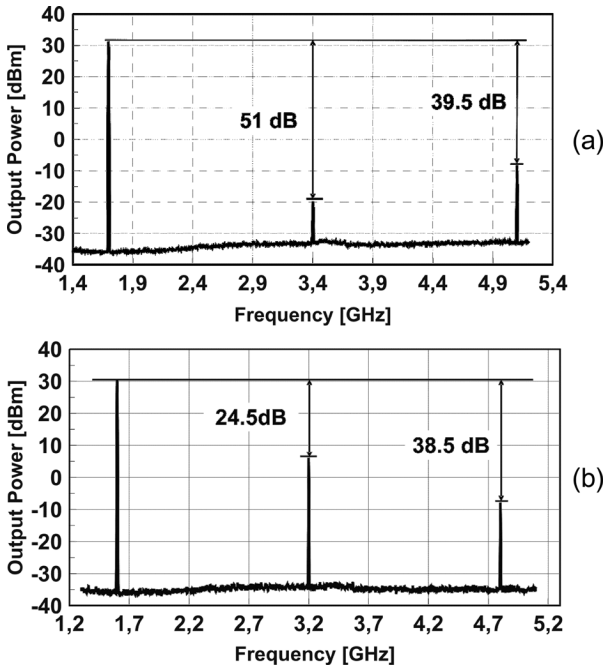

Fig. 11. Measured output spectrum for (a) differential output PA and (b) single-ended output PA with on-chip embedded balun.

$V_{\rm DD}$, extrapolating the lifetime at the maximum supply voltage $V_{\rm DD} = 2.5$ V, which largely exceeds 1000 hours.

Finally, to compare the performance of the fabricated prototypes against state-of-the-art solid-state power amplifiers we use the figure of merit (FoM) introduced by ITRS [22], which

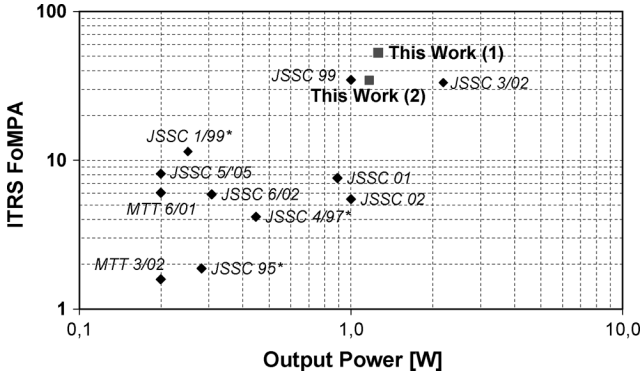

Fig. 12. Literature comparison through ITRS $\mathrm{FoM_{PA}}$. This work proposed PAs are highlighted with squares, with diamonds literature proposed CMOS PAs. $*$ indicates GaAs.

normalizes major performance, i.e., P_{OUT}, PAE, power gain (G) and the square of operating frequency (f_0^2):

$$\mathrm{FoM_{PA}} = P_{\mathrm{OUT}} \cdot \mathrm{PAE} \cdot G \cdot f_0^2 \tag{7}$$

Fig. 12 reports calculated $\mathrm{FoM_{PA}}$ versus maximum output power level for the two prototypes as well as published results. Both the proposed PAs show high performances even comparable with GaAs prototypes.

V. Conclusion

In this paper, we have presented insights in the design of high efficiency and reliable fully integrated CMOS Class-E PAs as the outcome of our recent work in this area. In particular, a cascode topology allows reliable and high efficient solutions, provided the power dissipated by the common gate device is reduced to a minimum, selecting a large area–low resistance common gate device which absorbs the output capacitance, and resonating out its source parasitic. A locked oscillator driver allows maximizing power gain with a minimal impact on PAE.

A fully integrated balun, based on the lumped implementation of $\lambda/4$ and $3\lambda/4$ branches into a single network, and customized for the Class-E power amplifiers, has been also presented. It employs minimum number of integrated inductors for minimum power loss and silicon area. Ultimate power efficiency is comparable with realizations based on off-chip power recombination.

Measured results show the proposed realization compares favorably against state of the art, even including implementations in GaAs. We think CMOS technology is mature for the realization of high power amplifiers with performance adequate for wireless applications. This work did not focus on coexistence of high power PAs with other analog blocks of the transmitter, which is also a key aspect for full integration.

Acknowledgment

The authors would like to thank T. Arnaud (STMicroelectronics) for technology access.

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