CDMA2000 PCS/Cell SiGe HBT Load Insensitive Power Amplifiers

Giuseppe Berretta, Domenico Cristaudo and Salvatore Scaccianoce

STMicroelectronics, Stradale Primosole 50, 95121, Catania, Italy

Abstract — A novel power amplifier design technique has been proposed that uses load pull measurements in order to optimize linearity and efficiency. Two SiGe HBT MMIC power amplifiers suitable for Cell and PCS applications have been realized in a 0.25 μm BiCMOS technology. Thanks to the design technique implemented, CDMA2000-1X specifications can be met under output load mismatch up to 4:1 VSWR, thus allowing the removal of the external isolator in the transmitter chain.

Index Terms — ACPR, CDMA2000, HBT, linear, power amplifier, RF, SiGe, VSWR.

I. INTRODUCTION

The evolution for new generation of mobile handset platforms requires the integration of transceivers and power amplifiers (PA) into System in Package (SiP) or even into System on Chip (SoC) solutions, in order to reduce cost and size of the mobile. This trend leads to a technology convergence between the transceiver and the PA. BiCMOS technologies offer a viable candidate to face this evolution, since PA can be designed by using high frequency bipolar transistors while transceivers can exploit full integration capability by using CMOS devices.

Following the same integration and scaling prospective, an effort has been done to get rid of the costly and bulky isolator, placed between the PA and the antenna. Due to the isolator absence the PA will not be loaded by 50 Ω anymore. In fact, depending on the environmental condition around the antenna, due to body effect or metallic surfaces, the PA will encounter severe load mismatch.

The hybrid phase shift keying (HPSK), a modulation technique with non-constant envelope, has been adopted for CDMA2000. Therefore, PAs with high linearity are required in the transmitter system. The linear behavior of the power amplifier has to be kept even under load mismatch conditions.

This work presents two SiGe HBT PAs for CDMA2000 Cell and PCS band respectively, which are able to withstand to a severe load mismatch with respect to the linear output power. Therefore the reported PAs can work properly without the use of an isolator.

Power amplifiers have been integrated by using STMicroelectronics 0.25µm BiCMOS technology (BiCMOS7RF).

The Cell (PCS) band PA is capable of delivering up to 28.5 (28) dBm output power with an adjacent channel power ratio (ACPR1) below -44 (-44) dBc, an alternate channel power ratio ACPR2 below -57 (-55) dBc, a power added efficiency (PAE) of 30 (30) % and a gain of 28 (28) dB. Thanks to the new design method, the Cell (PCS) band PA delivers up to 27.5 (26) dBm linear output power while complying with the threshold ACPR1 of -44 (-44) dBc and ACPR2 of -56 (-52) dBc, under 4:1 VSWR load mismatch.

II. DESIGN CRITERIA UNDER LOAD MISMATCH

Typically, performances of a PA (PAE, gain and ACPR) are optimized by tuning the output matching in order to transform the antenna impedance (e.g. 50 Ω) into the PA optimum load impedance. With reference to Fig. 1, the impedance looking toward the output matching network from the HBT collector is represented by Z_{LOAD} , while the antenna impedance is Z_{ANT} .

In mobile applications, a change in the boundary conditions around the antenna results into a change in the output VSWR. This affects dramatically PA performances. As depicted in Fig. 1, VSWR fluctuations can be emulated by using a tuner.

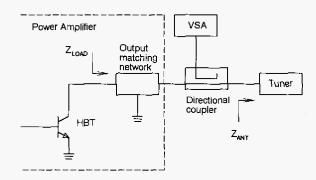


Fig. 1. Test configuration for a PA and antenna with variable VSWR.

As shown in Fig. 2, the antenna impedance Z_{ANT} is transformed by the output matching network into an impedance $Z_{LOAD} = Z_{OPT}$. A constant VSWR circle in the Smith Chart (e.g. the solid circle in Fig. 2 is a 4:1 VSWR circle referenced to 50 Ω) is mapped in the same way into another circle (dashed circle (a) in Fig. 2). Moreover, as it has been demonstrated in [3], the centre Γ_C and ray R of the mapped circle (a) are:

$$\Gamma_{\rm C} = \Gamma_{\rm OPT} \cdot \frac{1 - \rho^2}{1 - \rho^2 \cdot |\Gamma_{\rm OPT}|^2} \tag{1}$$

$$R = \rho \cdot \frac{1 - \left| \Gamma_{OPT} \right|^2}{1 - \rho^2 \cdot \left| \Gamma_{OPT} \right|^2}$$
 (2)

where, ρ is the VSWR and Γ_{OPT} is the reflection coefficient referenced to 50 Ω . It is worth noting that this circle (Γ_C and R) is independent on the chosen lossless network but depends only on the mapping between the Z_{ANT} and Z_{OPT} and on the VSWR = ρ .

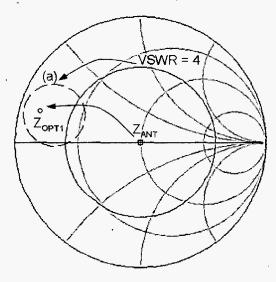


Fig. 2. Mapping of a constant VSWR circle (4:1).

If Z_{ANT} is quite constant (e.g. thanks to an isolator between the PA and the antenna) then the output matching network can be tuned (e.g. Z_{OPTI} as shown in Fig. 2) in order to achieve the maximum PAE with the needed ACPR at the required output power.

On the other hand, if $Z_{\rm ANT}$ can change due to mismatch conditions at the antenna, $Z_{\rm LOAD}$ will vary as mentioned before assuming all the values contained on or within the circle (a) in Fig. 2. Under these conditions, some of these mapped impedances lead to unsatisfactory ACPR performance, (either the adjacent channel power ratio, ACPR1, or the alternate channel power ratio, ACPR2).

In order to overcome this problem, the load-pull method has to take into account PAE and ACPR contours [4], in order to make the PA capable of driving an antenna impedance contained within a boundary defined by a 4.4 dB return loss circle referenced to a 50 Ω (4:1 VSWR). As shown in Fig. 3, the optimum impedance $Z_{\text{LOAD}} = Z_{\text{OPTI}}$, chosen with the conventional method, determines a mapped circle (long dashed circle (a)) not completely contained within the ACPR1<-44dBc (dash-dot curve) and ACPR2<-56dBc (dot curve) contours. Instead, the new optimum load impedance $Z_{\text{LOAD}} = Z_{\text{OPT2}}$ is selected, so that the relevant mapped circle lies completely within both ACPR contours. However, from a PAE point of view, Z_{OPT2} represents a sub-optimum compared to Z_{OPT1} .

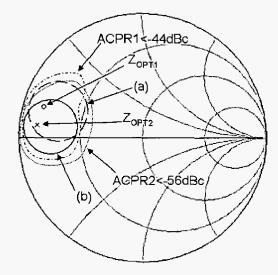


Fig. 3. ACPR contours.

IV. CIRCUIT DESIGN

Each PA has been integrated into two different dice for Cell and PCS band. A 0.25 μ m SiGe BiCMOS process technology (BiCMOS7RF) by STMicroelectronics has been selected to integrate the PA. This technology requires 31 mask steps and features shallow and deep oxide trench isolation, high resistivity substrate (50 Ω ·cm), five metal layers (thick top metal layer, 2.5 um), poly resistors, MIM capacitors (5 fF/ μ m²), and on chip inductors with patterned ground shield and quality factor in excess of 12 at 2 GHz. A high-voltage HBT with BV_{CEO} of 6.5 V and 30 GHz f_T is used for the PA.

A simplified schematic of the three gain stages (T1-T3) PCS band amplifier is reported in Fig. 4. Due to the lower frequency, a two stages PA has been designed for the Cell amplifier.

Input and inter-stage matching networks are integrated

on chip. Bond-wire inductance and a MIM capacitor have been used as matching network between the first and second stage, while two capacitors, bond-wire and an on-chip inductor have been used between the second and third stage. The input matching network is also implemented by the input capacitor, an on-chip inductor and two bond-wire inductances at the emitter and the base of the first stage. The output matching network has been designed by using the bond-wire inductance $L_{\rm W}$ and a partially distributed network realized on FR4 substrate.

The bias network has been implemented as explained in [1] and [2]. It includes linearization functionality, a shut-down and quiescent current regulation capability (V_{SD} and V_{CTRL} in Fig. 4, respectively).

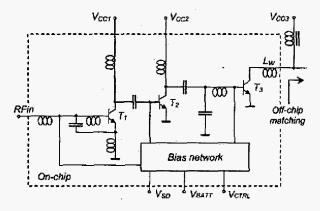


Fig. 4 Simplified schematic of the PCS band PA.

V. EXPERIMENTAL RESULTS

Die photographs of the PAs are shown in Fig. 5 and Fig. 6. The die size is $1.37\,\mathrm{mm}\times1.36\,\mathrm{mm}$ for both versions. Each die has been assembled in a standard $4\,\mathrm{mm}\times4\,\mathrm{mm}$ QFN 16-lead plastic package and mounted on a 400- μ m-thick FR4 substrate. The PAs work with a 3.4 V supply voltage and the operating frequency is set to 835 MHz (for the Cell band) and 1880 MHz (for the PCS band).

Performances of each PA have been measured by using both single-tone and modulated input signals. The modulated signal is a reverse link HPSK IS-2000 signal with a 1% CCDF Peak-to-Average-Ratio (PAR) of 4.2 dB.

Cell (PCS) PA performances under CW single-tone excitation in terms of output power, gain and PAE are shown in Fig. 7 (Fig. 10). A 28 (28) dB small-signal gain and a 34 (32) dBm saturated output power along with a 47 (43) % PAE have been achieved at room temperature.

Cell (PCS) PA performances under CDMA2000 excitation with 50 Ω antenna impedance are shown in Fig.

8 (Fig. 11),

A linear output power of 28.5 (28) dBm with a ACPR1 of -44 (-44) dBc, a ACPR2 of 57 (-55) dBc and a PAE of 30 (30) % is delivered to the load.

Cell (PCS) PA performances under CDMA2000 excitation with 4:1 VSWR antenna mismatch at an output power of 27.5 (26) dBm have been reported in Fig. 9 (Fig. 12).

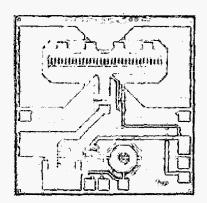


Fig. 5. Cell band PA die photograph.

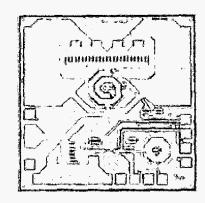


Fig. 6. PCS band PA die photograph.

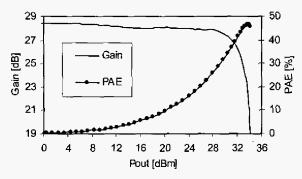


Fig. 7. Cell band PA single-tone performance (50 Ω).

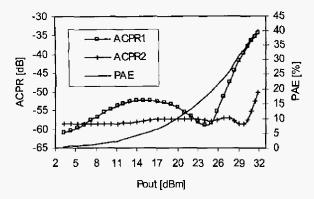


Fig. 8. Cell band PA ACPR performance (50 Ω).

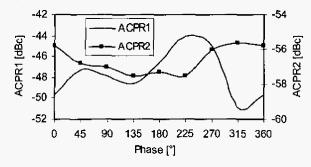


Fig. 9. Cell band PA ACPR under 4:1 VSWR load mismatch, all phase angles at 27.5 dBm output power.

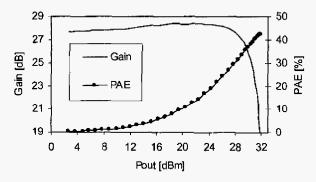


Fig. 10. PCS band PA single-tone performance (50 Ω).

VI. CONCLUSION

Two MMIC PAs (Cell and PCS band) have been integrated using a medium cost SiGe technology. They include an optimized bias network providing linearity enhancement, shut-down and quiescent current regulation functions.

With a CDMA2000 input signal, the Cell (PCS) band PA delivers an output power of 28.5 (28) dBm with a 30 (30) % PAE while complying with standard linearity requirements.

By an improved use of the load-pull method both PAs

are able to deliver a linear output power of 27.5 (26) dBm under 4:1 VSWR load mismatch. Hence the isolator usually interposed between the PA and the antenna can be removed in the transmitter chain.

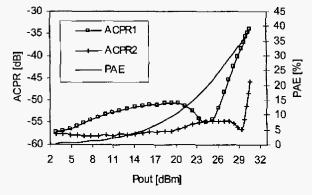


Fig. 11. PCS band PA ACPR performance (50 Ω).

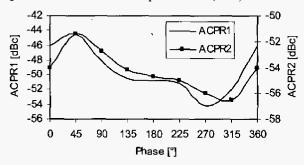


Fig. 12. PCS band PA ACPR under 4:1 VSWR load mismatch, all phase angles at 26 dBm output power.

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REFERENCES

- [1] J. H. Kim, Y. S. Noh, and C. S. Park, "A low quiescent current 3.3 V operation linear MMIC power amplifier for 5 GHz WLAN applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.2, pp. 867-870, June 2003.
- [2] A. Scuderi, D. Cristaudo, F. Carrara, and G. Palmisano, "A high performance silicon bipolar monolithic RF linear power amplifier for W-LAN IEEE 802.11g applications" in IEEE RFIC Symp. Dig., pp. 79-82, June 2004.
- [3] G. Gonzalez, Microwave Transistor Amplifiers Analysis and Design, Prentice Hall, 1997.
- [4] K. Ishida, H. Ikeda, H. Kosugi, M. Nishijima and T. Uwano, "A high efficiency and low distortion GaAs power MMIC design in the wide load impedance range by extended use of load-pull method", in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.2, pp. 775-778, June 1999.