A 40nm CMOS Single-Ended Switch-Capacitor Harmonic-Rejection Power Amplifier for ZigBee Applications

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***Abstract* — This paper describes a single-ended switch-capacitor harmonic-rejection power amplifier to operate in the 915 MHz ISM band for ZigBee applications. A multipath feed-forward harmonic-rejection technique is employed to suppress the 2nd/3rd/4th harmonics of the switch-capacitor power amplifier (PA) by 48/17/24 dB, respectively. The measured PA peak drain efficiency is 43% at a peak output power of 8.9dBm with the harmonic-rejection enabled. This PA was implemented in a 40nm TSMC CMOS process with an active area of 180µm×700µm.**

***Index Terms*—Switched capacitor circuits, Power amplifiers, CMOS, Harmonic distortion, and ZigBee.**

I. Introduction

Devices utilizing the Wireless Personal Area Network (WPAN) continue to proliferate with the advent of low-power radio applications including wearable electronics for health monitoring, new sensing features and components for industrial control. Implementation of these transceivers as a single-chip CMOS solution continues to be attractive from the perspective of low-cost, potentially very low power consumption and exceptionally small form factors. ZigBee has evolved as a popular WPAN standard to address numerous low-power applications.

ZigBee transceivers utilize constant-envelope BPSK/OQPSK modulation, thus allowing switch-mode topologies to implement small form-factor and high efficiency PAs. However, the non-linear nature of a switch-based PA will generate significant unwanted harmonic components. The fact that virtually all 915MHz ZigBee PAs are implemented as a single-ended device further exacerbates unwanted spurious components with a 2nd Harmonic falling in the crowded 1.8 GHz spectrum (DCS 1800). In addition, the 3rd and 4th order harmonics can potentially interfere with the International Mobile Telecommunication (IMT-E) and LTE bands.

PA output harmonic suppression has traditionally been addressed with discrete off-chip filters or notch circuitry acting as a "harmonic trap." Attempts at integrating a PA harmonic-suppression function has been demonstrated through the use of a polyphase multipath method [1] and conduction angle calibration [2][3]. However, these techniques have limitations with respect to targeting specific harmonics and are done at the expense of high power consumption and large silicon area.

This work presents a single-ended Switch-Capacitor (SC) Harmonic-Rejection Power Amplifier (HRPA) that achieves state-of-the-art performance with respect to cancellation of the 2nd, 3rd and 4th order harmonics. The PA harmonics may be categorized as arising from two sources: 1) the harmonics generated prior to the PA input, and 2) the harmonics generated by the PA driver and output stages (i.e. self-generated harmonics). The proposed SC-HRPA utilizes a multipath feed-forward cancellation technique to mitigate both the input and self-generated 2nd order harmonics, while simultaneously providing significant cancellation of the 3rd and 4th harmonics. Moreover, this approach is compact and only requires a single off-chip inductor to absorb the bond-wire inductance without the need of an on-chip area-consuming transformer or inductor.

Section II provides an overview of the underlying system concepts surrounding this HRPA technique. The circuit implementation details of the SC-HRPA are presented in Section III. Measurements of the fabricated 40nm CMOS prototype are provided in Section IV, while a conclusion, with a comparison to prior art, is given in Section V.

II. HRPA Overview

A. HRPA Concept

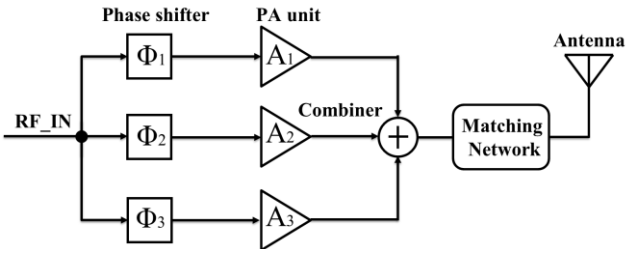

Fig. 1. Conceptual block diagram of the HRPA.

This HRPA (Fig.1) employs a cancellation technique similar to a harmonic-rejection mixer originally proposed in [4] and consists of three driver paths each of which contain a digital phase shifter, a PA unit, an output power combiner and matching network. Accordingly, the input RF signal propagates through multiple paths, each with a specific phase shift and gain; by properly choosing the phase and gain ratios among the pathways, specific undesired harmonics of the combined signal path can be

cancelled at the PA output, while the desired RF carrier is passed with little attenuation.

B. 2nd/3rd/4th Harmonic Cancellation

This HRPA (Fig.1) applies a phase shift before the PA driver to rotate the phase of the carrier, f_0 (fundamental carrier frequency) and each of the associated harmonics. If the phase of f_0 is shifted by Φ, then the 2nd harmonic component at the PA output will shift by 2Φ, independent of whether or not the harmonic is self-generated in the PA or was present at the input. Likewise, the 3rd harmonic will be shifted by 3Φ, the 4th by 4Φ, etc. This HRPA can be modelled with a phase shift of Φ_1, Φ_2, and Φ_3, and signal path gains of A_1, A_2 and A_3, respectively (Fig. 1). HD_2, HD_3 and HD_4 at the PA output, may be described by:

$$HD_2 = A_1 e^{-2j\Phi_1} + A_2 e^{-2j\Phi_2} + A_3 e^{-2j\Phi_3} \quad (1)$$

$$HD_3 = A_1 e^{-3j\Phi_1} + A_2 e^{-3j\Phi_2} + A_3 e^{-3j\Phi_3} \quad (2)$$

$$HD_4 = A_1 e^{-4j\Phi_1} + A_2 e^{-4j\Phi_2} + A_3 e^{-4j\Phi_3} \quad (3)$$

From Eq.1-3, setting HD_2=HD_3=HD_4=0 will result in too many equations for the number of unknown variables. Thus, a single solution using only three paths cannot be obtained to *completely* cancel all three harmonics, simultaneously. This can only be done with additional driver paths. In general, an N path system will at least cancel N-1 harmonics at the same time. However, for N=3, complete cancellation of one or two of the three harmonics may be achieved with partial cancellation of the remaining two or

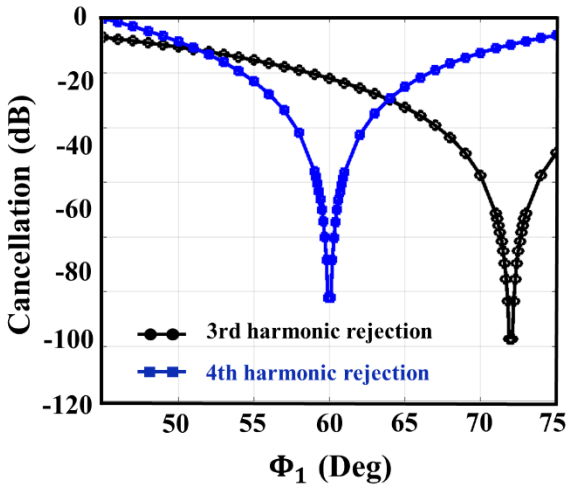

Fig. 2. 3rd/4th order harmonic cancellation with HD_2 set to zero.

one harmonics, respectively. For example, HD_2 may ideally be completely cancelled with partial cancellation of HD_3 and HD_4. Normalizing $A_1 = A_3 = 1$, $\Phi_3 = -\Phi_1$, and $\Phi_2 = 0$ and assuming no mismatch, from Eq.1, A_2 can be solved as a function of Φ_1 by setting HD_2=0; plots may be generated for HD_3 and HD_4 as a function of Φ_1 (Fig. 2). Although there is a window where the cancellation is greater than 20dB, the HD_3 and HD_4 suppression is maximized when Φ_1=64° which maps to an A_2=1.23.

C. HRPA Configuration for 2nd Order Harmonic Cancellation

The proposed HRPA can be configured to cancel both the 2nd order harmonics presented at the input and those that are self-generated. The relative phase-shifts and gain of each path is 64°/0°/-64°, and 1/1.23/1, respectively.

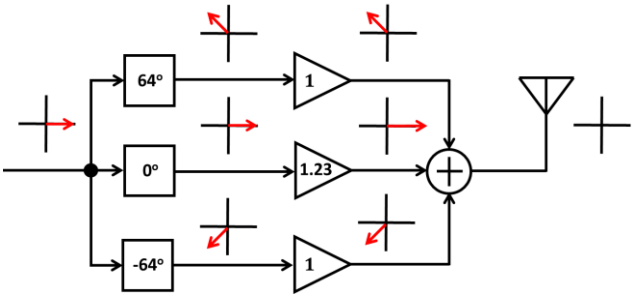

Fig. 3. Cancellation of input 2nd order harmonics.

The 2nd order harmonic presented at the PA input is shown as a red phasor with 0° phase shift (Fig. 3). After passing through the phase shifters, the 2nd order rotates such that it completes the cancellation at the output.

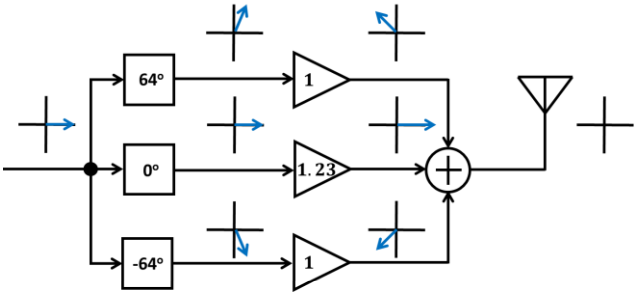

Fig. 4. HRPA configured for 2nd order harmonic cancellation of PA self-generated harmonics.

Each PA driver has its own non-linearity that self-generates 2nd order harmonics. Applying the same phasor argument (Fig. 4) with the blue arrow representing f_0, the phasor summation of the self-generated 2nd order, again sums to zero at the power combiner output. Accordingly, the 3-path HRPA can achieve cancellation of both the PA input and self-generated 2nd order harmonics.

D. Mutual Loading Issue

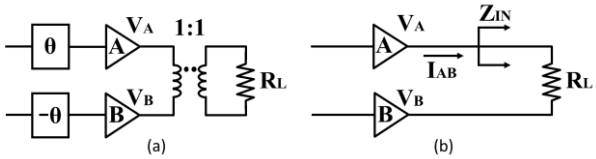

Fig. 5. (a) HRPA transformer output power combiner, (b) simplified model of power combiner loading on the drivers.

A key challenge of the HRPA design relates to the method of combining the power of each signal path in a way that minimizes degradation in the PA efficiency. This challenge is better understood when taking into consideration of the fact that each driver stage turns on and off with different phases, thus changing the impedance presented to the combiner. The effect of a modulated, time-dependent output impedance can be described with a large-signal model using a typical transformer output power combiner. Assuming the top and bottom PA unit (Fig.5) generate output signals with the same frequency and magnitude, but different phases (θ and -θ), the following describes the voltage at V_A and V_B [5]:

$$V_A = V_m \sin(\omega_0 t + \theta) \quad (4)$$

$$V_B = V_m \sin(\omega_0 t - \theta) \quad (5)$$

The input impedance, Z_{in}, of driver A, where $Z_{in} = V_A/I_{AB}$, can be described by:

$$Z_{in} = \frac{R_L}{2} - j\cot(\theta)\frac{R_L}{2} \quad (6)$$

The input impedance has a relatively large imaginary component introduced by the mutual loading (Eq. 6). For example, if θ=45° the equivalent imaginary impedance looks like a large capacitor, thus requiring a large area-consuming inductor to achieve resonance. The method of power combining for this HRPA significantly lowers this undesired capacitance, and thus the required inductance.

E. Switched-Capacitor Power Amplifier (SCPA)

The SCPA topology benefits from CMOS scaling and has a better linearity and efficiency performance compared to other PA approaches [6]. In an SCPA, each Class-D PA unit generates an output signal that toggles between V_{DD} and ground. The capacitors realize the output matching network and fulfil the role as a power combiner.

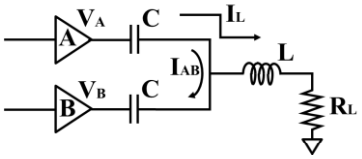

Fig. 6. Model describing effect of a time-varying driver load.

These capacitors have the added advantage of improving the isolation between the driver stages, thus minimizing the effect of a time-varying load impedance.

Using the prior analytical method (Eq. 4-5) to analyze the mutual loading (Fig. 6), the input impedance for PA unit A becomes:

$$Z_{in} = \frac{1}{A - jB} \quad (7)$$

$$A = \frac{R_L}{(\omega L')^2 + {R_L}^2} + \omega C \sin(\theta)\cos(\theta) \quad (8)$$

$$B = \frac{\omega L'}{(\omega L')^2 + {R_L}^2} + \omega C \cos^2(\theta) \quad (9)$$

The imaginary component (i.e. B), at the frequency of interest, is dominated by the value of Capacitor, C. Thus, a smaller C will significantly reduce the effective capacitance introduced by the driver time-varying output impedance. This is intuitively pleasing as generally, smaller capacitors present a larger series impedance.

III. Chip Implementation

The HRPA chip integrates the phase-shifters, pre-drivers and PA output drivers. The phase shifter is embedded with the PA pre-driver stage to minimize the power consumption and area. Both the coarse and fine phase tuning are realized based on RC inverter delay while coarse tuning is achieved by adjusting R, and fine tuning is by adjusting C. The design of the PA output driver is a Class-D output stage as

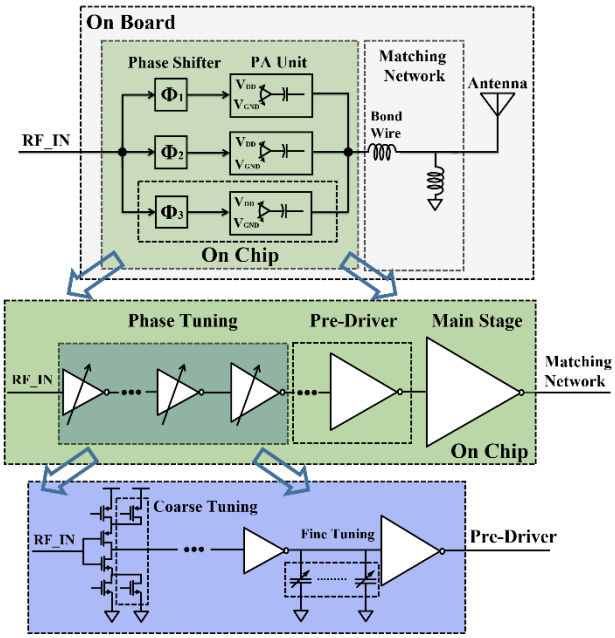

Fig. 7. HRPA schematic.

in [6]. A single discrete inductor is used with a bond-wire to form an L-matching network (Fig. 7).

The chip was fabricated in TSMC 40nm CMOS process. The PA active area is 178μm×700μm (Fig. 8).

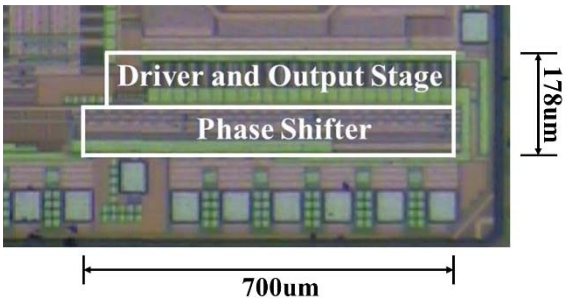

Fig. 8. Die photo of HRPA.

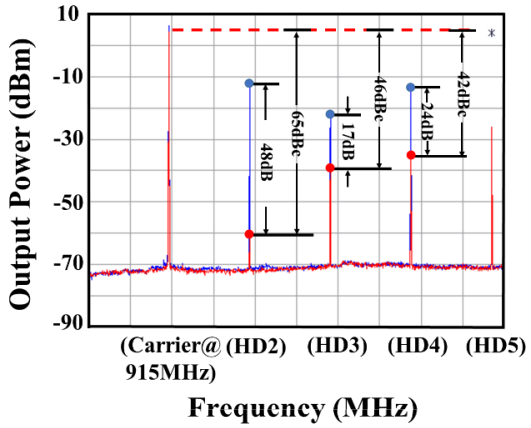

Fig. 9. Spectrum of HRPA.

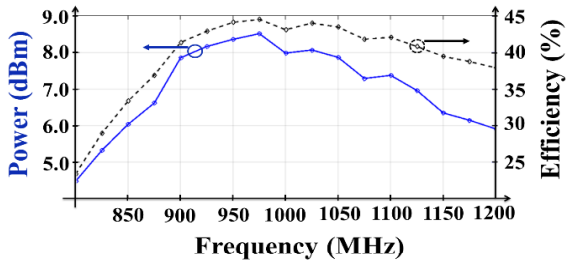

Fig. 10. HRPA efficiency and power output vs. frequency.

IV. Measurement Results

A measured output spectrum for the HRPA is in Fig. 9 with a single tone RF input signal. The measurement was taken with the HRPA function disabled (blue curve with equal phase shift in each of the three paths), and with the harmonic-rejection function enabled (red trace). This PA achieves a measured harmonic rejection of -48/-17/-24 dB on the 2nd/3rd/4th order harmonics, respectively. The ZigBee standard demands that all harmonic components be lower than -40dBm. The proposed HRPA is able to sufficiently cancel the 2nd order harmonic. The HRPA delivers a maximum +8.9dBm with a peak drain efficiency 43% (Fig. 10) in the 906-924MHz ZigBee band. The measured modulation spectrum (Fig.11) meets the requirements of the ZigBee spectral modulation mask [8].

V. Conclusion

A feed-forward, switch-capacitor HRPA was fabricated in 40nm TSMC CMOS process with the ability to cancel the 2nd/3rd/4th order harmonics by 48dB/17dB/24dB, respectively. This compact solution requires a single off-chip inductor with all other circuitry integrated on-chip. This solution is well suited for ZigBee applications due to its low power consumption and small form factor.

Acknowledgments

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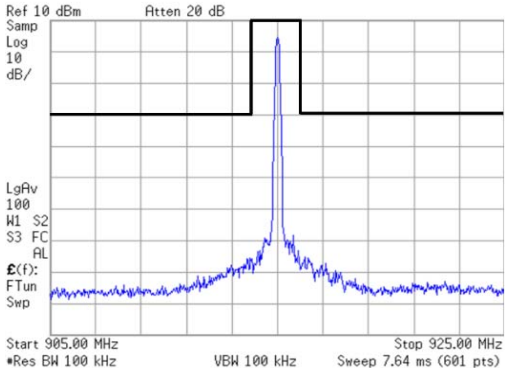

Fig. 11. In-band measured output spectrum with 802.15.4 mask (RBW = 100 kHz).

TABLE I
Comparison Table

Harmonic Rejection	T. Sano' 2015 ISSCC	A. Ba' 2014 RFIC	F.Jonas' 2010 ESSCIRC[7]	This Work
Architecture	Conduction Angle Calibration	Conduction Angle Calibration	Harmonic Reduction	HR SCPA
Technology/VDC	40nm/1.1V	40nm/1.0V	90nm/1.2V	40nm/1.1V
Output Power (dBm)	0	1.2	5.3	8.9
Frequency(GHz)	2.4	2.4	0.9	0.9
Drain Efficiency (%)	-NA-	39	62	43
Num. of Off-chip Components	No	3	3	1
HD2 (dBc)	-52.3	-50	-46.3	-65
HD3 (dBc)	-48	<-50	-45.3	-46
HD4 (dBc)	-NA-	<-50	<-55.3	-42

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