Design of 24 GHz SiGe HBT Balanced Power Amplifier for System-on-a-Chip Ultra-Wideband Applications

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Abstract — Design of a balanced, three-stage, common-emitter, 24 GHz SiGe HBT power amplifier for ultra-wideband applications is described. The unique features of the amplifier are very flat gain response in the frequency band of interest and sharp gain drop outside of the band, which are important considerations for a system-on-a-chip UWB application. The amplifier has 18 dB nominal gain in the frequency band of 24 GHz ± 2 GHz. The gain variation is ± 0.5 dB in the same frequency band. Saturated output power is 12 dBm at 24 GHz.

Index Terms — SiGe, ultra-wideband (UWB), MMIC, power amplifiers, balanced amplifiers, automotive.

I. Introduction

Ultra-wideband (UWB) systems have been gaining interest in recent years. One of the application areas of UWB systems is the high-resolution radar (HRR) for automotive applications at 24 GHz [1–4]. There is a UWB allocation specifically for automotive safety applications between 22–29GHz. Due to its relatively long range and immunity to weather conditions, a radar system can be an alternative to existing range sensors used for parking aid or blind-spot detection. However, especially for automotive applications, the cost-effective production of such UWB systems is necessary in order to compete with existing technologies (e.g., acoustic sensors). SiGe HBT technology can provide a unique solution to this problem because it enables high-density RF circuits thus reducing the overall cost [1, 2, 5].

In this paper, we will present the design of a class-A power amplifier for UWB systems at 24 GHz using SiGe HBT technology. The novel features of the amplifier presented in this paper are a very flat (± 0.5 dB) gain response in the frequency bandwidth of 4 GHz and sharp gain drop outside the bandwidth (–20 dB gain at 10 GHz), which are important for UWB systems. Note that it is important to have sufficiently low gain at lower frequencies to prevent any undesired oscillations. Another reason to have a narrow-band amplification is the FCC compliance that limits the amount of radiation to other frequencies. Satisfying both the gain-flatness and the high out-of-band rejection simultaneously is not trivial, and requires properly designed interstage matching networks. By employing a highpass interstage matching networks and using bandpass filters at the input and output of the amplifier, we were able to obtain a gain response similar to a bandpass filter, which is quite advantageous. To characterize the matching networks accurately, full-wave electromagnetic analyses of the complete RF signal path have been employed using *em* by Sonnet Software.

The measured center frequency and 3-dB bandwidth of the amplifier are 24 GHz and 6 GHz, respectively. The amplifier has three common-emitter (CE) stages matched using interstage matching circuits. It has an overall nominal gain of 18 dB at the center of the frequency band. Output saturated power of the amplifier is 12 dBm at 24 GHz. The dc current consumption is 110 mA at 5 V supply voltage (including bias circuits). The main reason for the relatively high current requirement is the necessity of keeping high collector current-density for HBTs to maintain the high transit frequency.

II. Design of the Balanced Amplifier

The two main criteria in designing the balanced amplifier were to provide sufficient gain (~ 20 dB) and output power (> 10 dBm saturated) in the frequency band of interest. To achieve these goals, it was decided to use three cascaded common-emitter (CE) Class-A balanced amplifier stages [6]. All matching networks were implemented using lumped elements to reduce the required chip real estate. Simplified schematic and microphotograph of the implemented amplifier are shown in Fig. 1.

Since the SiGe substrate employed is quite conductive ($\sigma = 0.1$ to 5 S/m) compared to a semi-insulating GaAs-substrate, transmission line dielectric losses are a paramount consideration. Besides, the width of a standard 50 Ohm microstrip transmission line is prohibitively large on the 180 μm thick SiGe substrate used. To address these issues, the amplifier has been designed using a balanced configuration since balanced transmission line offers relatively low insertion loss on the Si substrate. This is due to fact that most of the fields are concentrated around the vicinity of the lines, rather than penetrating deep into the conductive substrate. Other advantages of using a balanced configuration are the cancellation of even-order harmonics, high linearity, and reduced common-mode noise.

A. Selection of the Transistor

The important factors that must be considered in the selection of the transistors are the transit frequency, maximum collector current, maximum collector voltage, geometry of the transistor, and location of input and output impedances on the Smith chart at a given bias level.

The Atmel SiGe2RF process that we have employed offers SIC (selectively implanted collector) and non-SIC types of RF transistors with 50 and 80 GHz transit frequencies, respectively. The collector-emitter breakdown voltages

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(BV_{CEO}) of the SIC and non-SIC transistors are 2.5 Volts and 4.0 Volts, respectively. It must be noted that the BV_{CEO} is measured under the condition where the base terminal is open circuited. However, in most RF applications, the base sees impedance levels in the order of 50 to 200 Ohms. This enables the reverse base current (due to junction avalanche) exit the base terminal, pushing the attainable dynamic RF voltage swing be higher than the breakdown voltage [7, 8] (typically $1.5 \times BV_{CEO}$ to $2 \times BV_{CEO}$). It is therefore possible to increase the peak RF voltage on SiGe HBTs more than the open-circuit DC breakdown voltage thus increasing the output power.

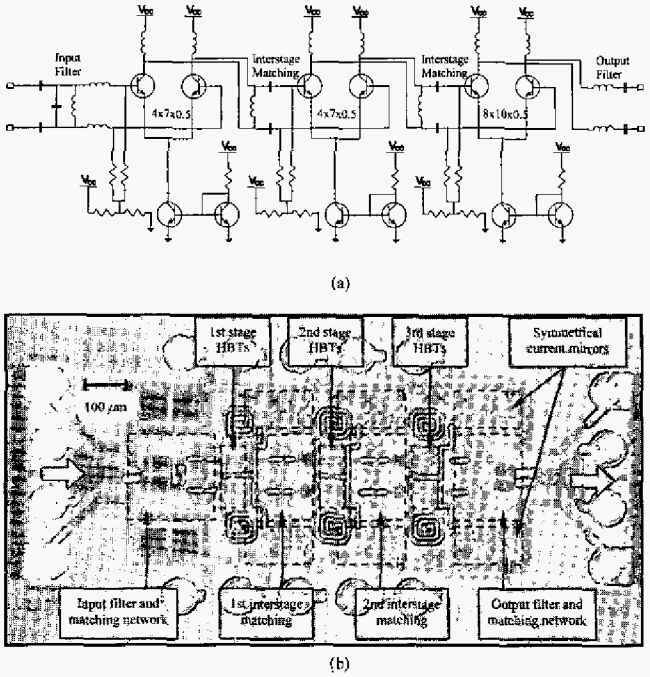

Figure 1 Simplified schematic and microphotograph of the SiGe HBT balanced amplifier. The numbers next to the transistors show the total number of transistors and transistor area. Highpass interstage matching networks and input/output filters provide the desired bandpass filter response.

An important consideration in SiGe HBTs is that the transit frequency is a function of collector current density. Therefore, if the frequency of operation is close to the transit frequency, then the collector current must be increased to the level where maximum transit frequency is obtained to get enough gain. Hence, there is a tradeoff between the power efficiency and maximum available gain from each stage in that case.

Another important point is the locations of the input and output impedances of the transistors on the Smith Chart. The transistor area should be chosen in a such a way that minimum amount of matching is required. For instance, one should adjust the area of the first stage HBTs so that the input impedance of the balanced transistors is in the capacitive region but close to the 50 ohm resistance circle. This will require only a serial inductor to match the input impedance simplifying the matching network.

Based on these requirements, we have selected a SiGe HBT with effective emitter dimensions of 0.5×10 μm in CBEB (Collector-Base-Emitter-Base) configuration. This transistor has a maximum transit frequency approximately of 80 GHz at a collector current density of 1.3 mA/μm^2, which gives approximately 6.5 mA collector current for the selected transistor. However, due to electromigration issues on the metallizations, collector current is limited to 5 mA in the design without any significant reduction in the gain.

B. Design of the Matching Networks

Interstage matching networks are important to harvest maximum available power from each stage. This is especially crucial at microwave frequencies where the transistor parasitics are comparable with impedance levels. Therefore, it was decided to design interstage matching networks between each stage instead of cascading many stages of amplifiers to compensate gain loss due to mismatch. This also provided a bandpass-filter-type gain response, which is advantageous as explained before. Perhaps one of the disadvantages of using interstage matching networks is the chip area required by matching components. Another one is the requirement of accurate modeling. The latter one is crucial in terms of the circuit performance and detailed further below.

The important point in the design process of matching circuits is the use of full-wave electromagnetic simulations. The full-wave simulation tool employed in this work is the *em* by Sonnet Software. Full-wave simulations ensure accurate modeling of the passive elements by taking into account all parasitics and coupling effects. To achieve this goal, a scalable, parameterized library for the various passive components (e.g., MIM capacitors, coupled inductors) was generated based on the foundry's MMIC process. This enabled optimization of the amplifier in the circuit simulator using full-wave analyzed passive components without degrading the accuracy, which was crucial. Implementation of the library in ADS is demonstrated in Fig. 2. Simulation of the whole RF signal path, including transistor feed networks, is also important. It was found that the feed networks have considerable effect and must be simulated using full-wave tools instead of just approximating them using simple transmission line elements.

Another important point in the design of the matching networks is to reduce gain of the amplifier at the outside of the band to prevent any undesirable oscillations as mentioned previously. Although the gain reduction in the high-frequency end is automatically satisfied with the falling gain slope of HBTs, same argument is not true for the lower end. The HBTs used in this work have extremely high gain at low frequencies. To address this, we employed two solutions: we first placed bandpass filter sections centered at 24 GHz at input and output (see Fig. 1). These bandpass filters also conveniently serve as dc-blocks and matching networks to input and output stages. Second, we implement interstage matching networks using shunt inductor-series capacitor (highpass) instead of shunt capacitor-series inductor (lowpass) configuration. Although both networks can be used to provide matching, first is advantageous here because the shunt inductance helps to attenuate low-frequency components. Note that one could also employ transformers as interstage matching networks. In fact,

if properly designed, transformers are ideal for interstage matching for the following reasons: (1) they automatically work as dc-blocks eliminating MIM capacitors, (2) low-frequency signals are attenuated, and (3) usage of different turn ratio enables the necessary impedance transformation between the stages.

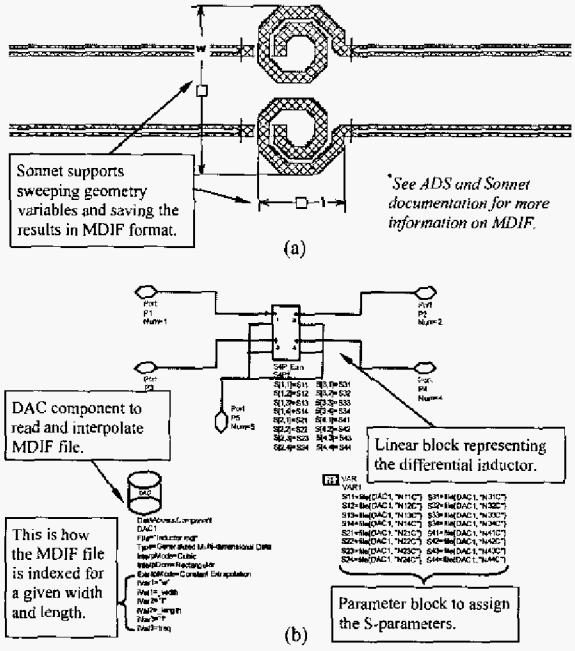

Figure 2 Implementation of scalable passive models using Sonnet and ADS. Note that the circuit parameters are interpolated automatically by the DAC component if the required parameter combination is not found in the data set.

C. Design of the Bias Circuits

For amplifiers with multiple stages, the bias circuits must be designed to minimize RF coupling between the stages as positive feedback through the bias circuits can put the entire amplifier into oscillation. This point is especially important in MMIC design where the biasing and RF circuits must be laid out in close proximity.

An unique aspect of a balanced amplifier configuration, which is helpful in feeding the bias voltages to the transistors, is the existence of virtual ground on the symmetry plane. At this point, the RF voltage with respect to either arm is ideally zero. To utilize this property, all the bias lines are first brought to the virtual ground point and then distributed to the current mirrors. This improved the isolation between bias circuits and RF transistors since the dc currents need to cross virtual-ground first before reaching the bias circuits attenuating any RF signal superimposed on them.

III. Measurement Results and Discussions

Measured gain of the amplifier using GS probes (the amplifier is designed to have a 50 ohm differential impedance) is shown in Figs. 3 and 4. From Fig. 3, it can be seen that the gain flatness is ± 0.5 dB in the frequency range of 22 GHz to 26 GHz. The bandwidth is also very well centered at the 24 GHz. On the other hand, the gain drops with a rate of 30 dB/octave at the outside of the frequency band (see Fig. 4). This filter-like behavior is due to interstage matching and input/output filter networks. Input and output return losses are shown in Figs. 5 and 6, respectively. The two-pole filter response increases the input matching bandwidth considerably.

Output power is shown in Fig. 7 at 24 GHz. As can be seen from the figure, the saturated power is around 12 dBm. Note that there is a very good correlation between the simulated and measured results. Variation of the gain with respect to temperature is given in Fig. 8. This relatively wide gain variation is due to the changing transconductance of transistors by temperature and can be compensated by including a PTAT circuit to control the transistor tail currents.

Finally, gain variation across the wafer and gain histogram are given in Figs. 9 and 10, respectively. Note that only 32 amplifier are sampled (i.e., one amplifier per reticule). The low gain samples essentially correspond to the samples located close to wafer edge.

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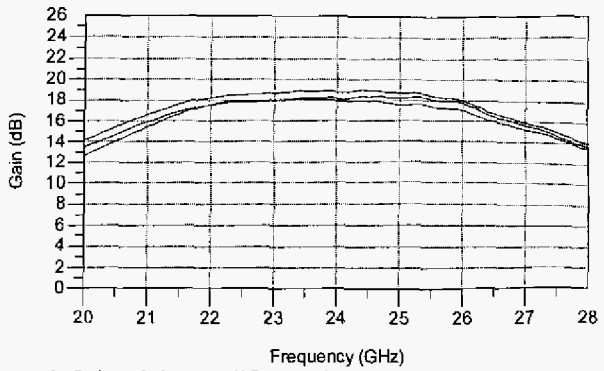

Figure 3 Gain of the amplifier in the frequency range of 20 to 28 GHz. Note to the gain flatness between 22 and 26 GHz.

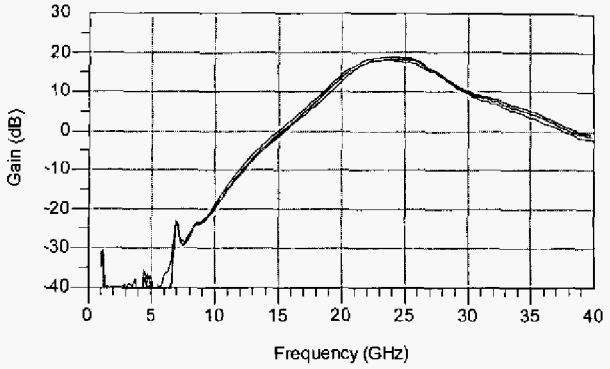

Figure 4 Gain of the amplifier in the frequency range of 1 to 40 GHz. Note that gain drops rapidly outside the band.

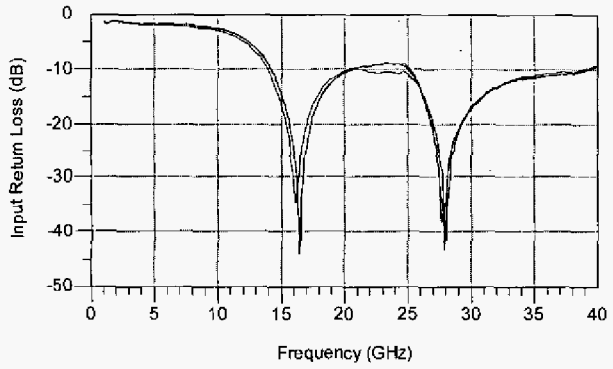

Figure 5 Input return loss of the amplifier in the frequency range of 1 to 40 GHz.

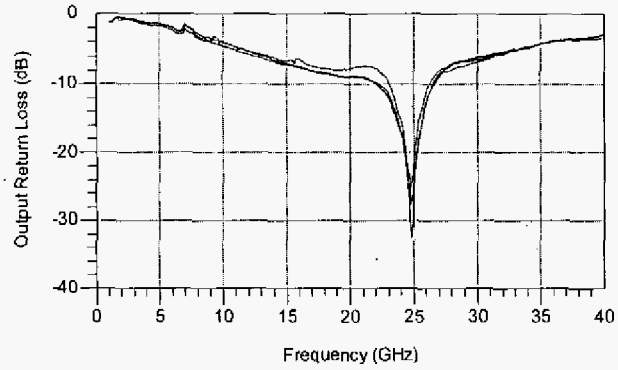

Figure 6 Output return loss of the amplifier in the frequency range of 1 to 40 GHz. Note that the operation band is 22 to 26 GHz.

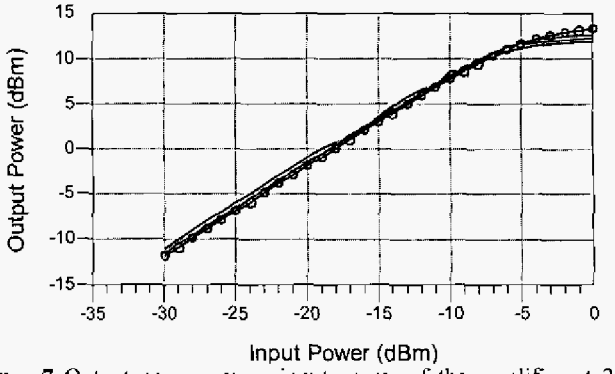

Figure 7 Output power versus input power of the amplifier at 24 GHz (circle: simulation, solid: on-wafer measurements).

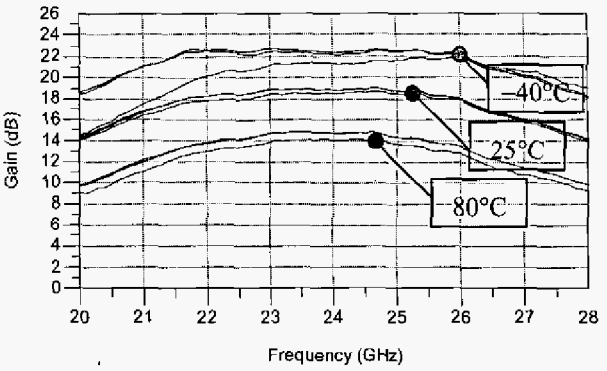

Figure 8 Gain of the amplifier at different base temperatures (–40°C, 25°C, and 80°C).

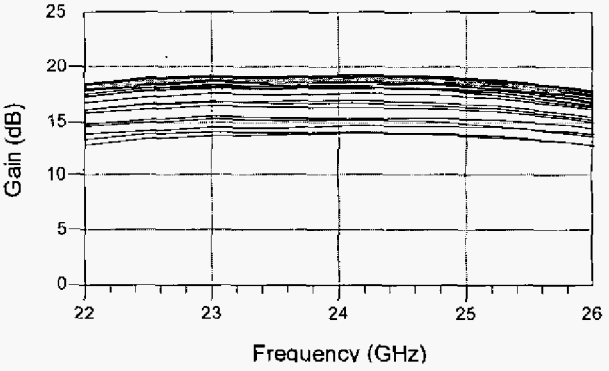

Figure 9 Gain variation of the amplifier across the wafer. The number of sampled amplifiers is 32.

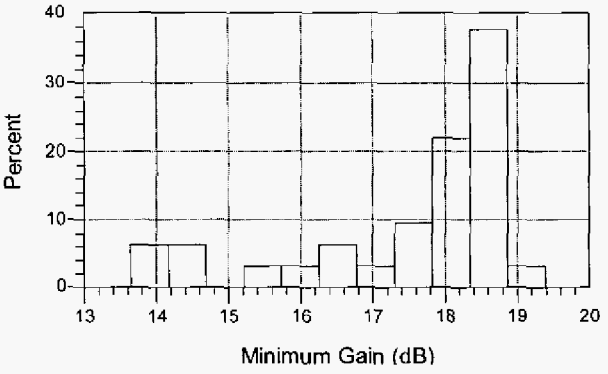

Figure 10 Gain histogram of the amplifier across the wafer.