# Design and Optimization of CMOS RF Power Amplifiers

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***Abstract*—A CMOS radio-frequency power amplifier including on-chip matching networks has been designed in a 0.6-$\mu$m n-well triple-metal digital CMOS process, and optimized using a simulated-annealing-based custom computer-aided design tool. A compact inductor model enables the incorporation of parasitics as an integral part of the parasitic-aware design and CAD optimization; low-*Q* metal3 spiral inductors are used in the input and output matching networks. A 3-V 85 -mW balanced fully integrated Class-C power amplifier with a measured drain efficiency of 55% at 900 MHz has been designed, optimized, integrated, and tested.**

***Index Terms*—CMOS analog integrated circuits, CMOSFET power amplifiers, power amplifiers, simulated annealing.**

## I. Introduction

RECENT years have seen a worldwide effort to develop highly integrated, low-cost radio-frequency (RF) transceiver circuits for wireless applications. Various global standards dictate that such systems meet stringent specifications at carrier frequencies ranging from 800 MHz to 5.6 GHz, and that the IC technology used maximize product portability and minimize cost. Consequently, CMOS has emerged as an attractive technology for implementing single-chip radios. At present, baseband and intermediate-frequency (IF) functions are easily integrated in CMOS while more difficult RF transceiver circuits are the subject of intense research [1]–[7], [20].

A major challenge in the design of CMOS RF ICs owes to the absence of high quality factor (high-*Q*) passive elements. The parasitics associated with on-chip inductors, capacitors, active devices, and the IC package have an adverse impact on the performance of RFICs. The traditional solution to this problem is the use of off-chip passive components which allows the designer to tune out parasitics and optimize the circuit on the test bench at the expense of increased board area, higher component count, and a bulkier product for the consumer.

In this paper, we describe the design and optimization of a fully integrated power amplifier (PA) using only on-chip matching networks fabricated in a standard 0.6-$\mu$m n-well triple-metal digital CMOS process. All matching networks are implemented using low-*Q* spiral inductors. A critical component of the design methodology is a custom CAD tool that optimizes the PA design for maximum drain efficiency in the presence of lossy on-chip matching networks. The presentation is organized as follows: Section II reviews basic Class A, B, and C power amplifiers. Section III describes a modeling approach for integrated inductors that is applicable to CAD optimization; Section IV details the CAD tool that performs *parasitic-aware optimization* including lossy on-chip matching networks, bondwire and package parasitics, etc. Measured results are presented in Section V for a balanced CMOS PA designed and optimized using the CAD tool, and conclusions are given in Section VI.

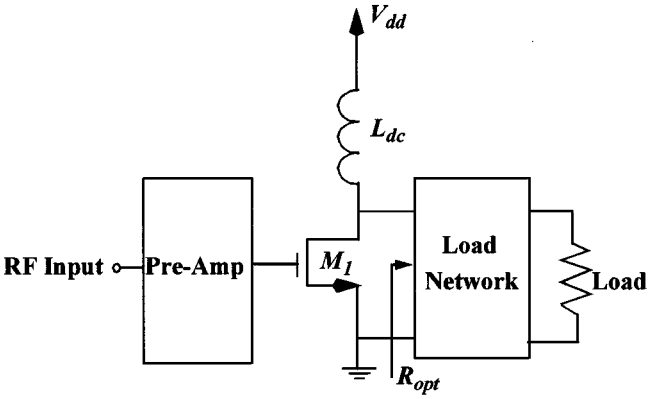


Fig. 1. Two-stage linear CMOS power amplifier topology.

## II. Class A, B, and C Power Amplifiers

In this section, we review Class A, B, and C power amplifiers, and highlight trade-offs between them. Class A PAs are highly linear, Class B PAs are less linear, and Class C PAs are even less so [8]. Shown in Fig. 1 is a basic two-stage linear RF PA which may be biased for operation in Class A, B, or C modes. The classes are distinguished by the fraction of the RF cycle over which the power transistor $M_1$ conducts: 100% corresponds to Class A, 50% to Class B, and less than 50% to Class C. Performance trade-offs among the various classes include efficiency, linearity, power gain, and output power. Linearity is quantified by the third-order intercept point (IP3), adjacent channel power, 1-dB compression point, or harmonic distortion. Drain efficiency is defined as

$$\eta_D = \frac{P_{\mathrm{rf,\,out}}}{P_{\mathrm{dc}}} \tag{1}$$

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and power-added efficiency (PAE) as

$$\mathrm{PAE} = \frac{P_{\mathrm{rf,\,out}} - P_{\mathrm{rf,\,in}}}{P_{\mathrm{dc}}} \tag{2}$$

where $P_{\mathrm{rf,\,out}}$ is the RF output power, $P_{\mathrm{dc}}$ is the dc power drawn from $V_{dd}$, and $P_{\mathrm{rf,\,in}}$ is the RF input power.

For classes A, B, and C, $M_1$ is operated as a transconductor rather than as a switch. Its drain current, $i(\theta)$, is modeled as the net *positive* portion of a cosine wave of peak amplitude $I_m$ superimposed upon a dc bias current $I_{dq}$ that is negative and less than $I_m$ for Class C, zero for Class B, and positive and greater than $I_m$ for Class A [8].

$$i(\theta) = \begin{pmatrix} I_m \cos\theta + I_{dq} \cdots -y/2 \le \theta \le y/2 \\ 0 \cdots \text{otherwise} \end{pmatrix} \tag{3}$$

where $y$ is the *conduction angle*. A Fourier series representation of the drain current is

$$i(\theta) = i_{\mathrm{dc}} + \sum_{n \ge 1} i_n \cos n\theta \tag{4}$$

where

$$\begin{aligned} i_{\mathrm{dc}} &= \left(\frac{I_m}{\pi}\right)\left(\sin\frac{y}{2} + \frac{y}{2}\cdot\frac{I_{dq}}{I_m}\right) \\ &= \left(\frac{I_m}{\pi}\right)\left(\sin\frac{y}{2} - \frac{y}{2}\cos\frac{y}{2}\right) \end{aligned} \tag{5}$$

and

$$\begin{aligned} i_n(y) = \frac{I_m}{2\pi}&\left(\frac{2}{n+1}\sin(n+1)\frac{y}{2} + \frac{2}{n-1}\sin(n-1)\frac{y}{2}\right) \\ &+ \frac{2I_{dq}}{n\pi}\sin n\frac{y}{2}. \end{aligned} \tag{6}$$

The relationship between $I_{dq}$ and $I_m$ for the conduction angle $y/2$ from (3) is used to simplify (5). The dc component is used to calculate the average power drawn from the supply. With an appropriately designed load network, only the fundamental component of drain current flows through the load resistor. Similarly, the inductor connected to the drain provides a path for the dc drain current, and offers high impedance to the signal current. Thus, a sinusoidal voltage is obtained at the output.

In order to obtain maximum voltage swing at the drain, a specific load resistance must be presented to the active device (Fig. 1). For a given conduction angle, $y$, the product of this load resistance, $R_{\mathrm{opt}}$, and the peak instantaneous value of the fundamental component of the drain current, should equal the desired maximum voltage swing. Hence, $R_{\mathrm{opt}}$ can be obtained from

$$V_{dd} - V_{\mathrm{dsat}} = i_1(y) \times R_{\mathrm{opt}} \tag{7}$$

where $i_1$ is the amplitude of the fundamental current for conduction angle $y$. With the optimum load impedance presented to the PA output, the maximum RF voltage swing of $V_{dd} - V_{\mathrm{dsat}}$ is obtained at the drain. Hence, the drain efficiency which is the ratio of the RF power [one-half of the product of the peak RF voltage swing and the peak RF current given by (6) for $n = 1$] to the dc power [the product of the supply voltage and average current given by (5)] is easily derived as

$$\eta_D = \frac{V_{dd} - V_{\mathrm{dsat}}}{V_{dd}} \cdot \frac{y - \sin y}{4\left(\sin\frac{y}{2} - \frac{y}{2}\cos\frac{y}{2}\right)}. \tag{8}$$

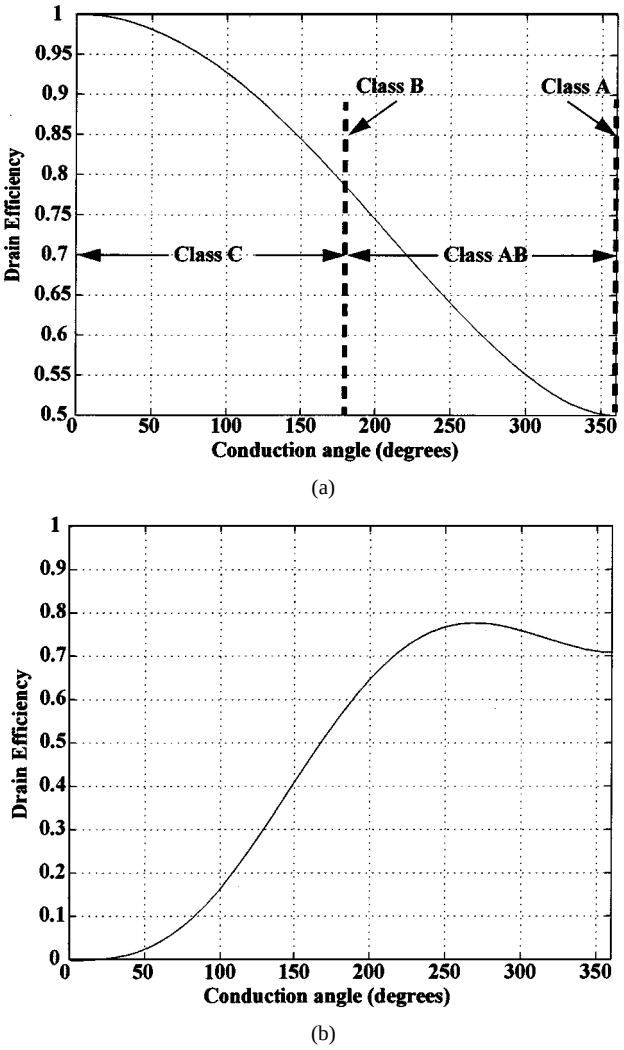


Fig. 2. PA drain efficiency versus conduction angle. (a) $R_{\mathrm{opt}}$ varied for maximum output voltage swing ($V_{dd}$) at each point. (b) $R_{\mathrm{opt}}$ fixed.

Shown in Fig. 2(a) is drain efficiency versus conduction angle. Note that $\eta_D$ increases as $y$ decreases. Also evident is the Class A efficiency of 50% and Class B efficiency of 78.5% (neglecting $V_{\mathrm{dsat}}$) corresponding to conduction angles of 360° and 180°, respectively. Implicit is the assumption that the peak output voltage swing is *maximum* ($V_{dd}$) for all values of $y$. Consequently, the load resistance must be different for each value of $y$. Thus, this curve does *not* represent how a PA with a *fixed* load resistance behaves if the conduction angle of the driver transistor is varied. It does give an upper limit for the drain efficiency achievable for a fixed optimum load resistance value. This efficiency is realized for a particular conduction angle for which the output voltage swing is maximum. An important implication for a PA with a fixed matching network optimized for a particular output power level is that its efficiency will degrade when operated at a reduced power level [Fig. 2(b)].

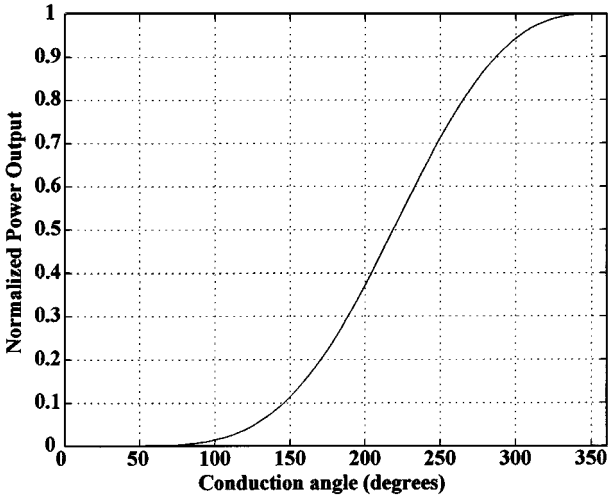


Fig. 3. PA output power (normalized to Class A) versus conduction angle.

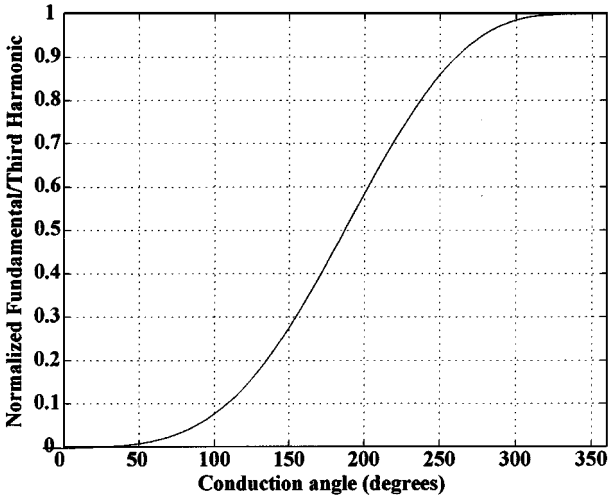


Fig. 4. PA normalized fundamental to third harmonic component ratio versus conduction angle.

The increased efficiency at a reduced conduction angle is achieved at the expense of decreased maximum power output. In the limit, one can design a Class C PA to achieve a drain efficiency approaching 100%, but the corresponding output power approaches zero. The output power is expressed as

$$P_o = \frac{1}{2} v_o i_1 = \frac{1}{2} (V_{dd} - V_{\text{dsat}}) \frac{I_m}{2\pi} (y - \sin y). \qquad (9)$$

Shown in Fig. 3 is a plot of the output power (normalized to that of a Class A PA) as a function of $y$, again assuming that the output voltage swing is maximum ($V_{dd}$). Clearly, the increased efficiency from reducing $y$ is achieved at the expense of reduced output power. Thus, there is a direct trade-off between drain efficiency and power output. As the conduction angle decreases, the harmonic content of the output signal also increases, illustrating a linearity-output power-efficiency trade-off. Fig. 4 shows a plot of the normalized ratio of the fundamental and the third harmonic components versus conduction angle. This plot indicates the behavior of IP3 as a function of conduction angle. A reduced conduction angle causes the fundamental component to decrease more rapidly than the third harmonic, resulting in a more nonlinear power amplifier. Depending upon the peak to average power ratio of the signal being amplified, the adjacent channel power performance also degrades as the conduction angle is reduced beyond a certain limit.

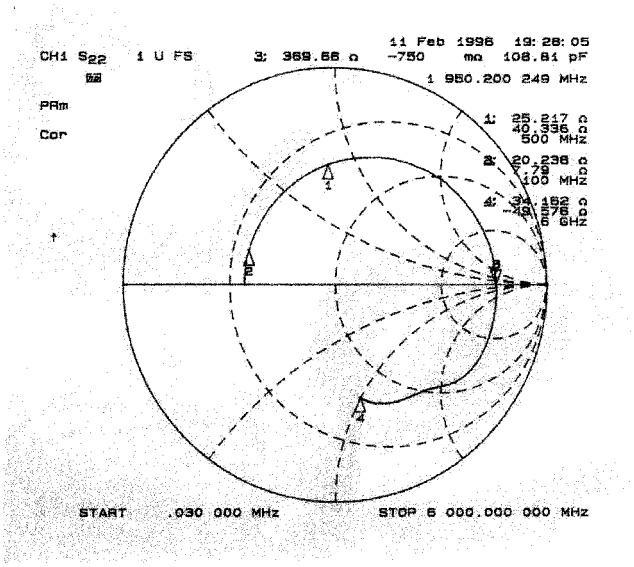


Fig. 5. Measured one-port $s$-parameter values for a metal3 square spiral inductor, 7.25 turns and 12.4 nH.

## III. Integrated Inductor Model for CAD Optimization

Shown in Fig. 5 is measured one-port $s$-parameter data for a square spiral inductor fabricated in a standard 0.6-$\mu$m triple-metal CMOS process. The 29-segment (7.25 turns) inductor formed on the metal3 layer was 15-$\mu$m wide with a 1.2-$\mu$m interturn spacing, and a 100-$\mu$m inner hole. The measured low-frequency inductance was 12.4 nH and the self-resonant frequency was 2.24 GHz. As expected, the inductor exhibits a low $Q$-factor because the measured impedance has a large resistive component. Since low-$Q$ integrated inductors have a significant impact on the performance of PAs, accurate compact inductor models are essential to design and optimization.

To obtain accurate parametric inductor models, we have adopted the approaches of [9]–[11]. Each metal3 segment of the square spiral is modeled using a lumped equivalent circuit comprising a self-inductance, a series resistance equal to the dc resistance of the segment, a shunt capacitance between the segment and the substrate, an effective substrate loss resistance, and an interturn coupling capacitance. Positive and negative mutual inductance coupling terms between adjacent segments as well as segments on opposite sides of the spiral are included. The effects of corners and bends are assumed to be negligible at the frequencies of interest. Fig. 6 shows a five-segment planar inductor and its full-blown lumped element model. Although accurate, this model is computationally unattractive for use in CAD optimization which often requires tens or hundreds of thousands of iterations to find the optimum design. Thus, simulated annealing optimization over a range of inductor values necessitates the use of a *compact* inductor model (Fig. 7) that approximates the impedance versus frequency behavior of the full-blown model of Fig. 6. Note that while the parasitics

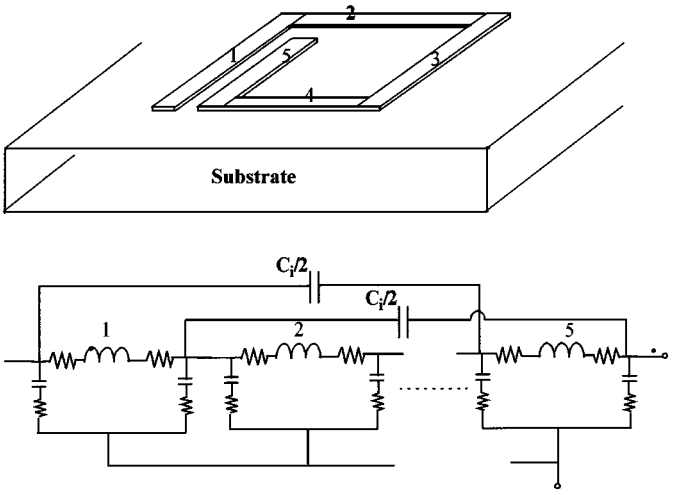


Fig. 6. Five-segment (1.25-turn) square spiral inductor and a lumped equivalent circuit model.

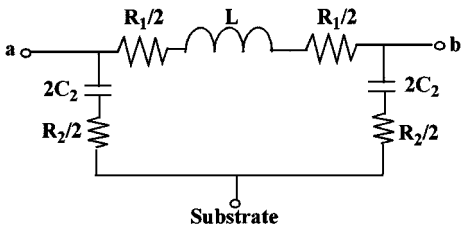


Fig. 7. Lumped element compact model representing the full-blown model of Fig. 6.

associated with the inductor's inner and outer ports are not identical, a symmetrical compact model is found to approximate the inductor response adequately in the frequency range of interest. The value of $L$ is obtained using Greenhouse's method [9]. $R_1$ is the calculated dc series resistance of all segments forming the inductor. $C_2$ and $R_2$ are selected so that the compact model has the same $Q$ and $f_{\max}$ as the full-blown model:

$$Q = \frac{1}{R_1 + R_2}\sqrt{\frac{L}{C_2}} \tag{10}$$

$$f_{\max} \approx f_n = \frac{1}{2\pi\sqrt{LC_2}}. \tag{11}$$

By repeating this procedure, $R_1$, $R_2$, and $C_2$ are obtained as functions of $L$ over a desired range of inductances. For the process and geometry parameters listed in Table I, the following polynomials were obtained for a *floating* inductor in the range of 1 nH to 18 nH:

$$R_1 = -0.0278L^2 + 1.741L + 2.3402 \tag{12}$$

$$2C_2 = -0.0005L^2 + 0.0307L + 0.0468 \tag{13}$$

$$R_2 = -0.0894L + 32.151 + 3.5064/L \tag{14}$$

where $L$ is in nH, $C_2$ is in pF, and $R_1$ and $R_2$ are in ohms. Note that a similar set of equations with different coefficient values is required for inductors used with one end grounded.

TABLE I
KEY CMOS PROCESS AND INDUCTOR GEOMETRY PARAMETERS

| Parameter | Value |
|---|---|
| Metal3 Sheet Resistance | 0.05 ohm/sq |
| Metal3 Capacitance to Substrate | 20 aF/$\mu m^2$ |
| Length of Shortest Segment | 100 $\mu$m |
| Width of Metal3 Segments | 15 $\mu$m |
| Spacing Between Turns | 1.2 $\mu$m |

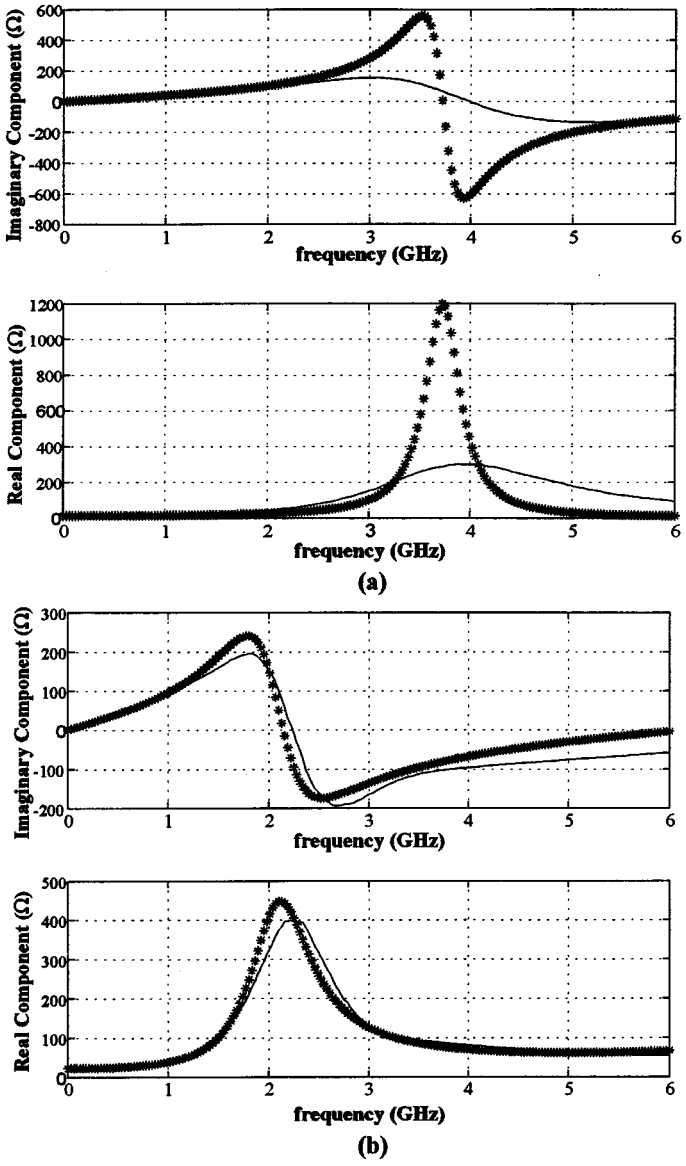


Fig. 8. Comparison of measured $(-)$ and predicted $(*)$ impedances of a 5.25-turn inductor versus frequency for (a) $K = 0$, and (b) $K = 70$.

Shown in Fig. 8(a) are both measured and simulated results for impedance versus frequency of a 6.18-nH 21-segment inductor using the circuit of Fig. 7 with values calculated using (12)–(14); the agreement is excellent up to about 2 GHz but poor near the first resonant frequency. The significant difference is attributed to substrate losses due to inductive coupling effects. In order to

maintain a simple compact model, we represent both inductive and capacitive substrate losses using an *effective* loss resistance

$$R_2 = K\left(\frac{\rho T}{WL}\right)\left\|\left(\frac{\rho}{2(W+L)}\right)\right. \tag{15}$$

where $\rho$ is the resistivity of the epitaxial layer, $T$ is its thickness, $W$ and $L$ are the width and length of the inductor, and $K$ is an empirical constant. The substrate resistance is initially calculated as the lateral spreading resistance [12], and then refined using the empirical factor $K$ obtained from fitting the model to the measured one-port $s$-parameter values. With proper choice of $K$, an excellent fit is achieved over a wide frequency range as shown in Fig. 8(b). In the next section, the parametric equations are incorporated into a CAD tool and used to predict inductor parasitics as the design space is explored during the optimization process.

## IV. CAD Optimization and Simulated Annealing

In the analysis presented in Section II, it was assumed that the optimum load to be presented to the PA output was purely resistive as given by (7). The analysis ignored the output impedance of the power transistor(s). In practice, however, the optimum load impedance that the PA requires also uses a reactive component to tune out the output impedance of the PA. Traditionally, load pull techniques have been used to determine the *large-signal* load impedance required for a particular power transistor. This involves using tuners to present a series of impedances to the PA and measuring its efficiency, linearity, etc., corresponding to these impedances. Off-chip matching networks are then realized as part of the design flow to transform the standard load to the desired load impedance. Designing the optimal matching networks generally involves significant effort on the test bench; the matching network loss, its bandwidth, and the interactions on the PC board are some significant factors that determine RF performance. In the completely integrated PA design, available active and passive device models are used, along with transient simulations, to determine the large-signal load impedance required by the PA.

### A. CAD for Integrated Power Amplifiers

The CAD tool described in this section mimics the process of load pull while simultaneously using on-chip lossy matching networks for the impedance transformation. While simple matching networks can be designed using lumped elements with the aid of a Smith chart, such an approach is not accurate enough for this case. The inductor and its associated parasitics can not be treated as distinct lumped elements because their values depend upon each other. Thus, if a given impedance value is required to be implemented by a matching network utilizing an on-chip inductor, an iterative approach needs to be taken to determine what inductance value, together with its associated parasitics, provides the impedance closest to the desired value. Even more significantly, the desired impedance value for optimum PAE is a function of the *loss* in the output matching network, as explained below. This process is too cumbersome for design by hand and requires a CAD tool.

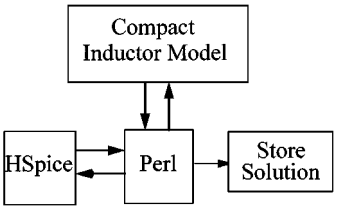


Fig. 9. Signal flow of the simulated annealing CAD tool using HSpice in the optimization loop.

The necessity of CAD optimization for integrated PAs can be justified by noting that an extremely significant difference between PAs using off-chip matching networks and fully integrated PAs is the impact of loss in the matching networks on the efficiency of the amplifier [13]. In the former case, the transistor efficiency primarily determines the overall PA efficiency as the matching network itself is low loss and can be assumed to transfer RF power from the transistor to the load with an efficiency approaching 100%. Therefore, the only consideration in the design of the matching network in this case is to transform the standard 50-$\Omega$ load to a desired impedance. As a result, the determination of the optimum load impedance and the corresponding matching network design can be carried out as two distinct design steps. However, in the case of integrated PAs, the overall PA efficiency is determined by *two* components—the efficiency at which the power transistor(s) operate and the efficiency of the matching networks. Note that the efficiencies of the transistor and the matching networks are *not* independent of each other. The transistor efficiency, for a given technology, depends primarily upon the load impedance presented to it, and hence on the elements comprising the matching network. Obviously, the matching network elements also determine the efficiency with which the matching network delivers RF power from the transistor to the load. Thus, there is a trade-off between the impedance transformation properties of the on-chip matching networks and the overall efficiency of the power amplifier. It is possible that the benefit in efficiency obtained by operating the transistor most efficiently requires a matching network whose loss offsets any improvement in overall efficiency of the PA. Using the traditional approach of determining the optimum load impedance using load-pull and subsequently designing the matching network is not adequate for the realization of high-efficiency *integrated* CMOS PAs. The design of fully monolithic PAs requires simultaneous determination of the load impedance and the corresponding matching network realization, allowing the maximum degree of optimization by fully exploring the trade-off between the matching network loss and its impedance transformation. It is likely that an integrated matching network may not perform an optimum load impedance transformation, but still results in higher overall efficiency due to lower loss in it, compared to an optimal (with respect to impedance transformation) integrated matching network. Alternatively, for integrated PAs, an optimum load network is more appropriately defined as one which results in best overall efficiency, and not as a network which performs the impedance transformation necessarily dictated by conventional load-pull. The CAD tool described here is designed to find such an optimum matching network for integrated PAs.

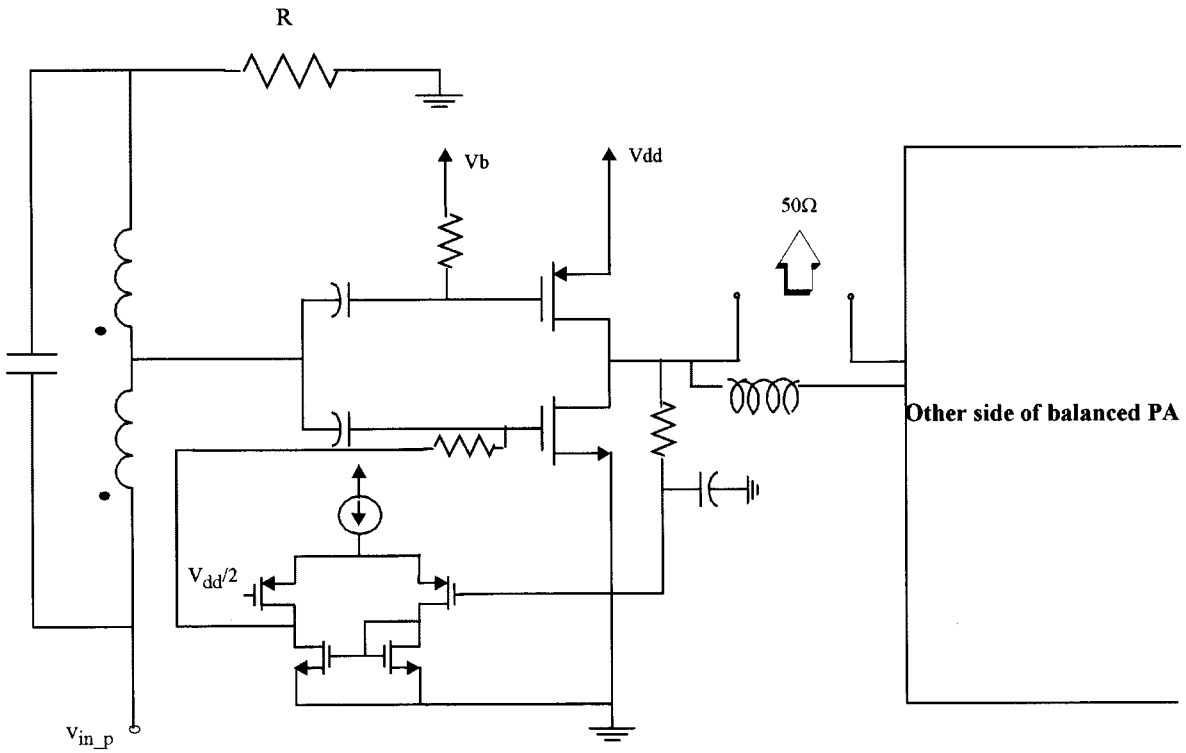


Fig. 10. Circuit schematic of the 900-MHz CMOS balanced power amplifier with integrated input and output matching networks. Note that the output matching network shown as an inductor is actually a $\pi$-match network when parastics are considered.

### *B. Simulated-Annealing-Based CAD Tool*

Simulated annealing is a heuristic [14], [15] which can be used to iteratively arrive at a solution to a problem while minimizing some cost function. Simulated annealing is not guaranteed to arrive at the best solution every time (hence it is a heuristic and not an algorithm). However, as the number of iterations increases, the probability of arriving at the best solution approaches unity. This algorithm is based on the metallurgical process of annealing. Annealing involves first heating a metal to a high temperature, and then allowing it to cool slowly at a controlled rate. Heating of the metal allows the atoms to rearrange into any one of numerous possible arrangements, and slow cooling allows these atoms to settle into a highly ordered structure. In simulated annealing, the attainment of the global optimum for an optimization problem is analogous to the formation of a highly ordered metal structure in the case of conventional annealing. Similar to its metallurgical counterpart, in this case too the "temperature" of the solution to the problem is gradually reduced and at lower temperatures, the system approaches the optimum solution (analogous to a highly ordered state in the metallurgical annealing of solids). This algorithm has the advantage that the probability of getting trapped in a local minima is low since at higher temperatures, the solution has enough energy to jump out of a local minimum. As the temperature is reduced, and if enough iterations are carried out at each temperature, the simulated annealing algorithm should settle down in the global minimum, rather than being trapped in a local minimum. A gradient algorithm like steepest descent only accepts solutions which result in improved cost, and therefore reaching the global minimum is dependent on the starting point, or initial conditions. In contrast, simulated annealing is likely to find the global minimum irrespective of the starting solution as it conditionally accepts solutions of higher cost from one iteration to the next. This property of simulated annealing makes it well suited to explore the trade-off in PA efficiency discussed previously to arrive at the optimum matching network.

As part of simulated-annealing-based optimization, a certain number of iterations are carried out at each temperature. Each iteration involves selecting a solution set (which may consist of values for the various passive elements, as well as package parasitic values corresponding to specific pins of the package) and evaluating the cost function which is the PAE in this case. The solution is accepted if it is better than the previously accepted solution, and conditionally accepted otherwise. This process is repeated for different temperature values until either a certain number of iterations are performed or the goal is met. The initial temperature, the cooling rate, and the number of iterations to be carried out at each temperature are determined by trying several values for these parameters. This tool has been implemented in Perl [16], and uses HSpice to evaluate the efficiency of the PA when delivering full output power. The algorithm is set up to run a certain number of iterations, and stops once that number is reached.

Fig. 9 illustrates the signal flow and control configuration of this CAD tool. The simulated-annealing algorithm, implemented in Perl, involves running transient analysis on the circuit to be optimized, reading the efficiency from the HSpice output file, deciding if the solution is to be accepted, generating a new solution set, modifying the HSpice netlist, and repeating the process. The accepted solutions, as well as the power output, efficiency, etc., are documented in a separate output file. The parametric inductor model equations described in Section II are also

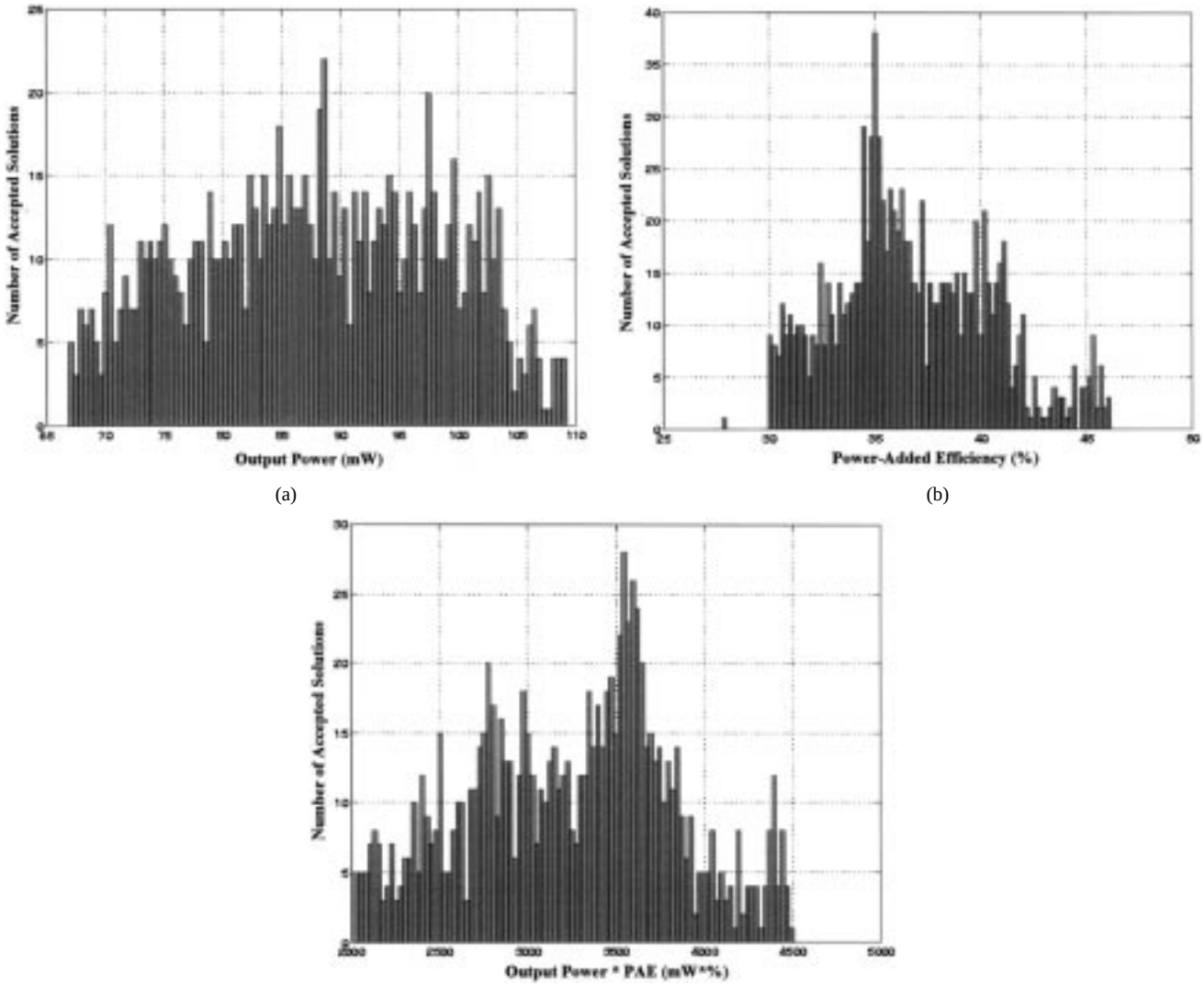


Fig. 11. Histograms of 1000 accepted solutions out of 28 000 total obtained from the simulated-annealing optimization of the CMOS balanced PA. (a) Output power. (b) Power-added efficiency (PAE). (c) Product of output power and PAE.

incorporated into the CAD tool. The implementation of the algorithm is fairly straightforward and can be tailored to interface with any simulation engine. This technique offers an attractive alternative to load-pull systems, and has the added advantage of allowing the design of optimized integrated matching networks. This eliminates the tuning on the PC board and reduces the impact of board layout and coupling on RF performance.

## V. CAD Optimized PA Design

This simulated-annealing-based CAD tool was used to optimize the balanced PA output stage of Fig. 10 for maximum PAE. The goal was to design an integrated PA stage to output 100 mW into a 50-$\Omega$ load at 900 MHz and operate from a single 3-V supply. In order to realize the maximum degree of optimization, the determination of the appropriate load impedance and the design of a corresponding matching network were combined into a single step by means of the CAD tool. The inductor traditionally connected to the drain of the power transistor has been replaced by a pMOS load. An inductor in the drain of the PA output stage allows a large peak voltage swing (ideally equal to $V_{dd}$) at the drain. This, in turn, makes it possible to deliver higher RF power, for a given

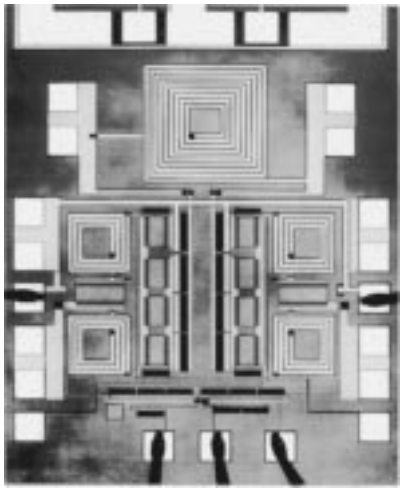

Fig. 12. Die micrograph of the fully balanced CMOS PA. Size including bonding pads is about 1.5 mm $\times$ 1.6 mm.

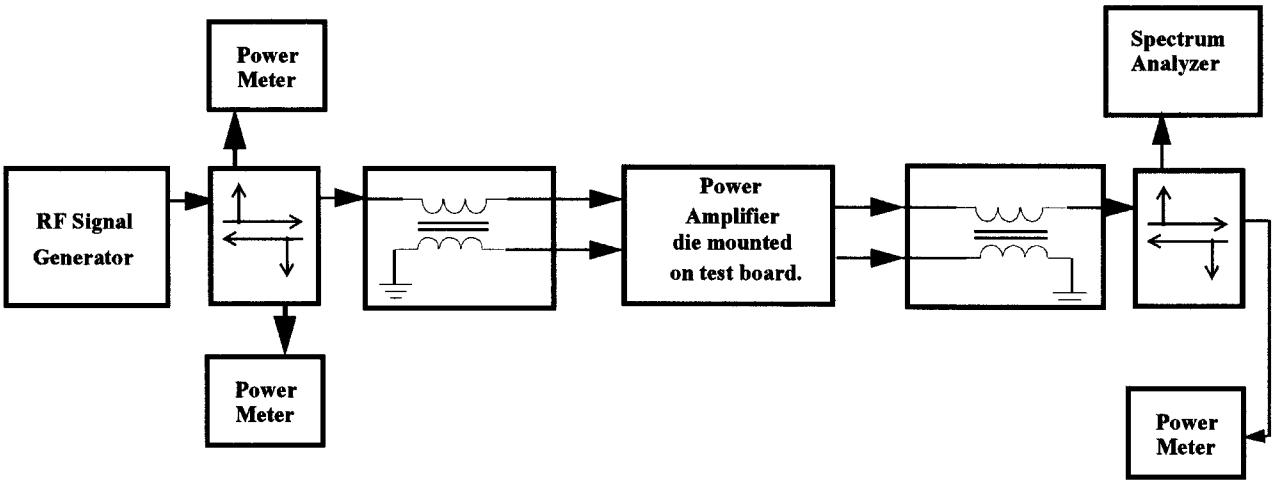


Fig. 13. Schematic of the test setup for the CMOS balanced PA.

current, than if the signal swing were 0.5 $V_{dd}$ (which would be the case if any other kind of load, like a pMOS transistor, were used). Thus, if the inductor is replaced by some other load, the RF power output decreases by $2\times$ (assuming the same signal current). Therefore, the efficiency of the output stage is also reduced by $2\times$. By applying the RF signal to the gate of both the nMOS and pMOS transistors [17], both devices contribute signal current, and if the impedance at the drain of the output stage transistors is low enough, this $2\times$ current does not result in a signal swing greater than 0.5 $V_{dd}$. Further, the $2\times$ increase in signal current does not require any additional dc current, so that the efficiency of the PA output stage will approach that of a stage with an ideal inductor load. In addition, a bridge T-coil is used as the input matching network [18].

The CAD tool was used to arrive at input and output matching networks by simultaneously optimizing their values for highest PAE for the amplifier, without imposing the additional constraint of optimizing for the input and output return loss. While the topology of the input matching network was fixed, $\pi$-network, high-pass and low-pass L-sections, and inductor topologies were investigated for output matching. Before optimization, the PA exhibited a drain efficiency of 36% using an L-section as an output match. After four days of optimization, a high-pass L-section was found for which the PA had an efficiency of 49%, while a simple shunt inductor used as the matching network achieved an efficiency of 57%. The $\pi$-section resulted in a maximum efficiency of only about 40%. The highest efficiency was obtained when using just a simple inductor as the output matching network. It is noteworthy that by utilizing the parasitics of the on-chip inductor, an impedance transformation that would ordinarily require at least an L-section is being performed. The histograms of Fig. 11 show the distributions of subsets of the solutions accepted by the simulated annealing CAD tool. It can be observed from these plots that the simulated annealing based CAD tool extensively explored the available solution space, finding matching networks which result in either high output power or high PAE [Fig. 11(a) and (b), respectively], as well as the more useful solutions resulting in high output power and high PAE [Fig. 11(c)].

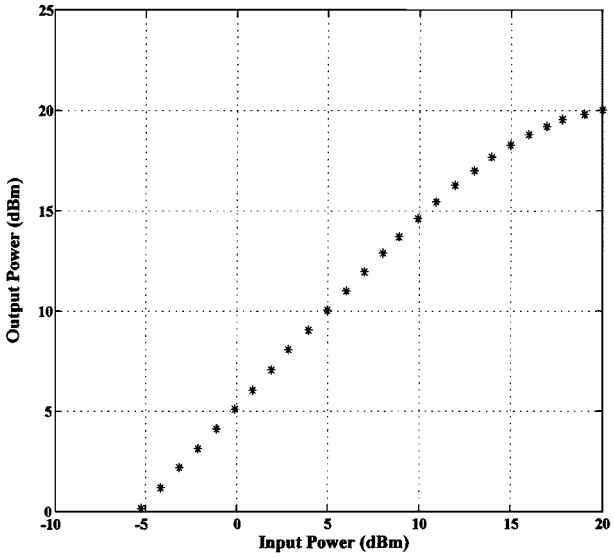


Fig. 14. Measured output power versus input power characteristic of the CMOS balanced PA at 900 MHz.

Fig. 12 is a die photograph of the PA. The inductors, fabricated using only metal3, are 15-$\mu$m wide with 1.2-$\mu$m spacing between turns, and with a 100-$\mu$m square hole in the center [19]. This amplifier has been fabricated in the HP 0.6-$\mu$m triple-metal n-well digital CMOS process offered through the MOSIS service. The PA was tested using chip-on-board assembly. The only off-chip components were baluns used for single-ended-to-differential conversion, and vice versa. This was necessitated in order to interface the PA with the measurement equipment. Fig. 13 shows the test setup used. Figs. 14–16 show the measured results for the PA. The PA exhibits a peak drain efficiency of 55% at 900 MHz, at an output power level of 85 mW. Using two-port $S$-parameter measurements, the input return loss for the PA was measured as 6.15 dB, and the output return loss is 17.9 dB. The reverse isolation is 25.6 dB. The relatively high return loss is attributed to inaccuracies near 900 MHz in the

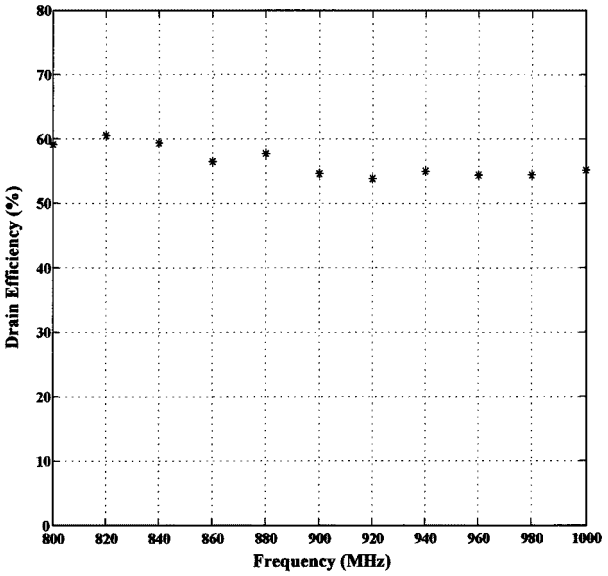


Fig. 15. Measured drain efficiency versus frequency characteristic of the CMOS balanced PA at 900 MHz.

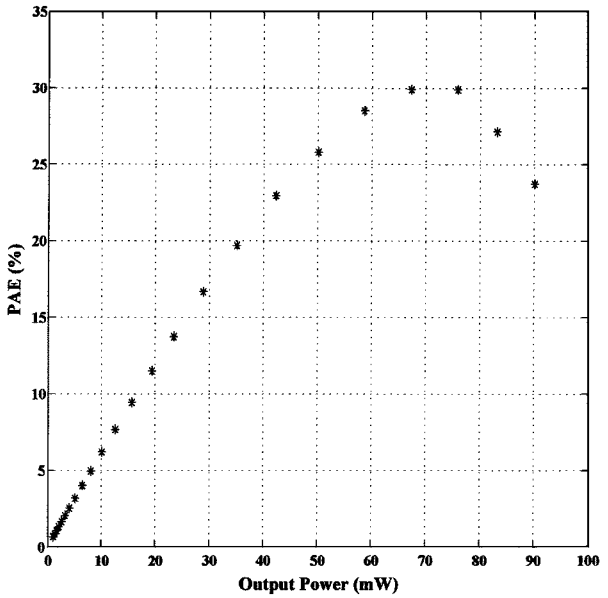


Fig. 16. Measured PAE versus output power characteristic of the CMOS balanced PA at 900 MHz.

transistor models used; it also contributes to the relatively low measured PAE value. The output power and drain efficiency obtained validate the design and optimization procedures.

## VI. Conclusion

A custom CAD tool, based on the simulated-annealing algorithm, has been developed to optimize the performance of power amplifiers for maximum efficiency using lossy matching networks. This CAD tool simulates the process of load-pull to determine the optimum *large-signal* load impedance for the PA, and simultaneously optimizes the matching network design based on the trade-off between the loss in the matching network and its impedance transformation properties. This trade-off is relevant in the case of high-loss matching networks only, as is the case in integrated RF CMOS ICs. This CAD tool has been used to optimize the efficiency of a balanced 85-mW CMOS PA operating at 900 MHz. Measured results validate the design and optimization process outlined in this work. It is demonstrated that in the design of RF CMOS PAs, significant benefits can be gained by incorporating parasitics into the parasitic-aware design process by means of CAD optimization.

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