A High Dynamic Range CMOS RF Power Amplifier with a Switchable Transformer for Polar Transmitters

[1]Younsuk Kim, [2]Bon-Hyun Ku, [2]Changkun Park, [2]Dong Ho Lee, and [2]Songcheol Hong

[1] Samsung Electro-Mechanics Co., Ltd., Suwon, 443-803, Republic of Korea

[2] School of Electrical Engineering and Computer Science, KAIST, Daejeon, 305-701, Korea

***Abstract* — A fully integrated CMOS RF power amplifier for a 1.8 GHz band EDGE polar transmitter is presented. It is implemented with 0.18-μm CMOS process. The output power is 33.4 ~ 33.5 dBm and the power added efficiency is 39 ~ 41 percent when the frequency varies from 1.71 to 1.91 GHz. The dynamic range is increased by 12 dB with the use of the proposed switchable transformer, which meets the EDGE dynamic range requirement of 37 dB when the supply voltage changes from 0.8 to 3.3 V.**

***Index Terms* — CMOS integrated circuits, MOSFET power amplifiers, MMIC power amplifiers, UHF power amplifiers.**

I. Introduction

CMOS power amplifiers (PAs) have been typically used as nonlinear PAs rather than as linear PAs, as CMOS PAs have a lower output power, lower efficiency, and less linearity than GaAs HBT PAs [1]-[2]. The output signals of the current wireless systems of EDGE, WCDMA, and WLAN contain information in the amplitude or envelope related to increasing the channel efficiency. This means that linear PAs or linearized PAs are required to amplify the signals without distortion. In an effort to achieve this linearity requirement with nonlinear PAs with high efficiency, EER or polar transmitter architecture was investigated [3]-[6].

Polar transmitters have numerous advantages compared to conventional transmitters [3]. However, they have a limited dynamic range due to the feed-through power [4]. To overcome this problem, a PA with a switchable transformer is proposed, which readily changes its output transformer ratio and its load impedance at a low power mode.

A fully integrated RF CMOS power amplifier for a 1.8 GHz band EDGE polar transmitter was designed. With the use of the proposed switchable transformer, the EDGE dynamic range requirement of 37dB is easily achieved.

This paper is organized as follows. Section II describes the dynamic range of the polar transmitter. Section III proposes a switchable transformer. In Section IV, the design of the PA is described. The measurement results are discussed in Section V and conclusions are given in Section VI.

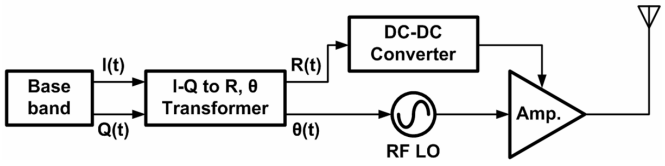

Fig. 1. Simplified block diagram of a polar transmitter.

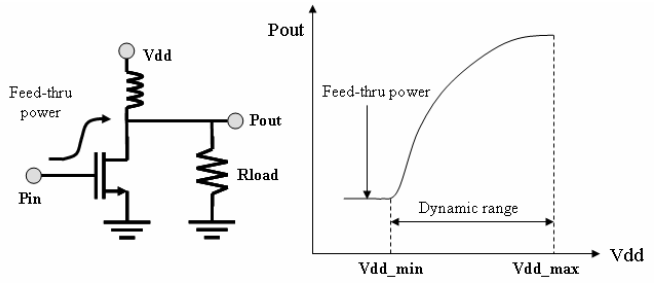

Fig 2. Dynamic range of the polar transmitter.

II. Dynamic Range of a Polar Transmitter

Fig. 1 shows the polar transmitter structure. The amplitude and phase information are separated and combined in a switching PA. The amplitude is modulated by the supply voltage controller of a LDO (low dropout voltage regulator) or a DC-DC converter. The constant amplitude phase modulated signal is fed to the PA. The output amplitude is only dependant on the supply voltage and the load impedance, rather than on the input signal amplitude.

Fig. 2 explains the dynamic range of the polar transmitter. The output power and dynamic range with fixed load impedance can be expressed as:

Authorized licensed use limited to: ULAKBIM UASL - SABANCI UNIVERSITY. Downloaded on December 06,2022 at 10:13:07 UTC from IEEE Xplore. Restrictions apply.

$$Output\ power = Eff * \frac{V_{dd}^2}{\alpha R_{load}} \quad (1)$$

$$Dynamic\ range\,(dB) = 20\log\left(\frac{V_{dd\_\max}}{V_{dd\_\min}}\right) \quad (2)$$

where V_{dd_max} and V_{dd_min} are the maximum and the minimum supply voltages of V_{dd}, E_{ff} is the PA efficiency, a is a proportion constant which varies from 1 to 2, and R_{load} is the load impedance. V_{dd_max} is decided by the battery voltage or the device breakdown voltage and V_{dd_min} is limited by the feed-thru power.

When the supply voltage is very low, the frequency response and the efficiency of the supply voltage controller is severely degraded [7]; moreover, a large phase distortion is produced which necessitates pre-distorters [4].

If the load impedance varies, the dynamic range of a polar transmitter can be improved by

$$Dynamic\ range\ improvement = 10\log\left(\frac{R_{load\_\max}}{R_{load\_\min}}\right) \quad (3)$$

where R_{load_max} and R_{load_min} are the maximum and the minimum load impedances, respectively, in a variable load PA.

III. Design of the Transformer

A. Transformer Ratio Decision

The PA output power is calculated by Eq. (1). When the load impedance is 50 ohm, the supply voltage 3.3 V, a = 1/1.365 (Class E), and the PA efficiency 70 percent, the output power is approximately 23 dBm as:

$$Output\ \ power = 1.365 * 0.7 * \frac{3.3^2}{50} = 0.21 \approx 23\,dBm \quad (4)$$

When the PA is differential, the output power is increased by 3 dB. If the transformer ratio doubles, it also raises the output power by 3 dB, as in Eq. (5). To achieve a higher output power than 33 dBm under the above conditions, four pairs of differential PAs (N=8) are needed with a 2 dB margin. would be

$$\begin{aligned} Output\ power &= 23dBm + 3dB * \log_2 N(number\ of\ cell) \\ &+ 3dB * \log_2 T(transformer\ ratio) \\ &= 23\,dBm + 9\,dB + 3\,dB * \log_2 2 = 35\,dBm \geq 33\,dBm \end{aligned} \quad (5)$$

B. Transformer Ratio Switching

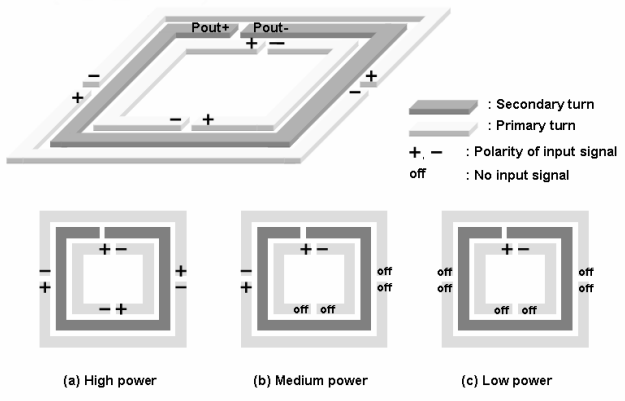

Fig.3. Transformer structure and shows the three operating modes of transformer ratio switching.

Fig. 3 shows the designed transformer and the three operating modes of transformer ratio switching. The transformer is a modified DAT (distributed active transformer) originally proposed by Aoki [1]. The primary turns are located both inside and outside the secondary turn. This double-sided coupling structure compared to a single-sided coupling structure can reduce the transformer size for an identical primary turn inductance. It also has a higher coupling coefficient, and makes possible the design of a higher powered and more efficient PA. The area of the transformer is 1.4 mm by 1.4 mm. The metal is 2.34 μm thick aluminum. The metal width of the primary turn, both inside and outside, is 60 μm; that of the secondary turn is 30 μm. The metal separations are 5 μm.

When all of the input signals are turned on, the transformer ratio is 2:1, as shown in Fig. 3 (a). When half of these are turned off, as shown in Fig. 3 (b), the transformer ratio is switched to 1:1 and the output power is decreased by 6 dB. When a quarter of these are turned on, as shown in Fig. 3 (c), the transformer ratio is 2:1 and output power is the same as that of Fig. 3 (b). However, Fig. 3 (c) shows definitely lower than 1/4 of the power operation because the transistor on-resistance of Fig. 3 (c) is higher than that of Fig. 3 (b). The dynamic range is increased by as much as 12 dB with this switchable transformer.

IV. Design of the Power Amplifier

Fig. 4 describes the circuit diagram of the designed PA. The power stage consists of four pairs of differential cascode amplifiers. The gate length and width of each common source power transistor are 0.18 μm and 4 mm, respectively; those of common gate transistor are 0.35 μm

Authorized licensed use limited to: ULAKBIM UASL - SABANCI UNIVERSITY. Downloaded on December 06,2022 at 10:13:07 UTC from IEEE Xplore. Restrictions apply.

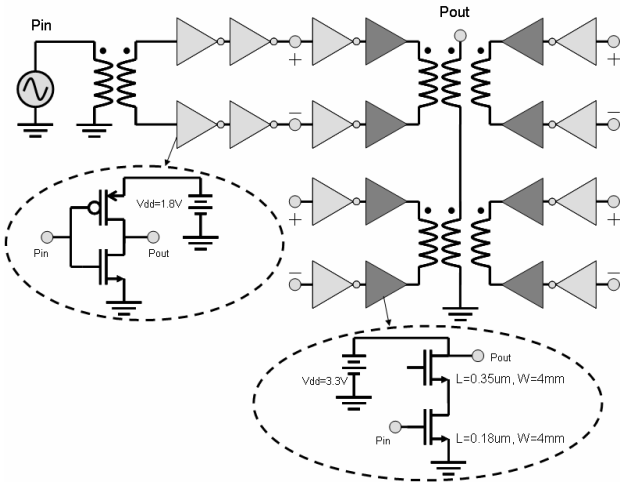

Fig. 4. Circuit diagram of the PA.

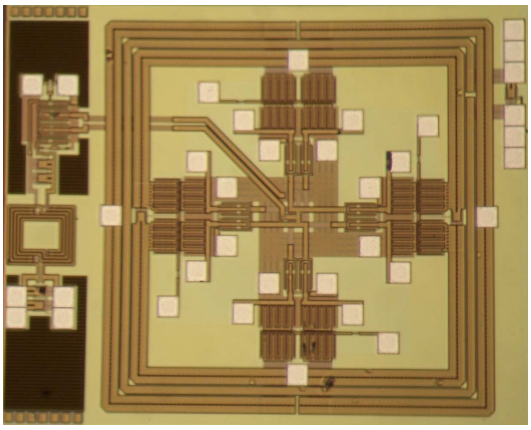

Fig. 5. Chip photograph of the PA.

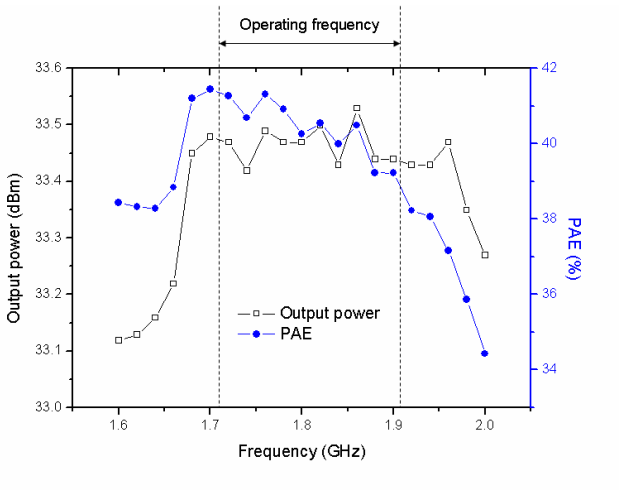

Fig. 6. Frequency response of the PA; Vdd = 3.3 V, Pin= 13 dBm.

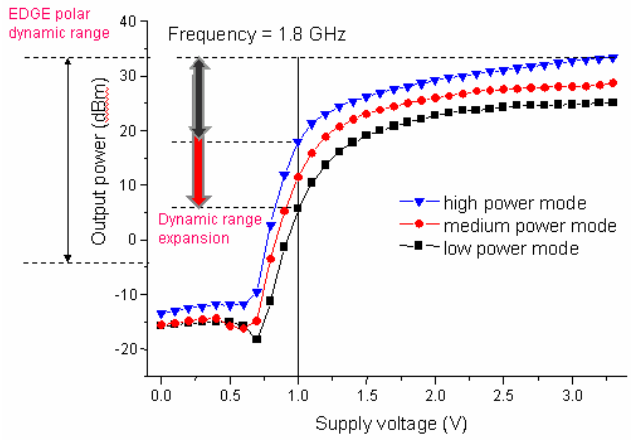

Fig. 7. Power vs. supply voltage according to the power mode.

and 4 mm. This cascade structure can tolerate a breakdown voltage of 9 V when no current flows.

The gates of the common gate power transistors were virtually grounded, and these gate bias voltages are turned on or off to select an operating mode, as shown in Fig. 3.

The driver amplifier consists of three stage CMOS inverter chains. A transformer balun is used to change the single-ended input signal to the differential. A supply voltage of 3.3 V is fed to the virtual ground of the transformer, as is 1.8 V to the driver amplifiers.

Fig. 5 shows a chip photograph of the designed PA. The chip area is 1.8 mm by 1.4 mm, inclusive of the input transformer and all of the pads. The power transistors are located inside the output transformer, as the magnetic field induced by the transformer is concentrated near the transformer. This possibility greatly minimized the chip area.

V. Measurement

Fig. 6 shows the frequency response of the designed PA. The supply voltage is 3.3 V and the input power is 13 dBm. The single-ended output power is higher than the EDGE requirement of 33 dBm over a frequency range of 1.71 ~ 1.91 GHz. The PAE (power added efficiency) is 39 ~ 41 percent for a 50 ohm load impedance, including the power consumption of the driver amplifier and all of the losses of the input transformer balun, the PCB interconnections, the bonding wires and other components.

Fig. 7 shows the output power versus supply voltage at 1.8 GHz. Four differential inputs of the transformer are turned on or off in order to select the operating mode, as shown in Fig. 3.

When half of the power transistors are turned off, as shown in Fig. 3 (b), the saturation power of the PA

Authorized licensed use limited to: ULAKBIM UASL - SABANCI UNIVERSITY. Downloaded on December 06,2022 at 10:13:07 UTC from IEEE Xplore. Restrictions apply.

decreases by 6 dB. For the same reason, when only one pair of the differential power transistors are turned on, the output power decreases by 12 dB. The 9/16 power mode, which is not shown in Fig. 3, occurs when one pair of transistors is turned off.

The dynamic range is increased by 12 dB, and the minimum supply voltage (V_{dd_min}) is increased from 0.7 V to 0.8 V to meet the dynamic range of the EDGE polar transmitter. Even if V_{dd_min} is increased by as little as 0.1 V, the AM-PM distortion of the PA may become much lower [1].

VI. Conclusion

A fully integrated CMOS PA meets the EDGE requirement in terms of power and dynamic range with reasonable efficiency. With the use of the switchable transformer, the dynamic range is increased by as much as 12 dB.

References

[1] I. Aoki, "Fully Integrated CMOS Power Amplifier Design Using the Distributed Active-Transformer Architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp.371-383, Mar. 2002.

[2] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, "A 1.4 Ghz – 2 Ghz Wideband CMOS Class-E Power Amplifier Delivering 23 Dbm Peak With 67 % PAE," *IEEE RFIC Symp., Dig. of Papers*, pp. 425–428, June 2005.

[3] M. R. Elliott, T. Montalvo, B. P. Jeffries, F. Murden, J. Strange, A. Hill, S. Nandipaku, and J. Harrebek "A Polar Modulator Transmitter for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2190–2199, Dec. 2004.

[4] P. Reynaert, and M. S. J. Steyaert, "A 1.75-GHz Polar Modulated CMOS RF Power Amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no.12, pp.2598-2608, Dec. 2005.

[5] Y. S. Jeon, H. S. Yang, and S. W, Nam, "A Novel EER Structure for Reducing Complexity Using Negative Resistance Amplifier," *IEEE Microwave Compon. Lett.*, vol. 14, no. 5, pp.195-197, May 2004.

[6] D. Su, and W. McFarland, "An IC for Linearizing RF Power Amplifiers Using Envelope Elimination and Restoration," in *ISSCC Digest of Technical Papers,* Feb. 1998. pp. 54–56.

[7] Y. Katayama, M. Edo, T. Denta, T. Kawashima, and T. Ninomiya, "Optimum Design Method of CMOS IC for DC-DC Converter that Integrates Power Stage MOSFETs," in *Power Electronics Specialists Conference 2004,* June 2004, vol. 6, pp. 4486 – 4491.

Authorized licensed use limited to: ULAKBIM UASL - SABANCI UNIVERSITY. Downloaded on December 06,2022 at 10:13:07 UTC from IEEE Xplore. Restrictions apply.