A 25-dBm High-Efficiency Digitally-Modulated SOI CMOS Power Amplifier for Multi-Standard RF Polar Transmitters

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***Abstract* — A single-ended digitally-modulated power amplifier (DPA) is demonstrated in a 0.13-µm 1.2-V SOI CMOS technology, to be used in a multi-standard RF polar transmitter. The amplitude modulation is done by digitally controlling the number of activated unit amplifiers whose currents are summed at the output. The DPA is designed for multi-mode multi-band functionality by avoiding frequency-selective components, except for the final-stage output matching network. The measured DPA is fully functioning and reliably delivers a 24.9-dBm peak output power at 900 MHz with a maximum power efficiency of 62.7%. It also exhibits similar high-efficiency performance for other carrier frequencies with a reconfigured matching network.**

***Index Terms* — Polar transmitter, multi-standard, silicon-on-insulator, SOI, CMOS, RF power amplifier.**

I. Introduction

With the continuing development of next-generation wireless communication systems, there has been a great interest in multi-standard transmitters (TXs), which would facilitate a smooth adoption of new standards as well as provide the possibility for global roaming in a single mobile device. To reduce the cost and the system complexity, multi-mode multi-band building blocks that can handle various standards without redundant hardware are attractive. The ideal solution is to have the whole system, from the digital baseband circuitry to the RF frontends, integrated onto a single CMOS chip. However, the design of a truly multi-standard CMOS TX is highly challenging, especially the integration of a multi-mode multi-band power amplifier (PA) since the PA needs to meet the stringent performance requirements of all integrated standards as well as provide highest-efficiency operation over a wide bandwidth.

Recently, several possible solutions for CMOS multi-mode RF TX systems were reported [1]-[3], [5]. The implementations in [1]-[3], however, provide low peak output power and would require one external PA with a large power gain for each frequency band. Moreover, the external PA is usually implemented by employing a conventional linear PA (class-A, AB) with a large power back-off to meet the stringent linearity requirements, resulting in much lower average power efficiency.

Power amplifiers (PAs) with a polar architecture provide advantages for linear amplification without severely compromising power efficiency. The signal is decomposed into a constant-envelope phase-modulated RF signal and an envelope baseband component, allowing the use of a high-efficiency nonlinear PA to amplify the RF phase signal, while the envelope portion is restored at the output. For greatest flexibility, the envelope signal can be delivered to the PA as a digital signal. This approach is especially promising in the highly-integrated CMOS technology where signal generation and linearity improvement can be achieved through the use of digital signal processing as successfully demonstrated in several papers [2]-[5].

This paper reports the development of a high-efficiency digitally-modulated PA (DPA) in a 0.13µm 1.2-V SOI CMOS technology. The DPA is to be used as the main building block in a proposed multi-standard CMOS RF polar TX that will be described in the next section.

II. Proposed Multi-Standard Polar Transmitter

Fig. 1 shows the block diagram of the proposed TX system. The DPA building block integrated in this silicon chip is inside the dotted line. As in a typical polar transmitter, the signal is separated into phase and envelope components. The constant-envelope phase-modulated RF signal can be generated using a digital phase-locked loop (PLL) [3]. The envelope signal is provided to the DPA as a 10-bit digital amplitude control word (*ACW*). The 7 most significant bits are decoded into a thermometer code and used to control the activation of 127 unit-weighted amplifiers, which are connected in parallel. The amplifiers' output currents are then combined at the drain to form the final RF output. The use of the binary-to-thermometer decoder helps avoid non-monotonic operation due to device mismatch. The 3 least significant bits of the *ACW* are used to control 3 binary-weighted amplifiers to provide extra resolution.

In fact, system simulations indicate that at least 7-bit resolution is required for amplitude modulation in order to meet the ACPR, EVM, and emission mask specifications for both GSM/EDGE and WCDMA with a reasonable margin [1],[5]. Here, the extra 3 least significant bits are introduced to compensate for the decrease in effective resolution due to the non-linearity of the amplitude modulation scheme.

Modern wireless communication standards also require a large transmit power control range (74 dB for WCDMA and 30 dB for GSM/EDGE) while maintaining a

sufficient signal quality. In this work, the transmit power control (*TPC*) will be provided by three components: supply variation, input attenuator, and output attenuator (to be reported in a separate paper).

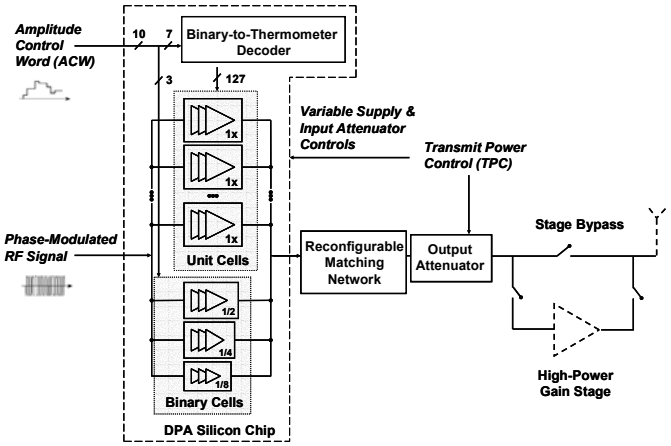

Figure 1: Block diagram of the proposed multi-standard polar transmitter.

The DPA is designed for multi-mode multi-band functionality by avoiding frequency-selective components, except for the final-stage output matching network, which can be implemented as an on-chip tunable circuit to provide highest power-efficiency for various frequency bands.

The choice of using SOI CMOS technology has several advantages over the standard bulk CMOS. The first is the availability of high-performance RF power switches. The high-resistivity substrate of the SOI CMOS also results in lower substrate coupling and lower-loss on-chip passive components. By arranging the RF switches as shown in Fig. 1, the DPA can be used to directly drive the antenna up to its full power (25-dBm peak output power) while an extra power amplifier is switched in only when the higher power is required, resulting in much improved average efficiency [6].

III. DPA Circuit Implementation

The simplified schematic of the DPA is illustrated in Fig. 2. Only one of the unit amplifiers is shown in detail. The 127 unit amplifiers and the 3 binary-weighted amplifiers are laid out in a rectangular array and connected in parallel by tree-structure input and output interconnects to minimize the phase mismatch.

The driver stage of the unit amplifier is composed of a chain of digital inverters (*M2-M3, M9-M14*) and an input attenuator (*R1, C1, M15-M16*), which can be used to reduce the input swing at the final stage through capacitive dividing, thus increasing the overall transmit power control range.

Each unit amplifier's activation is controlled by an enable signal (*EN*), which is decoded from the 10-bit *ACW* and synchronized through a register. A digital AND gate (*M4-M7*) is inserted at the input side of the driver stage. In this way, when the unit amplifier is deactivated, no switching power is consumed. In addition, when *EN* is low, transistors *M8* and *M17* are turned on to further ensure that the final power switch *M1* is off and all intermediate nodes are in defined states.

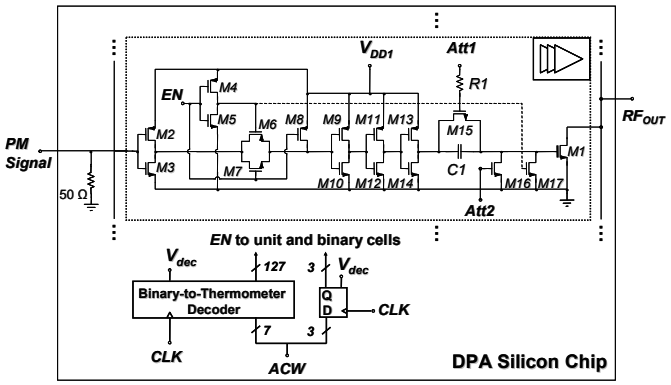

Figure 2: Simplified DPA schematic.

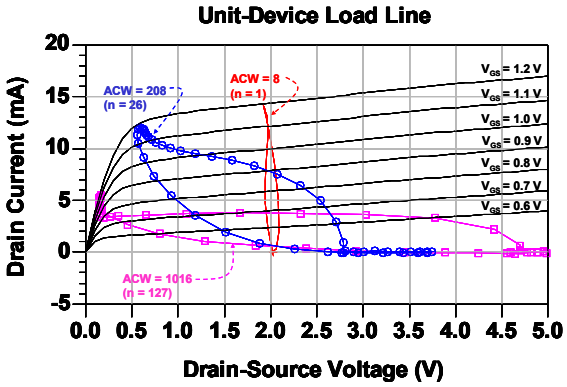

Figure 3: Simulated dynamic load line of an activated unit device with increasing *ACW* at 1.9 GHz

All transistors are 0.13-µm 1.2-V FETs, except for the final power switch, which is a 0.28-µm 2.5-V standard I/O FET. The supply voltage (V_{DD1}) for the driver stage is 1.2 V, while the final-stage drain bias (V_{DD2}) is varied between 0.5 V and 2.1 V to provide average transmit power control. A 50-Ω termination is placed after the input pad to have defined input impedance and driving power. The input is DC-biased at 0.6 V and an RF input power of at least 5.5 dBm is needed to create a 1.2-V full-swing input signal. In a fully-integrated TX system, however, the DPA would be driven directly by the phase-modulated RF output of the PLL.

The amplitude-modulation mechanism of the DPA can be explained by looking at the load line of a unit device (final-stage switch). When activated, the unit device is hard-switched as its input swings between V_{DD1} and ground, and its load line tracks the device I-V curve ($V_{GS} = V_{DD1} = 1.2$ V) as illustrated by the simulation in Fig. 3.

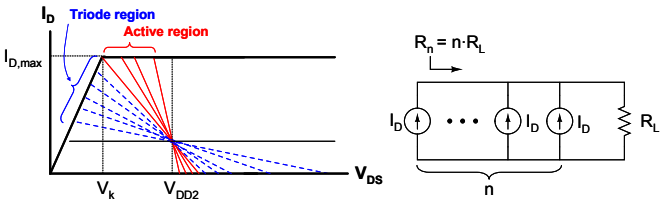

Figure 4: Load-pull effect on an activated unit-device load line.

To simplify the analysis, an idealized device model is assumed. When only one unit device is activated, the device sees a load resistance R_L and supplies a peak current $I_{D,max}$. As the number of activated unit amplifiers (n) increases, however, each unit device sees a larger load resistance of $n \cdot R_L$ due to the active load-pull effect and the device load line is rotated accordingly as shown in Fig. 4. The DPA can be described as operating in two separate regions depending on the number of activated unit devices.

When n is small, each unit device operates entirely in its active region and acts as a constant current source. Consequently, the total RF output current is linearly proportional to n. The output power and efficiency can be derived as:

$$P_{out} = \frac{1}{8} \cdot \left(I_{D,\max}^2 R_L \right) \cdot n^2 \qquad (1)$$

$$\frac{P_{out}}{P_{DC}} = \frac{1}{8} \cdot \left(\frac{I_{D,\max}^2 R_L}{V_{DD2} I_{DC,unit}} \right) \cdot n \propto \sqrt{P_{out}} . \qquad (2)$$

In the actual devices, however, other device effects such as channel-length modulation introduce AM distortion.

When n is large, the unit device will eventually enter its triode region ($V_{DS,min} < V_k$) and the RF current supplied by each device diminishes with the increasing n. As a result, the total output power delivered to the load saturates.

IV. Measurement Results

A die micrograph of the PA is shown in Fig. 5. The chip was fabricated in a 0.13-µm SOI CMOS technology. The total die area is 1.12x1.2 mm^2, including pads. The chip was mounted directly on a printed circuit board with off-chip output matching components, designed such that the DPA operation approaches a high-efficiency switching mode. The DPA is also designed to operate reliably according to a recent study on FET degradation under RF stress in CMOS PAs [7].

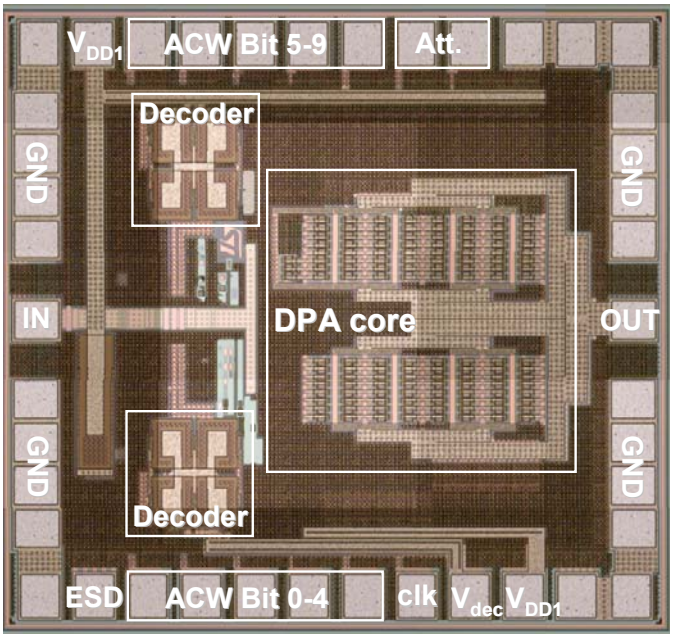

Figure 5: Chip micrograph.

Power measurements were performed under continuous-wave (CW) operation with a 900-MHz carrier frequency. Fig. 6 shows the monotonic variation of output power with *ACW*. The DPA delivered 24.9-dBm maximum output power with 62.7% maximum power efficiency, as well as achieving 43.9 dB of amplitude modulation (29 dB from the 7 most significant bits). Moreover, the input attenuator and supply variation together provided approximately 16 dB of transmit power control range. An output attenuator will be added in the future to meet the full required transmit power control range.

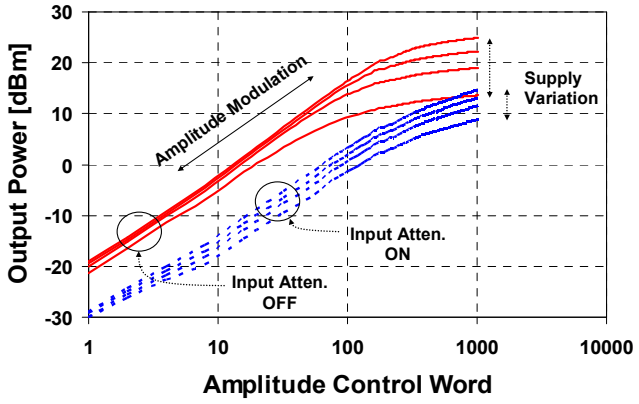

Figure 6: Measured output power vs. *ACW* at 900 MHz. The input attenuator and supply variation provide average transmit power control.

Fig. 7 illustrates the measured relationship between power efficiency and output power in log-log scale. The power efficiency is approximately proportional to the square root of the output power as described in the previous section.

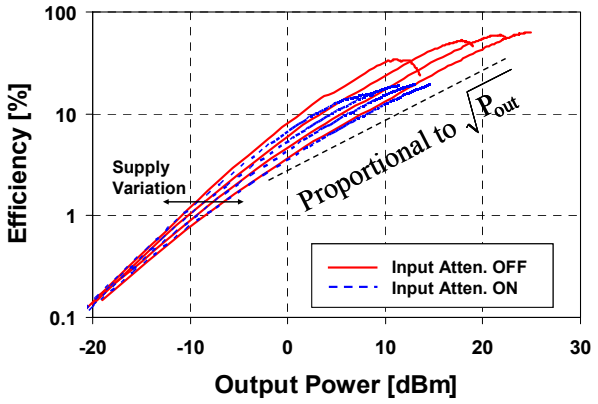

Figure 7: Measured efficiency vs. output power at 900 MHz.

With a large supply voltage and without input attenuation, the amplitude modulation is highly nonlinear due to the device operating in two regions as explained in the previous section. When the input attenuator is activated, however, the amplitude modulation becomes much more linear as the unit devices operate mostly in their active region. The worst-case phase distortion is measured to be lower than 21°. Both the amplitude and phase distortions can be corrected in the baseband using an adaptive digital predistortion (DPD).

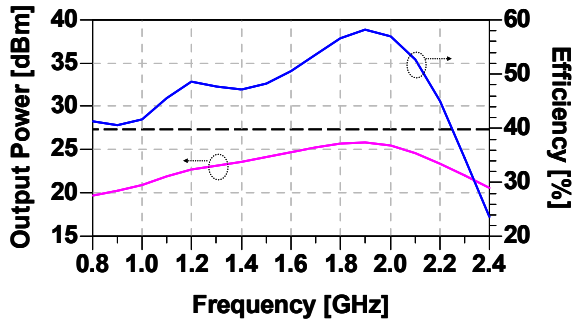

Fig 8: Simulated output power and efficiency vs. carrier frequency with a fixed output matching network optimized for a broadband performance.

Similar performance is obtained in the measurement at other carrier frequencies by reconfiguring the output matching network. Moreover, a further simulation shows that it is also possible to design an optimized matching network to achieve relatively high efficiency operation (> 40%) over a very broad bandwidth, albeit with slightly lower output power, as shown in Fig. 8. However, this possibility is limited in the measurement at the moment by the bond-wire inductance and PCB parasitic components.

V. Conclusion

A high-efficiency single-ended digitally-modulated power amplifier has been demonstrated in a 0.13-µm 1.2-V SOI CMOS technology. It reliably delivers a 24.9-dBm peak output power with a maximum power efficiency of 62.7% at 900 MHz, as well as exhibits multi-band functionality with a reconfigured matching network. The 10-bit resolution provides more than 40 dB of amplitude modulation; while the integrated input attenuator and supply variation together provide 16 dB of transmit power control range. The implemented DPA, together with the proposed polar architecture, is an attractive solution for the next-generation multi-standard RF transmitter design.

Acknowledgement

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