High-Performance CMOS Power Amplifier With Improved Envelope Tracking Supply Modulator

Byungjoon Park, Dongsu Kim, Seokhyeon Kim, Yunsung Cho, Jooseung Kim, Daehyun Kang, Sangsu Jin, Kyunghoon Moon, and Bumman Kim, *Fellow, IEEE*

***Abstract*—A differential cascode CMOS power amplifier (PA) with a supply modulator for envelope tracking (ET) has been implemented using 0.18-μm RF CMOS technology. For maximizing the PA's performance, the CMOS power cell has been optimized. The CMOS PA employs 2nd harmonic control circuits at the input, source, and output of the PA to improve efficiency and linearity at the same time. The CMOS PA utilizes an improved ET supply modulator, which is suitable for a CMOS PA with high knee voltage. By utilizing this modulator, we achieve not only higher linearity, but also higher efficiency in all power levels. For a long-term evolution signal at 1.70 GHz with a 10-MHz bandwidth and a 16-QAM 7.5-dB peak-to-average power ratio, the CMOS ET PA module achieves a power-added efficiency of 36.6%, an error vector magnitude of 3.0%, and an adjacent channel leakage ratio of −35.6 dBc at an average output power of 28.5 dBm. The proposed ET operation reduces the total current consumption over the standalone PA, by 10% at the peak power and up to 56% at a low power.**

***Index Terms*—CMOS, efficiency, envelope tracking (ET), linear, long-term evolution (LTE), power amplifier (PA), supply modulator.**

I. Introduction

THE smartphone has become an indispensable part of our everyday lives, and this smartphone should have a multifunctional capability. Not only calling and receiving calls, but also Web surfing, video catting, streaming video, etc. are all carried out by a single smartphone device. For a good quality of the services, the devices should ensure a longtime usage of battery. In a smartphone, the power amplifier (PA) is one of the most power consuming blocks, hence a lot of research is ongoing to the improve efficiency of the PA for a prolonged battery life.

To manage the increased information of the multi-contents using the limited available frequency spectrum, modern wireless applications, such as long-term evolution (LTE) and wideband code division multiple access (WCDMA), are coded for a high spectral efficiency. These modulated signals use quadrature amplitude modulation (QAM), quadrature phase-shift keying (QPSK), or orthogonal frequency division multiplexing (OFDM), and have large peak-to-average power ratios (PAPRs). Therefore, the PAs should be able to operate at the back-off power region with a high efficiency.

Furthermore, integration of RF integrated circuits (RFICs) with baseband processors is required for system-on-chip (SoC) realization to reduce cost and size of the handset devices. The RF PA is the toughest component to integrate for the SoC. Due to the reliability and performance issues, the RF PA is usally based on a GaAs substrate, whereas most of the other chips are based on a CMOS substrate. The GaAs substrate has limited integration capability and high cost compared to the CMOS substrate. Therefore, eventually PAs will be integrated into either a CMOS substrate with RFICs or a silicon-on-insulator (SOI) process with switches for a low cost and small size. The silicon devices have drawbacks of a low breakdown voltage, no back via to the ground, a high knee voltage, and a large substrate loss. Even if the SOI process overcomes the substrate loss issue with a high-resistivity insulator beneath the buried oxide, the other issues must be taken care of in the circuit level as in the bulk CMOS process [1]–[4]. A cascode structure provides a solution for the low breakdown voltage [5], [6]. A differential structure creates a virtual ground point and releases the source degeneration effect by the source-to-ground bonding wires [7]. The use of an output transformer helps to handle the substrate issues and the voltage combination increases the output load impedance of transistors also. Here, in this paper, an on-chip transformer is used to minimize the size and external components and utilized 2nd harmonic short circuits properly for a high efficiency and linearity at the same time. Before starting circuit-level design of a CMOS PA, there is an essential thing to do, layout an optimized power cell for high linearity, efficiency, and output power [8]–[12]. However, the power cell design for a CMOS device is tougher than that of GaAs's because of its lower power density.

As mentioned earlier, in addition to reducing the size and cost, improving the efficiency of the PA at a back-off power is also a hot issue. There has been lots of effort to improve the efficiency at the back-off power region for amplification of a signal with a high PAPR. The Doherty technique modulates the load impedance using a quarter-wavelength transformer for high efficiencies at the back-off power and the peak power [14], [15]. A reconfigurable output matching network according to the power level is also a good candidate for the high PAPR signals [16]. However, these techniques require complex output matching

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B. Park and Y. Cho are with the Division of Information Technology Convergence Engineering (ITCE), Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk 790-784, Korea.

D. Kim is with Samsung System LSI Business, Gyeonggi-do 445-330, Korea.

S. Kim, J. Kim, S. Jin, K. Moon, and B. Kim are with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk 790-784, Korea (e-mail: bmkim@postech.ac.kr).

D. Kang is with the Broadcom Corporation, Matawan, NJ 07747 USA.

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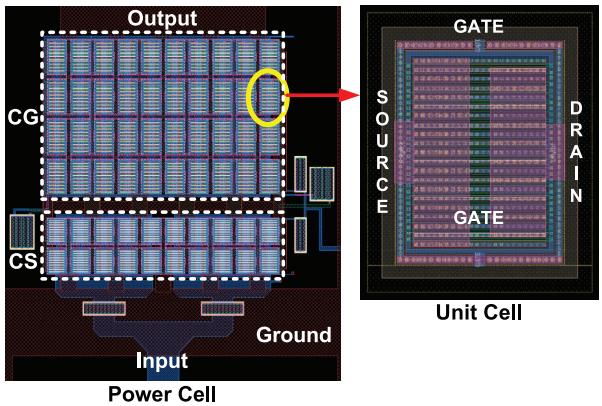


Fig. 1. Layout of a cascode structure power cell with an enlarged unit cell.

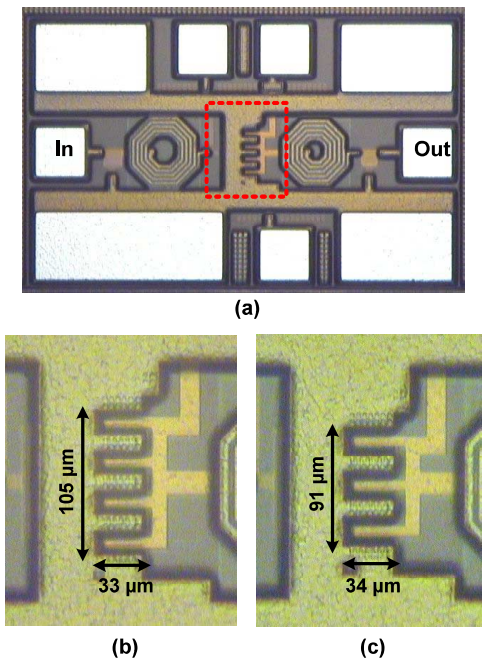


Fig. 2. (a) 8-μm gate-width cell with on-wafer probe test pattern. (b) 8-μm gate-width cell; each unit cell has 15 fingers and 16 unit cells are combined. (c) 10-μm gate-width cell; each unit cell has 16 fingers and 12 unit cells are combined.

networks, which generate a large loss and prevent a large bandwidth (BW) operation. Envelope tracking (ET) improves the efficiency by modulating the PA's supply voltage. The ET technique enables a linear operation by utilizing a linear PA and supply modulator without an additional linearization technique [17]. Thus we have chosen ET technique to improve the PA's performance and proposed a new supply modulator, which provides higher efficiency for CMOS PAs with a high knee voltage.

This paper is organized as follows. Section II presents the optimization of the CMOS power cell. The analysis of 2nd harmonic shorts to improve efficiency as well as linearity has been explained in Section III. In Section IV, an improved structure of the ET supply modulator for high knee voltage CMOS PAs have been introduced. Section V is the implementation of the proposed PA and supply modulator and experimental results. Finally, conclusions of this work are summarized in Section VI.

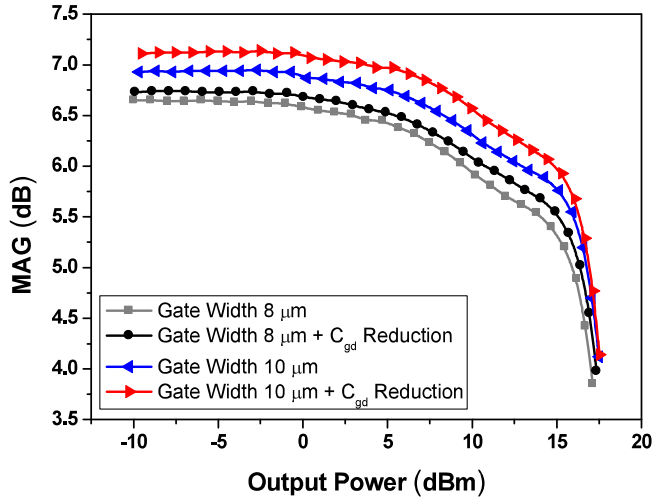


Fig. 3. On-wafer measurement result; optimizing the gate width and structure.

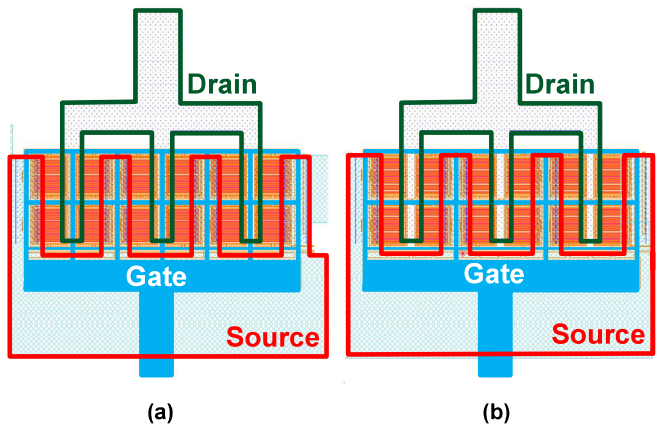


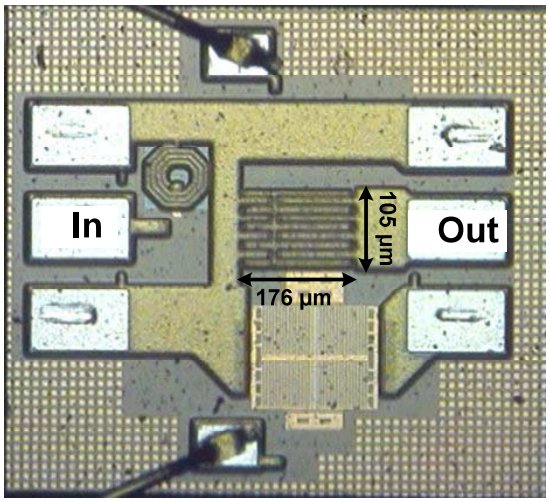
Fig. 4. (a) Original structure; gate feeding line overlapped with both the drain and source. (b) Modified structure; gate feeding line overlapped only with the source.

II. CMOS Power Cell Optimization for High-Performance PA

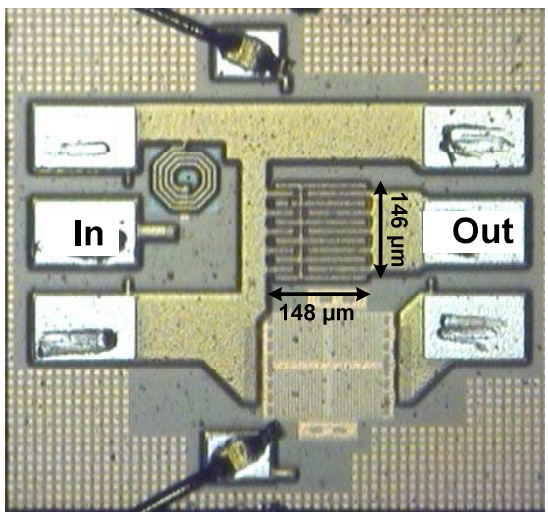
The first step of designing a high-performance PA is a proper power cell design. Without a well-designed power cell, it is impossible to achieve a high-performance PA, regardless of the substrate that is used [8]–[12]. In [13], optimization of gate width and number of fingers for a high-performance 0.5-W CMOS PA has been dealt. Here, we also looked at the gate width and fingers for optimization of the unit cell. However, additional cell optimization should be considered for the output power over 1 W.

Due to low power density of the CMOS device, its power cell should be designed in a large size. As shown in Fig. 1, the power cell is connected with numerous unit cells. Thus, the layout of the power cell affects a lot of the performance [18]. Since the power cell is huge, phase mismatch between the each unit cell can occur and a lot of unwanted parasitic can be added. Especially the gate-to-drain capacitance ($C_{\rm gd}$) parasitic should be minimized to improve the reverse isolation. When it comes to a high power device, oscillation also becomes an issue. Moreover, the intrinsic $C_{\rm gd}$ is small and it is susceptive to the parasitics.

The first procedure of making a power cell is design of the unit cell as large as possible. Selecting the gate width of the



(a)



(b)

Fig. 5. Layout of the: (a) narrow power cell and (b) wide power cell.

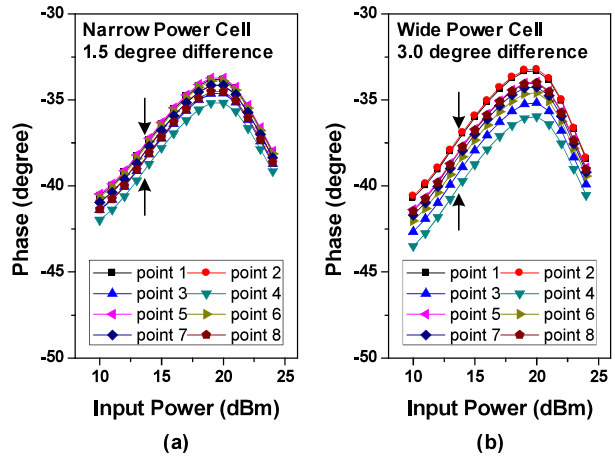


Fig. 6. Simulation results of the phase differences among unit cells. (a) Narrow power cell has the maximum phase difference of 1.5°. (b) Wide power cell has the maximum phase difference of 3°.

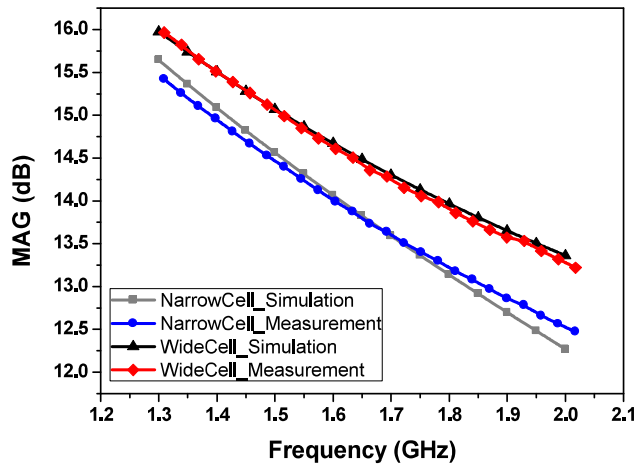


Fig. 7. On-wafer measured MAGs of the narrow and wide power cells.

unit cell is important. A longer gate width of the single unit cell reduces the overall cell size and the number of connections, reducing the parasitics. However, we cannot use a very wide gate because the signal decays exponentially along the poly gate line and cannot modulate the channel properly, degrading the performance. For the compact power cells with a longer gate width, heat dissipation becomes a problem too [11], [12] and the input resistance is larger (1), reducing the voltage gain,

$$r_g = \frac{1}{12}\rho_s \frac{W}{L} \tag{1}$$

where ρ_s is the resistivity of the gate, W is the gate width of the unit cell, and L is the gate length of the unit cell.

We have compared two power cells with 8- and 10-μm unit gate widths, but having the same total gate width of 1920 μm. For the 8-μm gate width cell, each unit cell has 15 fingers and the 16 unit cells are combined. For the 10-μm gate-width cell, each unit cell has 16 fingers and the 12 unit cells are combined. The number of connections are reduced by 20% (fingers $\times$ number of unit cells) for the 10-μm device. Fig. 2 is chip photographs of the two power cell test patterns, and both the 8-μm [see Fig. 2(b)] and 10-μm [see Fig. 2(c)] gate width power cells are designed for on-wafer probe measurement [see Fig. 2(a)]. We have measured the maximum available gain (MAG) and Fig. 3 shows the results, indicating that the 10-μm gate-width cell achieves a higher MAG.

Also the feeding and connection lines have to be carefully drawn to reduce the unwanted parasitics, and so that all unit cells are uniformly fed. As shown in Fig. 4, the gate feeding line is necessary to deliver the signal to the second row. Since the $C_{\rm gd}$ is smaller than the gate-to-source capacitance ($C_{\rm gs}$), additional $C_{\rm gd}$ parasitic from the layout should be minimized. This $C_{\rm gd}$ parasitic contributes to the feedback loop, reducing the gain and stability, and also generates nonlinear distortions. To reduce it, the gate feeding line is overlapped only on the source, as shown in Fig. 4. Fig. 3 clearly shows that by reducing the parasitics on $C_{\rm gd}$, MAG is improved.

After the unit cell is designed, we have optimized the shape of the power cell. Leaving the total gate width equal, the shape of the power cell can be changed (see Fig. 5), vertically spreading mainly affects the phase mismatch and horizontally affects the loss. Two kinds of power cells have been tested. Fig. 5 shows both cells, (a) is aimed to minimize the phase difference among

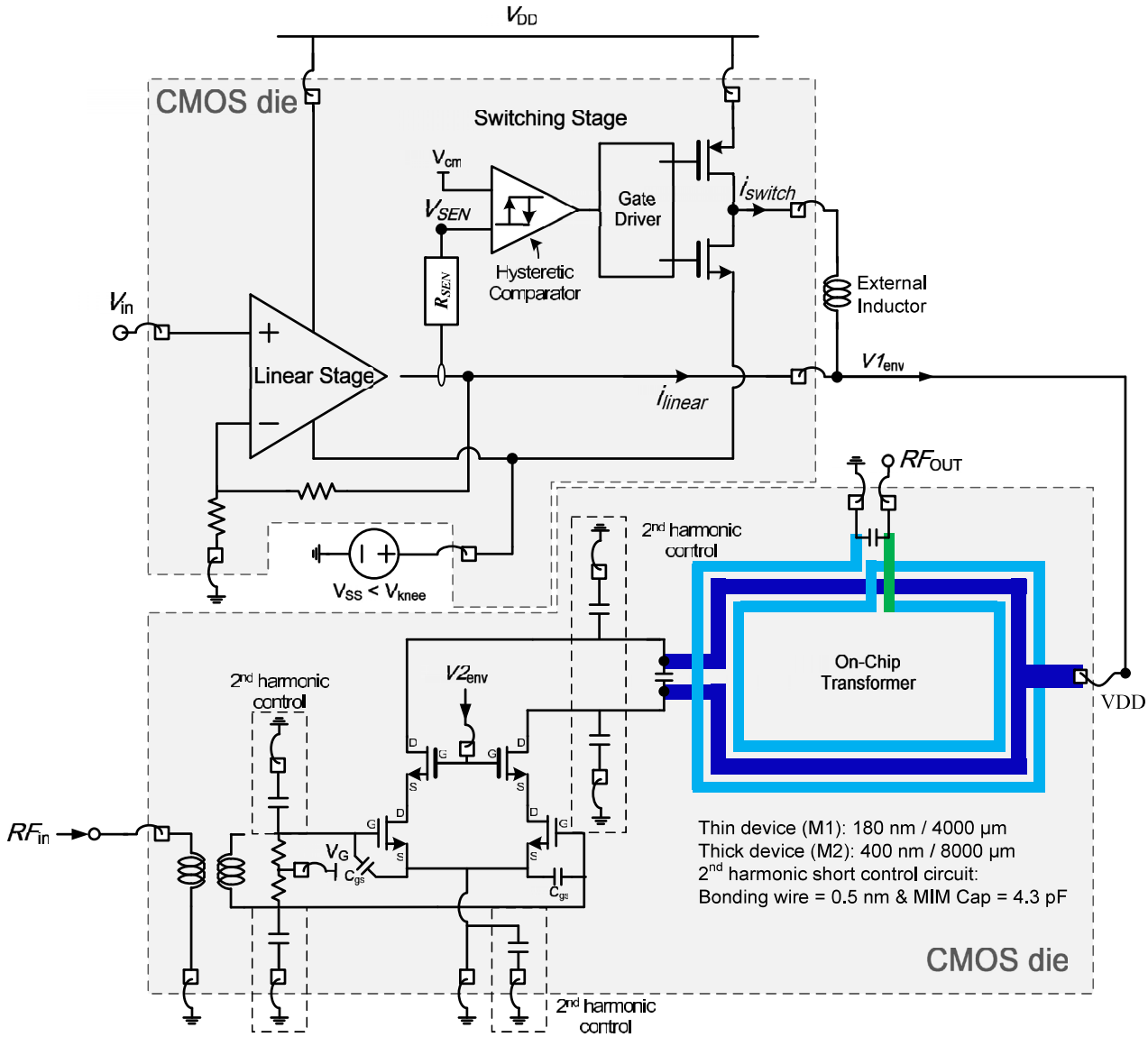


Fig. 8. Schematic of the proposed CMOS ET PA with the supply modulator.

each unit cells and (b) is aimed to minimize the loss of feeding lines. The simulation results in Fig. 6 shows that the phase mismatch difference between the two samples is minimal with mismatch of less than 3°, where points 1–8 in Fig. 6 are random points on the unit cells' gate in each power cell. This means that we can use a wide and short power cell. The length has reduced 20%, 176–148 μm. The measurement result verifies that the wider cell achieves larger MAG, as shown in Fig. 7.

Through these procedures, we finally design an optimized power cell for the high-power PAs. This power cell has been used in the CMOS PA in this paper and has been used also in [19] and [20], achieving high performances.

III. Harmonic Control Circuits to Enhance Linearity and Efficiency of the PA

Fig. 8 is a schematic of the CMOS PA with the ET supply modulator. The PA utilizes a single stage and differential structure to minimize the source degeneration. The 0.18-μm thin-oxide (breakdown voltage: 5 V) and 0.4-μm thick-oxide (breakdown voltage: 9 V) transistors are stacked to create a cascode structure, which releases the breakdown issue. The optimized CMOS power cell designed in Section II has been used. In addition, to enhance the efficiency and linearity of the PA, 2nd harmonic shorts are employed.

In [21], authors have tested the effect on linearity of the 2nd harmonic short circuits at various nodes and showed that either node, gate or source, can improve the linearity. The previous papers [6], [22], [23] focused on a single node, gate of the common-source (CS) transistor, to improve only the linearity performance of the CMOS PA. These previous papers clearly state that the 2nd harmonic short at either gate or source, or at both nodes improve linearity. On that premise we focus on the effect on efficiency by the 2nd harmonic short circuits.

For high efficiency, a class-F-like output matching is employed [24]. In the operation, the current waveform is positive half-sinusoidal, having fundamental, and in-phased 2nd harmonic components and the voltage is rectangular, having

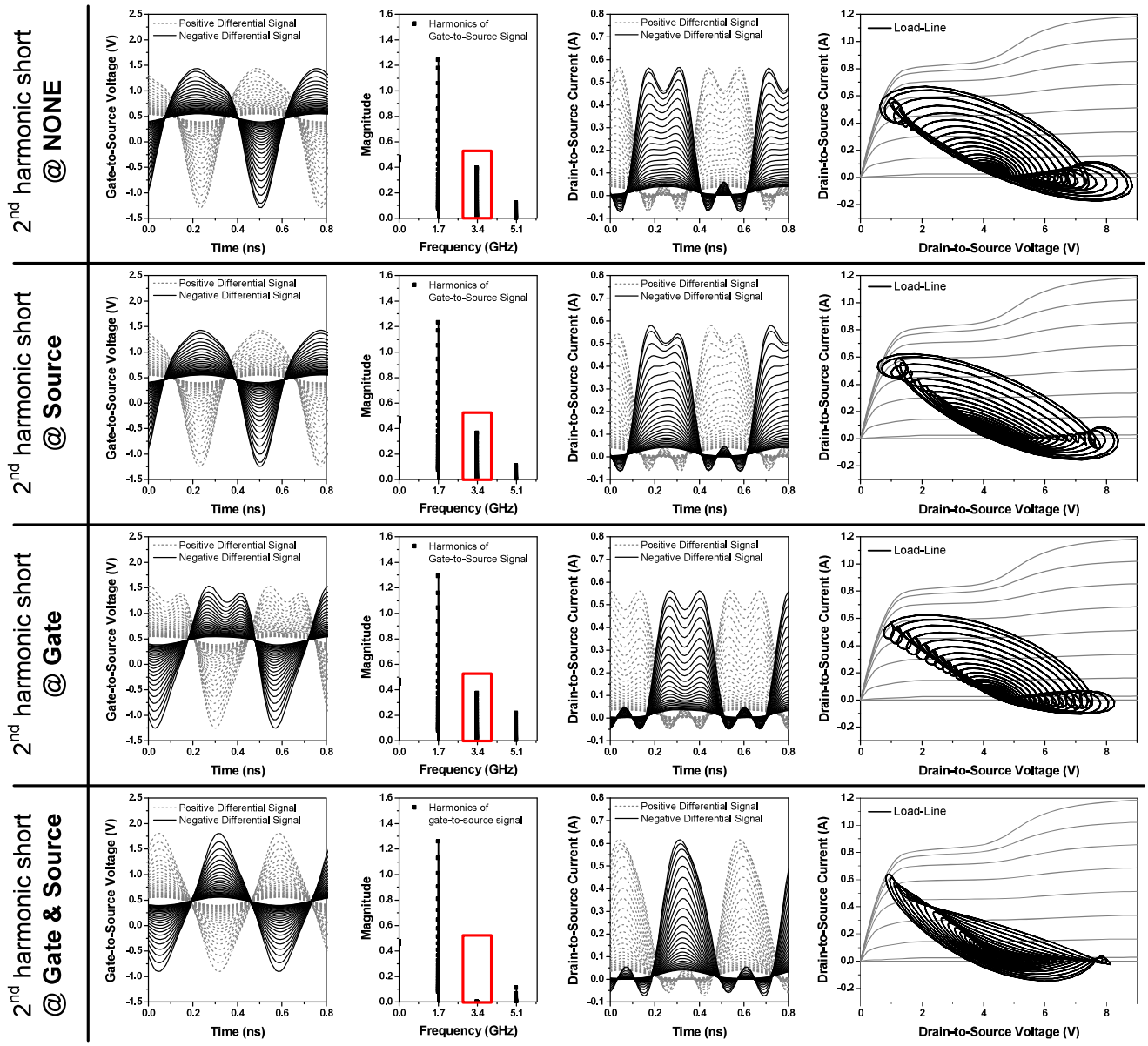


Fig. 9. Simulated $V_{\rm gs}$ waveforms, $V_{\rm gs}$ harmonics, $I_{\rm ds}$ waveforms, and loadlines of the PAs with different 2nd harmonic short circuits. All have an identical ideal output transformer and output 2nd harmonic short circuit.

fundamental and in-phased 3rd harmonic components. The input voltage waveform derives the output current waveform, and a proper harmonic control at the input is necessary. The effect on the input harmonic termination in HBT has been reported in [25]. In a class-F operation, the out-phased 2nd harmonic should be minimized in the gate voltage, which reduces the in-phased output 2nd harmonic current generation and efficiency. This out-phased 2nd harmonic at the input is generated by a nonlinear $C_{\rm gs}$. The behavior of the output current and voltage is the same for both CMOS and HBT. However, due to the deference in design structures, proper harmonic control for a CMOS PA needs to be investigated. The main difference is that CMOS PA utilizes a differential structure due to absence of a ground via-hole.

In this paper, we fix the output matching and change the output current waveform by the harmonic control at the input to have a high efficiency. Achieving a positive half-sinusoidal output current is the main goal. The CMOS PA is differential, and the common nodes such as the CS transistor's source node is ac shorted for all odd harmonics so the 3rd harmonic does not affect the performance, but even harmonics directly sees the source inductance. Therefore, as shown in Fig. 9 "2*nd* harmonic short @ Gate" row, even though the 2nd harmonic is terminated at the gate, the 2nd harmonic remains at the source node thereby the 2nd harmonic component is still generated at the $V_{\rm gs}$ waveform. This component produces the out-phased 2nd harmonic at the output current, reducing the efficiency. With the 2nd harmonic component at the $V_{\rm gs}$, the input voltage, $I_{\rm ds}$ waveform is rectangular rather than half-sinusoidal. This behavior is similar for the case of the "2*nd* harmonic short @ Source." These two circuits having the 2nd harmonic short circuits either at the gate or source improve in linearity [6], [21]–[23], but not the efficiency.

In the "2*nd* harmonic short @ Gate & Source" row in Fig. 9, all 2nd harmonics are terminated at the gate and source, without

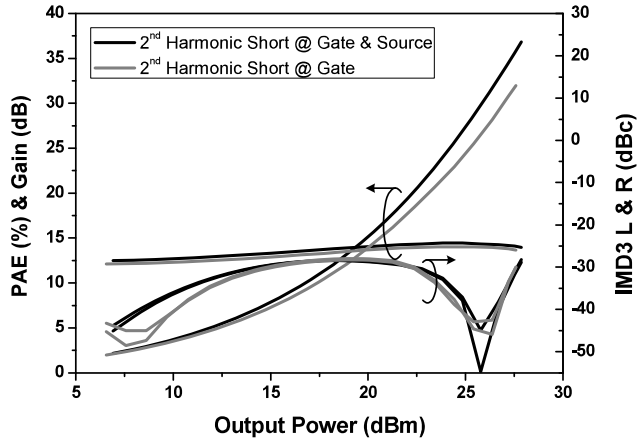


Fig. 10. Two-tone simulation results of two types of PAs. All have an identical ideal output transformer and output 2nd harmonic short circuit.

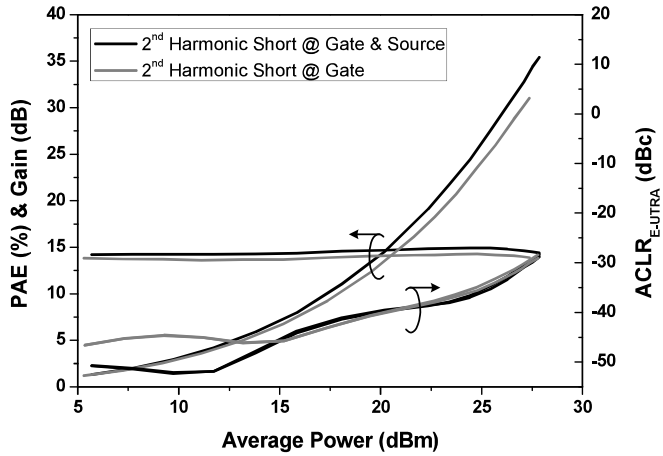


Fig. 11. Measured results of the two types of PAs. All have an identical output on-chip transformer and output 2nd harmonic short circuit. With 10-MHz BW 16-QAM 7.5-dB PAPR LTE signal.

any 2nd harmonic components on the $V_{\rm gs}$ waveform. This $V_{\rm gs}$ waveform is clearly distinguished from the other waveforms, i.e., symmetric and sinusoidal. As a result, an in-phased 2nd harmonic is generated at the output current and $I_{\rm ds}$ waveform is now half-sinusoidal, having lower conduction angel than that of the rectangle waveform. Due to the lower conduction angle, we can achieve higher efficiency. The loadline in Fig. 9 clearly shows that the voltage and current waveforms consume a less power internally.

As shown in [21], the 2nd harmonic short at gate node or source node gave linearity improvement and when the both nodes are shorted for 2nd harmonic, the improvement in linearity is even larger. However, as is mentioned in [21] and [26], $C_{\rm gs}$ the nonlinearity effect in linearity is dominant at a low-power region. As the power level increases, gm distortion can be dominant. When the $C_{\rm gs}$ nonlinearity is compensated by either the gate or source 2nd harmonic short and gm distortion becomes dominant, the linearity cannot be improved further by the two 2nd harmonic shorts. This is why we achieve similar linearity for both circuits in Fig. 10.

We compare the efficiency with the two circuits, one with the 2nd harmonic short at the gate and the other at both the gate and source. Fig. 10 shows the results that there are not much difference in linearity, but 4% higher efficiency at the peak output power. Measurement results with a 10-MHz BW 16-QAM 7.5-dB PAPR LTE signal are also depicted in Fig. 11. The measurement results show 3% higher efficiency at the peak average power. By applying the 2nd harmonic short circuits at the source and gate of the CS transistors, we have improved both efficiency and linearity at the same time.

IV. Improved ET Supply Modulator for CMOS PA With a High Knee Voltage

The ET system's merit is that the efficiency increases not only at the back-off region, but also at the peak power operation for amplifying a signal with a large PAPR. The ET system achieves the high efficiency by replacing the fixed dc supply with the dynamic supply voltage, which closely tracks the envelope of the transmitted RF signal. However, efficiency of the supply

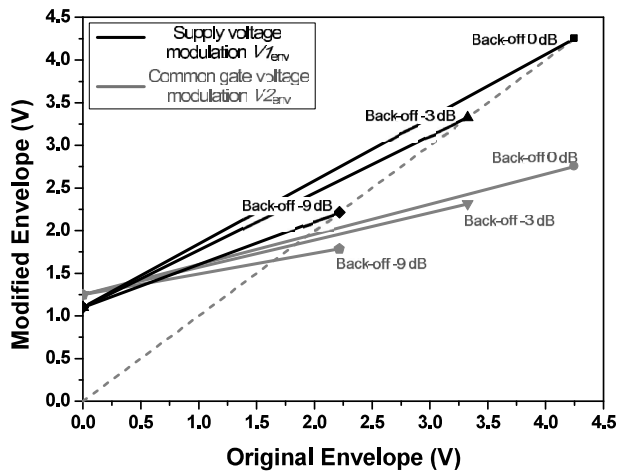


Fig. 12. Modified envelope shaping for the drain and the gate of the CG transistor.

TABLE I
Power Dissipation Comparison Summary Between Proposed and Conventional Supply Modulators

Envelope Output Voltage 1.1 ~ 3.0 V	$P_{diss.,S.M}$	=	$P_{dc,S.M.}$	–	$P_{out,S.M.}$
Proposed	125 mW	=	540 mW	–	415 mW
Conventional	145 mW	=	560 mW	–	415 mW

*S.M.: Supply Modulator

modulator should be high to get the enhanced overall efficiency. Total efficiency of the ET system can be derived as follows:

$$\eta_{\rm Total} = \eta_{\rm PA} \times \eta_{\rm SupplyModulator}. \quad (2)$$

In this paper, we propose an improved supply modulator suited for the CMOS PA. Most of the ET systems have been applied to GaAs HBT PAs due to its popularity in real handset implementation. However, by steadily improved performance and integration capability of the CMOS PA, the ET system on a CMOS PA becomes a hot issue. An important difference in characteristic between the CMOS and HBT PAs is the knee

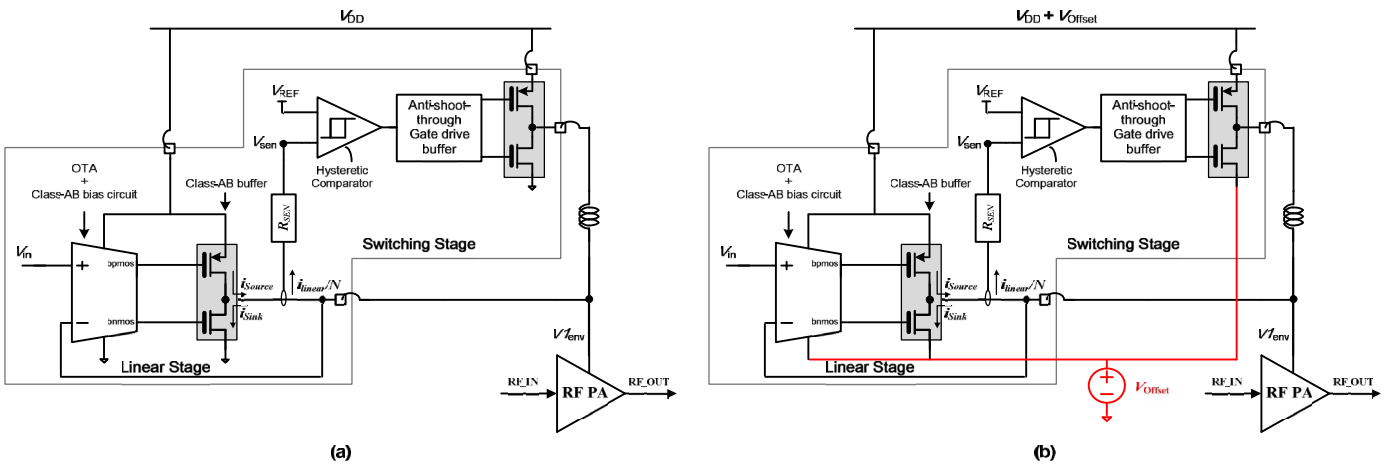


Fig. 13. (a) Schematic of the conventional ET supply modulator. (b) Schematic of the proposed nonzero V_{SS} ET supply modulator.

TABLE II
POWER DISSIPATION SUMMARY BETWEEN PROPOSED AND CONVENTIONAL MODULATOR'S LINEAR STAGES

Envelope Output Voltage 1.1 ~ 3.0 V	$P_{diss.,Linear}$	=	$\overline{(V_{DD}+V_{Offset}-V_{Out})\times I'_{Source}}$	+	$\overline{(V_{Out}-V_{Offset})\times I'_{Sink}}$	$\overline{I_{Source}}$ / $\overline{I_{Sink}}$
Proposed	93 mW	=	42 mW	+	51 mW	18.46 / 51.25
Conventional	114 mW	=	60 mW	+	54 mW	36.32 / 32.26

voltage. The CMOS PA's knee voltage is almost twice larger than the GaAs HBT PAs, which is about 1 V, due to the cascode structure. For the optimum operation of the ET system, the envelope is reshaped to follow the sweet spot of the IMD3, as shown in Fig. 12 [27]. The sweet spot tracking ET PA compensates the nonlinear distortions of the PA and achieves higher linearity; this is well described in [27] and [28]. The minimum value of the envelope is slightly larger than the knee voltage of the PA. For the HBT PAs, the minimum voltage of the shaped envelope is about 0.5 V, which is similar to the minimum voltage the supply modulator can provide, due to the voltage drop through the NMOS at the buffer of the linear stage. For the CMOS PA, however, additional offset is needed.

We propose a new supply modulator architecture to provide the additional offset needed for the CMOS PA. Fig. 13(a) shows the conventional supply modulator and (b) is the proposed modulator. The grounds of the proposed modulator's linear and switching stages are connected to a dc supply with a supply voltage equivalent to the additional offset voltage.

The I/O device has a voltage drop of about 0.4 V. Hence, the maximum voltage swing of the conventional supply modulator is 0.4 V $\sim$ 3.6 V when V_{DD} is 4.0 V. Since the CMOS PA has a high knee voltage of about 1.1 V, the envelope should be shaped to cover the envelope output voltage of 1.1 V $\sim$ 3.6 V. The voltage swing range of the modulator (0.4 V $\sim$ 3.6 V) is larger than the necessary range, and the efficiency is not optimal for the envelope shaping. To optimize the efficiency, 0.7-V offset voltage is added to the ground of the supply modulator. In that way, the 0.7-V portion of the output voltage is generated by the voltage generator with high efficiency. To maintain the rail-to-rail voltage of 4 V, V_{DD} of the proposed modulator is also increased to 4.7 V. Now the maximum voltage swing range for the supply modulator is 1.1 V $\sim$ 4.3 V. Since the minimum envelope output voltage is higher than the CMOS PA's knee voltage, the maximum swing can be used, achieving higher efficiency and output power than the conventional one.

The efficiency of the supply modulator can be defined as follows:

$$\eta_{\mathrm{S.M.}} = \frac{P_{\mathrm{Out,S.M.}}}{P_{\mathrm{dc,S.M.}}} \tag{3}$$

$$P_{\mathrm{diss.,S.M.}} = P_{\mathrm{dc,S.M.}} - P_{\mathrm{Out,S.M.}} \tag{4}$$

$$P_{\mathrm{diss.,S.M.}} = P_{\mathrm{diss.,Linear}} + P_{\mathrm{diss.,Switch}} \tag{5}$$

where $P_{\mathrm{Out,S.M.}}$, $P_{\mathrm{dc,S.M.}}$, and $P_{\mathrm{diss.,S.M}}$ are the output power, dc power, and dissipated power of the supply modulator, and $P_{\mathrm{diss.,Linear}}$ and $P_{\mathrm{diss.,Switch}}$ are the dissipated power of the linear stage and switching stage, respectively. Most of the internal power consumption has occurred at buffer of the linear regulator and switching, the grey colored boxes in Fig. 13.

Table I shows the values of the parameters in (4), when both supply modulators have the same envelope voltage range of 1.1 $\sim$ 3.0 V. As expected, the proposed supply modulator dissipates lower power than the conventional one.

At the linear stage, the class-AB buffer consumes most of the power, and the power consumption of the conventional modulator can be expressed as follows:

$$P_{\mathrm{diss.,Linear}} = \overline{(V_{DD} - V_{\mathrm{Out}}) \times I_{\mathrm{Source}}} + \overline{V_{\mathrm{Out}} \times I_{\mathrm{Sink}}} \tag{6}$$

where V_{DD} is the supply voltage of the supply modulator, V_{Out} is the output voltage of the supply modulator. I_{Source} and I_{Sink} are the dissipated currents in the PMOS and NMOS of the class-AB buffer, respectively. By providing the additional dc

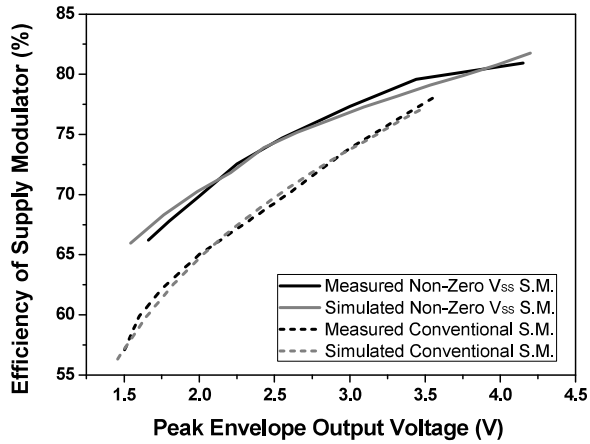


Fig. 14. Simulated and measured efficiencies of the conventional and proposed supply modulators with a fixed load. (Supply modulator: S.M.)

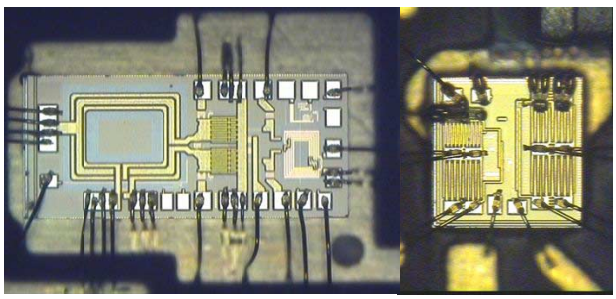


Fig. 15. Chip microphotographs of the CMOS ET PA and the supply modulator.

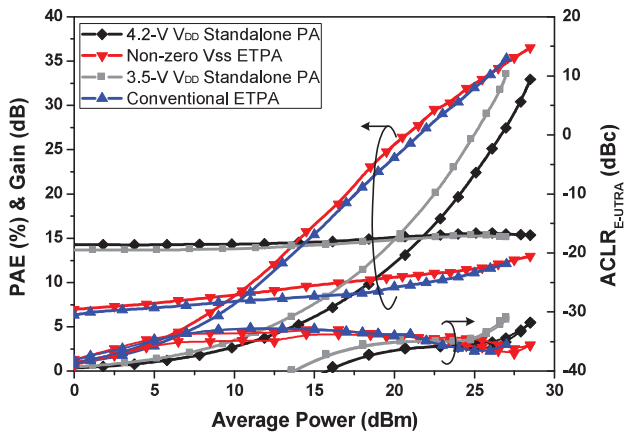


Fig. 16. Measured performance comparison between the conventional ET PA and the proposed ET PA at 1.70 GHz for a 10-MHz BW, 16-QAM, 7.5-dB PAPR LTE signal.

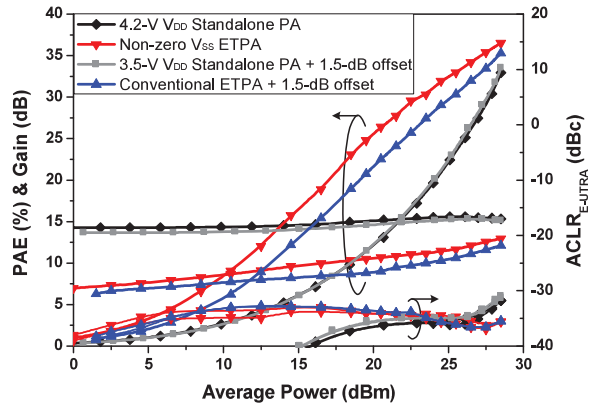


Fig. 17. Measured performance comparison between the conventional ET PA with 1.5-dB output power offset and the proposed ET PA at 1.70 GHz for a 10-MHz BW 16-QAM 7.5-dB PAPR LTE signal.

TABLE III
PERFORMANCE COMPARISON SUMMARY BETWEEN CONVENTIONAL AND PROPOSED ET PAS

	Standalone PA Vdd 3.5 V / 4.2 V	Conventional ET PA	Non-zero V_{SS} ET PA
PAE @ Peak Output Power	33.5% / 33.0%	35.3%	**36.6%**
PAE @ -10 dB Back-off Power	10% / 10%	19%	**23%**
ACLR @ Peak Output Power	-31.0 dBc / -31.8 dBc	-35.5 dBc	**-35.6 dBc**

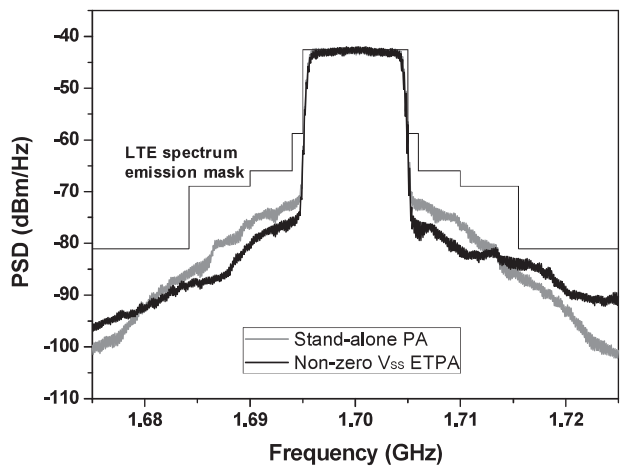


Fig. 18. Measured spectra of the PA at an average output power of 28.5 dBm for the 10-MHz BW 16-QAM 7.5-dB PAPR LTE signal.

offset voltage, V_{Offset}, at the ground of the linear and switching stages, the $P_{\mathrm{diss.,Linear}}$ is changed as

$$P_{\mathrm{diss.,Linear}} = \overline{((V_{DD}+V_{\mathrm{Offset}})-V_{\mathrm{Out}})\times I'_{\mathrm{Source}}} + \overline{(V_{\mathrm{Out}}-V_{\mathrm{Offset}})\times I'_{\mathrm{Sink}}} \quad (7)$$

where I'_{Source} and I'_{Sink} are the sourcing and sinking currents of the proposed modulator, respectively. The switching stage in the conventional module provides the average current. Therefore, the sinking and sourcing currents should be the same level. When the V_{DD} and the ground of the switching stage are increased by the offset voltage, the switching current (I_{SW}) increases since the voltage across the inductor is shifted by the offset voltage. Therefore, the sinking current should be increased by the same amount and the sourcing current is reduced by the comparable amount. The voltage across the sourcing PMOS is larger than that across the sinking NMOS. Therefore, the power consumption is reduced. Table II shows the detail values for (7).

The direct comparison between the two modulators cannot be made due to the difference in the peak envelope output voltage. However, still, it could clearly prove that the proposed structures achieves higher efficiency than the conventional version, especially at a low power operation, at the same voltage range. The measurement and simulation for the efficiency are shown in Fig. 14. The ET supply modulator is measured with a fixed

TABLE IV
COMPARISON OF THE ET PA MODULE WITH THE STATE-OF-THE-ART PAS

		[30]	[31]	[32]	[33] Commercial Avago PA	[34] ET PA	[35] ET PA	Previous Work [6]		This Work	
								Standalone PA	ET PA	**Standalone PA**	**ET PA**
Technology		0.18 μm CMOS	0.18 μm CMOS	90 nm CMOS	InGaP HBT	0.35 μm SiGe BiCMOS	65 nm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Frequency (GHz)		2.40	1.95	0.93	0.707	1.90	2.40	1.85	1.85	**1.70**	**1.70**
Application	CH BW (MHz)	20	3.84	10	10	5	20	10	10	**10**	**10**
	PAPR (dB)	-	3.5	6.9	-	7.5	~10	7.5	7.5	**7.5**	**7.5**
	Modulation	64QAM WLAN	QPSK WCDMA	16QAM LTE	LTE	16QAM LTE	64QAM WLAN	16QAM LTE	16QAM LTE	**16QAM LTE**	**16QAM LTE**
Supply (V)		3.3	3.4	2	3.4	5.5	1.2	3.5 / 4.5	5	**3.5 / 4.2**	**4.7**
Pavg (dBm)		23.5	28	25.1 / 26	27.5	26.1	22.7	23.8 / 26	26	**27 / 28.5**	**28.5**
PAE (%) @ Pavg		~13	36.4	15 / 17	37.1	35	-	31.8 / 31.2	34.1	**33.5 / 33**	**36.6**
PAE (%) @ P_{-10dB}		-	10*	5*	-	10*	-	9	12.5	**10**	**23**
ACLR (dBc)		-	-35	-	-36	-	-	-32.5 / -32	-34.2	**-31 / -31.8**	**-35.6**
EVM (%)		5.62	-	5.62	-	4.2	5	3.2 / 3.97	2.8	**4.62 / 4.4**	**3**
Silicon Area (mm x mm)		2.1 x 1.64	2.0 x 1.3	1.8 x 1.85	-	1.5 x 1.1	1.1 x 1.2	0.77 x 0.95	0.77 x 0.95, 1.3 x 1.3	**0.78 x 1.80**	**0.78 x 1.80, 0.75 x 0.80**
Output Matching Network		On-Chip	On-Chip	On-Chip	Off-Chip	Off-Chip	Off-Chip	Off-Chip	Off-Chip	**On-Chip**	**On-Chip**

*Graphically estimated.

7.8-Ω resistor at the output. The envelope shaping for the conventional modulator is modified to have a voltage swing range from 1.1 to 3.5 V and for the proposed version it is modified to have a range of 1.1 to 4.2 V. The peak efficiency of the proposed structure is 81.5%, 4.0% improvement from the conventional version efficiency, 77.5%. The efficiency improvement at the back-off envelope is even larger, about 10% point. The improvement at the back-off region is the most attractive characteristic of this modulator. Even with the dc/dc converter having an efficiency of 80% [29], proposed supply modulator outperforms the conventional supply modulator.

V. IMPLEMENTATION AND MEASUREMENT RESULTS

The proposed differential cascode CMOS PA and ET supply modulator are fabricated in a 0.18-μm RF CMOS technology. They are 0.78 mm $\times$ 1.80 mm and 0.75 mm $\times$ 0.80 mm in sizes, respectively. Chip micrographs of the fabricated PA and supply modulator are presented in Fig. 15. For measurement, the both chips are mounted on a FR-4 printed circuit board (PCB). The 2nd harmonic short circuits are implemented by connecting a 4.3-pF metal–insulator–metal (MIM) capacitor and a 0.5-nH bond-wire to minimize the loss and size. The output transformer is integrated on the chip to minimize the size and external components. A 1:2 transmission-line transformer (TLT) is employed, as shown in Fig. 8. Its insertion loss including two matching capacitors is 1.10 dB at 1.70 GHz. To maximize the efficiency, an external PCB transformer can be used [6], [20], [22], [23] since the insertion loss is about 0.5 dB lower, leading to 5% higher efficiency [20].

The fabricated ET PAs are measured using an LTE signal with 10-MHz BW 16-QAM 7.5-dB PAPR LTE signal at 1.70 GHz. Fig. 16 shows the four measurement results, standalone PA with 3.5-V V_{DD}, conventional ET PA, standalone PA with 4.2-V V_{DD}, and the nonzero V_{SS} ET PA. Here all four PAs utilize the 2nd harmonic control at the gate and source of the CS transistors and at the drain of the common-gate (CG) transistors for maximum performance. The 3.5-V V_{DD} standalone PA has a PAE of 33.5% and an $\mathrm{ACLR}_{\mathrm{E-UTRA}}$ of -31 dBc at an average output power of 27 dBm. A conventional ET supply modulator is applied to the 3.5-V V_{DD} PA. With the conventional modulator, the performance increases to a PAE of 35.3% and an $\mathrm{ACLR}_{\mathrm{E-UTRA}}$ of -35.5 dBc at an average output power of 27.0 dBm. The 4.2-V V_{DD} standalone PA has a PAE of 33.0% and an $\mathrm{ACLR}_{\mathrm{E-UTRA}}$ of -31.8 dBc at an

average output power of 28.5 dBm. With the proposed nonzero V_{SS} ET supply modulator, the performance increases to a PAE of 36.6% and an $\mathrm{ACLR_{E-UTRA}}$ of -35.6 dBc at an average output power of 28.5 dBm. As expected, the nonzero V_{SS} ET PA delivers a better efficiency across the all power level and significantly higher efficiency at a low power region compared to the conventional ET PA. However, the differences at the same output powers are small in this measurement (Fig. 16) because the proposed modulator operates at a low efficiency region, compared to the conventional one. By changing the V_{DD} from 3.5 to 4.2 V, the PA generates about 1.5 dB more power. To see efficiency improvement of the modulator, the maximum average output powers of the two ET PAs are matched by giving the 1.5-dB offset to the conventional version, as shown in Fig. 17. Now since the two PA's efficiencies are almost the same, the efficiency improvement of the modulator can be seen directly. This figure clearly shows that the proposed modulator is more efficient at the maximum average output power and more significantly at a back-off powers. The efficiency with the proposed modulator is improved by 1.8% point at the peak power compared to that of with the conventional ET supply modulator. At a 10-dB back-off power, the conventional ET supply modulator improves efficiency from 10% to 19% (9% improvement) over the standalone PA, and for the proposed version the efficiency improves from 10% to 23% (13% improvement). The comparison summary can be seen in Table III.

Fig. 18 depicts the measured spectra of the PAs at an output power of 28.5 dBm for the LTE signal, satisfying the system specification. The $\mathrm{ACLR_{E-UTRA}}$ is measured with a 9-MHz resolution BW at both a center frequency and a 10-MHz offset. The measured error vector magnitude (EVM) of the 4.2-V V_{DD} standalone PA and nonzero V_{SS} ET PA are 4.4% and 3.0%, respectively.

Table IV shows a comparison of the ET PA module with the state-of-the-art PAs. The proposed ET PA outperforms the CMOS PAs in terms of linearity and efficiency. With the optimized power cell, the proper harmonic control, and the nonzero V_{SS} ET supply modulator, the performance surpasses our previous work [6]. This performance is also competitive to the commercial InGaP HBT PA [33] and the SiGe BiCMOS ET PA [34] for LTE applications.

VI. Conclusion

The CMOS power cell has been optimized to maximize performance of the PA. To address the inferior CMOS process, the differential cascode structure is also adopted to reduce the degeneration effect of bonding wires at the source of the CS amplifier and to enhance the low breakdown voltage through the two transistors. A new type of output matching network, which is a PCB transformer embedded underneath the PA chip, has been proposed in this paper to maximize the performance and minimize size of the PA module. It has been proven by the simulations and measurements that the proposed PCB transformer can be successfully mounted underneath the PA chip die. To show the usefulness of the proposed PCB transformer, a 2.0 mm $\times$ 2.5 mm CMOS PA module has been developed for LTE application. The output matching loss has been improved significantly by the off-chip transformer, compared to the on-chip TLT. RF characteristics have not been degraded by using the PCB transformer underneath the PA chip die. The proposed approach can also be applied to other types of wireless applications requiring a differential-to-single transformer with compact size and high performance.

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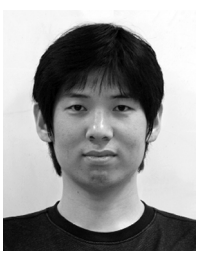
Byungjoon Park received the B.S. degree in electrical engineering from Hanyang University, Seoul, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea.

His main interests are CMOS RF circuits for wireless communications, especially highly efficient and linear RF transmitters and RF power amplifier (PA) design.

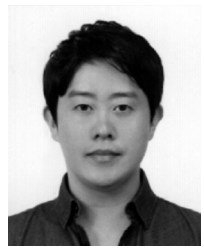


Dongsu Kim received the B.S. and Ph.D. degrees in electronic and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea, in 2007 and 2013, respectively.

He is currently with the Samsung System LSI Business, Gyeonggi-do, Korea. His research interests are CMOS RF circuits for wireless communications with a special focus on highly efficient and linear RF transmitter design.

Seokhyeon Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea, in 2011, and is currently working toward the Ph.D. degree in POSTECH.

His current research interests include highly linear and efficient RF power-amplifier design.

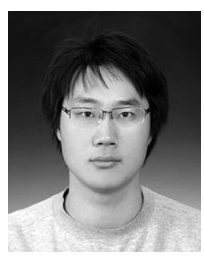


Yunsung Cho received the B.S. degree in electrical engineering from Hanyang University, Ansan, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea.

His main interests are RF circuits for wireless communications, especially highly efficient and linear RF transmitters and RF power-amplifier design.

Jooseung Kim received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea, in 2010, and is currently working toward the Ph.D. degree in electrical engineering at POSTECH.

His research interests are CMOS RF circuits for wireless communications, especially focused on highly efficient and linear RF transmitter design.



Daehyun Kang received the B.S. degree in electronic and electrical engineering from Kyungpook National University, Daegu, Korea, in 2006, and the Ph.D. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea, in 2012.

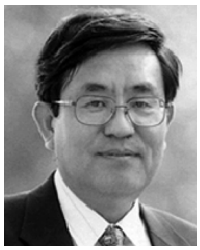
He is currently with the Broadcom Corporation, Matawan, NJ, USA. His research interests include the design of PAs and highly efficient and linear transmitter.

Sangsu Jin received the M.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea, in 2005 , and is currently working toward the Ph.D. degree at POSTECH.

From 2005 to 2011, he was with LG Electronics, Seoul, Korea, where he designed the low-noise amplifier for digital TV tuner integrated circuit (IC) and high-speed serial/parallel links and all-digital phase-locked loop (PLL) circuits for display interfaces. His research interests include RF power amplifiers (PAs) and CMOS RF/analog ICs.

Kyunghoon Moon received the B.S. degree in electrical engineering from Hanyang University, Ansan, Korea, in 2012, and is currently working toward the Ph.D. degree in electrical engineering at the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea.

His main interests are RF circuits for wireless communications, especially highly efficient and linear RF transmitters and RF PA design.



Bumman Kim (M'78–SM'97–F'07) received the Ph.D. degree in electrical engineering from Carnegie Mellon University, Pittsburgh, PA, USA.

He joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power field-effect transistors (FETs) and monolithic microwave integrated circuits (MMICs). He has developed a large-signal model of a power FETs, dual-gate FETs for gain control, high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Pohang, Gyeongbuk, Korea, where he is a POSTECH Fellow and a Namko Professor with the Department of Electrical Engineering, and Director of the Microwave Application Research Center. He is involved in device and circuit technology for RF integrated circuits (RFICs) and power amplifiers. He has authored over 400 technical papers.

Prof. Kim is a Member of the Korean Academy of Science and Technology and the National Academy of Engineering of Korea. He was an Associate Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, a Distinguished Lecturer of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), and an Administrative Committee (AdCom) Member.