

NB-IoT and GNSS All-In-One System-On-Chip Integrating RF Transceiver, 23-dBm CMOS Power Amplifier, Power Management Unit, and Clock Management System for Low Cost Solution

Jongsoo Lee^D, Jaeyeol Han, Chi-Lun Lo, Jongmi Lee, Wan Kim, *Student Member, IEEE*, Seungjin Kim, Byoungjoong Kang, Juyoung Han, Sangdon Jung, Takahiro Nomiya, Jongwoo Lee, *Senior Member, IEEE*, Thomas Byunghak Cho, *Senior Member, IEEE*, and Inyup Kang

Abstract—This article presents a fully integrated stand-alone narrowband Internet-of-Things (NB-IoT) and global navigation satellite system (GNSS) system-on-chip (SoC). It aims for an all-in-one system to integrate all necessary blocks such as an RF transceiver, a power management system (PMIP), and a clock management system and to save a bills-of-material (BOM) cost. An RF transceiver is integrated to support multi-band cellular IoT and GNSS with a CMOS RF power amplifier transmitting 23-dBm output power. A PMIP, including bucks, a boost, and low-dropout regulators (LDOs), is integrated to support coin cell or AAA battery and to support a wide input supply voltage range from 2.5 to 5 V. In addition, clock management system is embedded with a digitally controlled crystal oscillator (DCXO), a relaxation oscillator (RCO), and temperature sensor units (TSUs). It is fabricated in a standard 28-nm CMOS process and its size is 24.6 mm². The power consumption of always-on-block is 15 μ W, and the sleep current consumption is less than 10 μ A at 3.8 V.

Index Terms—All-digital phase-locked loop (ADPLL), analog baseband (ABB), analog baseband transformer (ABX), analog-to-digital converter (ADC), buck-booster, clock management, CMOS, digitally controlled crystal oscillator (DCXO), global navigation satellite system (GNSS), low-dropout regulator (LDO), narrowband Internet-of-Things (NB-IoT), power amplifier (PA), power management, real-time-clock (RTC), receiver (RX), relaxation oscillator (RCO), RF, synthesizer, system-on-chip (SoC), temperature compensated crystal oscillator (TCXO), temperature sensor unit (TSU), transceiver, transmitter (TX).

I. INTRODUCTION

HERE is growing demand for a low-power and low-cost system-on-chip (SoC) and a massive number of wireless devices due to extensive application prospects and huge market potential of narrowband Internet-of-Things (NB-IoT). Since IoT market demands massive volume, bills-of-material (BOM) cost reduction is very important, and integration is a key factor

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The authors are with the System LSI Business, Samsung Electronics, Hwaseong 445-330, South Korea (e-mail: jongsoo1.lee@samsung.com).

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for low cost. There is a strong demand for tracking service and global navigation satellite system (GNSS) integration is favorable. The most challenging blocks such as an RF transceiver including an RF power amplifier (RF-PA) and a high-power switching converter have to be integrated to remove the use of expensive multi-chip components [1]–[6]. However, integration of an RF-PA and a switching power converter into a CMOS transceiver leads to challenges [7]. An integrated RF-PA can be a high self-interference source for a voltage-controlled oscillator (VCO) in a phase-locked loop (PLL) and switching noise and thermal heating of a switching power converter may affect to sensitive analog and RF performances.

NB-IoT modules only transmit small amounts of infrequent data over long period of time. For longer standby time, the power saving mode (PSM) and the extended discontinuous reception (eDRX) are announced in Rel-12 and Rel-13, respectively. To support power scenarios of NB-IoT, low power circuits and highly efficient power regulators are needed simultaneously [8]. In addition, NB-IoT solution has to consume very low power consumption to fulfill long operation time requirement such as 10-year operation [1], [9]. In order to do so, it requires low power consumption of always-on system and well-defined power control system and clock control system.

A crystal oscillator is a crucial component in mobile devices as accurate reference clocks for wireless communications. While demanding for high accuracy in the oscillation frequency, a crystal oscillator suffers from ambient temperature variations. Thus, a temperature compensated crystal oscillator (TCXO) is inevitable. However, its price and power consumption weaken the competitiveness of products. Therefore, a solution that can replace a TCXO while maintaining frequency accuracy is highly demanded [10]. We propose a TCXO system which uses a low-cost temperature sensing crystal (TSX). In addition, a software-assisted self-calibrating wake-up timer is proposed to ensure the reliable peer-to-peer communication and reduce power consumption during a sleep mode in IoT applications. The proposed timer does not need additional calibration procedures by adjusting a counter value

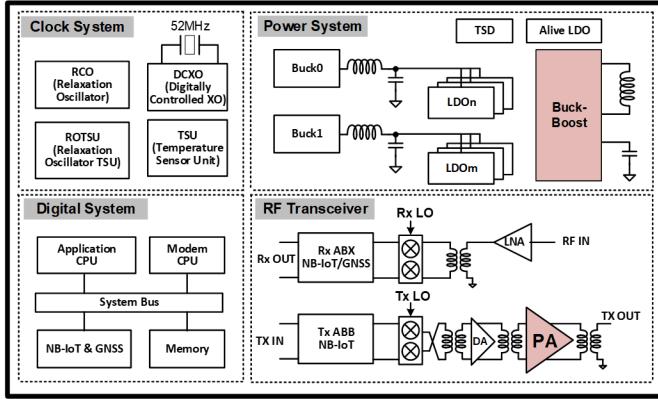


Fig. 1. NB-IoT and GNSS SoC architecture.

from software with respect to process, supply voltage, and temperature (PVT) variations and it reduces test time and costs.

This work aims for an all-in-one system to integrate all necessary blocks to save a BOM cost, as shown in Fig. 1. An RF transceiver is integrated to support multi-band cellular IoT and GNSS with a CMOS RF-PA. A power management system (PMIP), including bucks, a buck-boost, and low-dropout regulators (LDOs), is integrated to support coin cell or AAA battery and to support a wide input supply voltage range from 2.5 to 5 V. In addition, clock management system is embedded with a digitally controlled crystal oscillator (DCXO), a relaxation oscillator (RCO), and temperature sensor units (TSUs) [11] to support a low power operation.

This article is organized as follows. Section II describes the transceiver architecture including CMOS power amplifier (PA). In addition, it describes an innovative RX analog baseband (ABB) architecture that dramatically improves area and power efficiency by transforming its structure up to the signal bandwidth without any extra cost, and thus effectively supports the multi-standard operation. In Section III, a fully integrated PMIP is described. It has a high-power buck-boost (BB) converter for the CMOS PA. To minimize a noise coupling and a thermal heating from a switching converter, lower output ripple and high-efficient three-phase constant on-time (COT) hysteretic control is implemented. The internal voltage regulator is employed for a stand-alone operation. Section IV presents low cost TCXO system as well as self-calibrating wake-up timer. The TCXO system consists of TSU, compensation-and-learning unit (CLU), and DCXO. Embedded clock system compensates the crystal oscillator temperature characteristics and provides reference clock which is insensitive to temperature. Self-calibrating timer systems with RCO are implemented with software assistance. The measurement results are analyzed and compared with those of prior works in Section V. Finally, conclusion is given in Section VI.

II. RF TRANSCEIVER

A. Transceiver Architecture

Fig. 2 shows an RF transceiver architecture for NB-IoT and low-cost GNSS feature support with a constrained tracking scenario (i.e., time sharing between NB-IoT and GNSS).

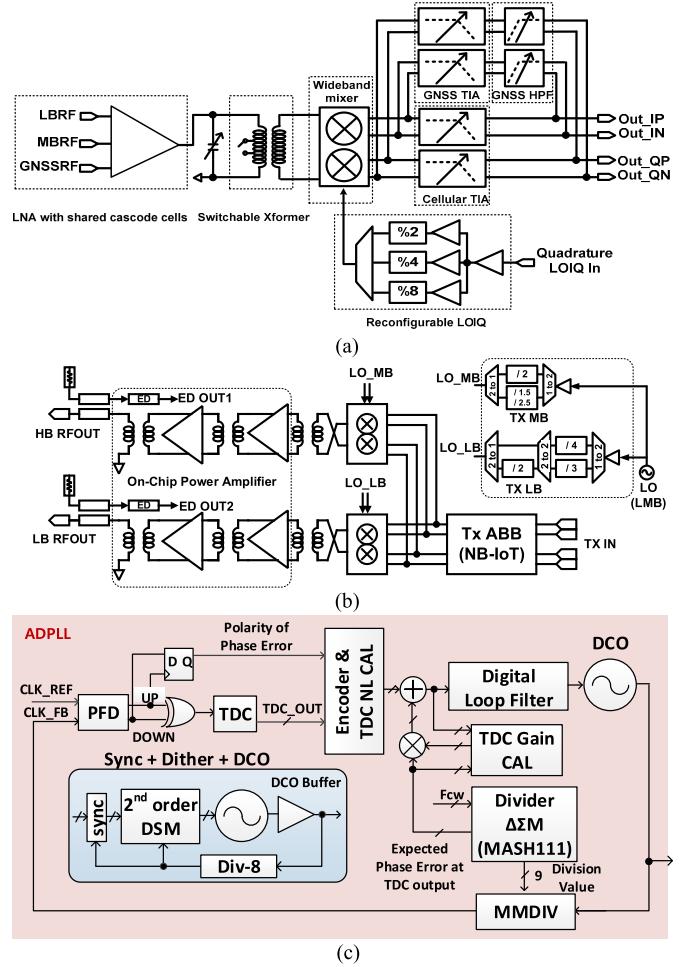


Fig. 2. Transceiver architecture. (a) RX. (b) TX. (c) All-digital PLL.

Infrequent data transfer to network in the target application of NB-IoT makes sense to the constrained tracking scenario for system architecture optimizations. NB-IoT and GNSS systems do not operate simultaneously. This enables the RF transceiver for NB-IoT and GNSS systems to share common blocks. A receiver (RX) consists of an LNA with three input ports for LB, MB, and quad-GNSS system (GPS and Glonass at 1575 MHz, Galileo at 1610 MHz, and Beidu at 1561 MHz). The LNA load is a switchable transformer to cover from 0.45 to 2.2 GHz. The transformer is connected to a single mixer. The single mixer covers all supporting bands with divide-by-2/4/8. Dedicated trans-impedance amplifiers (TIAs) for NB-IoT and GNSS are integrated since different channel BWs have to be supported. In addition, GNSS TIA is followed by a high-pass filter.

A transmitter (TX) has two transmit paths for low band and mid band depending on the operating frequencies. In addition, dedicated on-chip PA is integrated for each path, as shown in Fig. 3. The CMOS PA consists of two stages to obtain high-voltage gain in a driver stage and enough power gain in a power stage, respectively. For each stage, differential and cascode structure are adopted for high linearity, high output power, and reliability.

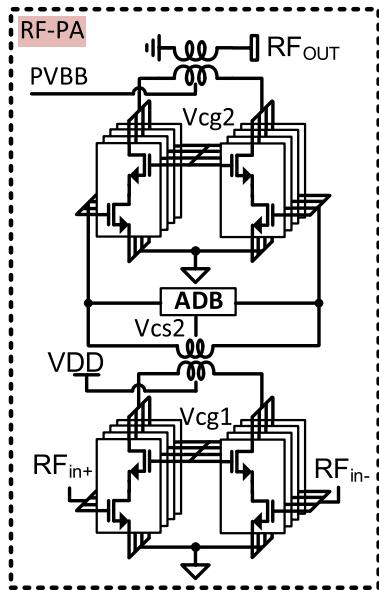


Fig. 3. CMOS PA block diagram.

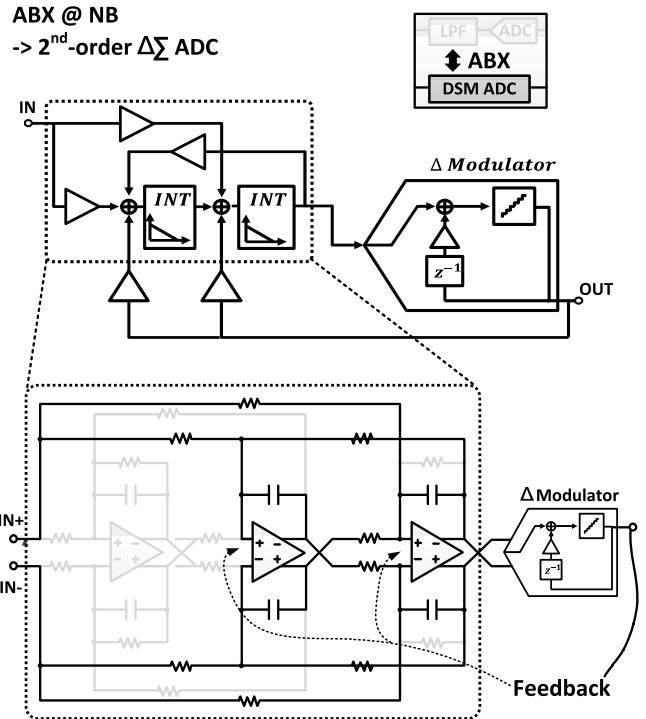
The CMOS PA produces a maximum output power of 29.0 dBm with current-efficient operation to guarantee 23-dBm transmitting output power, and it is fully integrated with transformer-based matching circuit to convert 50- Ω antenna impedance to 10 Ω . Adaptive biasing (ADB) with a power cell slicing technique is applied for the CMOS PA linearity as well as efficiency improvement. The ADB circuit includes an attenuator, a power detector, and a two-stage operational amplifier (OPA). The attenuator attenuates PA input waveform which is delivered to the power detector. The power detector is a very simplified envelop detector whose envelop is used for PA bias control through the OPA.

An all-digital PLL (ADPLL) is based on the classic delta-sigma fractional-N PLL in which the charge pump and loop filter of a conventional delta-sigma fractional-N PLL are replaced by a time-to-digital converter (TDC), a digitally controlled oscillator (DCO), and digital circuits in the digital PLL [12]. DCO is with a switchable inductor to cover NB-IoT and GNSS.

An integrated PA can be a high self-interference source for DCO in PLL. Divide-by-2 (DIV2) and divide-by-3 (DIV3) are affected by large TX 2nd and 3rd tone to DCO. Since PA and DCO are placed in the same die, the emission of harmonics by the PA into the DCO core will lead to amplitude modulation (AM)/frequency modulation (FM) conversion and thus degraded EVM performance. In extreme cases, the lock of the DPLL could be corrupted [7]. Divide-by-2.5 (DIV2.5) is integrated to reduce TX harmonic to DCO coupling effects for integrated PA since DIV2.5 has only coupling to 2 \times fDCO from 5th order of TX harmonic.

B. Analog Baseband Transformer (ABX)

NB-IoT and GNSS systems share RX path and require two extremely different bandwidth specifications, 90 kHz and 23 MHz, respectively. In order to overcome the inefficiency of the conventional ABBs supporting a wide range of signal bandwidth, a reconfigurable ABB, which we named analog

Fig. 4. Second-order CT- Δ Σ ADC mode in NB mode.

baseband transformer (ABX), is implemented [13]. As the difference of the desired bandwidths is large, the use of single ABB structure becomes inefficient since it is hard to optimize the power and area of the ABB for both bandwidths. Under these conditions, ABX is more suitable structure of baseband RX circuit. The ABX operates as an area-and-power-efficient Δ Σ analog-to-digital converter (ADC) for narrowband (NB) mode and as an active RC low-pass filter (LPF) for wideband (WB) mode for low power consumption. Most of the required analog building blocks such as OPAs and passive components are shared between all ABX modes, requiring no additional power, complexity, and area. In a 90-kHz bandwidth, ABX operates as a second-order Δ Σ ADC, and in 23-MHz bandwidth, it operates as third-order Chebyshev filter. Since the capacitors for narrow signal bandwidth mode mostly occupy the RC LPF ABB size, it is possible to reduce the size dramatically in the absence of NB-LPF in ABX. Furthermore, the ABX power in WB mode can be reduced because of its transformation from Δ Σ ADC to RC LPF.

Figs. 4 and 5 describe the two different modes of ABX, second-order Δ Σ ADC and third-order active RC LPF, respectively. The switch configurations of simplified paths in each mode are expressed as dark lines (ON) or light shaded lines (OFF). The ABX can reconfigure its structure into different modes by simply switching the path connections without additional complex circuits, as shown in Figs. 4 and 5. All of the switches that change mode of ABX are implemented using only NMOS at the input of OPAs, since the input nodes of the OPAs are virtual ground. To minimize interference between different modes, the thick-gate transistors are used.

The capacitors of LPF for bandwidth control in WB are reutilized as integrating capacitors of the Δ Σ ADC in NB. Moreover, the OPAs of ABX can efficiently operate with

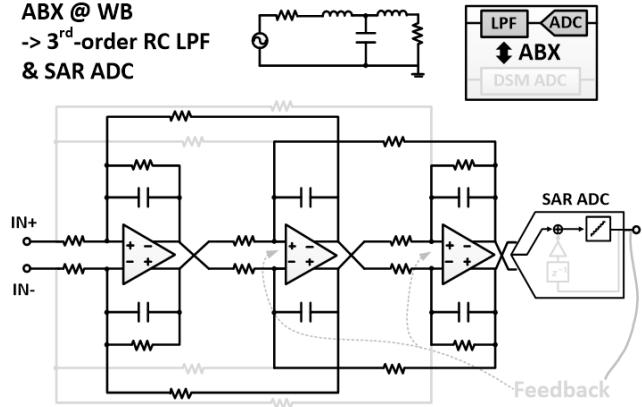


Fig. 5. Third-order active RC LPF mode in WB mode.

programmable connection changes depending on the bias current in both NB and WB modes.

In NB mode, the $\Delta\Sigma$ ADC adopts a second-order feedback topology with input feed-forward path to reduce the integrator internal swing. In order to avoid aliasing problem without use of a dedicated anti-aliasing filter, a continuous time (CT) $\Delta\Sigma$ ADC is implemented. The feedback current from the Δ modulator is injected by a 4-bit digital-to-analog converter (DAC) which utilizes data weighted averaging (DWA) technique [14] to improve linearity. The feedback, feedforward, and state scaling coefficients of the $\Delta\Sigma$ ADC are decided by system-level simulations to achieve the best signal-to-noise-and-distortion ratio (SNDR) performance with a 30.72 MHz of the sampling frequency. In this mode, only two OPAs are required; thus, one OPA is disabled to improve energy efficiency. The power down mode of OPA is done by interruption of current. The start-up time of NB-ABX is about 20 μ s which is enough settling time to change modes in an NB-IoT system for infrequent data communication.

In WB mode, WB-ABX consists of a third-order Chebyshev active LPF and a 5-bit successive approximation (SAR) ADC with a sampling rate of 98.214 MHz. Since the SAR ADC does not need constant power, the RC LPF and SAR ADC can be a good combination to support wide bandwidth. The Chebyshev filter which has 1-dB ripple and 23-MHz BW is initially synthesized as an RLC filter, and it is implemented by using resistors, capacitors, and OPAs. The WB-ABX is designed to have a programmable gain from 0 to 42 dB in a 6-dB step size, and the gain can be controlled by changing the input resistances and feedback resistances. The feedback capacitors which are related to bandwidth are also connected in the same way as integrating capacitor in NB-ABX, so only capacitance is changed during transformation from NB-ABX to WB-ABX. In addition, the switch size is decided to be optimal to avoid the gain degradation and the unexpected zero of the filter.

The output of the RC filter is connected to 5-bit ADC which has 23-dB SNR and -2-dBm max input range. The ADC in WB-ABX operates as a 5-bit SAR ADC and transforms its structure as a 4-bit Δ modulator which has fractional coefficient in NB-ABX, $\Delta\Sigma$ ADC mode.

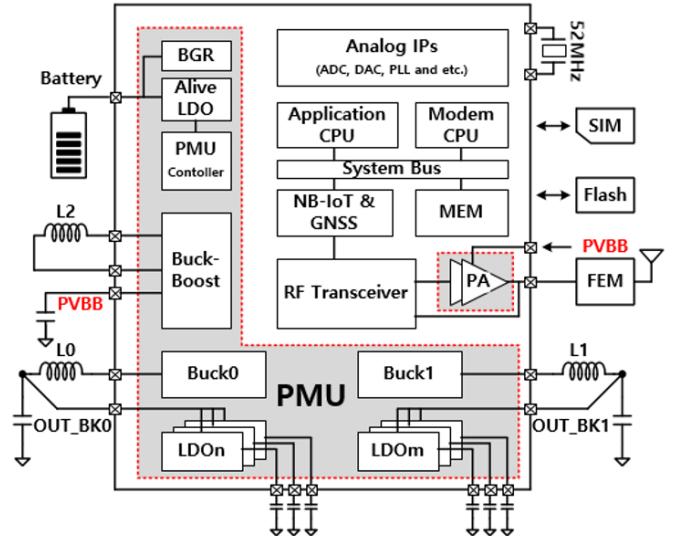


Fig. 6. Block diagram of the PMU integrated NB-IoT SoC.

III. POWER MANAGEMENT UNIT

A. PMU Integrated NB-IoT Architecture

Fig. 6 shows the overall NB-IoT SoC architecture and the power tree of the PMU. The PMU contains a bandgap reference (BGR), an alive LDO, a sequencing logic, two buck converters, six LDOs, and a BB converter.

The low power BGR and the alive LDO play a key role to decrease power consumption. The power sequencing logics control the PMU according to the power scenarios. The BGR and the alive LDO are designed to provide the supply voltage of the power sequencing logics called uPMU. When the battery is attached, the BGR and the alive LDO are automatically started.

Two buck converters and six LDOs provide the supply voltages to digital, analog, and RF building blocks with optimum power efficiency. When the NB-IoT chip wakes-up and starts to communicate with an LTE base station, bucks and LDOs are sequentially enabled.

The BB converter is synchronized with CMOS PA operation for power saving. The converters are based on the hysteretic controller using synchronous rectifications to obtain high efficiency. At low load current, the converters enter a pulse FM (PFM) mode automatically to maintain high efficiency over the complete load current range. The output voltage is programmable using digital control bits. The output voltage of the BB is typically 3.3 V with delivering up to 850 mA of output current.

B. Three-Phase COT Hysteretic Buck-Boost Converter

Fig. 7 shows the block diagram of the BB converter which consists of four LDMOS switches to have low ON-resistance and high breakdown voltage, internal voltage generators, an RC ripple injection block, two comparators, a COT generator, and several supplementary blocks. BB mode makes large switching noise and needs a high-voltage and high-current

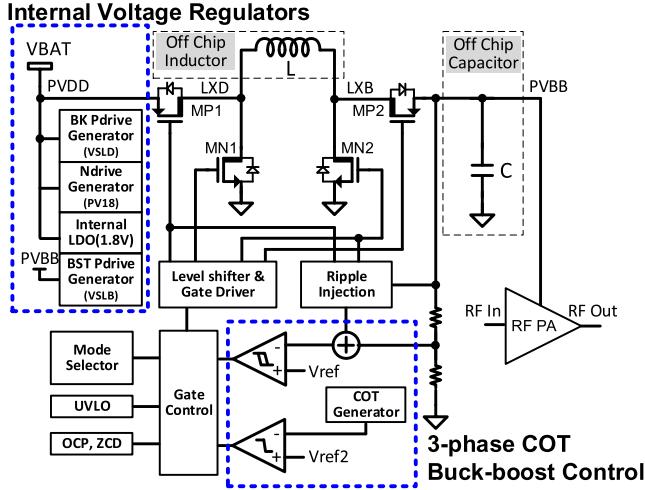


Fig. 7. Block diagram of the BB converter.

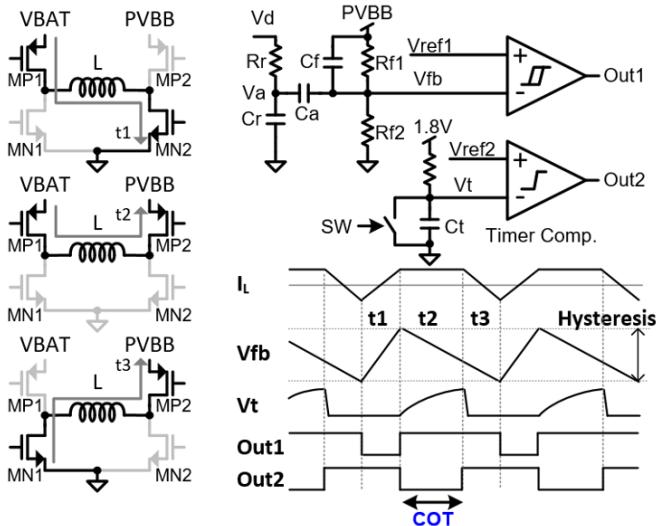


Fig. 8. Three-phase operation and a waveform in BB mode.

devices [15]. To reduce the switching noise in BB mode, three-phase COT hysteretic control is implemented compared with conventional two-phase BB mode. The three-phase COT hysteretic control achieves low average current and low switching noise, which leads to less than half output voltage ripple and inductor current. Also, a low inductor current ripple minimizes the root-mean-square (RMS) current and results in high power efficiency. In addition, the hysteretic control having excellent transient response is employed for supporting the dynamic load variation of CMOS PA. Thus, an implemented three-phase COT hysteretic control can achieve small output ripple and fast response, simultaneously. For reliability of the proposed converter, under voltage lock out (UVLO), over current protection (OCP), and zero current detector (ZCD) blocks are implemented.

Fig. 8 shows the operation and waveform in the step-up/down mode of the three-phase COT hysteretic control. Two comparators are employed to generate three-phase control signals. The first comparator compares the ripple injection

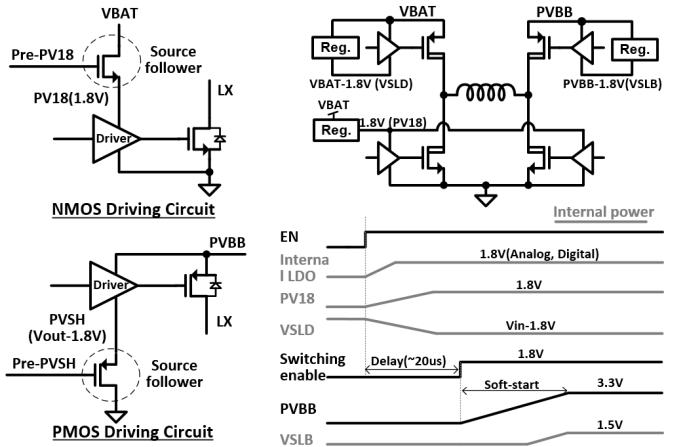


Fig. 9. Internal voltage generator circuit and waveform.

signal and a reference voltage 1 (V_{ref1}). The second comparator is used for generating a COT signal synchronized by COT generator for phase 2 with a reference voltage 2 (V_{ref2}) and COT generator. The switching frequency and the inductor current ripple are mainly optimized with phase 2. In the first phase, MP1 and MN2 are turned on, and MN1 and MP2 are turned off, so, inductor current is energized with a slope of $VBAT/L$. In the second phase, MP1 and MP2 are turned on, and MN1 and MN2 are turned off, so, inductor current is energized or de-energized with a slope of $(VBAT-PVBB)/L$. In the third phase, MN1 and MP2 are turned on, and MP1 and MN2 are turned off, so, inductor current is de-energized with a slope of $-PVBB/L$. From the RC time constant and the capacitor ratios, the voltage slope of V_{fb} can be expressed as

$$dV_{rise}/dt = [(V_d - V_a)/(R_r C_r)] \cdot C_a/(C_f + C_a) \quad (1)$$

$$dV_{fall}/dt = [(-V_a)/(R_r C_r)] \cdot C_a/(C_f + C_a). \quad (2)$$

The output voltage and the switching frequency of the BB converter can be derived from (1), (2), and the inductor volt-second principle. The sequence of the above three phase is appropriately arranged to efficiently generate an output voltage with a low inductor current level and make a fast transition.

C. Internal Voltage Regulator Circuit

For stand-alone operation, the BB converter generates 1.8 V analog and digital supply voltages powered by internal LDOs, as shown in Fig. 9. Because the maximum V_{gs} of LDMOS is limited to 1.8 V, the internal voltage generators are designed with a source follower which has low output impedance and a wide bandwidth. To achieve small form factor of NB-IoT applications, LDO does not use the external capacitors. For driving N-type LDMOS gate, PV18 (1.8 V) is generated by NMOS source follower (MNSF). Also, VSLD (VBAT-1.8 V) and VSLB (PVBB-1.8 V) are generated by PMOS source follower (MPSF) for driving PLDMOS gate. Each internal voltage should be settled before switching operation of the BB converter, so internal LDO is pre-enabled, which is controlled by operating sequence to satisfy timing requirements.

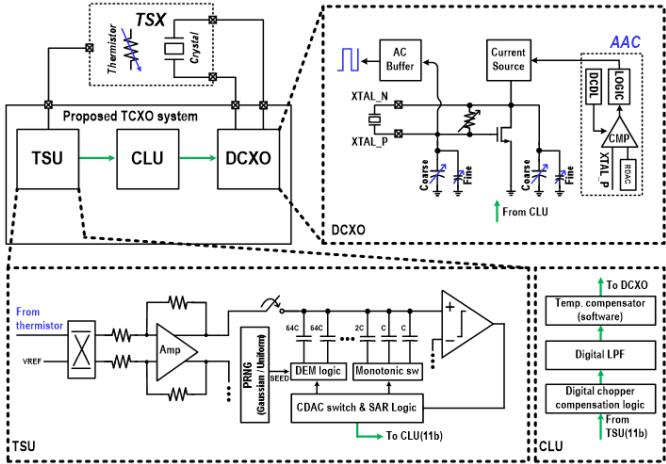


Fig. 10. Implemented TCXO system.

IV. CLOCK MANAGEMENT UNIT

A. Temperature Compensated Crystal Oscillator (TCXO)

A TCXO system is implemented along with DCXO, TSU, and CLU to substitute a costly TCXO with a low-price crystal oscillator, as shown in Fig. 10. A thermistor of TSX generates temperature information and a TSU converts it to digital codes for CLU. An inverse function of the temperature characteristic of the crystal oscillator is calculated in the CLU, and residual frequency error is minimized by means of adjusting a DCXO. The DCXO consists of a resistive feedback NMOS amplifier with a PMOS cascoded current source, automatic amplitude calibration (AAC) logic to ensure optimized phase noise performance, an AC buffer to convert the sine waveform to a rectangular waveform, and a digitally controlled capacitor array capable of controlling the frequency. The gate and drain of the NMOS amplifier are connected to each node of the crystal in the TSX, which can be modeled as a combination of passive inductor, resistor, and capacitor. By means of parallel resonance of the crystal and capacitor array, the output frequency can be determined. Therefore, the range and resolution of the capacitor array are the key design constraints. The capacitor array is categorized into two different mechanisms, coarse and fine. While the coarse cap is implemented with the MOS transistor cap to enlarge the cover range, the fine cap utilizes the parasitic capacitor of the metal line to accomplish the excellent tuning resolution. The current source guarantees superior power supply rejection ratio (PSRR) to block the influence of the supply noise by using cascaded PMOS with OPA-based bias circuit.

Since the DCXO is used as a reference clock, the noise characteristic should be taken care of. It is noted that the amplitude of the DCXO is directly correlated with the phase noise; hence, it implements an AAC scheme that can provide optimum phase noise performance without consuming DC. Also, the DCXO utilizes the phenomena that the peak amplitude information of sine wave is contained at the exact timing of quarter period. By using a digitally controlled delay line (DCDL), the peak amplitude point is tracked, and then the current flow into the amplifier is adjusted to calibrate to a certain amplitude to guarantee the optimum phase.

In order to control the DCXO with extremely fine frequency step (1 ppb Hz/step), 15-bit resolution of temperature change sensing is required according to the TCXO system analysis results as follows. It is expected that 0.01 °C temperature difference corresponds to about 13-bit ADC resolution and minimum step difference of the DCXO control resolution can be applied to track frequency offset. When 0.01 °C temperature change is detected, the frequency offset around 25 °C is 0.004 ppm which would not give performance degradations in a modem. If temperature sensing results are inaccurate or DCXO frequency offset control varies over the temperature, estimation of the frequency offset for a given temperature would be wrong such that the DCXO control or frequency offset calibration works incorrect. Therefore, it would be required to increase the accuracy of temperature sensing as well as the DCXO control accuracy. However, for low-power applications such as IoT, a high-resolution delta-sigma ADC is inefficient in terms of power and active area. Therefore, the TSU in the TCXO system has an 11-bit SAR ADC with digital averaging block.

The TSU consists of a single-to-differential amplifier which amplifies thermistor output voltage with low noise and 11-bit SAR ADC core, and a digital averaging block. The digital averaging block accumulates 8192 samples to improve SNDR performance by 39 dB, thereby 15-bit ADC is replaced with 11-bit ADC. In order to cancel out the flicker noise, analog and digital chopping techniques are employed to the amplifier and comparator. Note that the digital averaging block conducts not only averaging of the TSU outputs but also digital chopping operation.

In order to improve the averaging performance even more, a dithering technique is utilized to the SAR ADC. A dither is injected by using capacitor DAC (CDAC) with 8-bit resolution, and its added hardware burden is ignorable due to the very small size of the custom-designed unit capacitor (250 aF). For PVT-invariant dither injection, the dither is injected using Gaussian distributed probability. The 11-bit CDAC is implemented with a split-CDAC configuration. Thermometer structure is applied to 3 MSBs and binary structure is applied to 8 LBSs [16]. Dynamic element matching (DEM) technique is applied with uniformly distributed probability to the seven unary capacitors for the MSBs to enhance the linearity [16].

Another key component is the compensation-and-learning algorithm in the CLU. A crystal has characteristics that oscillation frequency varies depending on the temperature changes and it has 3rd order polynomial of frequency–temperature (F-T) relations as follows:

$$F_T = C_3(T - T_0)^3 + C_2(T - T_0)^2 + C_1(T - T_0) + C_0 \quad (3)$$

where C_0 , C_1 , C_2 , C_3 , and T_0 are the curve fitting coefficient values and inflection temperature of the crystal, respectively. Due to variations of the crystal oscillation frequency, a factory calibration for each crystal is required, and this procedure is named coarse compensation. During the factory calibration period, C_0 and C_1 coefficients are estimated by measuring the frequency under the two temperature conditions. By using C_0 and C_1 (from measurements) and referring to C_2 and C_3 (from typical value of crystal specifications) coefficients,

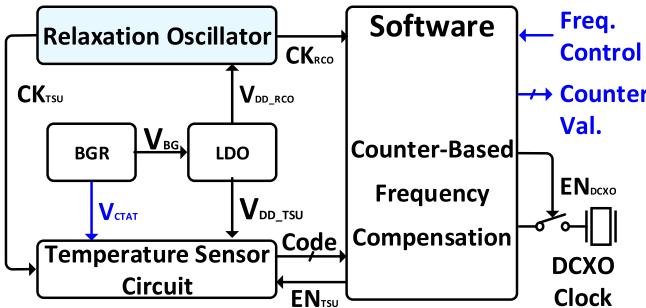


Fig. 11. SoC wake-up timer architecture.

inverse function of temperature characteristic of the crystal is calculated and stored in the look-up table (LUT). By referring to the temperature information from TSU and LUT data, the CLU controls the DCXO to minimize frequency error.

However, only compensation operation using LUT cannot cover the whole F-T characteristic; thus, frequency accuracy is limited, because typical 2nd- and 3rd-order fitting coefficients are different from actual values. To overcome this limitation, the CLU conducts an on-the-fly learning algorithm for a given temperature. When the modem with the TCXO system is attached to a cellular network, CLU keeps updating the frequency error to the LUT with a digital mixer and a fractional-N modem PLL (~ 100 ms) by estimating frequency difference between received cellular signal (LTE signal) and crystal oscillator. During the learning procedure, received cellular signal should be reliable, thus, updating the LUT is only conducted when signal-to-interference-plus-noise ratio (SINR) is larger than threshold level (> 30 dB); hence, the frequency estimation can be regarded as reliable.

B. Self-Calibrating Wake-Up Timer

To minimize the power consumption and cost in wireless-sensor node for low-power IoT applications, the on-chip oscillators, which replaces real-time-clock (RTC)-based crystal oscillator, have been generally employed. These oscillators are key always-on components in sleep operation. Extremely low power consumption as well as robust frequency stability with respect to PVT variations are required.

An RC-time constant-based RCO has been used as an on-chip wake-up timer due to its superior stability and compact size compared with other on-chip oscillators. However, most of the published oscillators [17]–[20] need one- and two-point calibration procedures for the frequency trimming and resistors' temperature compensation, causing considerable costs and test time. To address these challenges, a software-assisted factory-calibration-free timer is proposed.

The wake-up timer using a sub-threshold internal LDO and a temperature sensor circuit is implemented. The wake-up timer minimizes supply sensitivity by using the sub-threshold LDO and temperature sensitivity by adjusting a counter value based on the output of the TSU to compensate frequency variations.

Fig. 11 shows the architecture of the proposed timer, which is composed of an RCO, a TSU, a BGR, a crystal oscillator (XTAL), and software for process and temperature compensation. The BGR is implemented to provide the

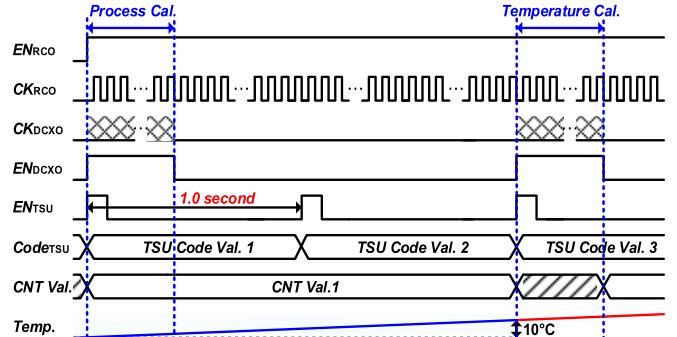


Fig. 12. Timing diagram of the frequency compensation method.

reference voltage and negative TC voltage for LDO and TSU. The real-time crystal oscillator, 32.768 kHz, represents the absolute time by counting the clock. For example, the absolute time can be expressed as 1 s by counting 32.768-kHz clock through 15-bit counter operation; therefore, the on-chip wake-up timer is required with the precise clock, which does not change against PVT variations. It implements a self-calibrating timer system, which improves the temperature characteristic as well as reduction of test time and cost thanks to software-assisted compensation method.

Fig. 12 shows an overall frequency trimming and temperature compensation procedure. At the system start (EN_{RCO} goes high), the software operates DCXO clock (CK_{DCXO}), which has constant frequency across PVT variation, to measure the frequency of RCO compared with that of DCXO and determine a counter value (CNT val.). If the frequency of RCO is lower than the target frequency, 32.768 kHz, due to process variation, CNT val. is decreased to maintain absolute time. After the frequency measurement finished, DCXO clock is disabled to save power.

In the next step, the timer system executes the temperature compensation procedure. The software periodically operates TSU (EN_{TSU}) once per second, and TSU transmits the temperature information ($Code_{TSU}$) to the software. At this time, if the temperature variation is larger than 10°C , the software wakes up DCXO again to adjust the counter value, CNT Val.; thus, this technique significantly improves the TC of the timer. Because there is no activity in the sleep state and the temperature does not change rapidly across the time, it is enough for TSU to wake up once per second. Here, the momentary operation of TSU and DCXO has a negligible impact on the power consumption of the sleep mode.

Fig. 13 shows the circuit diagram of RCO with an internal LDO. The overall operation of RCO is as follows. The negative input of the comparator is determined by the product of the current (I_A) and poly resistors (R_P). The mirrored current periodically charges the capacitors ($C_{T1,2}$), and V_{C1} and V_{C2} are reset when the positive input exceeds the threshold voltage. Thus, the frequency of RCO is the sum of the RC -time constant ($R_P C_{T1} + R_P C_{T2}$), comparator delay (t_C), and buffers delay (t_B). The 28-nm LPP poly resistor has positive TC and linearly varies, resulting in the TC of 238 ppm/ $^{\circ}\text{C}$ across the temperature range from -25°C to 85°C .

In this structure, the bias-current source (I_A) is proportional to the temperature as the threshold voltage of P1 PFET is

TABLE I
COMPARISON TABLE FOR FEATURE AND RF PERFORMANCE

	This work	[1]	[2]	[3]	[4]	[5]	[6]
Feature	NB-IoT	NB-IoT	NB-IoT	NB-IoT (Single-tone only)	eMTC/NB-IoT (PA only)	NB-IoT (PA only)	NB-IoT/EC-GSM
Navigation System	GNSS integrated	-	-	-	-	-	A-GPS integrated
PMIP	Integrated	Integrated	Integrated	-	-	-	-
CMOS PA	Integrated	-	Integrated	Integrated	PA only	PA only	-
TCXO system	Integrated	-	DCXO integrated	-	-	-	DCXO integrated
Clock system	Integrated	-	-	-	-	-	-
Technology	28nm CMOS	55nm CMOS	40nm CMOS	180nm CMOS	40nm CMOS	55nm CMOS	110nm CMOS
Die Size	24.4 mm ²	2.23 mm ² (Transceiver only)	7.1 mm ²	-	5.0 mm ²	1.11 mm ²	-
Frequency range	450~2200 MHz	450~2200 MHz	450~960MHz, 1561~2200MHz	750~960MHz	699~915MHz	850MHz/1.7GHz	700~900MHz/1.7~2.1GHz
SAW-less	Yes	Yes	Yes	-	-	-	Yes
TX Max Power	23 dBm	4 dBm	22.2 dBm (LB)/22 dBm (HB) 19.2 dBm (LB)/18.6 dBm (HB) for single-tone for multi-tone	23.2dBm for single-tone	27.1dBm (Continuous Wave)	24.4dBm/23dBm	-
TX EVM	1.13% @ 23dBm for single-tone 6.9% @ 23dBm for multi-tone	0.75% @ 4dBm for single-tone 3.5% @ 4dBm for multi-tone	1.5% (LB)/2.9% (HB) for single-tone 7.7% (LB)/8.3% (HB) for multi-tone	3.87% @ 18.87dBm for single-tone	3.1% for eMTC	-21.6dB (8.3%)	-
TX SEM @ 300kHz	-53dBc @ 23dBm	-57dBc @ 4dBm	-	-	-	-	-
TX Power Consumption	Refer to Table II	25.8mW	675mW @ 19.2dBm (LB) 585mW @ 18.6dBm (HB) for multi-tone	~ 480mW	-	-	-
Out-of-band Blocking (Range1/Range2/Range3)	-22dBm/-19dBm/-14dBm	-	-12dBm @ +/- 150MHz offset -14dBm @ +/- 200MHz offset	-	-	-	-
RX EVM	~ 1%	-	1.9% (LB)/3.5% (HB)	-	-	-	-
Sensitivity	-125dBm without repetition	-140dBm with repetition	-112.5dBm (LB)/-111.9dBm (HB) without repetition	NF=4dB	-	-	-115.9dBm
GNSS navigation sensitivity	-150dBm	-	-	-	-	-	-
RX Power Consumption	Refer to Table II	11.8mW	53mW (LB)/56mW(HB)	25mW	-	-	-

* 450MHz Band is supported with a limited condition

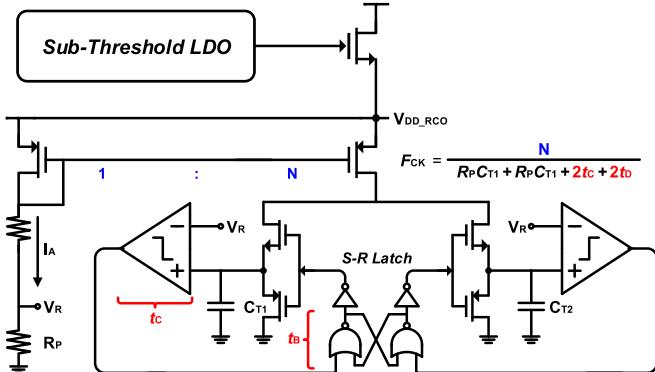


Fig. 13. RCO architecture.

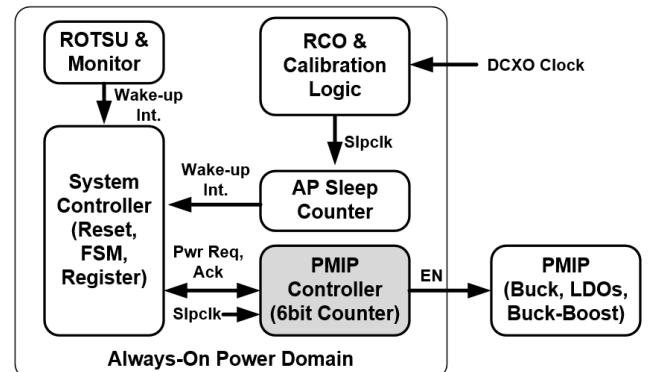


Fig. 15. Block diagram of always-on system.

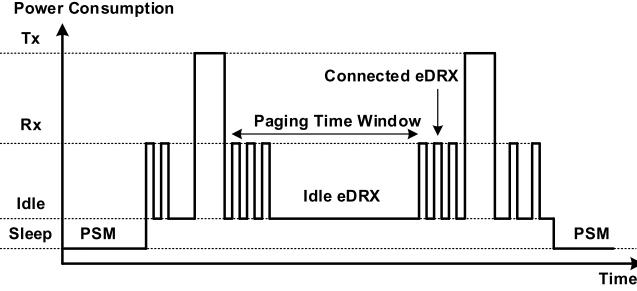


Fig. 14. Power scenarios of NB-IoT system; extended DRX mode and PSM.

decreased across the temperature; therefore, the comparators using I_A have the delay (t_C) of negative TC. As a result, the positive TC of R_P and negative TC of t_C are compensated each other. This RCO exhibits 48.4 ppm/ $^{\circ}$ C by using delay-compensation technique without calibration.

C. Power Modes and PMU Control

The PSM and the eDRX are introduced to reduce power consumption of IoT in Release 12 and Release 13, respectively. The PSM reduces energy consumption while the device is not transmitting or receiving. eDRX uses longer DRX timers to achieve further power consumption improvements [21]. To support above power scenarios of NB-IoT, as shown in Fig. 14, low power circuits and highly efficient power regulators are needed simultaneously.

A system controller, clock sources, a sleep counter, a temperature sensing unit, and PMU controller working on always-on power domain are employed, as shown in Fig. 15. The system controller has a finite state machine (FSM) which is mainly used for controlling power modes of PSM, eDRX, and active modes (TX/RX). An RC-based oscillator (RCO) is

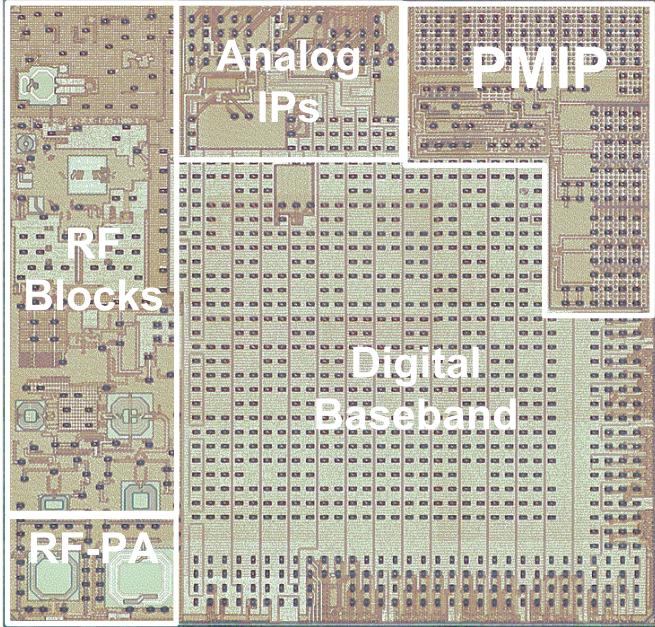


Fig. 16. Die photograph of the NB-IoT and GNSS SoC employing RF blocks, RF-PA, PMIP, and analog IPs.

TABLE II
POWER CONSUMPTION IN VARIOUS OPERATIONS [9]

Power consumption in various operations				
PSM	2.56s DRX	TX @ 20dBm	Active AP/CP	GNSS standalone
7μA	2.9mA	100mA	40mA	60mA

implemented for a lower cost, higher reliability, and smaller form factor. However, compared with the crystal-based oscillator, the accuracy and stability of the RCO are inferior due to a low Q factor and a temperature dependency. So, the calibration of the RCO frequency is implemented with a temperature sensing unit (ROTSU) and a digitally compensated crystal oscillator (DCXO). The system controller manages sleep and wake-up sequence through the interaction with the sleep counter. When entering wake-up mode or sleep mode, the system controller sends a power request to the PMU controller. It has a sequencing logic and 6-bit counter which use the 32-kHz RCO sleep clock. The power-up and power-down sequence of the PMU is configurable and programmable by resister setting. The BB converter enable is controlled by a software control which synchronizes with the CMOS PA.

V. MEASUREMENT

Fig. 16 shows the die photograph of the NB-IoT and GNSS SoC employing RF blocks, RF-PA (CMOS PA), PMIP, and analog IPs. The die size is $5.05 \times 4.87 \text{ mm}^2$.

With the buck booster supply voltage, TX with an integrated CMOS PA achieves 23-dBm output power with -47-dBc ACLR for UTRA and 34.4-dBc ACLR for GSM with sufficient margin of spectrum emission mask, as shown in Fig. 17, which meet the NB-IoT specifications. A summary of feature and RF performance is tabulated in Table I.

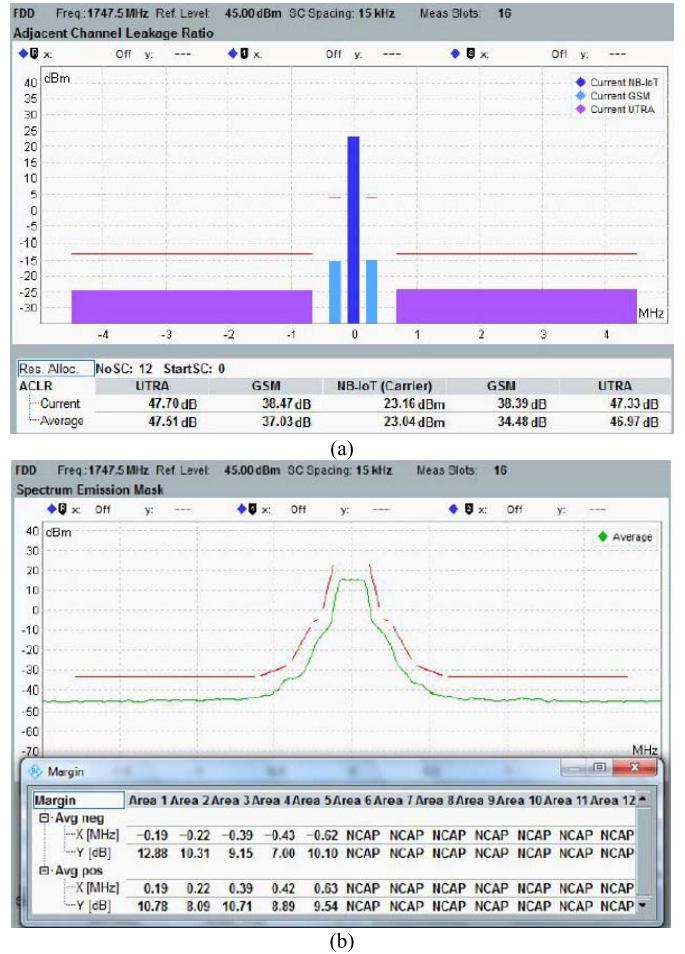


Fig. 17. TX Measurement results with CMOS PA and buck-booster. (a) Measured adjacent channel leakage ratio result at 23 dBm. (b) Measured spectrum emission mask result at 23 dBm.

The RF circuitry consumes 50 mW for receiving and 1610 mW for transmitting in an NB-IoT mode. The power consumption of always-on-block is $15 \mu\text{W}$, and the sleep current consumption is less than $10 \mu\text{A}$ at 3.8 V. Table II summarizes power consumptions in various operation modes [9]. Days-of-use (DoU) battery life over various daily tracking counts has been carried out with various counting ranges from 1 to 24. Each daily tracking count is assumed as follows: GNSS location search (assuming 30 s), active application processor (AP) and communication processor (CP) (assuming 30 s), TX at 20 dBm (assuming 0.03 s), DRX (assuming 180 s), and PSM idle (the rest of time). Table III summarizes the battery life results [9].

Table IV lists the comparison of the implemented NB-ABX's performance with previously reported active RC LPFs [22]–[25] and NB-ABX [13]. The areas of the referred NB-ABBs [22] are about 12 times larger than the proposed ABB, which is too large even considering the process difference, and the other LPFs [23]–[25] also occupy large areas even though their minimum bandwidths are higher than the proposed NB-ABX. In addition, the reported active RC filters also require additional ADCs to generate digitized outputs. In terms of power consumption, the NB-ABX consumes

TABLE III
TRACKING POWER AND DOU ESTIMATION [9]

DoU estimation for tracking (with 300mAH battery)			
Daily Tracking Count (Number)	Tracking Interval (Hour)	Average Current (mA)	Battery Life or DoU (days)
1	24.0	0.0408	306
2	12.0	0.0576	168
4	6.0	0.1170	88
6	4.0	0.1795	60
8	3.0	0.2440	45
10	2.4	0.3102	36
12	2.0	0.3777	30
14	1.7	0.4463	26
16	1.5	0.5159	23
18	1.3	0.5863	20
20	1.2	0.6575	18
22	1.1	0.7295	17
24	1.0	0.8020	15

TABLE IV
COMPARISON TABLE FOR NB-ABX

Parameters	This Work NB-ABX I&Q	[13] NB-ABX I&Q	Active RC Filter			
			[22]	[23]	[24]	[25]
Technology (nm)	28	14	65	65	65	90
Min. BW (MHz)	0.09	0.1	0.1	0.2	2.2	0.3
Size (mm^2) (active area)	0.17	0.11+ADC	2.03+ADC	1.6+ADC	0.98+ADC	0.68+ADC
Power (mW)	1.7	1.33	7.3+ADC	3.44+ADC	2.9+ADC	2.1+ADC
DR (dB)	86.32	90	[22]-[25]			
SNDR (dB)	85.63	85.01	[22]-[25]			
Fs (MHz)	30.72	52	[22]-[25]			

* The Power and size of reported active RC filters need additional ADC

1.7 mW, which is low power since the sampling frequency is low. Table V shows the specifications of the state-of-the-art $\Delta\Sigma$ ADCs [26]–[31], the previous WB-ABX [13], and the implemented WB-ABX. For a fair comparison, the power and area of the reported $\Delta\Sigma$ ADCs are multiplied by 2 because WB-ABX has I and Q paths. The FOM of WB-ABX is about 172.4 dB, which is efficient approach than the other $\Delta\Sigma$ ADCs. Some $\Delta\Sigma$ ADCs [28]–[31] have good FOM, but they [29]–[31] consume much more power compared with WB-ABX even though the bandwidth is lower than WB-ABX. For [28], it consumes 156 mW which is too high to adopt as RX ABB.

Fig. 18(a) shows that the waveforms of the BB converter depict the operation of implemented three-phase COT hysteretic control mode at the load of 300 mA. Fig. 18(b) shows the measured power efficiency of the BB converter according to the load current. The peak efficiency of the BB converter achieves 94.9%, 93.4%, and 91.7% in step-down, step-up, and step-up/down modes, respectively. Table VI lists the comparison of the measured performance of the three-phase COT BB converter with some other recently published works.

TCXO accuracy is about 2 ppm. After the calibration and automatic frequency control (AFC), DCXO accuracy must come down to 0.1 ppm. It does not mean that DCXO output accuracy is less than 0.1-ppm value. Once DCXO output presents less than 2-ppm frequency offset, the residual frequency error is compensated in a modem block with DCXO

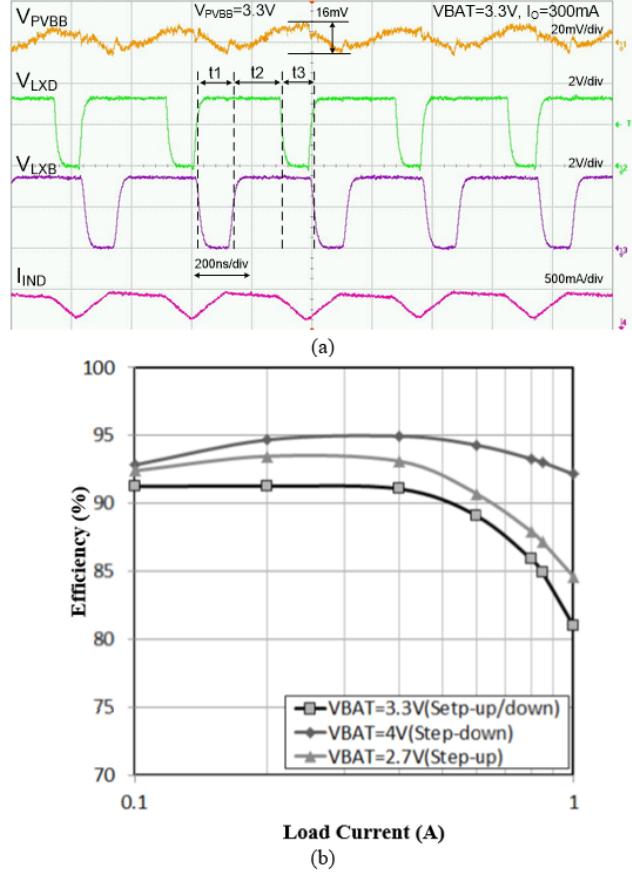


Fig. 18. PMIP measurement results. (a) Waveform of proposed three-phase COT BB at the load of 300 mA. (b) Measured power efficiency of the proposed BB converter for step-up/down, step-down, and step-up modes.

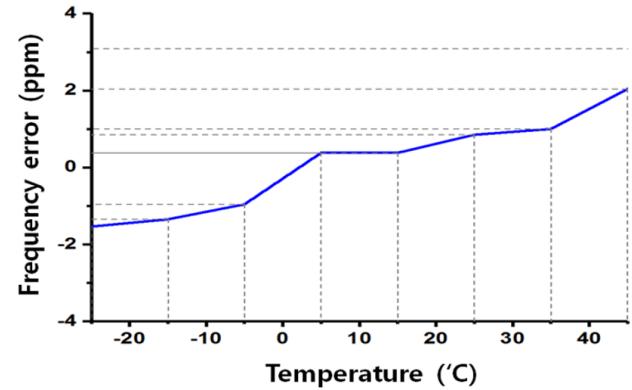


Fig. 19. TCXO system frequency error in terms of temperature.

and fractional-N modem PLL control. GNSS requires clock frequency accuracy is 0.5 ppm. The DCXO covers 60-ppm range with 1-ppb resolution. Also, TSU meets the resolution and Allen-deviation requirements for the TCXO system. In spite of the fact that a TSX frequency offset range is almost ± 40 ppm due to the temperature variation, the TCXO system shows ± 2 ppm error from -30 °C to 45 °C after two-point temperature calibration, as shown in Fig. 19, which ensures cellular and GNSS system requirements.

The temperature sensitivity and the power consumption of the wake-up timer are measured from -25 °C to 85 °C. The supply sensitivity is negligible thanks to the internal LDO.

TABLE V
COMPARISON TABLE FOR WB-ABX

Parameters	This Work	[13]	$\Delta\sum\text{ADC}$					
	WB-ABX I&Q	WB-ABX I&Q	[27]	[26]	[29]	[30]	[31]	[28]
Technology (nm)	28	14	65	65	28	130	28	28
Max. BW (MHz)	23	20	20	25	18	15	10	50
Fs (MHz)	98	98	1920	2200	640	640	320	1800
Size (mm ²)	0.17	0.11+ADC	0.15	0.5	0.16	0.34	0.2	0.68
Power (mW)	4.56	12.1+ADC	52	82.8	7.8	22.8	8.4	156
Effective DR (dB)	72.32*	30+ADC	76	77	78.1	82.9	80.8	85
ADC SNDR (dB)	30.32	-	73	77	73.6	80.4	74.4	74.6
* The WB-ABX's effective DR is sum of filter's max gain and SAR ADC's DR								
° The reported DSM ADC's power and size are doubled in this table to compare with ABX which has I&Q path								
FOM	172.4	-	160	164.8	174.7	174.1	174.5	173.1
FOM=DR+10log(BW/P)								

TABLE VI
PERFORMANCE COMPARISON OF BB CONVERTERS

Parameters	This Work	[15]	[32]
Technology (nm)	28	250	350
On-Die	O	X	X
Control	Hysteretic COT	Current-mode	Mixed-mode
V _{IN} /V _{OUT} (V)	2.5-5/3.3	2.5-4.5/2-4	2.5-5/3.3
V _{OUT} (V)	3.3	2 ~ 4	3.3
Ind./Cap. ($\mu\text{H}/\mu\text{F}$)	1/10	1/0.88	4.7/22
V _{RIPPLE} (mV)	16*	N/A	20*
I _{LOAD_MAX} (A)	0.85	0.4	0.3
f _{SW} (MHz)	2.5	5	0.5
Peak Eff.	0.917	0.91	0.935
Size (mm ²)	1.89mm ²	4.86mm ²	4.28mm ²

*VIN=3.3V, ILOAD=0.3A

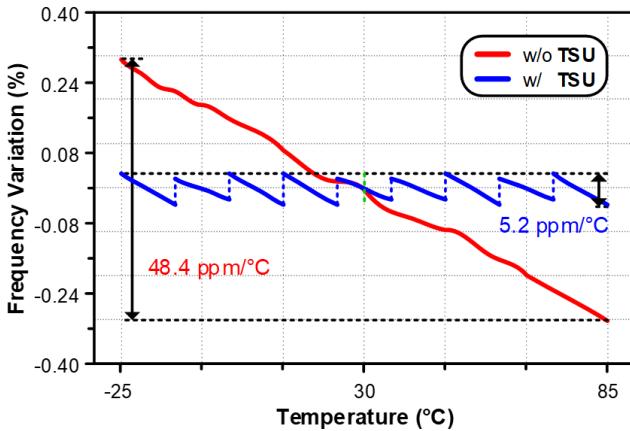


Fig. 20. Wake-up timer temperature sensitivities.

By using a delay-compensation technique using a PTAT current source, TC of the RCO is improved to 48.4 ppm/°C, which is 5.54× less than without the PTAT. The timer finally achieves

TABLE VII
PERFORMANCE COMPARISON OF WAKE-UP TIMER

Parameters	This Work		[17]	[18]	[19]	[20]
	w/o TSU	w/ TSU				
Technology (nm)	28		65	180	65	65
Frequency (kHz)	32.7		1350	3	33	18.5
Temp. Range (°C)	-25 ~ 85	0 ~ 145	-25 ~ 85	-20 ~ 90	-40 ~ 90	
TC* (ppm/°C)	48.4	5.2	96	13.8	38.2	38.5
Power (nW)	680		920	4.7	190	130
Size (mm ²)	0.11	0.23	0.005	0.5	0.015	0.032
Factory-Calibration	Free		2-Point Calibration			

* Temperature Coefficient (TC) = $(\text{Freq}_{\text{max}} - \text{Freq}_{\text{min}})/(\text{Freq}_{\text{avg}} \times (\text{Temp}_{\text{max}} - \text{Temp}_{\text{min}})) \times 10^6$

the excellent TC of 5.2 ppm/°C owing to the software-assisted method updating the counter value according to a TSU output, as shown in Fig. 20. At the room temperature, the power consumption of the timer system is only 680 nW at 32.7 kHz. The timer is compared with the state-of-the-arts timers in Table VII. This wake-up timer does not require the costing calibration procedure and accomplishes the lowest temperature sensitivity of 5.2 ppm/°C.

VI. CONCLUSION

This work aims for all-in-one SoC which integrates systems as much as possible and integrates RF transceiver to support NB-IoT and GNSS with on-chip PA. Integrated PMIPs include bucks, a boost, and LDOs. Clock management system embedded with DCXO, RCO, and TSUs is integrated.

NB-IoT and GNSS do not operate simultaneously. Therefore, a single RX path is shared for both applications. NB-IoT supports narrow bandwidth. On the other hand, GNSS has to be operated with wide bandwidth to cover multiple satellite system. Therefore, reconfigurable ABB called ABX is implemented to support NB and WB operation. TX is integrated with dedicated on-chip PA to support 23-dBm output power.

PMU is implemented to support a wide input voltage range from 2.5 to 5 V. To support an on-chip CMOS PA, a BB is integrated to provide 3.3-V supply as well as 850-mA max load current with three-phase constant-on-time controller for lower output ripple. For very long operation time, always-on-block current is critical and low power BGR and alive LDO for always-on system are implemented to support low power scenarios with the power as low as 15 μ W.

Low cost TCXO system as well as self-calibrating wake-up timer are implemented. The TCXO system replaces costly TCXO and on-the-fly learning algorithm is applied to correct the temperature variation of the system. A software-assisted self-calibrating wake-up timer is implemented to ensure the reliable peer-to-peer communication and reduce the power consumption during the sleep mode in IoT applications. The time does not need the additional calibration procedure by adjusting the counter value from the software according to PVT variations, thus, reducing the test time and cost.

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Jongsoo Lee received the B.S. degree in physics from Chung-Ang University, Seoul, South Korea, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from The Ohio State University (OSU), Columbus, OH, USA, in 2003 and 2008, respectively.

Since 2008, he has been with Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer and involved in cellular RF integrated circuit (RFIC) development. His research interests include the design of analog/RFICs and systems for a cellular application.



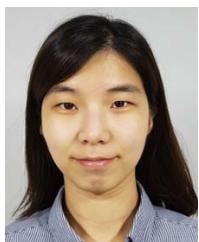
Jaeyeol Han received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, South Korea, in 2007 and 2009, respectively.

Since 2009, he has been with Samsung Electronics, Hwaseong, South Korea, where he is involved in power management chip development. His current research interests include the power management IC design of analog integrated circuits and RF systems.



Chi-Lun Lo was born in Taipei, Taiwan, in 1980. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, in 2003 and 2005, respectively.

He was with MediaTek Inc., Hsinchu, Taiwan, from 2007 to 2016, where he was involved in analog and mixed-signal circuits' development for wireless and wireline communication systems including WiMAX, GPS, WiFi, cellular, TV tuner, and ADSL/VDSL. From 2012 to 2014, he was expatriated to MediaTek Inc., Woburn, MA, USA, where he participated in high-speed wide bandwidth continuous time delta-sigma modulator development. Since 2016, he has been with Samsung Electronics, Hwaseong, South Korea. His current researches focus on high-efficient data converter design with wireless transceiver architecture optimizations.



Jongmi Lee received the B.S. and Ph.D. degrees in electronic engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2009 and 2015, respectively.

In 2015, she joined Samsung Electronics, Hwaseong, South Korea. Her current research interests include low power temperature sensor, delta-sigma modulated CT/DT analog-to-digital converter (ADC), and transceiver's analog baseband circuit.



Wan Kim (Student Member, IEEE) received the B.S. degree (Hons.) in electronic engineering from Inha University, Incheon, South Korea, in 2008, the M.S. degree in information and communications from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2010, and the Ph.D. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2016.

Since 2016, he has been a Staff Engineer with Samsung Electronics, Hwaseong, South Korea. His research interests include digital calibration techniques for high-resolution data converters and low-noise mixed-signal circuits' design for low-power applications.

Dr. Kim was a recipient of a Silver Prize for the Samsung HumanTech Paper Award in 2015.



Seungjin Kim received the B.S. degree in electrical engineering from Pusan National University, Pusan, South Korea, in 2006, the M.S. degree in electrical engineering from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2008, and the Ph.D. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2014.

Since 2014, he has been with Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer and involved in high-performance and low-power clocking circuit development. His research interests include analog/mixed-signal design such as phase-locked loops (PLLs), reference oscillators, and spread-spectrum clock generators (SSCGs) for wireless and wire-line communication systems using CMOS technology.



Byoungjoong Kang received the B.S. degree in electrical engineering from the University of Seoul, Seoul, South Korea, in 2001, and the M.S. degree in electrical engineering from Seoul National University, Seoul, in 2004.

In 2001, he joined Pantech Research and Development Institute, Seoul, where he was involved in the development of transceivers for GSM mobile communications. From 2002 to 2004, he was a Research Staff Member of the Center for 3-D Millimeter-Wave Integrated Systems, Seoul National University, where his work involved in the study of transmission lines, the design of microwave passive devices for biomedical applications, and the design of MMICs for millimeter-wave systems. In 2004, he joined Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer. Since 2004, his work has been focused on the design of RF integrated circuits (RFICs) for cellular and connectivity products.



Juyoung Han received the B.S. degree in electronic electrical engineering from the University of Seoul, Seoul, South Korea, in 2001.

She joined Samsung Electronics Company Ltd., Hwaseong, South Korea, in 2001, where she is currently an RFIC Design Engineer, developing cellular RF transceivers. Her current research interests include RF integrated circuits (RFICs), analog and digital phase-locked loops (PLLs), and local oscillators.



Sangdon Jung received the B.S. and M.S. degrees in engineering from Korea University, Seoul, South Korea, in 2007 and 2009, respectively.

In 2009, he joined Samsung Electronics, Hwaseong, South Korea, focusing on the mixed-signal circuit design including phase-locked loops, delay-locked loops, and oscillators for communication systems and mobile processors. His research interests include clock generation circuit and wireline transceivers.



Takahiro Nomiyama received the B.S. and M.S. degrees in engineering from Tsukuba University, Tsukuba, Japan, in 2002 and 2004, respectively.

In 2004, he joined Fuji Electric, where he was involved in developing high-voltage display driver IC products for flat panel display application. From 2008 to 2013, he was with Renesas Electronics, where he was involved in developing power management IC product for CPU of PC/Server applications. Since 2013, he has been with Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer and involved in power management IC and supply modulator IC development. His research interests include the design of power/analog integrated circuits and systems for a cellular application.



Jongwoo Lee (Senior Member, IEEE) received the B.S. degree in EE from Seoul National University, Seoul, South Korea, in 2001, and the M.S. and Ph.D. degrees in EE from the University of Michigan, Ann Arbor, MI, USA, in 2004 and 2008, respectively.

He was a Military Officer (1st LT) with the Ministry of Nation Defense, South Korea, for two and half years. He was an Analog Circuit Designer with BitWave Semiconductor, Inc, Lowell, MA, USA, from 2008 to 2010. He is currently a VP with the System LSI Division, Samsung Electronics. He is currently leading the IC Design Team for RF/Analog at the Mixed-signal Circuit Design Team. His research and products include RF/analog circuit for low power data converter, multi-mode RF transceivers including 5G millimeter wave, and power IC.

Dr. Lee has been a TPC Member of ISSCC from 2019 and ASSCC from 2013.



Thomas Byunghak Cho (Senior Member, IEEE) received the B.S. degree in electrical engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 1991 and 1995, respectively.

In 1996, he joined Level One Communications, where he was involved in developing CMOS RF transceiver products for cordless phone applications. In 2000, he co-founded Wireless Interface Technologies, where he was involved in developing CMOS RF transceivers for WPAN/WLAN applications. In 2004, he joined Marvell Semiconductor, Santa Clara, CA, USA, where he was involved in developing CMOS RF and analog IC products for various wired and wireless connectivity applications. Since 2012, he has been with Samsung Electronics, Hwaseong, South Korea, where he is currently the Executive Vice President of the Infra and Design Technology Center, in charge of RF/analog IC and multimedia IP development, digital physical implementation, and design verification.



Inyup Kang received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from UCLA, Los Angeles, CA, USA, in 1996.

From 1996 to 2009, he was a Vice President of technology with Qualcomm, where he led generations of cellular modem chipsets. After joining Samsung Electronics in 2010, he was the Chief Director of the DMC Lab, San Diego, CA, USA. He was an Executive Vice President with Samsung, in charge of research and development and commercialization of cellular baseband/RF chipsets, as well as software for 2G, 3G, and 4G. After appointed to the President, his vision in leading modem industry resulted in 5G that in 2019, the world-first commercialization of 5G has been successfully done by his effort to provide 5G total modem solution including Exynos S5100 Modem and RF chipsets. He led numerous research and development teams in and out of the company. He is currently the President and the General Manager of the System LSI Business, Device Solutions Division, Samsung Electronics. His achievements in system-on-chip (SoC) development include commercialization of the industry's first 14- and 10-nm SoC. The 10-nm SoC, Exynos 9 (8895), also integrates support for 5-band carrier aggregation modems for the first time in the industry. It directed to the development of ground-breaking 6-band and 7-band carrier aggregation which has also been under his management. Also, the efforts to bringing A.I. into processors have made the Exynos 9820 to implement the powerful A.I. supported by NPU. He is also in charge of other business such as image sensor and DDI which have been proven the best in the industry. The technology breakthrough has been made by applying three-stack structure which stacked sensor, logic, and DRAM to be integrated into one chip for faster image processing. This led to industry's first commercialization of the smallest 0.8- μ m pixel sized image sensor. Based on such advance, the image sensor business is leading the pixel technology by applying high resolution in small pixel. Moreover, in OLED Driver IC Industry, S.LSI is inevitably conveying the world's best pioneering technology based on 28-nm process and below. Owing to his experience and insight in technologies regarding overall system semiconductor, Samsung's System LSI Business has become one of the key players in the mobile industry with his development of numerous innovative products.