26.5 A Compact Dual-Band Digital Doherty Power Amplifier Using Parallel-Combining Transformer for Cellular NB-IoT Applications

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Narrowband Internet-of-Things (NB-IoT) is a newly developed 3GPP protocol optimized for low-power wide-area IoT applications and is evolving toward the future fifth-generation (5G) mobile communication. It specifies at least 23dBm maximum output power for long-range communication, stringent emission mask compatible with guard-band or in-band scenarios, and it supports multiple operation bands from 699 to 915MHz (LB) and from 1710 to 1980MHz (HB). For cost reduction, longer battery life, and fast time to market, the integration of high-power high-efficiency power amplifiers (PAs) on-chip is greatly demanded. To benefit from advanced CMOS technology, the digital polar transmitter has become a very attractive architecture for NB-IoT applications [1]. To simultaneously support dual bands for user flexibility, the traditional solution is to implement two separately optimized PAs [2], which requires extra design effort and increases die area. An ultra-compact single-transformer-based parallel power combiner proposed in [3] provides optimum load transformation in the two operation bands. Moreover, to support higher throughputs and achieve better spectral efficiency, high peak-to-average-power-ratio (PAPR) multi-subcarrier modulation is adopted in NB-IoT, which requires the PA to be efficient not only at peak power but also at power back-off (PBO) to extend battery life. Efficiency boosting techniques of digital Doherty PAs have been shown in [4-6], but two transformers are needed in the passive network. In this work, a high-power digital Doherty PA for NB-IoT applications is proposed and introduces a parallel-combining-transformer (PCT) power combiner for dual-band coverage, back-off efficiency enhancement, and ultra-compact implementation.

Figure 26.5.1 illustrates the operations of proposed Doherty PA through a PCT combiner. The 3-coil current-mode combiner acts as a 4-way power combiner, where the two primary coils are driven by two differential PA pairs to collect their output currents and provide optimum load transformation. The transformer combiner is configured as shown in Fig. 26.5.1 to maintain both PA pairs quasi-differential and close to each other, which is critical to minimize differential mismatch and to reduce effective ground parasitics. At peak power, both PAs are fully switched on and the currents flow through the two primary coils in-phase at full amplitude. Here, the single-ended impedance seen by each PA is 50Ω. In the case where both PAs are controlled synchronously, load impedance of each PA stays the same when output power is gradually backed off from peak. If operated as Class-B mode, at 6dB PBO, the DC power consumption is only reduced by half, which suffers from 50% efficiency degradation. In this work, each PA pair is controlled independently to perform as a Doherty PA. With output power decreased, output power from PA2 is gradually reduced, and the single-ended impedance seen by PA1 starts to increase until it reaches 100Ω. Then, an efficiency peaking at 6dB PBO is achieved when PA2 is fully switched off, thereby enhancing the average efficiency.

Figure 26.5.2 shows the block diagram of proposed digital Doherty PA. The switched-capacitor digital PA is employed due to its good linearity and efficiency. To meet the stringent NB-IoT emission mask, a total resolution of 10 bits is adopted, where PA1 and PA2 are identical 9b sub-PAs. To minimize layout mismatch and achieve better resolution, each sub-PA is constructed using a hybrid unary and binary array. The sub-PA is divided into 16 groups with the 4 MSBs, where each group consists of 7 thermometer-coded cells and 2b LSB binary-coded cells. A cascode inverter Class-D topology is employed in the unit PA cell to distribute $2\times V_{DD}$ voltage stress among 4 transistors and provide high output power. Single-ended PM signal is converted by an S-to-D block to generate differential signals, which are further level-shifted to two voltage domains. At off-state, the differential outputs of the unit PA are both connected to ground to avoid different fluctuations between supply and ground. Besides, metal-oxide-metal (MOM) switched capacitors formed by middle metal layers are used to reduce parasitic capacitors. In the floorplan, each sub-PA is arranged in order of groups and the "snake" traverse movements are performed among groups to improve the differential nonlinearities (DNL).

Figure 26.5.3 shows the implementation of dual-band passive matching network. The 3-coil parallel-combining transformer is implemented within a compact single-transformer footprint. PA1 and PA2 are placed at the same side of the transformer to maintain good differential symmetry. The output currents from PA1 and PA2 flow in parallel direction in the two primary coils, which achieves magnetic enhancement and increases the effective primary inductance, thus contributing to further size reduction and lower loss. This is important for on-chip matching design at sub-GHz. The passive matching network of the PA device parasitic capacitors, switched capacitors (C_0), a 3-coil transformer, and 3 capacitors (C_1 and C_2) transforms the optimum load for PA1 and PA2, which realizes two power peaks over LB and HB. The total passive loss from sub-PA to 50Ω load is less than 1.6dB over a wide frequency range. The balun function is implemented on-chip with a single-ended output pad. In this work, a total of 1.2nF decoupling capacitors are integrated to attenuate supply and ground ringing while improving the linearity and noise performance.

The proposed dual-band digital Doherty PA is implemented in a 55nm CMOS process (Fig. 26.5.7) and occupies an area of $1.26\times0.88mm^2$ including all decoupling capacitors and ESD I/O pads. The PA is packaged in a QFN package and surface mounted on an evaluation PCB board with a single-ended LO input and an RF output. The chip operates with dual power supplies of 2.4V and 1.2V, and the power consumption of all IO buffers, LO distribution drivers, logic blocks, and PAs is included in the PAE calculation. The measured dual-band continuous-wave (CW) results are shown in Fig. 26.5.4, where the LB achieves 28.9dBm peak power with 36.8% peak PAE, and the HB obtains 27.0dBm peak power with 25.4% peak PAE. The relatively flat output power is achieved over LB and HB, respectively, with the maximum power deviations of 0.3dB and 0.2dB within the frequency bands. Owing to the Doherty load, the PAE of 29.9% and 16.8% is achieved at 6dB PBO for 850MHz and 1.7GHz, respectively, showing the average efficiency enhancement.

In modulation tests, memoryless digital pre-distortion look-up tables are utilized to linearize the PA. With the 12-subcarrier NB-IoT signals, the PA output spectrum meets the stringent NB-IoT emission-mask requirements across both LB/HB bands, as demonstrated in Fig. 26.5.5. With -21.6dB EVM, the PA achieves the P_{avg} of 24.4dBm with average PAE of 29.5% at 850MHz, and the P_{avg} of 23.0dBm with average PAE of 17.9% at 1.7GHz. Moreover, this PA can be applied to wideband communication, such as WLAN and LTE. With 20MHz 64-QAM/256-QAM WLAN signals, the PA obtains 22.9dBm P_{avg}, 26.1% average PAE, -25.3dB EVM and 20.8dBm P_{avg}, 22.7% average PAE, -30.5dB EVM, respectively. The measured performance of proposed PA is summarized in Fig. 26.5.6 and compared with prior works. This work delivers a close-to-Watt-level peak output power and the best average PAE with on-chip matching at sub-GHz among results in Fig. 26.5.6. By using a parallel-combining-transformer power combiner, the dual-band frequency coverage, high output power, and backoff efficiency enhancement are simultaneously achieved with the smallest footprint, thus well-fitting low-cost NB-IoT applications.

Acknowledgements:
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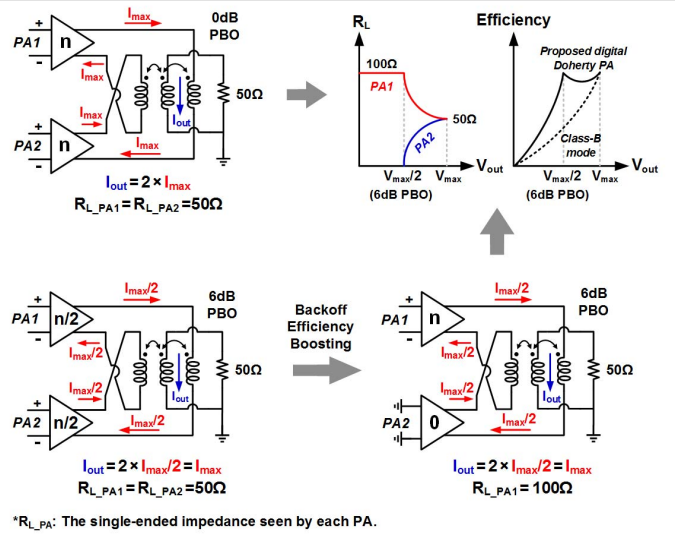

Figure 26.5.1: Digital Doherty PA operation at 0dB/6dB PBO using parallel combing transformer.

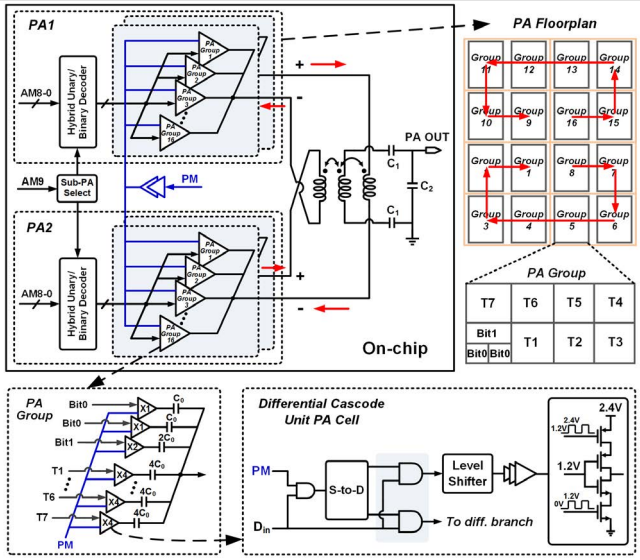

Figure 26.5.2: Block diagram of the proposed dual-band digital Doherty PA.

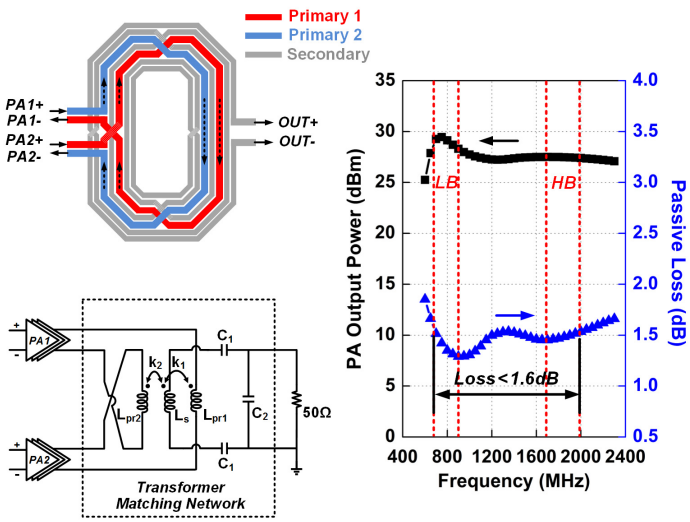

Figure 26.5.3: Implementation of dual-band passive matching network and its simulation results.

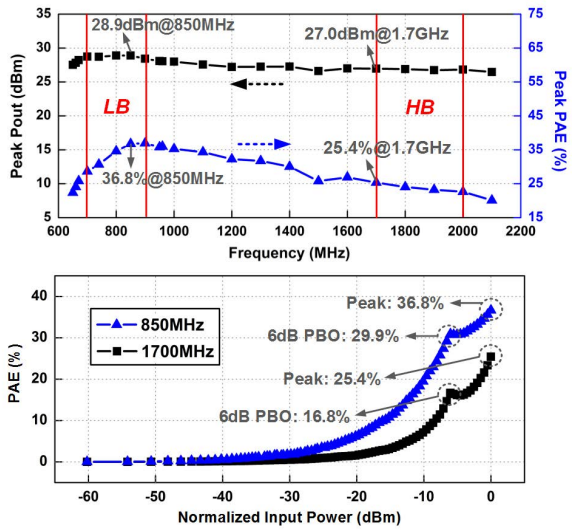

Figure 26.5.4: Measured dual-band CW results of output power, PAE and frequency response.

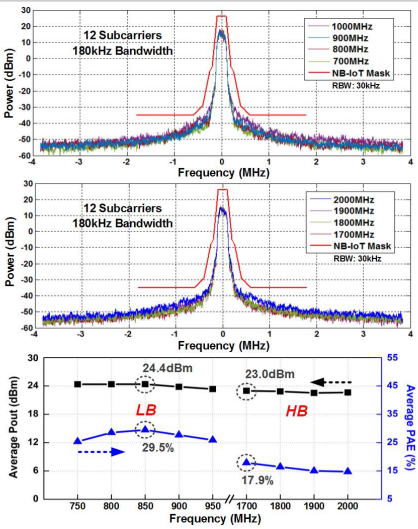

Figure 26.5.5: Measured PA NB-IoT output spectrums and its average P_{out} and PAE versus frequency.

	This work		TCAS-I 2017 [1]†	ISSCC 2015 [2]	JSSC 2016 [3]*	JSSC 2015 [4]*	ISSCC 2017 [5]*
Freq. (GHz)	0.85/1.7		0.891	0.95/1.95	2.6/4.5	3.82	3.5
On-chip Balun	Yes (1 transformer)		No (Off-chip matching)	Yes (2 transformer)	Yes (1 transformer)	Yes (2 transformer)	Yes (2 transformer)
Peak Pout (dBm)	28.9/27.0		23.2	32	28.1/26.0	27.3	25.3
Peak PAE (%)	36.8/25.4		44.5	-	35/21.2	32.5 (DE)	30.4
6dB PBO PAE (%)	29.9/16.8		-	-	-	22 (DE)**	25.3
Modulation	12 Subcarriers 180kHz NB-IoT	20MHz 64QAM/256QAM WLAN @LB	Single Carrier, 3.75kHz NB-IoT	HSPA	8MS/s 256QAM	500kS/s 16QAM	32 Carriers, 10MHz 256QAM
Pavg (dBm)	24.4/23.0	22.9/20.8	18.87	>26/>26	20.37/18.53	21.8	19.0
PAE (%)	29.5/17.9	26.1/22.7	33.4	23.7/23.8	16.26/13.42	22.1 (DE)	24.0
EVM (dB)	-21.6	-25.3/-30.5	-28.2	-26.6/-23.2	-36.3/-34.6	-25.0	-35.0
Supply (V)	1.2/2.4		2	3	1.5/3	1.2/3	1.2/2.4
Chip Size (mm²)	1.11		1.75	3‡	2.25	2.09	1.2
Technology	55nm CMOS		180nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	45nm CMOS SOI

†Results from the second prototype. ‡Estimated total area of RF DACs, LB PA and PA from chip micrograph.
*Results measured with GSG probe. **Estimated from Fig. 13 in [4].

Figure 26.5.6: Performance summary and comparison with prior works.

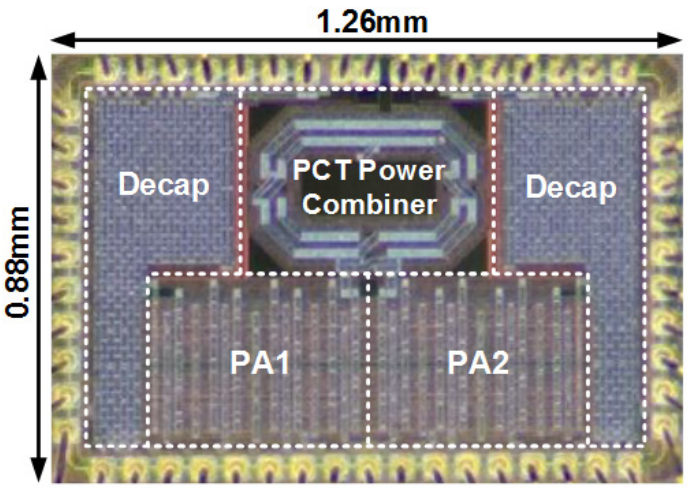

Figure 26.5.7: Die micrograph.

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