An Integrated 700–1200-MHz Class-F PA With Tunable Harmonic Terminations in 0.13-μm CMOS

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***Abstract*—A fully integrated class-F power amplifier (PA) with reconfigurable harmonic termination over a wide range of frequencies is presented. Reconfigurability is achieved by utilizing on-chip transformers as part of the output matching network. In addition, a stacked transistor architecture was used to boost the output power. The PA was fabricated in a 0.13-μm CMOS process and packaged in a 20-pin quad flat no-leads package. It was configured to operate at 700, 900, and 1200 MHz with a maximum measured saturated output power of +24.6 dBm with a power-added efficiency of 48.3%. The measured gain was 16.5 dB and was flat over the entire bandwidth. The total chip area, including pads, is 1.5 mm $\times$ 1.5 mm.**

***Index Terms*—Power amplifiers (PAs), reconfigurable matching network.**

I. Introduction

MAINTAINING high efficiency and good linearity across multiple different frequency bands, modulation standards, and bandwidths are fundamental challenges for next-generation power amplifier (PA) designers. With wireless technology becoming almost ubiquitous and with the types of enriched and enhanced features and services that are provided to the end user, mobile devices are in high demand to support higher data rates [1]–[5]. As a consequence, there is independent development of several spectrally efficient communication standards such as long-term evolution (LTE) and worldwide interoperability for microwave access (WiMAX), which is increasing the number of frequency bands and the amount of spectrum fragmentation [6]. This is creating an environment wherein wireless systems must communicate over many different, sometimes nonadjacent, frequency bands. Furthermore, to facilitate network migration and permit wide geographic roaming, systems must also support multiple legacy-standards as well, further complicating the problem.

In order to provide the required level of support, current transmitters utilize multiple parallel PAs with each separate PA dedicated to a specific communication standard and/or band within a given standard. As a result, large, complex, and expensive PA modules are inevitable. In an effort to address this issue, researchers have recently begun to develop frequency-agile PAs capable of covering several frequency bands [3], [7]–[9]. Several common techniques for increasing the versatility of PAs exist: using a single power cell bundled with many parallel matching networks and switches [7]; using reconfigurable matching networks [8]; and using broadband PAs that simultaneously cover all desired frequency bands [3], [9].

Using a single power cell with multiple switched matching networks is not much more area efficient than using multiple parallel PAs. The size of the passive matching network, which typically will not scale with technology, can easily rival the size of the power cell. Another potentially more serious issue with switchable matching networks is the insertion loss of the switches that directly reduces efficiency. The area of the matching network can be reduced by using a reconfigurable matching network, where the usage of tunable elements, most notably varactors [8], can allow the tuning of a single matching network over a wide range of frequencies. Using tunable elements in the signal path, however, can result in serious nonlinear distortion.

Another approach is to use broadband PAs in order to cover multiple bands simultaneously. A very common method to achieving wideband operation is to use a distributed architecture [10]. Unfortunately, distributed PAs suffer from large area and relatively low efficiencies. An alternative is to use a broadband output matching network [9], but these are not compatible with some currently popular high-efficiency PA architectures.

In this paper, we present a fully integrated CMOS class-F PA capable of reconfigurable operation from 700 to 1200 MHz. Other high-efficiency switch-mode/harmonic-tuned PA topologies exist, such as class-D, class-E, and class-J, but due to the limited device speed, class-D topologies are of limited use at microwave frequencies. Class-E PA topologies also have device speed limitations as well as drain voltages as large as 3.6 times the supply voltage, making class-E difficult to realize in low-breakdown technologies such as CMOS. Class-F, on the other hand, has a maximum drain voltage that is only two times higher than the supply, and therefore more amenable for CMOS implementation [11]–[14].

The bandwidth of a class-F PA is limited in practice by the requirement to precisely terminate the second and third harmonics at the output. One way to increase the bandwidth is to use a class-J topology, which requires a reactive component at the fundamental to maintain the second harmonic phasing thereby boosting efficiency [15]. Class-J becomes overly complex, however, and is not well suited for the type of load tuning we are proposing. The proposed system gets around this

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TABLE I
CLASS-F EFFICIENCY AS A FUNCTION OF VOLTAGE AND CURRENT HARMONIC CONTENT

Current Harmonic Comp.	Voltage Harmonic Component		
	1	1,3	1,3,5,…,∞
1	0.500	0.563	0.637
1,2	0.667	**0.750**	0.849
1,2,4,…,∞	0.785	0.884	1.000

issue by using a novel reconfigurable output matching network capable of providing real-time tuning of the second and third harmonic terminations to support a fundamental frequency range of 700–1200 MHz. High efficiency over the entire range of frequencies is thereby maintained. This reconfigurability is achieved through the use of integrated transformers [16]–[18] and a bank of parallel capacitors. It is important to realize that this PA is not intended for signals with instantaneous bandwidths of 500 MHz, instead it supports narrowband signals over a wide range of potential carrier frequencies. Moreover, all techniques presented can be easily adapted to a class-F^{-1} topology.

This paper is organized as follows. In Section II, the design theory of the proposed PA is presented and the reconfigurable output matching network is explained. The circuit implementation is discussed in Section III. In Section IV, experimental results are presented, and finally, this paper concludes in Section V.

II. DESIGN OF A TRANSFORMER-BASED RECONFIGURABLE PA

A. Traditional Class-F Operation

An ideal class-F PA can achieve a theoretical drain efficiency of 100% by using harmonic resonators in the output matching network to shape the drain–voltage and drain–current waveforms. A maximized efficiency is achieved when the drain–voltage is a square wave and the drain–current is a half-rectified sine wave and this condition is achieved by presenting a short-circuit to all even-order harmonics and an open-circuit to all odd-order harmonics. Table I shows how the efficiency changes with varying levels of harmonic control [19]. In practice, controlling harmonics beyond the third harmonic results in a significant increase in complexity with only marginal improvements in the overall efficiency [4] so many practical designs only control the second harmonic of the drain current and the third harmonic of the drain voltage, which, from Table I, results in a theoretical maximum drain efficiency of 75%.

B. Transformer-Based Output Network

In typical class-F operation, resonators (both lumped and distributed) are used for harmonic peaking at fixed frequencies, thereby limiting the overall bandwidth of the PA. At the heart of the proposed tunable class-F load is a high-order transformer-based resonator, shown in Fig. 1(a), that allows the user to control the frequency at which the load presents a short circuit (e.g., for terminating the second harmonic) and an open circuit (e.g., for terminating the third harmonic). A simple analysis of the resonator shows that the input impedance of the network is

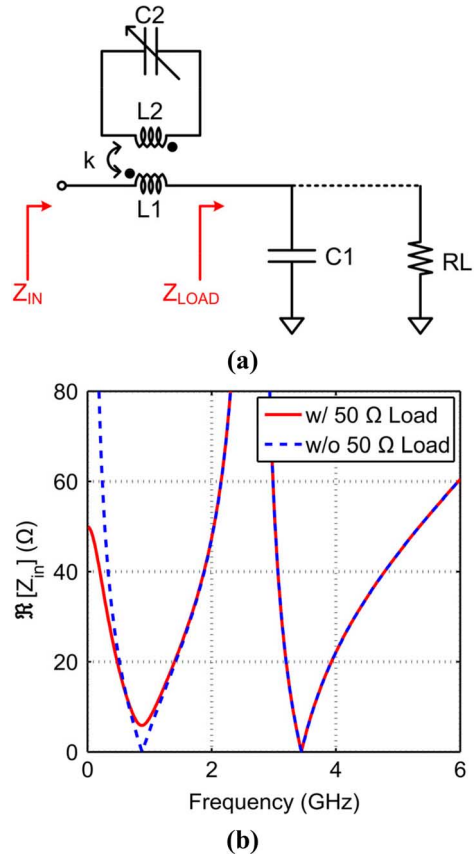

Fig. 1. (a) Schematic of the proposed fourth-order resonant tank and (b) frequency response of Z_{IN} with real and complex load.

$$Z_{\mathrm{IN}}(s) = sL_1 - \frac{s^2M^2}{sL_2 + 1/sC_2} + Z_{\mathrm{LOAD}}(s) \tag{1}$$

where $M = k\sqrt{L_1L_2}$ is the mutual inductance between inductors L_1 and L_2 with coupling coefficient k. In order to simplify the analysis and gain some insight, we begin by assuming that the load impedance is purely capacitive and $Z_{\mathrm{LOAD}} = 1/sC_1$. The input impedance can now be written as

$$Z_{\mathrm{IN}}(s) = \frac{s^4\left(L_1C_1C_2 - k^2C_1C_2L_1^2\right) + s^2\left(C_1 + C_2\right)L_1 + 1}{sC_1(s^2L_2C_2 + 1)}. \tag{2}$$

Under these assumptions, it can be shown that Z_{IN} has a pole at dc and a pair of complex conjugate poles located at

$$f_{p2,3} = \pm\frac{1}{2\pi}\sqrt{\frac{1}{L_2C_2}} \tag{3}$$

and two real zeroes located at

$$f_{z1} = \frac{f_1^2 + f_2^2 - \sqrt{f_1^4 + f_2^4 + f_1^2f_2^2(4k^2 - 2)}}{2(1 - k^2)} \tag{4}$$

$$f_{z2} = \frac{f_1^2 + f_2^2 + \sqrt{f_1^4 + f_2^4 + f_1^2f_2^2(4k^2 - 2)}}{2(1 - k^2)} \tag{5}$$

where $f_1 = 1/(2\pi\sqrt{L_1C_1})$ and $f_2 = 1/(2\pi\sqrt{L_2C_2})$.

We aim to control the location of the poles and zeroes given the five parameters L_1, C_1, L_2, C_2, and k. From this point forward, we will consider our system as having two distinct zeroes located at f_{z1} and f_{z2} and a pole located at $f_{p2,3}$ because the complex poles will have the same real part. It can be shown from (2)–(5) that only two of the three poles/zeroes can be independently controlled. In the realm of class-F PA design, we would like to place the low-frequency zero, f_{z1}, at the fundamental. A high-impedance open circuit can then be placed at the third harmonic by setting the complex conjugate poles, $f_{p2,3}$, appropriately. The high frequency zero, f_{z2}, will then fall outside of the band of interest.

In the above analysis, Z_{LOAD} was assumed to be purely capacitive. When a resistor, R_L, is added in parallel with C_1, the expression for the input impedance becomes (6), shown at the bottom of this page. Notice that the location of the poles $f_{p2,3}$ and the zeros $f_{z1,2}$ have not changed. The dc pole, however, has been shifted and is now located at $f_{p1} = 1/(2\pi R_L C_1)$. This will cause a slight change in the reactance of Z_{IN} at low frequencies (outside of the band of interest). What is perhaps not as obvious is the fact that the load network in Fig. 1(a) can be used as an impedance transformation network in the low band where the transformation ratio is controlled by the values of L_1 and C_1.

As an example, consider a class-F PA operating at 900 MHz. We wish to pass the fundamental frequency by setting $f_{z1} =$ 900 MHz while providing a high impedance to the third harmonic by setting $f_{p2,3} = 2700$ MHz (in this example, we are neglecting the short circuit presented at the second harmonic, which can be achieved by including an additional transformer network). Such a network can be realized using $L_1 = 4$ nH, $L_2 = 2.4$ nH, $k = 0.6, C_1 = 7.5$ pF, and $C_2 = 1.4$ pF. The input impedance for this example is plotted in Fig. 1(b) for two cases: when Z_{LOAD} is purely capacitive and when Z_{LOAD} is complex. As expected, the network presents a low impedance at 900 MHz and a very high impedance at 2700 MHz. Also notice that the load network has transformed the 50-Ω load down to approximately 5 Ω. Moreover, the high-frequency zero, f_{z2}, is located at 3450 MHz, well beyond the band of interest.

As previously mentioned, the locations for f_{z1}, f_{z2}, and $f_{p2,3}$ cannot all be set independently and it is seen in (3)–(5) that they all depend upon the values of f_1 and f_2. Graphical visualization is the best way to determine the values of f_1 and f_2 that realize a given desired location of the poles and zeroes. Fig. 2 shows the contours for three different pairs of f_{z1} and $f_{p2,3}$ plotted against f_1 and f_2 with the added condition that $f_{p2,3} = 3f_{z1}$. The points where the contours intersect represent values of f_1 and f_2 that are valid solutions for (3) and (4). To see where the high-frequency zero, f_{z2}, is located, (5) is also plotted in Fig. 2. Doing so shows that there is a unique contour for f_{z2} that passes through each intersection of f_{z1} and $f_{p2,3}$. The different solutions are marked in Fig. 2 by S1, S2, and S3, for the fundamental

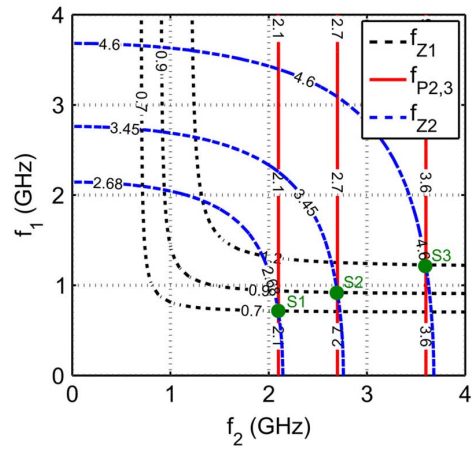

Fig. 2. Contour plot of f_{z1}, $f_{p2,3}$, and f_{z2} as functions of f_1 and f_2. Points S1, S2, and S3 indicate valid solutions of f_1 and f_2 for operation at 700, 900, and 1200 MHz, respectively.

frequencies of 700, 900, and 1200 MHz, respectively. In each case, the location of f_{z2} is located at frequencies higher than the third harmonic.

Once the values of f_1 and f_2 have been determined, it becomes necessary to determine the component values for the matching network. At this point, however, there are an infinite number of solutions that satisfy a given set of values for f_1 and f_2. The required impedance scaling, however, introduces an additional constraint that results in a set of unique values for L_1, C_1, L_2, and C_2 assuming that the coupling coefficient, k, has been previously set. The coupling coefficient is typically going to be determined by manufacturability considerations and values between 0.4–0.8 are commonly seen in on-chip transformers.

It is necessary, however, to examine the sensitivity of the matching network to variation in the value of the coupling coefficient. The coupling coefficient of on-chip transformers can vary by as much as 20%. To examine the effects of variation in k, the curves in Fig. 2 are re-plotted, keeping all values constant, but with either a 10% decrease in k [see Fig. 3(a)] or a 10% increase in k [see Fig. 3(b)]. It is seen that the location of the complex conjugate poles is insensitive to variations in the coupling coefficient, which is expected from (3). In addition, the low-frequency zero, f_{z1}, shows minimal sensitivity to k as is evidenced by the solutions of f_1 and f_2 for the three cases. The value for f_1/f_2 for points S1, S2, and S3 in Fig. 2 are 0.72/2.1, 0.92/2.7, and 1.23/3.6, respectively. When k is decreased by 10% these values become 0.71/2.1, 0.92/2.7, and 1.23/3.6 and when k is increased by 10% they become 0.72/2.1, 0.93/2.7, and 1.24/3.6. The high-frequency zero, f_{z2}, however, is significantly impacted by variations in the coupling coefficient. This is acceptable, however, because it still remains well above the third harmonic in all cases.

$$Z_{\mathrm{IN}}(s) = \frac{s^4 L_1 C_1 L_2 C_2 R_L (1-k^2) + s^3 L_2 C_2 L_1 (1-k^2) + s^2 R_L (L_1 C_1 + L_2 C_2) + sL_1 + 1}{(sC_1 R_L + 1)(s^2 L_2 C_2 + 1)} \tag{6}$$

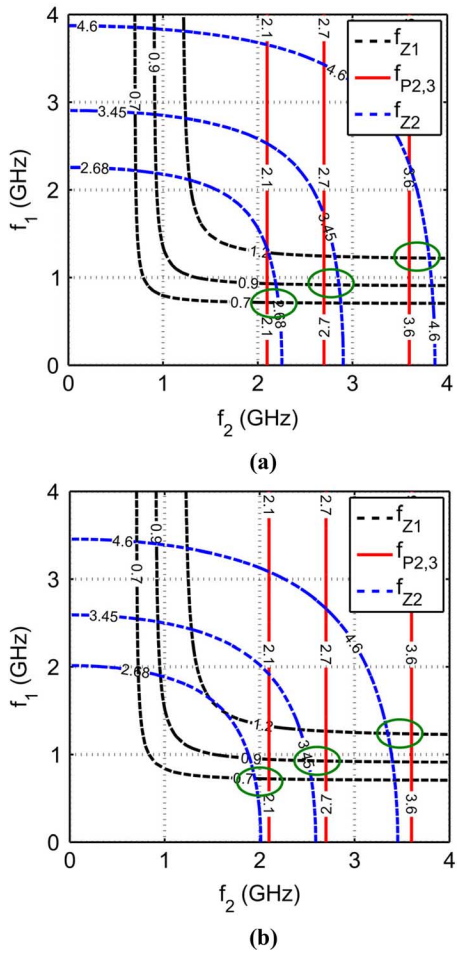

Fig. 3. Contour plots of f_{z1}, $f_{p2,3}$, and f_{z2} as functions of f_1 and f_2 showing variation when: (a) k is decreased by 10% ($k = 0.54$) and (b) k is increased by 10% ($k = 0.66$).

C. Design of the Stacked Field-Effect Transistor (FET) Active Device

Modern CMOS processes are not tolerant to high supply voltages due to the thin gate oxide and its associated low breakdown voltage. If the process-dictated supply voltage is used, a large impedance transformation ratio will be required and the associated loss in the output matching network will reduce efficiency and output power. One way to alleviate this issue is to use a stacked-FET topology [1]. By stacking the transistors, the power cell can withstand a higher supply voltage, resulting in an increased output power for a fixed load impedance. In general, the supply voltage can be scaled by a factor equal to the number of stacked transistors. Avalanche breakdown in the drain/bulk junction can occur, however, which places a fundamental limitation on the number of transistors that can be stacked.

III. Circuit Implementation

The schematic of the proposed fully integrated class-F PA with reconfigurable harmonic termination is shown in Fig. 4 with component values given in Table II. By stacking transistors M1–M4, as shown in Fig. 4, the power cell can now withstand a supply voltage that is four times greater than that of a single transistor. The sizing of transistors M1–M4 is done iteratively with the aid of load–pull simulations. All four devices are identically sized with a length of 0.12 μm and a width of 2400 μm (divided across 140 fingers). The number of fingers is dictated by the peak drain current and is chosen such that the current density through each finger is kept under process maximums. In the targeted 0.13-μm CMOS process, the avalanche breakdown voltage of the drain/bulk junction is greater than 10 V and the oxide breakdown voltage is greater than 4.25 V. From simulation, the maximum drain voltage of M4 is 9.75 V and the maximum voltage drop across any oxide is less than 4 V.

The reconfigurable output matching network is composed of two fourth-order resonators, which were described in Section II. The first resonator, consisting of L_1, L_2, C_1, and C_{T3} controls the location of the third-harmonic open-circuit termination as well as provides the necessary impedance transformation from 50 Ω to the optimum load impedance, as determined from load–pull simulations shown in Table III. Since we cannot dynamically control the real part of $Z_{\rm IN}$, we design the load network to provide the optimum match at 900 MHz knowing that the optimum termination at 700 and 1200 MHz will be close, but not exact, as seen in Table III.

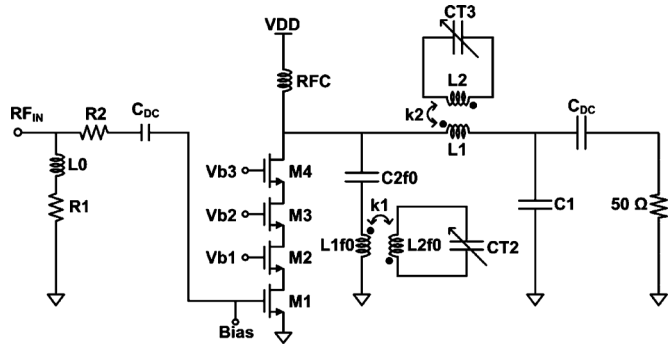

Fig. 4. Simplified schematic of the proposed class-F PA with tunable harmonic termination.

TABLE II
Component Values for Proposed Class-F PA

Component	Value	Component	Value
R1	118.4 Ω	L2f0	2.1 nH
R2	98.7 Ω	C_{DC}	15 pF
L1	4.0 nH	C1	7.5 pF
L2	1.9 nH	C2f0	1.99 pF
L1f0	1.74 nH	CT2	0.2 – 2 pF
L0	9.37 nH	RFC	9.37 nH
CT3	0.3-5.7 pF	k1/k2	0.52/0.65

TABLE III
Load–Pull Simulation at the Frequencies of Operation

Freq. (MHz)	Load (Ω)	Max Power Added Efficiency (%)	Max Pout (dBm)
700	18.93 + *j*14.61	62.00	28.00
900	18.02 + *j*15.36	62.00	28.00
1200	17.62 + *j*15.76	62.00	28.00

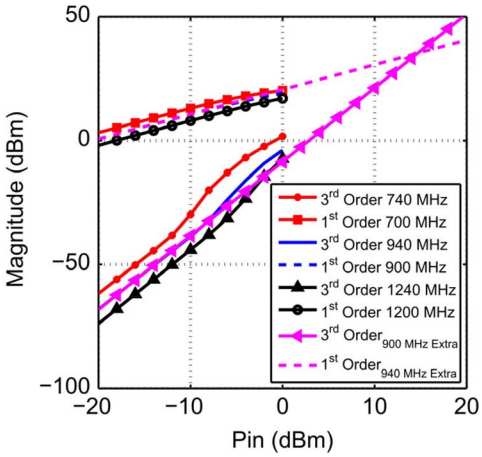

Fig. 5. Simulated OIP3 at 700, 900, and 1200 MHz.

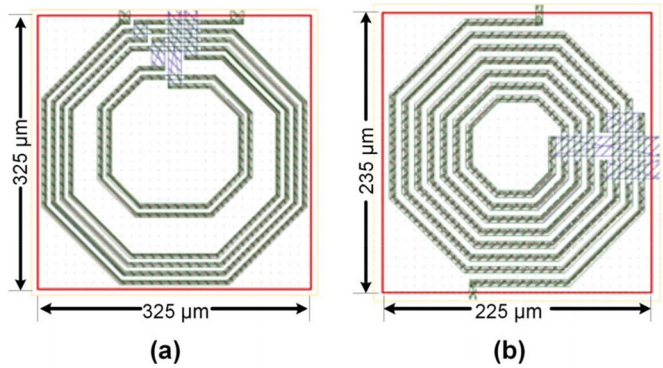

Fig. 6. Layout for the transformer used for: (a) controlling the third harmonic and (b) controlling the second harmonic.

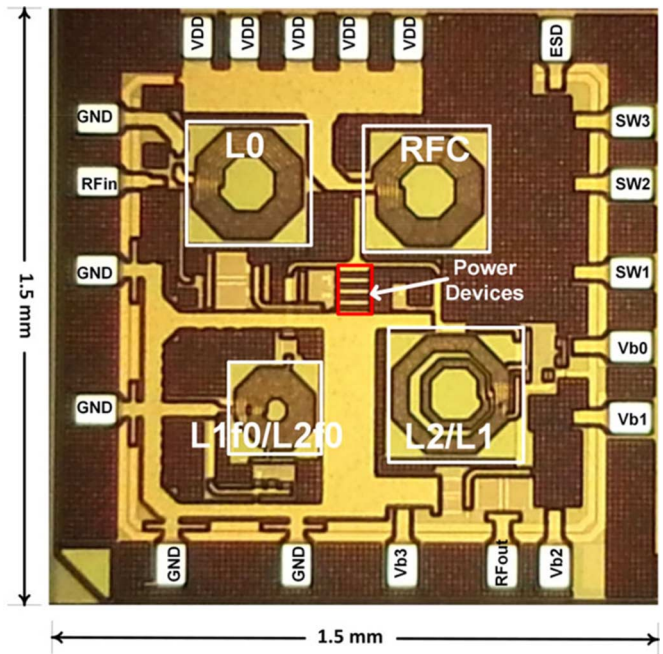

Fig. 7. Die microphotograph.

The second resonator, consisting of L_{1f0}, L_{2f0}, C_{2f0}, and C_{T2}, controls the location of the second-harmonic short-circuit termination. The frequency location of the open- and short-circuit termination can then be controlled via variable capacitors, C_{T3} and C_{T2}, which are realized using a bank of fixed capacitors and switches. All of the switches are identically sized for minimum on-resistance with $W = 750.21$ μm(divided into 51 fingers) and $L = 150$ nm.

Using switches at this point in the load network does not significantly impact the overall performance of the PA because they are partially isolated from the primary RF signal path by the coupling coefficient of the transformers. In addition, the transformer keeps the maximum voltage drop across the capacitor/switch pairs from becoming too large. Simulation results show that the maximum voltage drop across the switch/capacitor combination is only 7.2 V (despite the 9.75-V signal swing at the drain of M4), which is below the process defined maximum, which is greater than 7.5 V.

Any time a tunable element is introduced, there is a potential impact on linearity. The linearity of the PA was evaluated using a two-tone simulation with 20-MHz tone spacing. As shown in Fig. 5, the simulated output third-order intercept point (OIP3) is $+35.46$, $+34.89$, and $+33.07$ dBm at 700, 900, and 1200 MHz, respectively. All intercept points can be seen to be within 0.5 dB of each other, indicating no significant degradation of linearity due to the tunable matching network. This is because the capacitors are fixed-valued capacitors and switching does not occur during active transmission.

The transformers were designed and simulated using ADS Momentum and equivalent lumped-element models were created for use in both time- and frequency-domain simulations. A custom concentric transformer topology was used and the windings were realized as a parallel stack of the top two thick metal layers connected with a dense collection of vias. This will increase the quality factor of the windings and help to minimize the loss in the load network. The layout of the transformers used to control the third-harmonic termination of the drain voltage and second-harmonic termination of the drain current are shown in Fig. 6(a) and (b), respectively. The simulated loss of the matching network is -1.1, -1.5, and -2 dB at 700, 900, and 1200 MHz, respectively, and is dominated by the relatively low-Q of the integrated inductors.

Finally, the input matching network consists of a resistive network with a wideband response as proposed in [20]. The value of R_1 is given by the series combination of R_2 and the parasitic gate resistance of M1, R_g. Resistor R_2 is primarily used for stabilization. The parasitic gate–source capacitance of M1, $C_{\rm gs}$, and the value of R_1 are then used to determine the value of the inductor, L_0, following guidelines found in [20].

IV. Measurement Results

The proposed PA with real-time harmonic termination tuning capability was fabricated in a 0.13-μm CMOS process and occupies a total area of 1.5×1.5 mm^2 including pads. The tunable matching network supports fundamental frequencies between 700–1200 MHz. A die photograph is shown in Fig. 7. For testing purposes, the die was packaged in a 20-pin quad flat no-leads (QFN) package and mounted to a double-layer FR4

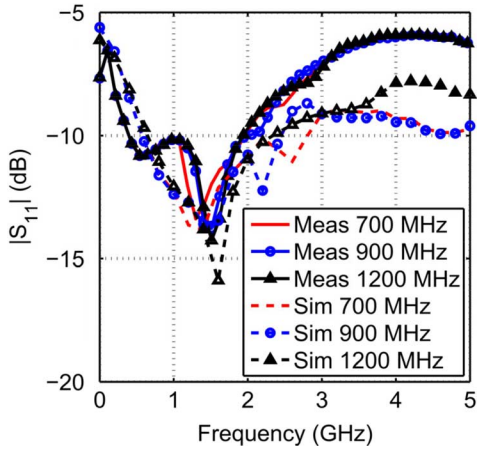

Fig. 8. Measured and simulated $S11$ for operation at 700, 900, and 1200 MHz.

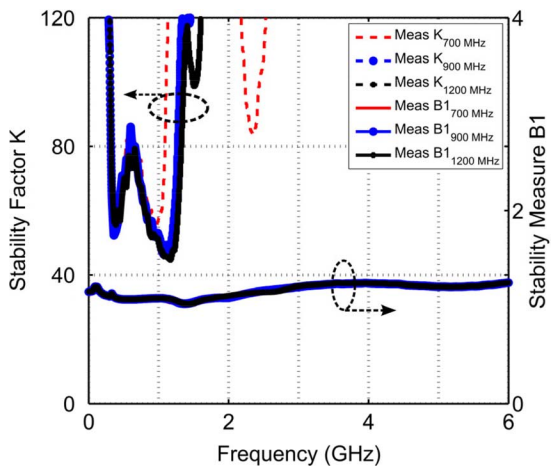

Fig. 9. Measured stability factor K and stability measure $B1$ for the proposed PA.

printed circuit board (PCB). All measurements are thus referred to the edge of the PCB.

Both small- and large-signal characterization was performed. An Agilent 5071C network analyzer was used to measure small-signal S-parameters. Measured $S11$ is compared to simulation in Fig. 8 when the PA is configured to operate at 700, 900, and 1200 MHz. The measured -10-dB bandwidth ranges from 400 to 1800 MHz. The slight deviation from simulated results at high frequencies can be attributed to parasitics in the bond wires and PCB traces The input impedance of the PA at 700, 900, and 1200 MHz is $50.1 - j29.6\ \Omega$, $43.3 - j29.6\ \Omega$, and $36.4 - j20.9\ \Omega$, respectively, and the measured $S22$ is -2.4, -3.5, and -10.3 dB, respectively. Finally, we verified stability over the frequency range from 300 kHz to 6 GHz by plotting the Rollett stability factor, K, and stability measure, $B1$, in Fig. 9 [21]. As seen in Fig. 9, $K > 1$ and $B1 > 0$ for all frequencies, thereby confirming stability.

Simulated and measured values for $S21$ are shown in Fig. 10(a) for 700-MHz operation, Fig. 10(b) for 900-MHz operation, and Fig. 10(c) for 1200-MHz operation. The second - and third-harmonic notches move across frequency to support the various fundamental frequencies in the fixed passband. As shown in Fig. 10, the absolute maximum gain occurs at a frequency lower than the frequency of operation. This is a

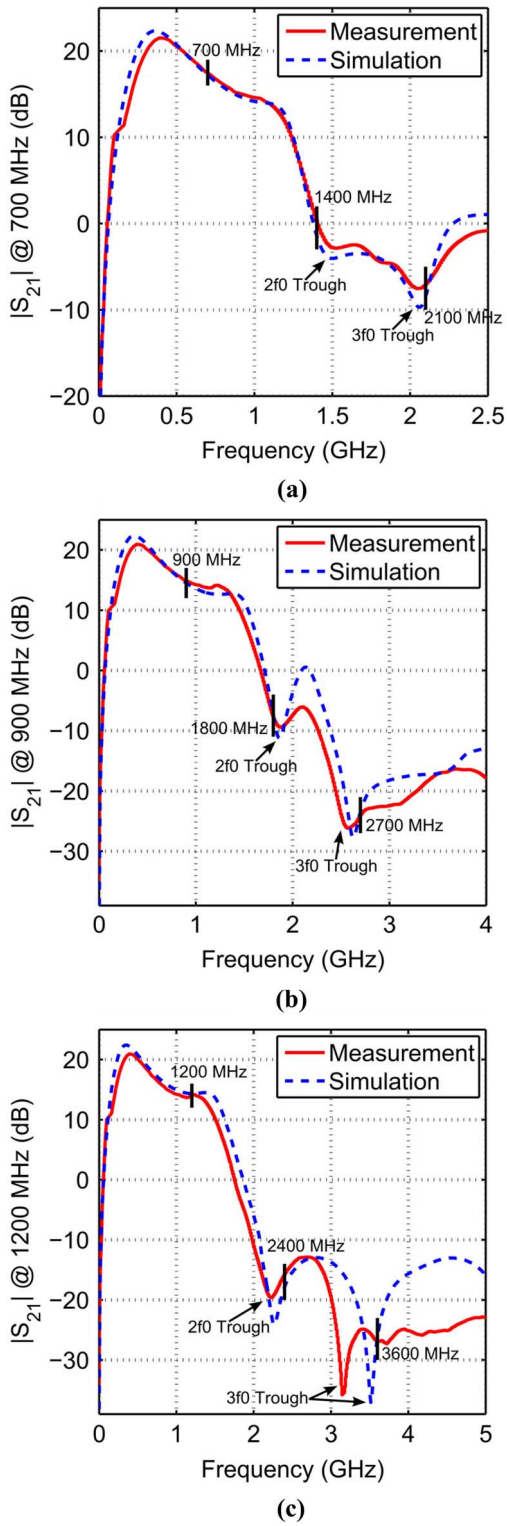

Fig. 10. Simulated and measured small-signal gain at: (a) 700 MHz, (b) 900 MHz, and (c) 1200 MHz.

device-dependent phenomenon also observed by others (e.g., [11]) and not a product of the matching network.

Large-signal characterization was performed using an Agilent E4438C vector signal generator to generate a continuous wave (CW) input and an Agilent E4418B power meter at the output for power measurements. The measured (simulated)

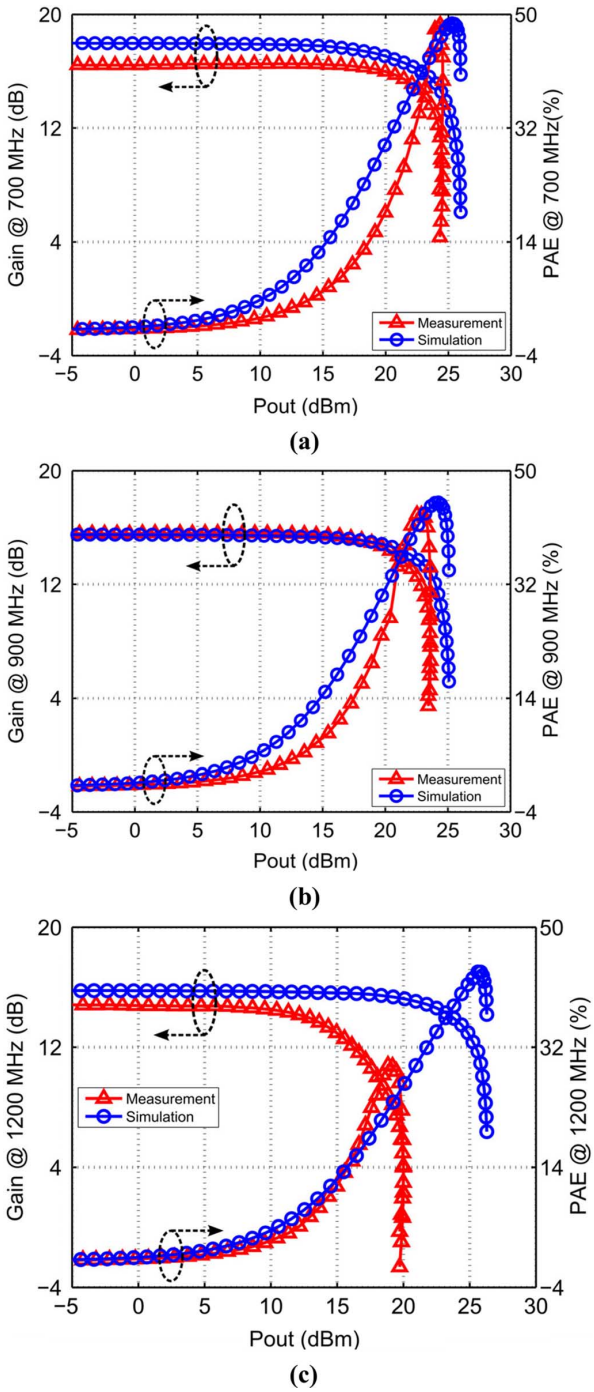

Fig. 11. Simulated and measured large-signal gain and PAE at: (a) 700, (b) 900, and (c) 1200 MHz.

power-added efficiency (PAE) with the PA configured to operate at 700, 900, and 1200 MHz is 48.3% (49%), 45.1% (47%), and 30% (49%), respectively, as shown in Fig. 11(a)–(c). The relatively large drop in PAE at 1200 MHz is attributed to the shift in the location of the third-harmonic termination seen in the small-signal response and will be discussed in more detail later.

The measured (simulated) power gain are also shown in Fig. 11(a)–(c) to be 16.5 dB (17.2 dB), 16.1 dB (16.1 dB), and 14.9 dB (15.6 dB) at 700, 900, and 1200 MHz, respectively. They are relatively flat up to the compression point

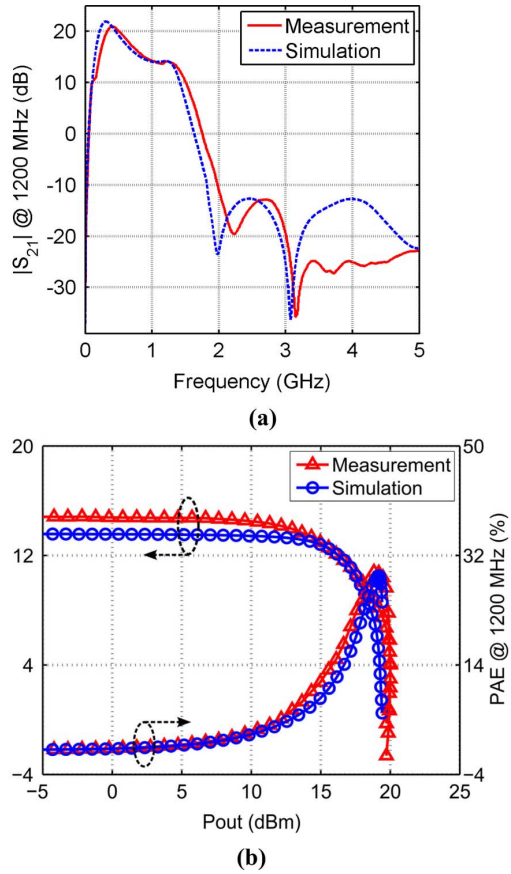

Fig. 12. Simulated and measured: (a) small-signal gain and (b) large-signal gain and PAE for 1200 MHz after model correction.

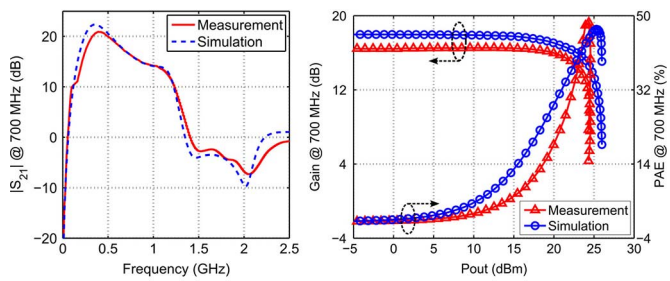

Fig. 13. Simulated and measured: (a) small-signal gain and (b) large-signal gain and PAE for 700 MHz after model correction.

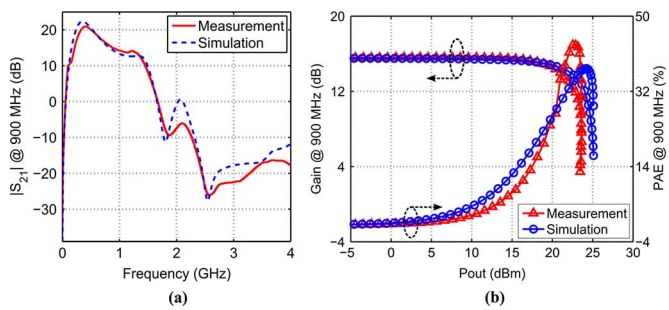

Fig. 14. Simulated and measured: (a) small-signal gain and (b) large-signal gain and PAE for 900 MHz after model correction.

for each mode. Finally, the measured (simulated) maximum saturated output power for each mode is 24.6 dBm (26.5 dBm), 24.0 dBm (26.0 dBm), and 20.1 dBm (25.0 dBm).

TABLE IV
SUMMARY OF PA PERFORMANCE COMPARED TO PREVIOUSLY PUBLISHED DESIGNS

Reference	Technology	Frequency (GHz)	Modulation Scheme	Max VDD (V)	Psat (dBm)	Peak PAE (%)	Max Gain (dB)	Area (mm^2)	Class	Notes
[1]	0.13 μm SOI CMOS	1.9	WCDMA	6.5	29.4	41.4	14.6	0.671	AB	OMN with off-chip stubs
[2]	0.18 μm CMOS	1–5	64 QAM 54 Mb/s	5.0	20–22	18–36	18–20	0.684	N/A	series transformers on-chip at input
[3]	90 nm CMOS	5.2–13	CW	2.8	25.2	21.6	18.5	0.698	AB	Fully integrated
[22]	0.13 μm CMOS	0.6–2.8	CW	1.5	21	16 (drain)	20	3.60	A	Fully integrated
[23]	0.18 μm CMOS	5.0	CW	2.0	15.4	40.6	NA	0.810	E	Fully integrated
[5]	0.13 μm CMOS	2.4	64 QAM 54 Mb/s	3.3	19.5	24.8	21	1.12	B/C	Fully integrated
[24]	65 nm CMOS	1.8	CW	3.3	18.0	21.3	12.5*	5.2	G	Fully integrated
[25]	0.18 μm CMOS	1.95	CW	3.4	26.0	46.4	26	0.832	N/A	Fully integrated
[26]	90 nm CMOS	1.9	CW	2.5	24.0	12	NA	3.69	E	Fully integrated
[27]	0.18 μm CMOS	1.95	WCDMA	3.3	26.0	20	19.9	1.32	N/A	Two chip with LINC**
[11]	0.6 μm CMOS	1.9	CW	3.0	22.8	42	10.5	N/A	F	MMIC
[12]	0.18 μm CMOS	2.6	WiMAX	1.8	20.2	24.4	13.1	0.998	F	Off chip Harmonic Control
[13]	65 nm CMOS	0.1 -1.5	CW	2.5	24.2	64.0	23	N/A	AB/F	Off chip Harmonic control
[28]	0.18 μm CMOS	0.824-0.915	3G LTE	3.3	26.7	32.2	31.2	1.496	F	Off chip OMN and feedback
[14]	0.18 μm CMOS	1.95	CW	3.4	30.5	42.1	24	2.727	N/A	Fully integrated
[29]	0.25 μm CMOS SOS	1.4	CW/LTE /WCDMA	16	34.4	38	11	2.16	N/A	Off chip Choke
This Work	0.13 μm CMOS	0.7–1.2	CW	4.8	24.6–20.1	48.3 – 30.0	16.5–14.9	2.25	F	Fully integrated

* Drain Efficiency ** Linear amplification using nonlinear components

In general, there is good agreement between measurements and simulation, especially at 700 and 900 MHz. There is, however, a downward shift in the location of the third-harmonic notch when the PA was tuned to operate at 1200 MHz. This has been investigated and the shift in frequencies is due to component variation, specifically, variation in the transformer. The high-frequency mode of operation is more sensitive to component variation than the low-frequency modes, which is partially indicated by Fig. 3. In addition, increased temperature also served as a source of discrepancy in both small- and large-signal performance, specifically in the saturated output power measurements (where heating is most likely to occur).

Our hypothesis was tested in simulation. First, the self-inductance of L_{2f0} was increased from 1.74 to 1.95 nH and L_2 was increased from 1.9 to 2.12 nH, a change of 1.2% and 12%, respectively. In addition, the part temperature was increased in simulation, which brought the measurement and simulation values into close agreement, as shown in Fig. 12. We also compared measurement results at 700 and 900 MHz to simulation using these new values for L_{2f0} and L_2 in Figs. 13 and 14. It can be seen that there is still good agreement between measurements and simulation supporting our hypothesis. Table IV summarizes the measured results and compares them with previously published works (both tunable and nontunable PAs). It is seen that the proposed PA has among the highest PAE and saturated output power of all fully integrated CMOS PAs. In addition, this design provides a significant tuning range, thus supporting a wide range of carrier frequencies. The relatively high output power achieved in [1] can be attributed to the use of off-chip components, including transmission lines, for the matching network, which provide higher Q.

V. CONCLUSION

A novel transformer-based 700–1200-MHz class-F PA with real-time tunable harmonic termination capability has been proposed and fabricated in a standard 0.13-μm CMOS process. A stacked-FET approach is used for the core device in order to overcome the low breakdown voltage common with CMOS processes. This, in turn, allows the use of a higher supply voltage for higher output power and high efficiency. The fabricated PA exhibits a maximum measured PAE of 48.3%, 45.1%, and 30% for operation at 700, 900, and 1200 MHz, respectively, with a saturated output power ranging from 20.1 to 24.6 dBm. We have demonstrated that the proposed reconfigurable harmonic matching network provides a means for achieving high output power and efficiency over a wide range of operating frequencies vital for next-generation cognitive wireless communication systems.

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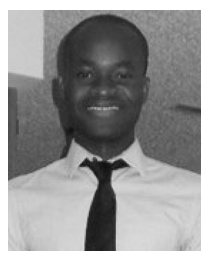

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