10.1 A 1.5W Class-F RF Power Amplifier in 0.2µm CMOS Technology

Timothy C. Kuo, Bruce B. Lusignan*

Philips Semiconductors, San Jose, CA
*Stanford University, Stanford, CA

Despite recent progress in RF CMOS, designing a power amplifier (PA) in deep sub-micron CMOS technology remains difficult. Although a standard digital CMOS process is not an attractive choice for power amplifier, A CMOS PA can provide significant market value when integrated with the rest of the CMOS transceiver. Designing a PA in deep sub-micron CMOS faces two major challenges: high knee voltage of the I-V curve and low oxide breakdown voltage. Methods of resolving these issues are the focus of this paper.

CMOS PAs implemented in class D [1] or class E [2,3] switching mode are reported recently. However, a class C or class F amplification-mode PA is not yet published. Compared with class F, the class E PA suffers a major disadvantage: stress on the device. The voltage swing on the output node for a class E PA can be as high as $3.6V_{dd}$ while for class F, only $2V_{dd}$ is needed. Therefore, a class F PA is more suitable for low breakdown voltage CMOS technology and is chosen for this implementation. Traditionally, amplification mode PA starts its design with the load line method as shown in Figure 10.1.1. The knee voltage divides saturation and linear regiosn of the transistor and can be defined as, for example, Vds at the 95% Imax point. The optimum load resistance is

$$R_{opt} = \frac{V_{sup} - V_{knee}}{I_{max}/2} \quad (1)$$

While this is an effective approach for most power transistors, it is not suitable for deep sub-micron CMOS transistors. This is mainly due to the fact that V_{knee} is only about 10 to 15% of the supply voltage for typical power transistors, while it can be as high as 50% of V_{sup} for a deep sub-micron CMOS transistor. Therefore, precluding the CMOS transistor from operating in the linear region does not result in optimum output power. In fact, a large portion of the RF cycle can be in the linear region. Therefore, both saturation and linear regions must be considered when determining R_{opt}. Although a SPICE-like simulator can take this into account, the process of finding R_{opt} is time consuming. To speed up the process, a DC I-V approach implemented in Matlab is proposed. The procedure is shown in Figure 10.1.2a. To account for the linear region, a unified I-V equation proposed by Tsividis is used [4]:

$$I_d = \frac{1}{2}\,\mu\,Cox\left(\frac{W}{L}\right)\left(\frac{1}{n}\right)\left[(V_{GS}-V_T)^2 - (2n\Phi_t)^2 \ln^2\left(1+e^{\frac{V_{GS}-V_T-nV_{DS}}{2n\Phi_t}}\right)\right] \quad (2)$$

Assume that the drain Vd is synchronized with gate-driving waveform Vg, the drain current Id is obtained from Equation 2. The RF power can be calculated from taking the Fourier component of Id and the efficiency can then be calculated. An efficiency and output power plot versus different output amplitude Vo and conduction angle ϕ for a 0.2µm transistor is shown in Figure 10.1.2b. Note that for a given ϕ, an optimum Vo exists for maximum output power, which corresponds to the R_{opt}. Although efficiency can be improved by reducing conduction angle, the output power also decreases. Therefore, for a fixed output power, a larger transistor is required, resulting in higher driver power and larger output parasitic capacitance. One of the major issues with a CMOS PA is the reliability concern due to low oxide breakdown voltage. Although class F amplifiers somewhat relax this requirement, the supply is still limited to about 1.2V for a 0.2µm transistor. Such a low supply voltage demands too low an impedence level, especially when package parasitics are considered. To boost the supply voltage, a cascode configuration is shown in Figure 10.1.3. To further boost the supply, a thick gate oxide (80Å) transistor is used for cascode transistor M2. The gate of M2 is biased at 3V, which allows the output node to sustain 7V without damaging the transistor. For a class F amplifier, the maximum supply voltage can be raised to 3.5V. The thin gate oxide transistor M1 is now protected by M2 with no reliability threat. Since dual gate oxide transistors are widely available in deep sub-micron CMOS, it is not considered a special process requirement. Note that higher supply voltage is gained at the cost of reduced power efficiency because M2 acts as a resistor in series resistor with the output. In addition to gate oxide, the pn junction can also break down. However, since the pn junction has a much higher breakdown voltage, it is not a major concern here.

Most PA pre-drivers are based on inductor tuning as shown in Figure 10.1.4a. However, this circuit is troublesome for high-efficiency (reduced conduction angle) operation. In this mode, the sine-wave amplitude must increase for maximum output current. This results in a negative voltage swing as shown in Figure 10.1.4b. Although this may not be an issue for GaAs MESFET, it is a major problem for CMOS. First, the negative voltage can potentially forward bias the drain junction diode. More importantly, since the output voltage peaks at the most negative input, this circuit will increase the peak voltage across the gate oxide of M1, making the already severe oxide breakdown problem worse. The CMOS inverter driver shown in Figure 10.1.4c solves this problem. The gate voltage swings between V_{dd} and 0, avoiding the negative voltage. In fact, a square-wave driver provides higher efficiency than a sine-wave driver [5]. The main concern is the power required to drive the output transistor. This power is proportional to CV^2 and drops quickly as technology advances. In this 0.2µm design, the driver accounts for <5% drop of the power added efficiency and this number will improve with future technology.

The complete PA schematic is shown in Figure 10.1.5. To form the class F load, a separate pinout at the output node is used to connect to a quarter-wave transmission line. An L-matching network is used for impedance transformation. In 0.2µm CMOS, the die is $1.0x2.0mm^2$. The chip micrograph is shown in Figure 10.1.6. To test the PA, the die is assembled in a 20-pin TSSOP package with exposed die paddle. Down-bonds reduce ground inductance. An external balun combines the differential path power to the test equipment. An interesting application for cascode configuration is power control by adjusting the cascode bias. The output power and efficiency at 900MHz versus cascode bias are shown in Figure 10.1.7. Peak output power is 1.5W with 43% PAE. Table 10.1.1 compares the result with recently-published CMOS PAs. Using a mixture of thin and thick gate oxide transistors, higher output power is achieved with deep sub-micron CMOS technology despite the low oxide-breakdown voltage.

References:

[1] D. Su, et al., "A 2.5-V 1-W Monolithic CMOS RF Power Amplifier," Proc. CICC, pp. 189-192, May, 1997.
[2] K.-C. Tsai, et al., "A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications," IEEE JSSC, pp. 962-970, Jul., 1999.
[3] C. Yoo, et al., "A Common-Gate Switched, 0.9W Class-E Power Amplifier with 41% PAE in 0.25µm CMOS," VLSI Circuits Symp. Dig. Tech. Papers, pp. 56-67, Jun., 2000.
[4] Y. Tsividis, et al., "Simple Reconciliation MOSFET Model Valid in All Regions," in *Electronics Lett.*, vol. 31, pp. 506-507, Mar., 1995.
[5] S. Toyoda, "High Efficiency Single and Push-Pull Power Amplifiers," in *IEEE MTT-S Dig.*, pp. 277-280, Jun., 1993.

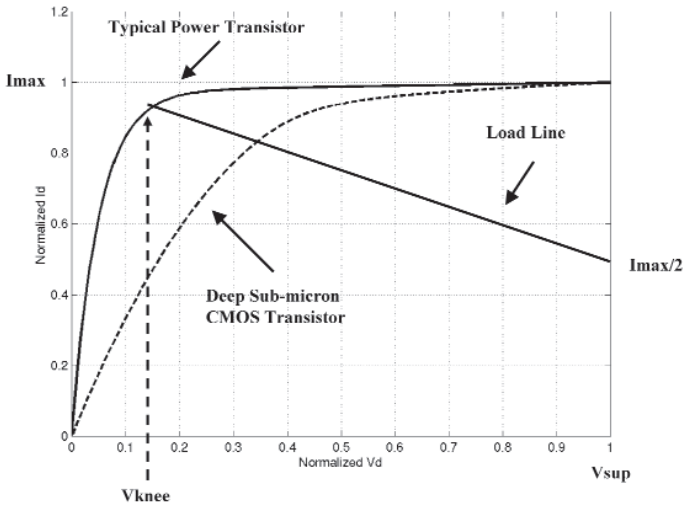

Figure 10.1.1: I-V curve and load line method.

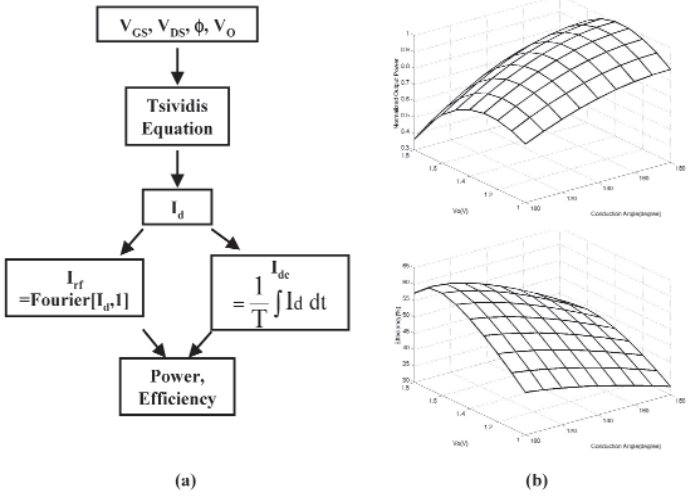

Figure 10.1.2: (a) Matlab procedure for power and efficiency calculation. (b) Power and efficiency plot for a 0.2μm transistor.

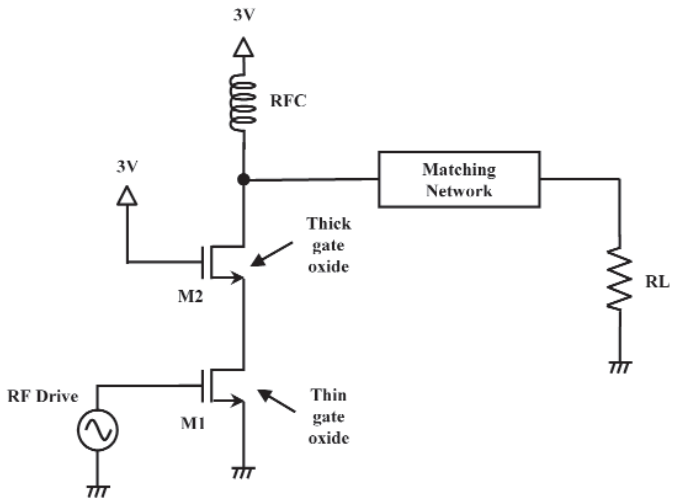

Figure 10.1.3: Output stage with thick gate oxide cascode transistor.

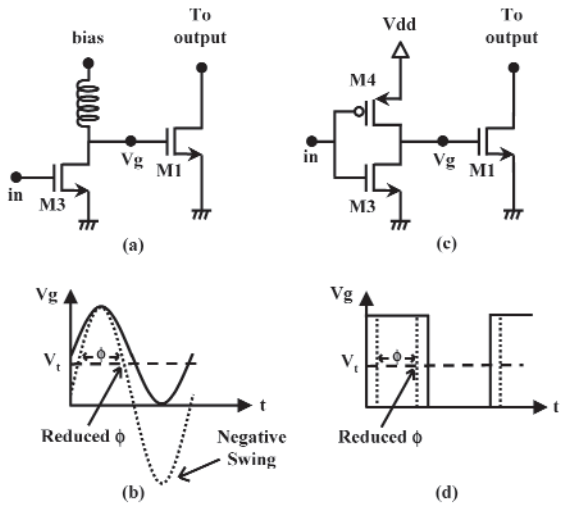

Figure 10.1.4: (a) Tuned load PA driver; (b) Reduced ϕ Vg waveform; (c) CMOS inverter driver; (d) Vg waveform

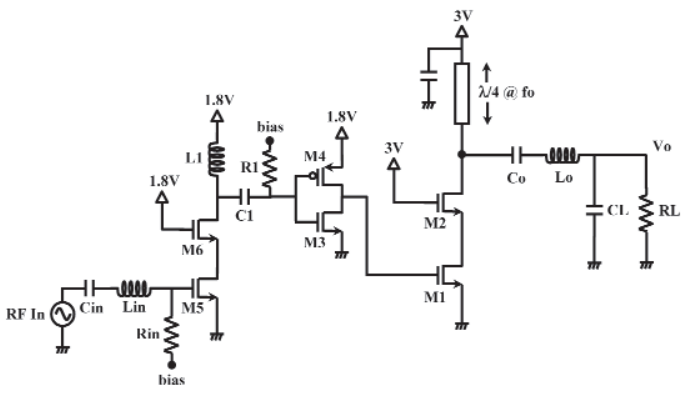

Figure 10.1.5: Complete PA schematic.

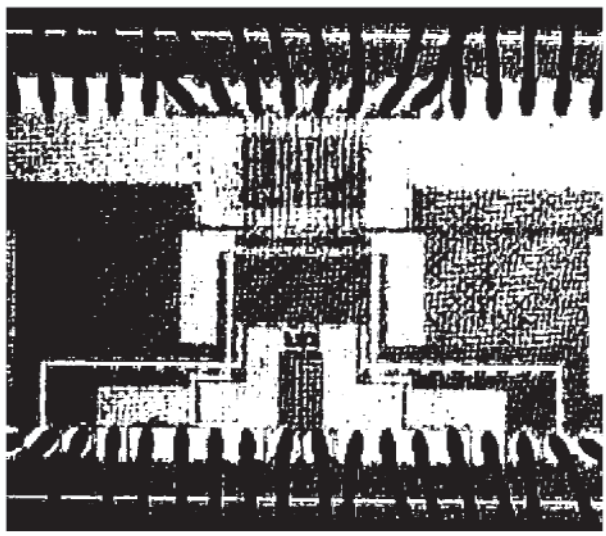

Figure 10.1.6: Chip micrograph.

Ref.	Technology	Frequency	V_{DD}(V)	Pout (W)	PAE(%)	Class
[1]	0.8 μm	850 MHz	2.5	1	42	D
[2]	0.35 μm	1900 MHz	2.0	1	48	E
[3]	0.25 μm	900 MHz	1.8	0.9	41	E
This Work	0.2 μm	900 MHz	1.8/3.0	1.5	43	F

Table 10.1.1: Performance comparison of recent published RF CMOS PAs.