26.3 A 1.3nJ/b IEEE 802.11ah Fully Digital Polar Transmitter for IoE Applications

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This paper presents an ultra-low-power (ULP) IEEE 802.11ah fully-digital polar transmitter (TX). IEEE 802.11ah is a new Wi-Fi protocol optimized for Internet-of-Everything (IoE) applications. Compared to other IoE standards like Bluetooth or ZigBee, its sub-GHz carrier frequency and mandatory modes with 1MHz/2MHz channel bandwidths allow devices to operate in a longer range with scalable data-rates from 150kb/s to 2.1Mb/s. Moreover, the use of OFDM improves link robustness against fading, especially in urban environments, and achieves a higher spectral efficiency. The key design challenges of an IEEE 802.11ah TX for IoE applications are to meet the tight spectral mask and error-vector-magnitude (EVM) requirements as for conventional Wi-Fi standards (e.g., 802.11n/g), while achieving low power consumption required by IoE applications. The presented TX applies a fully-digital polar architecture with a 1V supply, and it achieves more than 10× power reduction compared to the state-of-the-art OFDM transceivers [1-4]. Without any complicated PA pre-distortion techniques as in [5], it passes all the PHY requirements of the mandatory modes in IEEE 802.11ah with 4.4% EVM, while consuming 7.1mW with 0dBm output power.

A fully digital polar architecture is adopted for its excellent energy efficiency. Conventional analog Cartesian TXs [1-2] need power-hungry mixers and quadrature LO generators. State-of-the-art digital Cartesian TXs [3] directly upconvert IQ data to the RF domain, at the expense of high power consumption due to extensive usages of high-speed logic. A fully digital polar architecture is capable of handling the Cartesian-to-polar bandwidth extension for 802.11ah 1MHz/2MHz narrow-band OFDM signals, while avoiding IQ imbalance and LO leakage as in Cartesian TXs. The proposed TX, as shown in Fig. 26.3.1, consists of a 2-point all-digital PLL (ADPLL)-based frequency modulator [6] and a 6b $\Delta\Sigma$ switched-capacitor digitally-controlled PA (SC-DPA) [5]. Instead of using a 0.9GHz oscillator, a 1.8GHz LC digitally-controlled oscillator (DCO) together with a 1/2 divider occupies a smaller area and offers lower phase noise under the same power budget, as the Q-factor of a spiral inductor at 1.8GHz is approximately 40% higher. A 32MHz crystal oscillator (XO) is chosen as the system reference clock, since it can easily generate oversampling data clocks by a simple frequency division. The IQ data is first up-sampled to 32MHz and then fed to a low-complexity Cartesian-to-polar conversion module which has a resolution less than 1 degree. The PM data is differentiated, properly unwrapped to limit the frequency deviation range and then split into a highpass (HP) path and a lowpass (LP) path, which directly modulates the DCO and the ADPLL respectively. The accumulated phase error due to LSB truncation in the PM path is minimized by a $\Delta\Sigma$ quantization-error feedback to ensure a long-term phase coherency as illustrated in Fig. 26.3.1. In order to suppress the clock images of the AM data to meet the spectral mask, it is further fractionally up-sampled to $F_{rf}/4$ (i.e., ~225MHz). The $F_{rf}/4$ clock is reused from the counter in the ADPLL. In comparison to digital Cartesian TXs which require to up-sample both I and Q data [3], the proposed TX keeps the PM sampling rate at 32MHz as the ADPLL provides extra filtering for the far-out noise and clock images, and only up-samples the AM data that has higher impact on the spectral purity, thus achieving a better energy efficiency.

TX spectral purity and EVM highly rely on the quantization noise level, delay mismatch and the linearity of the AM modulation path shown in Fig. 26.3.2. After being fractionally up-sampled to $F_{rf}/4$, the AM data is filtered and fed to a $\Delta\Sigma$ modulator to improve the close-in spectral purity and reduce the required number-of-bits of the SC-DPA. Furthermore, the EVM is sensitive to the AM/PM delay mismatch as illustrated in the simulation result plotted in Fig. 26.3.2. For 1MHz/2MHz narrowband signals, the delay can be well-controlled in the digital domain, and is insensitive to PVT variations. A fine delay adjustment with a resolution of $4/F_{rf}$ is implemented to improve the accuracy. Since the transition of the AM data and the PM signal (the modulated RF signal from the divider) are not aligned, the AM data is retimed by the falling edge of the PM signal, as illustrated in Fig. 26.3.2, to ensure the AM switching glitch is removed, thus leading to a better far-out spectral purity. The D flip-flops of the AM-retiming module are implemented in True-Single-Phase-Clocked (TSPC) logic for lower power consumption. The SC-DPA matrix has 63 unit cells, each consisting of a NAND to apply the AM data to the PM signal and a driver stage to switch a 45fF metal capacitor. Since the AM linearity is guaranteed by the excellent capacitor matching in modern CMOS technologies, the measurement result in Fig. 26.3.3 shows this 6b SC-DPA achieves a 0.5LSB integral nonlinearity (INL) without any pre-distortion or calibration [5]. The unit cells are grouped into two segments to reduce the routing complexity and the power consumption of the buffers. The 3 MSBs are converted to 7b thermometer codes, each code controlling 8 unit cells. The 3 LSBs control another 7 unit cells in binary fashion. This differential SC-DPA with off-chip matching achieves a measured 8dBm peak output power with a 45% power-added efficiency (PAE), as shown in Fig. 26.3.3.

The digital-to-time-converter (DTC)-based ADPLL frequency modulator as adopted in [6] is further optimized for the 802.11ah OFDM signals. To achieve a wide modulation range with a fine frequency resolution, the HP/LP PM paths (Fig. 26.3.1) control two separate capacitor banks inside the DCO. The 7b HP bank achieves +/-8MHz range, while the LP bank provides a fine resolution of 30kHz to achieve low phase noise. The measured phase noise (Fig. 26.3.3) at 1.5MHz offset is -115dBc/Hz, which is 15dB lower than the 802.11ah spectral mask requirement. The DTC is realized as an inverter string loaded with switchable capacitors to achieve a good linearity, and this leads to a low fractional spur level of -55Bc, which is 15dB lower than the spectral mask requirement.

This digital polar TX passes the IEEE 802.11ah PHY requirements of the 1MHz/2MHz modes, including mandatory BPSK/QPSK and optional 16-QAM/64-QAM schemes (up to the MCS5 mode defined in 802.11ah). Figure 26.3.4 shows the spectral mask measurement with 1MHz/2MHz 64-QAM OFDM data packets. Both the far-out and close-in spectrum pass the mask with at least 4.8dB margin. With the AM-retiming module, the clock images are further suppressed by 10dB. Figure 26.3.5 shows the measured 64-QAM constellation and the EVM versus output power. The power breakdown shows that the total power consumption of the TX except SC-DPA is only 3.3mW. Together with a highly efficient SC-DPA optimized for ULP IoE applications, the presented TX achieves an excellent system efficiency of 14% when it is at 8dB back-off from the peak power.

Figure 26.3.6 summarizes the performance of this IEEE 802.11ah TX and compares with the state-of-the-art OFDM TXs. The presented fully digital low-voltage polar architecture offers more than 10× power reduction compared to the state-of-the-art sub-GHz OFDM transceiver [1], and 2× system efficiency improvement compared to recent literature [2-4]. Under the 64-QAM mode with 5.78Mb/s throughput, this TX achieves an energy efficiency of 1.3nJ/b, which is about 2× better than state-of-the-art Bluetooth/ZigBee TXs [6]. Together with digital filtering and AM retiming, it fulfills the spectral mask and EVM requirements with sufficient margin. Benefitting from the fully digital implementation, this TX scales with CMOS nodes for lower power consumption and smaller area, and is easy to be programmed for different application scenarios. It provides a competitive solution for emerging IoE applications. Fabricated in a 40nm CMOS process, this TX occupies a core area of 0.72mm^2 as shown in Fig. 26.3.7.

Acknowledgement:
The authors would like to thank Pepijn Boer and Mazin Al Noor for supporting the system evaluation.

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 978-1-4673-9467-3/16/$31.00

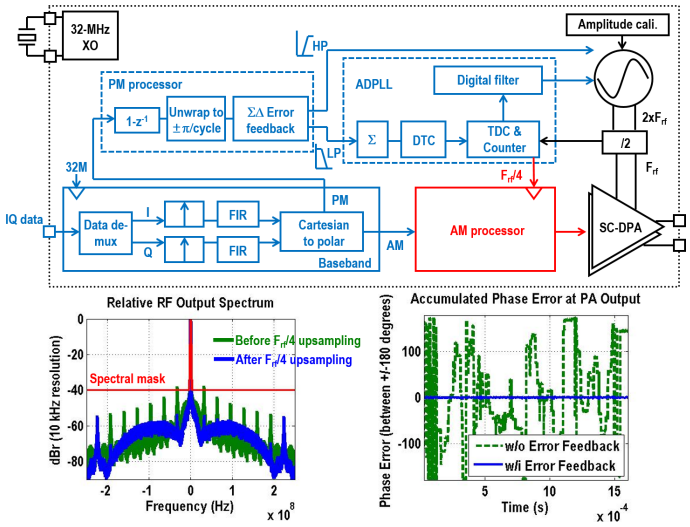

Figure 26.3.1: The simplified block diagram of the IEEE 802.11ah fully digital polar TX.

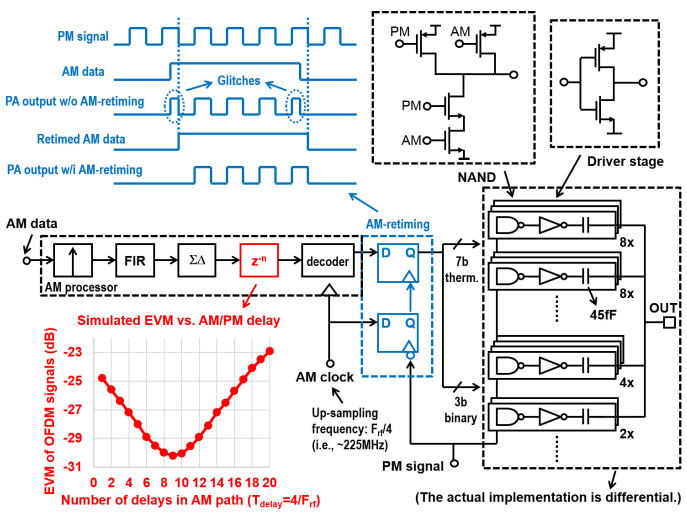

Figure 26.3.2: The simplified block diagram of the AM path, including AM processor and SC-DPA.

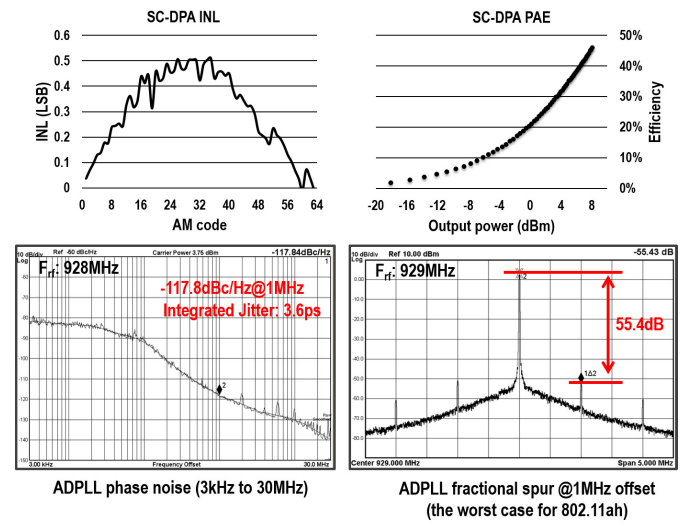

Figure 26.3.3: Top: measured SC-DPA linearity and efficiency; bottom: ADPLL phase noise and fractional spur level.

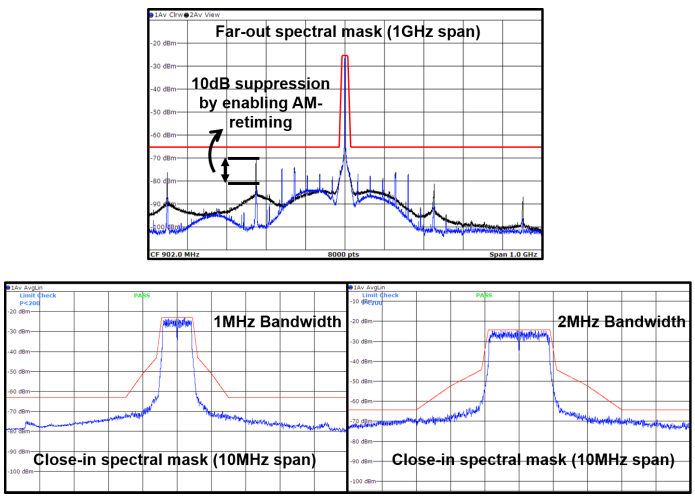

Figure 26.3.4: The spectral mask measurement with 1MHz/2MHz 64-QAM data packets.

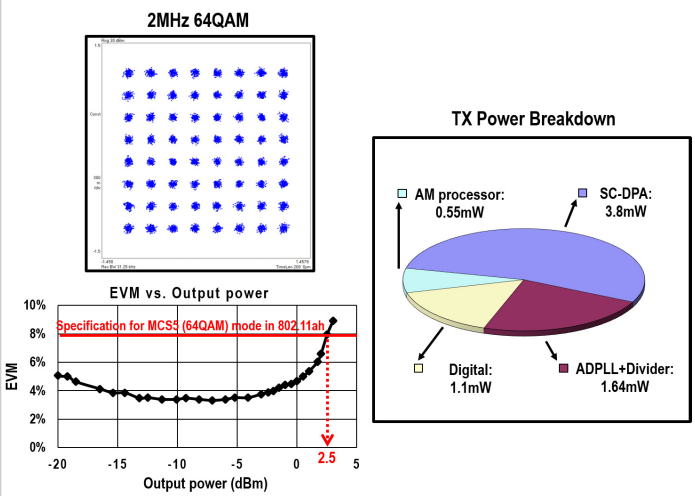

Figure 26.3.5: TX modulation accuracy and power-consumption breakdown.

	This work	[1] Semtech	[2] RFIC15	[3] ISSCC08	[4] JSSC15
Technology	**40nm**	-	180nm	65nm	65nm
VDD	**1V**	3.3V	1.7V	1.2V	1.2/2.1V
Architecture	**Digital Polar**	Analog IQ	Analog IQ	Digital IQ	Digital Polar
Modulation	**OFDM (11ah)**	OFDM (15.4g)	OFDM (LTE/11ah)	OFDM (11g)	OFDM (11g)
Frequency	**750-930MHz**	862-960MHz	750-930MHz	2.4GHz	1.7-2.6GHz
Bandwidth	**1/2MHz**	1MHz	1/2/8MHz	20MHz	20MHz
Average Pout	**0dBm**	-5dBm	8.9dBm[1]	2.6dBm	0/13.8dBm
Power Consumption	**7.1mW**	191.4mW	106.8mW	254mW	78/417mW
EVM	**4.4%**	-	3%	2.4%	4%
System Efficiency	**14%**	0.2%	7.3%	0.7%	1.3/5.8%
Peak Pout	**8dBm**	8dBm	13.6dBm	-	24dBm
Peak PAE	**45%**	-	25.5%	-	35%
Pre-Distortion Requirement	**No**	Support	Yes	Yes	Built-in linearization

[1] Measured with LTE 16QAM signal (5dB PAR).

Figure 26.3.6: Performance summary and comparison with prior art.

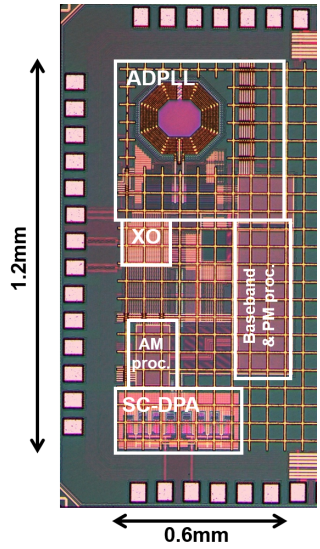

Figure 26.3.7: Die micrograph.

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