Fully Monolithic BiCMOS Reconfigurable Power Amplifier for Multi-Mode and Multi-Band Applications

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***Abstract*—A power amplifier (PA) supporting wideband code division multiple access, long-term evolution (LTE), and wireless local area network applications has been implemented in 0.18-μm SiGe BiCMOS technology. The PA integrates a tunable input matching network, a broadband output matching network, and adaptive bias circuits in a single chip to achieve high linearity and high power in different modulation schemes and operating bands. The three-stage PA adopts a differential-type configuration without using through-silicon-via technology to deliver 41.3–42 dB of gain and 28.2–28.6 dBm of 1-dB compression output power with a 20.8–27.6% power-added efficiency (PAE) at 1.85–2.5 GHz. To further validate the usefulness of the proposed PA, the envelope-tracking PA is designed to improve the PAE by 6.5% within the linearity specification of a 24.7-dBm average output power and a −33-dBc adjacent channel leakage ratio for 2.35-GHz 16 quadrature-amplitude-modulation time-division LTE signal with 20-MHz bandwidth.**

***Index Terms*—Adaptive bias circuit (ABC), broadband matching network, envelope-tracking (ET) circuit, long-term evolution (LTE), multi-band, multi-mode, power amplifier (PA), tunable matching network, wideband code division multiple access (WCDMA), wireless local area network (WLAN).**

I. Introduction

With the growing demand of complex mobile devices that can function in multi-standard wireless communication systems for various user roaming needs, multi-mode and multi-band power amplifiers (MMPAs) have become a critical component for future handset development because of their frequency flexibility, easy implementation, and small size. The MMPA adaptability enables the performance and cost constraint challenges on the reconfigurable RF front-end by reducing the number of the dedicated single-band power amplifiers (PAs) for each additional frequency band [1]–[5].

Distributed and balanced amplifiers are the most common techniques used for broadband applications [6]–[11]. However, the distributed amplifier topology requires a large number of transistors to obtain the constant gain, which increases cost and reduces efficiency. A balanced amplifier with a quarter-wavelength coupler has a relatively large chip size and is not practical at low gigahertz-range integrated circuits (ICs) for handset wireless communication.

Another approach is implementing tunable or multisection matching networks at the output port of an MMPA [12]–[18]. Although a matching network with multiple elements broadens operating bandwidth, its loss increases accordingly. For the tunable PA, the programmable output matching network with varactors or microelectromechanical systems (MEMS) switches are employed to achieve flexible load impedance [19]–[21]. The efficiency and linearity of the tunable PA are degraded by the low Q, restricted tuning range, and limited power-handling capability of the matching networks at the PA output port [22]–[24]. Moreover, many tunable matching networks have been implemented by off-chip devices with different processes and the sophisticated multi-chip-module packaging is required [2], [18], [25]. However, no study has yet proposed the fully integrated tunable input matching network of MMPA design.

The novel SiGe BiCMOS three-stage differential-type PA proposed in this study combines a power-combining transformer, a tunable input balun, and adaptive bias circuits (ABCs) in an on-chip configuration. Switched capacitors are adopted to reconfigure the input balun to match widely varying standards, including wideband code division multiple access (WCDMA), time-division long-term evolution (TD-LTE), and wireless local area networks (WLANs). The switched capacitor is operated in the low-input power region. Therefore, loss and nonlinearity effects can be avoided due to low RF voltage swing compared to the tuning elements at the PA output port. Furthermore, an envelope-tracking (ET) circuit is realized as a voltage supply modulator to enhance the power-added efficiency (PAE) of the MMPA, which is the first-reported envelope-tracking power amplifier (ETPA) using an ET circuit to dynamically change the collector voltage of the standalone MMPA for TD-LTE application.

In Section II, the source– and load–pull power contours and PAE contours of the PA input and output stages are analyzed. The need for a tunable input matching network that provides constant gain and 1-dB compression power over a wide operating band is demonstrated. Switched capacitors are optimized

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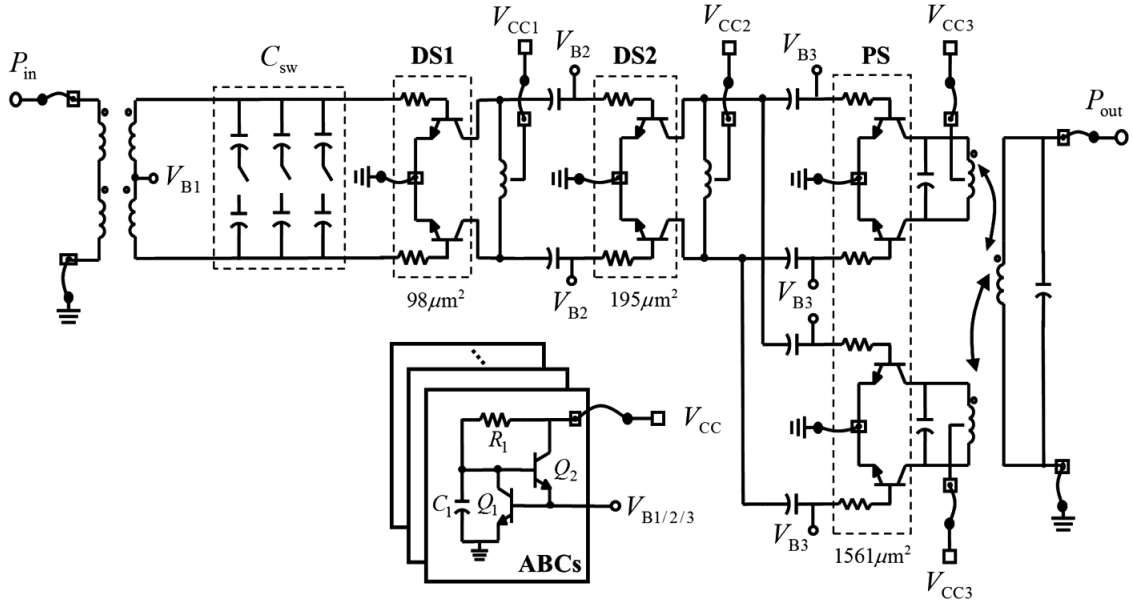

Fig. 1. Schematic of proposed fully monolithic three-stage reconfigurable MMPA.

in terms of input impedance and balun efficiency. The proposed MMPA is realized and measured in Section III. Measurements of gain flatness, adjacent channel leakage ratio (ACLR), error vector magnitude (EVM), and PAE verify the proposed MMPA and ETPA when operated at different frequencies and modulation schemes, i.e., 1.92–1.98-GHz quadrature phase-shift keying (QPSK) WCDMA with 3.84-MHz bandwidth, a 2.3–2.4-GHz 16 quadrature amplitude modulation (16QAM) TD-LTE with 20-MHz bandwidth, and a 2.4–2.5-GHz 64QAM 802.11g WLAN with 20-MHz bandwidth. Finally, conclusions are presented in Section IV.

II. Design

Fig. 1 is the schematic diagram of the proposed three-stage reconfigurable MMPA. The MMPA consists of an input balun with three switched capacitors $(C_{\rm sw})$, two series driver stages (DS1 and DS2), two shunt power stages (PS), and a two-primary parallel combining transformer (PCT) with a 1:1.7 turn ratio. The transistor sizes determined by the emitter area, i.e., emitter length $\times$ emitter width $\times$ emitter stripes, for DS1, DS2, and PS are approximately 98 μm^2 (10.16 μm $\times$ 0.6 μm $\times$ 16), 195 μm^2 (10.16 μm$\times$0.6 μm$\times$32), and 1561 μm^2 (10.16 μm$\times$ 0.6 μm $\times$ 256), respectively. The base and collector voltages of three stages are 0.83 and 3.5 V to bias this MMPA in class AB for good linearity and efficiency. The corresponding gains and loading impedances of DS1, DS2, and PS are (16 dB, $11-j55\ \Omega$), (15 dB, $5-j21\ \Omega$), and (13 dB, $12+j9\ \Omega$), respectively. The PCT is realized using a stack of two metal layers connected through vias, and the windings of PCT are 35-μm wide, 5-μm thick, and the gap between them is 8 μm. The quality factor of the primary/secondary stray inductor and coupling coefficient are 5.8/4.1 and 0.72, respectively. Compared to the other PAs using a PCT at the gigahertz band and 0.18-μm CMOS process [26], [27], our proposed structure presents the wider operating bandwidth of 30%.

The switched capacitor is implemented by an NMOS transistor switch and two metal–insulator–metal (MIM) capacitors in a series connection. The gate width of each switch is 2048 μm, and its corresponding $R_{\rm on}$ is 2.5 Ω and $C_{\rm off}$ is 1.45 pF. ABCs consisting of two transistors (Q_1 and Q_2) and passive components (R_1 and C_1) are employed in the bases of DS1, DS2, and PS to function as linearizers [28]. The differential configuration of individual driver and power stages produces a virtual ground, which avoids the emitter degeneration effect of grounding bond wires. Additionally, the differential topology reduces self-mixing of even-mode harmonics with the fundamental signal, which minimizes the third-order intermodulation distortion (IMD3).

Fig. 2(a) and (b) depicts the simulated load–pull power contours and PAE contours at the PS output port in Fig. 1 for the achievable output power and PAE at 1.95, 2.35, and 2.45 GHz. Results show that the power and PAE are consistent across a broad bandwidth. However, Fig. 3(a) shows that the source–pull analysis of the PA input port in Fig. 1 varies remarkably at different frequencies because of the frequency-dependent characteristic of the input impedance in DS1. Fig. 3(b) shows that the tuning $C_{\rm sw}$ at the input balun achieves frequency-independent power contours over operating bands. To demonstrate the usefulness of tunable $C_{\rm sw}$, the simulated power gain, output $P_{1\ \rm dB}$, and PAE with and without tuning $C_{\rm sw}$ are presented in Table I. Results show that the power gain variation is 4.7 dB for a fixed $C_{\rm sw}$ of 2.3 pF, but reduces to 1.8 dB when $C_{\rm sw}$ is tuning at different operating bands. Moreover, the loss due to the switch in the tunable $C_{\rm sw}$ is about 0.5–1.7 dB as compared to the power gain differences of the MMPA used with and without $C_{\rm sw}$ switches. Hence, the switch loss in $C_{\rm sw}$ is insignificant. Moreover, the advantage of the proposed tunable $C_{\rm sw}$ is further demonstrated by comparison with the single- and multi-stage matching networks at the input port of the MMPA. The circuit loss and 3-dB bandwidth of these circuit configurations are presented in Table II. Results validate that our proposed tunable $C_{\rm sw}$ with compact size possesses wider operating bandwidth and lower loss than those of the single-stage and multi-stage matching networks. To compensate the matching network loss,

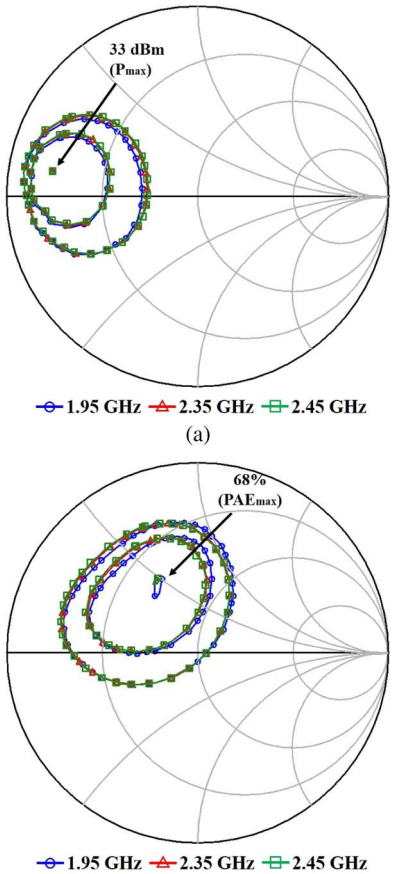

Fig. 2. Load–pull simulation of PS with 18-dBm input power at 1.95, 2.35, and 2.45 GHz. (a) Power contours. (b) PAE contours. (From the maximum power contour and PAE contour toward the outer contour with 1 dB and 10% decreasing per contour.)

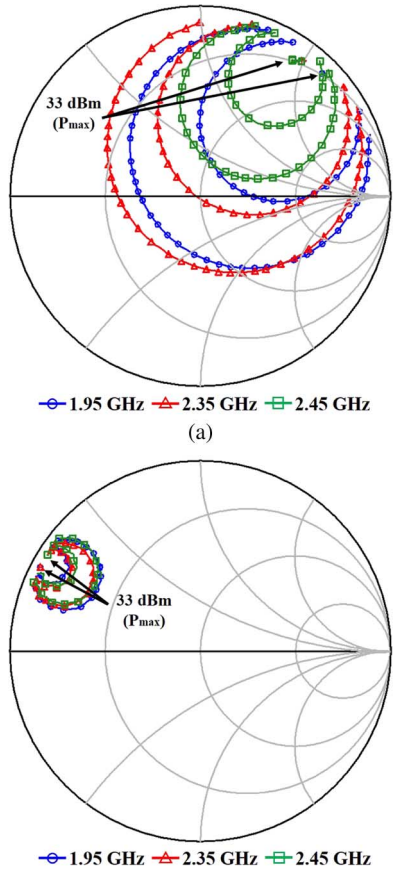

Fig. 3. Source–pull power contours of MMPA with −12-dBm input power at 1.95, 2.35, and 2.45 GHz. (a) Without tuning $C_{\rm sw}$. (b) With tuning $C_{\rm sw}$ from 1.75 to 3.3 pF. (From the maximum power contour toward the outer contour with 3 dB decreasing per contour.)

the three-stage configuration is chosen for PA architecture. The measured results shown in Table III demonstrate that the gain and linear power of the proposed PA are larger than those of two-stage PAs [29], [30].

The detailed equivalent circuit of the tunable input matching network in the single-ended configuration is illustrated in Fig. 4 for further investigation. Here, $Y_{\rm DS1} = G_{\rm DS1} + jB_{\rm DS1}$ is the input admittance of DS1 and $Y_{\rm load} = G_{\rm load} + jB_{\rm load} = 1/R_{\rm load} + j\omega C_{\rm load}$ is the load admittance of the balun output port. The single-ended switched capacitor ($C_{\rm sg}$) equals two times $C_{\rm sw}$ shown in Fig. 1. The mutual inductor M is located between the primary and secondary windings of the balun, and R_1 and R_2 are their respective resistances due to metal loss in these two windings. Assuming $R_1 \ll j\omega L_1$ and $R_2 \ll j\omega L_2$, the power in the balun output port is

$$P_{\rm out} = \frac{|V_2|^2}{2R_{\rm load}} = \frac{(\omega M|I_1|)^2}{2R_{\rm load}\left[(1-\omega^2 L_2 C_{\rm load})^2 + (\omega L_2 G_{\rm load})^2\right]}. \quad (1)$$

To maximize $P_{\rm out}$ with output capacitance $C_{\rm load}$

$$\frac{dP_{\rm out}}{dC_{\rm load}} = \frac{2\omega L_2 \times (1-\omega^2 L_2 C_{\rm load})^2 (\omega M|I_1|)^2}{\left[(1-\omega^2 L_2 C_{\rm load})^2 + (\omega L_2 G_{\rm load})^2\right]} = 0 \quad (2)$$

TABLE I
PERFORMANCE OF SIMULATED STANDALONE MMPA WITH AND WITHOUT TUNING $C_{\rm sw}$

Frequency (GHz)	1.95	2.35	2.45	1.95	2.35	2.45
C_{sw}	2.3 pF			3.3 pF	2.3 pF	1.75 pF
Power Gain (dB)	37.8	42.5	41.4	41.5 43.2*	42.5 43.3*	43.3 43.8*
$Pout_{1dB}$ (dBm)	27.8	28.7	28.7	28.2 28.2*	28.7 28.8*	28.7 28.9*
PAE_{1dB} (%)	27	27.4	26.8	28.3 28.4*	27.4 27.7*	26.8 27.4*

* Tuning without switch.

TABLE II
COMPARISON AMONG DIFFERENT INPUT MATCHING NETWORKS

Configuration	Tunable C_{sw}	Single-stage	Multi-stage
3-dB bandwidth (MHz)	900	800	840
Loss ($1-|S_{11}|^2-|S_{21}|^2$)	0.051	0.036	0.101

Note: All inductors, capacitors, and switches in this case are post-simulated TSMC models.

TABLE III
PERFORMANCE COMPARISON AMONG DIFFERENT PA ARCHITECTURES

Ref.	Freq. (GHz)	Gain (dB)	P_{linear} (dBm)	Supply (V)	Stage	Input / Output Matching	Technology
[29]	2.4-2.5	28	19.5 @ EVM = 3 %	3.3	2	On- / On-chip	SiGe BiCMOS with TSV
[30]	2.4	13.8	20 @ EVM = 5 %	3.3	2	On- / Off-chip	0.18 μm SiGe BiCMOS
This work	**2.45**	**42**	**20.2 @ EVM = 3 %**	**3.5**	**3**	**On- / On-chip**	**TSMC 0.18 μm SiGe BiCMOS**

Note: Modulation in this case is 64QAM 802.11g WLAN signal with 20-MHz bandwidth.

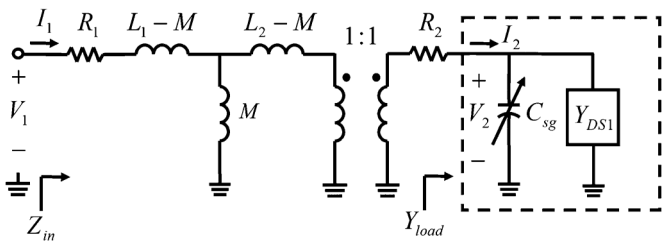

Fig. 4. Equivalent-circuit model of input matching network in single-ended configuration including input balun, switched capacitor ($C_{\rm sg}$), and input admittance of DS1 ($Y_{\rm DS1}$).

we obtain

$$C_{\rm load} = \frac{1}{\omega^2 L_2} = C_{\rm sg} + \frac{{\rm Im}(Y_{\rm DS1})}{j\omega} = C_{\rm sg} + \frac{B_{\rm DS1}}{\omega}. \quad (3)$$

The PA input impedance is (4), shown at the bottom of this page, where

$$C = R_2 + \frac{\frac{1}{R_{\rm load}}}{\left(\frac{1}{R_{\rm load}}\right)^2 + (\omega C_{\rm sg} + B_{\rm DS1})^2}$$
$$D = \frac{-(\omega C_{\rm sg} + B_{\rm DS1})}{\left(\frac{1}{R_{\rm load}}\right)^2 + (\omega C_{\rm sg} + B_{\rm DS1})^2}$$
$$E = C^2 - D^2 + \omega^2 L_2^2.$$

The power transfer efficiency of the balun under input impedance matching condition is

$$\eta = \frac{P_{\rm out}}{P_{\rm in}} = \frac{P_{\rm out}}{P_{\rm out} + P_{\rm loss}} = \frac{R_{\rm load}\left(\frac{M}{L_2}\right)^2}{R_1 + (R_{\rm load} + R_2)\left(\frac{M}{L_2}\right)^2 [1 + R_{\rm load}^2(\omega C_{\rm sg} + B_{\rm DS1})^2]}. \quad (5)$$

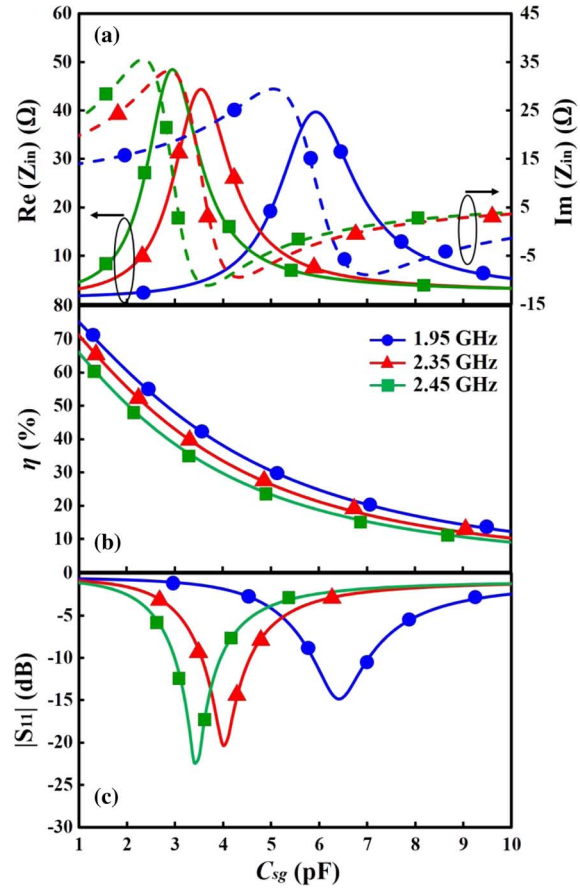

Fig. 5. (a) Calculated input impedance at the input matching network of MMPA versus $C_{\rm sg}$. (b) Calculated maximum power transfer efficiency of input matching network versus $C_{\rm sg}$. (c) Calculated $|S_{11}|$ of input matching network versus $C_{\rm sg}$.

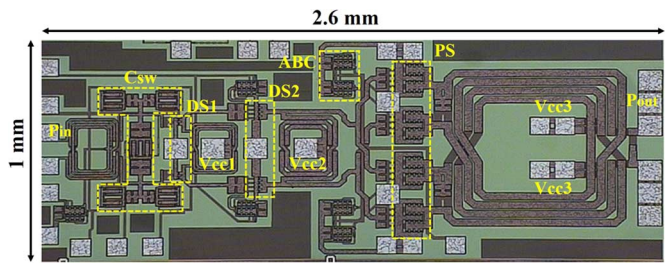

Fig. 6. Chip microphotograph of proposed standalone MMPA.

where $P_{\rm loss} = (R_1|I_1|^2 + R_2|I_2|^2)/2$ is the balun metal loss and $P_{\rm out}$ can be substituted from (1) when $C_{\rm load} = C_{\rm sg} + B_{\rm DS1}/\omega$.

The real and imaginary parts of $Z_{\rm in}$ calculated by (4) and η by (5) with various $C_{\rm sg}$ is depicted in Fig. 5(a) and (b), respec-

$$Z_{\rm in} = \left(R_1 + \frac{\omega^2 M^2 C\left[C^2 + (D - \omega L_2)^2\right]}{E^2 + 4C^2D^2}\right) + j\left[\omega(L_1 - M) + \frac{\omega^2 M^2 D\left(-D^2 - C + \omega^2 L_2^2\right) + \omega M(E^2 - EM\omega^2 L_2 + 4C^2D^2)}{E^2 + 4C^2D^2}\right] \quad (4)$$

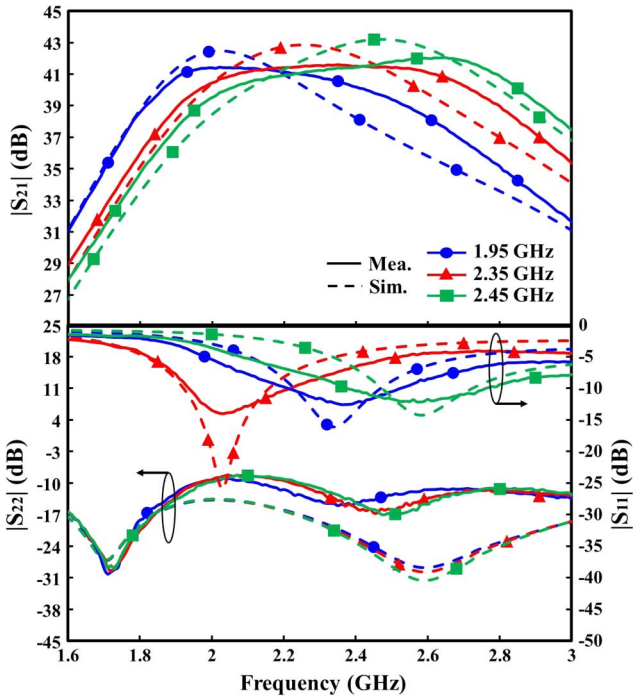

Fig. 7. Simulated and measured S-parameters of standalone MMPA in the three operating bands.

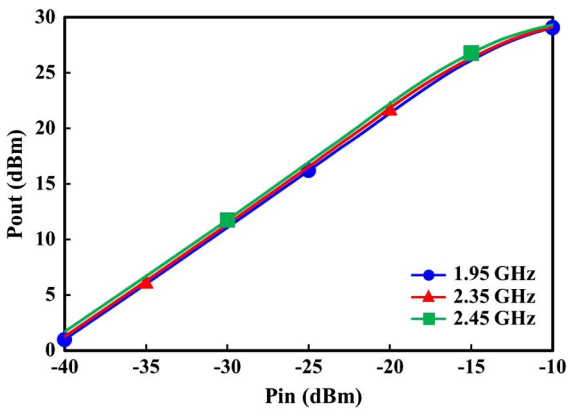

Fig. 8. Measured output power of standalone MMPA in the three operating bands versus input power.

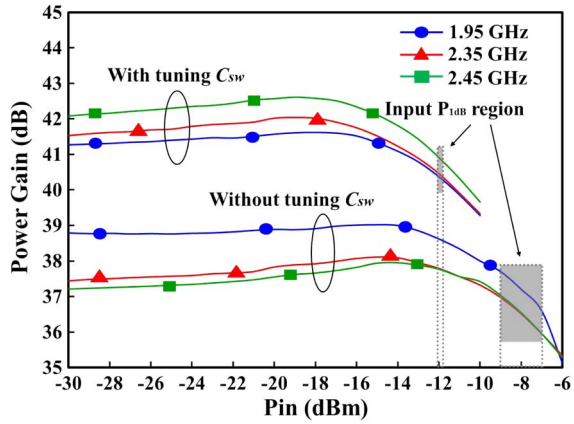

Fig. 9. Measured power gain of standalone MMPA with and without tuning $C_{\rm sw}$ in the three operating bands.

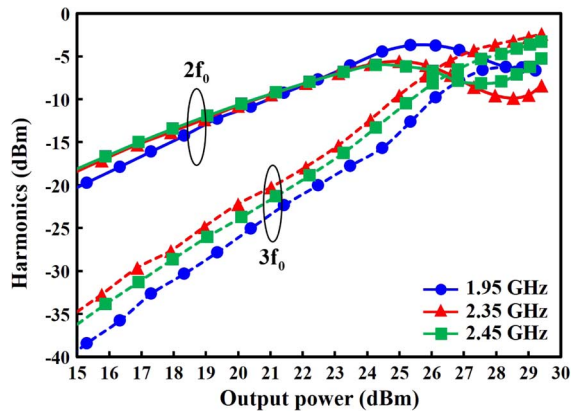

Fig. 10. Measured second- and third-harmonics of standalone MMPA in the three operating bands.

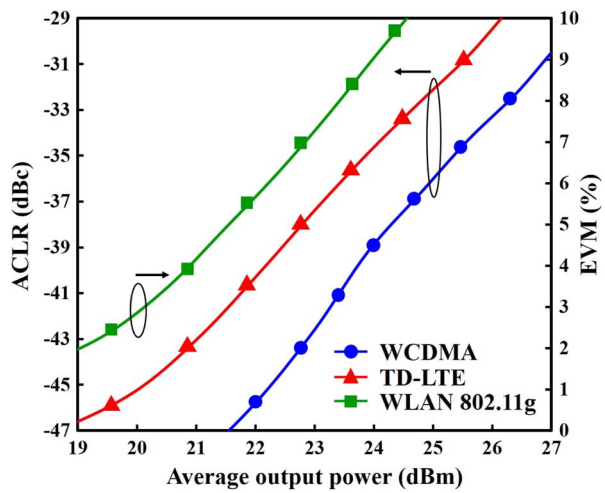

Fig. 11. Measured ACLR and EVM of standalone MMPA.

tively. Fig. 5(a) shows that the imaginary part of $Z_{\rm in}$ crosses zero from the positive value to negative value at different operating frequencies with the corresponding $C_{\rm sg}$. The effect of various $C_{\rm sg}$ on the power transfer efficiency η of the balun under input impedance matching condition is also presented in Fig. 5(b). The optimum $C_{\rm sg}$ at different frequencies can be determined by considering the minimum imaginary part of $Z_{\rm in}$ to obtain larger η and better input impedance matching. Since $C_{\rm load} = C_{\rm sg} + B_{\rm DS1}/\omega$ is used to resonate out the stray inductor L_2 in the secondary winding of balun, as shown in (3), the larger $C_{\rm sg}$ would results in the smaller V_2 shown in Fig. 4, and hence, the smaller η shown in Fig. 5(b). The return loss of the input matching network with different $C_{\rm sg}$ is shown in Fig. 5(c). Results show that the $C_{\rm sg}$ for $\mathrm{Im}(Z_{\rm in}) = 0$ are 6.3, 4, and 3.3 pF for 1.95, 2.35, and 2.45 GHz, respectively, which corresponds to the minimum $|S_{11}|$, as shown in Fig. 5(c). Thus, the optimum $C_{\rm sg}$ at different frequencies can be determined by considering

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON AMONG THE STATE-OF-THE-ART PAS AND ETPAS

Ref.	Modulation	Freq. (GHz)	Gain (dB)	$Pout_{1dB}$ (dBm)	PAE_{1dB} (%)	P_{linear} (dBm)	With Linearizer / ET	Supply (V)	Input / Output Matching	Technology	Die size (mm^2)
[14]	GSM	1.6-2.6	22.1	27.2 @ P_{max}	43 @ P_{max}	26	No / No	2.8	On- / On-chip	90 nm CMOS	4
[29]	WLAN 802.11g 64QAM 20MHz	2.4-2.5	28 ($\Delta G = 0.5$)	–	14.6 @ P_{linear}	19.5 @ EVM = 3 %	Yes / No	3.3	On- / On-chip	SiGe BiCMOS with TSV	–
[30]	WLAN 802.11g 64QAM 20MHz PAPR = 9 dB	2.4	13.8	23.8	23.8	20 @ EVM = 5 %	Yes / No (DPD)	3.3	On- / Off-chip	0.18 μm SiGe BiCMOS	–
[31]	LTE 16QAM 20MHz	2 (1.7-2.5)	23.8 ($\Delta G = 3$)	26.2	34	20 @ ACLR = -33 dBc	No / No	7.8	On- / On-chip	0.25 μm SiGe BiCMOS	1
[34]	LTE 16QAM 10MHz	1.95	28.5	29	26.6 @ P_{linear}	26 @ ACLR = -33 dBc ($\pm$10MHz offset)	Yes / No	3.4	Off- / Off-chip	0.35 μm SiGe BiCMOS with TSV	2.55
[35]	TD-LTE 16QAM 10MHz	2.3-2.4	33.7	30	18 @ 25 dBm	28.5**	Yes / No	3.3	On- / Off-chip	SiGe HBT	2.89
[36]	WCDMA 3.84MHz	1.9	–	29.6 @ P_{max}	33 @ P_{linear}	26**	Yes / Yes	3.3	On- / On-chip	0.18 μm CMOS	4
	LTE 5MHz	0.8	–	28 @ P_{max}	27 @ P_{linear}	23**					
		2.3	–	26.5 @ P_{max}	23 @ P_{linear}	22**					
[37]	LTE 16QAM 5MHz PAPR = 7 dB	0.8	22.8	24.4*	55*	23.5 @ EVM = 3.8 %	No / Yes	4.2	Off- / Off-chip	TSMC 0.35 μm SiGe BiCMOS	1.65
		1.75	19.5	25.3*	59.8*	24.2 @ EVM = 4.8 %					
		2.4	16.3	25*	55*	24.3 @ EVM = 5 %					
This work	**WCDMA QPSK 3.84MHz PAPR = 3.4 dB**	**1.95**	**41.3**	**28.2**	**27.6**	**25.6 @ ACLR = -33 dBc EVM = 2.9 %**	**Yes / No**	**3.5**	**On- / On-chip**	**TSMC 0.18 μm SiGe BiCMOS**	**2.6**
	WLAN 802.11g 64QAM 20MHz PAPR = 11.4 dB	**2.45**	**42**	**28.6**	**20.8**	**20.2 @ EVM = 3 %**					
	TD-LTE 16QAM 20MHz PAPR = 7.5 dB	**2.35**	**41.5**	**28.3**	**19 @ P_{linear}**	**24.6 @ ACLR = -33 dBc EVM = 5.1 %**					
			41.1	–	**25.5 @ P_{linear}**	**24.7 @ ACLR = -33 dBc EVM = 4.5 %**	**Yes / Yes**				**3.9**

Note: Above PAs are measured on printed circuit board (PCB) via bonding wires, except [31] is for on-wafer measurement and [14], [30] and [34] are for packaged configuration.
* Standalone PA is measured at a supplied voltage of 3.6 V and the loss of off-chip balun is de-embedded.
** Linear power meets the 3GPP requirement.

the minimum imaginary part of Z_{in} to achieve the impedance matching condition at the input port of balun.

III. IMPLEMENTATION AND MEASUREMENT

A. Standalone MMPA

The proposed reconfigurable MMPA was developed in TSMC 3P6M 0.18-μm SiGe BiCMOS technology. This process provides a 3.5-μm-thick AlCu UTM metal layer and 1.5-fF/μm^2 MIM capacitor on a 10-Ω-cm bulk Si substrate. Fig. 6 is a microphotograph of the proposed fully monolithic SiGe MMPA with on-chip input and output matching networks. The chip area of the standalone MMPA is 1 mm × 2.6 mm. Fig. 7 shows the measured and simulated small-signal gain responses of the proposed standalone MMPA in the three operating bands, i.e., 1.92–1.98 GHz for WCDMA Band 1, 2.3–2.4 GHz for TD-LTE Band 40, and 2.4–2.5 GHz for the 802.11g WLAN. The measured and simulated results agree well with each other within the operating bands, except that the gain value is slightly lower in measurement due to the lower quality factor of circuit implementation. As C_{sw} varies from 3.3 to 1.75 pF, the center frequency of the MMPA is tuned from 1.95 to 2.45 GHz, which approximates the calculated value shown in Fig. 5(a). Due to the low quality factor of the passive components in MMPA, the measured bandwidths are larger than the simulated data. The measured return loss at the MMPA input and output port are included in Fig. 7. Since the proposed MMPA uses the broadband output matching network PCT, as described in Section II, the output return loss is consistent and less than 10 dB at three operating frequencies of 1.95, 2.35, and 2.45 GHz.

The output power of the proposed MMPA is measured in Fig. 8, and the results show that the output power increased from 0 dBm to about 28.5 dBm when the input power sweeps from −40 to −12 dBm in three operation frequencies. The MMPA possesses efficient operation over a large input power range and a wide frequency band to accommodate the multi-standard transmitters with various peak-to-average power ratio (PAPR) modulation signals at different frequency bands.

Fig. 9 shows the measured power gain of the standalone MMPA with different input power. Results indicate that the

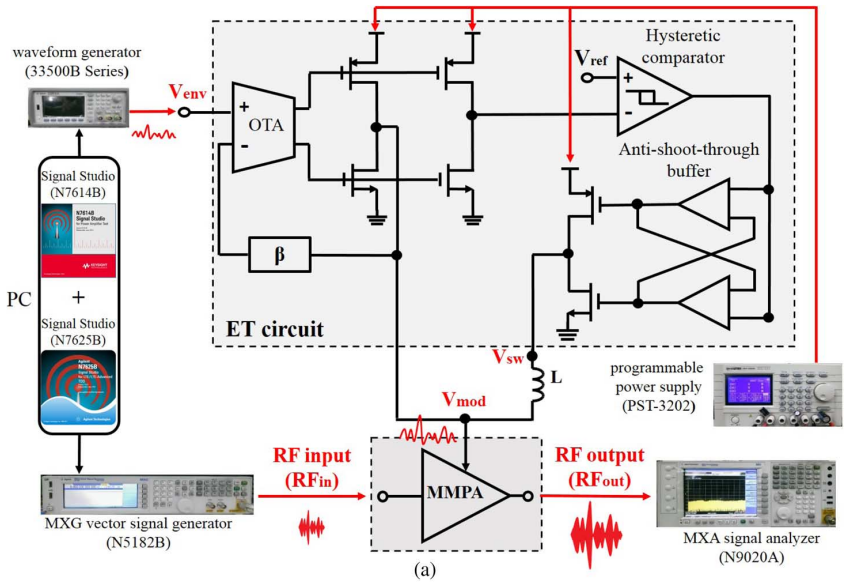

Fig. 12. (a) Circuit diagram of ET circuit and test bench setup for ETPA. (b) Measurement setup of test bench for ETPA.

power gain changes from 37.2 to 38.8 dB and input $P_{1\ \mathrm{dB}}$ varies from -7 to -9 dBm in the three operating bands when the mismatch condition has occurred at the MMPA input port, as depicted in the gray area of Fig. 9. In contrast, when the proposed MMPA is operated at the matching condition by tuning C_{sw} to minimize the MMPA input reflected power, the gain variation is lower than 0.7 dB from 1.95 to 2.45 GHz and the input $P_{1\ \mathrm{dB}}$ remains almost the same. This is essential for a multi-mode and multi-band transmitter design in which the output power fed to the external PA is constant [32], [33].

In Fig. 10, the measured second and third harmonics of the MMPA at 1.95, 2.35, and 2.45 GHz are smaller than -32 dBc for 28-dBm output power due to the low-pass characteristic of the PCT matching network. Fig. 11 shows the measured ACLR and EVM of the standalone MMPA. The standalone MMPA delivers an average output power of 25.6 dBm with an ACLR better than -33 dBc at 1.95 GHz $\pm$ 5-MHz offsets for QPSK WCDMA with 3.84-MHz bandwidth, and generates 24.6 dBm with a -33-dBc ACLR at 2.35 GHz $\pm$ 20-MHz offset for 16QAM TD-LTE with 20-MHz bandwidth. The measured EVM of less than 3% up to 20.2 dBm is obtained in the case of a 2.45-GHz 64QAM 802.11g WLAN with 20-MHz bandwidth. Table IV summarizes and compares the performances of designed standalone MMPA with the state-of-the-art PAs for wireless communication applications.

B. ETPA

The PAE of the presented standalone MMPA is further enhanced by employing an ET circuit on the collectors of the MMPA. Fig. 12(a) illustrates the schematic diagram of the ET circuit. The circuit consists of a linear stage, hysteretic comparator, and switching stage to track the envelope of a modulated signal. In the linear stage, an OP-Amp provides an independent voltage source through the feedback network. In the switching stage, a large PMOS and an anti-shoot-through buffer

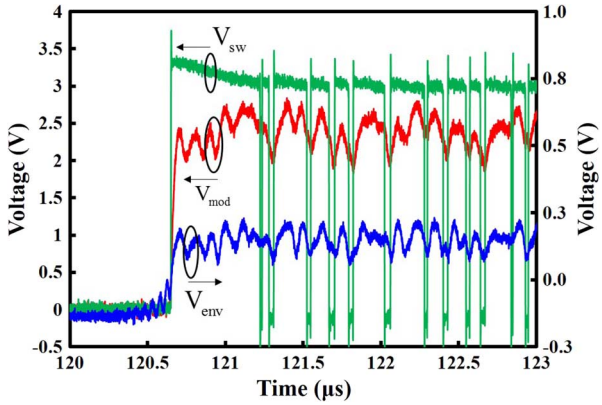

Fig. 13. Measured time-domain waveforms of V_{env}, V_{mod}, and V_{sw}.

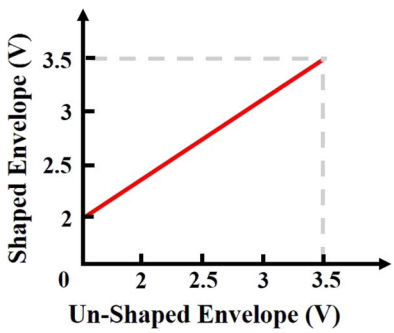

Fig. 14. Envelope shaping function of ET circuit.

operate as a dependent current source to provide most of the current to the PA bias. The hysteretic comparator, which has a current sensing circuit at the output of the linear stage, realizes the smooth current split between linear and switching stages. A detailed configuration of the ET circuit was described in [4], [38], and [39]. The test bench setup is also shown in Fig. 12(a) [40], [41]. Keysight N7625B Signal Studio and Keysight N7614B Signal Studio for PA test are used for generating an IQ waveform with the shaping table manager. The generated IQ and envelope waveform are downloaded to the Keysight N5182B MXG signal generator and 33500B arbitrary waveform generator and, respectively, are connected to the standalone MMPA and ET circuit. The power spectrum and ACLR of the ETPA consisting of the standalone MMPA and the ET circuit are measured using the Keysight MXA N9020A vector signal analyzer. The experimental setup of the ETPA is established in Fig. 12(b).

To characterize the performance of the proposed ET circuit, the MMPA is modeled as a 5-Ω resistive load. The measured time-domain input (V_{env}) and output (V_{mod}) envelope signals of the ET circuit in conjunction with the switching stage output waveform (V_{sw}) are shown in Fig. 13. The configuration is shown in Fig. 12. The alignment between the RF signal at the MMPA output port and V_{mod} is achieved by using the time-alignment tool embedded in the Keysight N7614B Signal Studio to manually control the time delay to minimize the misalignment. In TD-LTE operation, the uplink and downlink of the transceiver are distinguished by time instead of frequency. Hence, the ET circuit is turn-on and turn-off at some specific time frames to reduce the power consumption. In Fig. 13, the

TABLE V
PERFORMANCE COMPARISON AMONG PREVIOUS ET CIRCUITS

Ref.	Modulation	PAPR (dB)	Bandwidth (MHz)	Supply (V)	R_{load} (Ω)	Efficiency (%)
[43]	LTE	-	10	5 / 3.6*	4.7	76.8
[44]	LTE 16QAM	7.5	5	3.5	10	71
[45]	LTE 16QAM	6.44	10	5 / 3.4*	6.5	76.2
[46]	LTE	6.1	20	5	5.7	73
This work	**LTE 16QAM**	**7.5**	**20**	**3.5**	**5**	**76.8**

* Supply voltage of linear amplifier/supply voltage of switching amplifier.

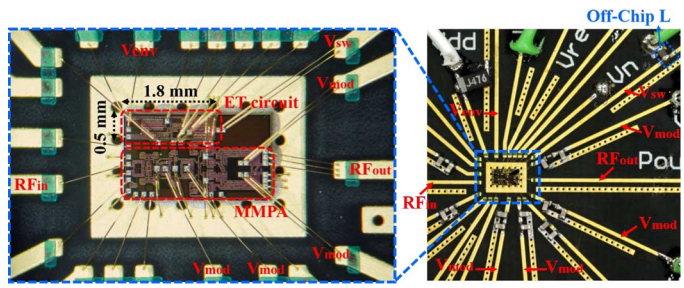

Fig. 15. PCB layout of designed ETPA. The indicated $\mathrm{RF_{in}}$, $\mathrm{RF_{out}}$, V_{env}, V_{sw}, V_{mod},and off-chip inductor Lcorrespond to the ETPA configuration in Fig. 12.

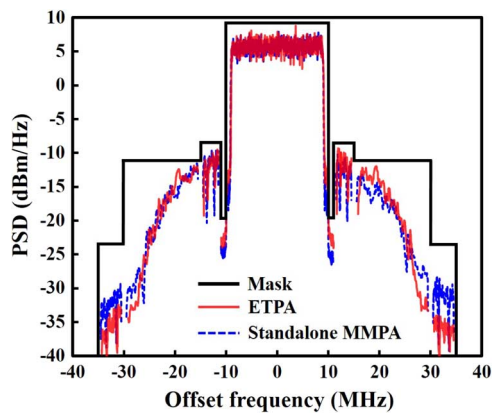

Fig. 16. Measured spectra of standalone MMPA and ETPA at average output power of 25.5 dBm for 2.35-GHz 16QAM TD-LTE with 20-MHz bandwidth.

ETPA is operated at TD-LTE subframe configuration 0 [42] and turned on at 120.6 μs. The rail-to-rail level of the switching voltage V_{sw} is approximately 3.3 V and the output voltage of the ET circuit V_{mod} is 11 times the input voltage V_{env}, and both V_{mod} and V_{env} waveforms are almost identical. The envelope shaping function shown in Fig. 14 and the off-chip inductor L in Fig. 12 are optimized to reduce the burden of the ET circuit and to achieve the high linearity and high efficiency of the ETPA. The performance and comparison among the other ET circuits are summarized in Table V.

Fig. 15 shows the implementation of the ETPA on an FR4 PCB with wire-bonding interconnection. The output envelope signal of the ET circuit is connected to the four pads V_{mod} of the ETPA die to provide the dynamic collector voltage of the standalone MMPA. By using PCB routing, these four pads are

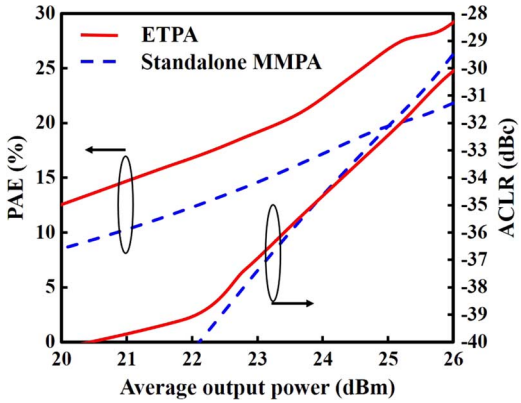

Fig. 17. Measured PAE and ACLR of standalone MMPA and ETPA for 2.35-GHz 16QAM TD-LTE signal with 20-MHz bandwidth.

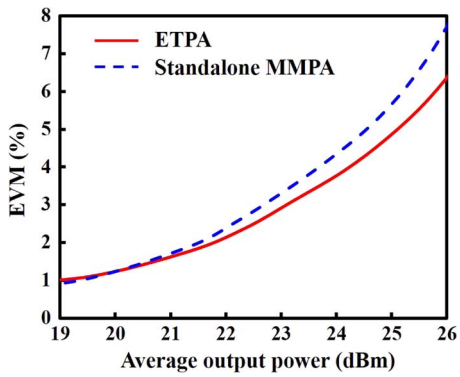

Fig. 18. Measured EVM of standalone MMPA and ETPA for 2.35-GHz 16QAM TD-LTE signal with 20-MHz bandwidth.

connected to the linear stage output and the switching stage output ($V_{\rm sw}$) with inductor L, as depicted in Fig. 15. The chip size of the ETPA is 1.5 mm $\times$ 2.6 mm and can be further reduced by removing some test pads. Fig. 16 depicts the measured spectra of the standalone MMPA and ETPA at the same output power of 25.5 dBm for 2.35-GHz 16QAM TD-LTE with 7.5-dB PAPR and 20-MHz bandwidth. Fig. 17 shows the measured PAE and ACLR of the standalone MMPA and ETPA for the TD-LTE signal. The ACLR is measured with a resolution bandwidth of 100 kHz at the center frequency of 2.35 GHz and 20-MHz offset. The standalone MMPA with a supply voltage of 3.5 V achieves a PAE of 19% and an ACLR of -33 dBc at an average output power of 24.6 dBm. Compared to the standalone MMPA, the ETPA with the same specifications of -33-dBc ACLR and 24.7-dBm average output power improves PAE by 6.5% when the PAE is calculated by multiplying the applied voltage and current of the ET circuit from the power supply. The measured EVM results of the standalone MMPA and ETPA for the 16QAM TD-LTE signal with center frequency of 2.35 GHz and 20-MHz bandwidth are also included in Fig. 18. The linear output powers of the standalone MMPA and ETPA are 22.6 and 23.1 dBm for EVM smaller than 3%, which is suitable for the EVM specification of the practical PA module to accommodate the distortion from the nonideal RF transceiver [47]. The EVM improvement of the ETPA is achieved by optimizing the envelope shaping function (Fig. 14) to reduce the AM–AM distortion [48]. The proposed ETPA performance is also included in Table IV.

IV. Conclusion

This paper has proposed a fully monolithic three-stage reconfigurable MMPA for WCDMA, TD-LTE, and WLAN applications in TSMC 0.18-μm SiGe BiCMOS technology. To obtain the high output power and high linearity in different modulation schemes and operating bands, a tunable input matching network, a broadband transformer-type output matching network, and adaptive bias networks are adopted in the MMPA design. Instead of using a conventional tunable matching network at the PA output, the input tunable matching network consisting of a balun and switched capacitors is investigated and realized to achieve frequency-independent characteristics of the MMPA over three operating bands. By optimizing the switched capacitors, the MMPA delivers the gain of 41.3–42 dB and 1-dB compression output power of 28.2–28.6 dBm with 20.8–27.6% PAE at 1.92–1.98 GHz for WCDMA Band 1, 2.3–2.4 GHz for TD-LTE Band 40, and 2.4–2.5 GHz for the 802.11g WLAN. The measured respective average output powers for WCDMA and TD-LTE signals are 25.6 and 24.6 dBm with -33-dBc ACLR. The measured output power of EVM of less than 3% is 20.2 dBm for the 64QAM 802.11g WLAN with 20-MHz bandwidth. To reduce the power consumption of the standalone MMPA, the ET circuit consisting of a linear stage, hysteretic comparator, and switching stage was applied to the standalone MMPA to realize the ETPA. Compared to the standalone MMPA, the ETPA improved the PAE by 6.5% under the average output power of 24.7 dBm and -33-dBc ACLR for the 16QAM 7.5-dB PAPR TD-LTE signal with 20 MHz bandwidth. The output power of the ETPA for EVM smaller than 3% is 23.1 dBm without employing digital predistortion. Based on these results, using the proposed MMPA in combination with the ET circuit enables the presented ETPA with high-linearity, high-power, and high-efficiency characteristics for multi-mode and multi-band wireless communication systems. Novel MMPA architectures with different output power levels and the corresponding ET circuits are currently under investigation.

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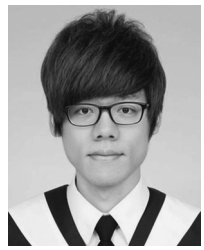

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