A 16.5–28 GHz 0.18-μm BiCMOS Power Amplifier With Flat 19.4 $\pm$ 1.2 dBm Output Power

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***Abstract*—A broadband fully integrated power amplifier (PA) with 3 dB bandwidth from 16.5 to 28 GHz was designed using a 0.18 μm SiGe BiCMOS process. The PA consists of a drive amplifier and two parallel main amplifiers. Lumped-element Wilkinson power divider and combiner are especially used to combine the main amplifiers as well as to provide suppression for the harmonics through their inherent low-pass filtering characteristic. The PA exhibits measured gain of more than 34.5 dB and very flat output power of 19.4 $\pm$ 1.2 dBm across 16.5–28 GHz, and power added efficiency (PAE) higher than 20% and 17% between 16–24.5 GHz and up to 28 GHz, respectively. Specifically at 24 GHz, it achieves 19.4 dBm output power, 22.3% PAE, and 37.6 dB gain.**

***Index Terms*—CMOS/BiCMOS power amplifier, power amplifier (PA), RFIC.**

I. Introduction

THE design of power amplifiers (PAs) on silicon substrates is still one of the most challenging works. Devices on silicon have low breakdown voltages which constrain the voltage swings and lead to reduced power gain. Furthermore, silicon substrates are highly conductive and hence very lossy at high frequencies, leading to reduced gain and output power. In order to resolve the low breakdown voltage problem and have more headroom for the voltage swings, cascode structure, that has higher breakdown voltage than single common emitter (CE) or base (CB), has been used for PAs designed with silicon technologies [1]–[6]. Nevertheless, it is still difficult to achieve high gain and output power with decent PAE simultaneously across wide frequency ranges for silicon-based PAs. Such PAs are always in demand, particularly at commonly used frequencies such as the ISM frequency of 24 GHz.

In this letter, we report the development of a broadband PA covering more than K-band (18–26.5 GHz) with high gain, flat and high output power, and high PAE on a 0.18 μm BiCMOS process. The PA employs two identical amplifiers in parallel, each with a cascode gain stage, and achieves good performance with output power of 19.4 $\pm$ 1.2 dBm, gain of more than 34.5 dB across 16.5 to 28 GHz, and PAE of higher than 20% from 16–24.5 GHz and 17% up to 28 GHz. Specifically, at the popular ISM frequency of 24 GHz, the PA achieves 19.4 dBm output power, 22.3% PAE, and 37.6 dB gain. We implement lumped-element Wilkinson power divider/combiner especially designed to exhibit the low-pass filtering characteristic that helps suppress the harmonics as well as enhance the bandwidth, primarily resulting in good PA performance over a wide frequency range. To the best of our knowledge, there has been no silicon-based PA reported that implements the lumped-element Wilkinson device and exploits its wideband low-pass filtering behavior.

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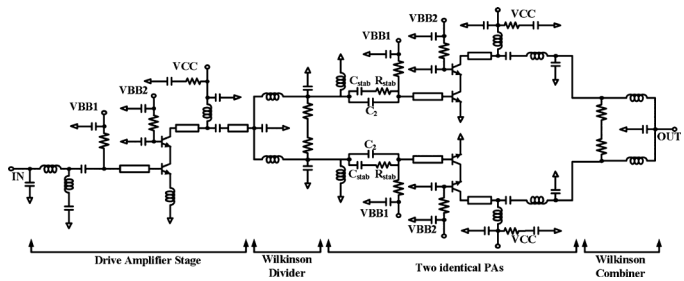

Fig. 1. Schematic of the PA.

II. Circuit Design

Fig. 1 shows the schematic of the PA, which includes a driver amplifier, Wilkinson power divider and combiner, and two identical main amplifiers. Power combining is employed to attain 3 dBm increase in output power. The main and driver amplifiers employ cascode structure, which has more gain than the CE or CB structure, for all the gain cells to achieve high gain. This leads to large device size ratio between the transistors of the main and drive amplifiers, hence resulting in desirably less burden for the drive amplifier. Furthermore, the cascode configuration also provides better reverse isolation, making it function more unilateral, hence facilitating the design.

Fig. 2 shows a photograph of the designed PA fabricated using Jazz 0.18 μm SiGe BiCMOS process [7]. The chip area is 2×1 mm^2 or 1.65×0.67 mm^2 with or without the RF and dc pads, respectively. As can be seen, all of the spiral inductors and transmission lines for the input and output feeding as well as interconnections are implemented using coplanar waveguide (CPW) on the topmost metal layer for the lowest possible loss. The common ground plane for the CPW is also extended around all the inductors to isolate the inductors from nearby elements, hence minimizing the coupling, as well as to provide a continuous ground plane as large as possible for the entire PA chip. For RFIC operating at high frequencies, a ground should

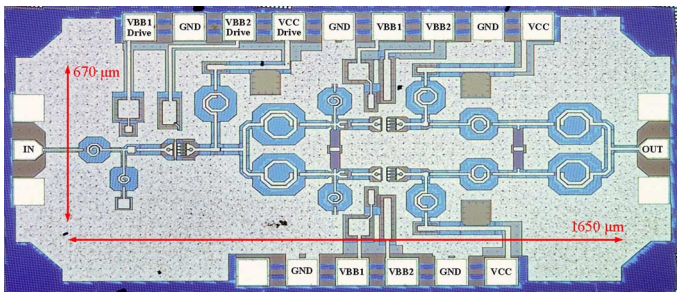

Fig. 2. Photograph of the fabricated PA.

be considered as a distributed structure, and maintaining a possible large continuous ground plane is crucial for the performance of RFICs, especially at high frequencies and/or for large chips. These components were designed and simulated using the EM simulator IE3D [8]. Furthermore, the RCX simulation in Cadence [9] was also conducted for the whole PA to extract the parasitic elements produced by the layout.

A. Main Amplifier Design

Each transistor in the main amplifiers consists of four transistor constituents, each having 0.15 μm emitter width and 10.16μm emitter length selected based on load-pull simulations for high output power under the class AB bias point. In general, PAs typically employ large transistors, thereby making them more prone to instability. To improve the PA stability and attain unconditional stability at lower frequencies, series RC circuit with shunt capacitor (C_2) [1] is connected to the input of the main amplifier as shown in Fig. 1. This RC network is designed to produce resistive loss at low frequencies so that the excessive gain of the active devices at lower frequencies can be reduced, thereby resulting in an improvement for the stability. To further improve the low-frequency stability, a 4.2 pF bypass capacitor connected in parallel with a series combination of a small 5 Ω resistor and a larger 13.2 pF bypass capacitor are used at the collector's dc supply node (V_{CC}). The simulated stability factor (K) of the amplifier is greater than 30 for all frequencies between dc and 60 GHz.

B. Lumped-Element Wilkinson Power Divider/Combiner Design

Traditionally, Wilkinson power divider/combiner is designed using two quarter-wavelength transmission lines. Using such transmission lines, however, is not desirable at 16.5–28 GHz for CMOS/BiCMOS RFICs due to their rather long length. To minimize the chip size, lumped-element Wilkinson power divider/combiner [10], [11] is implemented. The traditional quarter-wavelength transmission line is replaced with a pi-network as shown in Fig. 1. The inductance and capacitance of the pi-network can be derived as $L = Z_0/2\pi f_0$ and $C = 1/2\pi f_0 Z_0$, respectively, where Z_0 is the transmission line's characteristic impedance and f_0 is the design frequency. Fig. 3(a) shows the simulated S-parameters of the designed lumped-element Wilkinson power divider/combiner. At 24 GHz, the insertion loss is 3.66 dB and its second harmonic is rejected by more than 16 dB. As can be seen, the designed lumped-element power divider/combiner exhibits a low-pass filtering response over a wide bandwidth. This is due

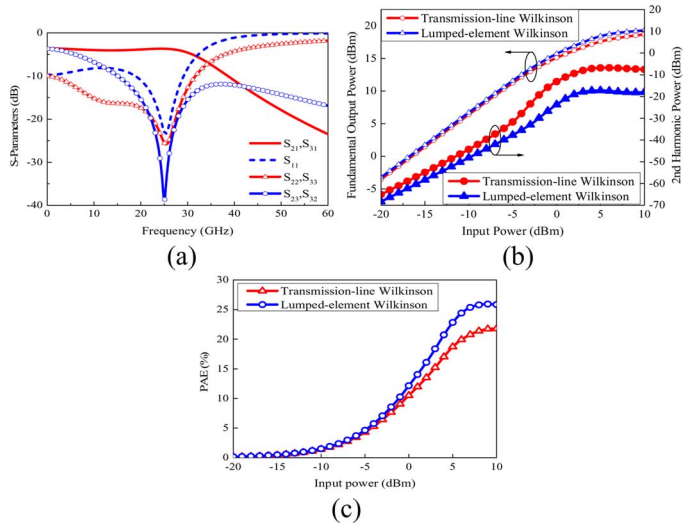

Fig. 3. (a) Performance of the lumped-element Wilkinson divider/combiner. 1 and 2, 3 are the input and two output ports, respectively. Simulated fundamental and 2nd harmonic power (b) and PAE (c) of PAs with lumped-element and transmission-line Wilkinson power dividers/combiners.

to the fact that each of its two arms resembles a synthetic transmission line which operates as a wideband low-pass filter up to a cut-off frequency. This wideband low-pass filtering behavior is exploited to suppress the undesired harmonics, which cannot be otherwise achieved on PAs employing transmission-line Wilkinson devices, as well as to enhance the bandwidth of the PA. In order to verify the harmonic suppression and improved PAE on PAs due to the use of the lumped-element Wilkinson devices with low-pass filtering, we simulated two PAs designed with lumped-element and transmission-line Wilkinson power dividers/combiners. Figs. 3(b) and (c) show the simulated output powers of the 24 GHz fundamental and 48 GHz second-harmonic signals and the PAE. As can be seen, the PA with the lumped-element Wilkinson power divider/combiner provides more suppression of the second harmonic, while producing slightly higher fundamental output power, and higher PAE.

C. Driver Amplifier Design

The driver amplifier is designed to provide the required input power for the main amplifiers. Each device of the driver amplifier combines four transistors each having 0.15 μm emitter width and 4.52 μm emitter length. With respect to the main and driver amplifiers' device sizes, the device size ratio of the input and output for the PA is larger than 4:1. A degeneration inductor, implemented by a short transmission line, is used at the emitter of the CE constituent. Inductive emitter degeneration introduces negative series feedback and enables broadband input matching. An input matching network is also included for the driver amplifier.

III. Performance

The PA was measured on-wafer. The collector voltage of the cascode device (V_{CC}) was set to 2.4 V and the dc current of drive and main amplifiers were 30 mA and 65 mA, respectively. Fig. 4(a) shows the measured and simulated small-signal S-parameters of the designed PA. The measured small-signal gain

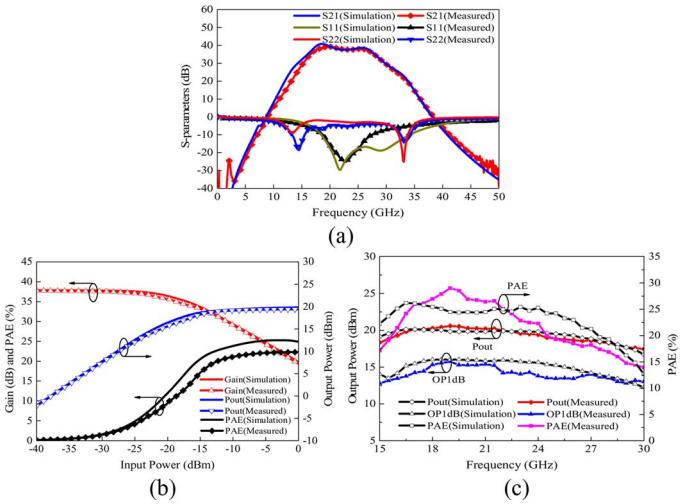

Fig. 4. Measured and simulated (a) S-parameters, (b) power gain, output power, and PAE at 24 GHz, and (c) saturated output power, OP1dB, and PAE.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH REPORTED PAS

Parameter	This work	[2]	[3]	[4]	[5]	[6]
Process	0.18μm BiCMOS	0.13μm CMOS	0.18μm CMOS	65 nm CMOS	0.18μm CMOS	0.13μm CMOS
3-dB-Gain Frequency Range (GHz)	16.5-28	24*	24*	18-22	18-23	21*
Gain (dB)	37.6 @ 24 GHz > 34.5 (16.5-28 GHz)	15.6	19	22 @ 19 GHz 26 @ 21 GHz	22.5 @ 20.5 GHz*	19.5 @ 21 GHz*
Pout (dBm)	19.4 @ 24GHz 18.3-20.6 (16.5-28 GHz)	16	19	23.8 @ 19 GHz 21 @ 24GHz 17.5-23.8 (16.5-27 GHz)	20.1 @ 20 GHz 18.1-20.1(19-22 GHz)	20 @ 21 GHz 15.4-20**
PAE (%)	22.3 @ 24 GHz 17-29 (16.5-28 GHz)	17.7	24.7	25.1 @ 19 GHz 18 @ 24 GHz	9.3 @ 20 GHz 7.3-9.3 (19-22 GHz)	12.4 @ 21 GHz 4.3-12.7**
Topology	2 Stages, Cascode	2 Stages Transformer Coupled	2 Stages, Cascode	2 Stages Transformer Coupled	3 Stages, Cascode	2 Stages, Cascode

* Only single frequency provided **Measured from 20-25 GHz

across the 3 dB gain bandwidth of 16.5 to 28 GHz is larger than 34.5 dB and matches very well with that simulated. Specifically at 24 GHz, the gain was measured as 37.6 dB which is very close to the simulation result of 37.8 dB. The measured and simulated input and output return losses also agree reasonably well. The measured input return loss is below 10 dB from 18.7 to 28 GHz. Fig. 4(b) shows the measurement and simulation results of power gain, output power, and PAE with respect to the input power at 24 GHz. At 24 GHz, the saturated output power is 19.4 dBm corresponding to the peak PAE of 22.3%, and the output power at 1 dB compression point (OP1dB) is 13.8 dBm. Fig. 4(c) shows the measured and simulated saturated output power, 1 dB compressed output power, and PAE from 15–30 GHz. As can be seen, the measured saturated output power is highest at 20.6 dBm at 19 GHz. Between 17–22 GHz, 16–25 GHz, and 25.5–28 GHz, the measured saturated output power reaches more than 20, 19, and 18.3 dBm, respectively. It is also observed that the measured saturated output power from 16.5–28 GHz is very flat within ±1.2 dBm. The measured PAE is more than 20% between 16 and 24.5 GHz and greater than 17% up to 28 GHz. The discrepancy between the simulated and measured PAE is mainly due to the differences in the simulated and measured bias conditions for the PA, which are primarily due to the unavoidable, yet expected, process variation.

Table I compares the performance of the designed PA with other reported silicon-based PAs in K-band [2]–[6]. The designed PA has the highest gain (37.6 dB at 24 GHz, higher than 34.5 dB across 16.5–28 GHz), widest 3 dB-gain bandwidth (51.7%), and very flat power response across the 3 dB bandwidth (±1.2 dBm). It also has the highest output power among the reported PA at 24 GHz, except that in [4]. However, it has better overall output power and PAE performance of 18.3–20.6 dBm and 17–29% across 16.5–28 GHz as compared to around 17.5–23.8 dBm and 5–25.1% from 16.5–27 GHz in [4], respectively. Moreover, the PA in [4] was realized on 65-nm CMOS process, its 3 dB bandwidth is only 18–22 GHz, and the power variation is larger than that of the designed PA. Although the PAE of the designed PA is lower than that of the PA reported in [3] at 24 GHz, it is higher than those in [2] and [4]–[6]. Moreover, it has high PAE across a wide bandwidth of 16.5–28 GHz, which has not been reported in other PAs [2]–[6].

IV. CONCLUSION

A broadband PA working across a bandwidth wider than K-band was designed using a 0.18 μm SiGe BiCMOS process. The PA achieves more than 34.5 dB gain and very flat out power of 19.4 ± 1.2 dBm across 16.5–28 GHz with PAE higher than 20% and 17% between 16–24.5 GHz and up to 28 GHz, respectively. At 24 GHz, the measured output power is 19.4 dBm with peak PAE of 22.3%. These results, predominantly made possible with the incorporation of a lumped-element Wilkinson power divider/combiner having a wideband low-pass filtering characteristics, demonstrate possibility of designing high-performance PAs covering wide bandwidths with high, flat output power, and good efficiency using silicon processes, which are desired for Si-based fully integrated broadband systems.

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