A Methodology for Fast VSWR Protection Implemented in a Monolithic 3-W 55% PAE RF CMOS Power Amplifier

Francesco Carrara, *Member, IEEE*, Calogero D. Presti, *Member, IEEE*, Antonino Scuderi, *Member, IEEE*, Carmelo Santagati, and Giuseppe Palmisano

***Abstract*—In this paper, the protection of CMOS power amplifiers against load mismatch is addressed. To this purpose, a closed-loop protection circuit is proposed, which is based on a novel current-mode detection and comparison technique. The circuit allows a faster protection lock-in, by enabling peak detection and loop frequency compensation to be performed at the same circuit node, thus reducing the number of low-frequency poles and improving loop bandwidth.**

The effectiveness of the method is demonstrated through the implementation of a monolithic 0.25-μm 2-V CMOS power amplifier for GSM applications, which can deliver a 3-W output power with 55% overall PAE. The amplifier is able to sustain a 20:1 load VSWR at full power. Excellent RF performance and VSWR ruggedness are hence attained simultaneously, despite a simple common-emitter power stage is used.

An experimental reliability assessment allowed the cognizant choice of the maximum drain-gate stress that could be tolerated. Device degradation was characterized by operating a power gain cell at RF, under real-world load and power conditions. Analysis of the degradation data enabled the design of an efficient, yet provably reliable, power amplifier.

***Index Terms*—CMOS analog integrated circuits, CMOS power amplifiers, CMOS radio frequency integrated circuits, CMOS reliability, differential amplifiers, high-efficiency amplifiers, mismatch protection, peak detectors, RF stress, voltage standing-wave ratio (VSWR), wear-out modeling.**

I. Introduction

THE exploitation of a standard CMOS technology for the fabrication of radio-frequency circuits aroused great interest from researchers and equipment manufacturers during the last decade [1]. Huge research and development investments were driven by the chance of designing cheap and powerful handsets, by leveraging on the high computing power, memory resources, large scale of integration, etc., all of which are unparalleled features of the digital CMOS world. Eventually, competitive designs in deep-submicron CMOS technologies appeared, for cellular applications [2] or wireless local area networks [3], thus accelerating the advent of innovative communication devices and services.

The power amplifier (PA) is one of the most critical blocks to be integrated onto a CMOS chip. The PA is, still nowadays, often fabricated in expensive technologies, such as GaAs, SiGe HBT, or LDMOS, since they exhibit several attractive features, including high-frequency/high-voltage transistors, through-hole vias for grounding, or even a semi-insulating substrate (GaAs) for high-Q passive components. Although the actual economic convenience of designing a complete single-chip multi-mode radio has been sometimes questioned [4], the realization of a CMOS PA certainly offers a broad set of design advantages, such as the possibility of integrating the PA with some functional radio blocks (thus simplifying the radio front-end module), or, more interestingly, the inclusion on the PA chip of other complex circuits that add functionality to the PA itself.

Unfortunately, the design of an efficient PA in a submicron CMOS technology [5]–[12] faces a tight trade-off between ruggedness and RF performance, especially at the high power levels required in the cellular low frequency band (824–849 MHz, 880–915 MHz). Indeed, in order to achieve satisfactory performance at RF frequencies from a CMOS PA, the use of a sub-μm channel length cannot be avoided, thus dramatically reducing the transistor breakdown voltage, which reveals to be particularly low if compared to Si-bipolar or III-V technologies with similar cutoff frequencies or current capabilities.[1] To achieve the watt-level output power required in long-range cellular communications, the transistor must be operated reasonably close to its breakdown limit, to provide a competitive efficiency.

Pioneering works demonstrated that, in saturated applications, CMOS PAs are conveniently operated in a class-E-like mode [5]–[8]. In order to obtain a high efficiency, the peak of the drain voltage is often set to be 2 to 3 times the recommended maximum supply rating of the technology. Under such a severe voltage stress, Fowler–Nordheim tunnel current through the gate oxide can degrade the insulator and device performance, even if no hard oxide breakdown occurs.

Under nominal load conditions, the gate oxide stress can be mitigated by using a variety of techniques, which have been

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[1]For example, the 2.5-V 0.25-μm NMOS transistors employed in this paper have an $f_{\max}$ of 45 GHz, which is similar to that of a high-voltage Si BJT, featuring a 6.4-V BV_{CEO} [16].

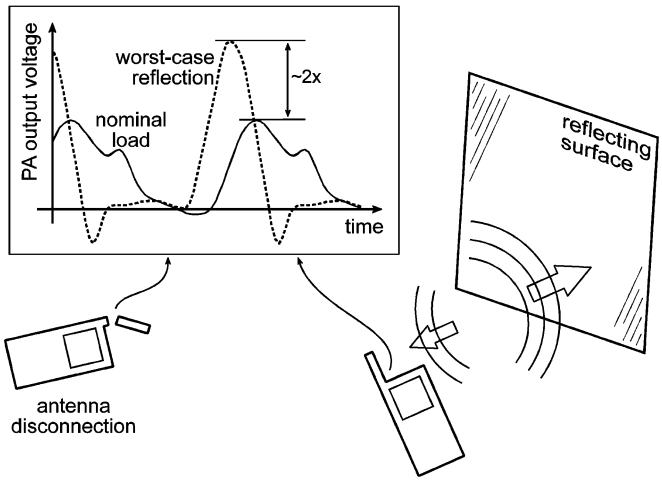

Fig. 1. Some causes of VSWR at a handset's antenna and their effect on PA output voltage.

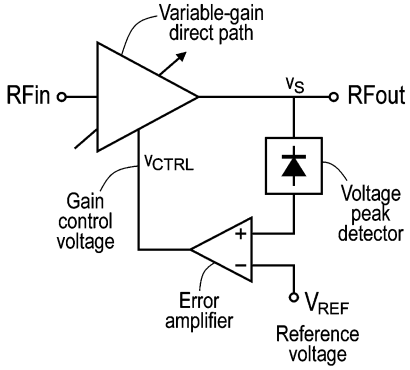

Fig. 2. Basic block diagram of a closed-loop voltage peak control system with voltage sensing and comparison.

the subject of recent literature. The use of a thick-oxide transistor is certainly beneficial, when a reduced frequency performance can be tolerated. Additionally, the exploitation of a cascode topology [10]–[12] or the stacking of more than two transistors [13]–[15] allows the output node voltage swing to be shared among multiple devices, thus augmenting the maximum supply voltage and hence improving PA efficiency.

However, device robustness has to be also guaranteed under severely mismatched conditions [16]. As it is schematically illustrated in Fig. 1, device-testing procedures, accidental disconnection of the antenna, or reflecting surfaces close to the handset may cause strong signal reflection. A circulator could be used at the transmitter output, to direct the reflected power towards a dummy load, but the additional cost makes this solution unattractive, especially in saturated applications.[2] The resulting increased drain swing, occurring at selected phase angles of the reflection coefficient, can substantially reduce the time to failure of the PA. In practical cases, the peak voltage can be even twice as large as the nominal (50-Ω) case [16]. Therefore, in order to maintain the device robustness, the maximum tolerable supply voltage should be approximately halved, unless some sort of voltage standing-wave ratio (VSWR) protection is adopted. A suitable VSWR protection circuit should: 1) exhibit fast lock-in time, since the gate oxide damage is proportional to the overall stress time [17]; 2) have no effect on RF performance under nominal conditions; 3) provide good overvoltage detection accuracy to avoid the need for an excessively conservative design; and 4) be able to process the voltage levels at PA terminals, which largely exceed the supply voltage range ($V_{\rm DD}$, ground).

This paper presents a novel PA closed-loop protection technique and its application in a CMOS power amplifier [18]. The new methodology allows both better loop bandwidth and detection accuracy to be achieved. A monolithic CMOS power amplifier is also described, featuring both watt-level state-of-the-art RF performance and tolerance to severe load VSWR. This result is achieved within a simple common-emitter topology, without the exploitation of any transistor stacking or power combining techniques, and hence better illustrates the benefits of the adopted VSWR protection methodology.

The paper is organized as follows. Section II contains a description of the protection technique and some circuit implementations. The actual protected PA integrated circuit (PA IC) design, together with its experimental characterization, is described in Section III. Finally, the Appendix summarizes the results of an in-depth experimental reliability assessment [19], which was carried out on a power gain cell under real-world load and power conditions, to find a suitable maximum operating voltage for the PA IC design.

II. Closed-Loop VSWR Protection Technique Based on Current-Mode Detection and Comparison

Closed-loop drain overvoltage control [20] can prevent PA failure without affecting the RF performance under nominal conditions. It was effectively adopted for the protection of silicon bipolar PAs [16]. This technique is a specific implementation of a more general class of systems. Indeed, closed-loop control of the peak attained by a voltage waveform is the ultimate goal pursued by several electronic equipments, such as output power control loops for radio transmitters [21], envelope feedback linearizers [22], and automatic gain control (AGC) systems [23].

In principle, all of the above-mentioned feedback systems can be basically represented by the simple block diagram shown in Fig. 2. Usually, a variable-gain block constitutes the direct path, which processes periodic signals. Output voltage $v_S(t)$ is monitored by a peak detector and the detected peak is compared with a reference voltage, $V_{\rm REF}$, by an error amplifier, whose output drives the gain control terminal of the direct chain. Provided that a suitably high loop gain is guaranteed, the feedback forces the steady-state value of the output peak to follow the reference voltage.

As already mentioned, the bandwidth requirement is usually critical for such systems (e.g., in the specific case of PA protection, high bandwidth means fast response to the overvoltage stress on the final stage). Regrettably, customary implementations of the method in Fig. 2 suffer from inherent bandwidth limitations. Indeed, feedback systems require an appropriate com-

[2]Some linear transmitter designs are, still nowadays, forced to include an output circulator to fulfill the stringent linearity specifications, even when robust transistors are used.

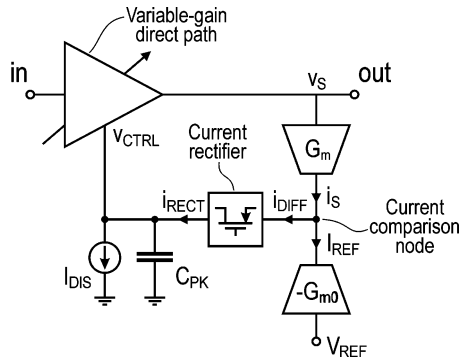

Fig. 3. Proposed current-mode approach for peak detection and comparison.

pensation to guarantee a proper phase margin to the loop frequency response. In this specific case (Fig. 2), the loop gain exhibits a low-frequency pole associated with the hold capacitor at the peak detection node. Since frequency compensation cannot be achieved at the peak detection node, due to the low impedance (too much capacitance would be required), another pole is usually introduced at a high-impedance node within the error amplifier, to be exploited as the dominant pole of the frequency response. In such a condition, the loop bandwidth is greatly limited by the peak detector's pole, which is quite slow, because proper peak detection requires this pole to be orders of magnitude below the carrier frequency.

The performance of traditional peak control loops is further limited by the accuracy of peak detectors. Usually, open-loop peak detectors are based on a diode or a transistor [25], acting as a rectifying element. Both solutions suffer from a non-zero voltage drop across the rectifying $p-n$ junction. The resulting error can be properly compensated for, but the correction accuracy is affected by the dependence of the junction voltage drop on the crest factor of the input waveform [26]. On the other hand, resorting to feedback peak detectors [27] for better accuracy is only possible at a relatively low carrier frequency.

A. Description of the Proposed Methodology

Fig. 3 shows a block diagram of a voltage peak control loop implemented according to the proposed approach [24]. This solution is based on a *current-mode* signal processing through the feedback path, rather than the usual voltage-mode one in Fig. 2. To this aim, periodic voltage $v_S(t)$ and reference voltage $V_{\rm REF}$ are converted into currents by respective transconductors G_m and G_{m0}, thus obtaining

$$i_S(t) = G_m v_S(t) \tag{1}$$

$$I_{\rm REF} = G_{m0} V_{\rm REF}. \tag{2}$$

Both currents are fed to the same circuit node, where comparison is actually performed. Indeed, by properly setting the sign of $I_{\rm REF}$, we get

$$i_{\rm DIFF}(t) = i_S(t) - I_{\rm REF} = G_m \left[v_S(t) - \frac{G_{m0}}{G_m} V_{\rm REF} \right]. \tag{3}$$

This difference current drains to a current rectifier, whose high-impedance output is connected to an integrating capacitor $C_{\rm PK}$ and to the gain control terminal, $v_{\rm CTRL}(t)$. The current rectifier only reproduces the positive portion of the input current waveform. Therefore,

$$i_{\rm RECT}(t) = \mathrm{pos}\left\{ i_{\rm DIFF}(t) \right\} \tag{4}$$

where $pos\{\cdot\}$ is defined as

$$\mathrm{pos}\{x\} = \begin{cases} x, & \text{for } x \geq 0 \\ 0, & \text{for } x < 0. \end{cases} \tag{5}$$

As long as difference current $i_{\rm DIFF}(t)$ is negative (i.e., as long as $v_S(t)$ remains lower than $(G_{m0}/G_m) \cdot V_{\rm REF}$), output current $i_{\rm RECT}(t)$ is zero, voltage $v_{\rm CTRL}(t)$ remains low (thanks to $I_{\rm DIS}$), and the loop is inactive. On the other hand, current pulses are generated at the output of the current rectifier each time $i_{\rm DIFF}(t)$ goes positive, thus charging $C_{\rm PK}$ and increasing $v_{\rm CTRL}(t)$.

Assuming that the loop gain is sufficiently high, the overall feedback system will reach a steady state condition, where the net average current flowing into $C_{\rm PK}$ is zero, that is:

$$\overline{\mathrm{pos}\left\{ i_{\rm DIFF}(t) \right\}} = I_{\rm DIS} \tag{6}$$

where symbol $\bar{\cdot}$ designates the time average of the periodic argument.

We are ultimately interested in the peak value of $i_{\rm DIFF}(t)$, i.e. $\max\{i_{\rm DIFF}(t)\}$. It can be shown that quantity $\overline{\mathrm{pos}\{i_{\rm DIFF}(t)\}}$ is an increasing monotonic function of the quantity $\max\{i_{\rm DIFF}(t)\}$, which can be locally simplified through a linear approximation, i.e., $\overline{\mathrm{pos}\{i_{\rm DIFF}(t)\}} \approx H \max\{i_{\rm DIFF}(t)\}$, having indicated with H a proportionality constant. By recalling (6) and (3) we obtain that, when the loop is locked,

$$H \cdot \max\left\{ G_m \left(v_S(t) - \frac{G_{m0}}{G_m} V_{\rm REF} \right) \right\} = I_{\rm DIS}. \tag{7}$$

Furthermore, assuming for simplicity that the current $I_{\rm DIS}$ is negligible if compared to the rectifier's output, (7) becomes

$$\max\left\{ v_S(t) \right\} = \frac{G_{m0}}{G_m} V_{\rm REF}. \tag{8}$$

Equation (8) demonstrates that both peak detection and comparison are actually implemented by the proposed approach, i.e., the approach in Fig. 3 is *functionally equivalent* to the one in Fig. 2.

It can be also recognized that the equivalent small-signal gain of the overall circuit is $H \cdot G_m \cdot R_O$, where R_O is the overall equivalent impedance at the output node of the current rectifier. It is clear, hence, that the loop gain is high as long as the current rectifier has high output impedance.

Incidentally, it can be observed that the proposed solution reverses the order of the feedback functions compared to the scheme in Fig. 2, since comparison is actually carried out *before* peak detection.

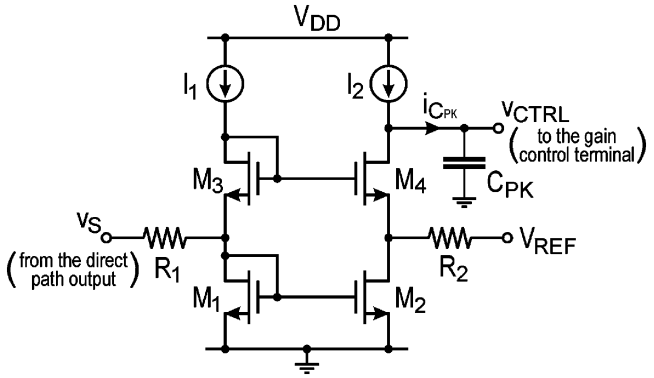

Fig. 4. Basic circuit implementation of the proposed methodology for peak detection and comparison.

B. Circuit Implementation

A simple yet effective circuit implementation of the feedback chain in Fig. 3 (i.e., the path from v_S to $v_{\rm CTRL}$) is shown in Fig. 4. The operating principle of this circuit can be understood through a one-to-one analogy with the block diagram in Fig. 3. Current comparison node is the source node of transistor M_4. Since the current in M_4 can only flow downward, this transistor performs the current rectification. The voltage-to-current conversion is obtained through resistors R_1 and R_2. Current mirror M_1–M_2 provides the sign inversion for the current signal coming from v_S, thus allowing the comparison with the reference current generated from $V_{\rm REF}$. Finally, $C_{\rm PK}$ and I_2 play the role of integration capacitor and discharge current generator, respectively.

When M_4 is on, the current balance at the output node yields

$$i_{\rm CPK}(t) = \frac{V_{\rm REF} - v_{D2}(t)}{R_2} + I_2 - \frac{(W/L)_2}{(W/L)_1}\left(\frac{v_S(t) - v_{D1}(t)}{R_1} + I_1\right) \quad (9)$$

where $i_{\rm CPK}(t)$ is the current flowing into capacitor $C_{\rm PK}$, whereas $v_{D1}(t)$ and $v_{D2}(t)$ are the drain voltages of M_1 and M_2, respectively. By setting

$$\frac{(W/L)_{2,4}}{(W/L)_{1,3}} = \frac{R_1}{R_2} = \frac{I_2}{I_1} \quad (10)$$

voltages $v_{D1}(t)$ and $v_{D2}(t)$ are approximately equal and cancel out, thus giving

$$i_{\rm CPK}(t) = -\frac{v_S(t) - V_{\rm REF}}{R_2}. \quad (11)$$

Hence, it may be stated that the use of M_3 (and its bias current I_1) is aimed at canceling the offset terms that arise in the voltage-to-current conversion performed by R_1 and R_2. Moreover, bias current I_1 compensates for the discharge current $I_{\rm DIS}$ and hence further improves detection accuracy. Incidentally, we note that the solution in Fig. 4 produces a sign inversion in the transfer characteristic. Circuit variations for higher gain or multiple input capability can easily be implemented [24].

The most important benefit of the proposed circuit is that rectification is performed at a high impedance node (i.e., the drain of M_4). The pole associated with the hold capacitor of the peak detector can thus be used to perform frequency compensation, by adding a fair amount of capacitance. Therefore, as opposed to traditional implementations (Fig. 2), there is no need to introduce another pole for compensation. Only *one low-frequency pole* will then be present, which enables a wider closed-loop bandwidth to be achieved.

Moreover, the voltage-to-current conversion in our circuit is implemented via resistors, therefore input voltages exceeding the supply range can be handled. Finally, the proposed approach is not affected by the error due to the voltage drop across customary diode- or transistor-based rectifiers. Theses features, together with the fast circuit response, make our solution very attractive for PA protection.

III. PA Circuit Design and Experimental Results

As a demonstration of the proposed protection technique, we will describe the design and experimental characterization of a power amplifier for cellular applications with integrated VSWR protection. The circuit design was performed by using a 0.25-μm CMOS technology.

The actual transistor maximum operating voltage conditions were assessed through an extensive on-wafer characterization (see the Appendix). An allowable *drain-gate* voltage swing of around 5.5 V was found.

The design effort was aimed at obtaining a 3-W RF power in the low cellular band, preserving efficiency, and ensuring VSWR ruggedness at the same time. As already mentioned, a simple common-emitter topology was chosen (neither transistor stacking nor power combining to relax the PA design trade-offs), to better demonstrate the effectiveness of the proposed protection approach.

With reference to the diagram in Fig. 3, the complete PA IC can be divided into two blocks, namely a variable-gain PA and a feedback protection circuit.

A. Variable-Gain PA

The RF variable-gain direct path is sketched in Fig. 5. It is a two-stage fully differential amplifier, with on chip inter-stage matching. The differential topology was preferred because of lower substrate noise generation, better ground impedance control, and hence simpler design of the matching networks.

The final stage comprises two common-emitter 40 mm/0.25 μm devices (M_3–M_4). To maximize the drain voltage swing and improve the efficiency, the output matching network was designed for class-E-like switching operation. To this purpose, a series resonance was implemented at the drain terminal of the final stage by exploiting the bonding wires of the package, thus creating a high impedance for the harmonics of the fundamental frequency [16]. Parasitic capacitances of drain pads and connections were carefully evaluated and absorbed in the output matching topology.

Similarly to all critical RF interconnects, inter-stage matching inductors L_{M1} and L_{M2} were designed by recourse to electromagnetic simulations and implemented by using the topmost metal layer. On-wafer experimental characterization confirmed the accuracy of the design and the good quality of those components. Indeed, a 1.43 nH inductance was measured at 900 MHz (instead of a simulated value of 1.38 nH), along with a quality

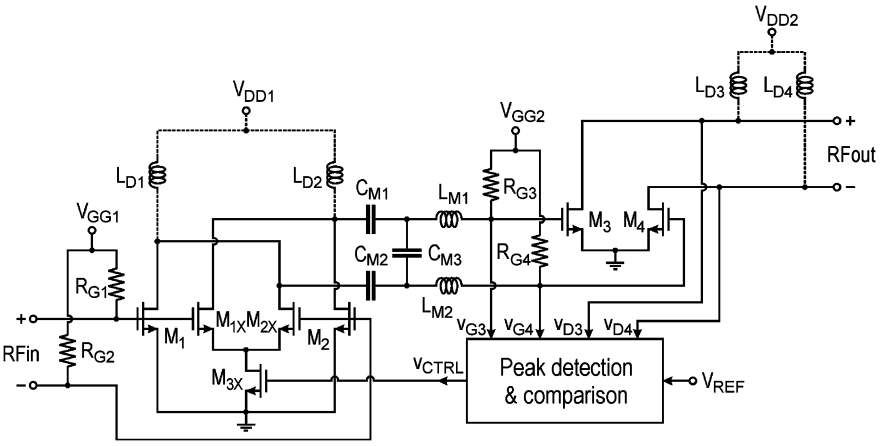

Fig. 5. Schematic of the variable-gain RF direct path.

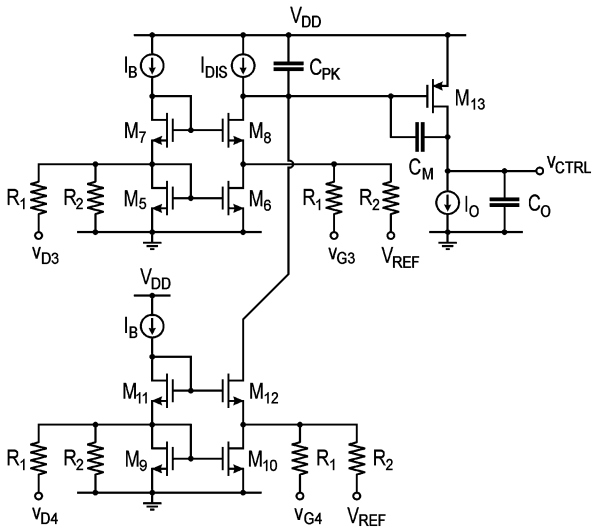

Fig. 6. Schematic of the feedback circuit for peak detection and comparison.

factor of 17.5 at the same frequency (instead of a simulated $\mathrm{Q} = 18$).

The gain variation is achieved by the cross coupled differential pair $M_{1\mathrm{X}}$–$M_{2\mathrm{X}}$ and transistor $M_{3\mathrm{X}}$. When V_{CTRL} is low, transistor $M_{3\mathrm{X}}$ is off, $M_{1\mathrm{X}}$ and $M_{2\mathrm{X}}$ are off, and the gain is at its maximum. As V_{CTRL} is increased, $M_{1\mathrm{X}}$ and $M_{2\mathrm{X}}$ are turned on by $M_{3\mathrm{X}}$ and decrease the gain of the cell, since output signal currents cancel each other. It is worth noting that $M_{1\mathrm{X}}$ and $M_{2\mathrm{X}}$ produce a beneficial effect on the amplifier stability, since they increase the reverse isolation of the RF chain by compensating the gate-drain capacitance of M_1 and M_2. Moreover, the proposed variable-gain topology features a minor variation of the PA IC input impedance with the gain setting. Indeed, to the first order, the input capacitance is constantly equal to the gate-source capacitance of M_1, M_2, $M_{1\mathrm{X}}$, and $M_{2\mathrm{X}}$ (no input disconnection or shorting ever occurs).

B. Feedback Protection Circuit

Fig. 6 shows a detailed schematic of the feedback circuit for peak detection and comparison, which is a multiple-input double-half-wave implementation of the circuit discussed in the previous section. Only one of the two rectifying paths will be described for simplicity.

The function of the circuit is to compare the peak of the final stage drain-gate voltage v_{DG3} to V_{REF}. To this purpose, a linear combination of the gate, drain, and reference voltage is created by adding two resistors to the basic scheme in Fig. 4. Indeed, by generalizing the calculations shown in the previous section, it can be stated that the circuit composed of M_5–M_8 and resistors R_1–R_2 produces a difference current $i_{\mathrm{DIFF}}(t)$ at the drain node of M_6, according to the following expression:

$$i_{\mathrm{DIFF}}(t) = \frac{1}{R_1}\left[v_{DG3}(t) - \frac{R_1}{R_2}V_{\mathrm{REF}}\right] \tag{12}$$

provided that $(W/L)_{5,7} = (W/L)_{6,8}$.

The difference current is then fed to the source of M_8, which is the current comparison node. If the peak of v_{DG3} is lower than $V_{\mathrm{REF}} \cdot \mathrm{R}_1/\mathrm{R}_2$, M_8 is off and C_{PK} is precharged to V_{DD} by I_{DIS}. As soon as v_{DG3} peak goes beyond $V_{\mathrm{REF}} \cdot \mathrm{R}_1/\mathrm{R}_2$, current pulses start flowing through M_8 (i.e., the current rectifier) and are integrated by C_{PK}. As a consequence, V_{CTRL} is increased and the RF gain is lowered. The loop is compensated by a Miller capacitor across common source stage M_{13}. Besides the obvious gain increase, this profitably pushes the pole at V_{CTRL} node (i.e., the gate of $M_{3\mathrm{X}}$) towards higher frequencies, thus improving the loop phase margin.

Closed-loop performance is compared with the unprotected open-loop one in the simulation results of Fig. 7. Under closed-loop operation, the peak voltage across the gate oxide is safely clamped at 5.5 V, i.e. at $V_{\mathrm{REF}} \cdot R_1/R_2$, with a 10:1 VSWR, for any possible phase of the reflection coefficient. On the other hand, open-loop drain-gate voltage can become larger than 9 V in the same conditions, which would suddenly destroy the gate oxide in real circumstances.

The loop stability and speed were estimated by means of the loop frequency response at the load phase corresponding to the maximum *drain-gate* overvoltage. Fig. 8 shows the simulated loop gain magnitude and phase. The loop is characterized by a 53-dB gain, a dominant pole around 40 kHz (corresponding to the drain node of M_8 in Fig. 6) and an additional second-order low-pass response around 30 MHz caused by the RF direct path.

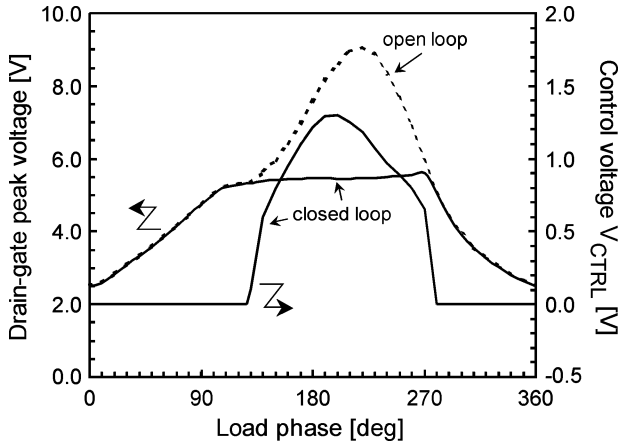

Fig. 7. Simulated drain-gate peak voltage and closed-loop gain control voltage $V_{\rm CTRL}$ versus load phase angle under 10:1 VSWR load mismatch ($f_{\rm RF}$ = 870 MHz, $V_{\rm DD}$ = 2 V, $V_{\rm REF}$ = 1.38 V, $P_{\rm in}$ = 13 dBm).

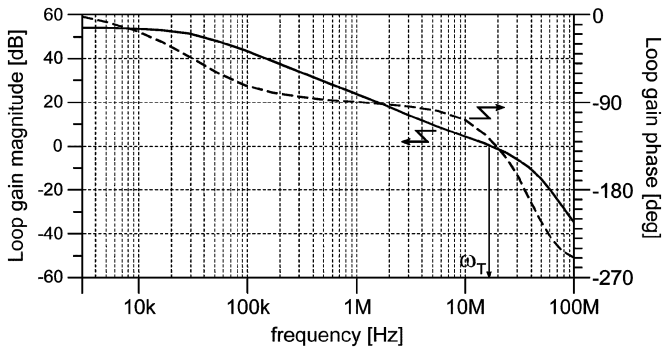

Fig. 8. Simulated frequency response of the whole VSWR protection loop gain ($f_{\rm RF}$ = 870 MHz, $V_{\rm DD}$ = 2 V, $V_{\rm REF}$ = 1.38 V, $P_{\rm in}$ = 13 dBm, for a load phase of 230° in Fig. 7).

Calculations suggest that the pole at the $V_{\rm CTRL}$ node (corresponding to a capacitive load of 13 pF) is pushed to a frequency of about 150 MHz by the Miller compensation.

The loop gain crossover frequency is f_T = 18 MHz, with a phase margin of 55°. This guarantees a well-behaved lock-in transient, with an estimated rise-time t_R of about 20 ns (since $2\pi f_T t_R \sim 3$), thus confirming the potential of the proposed technique for a fast PA protection. As already mentioned, traditional peak detection approaches (Fig. 2), would have suffered from another low-frequency pole (i.e., the pole associated with the peak detector), thus reducing the attainable loop crossover frequency to few megahertz.

As already mentioned, a varying load is present at the PA output because of moving reflecting surfaces close to the handset, accidental disconnection of the antenna, or device-testing procedures. It is therefore useful to discuss how fast the stress buildup is likely to be, in those situations.

The fastest stress increase during *normal operation* is likely to occur at the burst ramp-up, provided that a reflecting surface is already present when the transmission is initiated. As a practical example, in the GSM system the burst rise-time is limited to $\sim 10\,\mu$s, due to stringent spectrum requirements. In this specific case, then, the ~20-ns speed of the proposed implementation is even more than needed.

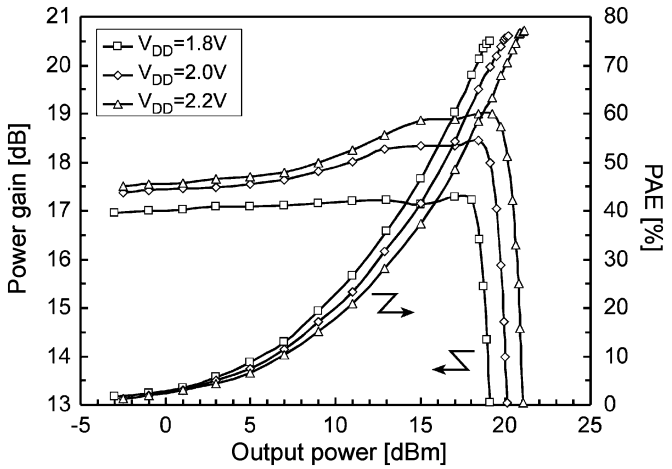

Fig. 9. Harmonic load-pull performance of the unit power transistor (W = 1.3 mm, L = 0.25 μm, $f_{\rm RF}$ = 1.9 GHz, $I_{\rm D,Quiescent}$ = 20 mA).

On the other hand, under *extreme operating conditions* the VSWR growth rate cannot be predicted so easily. For example, if the antenna can be mechanically disconnected, the VSWR change will occur at an extremely high speed. Most importantly, during device testing procedures in high-volume production, a PA should go through different performance measurements as quickly as possible. If the PA is not VSWR-rugged, the synchronization of the testing components has to be carefully considered, together with the transient behavior of the switches that are present in the test equipment. For example, an unprotected PA should be turned on only when the load is firmly connected at the output. This is certainly undesirable, since it complicates device testing, resulting in increased cost. In these extreme conditions, then, the practical benefits of the fast lock-in transient featured by the proposed implementation can be more clearly recognized.

C. Experimental Results

The PA circuit was fabricated using the 0.25-μm CMOS core of a BiCMOS technology, which offers five metal layers (4-μm -thick copper option for the topmost one) and 5-fF/μm^2 MIM capacitors. The gate oxide thickness is 5 nm. The nMOS transistors have f_T around 35 GHz and $f_{\rm max}$ of about 45 GHz.

A unit power transistor to be used as a basic cell for the PA's implementation was developed. The device is a 0.25-μm multi-finger nMOS transistor, having a total gate width of 1.3 mm (the same device was also exploited for the reliability study summarized in the Appendix).

This unit power transistor was characterized on wafer under large signal conditions by means of a multi-harmonic load-pull test bench. The impedance at the second and third harmonic frequencies was set to an open circuit, in order to reproduce the matching network implemented for the PA IC. The load at the fundamental frequency was tuned for maximum efficiency. The input signal was a continuous-wave (CW) carrier at 1.9 GHz. These measurements were conducted at an ambient temperature of 25 °C.

The power delivered by the unit transistor and the corresponding power-added efficiency (PAE) are reported in Fig. 9, for various supply voltage values. The transistor was able

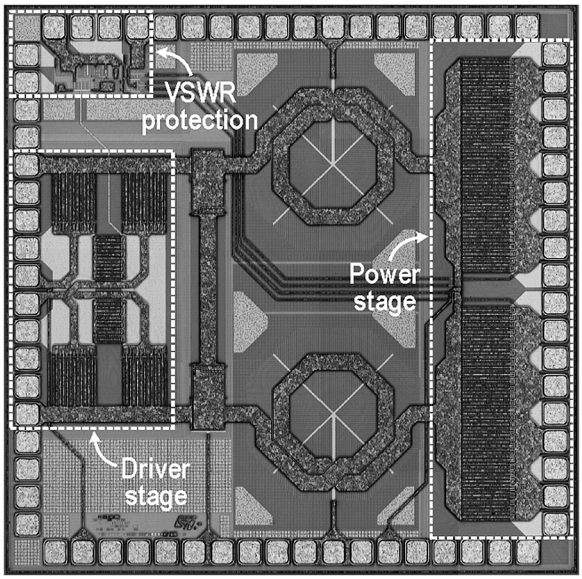

Fig. 10. Die micrograph.

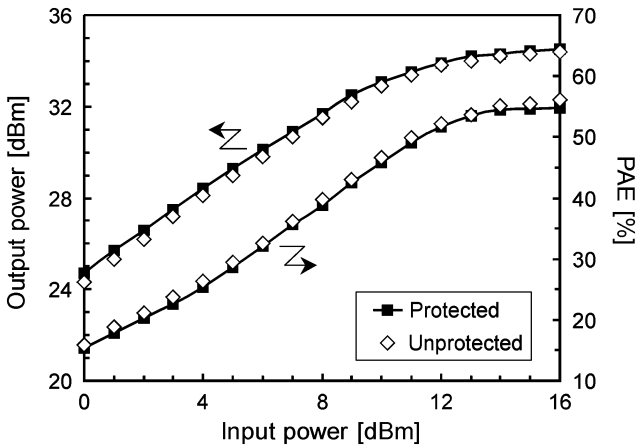

Fig. 11. Measured output power and PAE versus input power ($f_{\mathrm{RF}} = 870$ MHz, $V_{\mathrm{DD}} = 2$ V, $T_a = 25\,^{\circ}$C, pulsed mode test with 1/8 duty cycle).

to deliver a saturated output power ranging from 19 dBm to 21 dBm, with an excellent efficiency of about 75%. Power and efficiency measurements are referred to the device connections, since the input and output test bench loss had been calibrated out.

Fig. 10 is a photograph of the PA IC. The circuit was packaged in a 3 mm $\times$ 3 mm leadless quad flat plastic package with exposed ground pad, and mounted on a low-cost FR4 differential printed circuit board with discrete input and output matching networks. Measurements are referred to the differential board connectors. An array of filled metallic vias between the package exposed pad and the bottom ground plane was used for thermal dissipation. The chip size is 1.8×1.8 mm^2 including pads.

A reference PA without protection was also integrated and characterized for performance comparison.

The output power and PAE versus input power at 870 MHz are shown in Fig. 11. Under a nominal 2-V supply, a 3-W output power is achieved with a 55% PAE. The protected and unprotected PAs exhibited very similar RF performance, which

TABLE I
RUGGEDNESS TEST RESULTS

VSWR	Supply voltage [V]	With VSWR protection	Without VSWR protection
4:1	2	PASSED	PASSED
6:1	2	PASSED	PASSED
10:1	2	PASSED	FAILED
20:1	2	PASSED	
10:1	2.2	PASSED	
10:1	2.3	PASSED	
10:1	2.5	PASSED	

Test conditions: $f_{\mathrm{RF}} = 870$ MHz, $P_{\mathrm{in}} = 13$ dBm, V_{REF} for $P_{\mathrm{out}} = 34.7$ dBm in matched conditions, $T_a = 25\,^{\circ}$C, pulsed mode, all phase angles tested.

demonstrates that the loading effect of the protection circuit is negligible.[3]

Load VSWR tests were carried out on a large number of samples. The tests were conducted at an ambient temperature of 25 °C. For each VSWR value, the load phase was swept across 360°, in 5-degree steps. Approximately 30 GSM standard bursts were transmitted at each phase angle (with 12.5% duty cycle), thus giving a duration of $\sim$150 ms per each phase. The output power and the DC current under nominal conditions were monitored before and after each complete phase sweep. A chip was considered to have passed the test when the measured output power drop was less than 0.1 dB and DC current level was within $\pm 3\%$ of its starting value.

PAs without protection cannot sustain a 10:1 load VSWR when operating at 2 V. On one hand, most unprotected chips failed the test by incurring breakdown, at the final stage only, as revealed by the observation of the current drawn from the supply. A short circuit to ground was found at the gate of the broken transistors, thus suggesting that a destruction of the gate oxide occurred (i.e., a gate to bulk short). On the other hand, a few chips failed the test by revealing a power loss, which was in the range of 0.3–0.5 dB.

In contrast, protected PAs revealed no failure after a VSWR test as severe as 20:1 (0.5-dB loss at the output hybrid) under the same supply voltage. These results confirm the effectiveness of the proposed approach. They are summarized in Table I.

In order to exhaustively characterize the PA IC, due to the importance of noise performance in real-world applications, the noise generated by the PA IC in the GSM RX band was measured in a specifically designed test bench. An 850-MHz input signal was fed to the PA, after passing through a filter with $>$70 dB attenuation in the RX band (at 895 MHz) to reject the additional noise from the signal source itself. The PA output signal was then split up into the TX and RX bands, by using a duplexer with selectivity better than 70 dB. The TX signal power was measured while the noise in the RX band was being monitored. The results of this test are summarized in Fig. 12. The GSM specification for the whole transmitter is -129 dBm/Hz.

[3]According to measurements, the PA IC can deliver a saturated output power as high as 4 W when operating at 2.5 V. However, higher power levels are traded for efficiency as V_{DD} is increased, due to the lock in of the protection circuit above the nominal supply voltage.

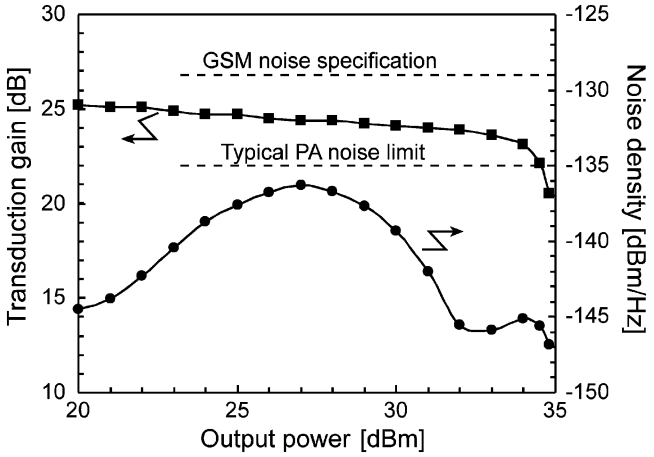

Fig. 12. Measured power gain and noise emission in the RX band ($f_{\rm TX} = 850$ MHz, $f_{\rm RX} = 895$ MHz, $V_{\rm DD} = 2$ V, $T_a = 25\,^{\circ}$C, pulsed mode test with 1/8 duty cycle).

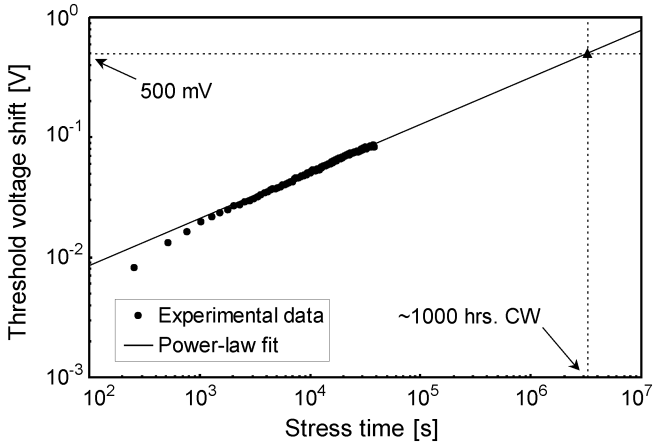

Fig. 13. Threshold voltage shift versus stress time (on-wafer accelerated ageing at $V_{\rm DD} = 2.2$ V, 3-dB compression point, continuous wave).

Typical commercial requirements for the PA alone are around −135 dBm/Hz. This limit is fulfilled with margin, especially when the PA works in saturated conditions.

IV. Conclusion

In this paper, a novel VSWR protection approach has been described and reduced to practice in a monolithic watt-level CMOS PA for cellular applications, featuring state-of-the art RF performance and ruggedness against load mismatch at the same time.

To this purpose, a novel current-mode approach for detection and comparison in voltage peak control loops has been presented, together with its circuit embodiment. The proposed solution allows peak detection and loop compensation to be carried out at the same high-impedance node, thus lowering the number of low-frequency poles and enabling faster response.

Although the proposed VSWR protection circuit can be profitably exploited in combination with other CMOS PA design techniques, such as transistor stacking or power combining, a PA featuring a common-emitter switching final stage was designed to demonstrate the effectiveness of the approach. Indeed the design trade-offs between efficiency, power, and robustness are mostly apparent in such amplifier topology. Nonetheless, the PA is capable of delivering a 3-W output power with a 55% overall PAE from a 2-V power supply, being able to sustain load VSWR values as high as 20:1.

Appendix
Power Transistor Degradation Under RF Stress

Although not always explicitly pointed out, CMOS power amplifier designers have often exceeded the voltage limits of the technology they were using by a large amount. A common rule of thumb is to set the maximum voltage swing to be about twice the recommended supply [10], [11].

The protection loop described in this paper was adjusted to clamp the *drain-gate* voltage to 5.5 V, despite the exploitation of 2.5-V nMOS transistors. This limit had to be experimentally found by studying the degradation dynamics of the power transistor [19]. Indeed, there is not any unanimously accepted transistor degradation theory under RF stress, since CMOS reliability is a well understood problem only as far as traditional (primarily digital) applications are concerned [11]. Recently, the impact of the degradation of transistor parameter on the RF performance has been studied by some researchers, by stressing the transistor with dc [28], [30], [31] or high-frequency inverter-like [29] voltage waveforms. It should be noticed, however, that the stress conditions occurring during the actual RF operation of a PA are peculiar. First of all, a switching PA is believed to suffer only from Fowler–Nordheim (FN) carrier tunneling [11], because the overlap of current and voltage is ideally zero, as opposed to high-frequency digital circuits, where hot carrier injection dominates. On the other hand, the extrapolation of a low-frequency FN characterization to multi-GHz signals is questionable.

As a consequence, there is certainly a need to characterize in detail the transistor degradation under the actual operating conditions occurring in PA applications.

A. Experimental Characterization of Degradation Dynamics

The device under test is the same unit power transistor whose performance has been already discussed in Section III-C. This device was operated on wafer, at an ambient temperature of 25 °C, under the same experimental conditions exploited for the measurements in Fig. 9.

In addition, harmonic-balance RF simulations were performed on a model of the power cell, in order to estimate the peak drain voltage occurring at each supply voltage level.

Several cyclic stress-and-sample measurements were performed to study the dynamics of degradation. During the RF stress phase, the device was driven into saturation. During the dc sampling phase, the subthreshold drain current was recorded, as an indicator of device damage. Indeed, the threshold voltage V_t increased with the stress time. This is an indication of the trapping and accumulation of negative charge in the oxide [17].

As an example, a 10-hour long accelerated ageing experiment at $V_{\rm DD} = 2.2$ V is summarized in Fig. 13. The threshold voltage approximately increases with the 0.4-th power of time.

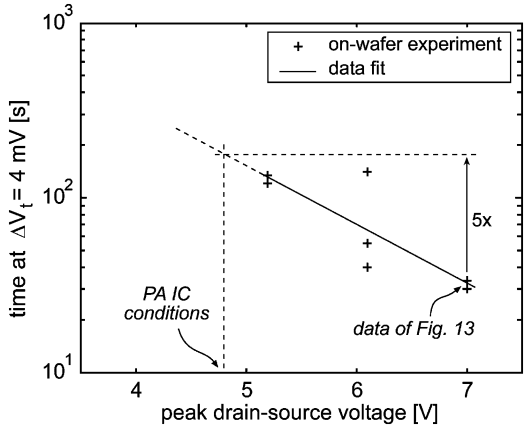

Fig. 14. Summary of on-wafer reliability characterization: time needed to reach a small 4-mV threshold voltage shift versus peak drain-source voltage. Extrapolation to PA IC operating conditions is also shown.

A 500-mV shift was assumed as the ultimate limit, since RF performance under saturated operation is relatively insensitive to the threshold voltage shift. Under such assumption, the extrapolated CW lifetime is about 1000 hours. The CW lifetime is even longer when real-world operating conditions are considered. Indeed, (a) a lower supply voltage was employed for the PA IC (2.0 V instead of 2.2 V); and (b) the source inductance found on wafer is much smaller than that present on the PA IC, and this causes a much larger peak drain voltage in the on-wafer conditions for the same value of the supply voltage.[4]

Such lifetime increase is demonstrated in Fig. 14. Similar sample-and-stress experiments were repeated on several new unit devices, while varying the supply voltage $V_{\rm DD}$ to control the stress severity. The time needed to reach a small 4-mV V_t shift, which is a good indication of the wear-out rapidity, is plotted in Fig. 14 versus the simulated peak drain voltage. The operating conditions of the PA IC $(\max(v_{\rm DG}) = 5.5\ {\rm V})$ correspond to a maximum $v_{\rm DS}$ of 4.8 V. Therefore, a 5-fold larger lifetime can be deduced for the PA IC compared to the on-wafer experiment of Fig. 13, i.e., 5000 hours of full-power CW operation for a 500-mV V_t shift are expected.

As a final remark, it is worth noting that the GSM/GPRS communication standard provides a transmission duty cycle ranging between 12.5% (GSM or Class-2 GPRS) and 50% (Class-12 GPRS), which should extend the PA IC lifetime accordingly.

ACKNOWLEDGMENT

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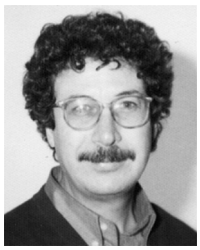

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