A 1.9GHz SiGe BiCMOS PHS Transceiver with an Integrated PA and a Fast Settling PLL

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Abstract — **A fully integrated PHS transceiver achieving -105dBm sensitivity and +21dBm output power is presented. The transceiver is implemented in a 0.35μm SiGe BiCMOS process occupying an area of 13 mm^2 and dissipating 74mA in receive mode and 280mA in transmit from 3V supply. The receiver is based on a low-IF architecture and does not require any external filters. The TX integrates a linear +21dBm Power Amplifier and achieves 5% EVM and -60dBc ACP. The transceiver integrates a fractional-N synthesizer with <30μs lock time and -120dBc/Hz phase noise @ 600kHz offset frequency. The base-band interface is at 1.2MHz, compatible with commercially available PHS base-band chips to create a two chip solution for PHS phones.**

Index Terms — **PHS, Transceiver, Low-IF Architecture, Power Amplifier, PLL, SiGe BiCMOS.**

I. Introduction

The personal handy phone system (PHS) operates at 1.9GHz, and can be used as a home cordless phone or a microcell mobile phone. Current generation PHS transceivers are usually implemented as a multi-RF chip solution, with SAW filters, ceramic filters, two RF VCOs, an external phase locked loop (PLL), and at least 150 discrete components, which increase both complexity and cost. In [1], the RF front end, consisting of a low noise amplifier (LNA), power amplifier (PA) and antenna switch, was implemented in GaAs, while the up/down conversion, IF section and PLL were implemented in BiCMOS. A similar approach was taken in [2], while in [3] an up-converter together with an automatic gain control amplifier was implemented in GaAs in order to integrate the whole transceiver in a single chip.

The transceiver presented in this paper is the most highly integrated, lowest Bill of Materials (BOM) PHS transceiver reported. It incorporates a low-IF receiver with -105dBm sensitivity, a transmitter with an on-chip +21dBm output PA and a fractional-N synthesizer with <30μs lock time. The total BOM is 37 components including the TRX switch and TCXO. The transceiver was fabricated in a 0.35μm SiGe BiCMOS process and fully complies with the RCR-28 PHS standard. A block diagram of the transceiver is shown in Fig. 1.

II. Transceiver Design

A. Receiver Design

The receiver subsystem consists of an RF I/Q down-converter which establishes the noise level of the entire receiver subsystem by providing high gain and low noise signal to the IF receiver, and an IF up-converter that provides channel selectivity, a 1.2MHz receiver interface compliant to commercially available PHS base-band ICs, and a test interface.

The RF down-converter section consists of a differential LNA and an image reject mixer. Since the required sensitivity is -100dBm and blockers can be as high as -47dBm, the RF front end requires a minimum instantaneous dynamic range in excess of 53dB. To obtain a high front end gain, a two stage LNA with a differential cascode as the first stage was used, as depicted in Fig. 2 (a). A double balanced Gilbert cell mixer, as shown in Fig. 2 (b), down-converts the 1.9GHz signal to a low-IF of 450KHz, with RL, CL and CL2 providing out of band low pass filtering. NMOS input devices M1-M4 provide high linearity, while bipolar commutating switches reduce the required LO swing while minimizing flicker noise. The designed front end has a total voltage gain of 37dB and noise figure of 2.5dB.

The IF up-converter subsystem consists of a 450kHz band pass filter (BPF), an IF amplifier, an up-converter, a 1.2MHz BPF, a second IF buffer, and a poly-phase network. A Chebychev BPF with 0.5dB ripple provides additional filtering after the up-conversion to 1.2MHz. Total combined group delay is less than 30μs with a maximum group delay variation of 4μS. Channel selection is realized by a 7 pole 450kHz BPF Gaussian op-amp RC filter. The BPF has a gain of 12dB to offset its noise contribution, which allows the use of smaller capacitors to minimize area as compared to [4]. To prevent saturating the filter, an IF programmable gain amplifier (IF-PGA) is used to attenuate the input signal by up to 30dB from a maximum gain of 12dB. In addition, DC offset compensation and automatic filter calibrations are utilized.

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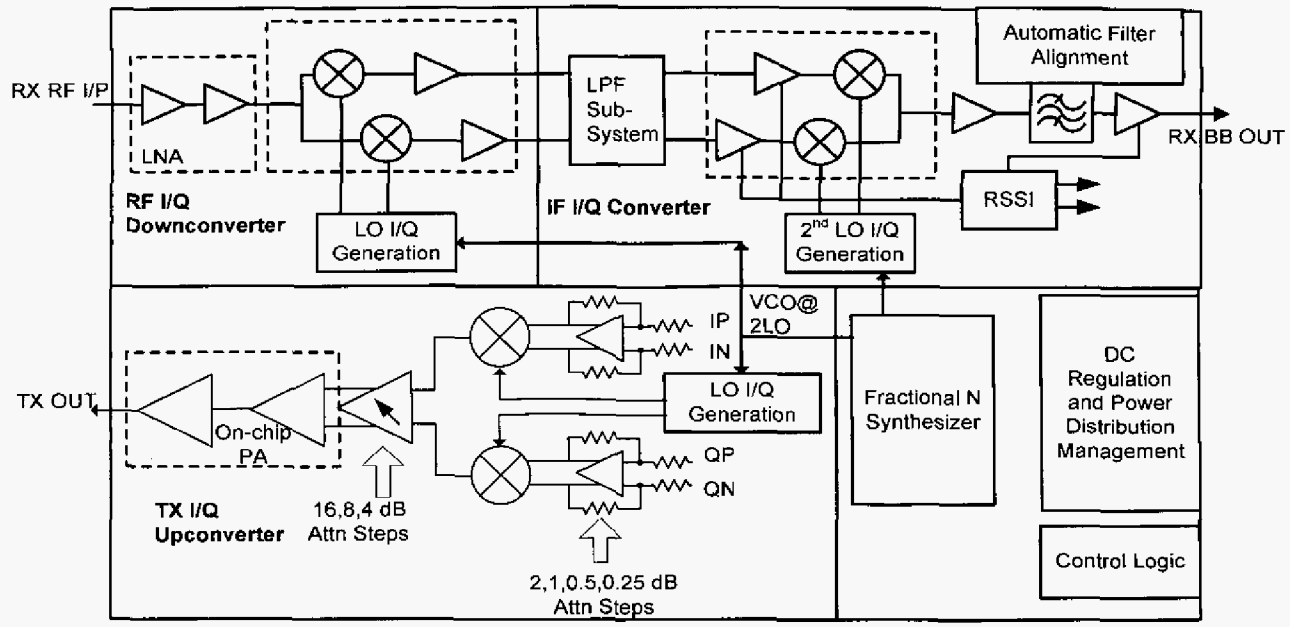

Fig. 1. Transceiver Block Diagram

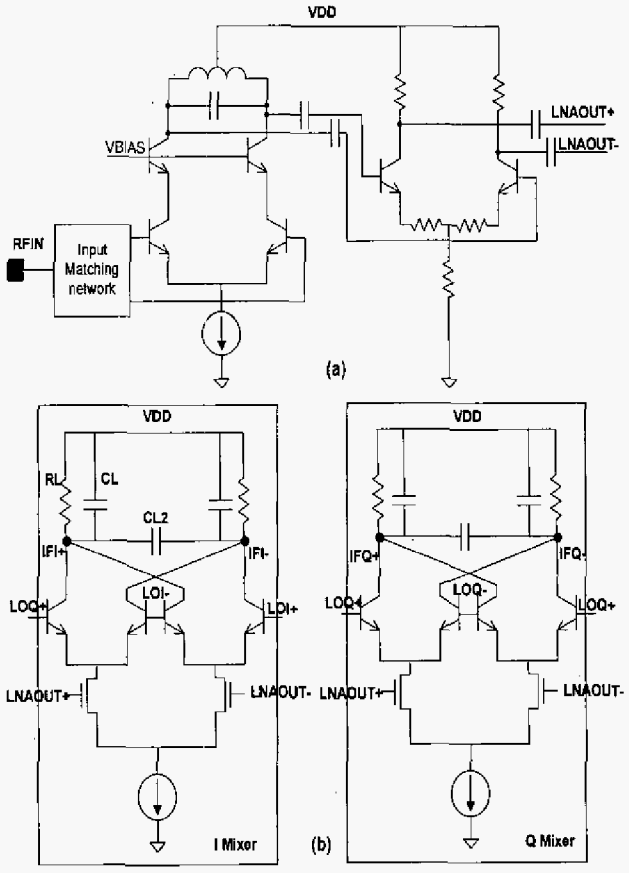

Fig. 2. Simplified schematic for the LNA (a) and I/Q down-conversion mixer (b)

Embedded within the IF amplifier stages is a received signal strength indicator (RSSI) using a successive detection architecture that delivers an RSSI voltage, dB linear to the input signal power for use by the base-band chip [5]. This signal is also used to control the gain of the IF-PGA. The signal level to the second mixer input needs to be maximized to reduce the self-jamming effects of the second LO leakage. Direct digital frequency synthesis [6] was employed to generate the second LO. The 1.2MHz BPF filters the unwanted mixing products generated by the 2nd mixer before it is amplified by the output buffer.

B. Transmitter Design

The transmit circuit block diagram is shown in Fig. 1. The transmitter is designed to accept DC coupled quadrature PHS base-band inputs, and includes compensation circuitry to remove up to 30mV of DC offset. The base-band signals are buffered and applied to the quadrature modulator where they are combined and directly converted to the 1.9GHz RF.

The modulator was designed with a similar topology to the one used in the RX to achieve high linearity. The quadrature signals were summed into a current combining load. The design relies upon layout matching and device sizing to obtain the best sideband suppression. The TX chain includes a digitally controlled 32dB programmable gain amplifier (PGA) with 0.25dB resolution that is used to shape ramp profiles during transmission power-up and power-down cycles, and as a digital control for factory calibration of the output power. The PGA is distributed between the TX IF and RF sections. The least significant

4dB is implemented in the TX IF while the remaining gain control is implemented at the RF as shown in Fig. 1. A differential to single-ended conversion stage is implemented before the PA.

The PA consists of two stages of class-A common emitter topology with external inductors for matching and DC supply. The bias circuit for the first stage is current controlled. As the input power is increased, the DC base voltage drops in order to maintain a constant collector current. The bias circuit for the output stage is voltage controlled. An increase in RF power to this stage causes an increase in the rectified DC base-to-emitter junction current. Unlike the first stage, this allows the collector current to increase with RF input power. Both bias circuits use external high precision resistors to set the bias current or voltage.

C. PLL Design

A highly configurable fractional-N architecture was selected in order to meet the challenging phase noise and switching time requirements of PHS standard. Fractional-N synthesizers break the traditional tight relationship between PLL bandwidth, resolution and reference spur level. A fractional-N synthesizer provides the opportunity to have extremely fine resolution while simultaneously keeping a large loop bandwidth. Compared to their Integer-N counterparts, fractional-N synthesizers have smaller settling time and lower close-in phase noise at the expense of higher out of band noise and spurs. A third order sigma-delta modulator was used for shaping the quantization noise as well as distributing the energy of bit-note signals inherently present in fractional-N synthesizers. The modulator has a MASH architecture with internal accuracy of 18 bits providing a resolution of 73Hz at 1.9GHz. The sigma-delta modulator directly modulates the division value of a Multi-Modulus Prescaler and a programmable divider. A 3.8GHz VCO with average KVCO of 250MHz/V is used followed by a low noise divide by 2 to generate the LO.

III. MEASUREMENT RESULTS

This highly integrated PHS transceiver was fabricated in a 0.35μm SiGe BiCMOS process and the die photo is shown in Fig. 3. The total area is 13 mm^2. The receiver sensitivity is measured by sending a 384kbps π/4 QPSK modulated signal as an input to the receiver. Fig. 4 shows the receiver sensitivity of -105dBm at BER < $1x10^{-2}$ and BER < $1x10^{-5}$ for input levels > -98dBm meeting the PHS standard with good margin. An image rejection of 30dB and -18dBm IIP3 was measured. The TX +21dBm output power is shown in Fig. 5. At this power level the EVM did not exceed 5% rms while the ACP was lower than -60dBc. Fig. 6 shows the phase noise measurements for the PLL achieving lower than -120dBc/Hz at 600kHz offset. At this level of noise, the lock time for 45MHz frequency jump at 1.9GHz center frequency was measured to be less than 30μs as shown in Fig.7. From a 3V supply, the RX consumes 74mA while the TX consumes 280mA.

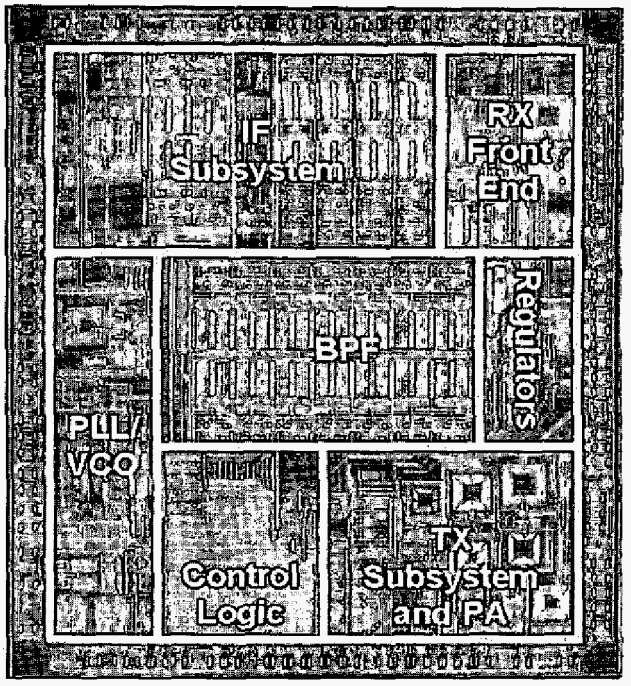

Fig. 3. PHS transceiver die photo.

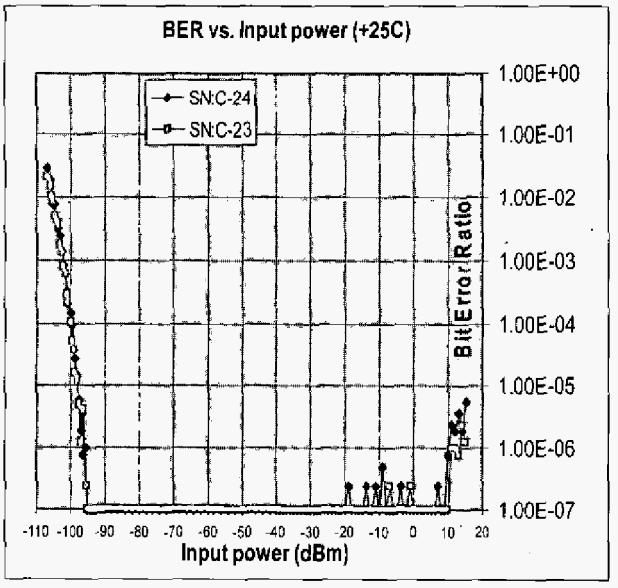

Fig. 4. Measured BER for 2 chips.

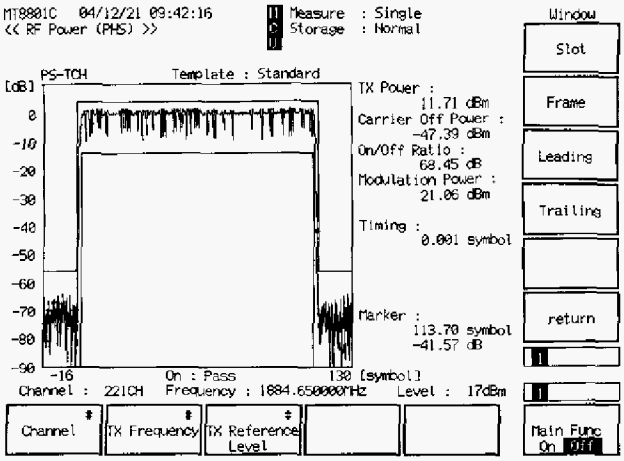

Fig. 5. TX output power within PHS mask

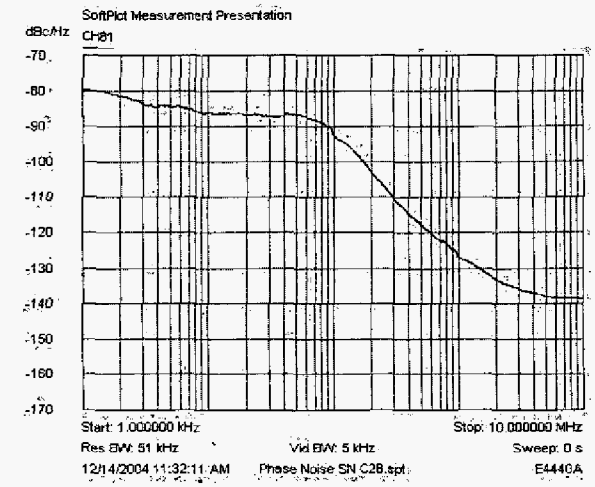

Fig. 6. Phase noise measurements

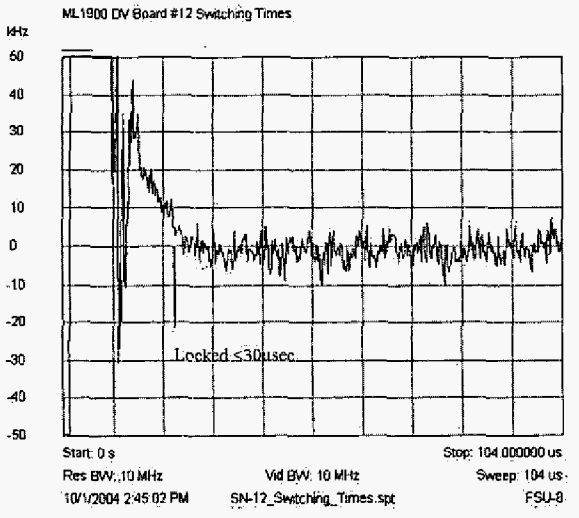

Fig. 7. PLL lock time measurements

IV. Conclusion

This paper presents a fully integrated PHS transceiver with a low BOM count that reduces the complexity and cost of PHS phones by integrating most of the radio functional blocks into a single chip. It includes a +21dBm PA, a -105dBm sensitivity RX, a fractional-N synthesizer with <30μs lock time and superior phase noise-tuning range combination. Table 1 summarizes the transceiver performance.

Table 1
Summary of transceiver performance

Receiver sensitivity	-105dBm @ BER<$1x10^{-2}$
	-98dBm @ BER<$1x10^{-5}$
RX image rejection	30dB
TX O/P power @1.9GHz	+21dBm
TX EVM@21dBm power	5%rms
TX ACP @600kHz	-60dBc
PLL lock time	<30μs
PLL Phase noise	-120dBc @ 600kHz
Current consumption	RX: 74mA, TX: 280mA
Area	$13mm^2$
Technology	0.35um SiGe BiCMOS

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