A High-Efficiency SOI CMOS Stacked-FET Power Amplifier Using Phase-Based Linearization

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***Abstract*—A linearization technique based on the phase correction is proposed for a CMOS stacked-FET power amplifier (PA). The linearizer employs a phase injection circuit as a main linearizer. The phase injection circuit presents envelope-reshaped capacitance to the gate of a driver amplifier to correct for phase compression near saturation. It also helps with AM-AM linearization. Hybrid bias circuit consisting of a diode and a resistor is also employed for static adaptive biasing, which allows the PA to meet stringent linearity requirement across the entire power range. Two stacked-FET linear PAs with the proposed linearizers have been designed using a silicon-on-insulator (SOI) CMOS process at 1.88 and 0.9 GHz. The fabricated PAs show adjacent channel leakage ratios (ACLRs) better than -39 dBc with peak power-added efficiencies (PAEs) of 44.3 and 49.2% at 1.88 and 0.9 GHz, respectively, using 3GPP uplink W-CDMA signal.**

***Index Terms*—CMOS, envelope injection, linear, linearization, power amplifier (PA), SOI, stacked-FET, W-CDMA.**

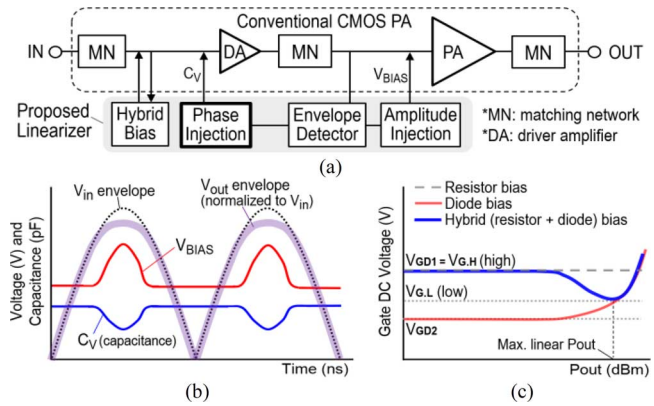

Fig. 1. (a) Block diagram of the proposed linear CMOS PA. (b) Capacitance ($C_{\rm V}$) and gate bias voltage ($V_{\rm BIAS}$) profiles by the phase and amplitude injection circuits. (c) Gate dc voltage profile by the hybrid bias circuit.

I. Introduction

CMOS power amplifier (PA) can play an important role not only for WiFi but also for 3G/4G mobile terminals due to the cost and size benefits. However, low breakdown voltage and highly nonlinear nature of the CMOS devices make the design of a watt-level linear PA very challenging, in particular, for applications using high-level modulation schemes. To achieve the required power level for 3G/4G handsets, several power combining techniques such as the stacked-FET and differential cascode have been introduced [1]–[3]. To improve the PA linearity, various linearization techniques have been proposed such as the capacitance compensation, PA-closed loop feedback, and adaptive bias [2]–[7]. However, the overall linearity and PAE cannot match those of GaAs HBT PAs [8].

For modulated signals, PA nonlinearity is determined by the dynamic AM-AM and AM-PM characteristics. The previous works on PA linearization have focused on the correction of AM-AM distortion at high output power ($P_{\rm out}$) using adaptive biasing or envelope-reshaped gate bias [3]. These methods do not correct for AM-PM distortion and, in some cases, degrade the linearity at backed-off power levels [9]. The idea of using a varactor for AM-PM correction has been presented in [7]. However, the method is limited to the quasi-linear region with negligible AM-AM distortion. Also, it requires a separate DSP chip and D/A converter, which makes the application to the self-contained mobile phone PA practically difficult.

In this work, a new linearizer based on AM-PM correction is proposed using an envelope-dependent capacitance injection technique. The AM-PM linearizer of this work also helps recover AM-AM distortion. Combined with auxiliary amplitude injection and hybrid biasing techniques, 1.88 GHz and 0.9 GHz SOI CMOS PAs of this work achieve 44% and 49% PAEs at 28.7 and 29 dBm, respectively, while meeting W-CDMA ACLR of -39 dBc. These efficiencies are among the highest ever reported from CMOS PAs for handset applications.

II. Circuit Design

Fig. 1(a) shows an overall block diagram of the proposed PA. The linearizer consists of an envelope-dependent phase injection (PI) circuit and an amplitude injection (AI) circuit as well as a hybrid bias circuit. As described in [3], the AI provides the envelope-reshaped gate bias ($V_{\rm BIAS}$) to the main-stage amplifier to recover the compressed envelope magnitude, thus improving AM-AM linearity. However, it often degrades AM-PM since higher $V_{\rm BIAS}$ during compression increases gate-source capacitance ($C_{\rm gs}$) of common-source (CS) transistor, which further compresses AM-PM characteristics [4]. In this work, we have employed a PI circuit as a main linearizer and used AI circuit as an auxiliary. To correct for AM-PM distortion, the PI circuit presents the envelope-reshaped capacitance ($C_{\rm V}$) to the input of the driver amplifier as shown in Fig. 1(b). In addition, this PA contains a hybrid bias circuit to set the power-dependent static bias to the driver-stage as shown in Fig. 1(c). This helps recover the linearity at backed-off power levels.

The overall circuit schematic of the two-stage CMOS PA is shown in Fig. 2. The power- and driver-stages use a quadruple-stacked FET with 20 mm gate-width and a triple-stack with 2 mm gate-width, respectively [1]. The bias of the driver-stage

Manuscript received July 10, 2014; accepted September 03, 2014. Date of publication September 19, 2014; date of current version December 01, 2014. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) 2013R1A2A1A05006502.

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Digital Object Identifier 10.1109/LMWC.2014.2357782

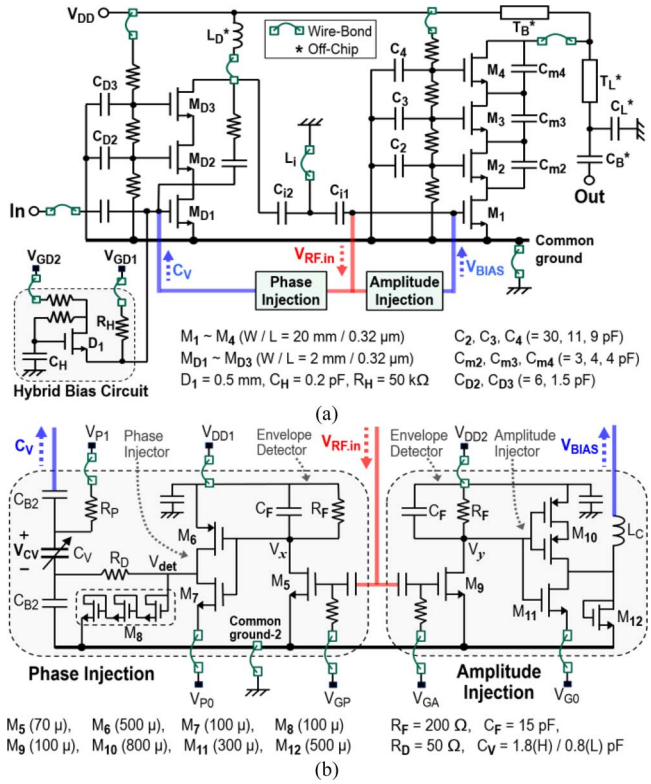

Fig. 2. (a) Schematic of the proposed linear PA for 1.9 GHz operation. (b)Detailed schematic of the phase and amplitude injection circuits.

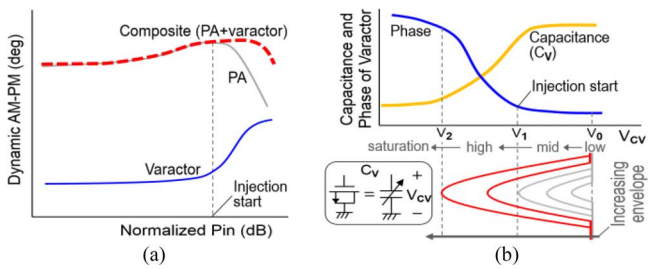

Fig. 3. Operation of the phase injector. (a) Dynamic AM-PM curves with phase injection. (b) $C_{\rm V}$ and phase ($\angle S_{21}$) of the varactor as a function of $V_{\rm CV}$.

is set at a higher level than the power-stage. This FET sizing and biasing allows the PA to achieve optimum efficiency and linearity in conjunction with the proposed linearizer. The envelope is detected at the power-stage input, and the envelope-reshaped $C_{\rm V}$ and $V_{\rm BIAS}$ are generated by the PI and AI circuits, respectively. $C_{\rm V}$ is injected to the gate of the driver-stage CS transistor while $V_{\rm BIAS}$ is applied to the main-stage CS transistor (M_1). Since $C_{\rm gs}$ of M_1 is very large ($\sim$ 22 pF), $C_{\rm V}$ is injected to the driver-stage to avoid excessive capacitance loading ($= C_{\rm gs,M1} + C_{\rm V}$) of the power-stage.

The details of the PI and AI circuits are shown in Fig. 2(b). Envelope detection is performed using two envelope detectors (M_5, M_9, $C_{\rm F}$, and $R_{\rm F}$). Because the CS detectors generate the output envelopes ($V_{\rm x}$ and $V_{\rm y}$) in opposite phase to the input envelope, $V_{\rm x}$ and $V_{\rm y}$ are flipped again by the inverter-like envelope shapers (M_6, M_7, M_{10}, and M_{11}). To avoid excessive voltage injection near saturation, two limiters (M_8 and M_{12}) are used.

To explain the PI mechanism, the phase and capacitance variations of a shunt varactor are plotted in Fig. 3. Since the typical AM-PM of the CMOS FET shows compressive characteristics

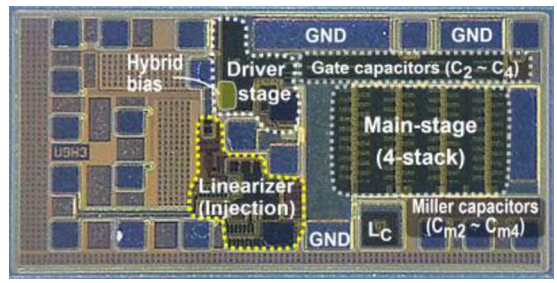

Fig. 4. Photograph of 1.9 GHz SOI CMOS IC (size $= 1.4\ {\rm mm} \times 0.68\ {\rm mm}$).

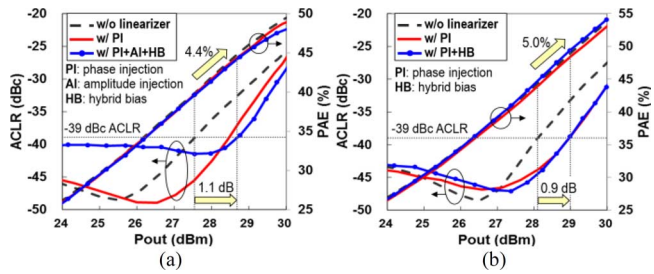

Fig. 5. Measured W-CDMA results: (a) 1.88 GHz PA. (b) 0.9 GHz PA.

as shown in Fig. 3(a), the phase injector is required to provide positive slope vs the envelope, which requires negative capacitance slope. Thus, the voltage across the varactor ($V_{\rm CV}$) is required to track the envelope signal in the opposite direction. This is achieved by applying the detected envelope signal [$V_{\rm det}$ in Fig. 2(b)] to the cathode of the varactor. The varactor is realized using source-drain connected nMOS capacitor. During low to mid $P_{\rm out}$ region, $V_{\rm CV}$ stays between V_0 and V_1 in Fig. 3(b), where $C_{\rm V}$ is almost constant, resulting in little PI. When $P_{\rm out}$ is further increased, $V_{\rm CV}$ decreases below V_1, reaching V_2 at the maximum swing. Due to the reduced capacitance of the varactor, positive PI occurs in this region. Thus, the resultant dynamic AM-PM of the composite PA is flattened as shown in Fig. 3(a). Finally, when the PA enters strongly saturation, the limiter (M_8) is turned on and prevents $V_{\rm CV}$ from decreasing below V_2. It is worthwhile to note that the PI also improves AM-AM linearity since the dynamic $C_{\rm V}$ correction by the phase injector improves input matching at high power levels where AM-AM is compressed. Simulation shows that gain compression is reduced from 1.8 dB to 1 dB when the PI is applied. The AI circuit works as an auxiliary correction to provide fine adjustment to AM-AM distortion. The required $V_{\rm BIAS}$ injection range becomes much smaller than that without PI [3], resulting in minimal efficiency degradation. The linearization effect of the circuits can be limited for wide bandwidth signal if the time delay between the incoming RF signal and PI/AI signal ($C_{\rm V}$ and $V_{\rm BIAS}$) cannot be adjusted properly.

To achieve sufficient linearity margin across the entire power range, it is desirable to set high bias at low power region, lower the bias as the power reaches soft compression and then inject the envelope amplitude at hard compression as shown in Fig. 1(c) [2], [9]. In this work, a hybrid bias circuit consisting of a resistor and a diode is applied to the driver-stage to realize the desired adaptive biasing. As shown in Fig. 2(a), the resistor and the diode are biased differently using dual biases ($V_{\rm GD1}$ and $V_{\rm GD2}$). The required gate voltage step, $V_{\rm G.H} - V_{\rm G.L}$ in Fig. 1(c), can be controlled with the voltage difference ($V_{\rm GD1} - V_{\rm GD2} > 0$).

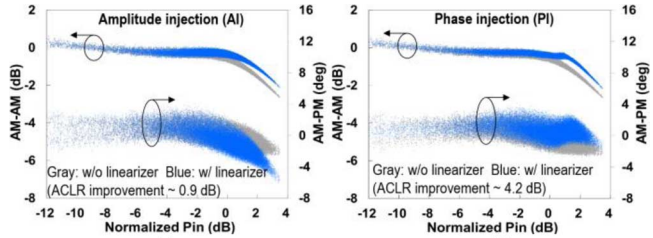

Fig. 6. Measured dynamic AM-AM and AM-PM of 1.88 GHz PA at $P_{\rm out} = 28.7$ dBm using a W-CDMA signal. (a) AI only. (b) PI only.

TABLE I
PERFORMANCE COMPARISON OF THE STATE-OF-THE-ART LINEAR CMOS PAS

Ref	CMOS Technology	Signal	Freq (GHz)	$P_{\rm out}$ (dBm)	Gain (dB)	PAE (%)	ACLR (dBc)	$V_{\rm DD}$ (V)
[8]	GaAs HBT	W-CDMA	1.95	28	N/A	44.5	–38	3.4
[1]*	0.13 μm (SOI)	W-CDMA	1.9	28.5	14.6	38.7	–38	6.5
[2]†	0.13 μm	W-CDMA	1.88	27.1	28.3	28	–40	3.0
[3]*	0.18 μm & IPD	W-CDMA	1.85	26.8	15.8	43.3	–37	3.5
[4]	0.5 μm	W-CDMA	1.75	24	23.9	29	–35	3.3
[6]†	0.18 μm	W-CDMA	1.95	23.5	26	40	–33	3.4
[10]	0.32 μm (SOI)	W-CDMA	0.84	27.1	N/A	47.5	–36	4.0
[11]*	0.18 μm	LTE‡	1.85	27.8	14.2	41	–31	3.5
This work	0.32 μm (SOI)	W-CDMA	0.9	29	28	49.2	–39	4.0
			1.88	28.7	24.5	44.3	–39	4.0
		LTE‡	0.9	27.7 26.3	28 28.3	42.9 36.5	–31 –35.5	4.0
			1.88	27.3 26.2	24.5 24.7	38.5§ 34.3	–31 –35.5	4.0

*Single-stage PAs. †On-chip output matching.
‡Uplink LTE 10 MHz-bandwidth 16-QAM (PAPR = 7.5 dB)
§Estimated PAE of the main-stage amplifier only is 40.5%.

III. FABRICATION AND MEASUREMENT

The designed PA was fabricated using an SOI CMOS process. All the MOSFETs have 0.32 μm gate length with an oxide thickness of 5.2 nm. Fig. 4 shows a photograph of the fabricated SOI CMOS PA IC for 1.9 GHz operation. The IC was mounted on a 400 μm-thick FR4 PCB, where LC-based off-chip output matching network with a loss of 0.33 dB was implemented. The PA was first tested using 3GPP uplink W-CDMA signal at 1.88 GHz. $V_{\rm DD}$ was set at 4 V and the quiescent currents of the driver and main stages were 14 and 80 mA, respectively. Considering the small dc voltage and swing across each FET stack in the quadruple design ($V_{\rm DC} = 1$ V for each stack), we have employed Class- $\rm F^{-1}$-type harmonic load termination to improve the efficiency of the stand-alone PA. The measured results are plotted in Fig. 5(a). Three different cases are compared, PI only, both PI/AI with hybrid biasing and no linearization (reference). With both linearizers, the PA shows a gain of 24.5 dB, an ACLR of -39 dBc, and a PAE of 44.3% at $P_{\rm out} = 28.7$ dBm. Compared with the case of no linearization, the maximum linear $P_{\rm out}$, defined by the power meeting -39 dBc ACLR, is increased by 1.1 dB and PAE by 4.4%. As one can see from Fig. 5(a), most of the linearization effect comes from the PI as expected. The addition of hybrid bias helps improve ACLR in the max power region while trading off ACLR in the mid-power region. PAE degradation by dc power consumption of the linearizer is less than 0.5%. Also, a 900 MHz PA was designed with the similar architecture and fabricated using the same process. W-CDMA test results are plotted in Fig. 5(b), showing a gain of 28 dB, an ACLR of -39 dBc, and a PAE of 49.2% at $P_{\rm out} = 29$ dBm, in which the linear $P_{\rm out}$ and PAE is improved by 0.9 dB and 5%, compared to the reference PA. In the case of 900 MHz PA, no measurable improvement was achieved using AI. LTE performance was also measured with 10 MHz 16-QAM signal. 1.88 GHz PA showed a PAE of 38.5% at $P_{\rm out} = 27.3$ dBm and 0.9 GHz PA showed a PAE of 42.9% at $P_{\rm out} = 27.7$ dBm while meeting $\rm ACLR_{E-UTRA} = -31$ dBc. The PAE of the main-stage alone is estimated to be 40.5% for 1.88 GHz PA.

To validate the linearization effect of the proposed linearizer, the dynamic AM-AM and AM-PM of 1.88 GHz PA were measured with AI and PI circuits separately and the results are plotted in Fig. 6. It is worthwhile to note that the AI degrades AM-PM linearity and shows limited ACLR improvement ($\sim$ 0.9 dB). On the other hand, the proposed PI recovers both AM-AM and AM-PM distortion as shown in Fig. 6(b) and improves ACLR by 4.2 dB. The performance of recently reported linear CMOS PAs is summarized in Table I [10], [11]. The measured efficiency and ACLR are among the best reported from CMOS PAs.

IV. CONCLUSION

A linearizer based on the envelope-dependent PI has been proposed for a CMOS stacked-FET PA. Together with the auxiliary AI and hybrid bias circuit, the 1.88 GHz W-CDMA CMOS PA meets the stringent linearity ($\rm ACLR < -39$ dBc) across the entire $P_{\rm out}$ range and shows a PAE higher than 44% at 28.7 dBm, which is comparable to that of a GaAs-based PA.

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