A 1W CMOS POWER AMPLIFIER FOR GSM-1800 WITH 55% PAE

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Abstract – **Until recently it was the common opinion that CMOS RF power amplifiers were not feasible for mobile handsets. This paper presents a CMOS power amplifier for the GSM-1800 standard, with only two external matching components and a few decoupling capacitors. The performance of the power amplifier is better than any other CMOS power amplifier reported and comparable to commercially available power amplifiers in other technologies.**

I. INTRODUCTION

This paper presents the results achieved in the design of a 1W CMOS power amplifier for GSM-1800. Due to the high yield in CMOS fabrication, higher integration is possible than e.g. in GaAs processes. A CMOS power amplifier therefore promises higher integration as well as lower cost. A typical power amplifier module for wireless communication consists of 2-3 dice and 15-20 passive components. The CMOS power amplifier component count can be reduced to one die and 2-5 passives plus decoupling. This reduction in component count leads to a significant reduction in power amplifier cost.

The power amplifier presented in this work is targeted towards the GSM-1800 standard, which has a transmit frequency for the handset of 1710 to 1785 MHz. The goal has been to design a power amplifier with a 1 W output power

II. DESIGN

The design of this power amplifier followed the design and simulation methodologies described in [1]. The design is the second iteration of a 1W CMOS power amplifier for GSM-1800, results of the first iteration have previously been presented [2]. This power amplifier shows higher integration and much better efficiency than previously presented.

The power amplifier is designed for a 0.35 μm bulk CMOS process with a substrate resistivity of 10-20 Ω-cm. The process has 5 metal layers and thin-oxide metal-metal capacitors. The thin-oxide metal-metal capacitors have a high density and therefore the die size (cost) of the complete power amplifier can be reduced.

The first choice to make was the number of stages in the power amplifier. In this case a two-stage methodology was chosen.

Then the class of operation was chosen for each of the stages. The input and output stages operates in class AB close to class B. There are a number of reasons to choose this mode of operation:

1. Class AB close to class B is relatively linear. This is not the case for class C and E amplifiers. The linearity is, however, not as good as class A.
2. The efficiency is relatively good, the theoretical maximum is 78.5%, compared with 50% for the class A amplifiers and Class C and E amplifiers have theoretical efficiencies of up to 100%.
3. The maximum drain voltage is twice the supply voltage, this is important due to the possible breakdown of the gate-oxide. Class C and E amplifiers easily exceed three times the supply voltage.
4. The power utilization factor (PUF), which is a measure of the gain compared to the output power, is reasonable compared with class A, and better than class C and E.
5. The required output load impedance is not too low to implement efficiently, which is often the case for class C.

Once the class of operation was chosen for the output stage it was possible to start the dimensioning of the output transistor. This dimensioning was an iterative process where the initial guess originated from the I-V characteristic of the power amplifier. From the I-V characteristic it was possible to find the voltage and current swings possible for a given load-line. From the voltage and current swings the maximum output power was then determined and a reasonable size of the transistor was found.

After an initial value is selected the more accurate RF behavior is found using load-pull simulations. The load-pull simulations are the simulation equivalent of the load-pull measurements.

The final schematic of the power amplifier is shown in Fig 1 where the components mentioned below can be located. The output transistor (M_2) was then chosen to be 8

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mm wide and with a length of 0.35 μm. The transistor is partitioned into 6 separate finger transistors, with 70 fingers each. The input stage also operates in class AB. The transistor of the input stage (M_1) is 1 mm wide and 0.35 μm long. The load-pull simulation results for the transistor is shown in Fig 1.

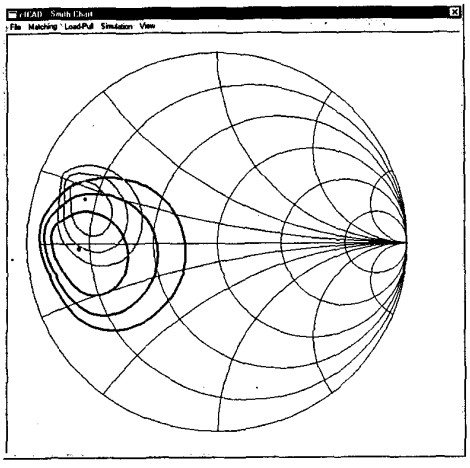

Fig 1. Load-pull simulation results.

The output matching network is placed primarily off-chip due to efficiency considerations. In order to have better harmonic termination, a capacitor (C_1) is placed on-chip, directly at the drain of the transistor, in parallel with the drain-source capacitor of the transistor. This capacitor terminates the harmonics at the drain, but at the same time it transforms the output impedance even lower, leaving a more difficult matching problem. The RF chokes (RFC_1, RFC_2) for the output stage as well as the input stage are relatively short microstrips, which can be implemented without increasing the overall PCB size. The output matching network consists of a bandpass T section (L_1, C_2, C_3), due to the high transformation factor from 4 Ω to 50 Ω. The choice of the T section gives a larger bandwidth than a single L section. The inductor in the T section consists of a contribution from the bondwires as well as from the microstrip. In the design of the network, the parasitics of the RFC microstrip were also included.

The input and interstage matching networks were both made with a fully integrated highpass LC matching section. This was chosen because it incorporates DC blocking and biasing at the same time as the impedance matching. The on-chip inductors are spiral inductors implemented in the top metal layer, while the capacitors are made thin-oxide metal-metal capacitors in the two lowest metal layers.

III. Simulation

Although it is possible for modern CAD tools to extract every parasitic component in a layout, it is not desirable to blindly use those parasitics. In general the slowdown of the simulator will be significant if all parasitics are included. During the design phase the designer will have to make some decisions, although complexity of the simulations will increase.

There are a large number of simulation models available for MOS transistors. The gate resistance is usually not included in the transistor models from the vendor, it is therefore important to take it into account.In this work the MOS9 model has been used.

Over the last couple of years a lot of research effort has been put into the characterization and modeling of the on-chip inductors. The capacitor can be modeled as the intended capacitor, with an additional capacitor from the bottom plate to the substrate. A parasitic series resistance is associated with each of the two plates.

One of the important things when trying to simulate a complete chip is to maintain the overview. If all interconnects were modeled regardless of their impact on the performance, the simulation speed would increase drastically and hence prevent simulation of the complete chip. It is therefore important to carefully select which interconnects should be modeled.

The bondwires are an important part of the entire RF design. The bondwires have inductance, capacitance and resistance associated with them. The PCB is modeled using microstrips. In some simulator e.g. APLAC, a number of microstrip components are implemented. The models from the vendor have been sufficient to get accurate simulations. Other issues like thermal modeling of the pulsed power amplifier have also been addressed.

In the design phase a number of different simulation methods are used. The most important method is harmonic balance simulations to get the steady-state response from the circuit. Another important simulation is the classical small-signal simulation to get initial design guesses and various small-signal parameters such as small-signal gain and stability. At last the transient simulations are also used to obtain information about time-domain phenomena such as stability, modulation and power ramping.

IV. Measurements

The CMOS power amplifier IC was been mounted directly on the PCB and wire bonded directly onto the PCB microstrips. To enable the wire bonding, the PCB was gold plated, the dielectric used in this work was standard FR4, with a relative dielectric constant of approximately 4.3 at 1.75 GHz.

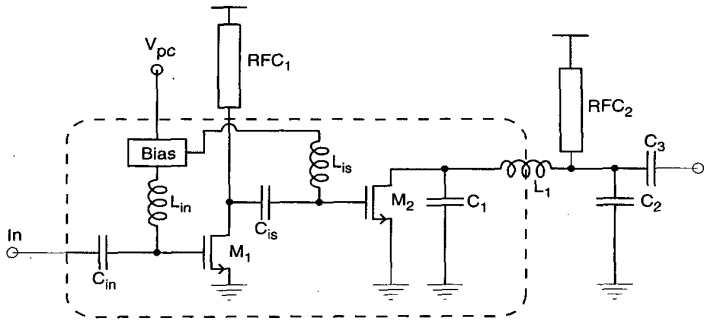

Fig 1. Simplified schematic of the power amplifier.

The passive components used on the PCB were 0402 SMD components. The SMA connectors were mounted horizontally on the edge of the PCB, in order to reduce the effects of the transition from SMA connector to PCB microstrip.

To get a realistic picture of the performance, the measurements were made in pulsed mode according to the GSM1800 specifications, this means a duty cycle of 12.5%.

The highest power added efficiency was 55% at 1750 MHz, with an output power of 30.4 dBm. The output power and efficiency measurements with the power amplifier biased for maximum power added efficiency vs. frequency are shown in Fig 2.

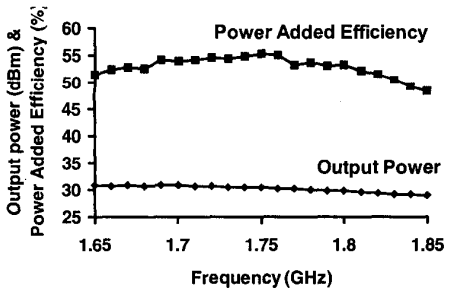

Fig 2. Output power and power added efficiency vs. frequency.

The power amplifier operates on a supply voltage from 1 V to 3.4 V. The output power and efficiency vs. supply voltage is shown in Fig 3. The output power is 20.8 dBm at 1V and 31.4 dBm at 3.4 V. The power added efficiency varies from 43% to 55% at 1V and 3.4V respectively.

A comparison of all the published CMOS power amplifier results is shown in Table I. As can be seen from the table no other CMOS power amplifier has been published

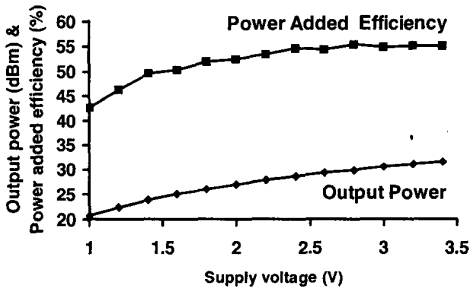

Fig 3. Measured output power and power added efficiency vs. supply voltage at 1750 MHz.

with output power or power added efficiency as high as the work presented here.

The simulations for the complete power amplifier including the PCB showed very good agreement between the simulated and measured results. The measured output power was predicted within a few tenths of a dB. The efficiency deviated less than 1%. The comparison between simulated and measured output power is shown in Fig 4.

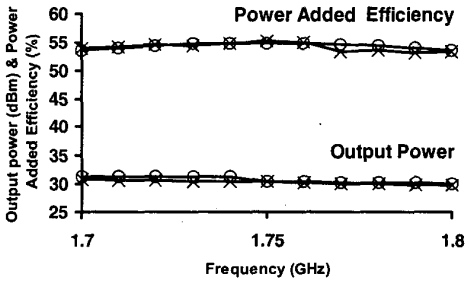

Fig 4. Comparison of simulated and measured data.

V. Conclusion

A CMOS power amplifier has been presented with a power added efficiency of 55% with an output power of 30.4 dBm at 1750 MHz. The power amplifier is designed for GSM-1800 with a supply voltage of 3V, although it performs very well from 1V to 3.4V. The die area including pads is 1.1 sq. mm. By accurately modeling bondwires, microstrips and SMD components the accuracy of the simulations was within a few tenths of a dB, compared to measured results.

The power amplifier consists of one die, two short microstrips and two matching components plus decoupling capacitors, compared to 3 dice and 15-20 passives plus decoupling capacitors for a typical GaAs power amplifier. The power amplifier has higher power added efficiency than any other CMOS power amplifier results published so far, whether they operate linearly [3][4][5][2] or nonlinearly [6][7][8][9].

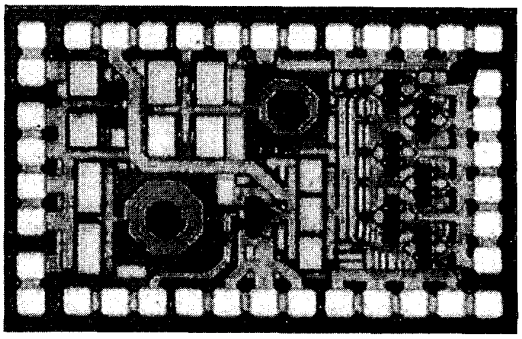

Fig 5. Die photograph.

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TABLE I

Comparison of CMOS power amplifiers.

	Frequency (MHz)	**P_{out} (dBm)**	**PAE (%)**	**Class**
T. Melly et. al. [6]	430	4.0	15	C
S.-J. Yoo et. al. [3]	433	13.0	30	AB
D. Su et. al. [7]	830	30.0	42	D
B. Ballweber et. al. [4]	900	19.3	23	AB
C. Yoo et. al. [8]	900	29.5	41	E
K.-C. Tsai et. al. [9]	1980	30.0	41	E
Asbeck et. al. [5]	1950	29.2	27	B
Fallesen et. al. [2]	1730	30.4	45	AB
This work	***1750***	***30.4***	***55***	***AB***