A 0.75–2.5-GHz All-Digital RF Transmitter With Integrated Class-E Power Amplifier for Spectrum Sharing Applications in 5G Radios

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***Abstract*— We propose a digitally intensive, reconfigurable RF transmitter with an integrated, tunable Class-E power amplifier (PA) which can be configured to operate from 0.75 to 2.5 GHz in discrete bands, while delivering an output power of 11.5 dBm up to 1.5 GHz and 6.5 dBm up to 2.5 GHz. Digital signal processing is exploited to suppress sampling spurs up to the harmonics of the carrier, thus eliminating the need for sharp RF filters. The proposed techniques make the transmitter adaptable to signals of different bandwidths and to different carrier frequencies with minimal overhead in power and area when compared to other digital transmitter designs. Digital predistortion is used to linearize the PA. The transmitter also includes clock correction circuitry for correcting duty cycle and quadrature errors. A generic design methodology is mathematically developed for a reconfigurable Class-E PA with a fixed series inductor. This transmitter scales well with technology and can be potentially used for spectrum sharing (SS) applications in fifth generation (5G) radios. Implemented in a 130-nm CMOS technology, the proposed transmitter occupies an area of 1 mm^2. A maximum output power of 13.7 dBm with a maximum efficiency of 27% is obtained at 1 GHz.**

***Index Terms*— Class-E power amplifier (PA), cognitive radio (CR) transmitter, digital filtering, duty cycle correction, fifth generation (5G) spectrum sharing (SS), frequency reconfigurable Class-E PA, on-chip tunable network, PAs, quadrature correction, reconfigurable TX, software-defined radio (SDR)/CR, SDR transmitter, wideband transmitter.**

I. Introduction

RECENTLY, enhanced cognitive radio networks (E-CRNs) based on spectrum sharing (SS) and spectrum aggregation (SA) have been proposed for fifth generation (5G) wireless networks [1]. Cognitive radios (CRs) enable effective utilization of radio frequency bands that have been opened up for communication purposes [2]. Software-defined radios (SDRs) and CRs are the future of wireless communication [3]. By definition, an SDR is a radio that can be easily reconfigured to operate at different frequencies, with different bandwidths, with different modulation schemes by software reprogramming [4]. Cellular mobile transceivers need to cover spectrum bands which support legacy modes such as 2G and 3G, along with the recent 4G and 5G standards, that utilize blocks of spectrum extending from 600 MHz to 6 GHz with a signal bandwidth of up to 100 MHz. Conventional transceiver architectures support multiple transceiver chains, each of which is tuned to a smaller range of frequencies, leading to a large chip area.

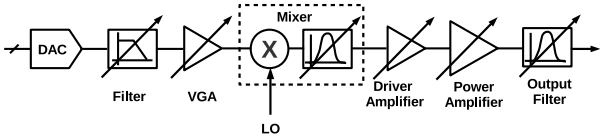

Fig. 1. Traditional transmitter architecture adapted for wideband SS radios.

A single transceiver solution could be envisioned as a cost-effective replacement for the current multitransceiver approach [5]. This, however, requires a reduction in the number of transmitter and receiver chains, which in itself is a considerable challenge. It is therefore very attractive to explore circuit techniques that enable area savings. In particular, power amplifiers (PAs) and driver amplifiers do not yield easily to flexible operation. Maintaining good efficiency while transmitting a sufficient amount of RF power linearly across a wide range of frequencies is a significant challenge, especially when meeting the stringent out-of-band emission specifications imposed by modern communications standards.

To adapt a traditional transmitter for an SDR, several modifications are required as shown in Fig. 1. The low-pass filter following the digital-to-analog converter (DAC) needs to be tunable to handle signals with different bandwidth requirements. The mixer, driver amplifiers, and the PA need to be made tunable for different carrier frequencies simultaneously to optimize output power and efficiency. Due to interactions between the multiple analog stages, such tuning comes with a multitude of challenges. In the literature, several analog designs have been proposed, employing multiple transmitter chains to cover a wide frequency range. A filter-less transmitter for SDR from dc to 2.4 GHz is presented in [6], where a polyphase multipath technique is used to remove harmonics

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and some intermodulation components, thus obviating an output filter. In [7], an analog transmitter with three parallel mixers and drivers to cover three frequency bands between 100 MHz and 2.5 GHz is presented. A SAW-less transmitter design is proposed in [8] and [9], where an analog architecture is used. The output stage is a Class-AB prepower amplifier with two on-chip baluns. In [10], a wideband analog front-end for universal radio applications is presented, which operates up to 9 GHz. A Darlington prepower amplifier is used to produce an approximate output power level of 4 dBm. Inductive degeneration is used to ensure wideband operation. Another analog implementation in [11] covers a wide frequency range of 50 MHz–6 GHz by appropriately mixing two LOs and uses on-chip transmission lines for the prepower amplifier. In [12], a 4-band solution is attempted to cover a frequency range of 100 MHz–6 GHz. In all these solutions, the output power is limited and in many cases, the efficiency is also poor.

A digitally intense RF front-end design scales well with technology as opposed to a fully analog design. Digital RF transmitters have the added advantage of being well-integrated with other non-RF circuits in systems-on-chip (SoCs). The use of digital-intensive architectures mandates the use of switching PAs in the final stage. In order to transmit signals with varying envelopes, there are four major techniques presented in the literature [13], [14]. The polar transmitter is a popular architecture for SDR. However, it carries with it the burden of converting the coordinates to the polar form, using a coordinate rotation digital computer (CORDIC). This introduces additional complexity, power, and area penalties. Another major drawback in polar transmitters is the bandwidth expansion that occurs during coordinate rotation. This demands that the circuits have much higher bandwidths than the actual signal itself. Polar transmitters for SDR, that operate between 0.8–2 GHz [15], and between 0.9–1.9 GHz [16] have been developed with off-chip output matching. A dual-band polar transmitter for 2 and 5 GHz with two PAs is designed in [17]. All the above transmitters employ RF DAC PA for amplitude modulation. The work in [18] and [19] use a supply modulator to provide amplitude modulation to a switching PA. Matching two heterogenous paths across a wide range of carrier frequencies is a challenge in polar transmitters. The outphasing architecture [5] combines two switching PAs with phase modulation on those signals. A major challenge in outphasing PAs is the design of the output combiner, to enable it to work over a wide range of carrier frequencies. They also have a huge digital overhead for converting the signal to two outphasing vectors. An all-digital outphasing modulator in CMOS is presented in [5] that operates between 1 and 2 GHz. The PA and combiner are described in [20] and [21]. The output matching and combining networks are implemented off-chip. A 2.6-GHz outphasing PA using a delay-based phase modulator is detailed in [22]. Reconfigurable load impedance matching has recently been reported for other classes of PA [23]. A triphasing PA is presented in [24]. Another emerging technique is to use a delta-sigma modulator [25] and drive a switching PA. This technique requires a sharp bandpass filter at the output which needs to be tunable across the entire frequency range, which is difficult to implement. Also, using higher oversampling ratios is severely limited by technology. There are also some combinations of these techniques such as [26].

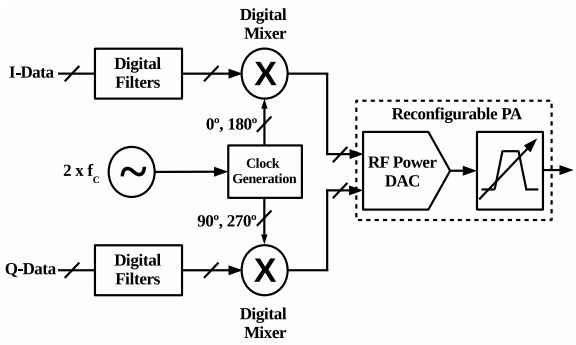


Fig. 2. Architecture of the proposed transmitter.

Digital IQ transmitters [27]–[33] are promising for SDR applications. I and Q digital signals are up-sampled, filtered, mixed digitally, and combined with an RF-DAC. An RF power DAC (RFDAC) with off-chip PA is used in [27]. The PA is integrated into the DAC in [29] and [32]. An IQ cell-sharing architecture with off-chip matching network is described in [30]. Another direct-digital RF modulator with wideband off-chip matching is shown in [31]. A digital IQ transmitter with DSP-based Rx band noise programming is described in [33]. The proposed transmitter is shown in Fig. 2 and follows the digital IQ architecture. This work focuses on two major challenges in the design of digital IQ transmitters. The first one is the problem of sampling spurs, which is critical in transmitters operating over a wide frequency range. This article proposes a power- and area-efficient technique to remove all sampling spurs up to the harmonics of the carrier frequency. The second challenge is the design of a single PA which can be tuned to large range of carrier frequencies, approaching two octaves. A Class-E switching PA is chosen in this design and an algorithm is presented with mathematical foundations derived from prior art. A digitally intense transmitter, which includes an on-chip Class-E PA with an integrated tunable matching network is designed. The design consists of a single transmitter chain with an integrated PA that covers the frequency range of 750 MHz–2.5 GHz. Section II of this article explains the overall architecture of the transmitter. The digital signal processing is explained in Section III. The digital frequency upconversion process is described in Section IV. The theory and methodology for designing reconfigurable Class-E PAs with a single series inductor is developed in Section V. The implementation issues are discussed in Section V-D, and the design of the RFDAC is described in Section VI. The measured results are presented in Section VII.

II. Transmitter Architecture

A detailed diagram of the proposed transmitter architecture is shown in Fig. 3. Digital I and Q data streams are sampled and filtered digitally. A two-step up-sampling DSP is proposed in this article to eliminate the sampling spurs, which is a major

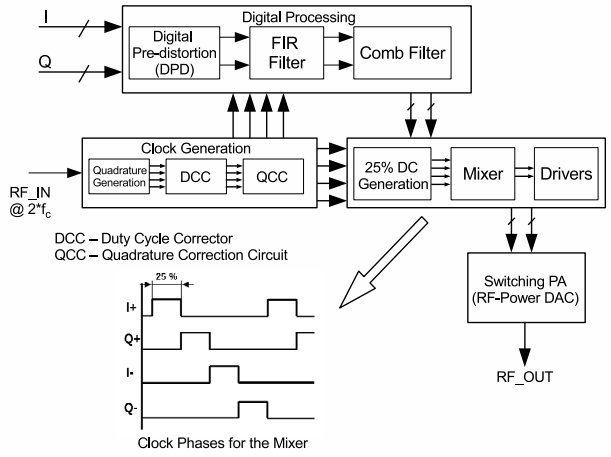


Fig. 3. Detailed system diagram of the proposed transmitter.

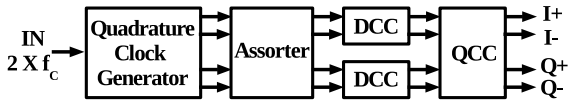


Fig. 4. Quadrature clock generation and correction scheme. DCC: duty cycle corrector. QCC: quadrature correction circuit.

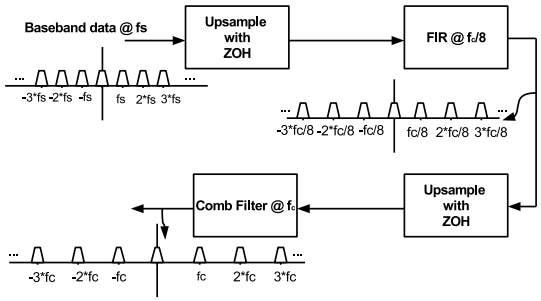


Fig. 5. Digital processing of the input signal for spur suppression.

problem in most digital transmitters. The proposed scheme ensures that all the sampling spurs are eliminated up to the harmonics of the carrier frequency, while having a lower power and area overhead. The digital processing block in Fig. 3 consists of a digital predistortion (DPD) block followed by an FIR filter and a comb filter.

The clock is derived from a continuous wave (CW) source at two times the carrier frequency. Four phase clocks are generated by the clock generation block (see Fig. 4). The phases thus generated are indeterminate and hence an assorter is used to arrange the phases to I and Q clocks. These clock signals can have impairments in duty cycle and quadrature separation across the frequency range due to mismatch, process corners, and voltage and temperature variation. For a wideband transmitter such as this, these impairments need continuous correction. A pair of wideband duty cycle correction circuits correct the duty-cycle to 50% as explained in [34]. The duty cycle corrected clocks are fed to a quadrature correction circuit [35], which continuously corrects for quadrature errors. The 25% duty cycle clocks are derived from these corrected phases.

The I and Q data are mixed digitally with the four phase clocks of 25% duty cycle clock and are buffered to drive the digital PA. The buffers are sized such that they are able to drive the largest transistor switch in the PA. The PA is essentially an RFDAC. The I and Q paths are combined in the output stage. The switches of the PA are binary weighted, such that the switch resistance is a function of the digital inputs. The output network of the PA is tuned to different frequencies. The output network down-converts the standard 50-Ω impedance to a lower complex impedance which is required by the Class-E PA for wave-shaping to ensure zero-voltage switching. A larger number of elements in the output network leads to increased loss and reduced efficiency. Hence the output network is implemented with a single fixed series inductor and two capacitor banks.

The advantage of this architecture is that only the final stage needs to be tuned to different carrier frequencies. The other blocks are either unaffected by the carrier frequency or are capable of working across the wide frequency range.

III. Digital Signal Processing for Spur Suppression

Sampled signals have their spectra replicated at all the harmonics of the sampling frequency. When these digital signals are up-converted and transmitted, spurs occur on both sides of the carrier frequency with a spacing equal to that of the sampling frequency. For a wideband system such as this, narrowband off-chip filters cannot be used. Having a tunable, high-Q on-chip filter at the output of the PA is also not feasible. Hence a digital baseband technique is needed to remove these spurs. Many DSP-based solutions have been proposed to eliminate sampling spurs. All-digital transmitters as in [32] and polar transmitters such as [19], [15], and [18], describe DSP techniques where the spurs are eliminated up to a fraction of the carrier frequency. A second-order hold interpolator is used in [31] to remove the sampling spurs up to the carrier frequency which is chosen to be four times the baseband sampling frequency. A configurable sampling rate converter in [36] uses a combination of cubic Lagrange filters with cascaded integrator-comb (CIC) filters to remove sampling spurs up to half the carrier frequency above 1.4 GHz and up to the carrier frequency below 1.4 GHz. Since the range of operation of the proposed transmitter is close to two octaves, and the Q of the output matching network is low, there is a need to efficiently remove all sampling spurs up to the carrier frequency. In this transmitter, the sampling frequency is taken to be twice the Nyquist frequency and a signal bandwidth of up to 20 MHz is supported. The carrier frequency and the sampling frequency are not in any particular relationship. We propose a novel arrangement of well-known filtering techniques to remove the spurs up to the carrier frequency. We address this problem with a two-step solution.

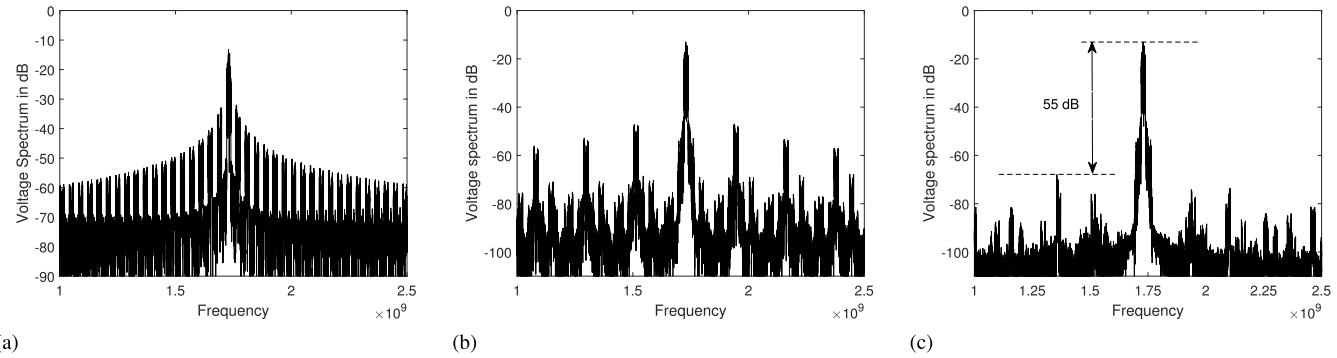


Fig. 6. Simulated output spectrum of an LTE 20 MHz, 64-QAM signal at 1730 MHz. (a) Without DSP. (b) Up-sampled to $f_c/8$ with only FIR filtering. (c) Up-sampled to f_c with FIR and comb filtering.

A. First Level Filtering—The FIR Filter

As shown in Fig. 5, the baseband data is up-sampled to one-eighth of the carrier frequency ($f_c/8$) with a zero-order hold. For an up-sampling factor of N, $N-1$ copies of the current sample are inserted between the current sample and the next sample. This is implemented by resampling the input signals at $f_c/8$. A reconfigurable low-pass FIR filter operating at $f_c/8$ filters this signal. The corner frequency of the low-pass FIR filter is determined based on the bandwidth of the signal (f_b) to be transmitted and the carrier frequency. The normalized minimum passband frequency is $f_b/f_c/8$ and the stopband frequency is $f_s/f_c/8$. The system can thus process signals with different bandwidths at any given carrier frequency. The filtered signal at this point is cleared of all spurs in the interval of $f_c/8$. The number of taps required varies with different bandwidths and carrier frequencies from 10 to 45 taps. The processor is expected to have an 18-bit resolution for the computation. The data is finally rounded off to 9 bits.

B. Second Level Filtering—The Comb Filter

This signal, if transmitted as such at f_c, has spurs at an interval of $f_c/8$ as shown in Fig. 6(b). To suppress these spurs, a tunable high-Q filter is required at the output of the PA, which is not practical. Hence the need for a second level of digital filtering. The data is up-sampled again by a factor of 8 with a zero-order hold. Now the sampling frequency is the same as the carrier frequency (f_c). Given that the sampling frequency of the previous stage is at a constant ratio with the carrier frequency, a comb filter would be an ideal choice to remove the sampling spurs at multiples of $f_c/8$ [37]. A 7-tap comb-filter running at f_c notches out these spurs at $f_c/8$ interval. For high frequency operation, this is very efficient in terms of power and area. Since the FIR runs at $f_c/8$, the comb filter does not need to be reconfigured. The output is now clean up to f_c on both sides of the carrier frequency, which means that the spurs now occur only at the harmonics of the carrier frequency (see Fig. 5). Based on the LTE bands and bandwidths in use, the worst case sinc attenuation is calculated to be -0.016 dB for an LTE 20-MHz signal at 750 MHz, which is acceptable.

The simulation results for an LTE 20 MHz, 64 QAM signal at 1730 MHz without DSP is shown in Fig. 6(a). After up-sampling to $f_c/8$ and FIR filtering, the resulting spectrum is shown in Fig. 6(b). The final output after up-sampling to f_c with comb filtering is shown in Fig. 6. The largest spur is 55 dB below the carrier. This is close to the quantization noise floor of -55.94 dBc for a 9-bit resolution. The advantage of this technique is that the specifications of the reconfigurable output filter are relaxed. This is important given that the output filter also plays the role of an impedance transformation network to down-convert the impedance from 50 Ω to the optimal impedance required by the PA at the output. Another significant advantage is that this technique can be used for processing signals with any type of modulation with varying bandwidths while transmitting at any carrier frequency. FIR reconfigurability is much simpler when compared to the complexity of reconfiguring traditional transmitters to handle such varying signals. The power consumption of the high speed digital blocks is higher while implementing it in an older technology. However, this technique scales very well with technology and the power numbers become significantly lower at more advanced technology nodes.

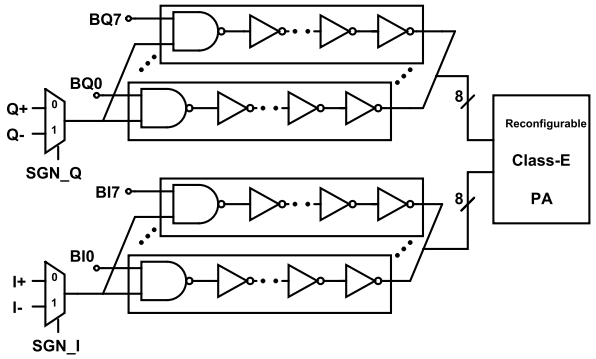


Fig. 7. Schematic of the mixer and drivers.

IV. Frequency Upconversion

After the data stream has been up-sampled and the spectrum has been cleaned up using the filtering techniques described above, the data is now up-converted in frequency by mixing it with the clock signals generated by the clock generation block, shown in Fig. 3. Digital mixing is performed with NAND gates

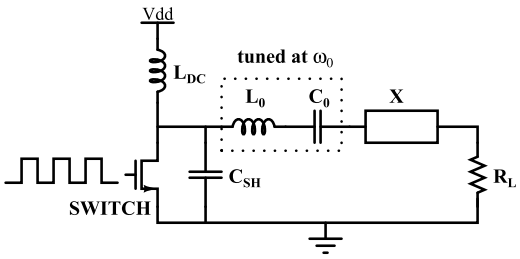


Fig. 8. Traditional Class-E PA schematic.

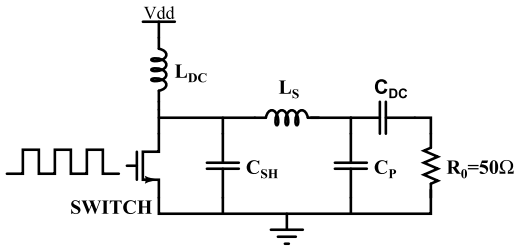


Fig. 9. Implementation of a Class-E PA showing the impedance transformation network.

as shown in Fig. 7, using 25% duty cycle clock phases generated for the mixer. The output of the quadrature correction block has clock signals which are in quadrature having a duty cycle of 50%. By appropriate logical combinations, the four clock phases as shown in Fig. 3, each with 25% duty cycle are generated. A multiplexer selects the clock or its complement based on the sign in both I and Q paths. 9 bits (8 bits of amplitude resolution and 1 sign bit) of resolution are used to encode the I and Q data to be transmitted. The output of the NAND mixers are buffered to drive the switching PA (Class-E), described next.

V. Wideband Reconfigurable PA

A. Class-E PA Design Constraints—The Output Network

Classes D, E, and F are the most commonly used switching PAs. Class-F PAs do not yeild easily to tunability since all the harmonic terminations need to be tuned simultaneously. Class-E PAs offer higher efficiency than Class-D due to the drain waveshaping. Class-E is inherently a narrowband PA configuration. A typical class-E PA is shown in Fig. 8. The switch is implemented as an NMOS transistor. The output network consists of a tuned L-C network and load resistance (R_L) with an excess reactance jX. To synthesize jX and R_L, a circuit as shown [38] in Fig. 9 is implemented. An L-match network consisting of C_P and L_S transforms the standard load impedance of 50 Ω to a suitable R_L. $C_{\rm dc}$ is used to block the dc and is implemented as an off-chip element which is large enough that it does not affect the impedance at the frequencies of interest. $C_{\rm SH}$ helps with the wave shaping to ensure zero-voltage switching. The parasitic capacitance of the MOS switches is absorbed into $C_{\rm SH}$. The impedance presented by the L-match network (Z_L) is given by

$$Z_L = \frac{R_0}{1+(\omega R_0 C_P)^2} + j\left(\omega L_S - \frac{\omega R_0^2 C_P}{1+(\omega R_0 C_P)^2}\right). \quad (1)$$

TABLE I

Table of Component Values Calculated for Operation From 0.75 to 2.5 GHz Based on Traditional Class-E Equations

P_{OUT} = 18 dBm R_L = 18Ω V_{DD} = 1.5 V

Frequency	C_P	L_S	C_{SH}
750 MHz	5.08 pF	10.25 nH	1.89 pF
800 MHz	4.76 pF	9.6 nH	1.77 pF
1 GHz	3.8 pF	7.68 nH	1.42 pF
1.5 GHz	2.54 pF	5.12 nH	947 fF
2 GHz	1.9 pF	3.84 nH	710 fF
2.5 GHz	1.52 pF	3.07 nH	568 fF

Expressing $Z_L = R_L + jX$

$$R_L = \frac{R_0}{1+(\omega R_0 C_P)^2} \quad (2)$$

$$jX = j\left(\omega L_S - \frac{\omega R_0^2 C_P}{1+(\omega R_0 C_P)^2}\right) \quad (3)$$

the component values are calculated as follows:

$$C_P = \frac{1}{\omega R_0}\sqrt{\frac{R_0}{R_L} - 1} \quad (4)$$

$$L_S = \frac{1}{\omega}\left(X + \frac{\omega R_0^2 C_P}{1+(\omega R_0 C_P)^2}\right). \quad (5)$$

For transmitting at a fixed frequency, well-defined equations have been derived and experimentally verified in [39] and [40]. The optimal Class-E output network component values at different frequencies between 0.75 and 2.5 GHz are calculated and tabulated in Table I. The classical Class-E assumptions of a large dc feed inductance (RF-Choke) and an infinite output loaded Q (Q_L) are used. An RF choke can be treated as a constant current source. An infinite Q_L is assumed so that the current through the output load is taken to be purely sinusoidal.

To enable a reconfigurable Class-E PA to operate from 0.75 to 2.5 GHz, the output network components need to be tuned appropriately. C_P and $C_{\rm SH}$ can be made tunable by implementing capacitor banks and using digital bits to enable or disable smaller unit capacitors. However, making the inductor (L_S) tunable is not easily accomplished. In [41], a transformer based tuning arrangement is used. However, the amount of change in the inductance is not large enough to accommodate the range specified in Table I. A similar technique in [42] uses multiple taps on the secondary of a transformer to vary the inductance of the series inductor which is formed by the primary of the transformer. More complex networks with multiple inductors can be explored. However, the inductor losses in the series path of the PA reduce its efficiency.

It is clear that using a classical design approach to design the component values and tuning them is not a viable solution for a wideband transmitter such as this. The main requirement is that the series inductor (L_S) remains constant and nontunable across the frequency range. This article focuses on developing

TABLE II
DESIGN SET FOR $(0.6 < q < 1)$ [43]

$K_L(q) = 44.93q^2 - 94.32q + 52.46$
$K_C(q) = 0.426q^2 - 0.379q + 0.3$
$K_P(q) = 0.74q^2 - 0.6q + 0.76$
$K_X(q) = -0.73q^2 + 0.411q + 1.03$

TABLE III
DESIGN SET FOR $(1 < q < 1.65)$ [43]

$K_L(q) = 8.085q^2 - 24.53q + 19.23$
$K_C(q) = -6.97q^3 + 25.93q^2 - 31.071q + 12.48$
$K_P(q) = -11.90q^3 + 42.753q^2 - 49.63q + 19.70$
$K_X(q) = -2.9q^3 + 8.8q^2 - 10.2q + 5.02$

a novel design technique using which a narrowband Class-E amplifier can be made reconfigurable, while retaining a single, fixed series inductor. The technique exploits the use of smaller dc feed inductance ($L_{\rm dc}$) instead of the RF choke. The capacitors C_P and $C_{\rm SH}$ are tuned to provide the required impedances for wave-shaping at the drain node of the PA across the frequency range, while using a single, fixed series inductor.

B. Class-E Parametric Design Space Approach

The classical equations assume that the RF choke is an inductor whose value is large enough to be considered as infinite. Inductors of the order of a few nanohenries imply that these equations do not hold good. In [43], a parametric set of design equations have been developed for Class-E PAs. These equations include the effects of a finite dc feed inductance and a finite Q_L. The equation sets are parametric with a variable q. Hence instead of having a unique set of component values for given specifications, a set of solutions is now possible. We use these equations to develop a design methodology for reconfigurable Class-E PAs.

The variables used in designing Class-E PAs are $\{P_{OUT}, V_{\rm DD}, L_{\rm dc}, R_L, X, C_{\rm SH}\}$. In the current implementation shown in Fig. 9, the set now becomes $\{P_{OUT}, V_{\rm DD}, L_{\rm dc}, C_P, L_S, C_{\rm SH}\}$. Following the analysis in [43], let $K = \{K_L, K_C, K_P, K_X\}$, where

$$K_L = \frac{\omega L_{\rm dc}}{R_L} \tag{6}$$

$$K_C = \omega C_{\rm SH} R_L \tag{7}$$

$$K_P = \frac{P_{OUT} R_L}{V_{\rm DD}^2} \tag{8}$$

$$K_X = \frac{X}{R_L}. \tag{9}$$

For classical Class-E PA design as in [39], $K = \{\infty, 0.1836, 0.5768, 1.152\}$. The polynomial-fit equations for K are presented in Tables II and III for different ranges of q [43]. Of the design variables used in designing a wideband reconfigurable Class-E PA, some are constant and some are variable. L_S, $L_{\rm dc}$, and $V_{\rm DD}$ are constant across the frequency range. P_{OUT} is expected to be constant across the frequency range, but there is some tolerance. $\{R_L, X, C_{\rm SH}\}$ are variable. This corresponds to $\{C_P, C_{\rm SH}\}$ being variable in the implementation.

The requirement that a single fixed inductor be used for operation over the entire frequency range forces certain constraints. The required excess reactance (jX) in addition to R_L is to be synthesized from the L-match network for all frequencies ($X = {\rm Im}\{Z_L\}$). Using (3) and taking R_0 to be 50 Ω, we get

$$X = R_L\left(\frac{\omega L_S}{50} - \sqrt{\frac{50}{R_L} - 1}\right). \tag{10}$$

A subspace of solutions is identified for the PA, where (10) is satisfied at different frequencies. Then we impose the condition for uniform output power (with a certain tolerance) across the frequency range. Thus, a solution set is obtained for a Class-E PA which can be reconfigured by merely tuning C_P and $C_{\rm SH}$ to make it operational across a wide frequency range.

C. Design Methodology

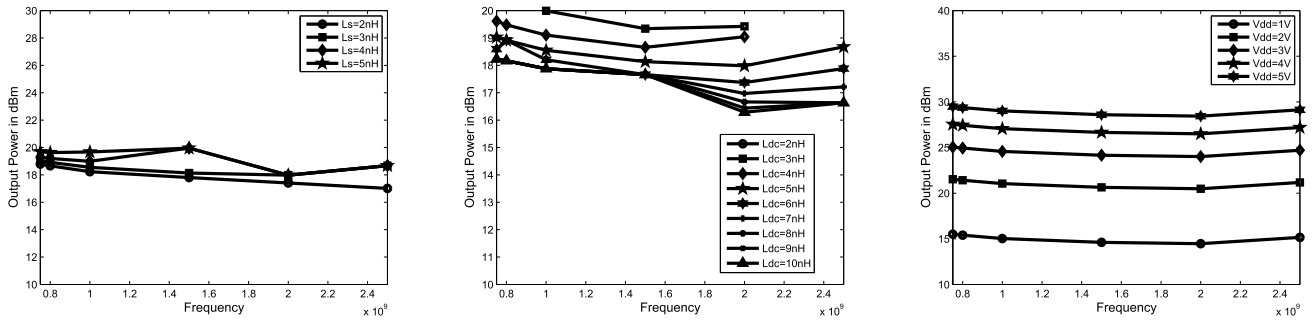
The following procedure has been developed to establish a design methodology for wideband reconfigurable Class-E PAs. It involves a certain degree of iteration to arrive at the best set of component values to meet the needs of the application.

1) Fix $L_{\rm dc}$ to have a value that is feasible for implementation.
2) Tables II and III offer two sets of equations based on the value of q. The choice is made after a preliminary investigation as to which range of q provides a feasible set of solutions which meet specifications such as frequency range of operation, minimum output power required, etc.
3) For every frequency point and for every q, calculate $R_L, X, C_{\rm SH}, C_P, L_S$ using (4), (6), (7), and (9). The output power is estimated by using (8).
4) Eliminate solutions which contain invalid values of L_S generated in step 3, such as negative values or complex values. Pick a value of L_S which is found in the solutions at all frequencies. Usually there is a range of inductances which are valid over the frequency band of interest. Different values of L_S correspond to different output power numbers, and Q_L. Based on these specifications a suitable L_S is selected.
5) In step 4, for the same value of L_S there can be multiple values of q which result in different output power numbers. Of all the solutions in step 4, choose the solutions which provide uniform power numbers across the frequency range of interest.
6) Steps 2–5 can be repeated with different values of $L_{\rm dc}$.

Thus a reconfigurable PA can be designed with different drain impedances for different frequencies, which sustain the zero-voltage switching criteria of a Class-E.

D. Analysis of the Impact of Design Variables

L_S, $L_{\rm dc}$, and $V_{\rm DD}$ are variables which can be set with a certain degree of flexibility. Fig. 10(a) shows the variation of



(a) (b) (c)

Fig. 10. Variation of output power versus frequency for different values of (a) L_S ($L_{\rm dc} = 5$ nH and $V_{\rm DD} = 1.5$ V), (b) $L_{\rm dc}$ ($L_S = 3$ nH and $V_{\rm DD} = 1.5$ V), and (c) $V_{\rm DD}$ ($L_{\rm dc} = 5$ nH and $L_S = 3$ nH).

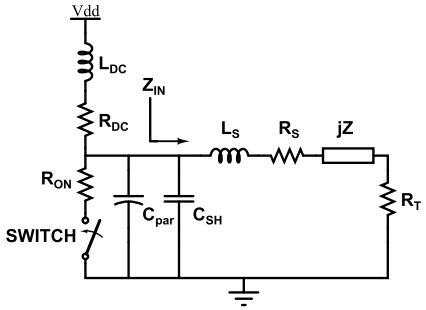


Fig. 11. Parasitics in the implementation of a CMOS PA.

output power across the frequency range for different values of the series inductor L_S. It is observed that the output power does not vary much with L_S. Fig. 10(b) plots the variation of the output power across the frequency range for different values of the dc feed inductor, $L_{\rm dc}$. An interesting observation is that the solution set does not exist across the entire frequency range for all values of the inductor. For $L_{\rm dc} = 2$, 3, and 4 nH, the solution is nonexistent for some frequencies. In general, it can be stated that the frequency range over which the solution exists for the proposed methodology, changes with the actual inductor values. Fig. 10 shows the variation of the output power across the frequency range for different supply voltages. The output power is proportional to $V_{\rm DD}^2$.

E. Finite Quality Factor of Inductors

For integrated CMOS PAs, one of the major challenges is the low quality factor of on-chip spiral inductors. In Fig. 11 the different inductor parasitics are shown. $R_{\rm dc}$ and R_S are the parasitic resistances of the inductors $L_{\rm dc}$ and L_S, respectively. $R_T + jZ$ is the transformed impedance from the standard 50-Ω load by the shunt capacitance C_P as shown in Fig. 9. The total resistance seen by the switching transistor is $R_T + R_S$. R_S forms a resistive divider with R_T, thus reducing the effective output power delivered to the load while reducing the efficiency. Fig. 12(c) shows the variation of the series resistance with frequency. This frequency-dependent series resistance also needs to be included in the calculations in order to estimate the power delivered to the load.

F. Variation of L and Q of On-Chip Inductors With Frequency

The series inductor of the output matching network (L_S) is implemented as an on-chip spiral inductor. The characteristics of the inductor vary across the frequency range of interest. Fig. 12(a) shows the inductance variation with frequency and Fig. 12(b) shows the variation of its quality factor with frequency. This variation of inductance has to be taken into account while using the design methodology described earlier.

G. Impact of Package Parasitics

The output network assumes a 50-Ω resistive load. The interface to the chip through the bond wires and the pads changes the impedance to some extent. By estimating their impact before-hand, the effects can be absorbed in the design, to a first order. A typical package model [44] is shown in Fig. 13. $C_{\rm PAD}$ refers to the pad capacitance on-chip. L_1 models the bondwire inductance and L_2 models the inductance of the lead. C_1 and C_2 model the capacitance in the lead of the package.

H. Refined Design Methodology

The issues described above require the following modifications to the design procedure established in Section V-C.

1) For a given frequency range, determine a suitable $L_{\rm dc}$ and L_S using the methodology in Section V-C.
2) Implement $L_{\rm dc}$ and L_S in the technology of choice and determine the variation of inductance and quality factor across the frequency range. Use the realistic values for $L_{\rm dc}$ and L_S and rerun the design process.
3) Use the package model relevant to the design implementation and model the impedance transformation produced by the package parasitics. Rerun the design methodology with the new impedance rather than $R_0 = 50\ \Omega$.
4) Adjust R_L across the frequency range due to the variation of R_S with frequency. The new load impedance is

$$R'_L(\omega) = \frac{\omega L_{\rm dc}}{K_L} + R_S(\omega) \tag{11}$$

and use $R'_L(\omega)$ to compute the other component values.

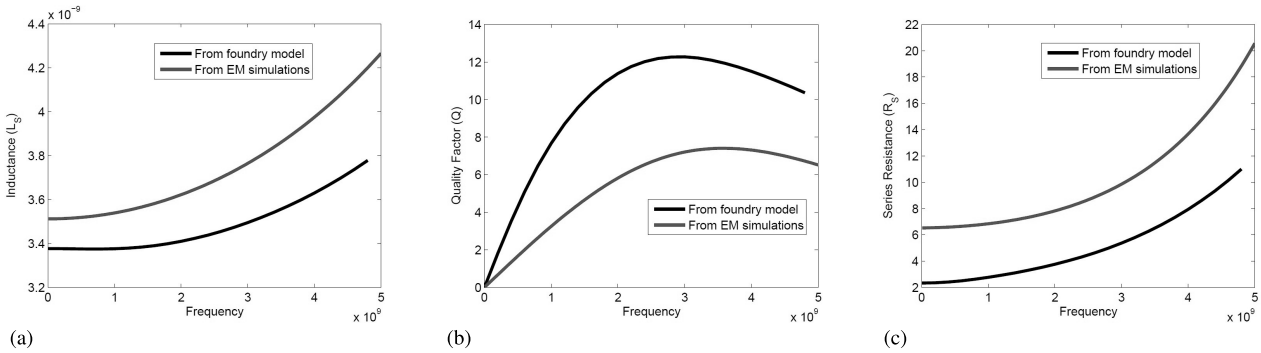


Fig. 12. Variation of inductance and its quality factor versus frequency for a 3.5-nH spiral inductor implemented using a 130-nm CMOS technology. (a) Inductance versus frequency. (b) Quality factor versus frequency. (c) Series resistance versus frequency.

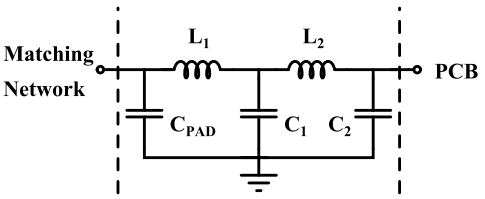


Fig. 13. Typical package model.

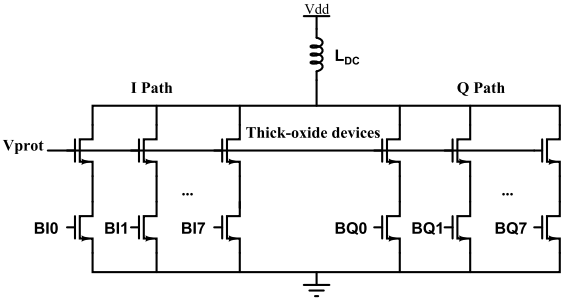


Fig. 14. Integrated DAC switches in PA using a combination of regular and thick oxide devices.

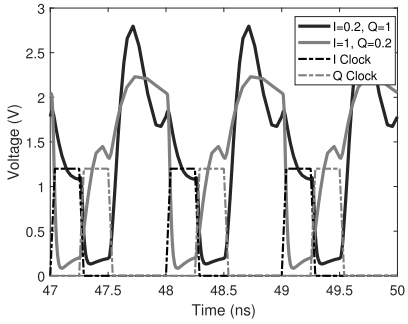


Fig. 15. Drain waveforms for I = 1, Q = 0.2 and I = 0.2, Q = 1. The drain asymmetric behavior arises due to the memory effects.

VI. Reconfigurable Power DAC

The incoming data is modulated by the clock at the carrier frequency. By having four phases of 25% duty cycle quadrature clocks, a vector in any of the four quadrants can be produced by the appropriate selection of clock phases. The amplitude modulation along the *I*- and the *Q*- axes are produced, respectively, by the DACs for each of the paths. Finally the two paths are combined by current addition. The *I* path and the *Q* path are each ON for 25% of the time period. Together they are ON for 50% of the time period of the carrier clock at peak power. The duty cycle drops to 25% when either *I* or *Q* code is zero. At other times, the switch is ON for 50% of the time period, but with different ON-resistances, according to the input code.

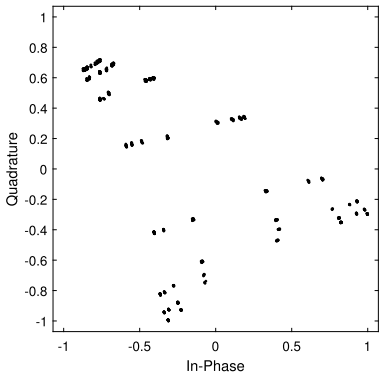


Fig. 16. Simulated constellation of 40-MHz 64-QAM signal transmitted at 1730 MHz without DPD.

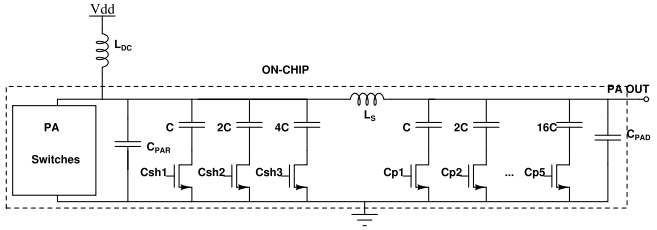


Fig. 17. Schematic of the reconfigurable matching network with the PA switches.

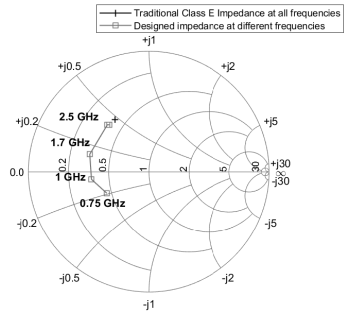


Fig. 18. Traditional Class-E impedance and designed impedance overlaid in smith chart for the frequency range of 0.75–2.5 GHz.

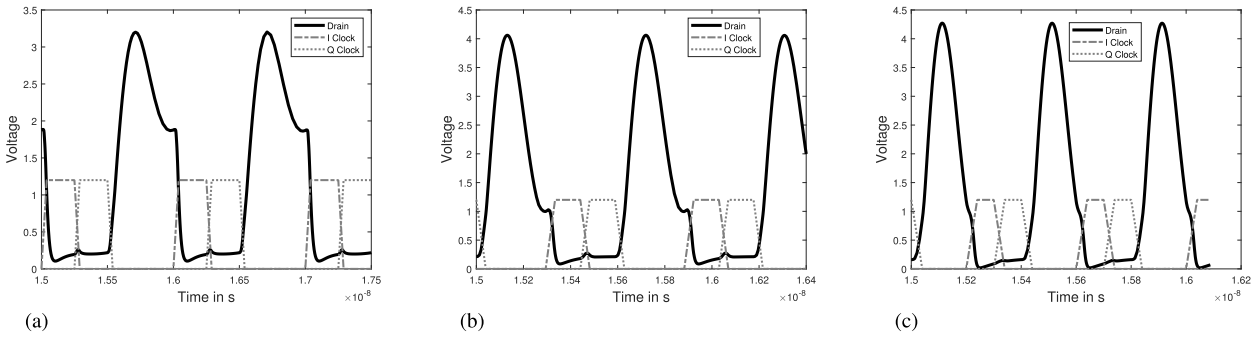


Fig. 19. Simulated drain and gate waveforms at (a) 1, (b) 1.7, and (c) 2.5 GHz.

The DAC operation can be understood as follows: The R_{on} of the PA switch is variable with the input code. As the R_{on} changes, the output power varies. In a strict sense, this violates the assumption of a traditional Class-E PA, where a negligible switch resistance is assumed. This violation however leads to a Class-AB type efficiency profile. The I path is on for 25% of the time period and the Q for another 25% of the time period. During each of these ON times, the R_{on} is a function of the amplitude code in the respective axes, and the output follows the conventional cartesian equation of

$$v_{\text{out}}(t) = A_I(t) \times \cos(\omega t) + jA_Q(t) \times \sin(\omega t). \quad (12)$$

A. Digital-to-RF Conversion

The digital-to-RF conversion is implemented by binary-weighted switches of the PA as shown in Fig. 14. The effective width of the PA's switching transistor is modified according to the incoming data, producing an RF output which is proportional to the digital code. For a Class-E PA, the drain voltage can swing up to $3.6 \times V_{\text{DD}}$. Hence a thick-oxide transistor, which is also binary weighted, is placed in cascode with the switching transistors for protection. The gates of these transistors are connected to V_{prot} which is kept at a voltage such that $V_{\text{prot}} - V_{\text{thT}} < V_{\text{drain\_max}}$ where V_{thT} is the threshold voltage of the thick oxide transistor and $V_{\text{drain\_max}}$ is the maximum allowable drain voltage of the switching transistor for safe operation. Digital power control of the transmitter is possible by directly scaling the digital inputs.

The I and Q arms are combined through current addition at the drain node of the switches. Each arm is turned ON for 25% of the clock cycle. Due to memory effects, there is interaction between the I and the Q arms. Fig. 15 shows the drain waveforms for two conditions: I = 1, Q = 0.2 and I = 0.2, Q = 1 at 1 GHz. The waveforms are asymmetric, due to memory effects. A sample 40-MHz 64-QAM constellation at 1730 MHz is shown in Fig. 16. Due to the interaction between the I and Q arms, the constellation is warped and this effect can be mitigated with the use of 2-D DPD [28]. The DPD table needs to be updated across frequency bands, as the magnitude of interaction between I and Q vary with frequency.

B. Tunable Output Network

The output network is shown in Fig. 17, where C_P and C_{SH} are control bits for the tunable capacitance bank. The optimal impedance required by the PA at different frequencies under the constraint of using a single inductor is determined. C_{PAR} adds to the C_{SH} capacitor bank and the pad capacitance C_{PAD} adds to the C_P capacitor bank. MOM capacitors are used for better linearity and the capacitor bank is implemented as weighted capacitors with wide NMOS switches to ground. Binary weighting of switches drastically reduces the efficiency when the smaller capacitors are turned ON. Wide switches result in larger parasitic capacitances which result in loss of capacitor accuracy, especially for the LSB capacitors. However, the accuracy of the capacitor bank is not critical, and is tradedoff for efficiency. The problem is mitigated by segmenting the smaller capacitors, so that effective tuning can be accomplished. The C_P capacitor has 5-bit control while the C_{SH} capacitor has 3-bit control.

TABLE IV
TABLE OF COMPONENT VALUES FOR DIFFERENT FREQUENCY POINTS

Frequency	C_P	C_{SH}	Impedance
750 MHz	5.5 pF	3.5 pF	$22.83 - j9.56$
1 GHz	5 pF	3 pF	$17.6 - j2.83$
1.5 GHz	3.5 pF	1.5 pF	$16.43 + j6.5$
2 GHz	2 pF	0.5 pF	$18.56 + j19.96$
2.5 GHz	1 pF	0 pF	$19.3 + j20.33$

The final component values and the corresponding impedance values presented to the switching transistors are listed in Table IV for different frequencies between 750 MHz and 2.5 GHz. In contrast, for the same output power, while using the traditional Class-E PA, the impedance has to be $20 + j23.6$. The comparison is shown in Fig. 18. The simulated drain waveforms along with the 25% duty cycle I and Q clock phases are shown in Fig. 19(a)–(c) at 1, 1.7, and 2.5 GHz, respectively. The drain waveform is characteristic of Class-E operation at all these frequencies. Fig. 20 shows the performance of the PA when the matching network is tuned to different frequencies, comparing it with the performance obtained when the output matching network is fixed. The matching network is able to tune the PA such that a constant output power is obtained across the frequency range with high efficiency.

C. Harmonic Suppression

Since there is no off-chip filter to remove the harmonics, the output network has to attenuate them sufficiently. The second harmonic for f_c up to 1.25 GHz and the third harmonic

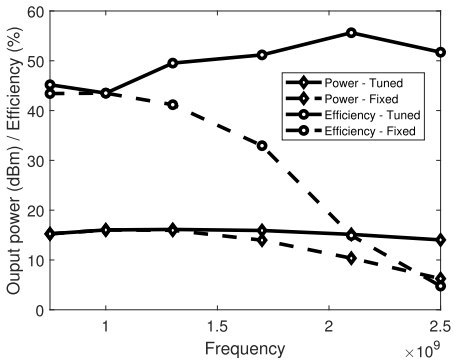


Fig. 20. Simulated output power and efficiency with the output matching network tuned and fixed.

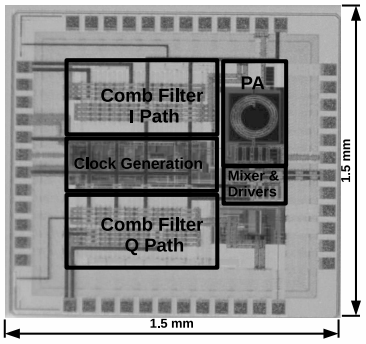


Fig. 21. Chip photomicrograph.

for f_c up to 800 MHz lie within the band of interest which need to be suppressed. A harmonic suppression of -25 dBc is targetted. A differential implementation of the same can help in suppressing the even order harmonics. However, in this test-chip, a single-ended implementation was done.

D. Predistortion Linearization

Predistortion is required to linearize the DAC. A lookup table (LUT) is constructed by comparing the output of the PA to the ideal DAC response. The use of end-fit linearization scheme for the proposed PA ensures that there is no need for back-off while transmitting signals with amplitude modulation on them. This implies that the full power and efficiency range of the PA can be utilized.

VII. Measured Results

A test chip (see Fig. 21) with an active area of 1 mm × 1 mm was designed and fabricated in a 130-nm CMOS process and packaged in a QFN48 package. The FIR filter, DPD segments and the supply choke inductor were implemented off-chip. The test setup is shown in Fig. 22. I and Q analog baseband signals are obtained from the back panels of the vector signal generator (VSG). The signals are digitized and processed in MATLAB for DPD and FIR filtering. The processed waveforms are sent as digital bits to the chip through a digital IO card. The clock source is derived from a continuous wave source at twice the carrier frequency. The far-out measured spectrum while transmitting a 25-kS/s 16-QAM signal at

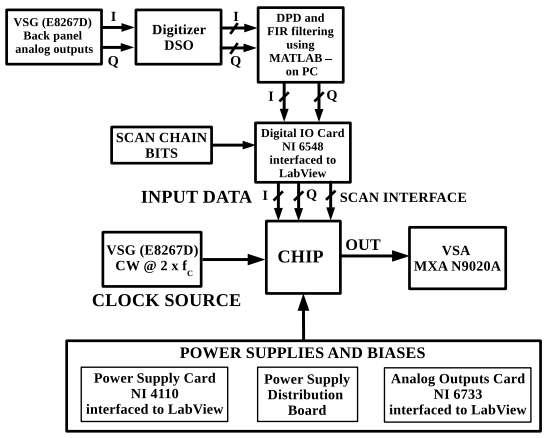


Fig. 22. Experimental setup for characterization of the transmitter IC.

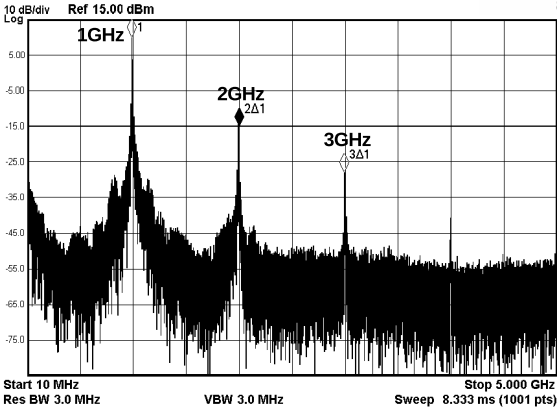


Fig. 23. Wideband spectrum while transmitting at 1 GHz. The spurs exist only at the harmonics of 1 GHz. The other spurs are cleaned up by the digital processing block.

1 GHz is shown in Fig. 23. The baseband signal was sampled at 1 MHz. The measured spectrum shows that the sampling spurs are eliminated till the carrier frequency. The transmitter can be operated from 0.75 to 2.5 GHz in separate bands. For each band, the output network is reconfigured, thus presenting the optimal impedance to the PA switches. Fig. 24(a) shows the maximum output power at different frequencies between 0.75 and 2.5 GHz. Fig. 24(b) shows the corresponding maximum efficiency. The simulated data is overlaid with the measured data. The simulated performance of the PA, with conventional parasitic extraction (caliber) is shown. When the EM-simulated model of the inductor is included, some degradation in performance is observed. This discrepancy is observed specifically at higher frequencies because the choke was placed off-chip. The PA's dc feed line trace on the PCB was also modeled and included in the simulations as shown. Further degradation seen at higher frequencies in the measured results are captured with the ground line parasitics. At 1 GHz a maximum output power of 13.7 dBm with an efficiency of 27% is observed. Up to 1.5 GHz, the output power is greater than 11.5 dBm. The improved efficiency numbers at lower frequencies [see Fig. 24(b)] can be attributed to the lack of resonance in the dc feed line. At higher frequencies,

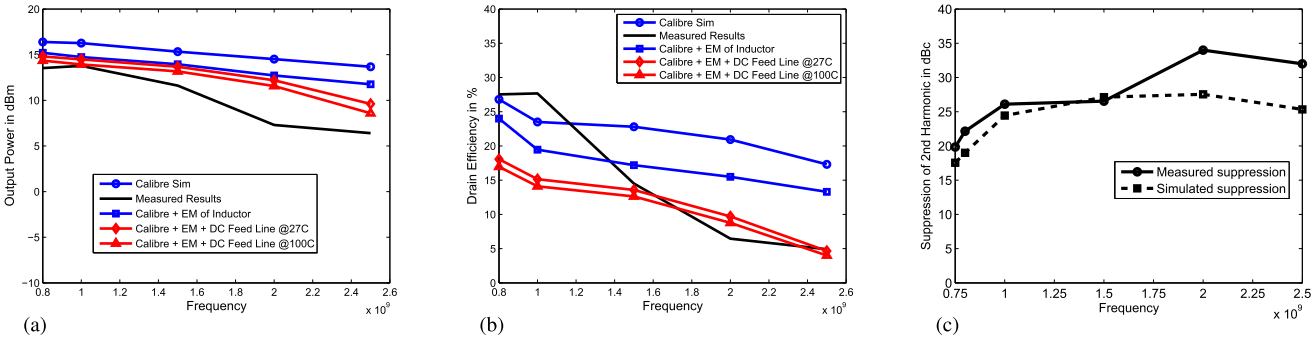


Fig. 24. Measured and simulated (a) output power, (b) efficiency, and (c) suppression of second harmonic component. The output network is reconfigured for each band from 0.75 to 2.5 GHz.

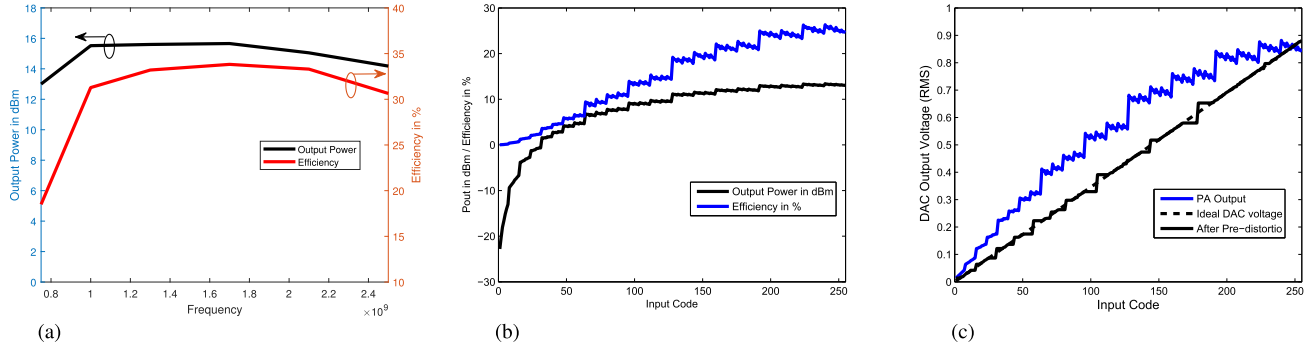


Fig. 25. (a) Simulated output power and efficiency of the PA with an integrated dc feed inductor. (b) Measured results showing output power and efficiency versus input code at 1 GHz. (c) Measured results showing correction using DPD for linearization.

TABLE V
MEASURED LINEARITY METRICS OF THE TRANSMITTER AT 0.8, 1, AND 2 GHz

Frequency	800 MHz	1 GHz	2 GHz
EVM (RMS)	3.1%	4%	13.4%
Magnitude Error	1.6%	1.9%	8.3%
Phase Error	2.15 deg	3.5 deg	10.4 deg
Quadrature Error	0.7 deg	1.1 deg	3.6 deg
Gain Imbalance	0.3 dB	0.3 dB	0.14 dB

however, the resonant behavior of the dc feed-line dominates, decreasing output power [see Fig. 24(a)] and efficiency [see Fig. 24(b)]. Fig. 24 shows the suppression of the second harmonic component across the frequency band. As a result of the digital processing, the residual spurs occur only at the harmonics of the carrier. The most prominent among them is the second harmonic. More than 25 dB of second harmonic suppression is measured between 0.8 and 2.5 GHz. By implementing a balun and a differential PA, the even order harmonics can be suppressed further.

The modification of the drain node impedance due to the off-chip RF choke was determined to be the reason behind the degraded performance higher frequencies, as predicted by simulations of the dc feedline. Hence a second version of the PA was designed with an integrated inductor. The layout parasitic-extracted simulation results are shown in Fig. 25(a). A on-chip dc feed inductor of 5 nH was used. The output power and efficiency are found to be fairly constant over the

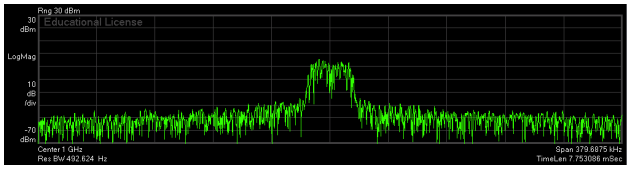


Fig. 26. Close-up spectrum while transmitting a 16-QAM signal at 1 GHz.

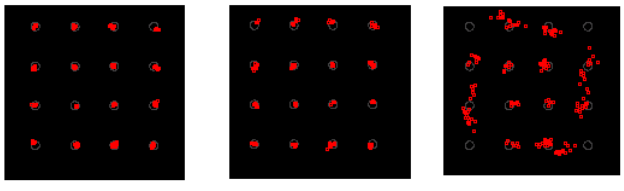


Fig. 27. Constellation plot while transmitting a 16-QAM signal at 800 MHz, 1 GHz, and 2 GHz.

frequency range of 750 MHz–2.5 GHz, implying that although an on-chip RF-choke is area in-efficient, it improves overall system performance across a wide range of frequencies.

The output power and efficiency variation with respect to the digital inputs to the PA is plotted in Fig. 25(b). We observe that there is non-monotonicity arising out of binary-weighted switches. A segmented architecture should potentially solve the problem. DPD is employed to linearize the PA. An end-fit scheme of predistortion is used to map the measured response to the ideal straight line characteristics of the DAC and a LUT

TABLE VI
COMPARISON WITH THE STATE-OF-THE-ART

Reference	Frequency Range	Architecture	Output Power	Efficiency	Matching Network	EVM	Frequency tunability	Technology
Shreshtha06 [6]	DC-2.4 GHz	Polyphase modulator	9 dBm	11%	Off-chip RF choke	NA	Yes	130nm CMOS
Ingels10 [8]	0.75-2.5 GHz	Analog TX	0-4 dBm	NA	On-chip	NA	Yes	40nm CMOS
Hampel12 [10]	9 GHz	Analog TX Inductive Degeneration	4 dBm	NA	Bondwires as RF Choke	NA	No	65nm CMOS
Analui14 [11]	50 MHz-6 GHz	Analog TX	0.2-2.7 dBm	NA	On-chip wideband Trans. Lines	NA	Yes	130nm CMOS
Yin15 [12]	0.1-6 GHz	Analog TX 4-band solution	2 dBm	NA	On-Chip	1.8% for WCDMA	Yes	65nm CMOS
Presti09 [15]	0.8-2 GHz	Polar TX	23.5-25 dBm	40-47%	Off-chip matching & tuning network	1.5% for 5 MHz WiMAX	No	130nm SOI CMOS
Werquin13 [16]	0.9-1.9 GHz	Polar TX	16.7 dBm	12.4%	Off-chip matching network	-28 dB for 64 QAM	No	65nm CMOS
Moloudi09 [21]	900 MHz	Outphasing TX	16-13 dBm	49%	Off-chip combining & matching network	NA	No	90nm CMOS
Lemberg19 [25]	1.5-1.9 GHz	Triphasing	29.7 dBm	35%	Off-chip power combiner	5.2% for 40 MHz 64 QAM OFDM	No	28nm CMOS
Lu13 [33]	2.4 GHz	Digital IQ TX	24.7 dBm	37%	On-chip balun	-25 dB for 802.11g	No	40nm CMOS
Zhu17 [19]	2.08 GHz	Polar TX	21.9 dBm	41%	On-chip balun	4.5% for 40 MHz 64 QAM	No	55nm CMOS
This work	0.75-2.5 GHz	Digital IQ	6.5-13 dBm	27% @ 1 GHz	On-chip (Off-chip RF choke)	4% for 25 KHz 16 QAM	Yes	130nm CMOS

is formed. In Fig. 25, the measured DAC performance and the post-DPD performance are overlaid, demonstrating significant improvement due to the DPD.

A 16-QAM baseband signal is digitized and fed to the transmitter. The output of the transmitter is analyzed using an Keysight MXA N9020A Vector Signal Analyzer. The PA output has an EVM of 4% while transmitting at 1 GHz. The measured spectrum is shown in Fig. 26. Table V tabulates the measured linearity metrics at 0.8 GHz, 1 GHz, and 2 GHz. The constellation plots at 800 MHz, 1 GHz, and 2 GHz are shown in Fig. 27. At 800 MHz, the transmitter achieves an EVM of 3.1% and 13% at 2 GHz.

The clock circuitry consumes 67 mA. The mixer, PA drivers along with additional circuitry driving 50-Ω loads for test purposes together consume 74 mA at 1 GHz. The power consumption in clock, DSP, and drivers can be significantly reduced with the use of more advanced technology nodes.

Table VI compares this design with other transmitters for SDR/CR. Compared to other wideband analog transmitters, this design achieves higher output power and efficiency, while covering a significantly wide range of frequencies. When compared to other digital wideband transmitters, this design achieves a wider frequency range of operation than those reported in literature. Many of the digital wideband transmitters compared here use off-chip matching networks or operate at a fixed frequency range. There is no frequency tunability. Though off-chip matching elements help improve efficiency, they are not cost-effective. The proposed design is one of the very few transmitters in literature with an integrated matching network, operational across a wide range of frequency, close to two octaves.

VIII. CONCLUSION

This article presents a wideband reconfigurable transmitter which can be operated from 750 MHz to 2.5 GHz. The problem of sampling spurs is solved with an efficient two-step digital filtering process. A mathematical approach to designing reconfigurable Class-E PAs is laid out and practical challenges are addressed. A chip has been fabricated to verify these ideas and the measured results are presented. The proposed transmitter holds great promise for SS applications, especially in the context of 5G radios, due to its versatility and low digital overhead when compared to other digital transmitter architectures. The transmitter is scalable and future implementations on advanced technology nodes are expected to be more power efficient.

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