Highly Efficient Packaged 11–13 GHz Power Amplifier in SiGe-Technology With 37.3% of PAE

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***Abstract*—A power amplifier for a frequency range of 11–13 GHz that is incorporated in 0.35 μm SiGe-technology is presented in this letter. The two-stage push-pull amplifier uses monolithically integrated transformers for input and interstage matching and a monolithically integrated modified LC-balun as an output—matching network. For stabilization purposes and gain improvement in the operating frequency range a passive frequency selective feedback in parallel to the base—collector was introduced. The power amplifier is mounted on a 7 × 7 mm VQFN package. From a single 1.8 V voltage supply, the amplifier has a power-added efficiency of greater than 30% from 11.2 to 13 GHz with a maximum of 37.3% at 12.5 GHz. The maximum output power is 23.4 dBm (saturation), as measured in the continuous mode.**

***Index Terms*—LC-balun, Power amplifier (PA), SiGe HBT.**

I. Introduction

INVESTIGATIONS on power amplifiers (PA) in SiGe technology continue to be of great interest because they offer good radio frequency performance at moderate costs relative to III–V semiconductor technologies [1]. The capability to use SiGe-technologies for power amplifier applications in the X/Ku-band is well demonstrated. Recently, published power amplifiers with nearly 1 W output power [2] and high values of power-added efficiency (PAE) [3], [4] have been reported. However, although the demonstrated PAs are either directly mounted on a substrate or measured on-chip, they are not mounted on a standard package. This letter presents the next step, a power amplifier for 11–13 GHz, which is mounted on a package for a specific output power.

A circuit description of the PA is given in Section II, followed by a brief discussion of the introduced frequency selective feedback in Section III. A successful usage of this feedback in a low noise amplifier was presented by the authors in [5]. The measurement results of the PA in Section IV demonstrate a highly efficient operation of the amplifier, mounted on a 7 × 7 mm VQFN package. A maximum PAE of 37.3% without external matching from a single 1.8 V voltage supply was obtained. The maximum predefined output power is 23.4 dBm at 12.5 GHz.

II. Circuit Description

A 0.35 μm 200 GHz-f_t SiGe process, provided by Infineon, was used as the design technology. This technology offers four metal layers with one thick top metal layer for high Q passive structures such as inductors and transformers. The BEOL (back end of line) of this process uses copper for metallization with a maximum thickness of 2.75 μm for the top metal. The used transistors have a breakdown voltage of $BV_{CEO} = 1.7$ V and the transit frequency is $f_t = 170$ GHz.

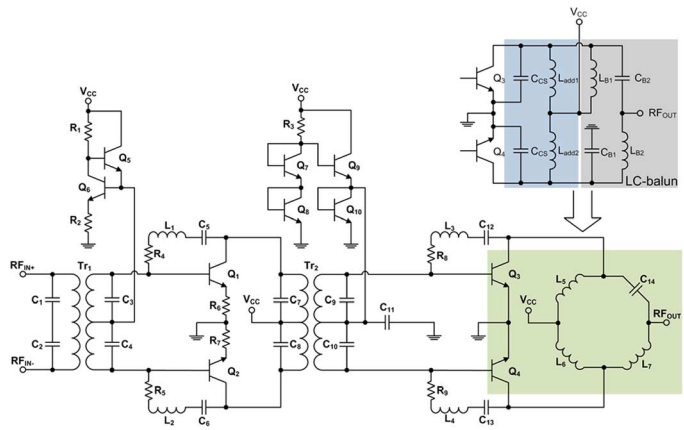

Fig. 1. Circuit diagram of the power amplifier with a modified LC-balun.

As one component of a phased array transceiver, the power amplifier is driven by a differential mixer architecture. A single-ended output of the PA is used to feed an antenna element. Fig. 1 depicts the circuit diagram of the PA. A two-stage push-pull topology was selected for two reasons. First, a single-stage amplifier provides insufficient overall gain for most applications. Therefore, a driving stage was added to increase the gain of the power amplifier. The second reason for the use of this topology is an easier impedance matching. The input and output impedance is doubled relative to a single-ended design. Furthermore, the negative impact of the common lead impedance on the performance is reduced [6].

The monolithically integrated transformers Tr_1 and Tr_2 are used for impedance matching and DC decoupling. Capacitors were used to bring the transformers to resonance at the operation frequency. The turns ratio of the input transformer is 3:2 with a chip area of 95×95 μm^2. The interstage transformer Tr_2 uses an area of 140×140 μm^2 with a turns ratio of 2:1.

The output matching circuit was realized using a modified LC-balun [3]. The idea was not only to match the load resistance with the transistors' output resistance, but also to transform the complex output impedance of the output stage with additional inductances to pure ohmic one. For clarification, a simplified circuit diagram in Fig. 1 was presented. A conventional Lattice-type LC-balun (L_{B1}, C_{B1}, L_{B2} and C_{B2}) is shown in the gray shaded area of Fig. 1, considering that L_{B1} and C_{B1}

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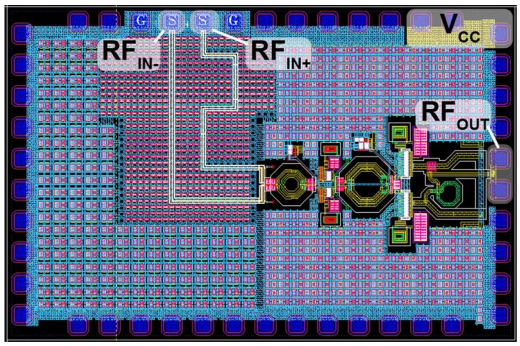

Fig. 2. Layout screen shot of the test chip.

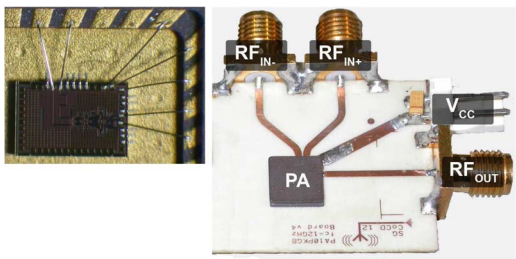

Fig. 3. Measurement setup with the chip mounted on the package and soldered on a printed circuit board.

are virtually grounded. The parasitic collector—substrate capacitances C_{CS} can be neutralized by using additional inductances (L_{add1} and L_{add2}), shown in the blue highlighted section of Fig. 1. Furthermore, both additional inductances are in parallel with L_{B1} and C_{B1}, respectively. Consequently, they can be substituted by equivalent impedances. This approach results in the modified LC-balun that is depicted in the green shaded area in Fig. 1. The insertion loss of the simulated balun itself is 1.4 dB. Compared to the conventional LC-balun design, the performance of the output matching network, including C_{CS}, is improved by 0.4 dB for this PA. A further advantage, also for an LC-balun in general, is the easier scalability compared to monolithically integrated transformers. With the same amplifier architecture, the demand for a higher output power is accompanied by an enlargement of the output stage. This scaling results in a wider trace width because of larger currents in the output matching network. For an LC-balun, it mainly affects the quality factor of the inductances. However, this influence is smaller and easier to handle than a performance degradation of the transformer due to a wider trace width.

The effective emitter area of the output stage transistors is 67.2 $\mu\mathrm{m}^2$, as determined primarily by the required output power in accordance with the maximum current density. The input stage is three times smaller. Both stages are on-chip biased through the center tap of the transformers with low impedance reference networks, to overcome the limit of $\mathrm{BV_{CEO}}$ for the maximum collector voltage [7]. The input stage uses low value resistors ($R_6, R_7 = 4\ \Omega$) at the emitter for a weak emitter degeneration, which improves the linearity of the input stage at the expense of gain. Obviously, a emitter degeneration with resistors in the output stage is unsuitable. High currents in the output stage and a low supply voltage result in a high degradation of the power-added efficiency.

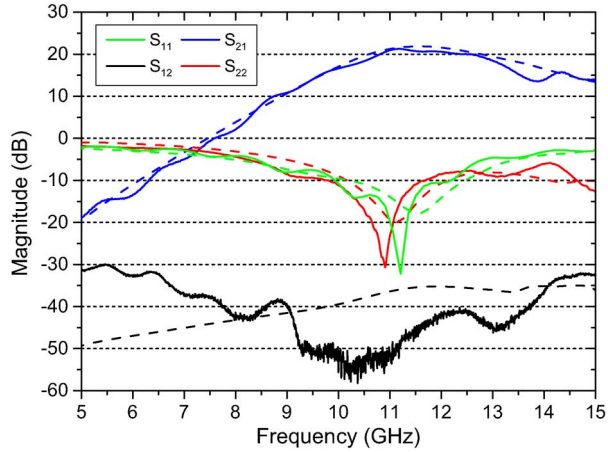

Fig. 4. Results of the small signal measurement, simulation results are dashed lines.

III. Stability Considerations

Circuit stability is typically an important aspect of amplifier design. Especially in power amplifier designs it is a very challenging task to attain stable circuit operation because of the large transistors in the output stage. Among many other sources of instability in a circuit, the intrinsic feedback of a transistor by the base—collector capacitance (C_{jc}) is one of the most important sources. A simplified analysis of the impedance transformation of the load impedance through C_{jc} forward to the input is given in [6]. It is derived, that with a certain given inductive load impedance, the input resistance of the transistor becomes negative, which can excites unwanted oscillations.

To counteract this situation, a passive frequency selective feedback (FB) in parallel to the base—collector capacitance was introduced. Fig. 1 presents it as the RLC network between the base and collector at the input and output stage. The network is used in two ways:

1) As a parallel resonant circuit ($L_{FB} \| C_{eq}$),[1] it neutralizes base—collector capacitance [5], [8]. L_{FB} and C_{FB} denote feedback components (e.g. L_1 and C_5 in Fig. 1).
2) As a series resonant circuit to decrease the gain and transform the impedance in the frequency range of possible instability [5].

As opposed to other stabilization methods, the frequency selective feedback can be applied at the input and output stage with negligible influence on the maximum output power and efficiency.

IV. Experimental Results

The power amplifier is intended to be integrated in a complete T/R-system. For a first characterization, a test chip with an overall area of $1.07 \times 1.6\ \mathrm{mm}^2$ was fabricated. The chip area that was used for the PA itself is $0.52 \times 0.75\ \mathrm{mm}^2$. A layout screen shot is shown in Fig. 2. The chip was glued onto the thermal exposed pad of the VQFN package and bonded to the package pads. Fig. 3 depicts the bonded die. The reason for the considerably long bond wires visible is as follow. The only degree of freedom to compensate the package parasitics is the length of the bond wires. To determine the optimal bond wire lengths,

[1] $C_{eq} = C_{FB}C_{jc}/(C_{FB} + C_{jc})$

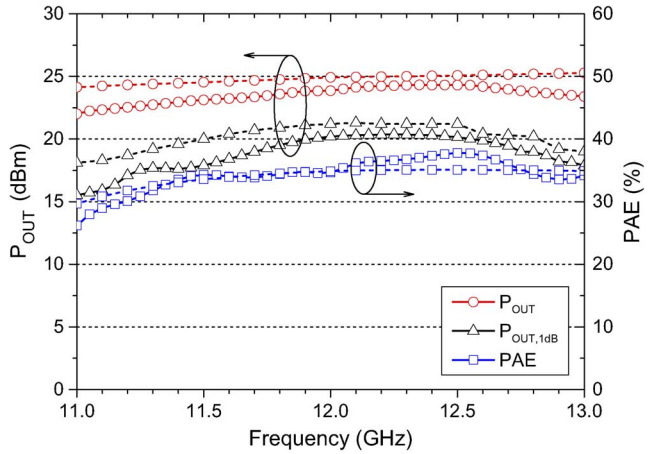

Fig. 5. Large signal results as function of frequency. For comparison, simulation results (dashed lines) and measurement results (solid lines) are plotted.

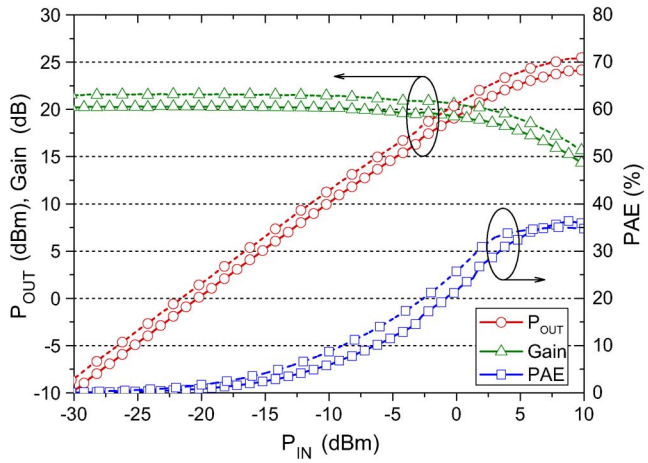

Fig. 6. Power transfer characteristic of the packaged PA at 12.1 GHz with simulation (dashed lines) and measurement results ((solid lines).

TABLE I
COMPARISON WITH PREVIOUS PUBLISHED WORKS

Ref.	Gain dB	P_{OUT} (in sat.) dBm	PAE %	OP1dB dBm	Chip area mm^2	PA Architecture
[2]	13.5	29.3	18	28 (from graph)	4.5	single-ended cascode, one stage
[3]	23	23	32	17	1.8	differential two stages
[4]	16	24.45	29.1	21.2	0.384	single-ended cascode, one stage
[9]	25.5	23.3	28	22.2	0.6 (core)	single-ended cascode, two stages
[10]	41	21.4	26	19.6	1.3	single-ended cascode, two stages
[11]	12.2	21.2	27.4	20.8	0.86	single-ended one stage
This work	**21.2**	**23.4**	**37.3**	**20.4**	**1.71**	**differential two stages**

and consequently the optimal chip position in the package, 3-D electromagnetic simulations was intensively used.

The measurements were performed on a Rogers 4003C substrate with 50 Ω input and output transmission lines, shown in Fig. 3. A single 1.8 V voltage supply for V_{CC} working in continuous mode was used. No additional power supplies were necessary.

Fig. 4 shows the measured and simulated S-parameters of the power amplifier. The differential input was driven by a single-ended signal source. An external rat-race coupler with a center frequency of 12 GHz was used to convert the signal. The loss of the 180 hybrid coupler was taken into account. In contrast, the losses of the evaluation board are not considered in measurement results but in simulation results. Fig. 5 depicts the maximum output power in saturation and maximum PAE versus input signal frequency. Additionally, the output power at the 1 dB compression point is shown. The measurement results demonstrate good agreement with the simulation results for large and small signal characteristic. In Fig. 6, the power transfer characteristics is exemplary plotted for 12.1 GHz. A two-tone test with a center frequency of 12.05 GHz results in an output third-order intercept point of 23.1 dBm.

Table I provides a comparison of recently published X/Ku-band SiGe-power amplifier with this PA [9]–[11].

V. CONCLUSION

A highly efficient power amplifier that is mounted on a VQFN package for 11–13 GHz with a maximum PAE of 37.3% was presented in this letter. To the authors' knowledge this is the highest reported power-added efficiency of a package-mounted and fully matched X/Ku-band power amplifier in SiGe-technology with a single voltage supply.

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