A Two-Point Modulation Technique for CMOS Power Amplifier in Polar Transmitter Architecture

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***Abstract*—A two-point modulation technique is presented that improves the performance of nonlinear power amplifiers (PAs) in polar transmitters. In this scheme, the output amplitude modulation is performed by controlling the current of the PA. The current control technique enables the PA to provide wideband amplitude modulation, as well as high power control dynamic range. In addition, the supply voltage of the PA is adjusted based on the output power level. The voltage supply adjustment substantially improves the effective power efficiency of the PA. The voltage supply control is performed using a second-order sigma–delta dc–dc converter, which presents an efficiency of over 95% in its operational range. The PA operates at 900 MHz with maximum output power of 27.8 dBm and power efficiency of 34% at maximum output power. The proposed PA achieves 62-dB power control dynamic range with amplitude modulation bandwidth of over 17.1 MHz. The circuits are fabricated in a CMOS 0.18-μm process with a 3.3-V power supply.**

***Index Terms*—Amplitude modulation, CMOS power amplifier (PA), nonlinear PA, polar transmitter, transmitter.**

I. Introduction

THE CMOS power amplifier (PA) suffers from low output power, as well as low power efficiency [1]–[3]. To overcome these issues, it is suggested in many papers to employ a polar transmitter architecture, which enables the use of high-power highly efficient nonlinear PAs [4]–[7]. In a polar transmitter, the phase component of the RF signal is amplified through a nonlinear PA, while the amplitude information is applied at the output. Fig. 1 shows the conventional amplitude modulation techniques that are mainly based on the modulation of the supply voltage [4].

In general, the amplitude and phase components in a polar modulator occupy several times more bandwidth compare to the complex signal [4]. This requires a very wideband amplitude modulation technique to be employed for the PA. Moreover, many wireless systems require the transmitter to continuously adjust its output power level to maintain the received signal from all users at the same level. The conventional amplitude modulation techniques suffer from bandwidth limitation, as well as very poor power control capability [8]. To address these issues, a new PA architecture is proposed in [5] that employs a current control technique for amplitude modulation and power control. Compared to conventional methods, the new technique provides superior amplitude modulation bandwidth and power control dynamic range. However, it suffers from the low power efficiency at low output power levels.

In this paper, a two-point modulation technique is proposed, in which the supply voltage is adjusted based on the output power level, while the amplitude is set through the tail current source. The voltage supply adjustment leads to substantial improvement of the efficiency at a low power level. In addition, the circuit takes the advantage of a current-based amplitude modulation technique [5], which results in a very high-power control dynamic range, as well as wideband amplitude modulation. The proposed architecture is explained in detail in Sections II and III. The measurement results of the circuit are presented in Section IV, and finally, a summary and conclusions are provided in Section V.

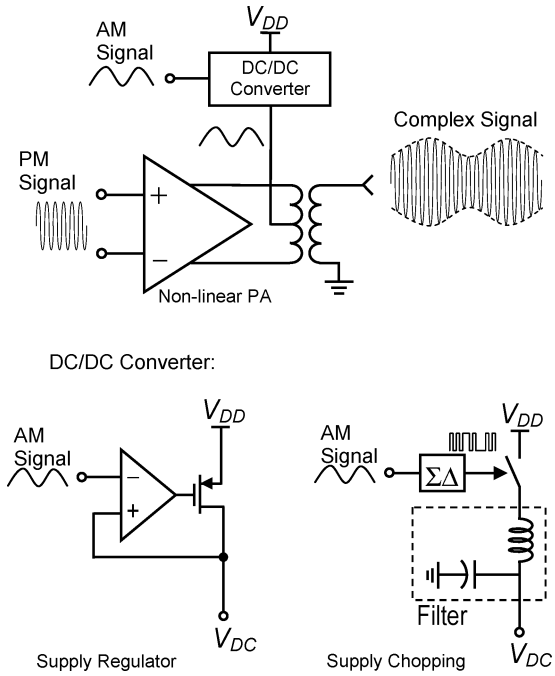

Fig. 1. Conventional amplitude/power control techniques in polar transmitters.

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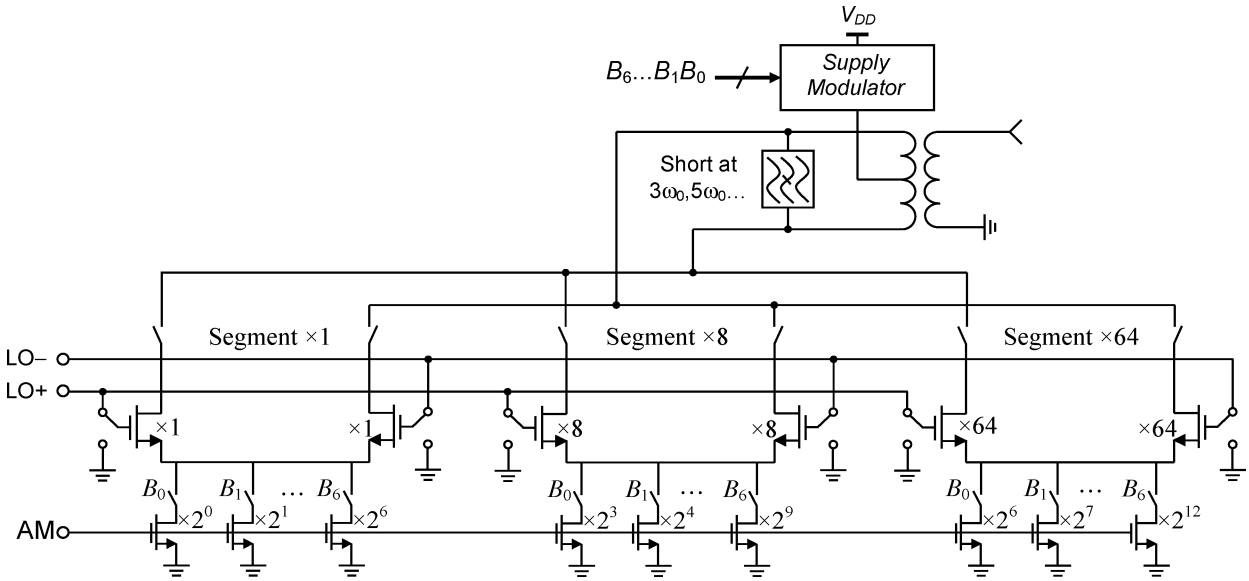

Fig. 2. Proposed switching PA using two-point modulation technique.

II. CMOS Switching PA

Shown in Fig. 2 is the proposed PA that employs a two-point modulation technique. In this structure, the output amplitude is controlled by the bias current of the PA. As shown in Fig. 2, the amplitude data and power control command are applied to the tail current source, which generates a current proportional to envelope of the RF output signal [5]. The current is up-converted to the frequency of interest by applying the output of the frequency synthesizer to the switching transistors. This configuration acts similar to a single balanced mixer in which the low-frequency amplitude data is up-converted to the RF frequency using a phase-modulated local oscillator (LO) signal. The tail current source of the PA is designed as a binary weighted digital-to-analog converter (DAC). The generated current is given by

$$I_B(t) = I_{\rm ref}(t) \cdot \left(B_0 \times 2^0 + B_1 \times 2^1 + \cdots + B_{N-1} \times 2^{N-1}\right) \tag{1}$$

where parameter $I_{\rm ref}$ is the DAC reference current that is used for amplitude modulation. The digital word $[B_{N-1} \ldots B_0]$ is the power control command that is applied to the digital input of the DAC. Due to the separation between the amplitude modulation and power control, the PA is capable of providing high-resolution amplitude modulation along with a high-power control dynamic range. In addition, the current modulation is relatively fast and is, therefore, suitable for high data-rate wideband applications. The supply voltage of the PA is also adjusted to reduce the dc voltage drop out over the tail current source at a low power level, which improves the efficiency of the circuit. To reduce the LO feedthrough, the PA uses three segments of ×1, ×8, and ×64 [5].

Assuming that the bandwidth of the amplitude modulation data is much lower than the LO frequency, the output envelope can be expressed as [5]

$$\hat{u}_a = \frac{2}{\pi} I_B(t) \cdot R_L. \tag{2}$$

To generate the complex output RF signal including amplitude and phase data, the phase information of the signal is applied to the LO input of the PA, which triggers the switching transistors. As a result, the current waveforms of the switching transistors are expressed as

$$i_{M1}(t) = i_{M2}(t + \pi/\omega_0) = I_{B0}(t) \cdot \operatorname{sign}\left[\cos\left(\omega_0 t + \varphi(t)\right)\right] \tag{3}$$

where

$$\operatorname{sign}(x) = \begin{cases} 0, & x < 0 \\ 1, & x \geq 0. \end{cases} \tag{4}$$

It can be shown that the response of a nonlinear system to a phase modulated signal, i.e., $s(t) = \cos[\omega_c t + \varphi(t)]$, can be expressed as a quasi-Fourier series [9]

$$r(t) = \sum_{n=0}^{n=\infty} b_n \cos\left(n\omega_0 t + n\varphi(t)\right) \tag{5}$$

where the b_n's are the same as Fourier coefficients of the system's response to a sinusoidal wave at the frequency of ω_0. This implies that by applying the phase modulation data to the LO signal, the phase of the output is modulated. Therefore, the output voltage waveform can be expressed as

$$v_{\rm RF}(t) = \hat{u}_{\rm RF}(t) \cdot \cos\left(\omega_0 t + \varphi(t)\right). \tag{6}$$

As can be seen in (6), the proposed PA generates the output RF signal by combining the phase and amplitude data. In reality, however, the nonidealities of the circuit results in the distortion of the amplitude data. The increase of the input amplitude modulation signal leads to saturation of the output envelope, which is known as AM–AM distortion [7]. The AM–AM distortion can be reduced by using a predistortion filter, which distorts the amplitude data in order to compensate the nonlinearity effect of the PA. In addition, using a closed-loop polar transmitter can substantially reduce the AM–AM distortion of the PA [6].

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The main issue of using the current control technique for amplitude modulation is the dependency of the power efficiency on the output level [5]. This problem has been solved by adjusting the supply voltage based on the output envelope. This technique is explained in detail in Section III.

III. Efficiency Improvement Technique

Equation (2) can be used to express the instantaneous output power of the circuit as

$$P_{\text{out}}(t) = \frac{2}{\pi^2} \cdot I_B^2(t) \cdot R_L. \tag{7}$$

Using (2) and (7), the instantaneous power efficiency of the circuit can be expressed as

$$\eta(t) = \frac{P_{\text{out}}(t)}{V_{DD} \cdot I_B(t)} = \frac{\hat{u}_a(t)}{\pi \cdot V_{DD}}. \tag{8}$$

Equation (8) indicates the circuit has low power efficiency when the output envelope is small. This phenomenon is more critical in applications with high power control dynamic range. As implied by (8), the efficiency of the circuit can be improved by adjusting the supply voltage according to the output level. Theoretically, the output envelope is independent of the voltage for supply voltage level of higher than a minimum required amount to keep the tail current source in the active region. Therefore, if the supply control is performed at a high efficiency, it will improve the efficiency of the circuit at low output levels.

In the proposed PA, the supply voltage is adjusted according to the power control command. Since the power control rate is slower compare to the envelope modulation, the supply modulation can be performed by using a high-efficiency switching regulator. This technique is very effective to improve the effective efficiency of the PA. The effective efficiency represents the amount of power transmitted to the antenna, for a long period of time, divided by the total consumed power. This parameter depends on the probability distribution function (PDF) of the transmitter's output power and can be expressed as

$$\eta_{\text{eff}} = \frac{\overline{P}_{\text{OUT}}}{\overline{P}_{\text{IN}}} = \frac{\displaystyle\int_{P_{\min}}^{P_{\max}} p \cdot \text{PDF}(p) \cdot dp}{\displaystyle\int_{P_{\min}}^{P_{\max}} \frac{p}{\eta_{\text{av}}(p)} \cdot \text{PDF}(p) \cdot dp} \tag{9}$$

where $\eta_{\text{av}}(p)$ is the average power efficiency at the output power level of p and $P_{\max}$ and $P_{\min}$ are the maximum and minimum output power levels of the system. The effective efficiency indicates the maximum battery life, which is a very important parameter in wireless applications. On the other hand, the maximum efficiency indicates the maximum power dissipation of the circuit, which is important for thermal behavior of the chip. As an example, the PDF of the output power for wideband code division multiple access (WCDMA) transmitter (data link) is shown in Fig. 3. According to this graph, the output power level is around 10 dBm for the most of the operation time. Therefore, in this system, it is very important to have high efficiency at 10-dBm output power.

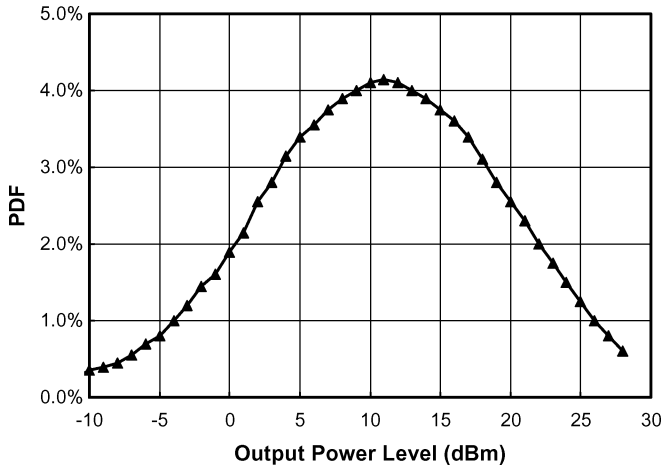

Fig. 3. PDF of transmitting power for WCDMA (data link).

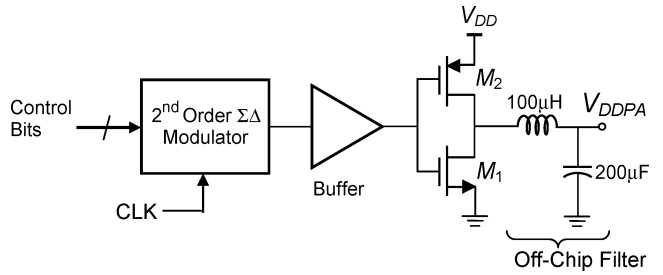

Fig. 4. Supply control circuit.

To control the supply voltage, we need to determine the minimum required supply voltage for a specific output power level. It can be shown that the amplitude of the differential voltage over the balance port of the balun is given by [5]

$$\hat{u}_a = \pi(V_{DD} - V_B) \tag{10}$$

where V_B is the voltage over the tail current source. Using (10), the supply voltage level has to be higher than a specific value given by

$$V_{DD,\min} = V_{B,\min} + \frac{1}{\pi}\sqrt{2 \cdot R_L \cdot P_{\max}} \tag{11}$$

where $P_{\max}$ is the maximum instantaneous power and $V_{B,\min}$ is the minimum voltage required over the tail current source.

The supply adjustment is performed using a switching sigma–delta dc–dc converter shown in Fig. 4. The circuit includes a low-pass second-order sigma–delta modulator, which generates a digital pulse train according to the 5-bit digital input [10], [11]. The sigma–delta modulator is implemented on field-programmable gate array (FPGA). The digital input indicates the level of the required voltage and varies from "00,. . .,0" to "11,. . .,1" for the output dc voltage of 0–3.3 V. The modulator output is applied to the switching inverter, which switches on/off the supply voltage of the PA according to the output of the sigma–delta modulator. Using a low-pass *LC* filter, the desired supply voltage is generated at the output. Due to the high dc current of the inductor and low cutoff frequency of the *LC* filter, the filter is realized by using off-chip components $L = 100\ \mu$H and $C = 300\ \mu$F.

The efficiency of the proposed circuit can be calculated similar to a class-D amplifier [12]–[14]. The quality factor of the

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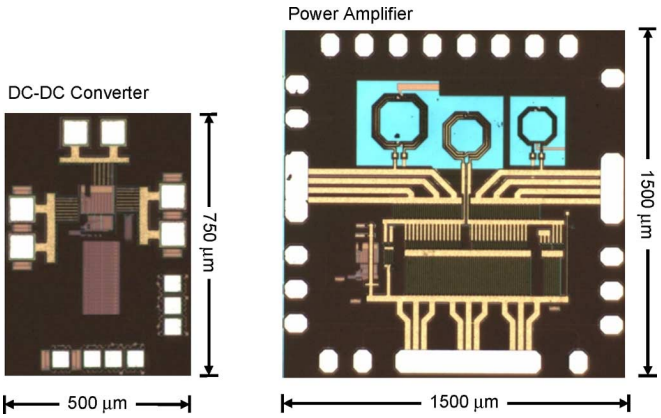

Fig. 5. Microphotographs of the fabricated test chips.

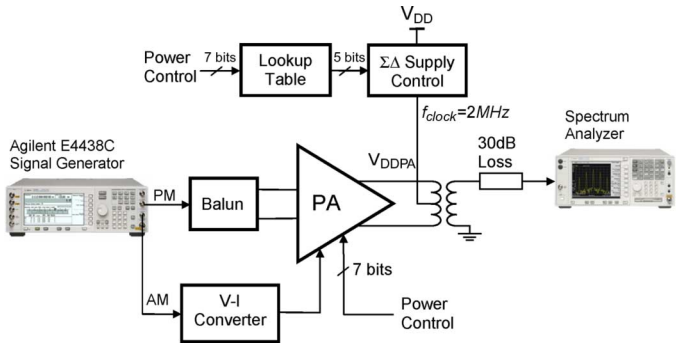

Fig. 6. Measurement setup.

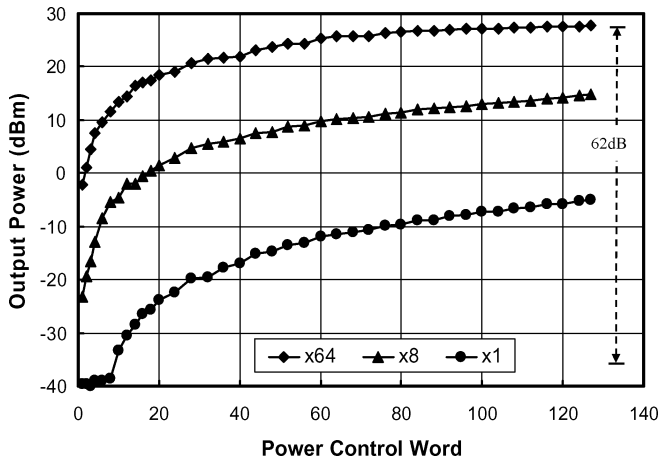

Fig. 7. Measured output power versus the input power control word for different segments of $\times 1$, $\times 8$, and $\times 64$.

off-chip inductor is high and, therefore, the loss of the output filter is negligible. In addition, using large devices for the output driver M_1 and M_2 guarantees the low voltage drop over each of the switching transistors when it is on. However, at each switching transition of high-to-low or low-to-high, the parasitic capacitor at the output node of the driver is charged or discharged accordingly. This introduces a power loss in the circuit. The parasitic capacitance at the output is relatively large due to the large transistor sizes and, therefore, the main source of the loss in the circuit is the switching loss, which is a function of the clock frequency. Due to the low power control rate, i.e., a few kilohertz, the dc output level of the switching dc–dc converter varies at low frequency. Therefore, the switching can be performed at a low rate, which guarantees the high efficiency of the circuit. The fabricated circuit operates at the clock frequency of 2 MHz.

IV. Measurement Results

The proposed switching PA and the dc–dc converter have been fabricated using a TSMC CMOS 0.18-μm process. The die photographs of these circuits are shown in Fig. 5. The PA occupies an area of 2.25 mm^2, which includes the bandstop filter that suppresses $3\omega_0$ and $5\omega_0$. The PA requires an off-chip balun to deliver the output power to a single-ended load. The dc–dc converter occupies an area of 0.375 mm^2 and employs an off-chip low-pass *LC* filter. The PA operates at frequency of 900 MHz, and the dc–dc converter uses the clock frequency of 2 MHz. The circuits employ 3.3-V supply voltage.

a The measurement setup is shown in Fig. 6. In order to test the PA in polar configuration, the PA is driven using Agilent Technologies' E4438C signal generator. This signal generator consists of two baseband generators, i.e., BB1 and BB2, that can be operated at the same time. There is an internal upconverter mixer, which is configured to upconvert the output of BB1 with a 900-MHz carrier signal. To drive the PM and AM paths of the PA, the baseband PM and AM data of a particular modulation is uploaded to BB1 and BB2, respectively. The RF output, which is the output of the internal mixer, is applied to the LO path of the PA, while the AM path is driven using the BB2 output. The synchronization of AM and PM data can be internally performed through the signal generator. In addition, the output power is controlled by a power control word, which is also used to set the level of the supply voltage. The proper voltage level for each power control word is stored in a lookup table, as shown in Fig. 6.

Shown in Fig. 7 is the measured output power of the PA for different segments of $\times 1$, $\times 8$, and $\times 64$. The output power is measured for different values of a 7-bit power control word varying from 1 to 127 for each segment of the circuit. The circuit presents 62-dB power control dynamic range with a maximum output power of 27.8 dBm. The minimum output power level of the circuit is mainly limited by the LO feedthrough, which covers the output signal of the PA for output power levels of less than -34 dBm. The power efficiency of the PA is shown in Fig. 8 versus the output power. The circuit achieves the power efficiency of 34% at its maximum output power level. The power efficiency is decreased as the PA operates at lower output power levels. It is shown in Fig. 8 that the voltage adjustment technique effectively improves the power efficiency at low output power levels. This data includes the loss of the switching dc–dc converter. The efficiency of the dc–dc converter is shown in Fig. 9 for different output voltage of the circuit while it drives a resistive load of 6 Ω. Fig. 9 indicates that the efficiency of the circuit in the range of operation, 1–3.3 V, is more than 95%.

To compare the power efficiency of the fabricated circuit with the existing PAs, the power efficiency versus the output power of various commercial WCDMA PAs are measured. Using this

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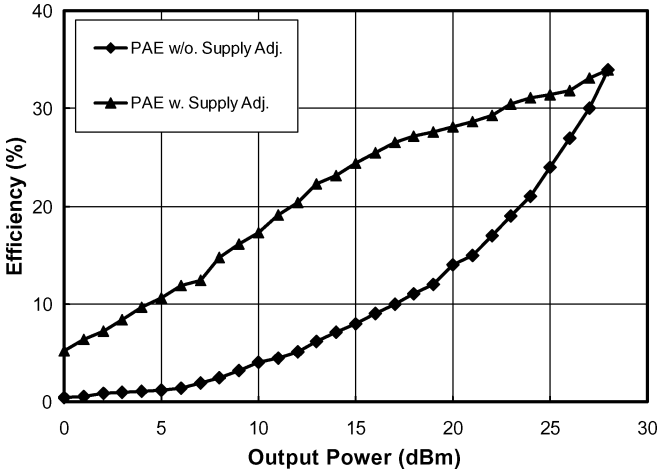

Fig. 8. Measured power efficiency versus output power for: (1) a fixed 3.3-V supply and (2) adjusted supply voltage according to the output power.

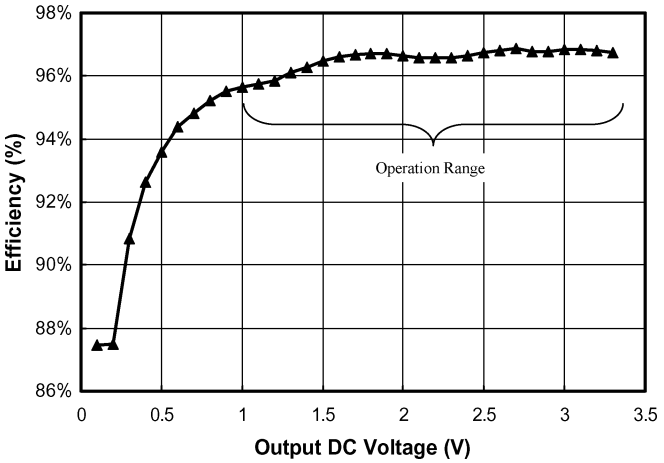

Fig. 9. Efficiency of the sigma–delta supply control circuit with load of 6 Ω.

TABLE I
MAXIMUM AND EFFECTIVE POWER EFFICIENCY OF DIFFERENT PAS FOR WCDMA (DATA LINK)

	$f_{carrier}$	η_{max}	$P_{in,av}$	η_{eff}
Proposed PA w. Adj.	900MHz	34.0%	170mW	26.5%
Proposed. PA w/o Adj.	900MHz	34.0%	375mW	12.0%
Skyworks 77173	1950MHz	36.8%	344mW	13.1%
Anadigics AWT6272R	836MHz	38.6%	365mW	12.3%
RFMD 5188	1950MHz	44.2%	413mW	10.9%

data and also the PDF function of the WCDMA transmitting power, shown in Fig. 3, the effective efficiency of each PA is calculated. The results are shown in Table I. As shown in this table, the effective efficiency of the proposed PA with a supply control loop is almost more than twice the effective efficiency of any other PA. In addition, the proposed PA is fabricated in the CMOS process, which enables the integration of the complete transceiver on a single die.

The two-tone test is performed by applying two tones with $f_1 = 1.9$ MHz and $f_2 = 2.1$ MHz to the amplitude modulation

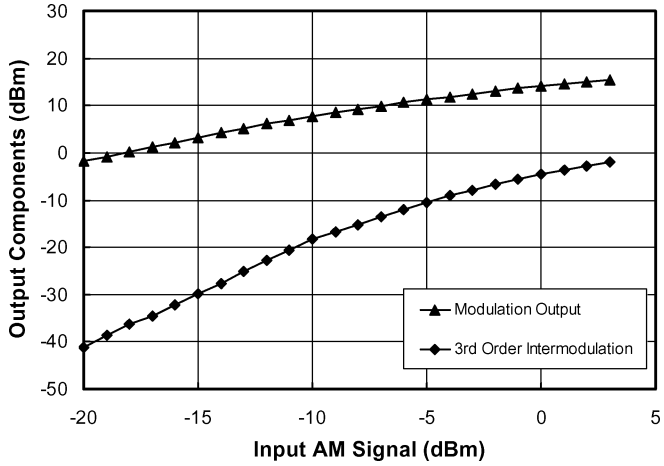

Fig. 10. Measured two-tone test results of the amplitude modulation for $P_{\text{out}} = 25.7$ dBm and $f_1 = 1.9$ MHz and $f_2 = 2.1$ MHz.

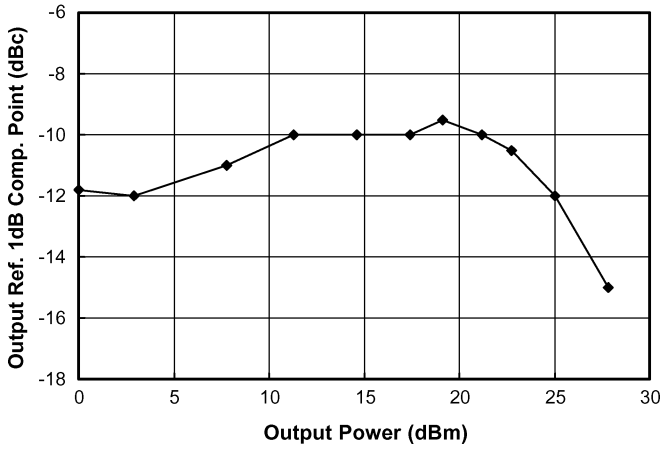

Fig. 11. Measured output referred −1-dB compression point of the amplitude modulation versus carrier output power (relative to the carrier).

path. In this measurement, the output power is set to 25.7 dBm and a 2-MHz tone is applied to the amplitude modulation path, while a 900-MHz LO signal is applied to switching transistors. Due to nonlinearity effects of the circuit, the output spectrum contains intermodulation components. Fig. 10 shows the measured first harmonic and the third-order intermodulation term of the modulated signal at the output spectrum for the output power of 25.7 dBm. The circuit exhibits the third-order output intercept point (OIP3) of −26.7 dBm. In the proposed PA, the linearity of the amplitude modulation is a function of the output power. Fig. 11 shows the output referred −1-dB compression point of the amplitude modulation for different output power levels. The bandwidth of the amplitude modulation is measured by applying a tone to the AM path and measuring the frequency at which the AM component at the output drops by 3 dB. The results are shown in Fig. 12 for different output power levels. At the maximum output power level, the circuit exhibits the AM bandwidth of 17.1 MHz, which is the highest reported among switching PAs designed for polar transmitters.

The AM–PM conversion is measured using a network analyzer to measure the variations of the carrier's phase versus the normalized output envelope. The results are shown in Fig. 13

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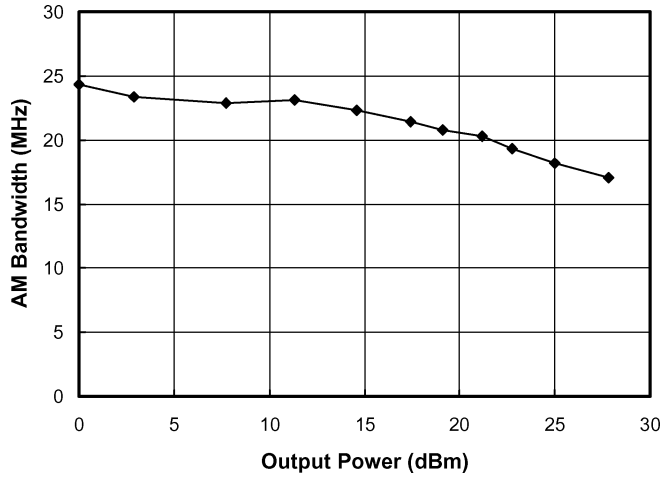

Fig. 12. Measured amplitude modulation −3-dB bandwidth for different output power levels.

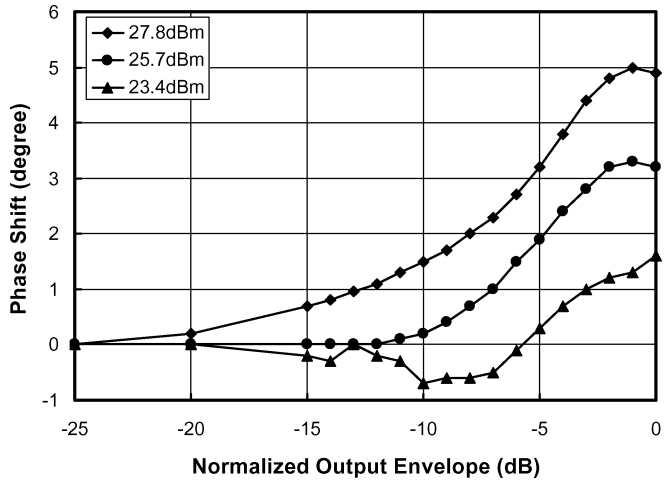

Fig. 13. Measured AM–PM conversion of the proposed switching PA for various output power levels.

for output power levels of 27.8, 25.7, and 23.4 dBm that correspond to the power control words of "1111111," "1011111," and "1001111," respectively. As shown in this figure, the AM–PM conversion is increased by increasing the output power level of the PA. The circuit exhibits the maximum phase shift of 5° at carrier output power of 27.8 dBm.

To better examine the performance of the fabricated PA, the circuit is tested by both EDGE and WCDMA signals. The output spectrum for EDGE and WCDMA signals are shown in Figs. 14 and 15, respectively. In both cases, the AM signal loaded into the BB2 of the signal generator is pre-distorted to compensate for the nonlinearity of the AM path. However, as the output power increases, both AM–AM and AM–PM characteristics of the PA become worst and, therefore, the output spectrum spreads out. This effect can be seen in Figs. 14 and 15 for EDGE and WCDMA signals. To avoid the violation of the output spectrum mask at high output power levels, it is required to use other techniques to compensate the nonlinearity of the PA. An example of these could be closed-loop feedback, although loop stability might have to be carefully checked. The summary of the measurement results of the fabricated test chips is shown in Table II.

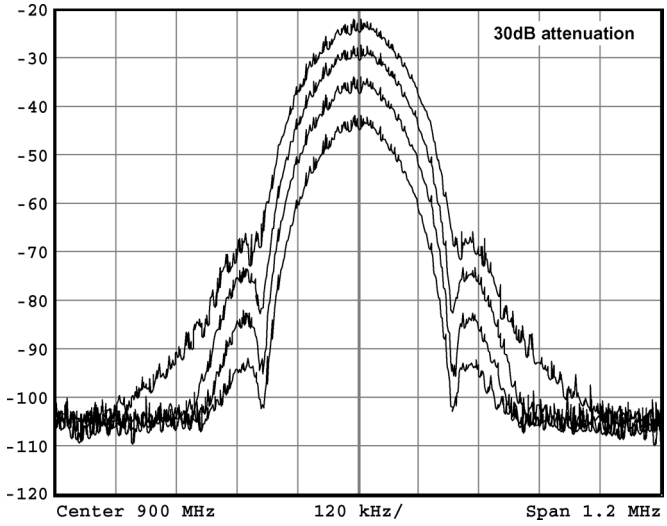

Fig. 14. Measured output spectrum for EDGE signal for output power level of 22, 16, 10, and 4 dBm.

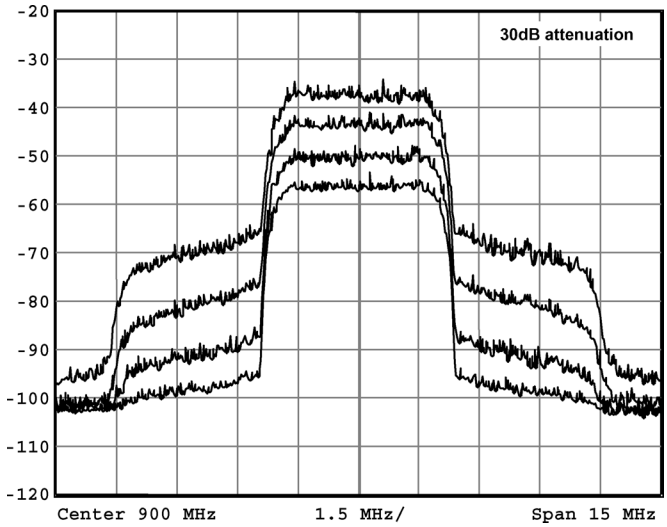

Fig. 15. Measured output spectrum for WCDMA signal for output power level of 22, 16, 10, and 4 dBm.

TABLE II
SUMMARY OF THE FABRICATED PA CIRCUIT

Operational frequency	900MHz
Maximum output power	27.8 dBm
Power efficiency @ P_{out} = 27.8dBm	34%
Power control dynamic range	> 62 dB
Amplitude Modulation BW	≥ 17.1 MHz
Amp. Mod. $P_{-1dB,output}$ @ P_{out} = 25.7dBm	-12.6 dBc
Amp. Mod. OIP3 @ P_{out} = 25.7dBm	-1 dBc
AM to PM @ P_{out} = 27.8dBm	< 0.4 degree/dB
Efficiency of the DC-DC Converter	> 95% ; 1V<V_{DDPA}<3.3V

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V. Conclusions

This paper introduces a new technique to modulate the output amplitude of nonlinear PAs in polar transmitters. The proposed method substantially improves the performance of the circuit. The measurement results show substantial improvement in the amplitude modulation capability, as well as the power control dynamic range compare to the existing nonlinear PAs. It is also shown that the proposed method considerably improves the effective efficiency of the PA.

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