A Load-Shared CMOS Power Amplifier With Efficiency Boosting at Low Power Mode for Polar Transmitters

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***Abstract*—A load-shared CMOS power amplifier (PA) for 1.8-GHz polar transmitter applications has been implemented in standard 0.18-μm CMOS technology and fully characterized to demonstrate its efficiency boosting technique in low power mode. With the aid of cascode amplifiers, the load-shared configuration achieves efficiency improvement at low supply voltage in a polar transmitter. A differential class-E amplifier with a parallel resonant circuit is analyzed and incorporated in the load-shared PA. The load-shared configuration is composed of driver amplifiers (DAs) and PAs whose output loads are shared. The DA has a constant gate voltage biasing of a cascode amplifier for efficiency boosting, whereas the PA has a self-biased cascode configuration to be turned on and off by a supply voltage. The measurement results of the load-shared configuration show a drain efficiency increase from 6% to 30% at 16-dBm output power compared with a conventional self-biased cascode amplifier. The load-shared PA is reported with 35.6% of power-added efficiency and 32.2 dBm of output power at 1.88 GHz.**

***Index Terms*—Cascode amplifiers, CMOSFET power amplifiers (PAs), mode locking, monolithic microwave integrated circuit (MMIC) PAs, polar transmitters.**

I. Introduction

A POWER amplifier (PA) is a key element in wireless communication systems. Since the PA consumes most of the battery power in mobile handsets, its efficiency directly affects overall talk time. Therefore, efficiency improvement has been a major issue in mobile PAs. Generally, amplifiers have high efficiency at peak output power, but the efficiency is decreased drastically as the output power decreases. Furthermore, PAs of mobile handsets in some applications operate mostly in the low power region. In those applications, efficiency boosting at the low power region will be very important.

Numerous methods to increase the efficiency in linear amplifiers have been reported. Notable approaches that have been studied and implemented include a Doherty amplifier [1], a PA with a dc–dc converter [2], a PA with low-power/high-power mode selection [3], [4], and an adaptive biasing PA [5].

PAs for polar transmitters are switching-mode amplifiers, which are different from linear PAs. The switching-mode amplifiers operate at the saturated region, and the envelope information is loaded through linear regulators such as low dropout (LDO) regulators or dc–dc converters [6], [7]. In polar transmitters, the low power output region corresponds precisely to the low supply-voltage region. Therefore, it is important to increase the efficiency at the low supply voltage. The efficiency boosting approach can also be distinguished from those in linear PAs because the input power is fixed and the supply voltage varies unlike linear PAs. The other significant requirement in polar transmitters is the wide dynamic range of output power controlled by the supply voltage. Theoretically, the dynamic range from 0.5 to 3.3 V of the supply voltage is only 16.4 dB [8]. To meet the dynamic-range specification, additional techniques are required to overcome the theoretical dynamic-range limitation [9].

In this paper, a new PA for polar transmitters is proposed. The proposed amplifier shows high efficiency at the low output power region. The cascode amplifier, whose common-gate (CG) transistor is biased at constant gate voltage, provides an efficiency boosting characteristic as the supply voltage decreases. It is presented in Section II. Equations for differential class-E amplifier design are derived in Section III. The PA with low power efficiency boosting is described from concept to implementation in Sections IV–VI. Measured results are presented and compared in Section VII, followed by conclusions in Section VIII.

II. Cascode Amplifier With Drain Efficiency Boosting

The design of a watt-level CMOS PA becomes more difficult as technology scales down due to the reduction of the supply voltage and the load resistance. Therefore, for 0.25-μm or less CMOS technology, the cascode configuration is preferred in order to relieve the pressure on the supply voltage [10]–[12]. Even though we use a cascode configuration in this study, the maximum reliable supply voltage is not enough in 0.18-μm CMOS technology. In order not to exceed the maximum reliable voltage, a self-biased cascode configuration was presented [11].

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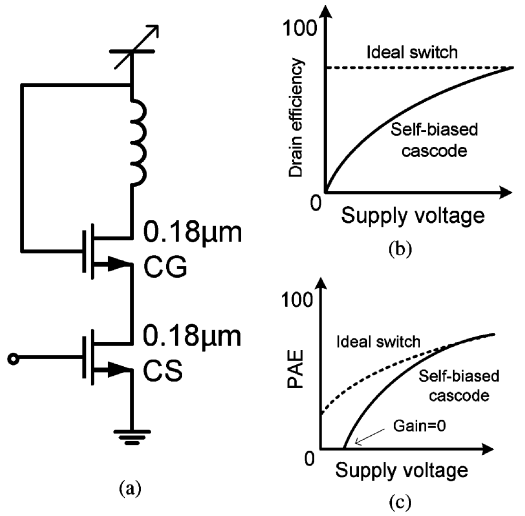

Fig. 1. (a) Self-biased cascode amplifier. (b) Drain efficiency versus supply voltage. (c) PAE versus supply voltage.

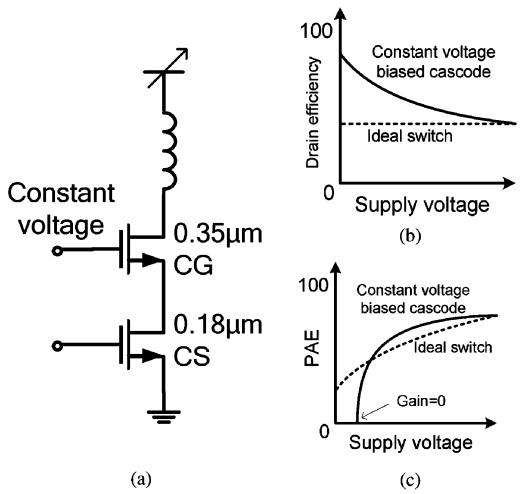

Fig. 2. (a) Constant gate voltage biased cascode amplifier. (b) Drain efficiency versus supply voltage. (c) PAE versus supply voltage.

In this case, both the common-source (CS) and CG transistors have a minimum gate length of 0.18 μm. The self-biased cascode configuration assures that the maximum voltage is under the maximum reliable voltage. However, this configuration decreases the drain efficiency and power-added efficiency (PAE) at the low supply-voltage region, as shown in Fig. 1. As the supply voltage decreases, the gate–source voltage of the CG transistor also decreases, and the on-resistance ($R_{\rm ON}$) of the CG transistor then increases. The increasing $R_{\rm ON}$ indicates an increasing series resistance in the cascode amplifier. Therefore, the efficiency of the cascode amplifier is degraded as the supply voltage is decreased.

By replacing the 0.18-μm nMOS of the CG transistor with a 0.35-μm-thick oxide NMOS, an additional margin of the maximum voltage can be obtained. Therefore, we adopt the 0.18-μm nMOS as the CS transistor and the 0.35-μm nMOS as the CG transistor, as shown in Fig. 2(a). With constant gate voltage biasing of the CG transistor, as the supply voltage goes down, the source voltage of the CG transistor also decreases. Since the gate voltage is fixed, the gate–source voltage of the CG transistor rises. This means that the $R_{\rm ON}$ of the CG transistor decreases as the supply voltage decreases. Eventually, a drain efficiency boosting phenomenon is observed at the low supply voltage, as illustrated in Fig. 2(b). The PAE of the constant gate voltage biased cascode amplifier is illustrated in Fig. 2(c). The zero crossing point refers to the zero gain point of the amplifier.

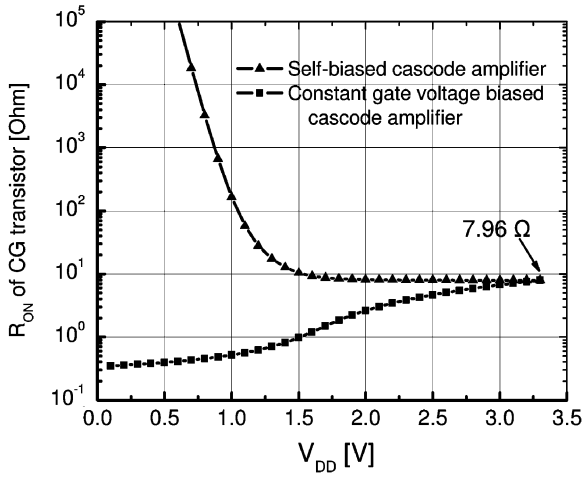

Fig. 3. Simulated on resistance of CG transistors in cascode amplifiers versus supply voltage.

Fig. 3 shows the simulated $R_{\rm ON}$ of the CG transistors in the self-biased cascode amplifier and the constant gate voltage biased cascode amplifier. Both gatewidths of the CG and CS transistors in the amplifiers are 4 mm. As expected, the $R_{\rm ON}$ of the CG transistor in the self-biased cascode amplifier goes up over a few hundred kiloohms, and the $R_{\rm ON}$ of the CG transistors in the constant gate voltage biased cascode amplifier decreases from 7.96 to 0.35 Ω as the supply voltage decreases from 3.3 to 0.1 V.

III. Differential Class-E Amplifier With Parallel Resonant Circuit

Class-E amplifiers have been widely applied to microwave PAs due to their high efficiency at high frequency and simple configuration [13]. The operation of these amplifiers was analyzed and the output network design equations were derived by Raab [14], [15]. A single-ended class-E PA topology is given in Fig. 4(a). C_S and L_S are derived from the zero voltage switching (ZVS) condition, and L_0 and C_0 are determined by the loaded quality factor Q_L.

A single-ended class-E amplifier can be transformed to the differential class-E amplifier, as shown in Fig. 4(b). When the ratio of reactance to resistance of the differential class-E output network is the same as that of the single-ended one, the differential amplifier can operate as a class-E amplifier. The series resonant filter (L_0, C_0) and the series *RL* circuit (R_S, L_S) in the single-ended class-E amplifier can be transformed to a parallel resonant filter (L_{0P}, C_{0P}) and a parallel *RL* circuit (R_P, L_P) in the differential class-E, respectively. The series *RL* circuit can be transformed to a parallel *RL* circuit, as shown in Fig. 5. R_S

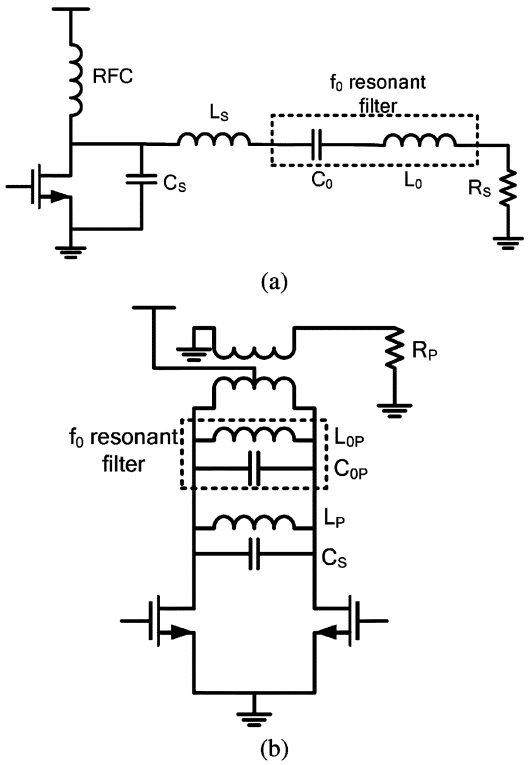

Fig. 4. (a) Single-ended class-E amplifier. (b) Differential class-E amplifier with a parallel resonant circuit.

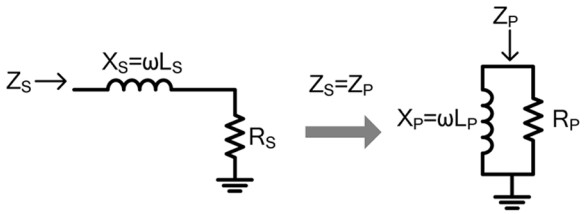

Fig. 5. Transforming a series *RL* circuit to a parallel *RL* circuit ($X_S = \omega L_S, X_P = \omega L_P$).

and X_S in the single-ended class-E amplifier can be transformed as follows:

$$R_P = \frac{\pi^4 - 12\pi^2 + 64}{32\pi\omega Cs} \tag{1}$$

$$X_P = \omega L_P = \frac{\pi^4 - 12\pi^2 + 64}{2\pi^2\omega Cs(\pi^2 - 4)} = \frac{16R_P}{\pi(\pi^2 - 4)}. \tag{2}$$

Using C_S from (1), P_O becomes

$$P_O = \pi\omega C_S V_{\mathrm{DC}}^2 = \frac{\pi^4 - 12\pi^2 + 64}{32}\frac{V_{\mathrm{DC}}^2}{R_P} = 1.343\frac{V_{\mathrm{DC}}^2}{R_P}. \tag{3}$$

From (2) and (3), L_P and C_S can be expressed as

$$L_P = 0.8677\frac{R_P}{\omega} \tag{4}$$

and

$$C_S = 0.4275\frac{1}{\omega R_P}. \tag{5}$$

The parallel resonant circuit is defined as follows:

$$L_{0P} = \frac{R_P}{\omega Q_L} \tag{6}$$

$$C_{0P} = \frac{Q_L}{\omega R_P} \tag{7}$$

where Q_L is the loaded quality factor of the parallel resonant circuit.

We can choose innumerable sets of L_{0P} and C_{0P} as Q_L. Moreover, L_P and C_S can be merged into the parallel resonant circuit components L_{0P} and C_{0P}, respectively. Therefore, we are able to design a differential class-E amplifier with a large degree of freedom with the selection of L and C. Moreover, the required inductance can be replaced with the inductance of the output transformer. Therefore, the output network can be simplified by only a shunt capacitor (C_S) and an output transformer.

IV. Load-Shared Configuration

PAs with a switched gain stage and an appended PA aim for improving efficiency at the low power region in Fig. 6 [3], [4]. At low power operation, the PA with a switched gain stage bypasses the output transistor through a switch between the input and output of the output transistor, while the output transistor is off. Therefore, the driver transistor operates alone with power saving of the output transistor. In the appended PA, the switch is replaced with a small appended transistor. In the high power mode, both the output transistor and appended transistor operate, while in the low power mode, only the appended transistor operates with the output transistor turned off. Therefore, the power consumption by the output transistor can be reduced in the low power mode. The PA with a switched gain stage requires a low loss switch in order to minimize loss of the output power and prevent oscillation via the feedback path. The appended PA requires a matching network to satisfy both modes; however, it is not easy to find the matching network.

A distributed active transformer (DAT) is the effective power-combining method that is used with several push–pull amplifiers [16]–[18]. With magnetic couplings of the DAT, the differential signals are combined and the output impedance is transformed to 50 Ω without the aid of off-chip components such as inductors, capacitors, bond wires, or microstrip lines. Moreover, the virtual ac grounds from the differential configuration desensitize the amplifier operation from bond wire variation. The DAT has been used as a power-combining structure in the load-shared PA for its advantages.

The concept of the proposed load-shared PA is shown in Fig. 7. This is a variation of the PA with a switched gain stage. The switch was replaced by a transformer and an inductor L_A. The PA output impedance is low and the DA output impedance is relatively high because the output impedance depends on the transistor size. Adding an additional inductance, i.e., L_A,

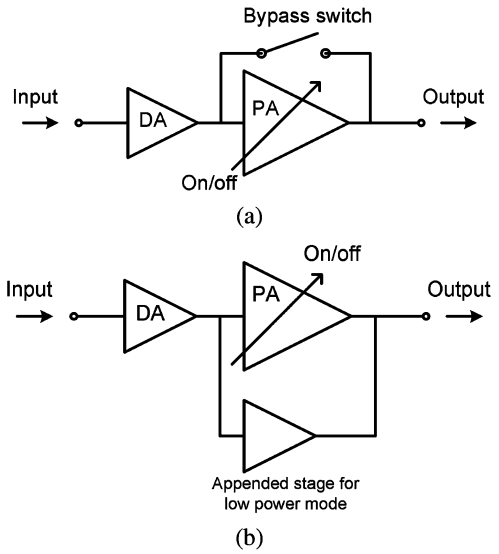

Fig. 6. (a) PA with a switched gain stage. (b) Appended PA.

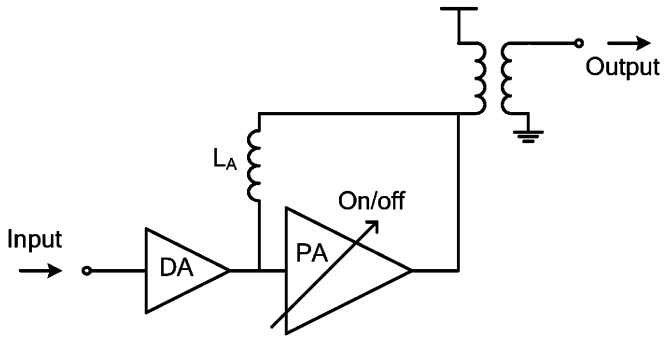

Fig. 7. Concept of load-shared PA.

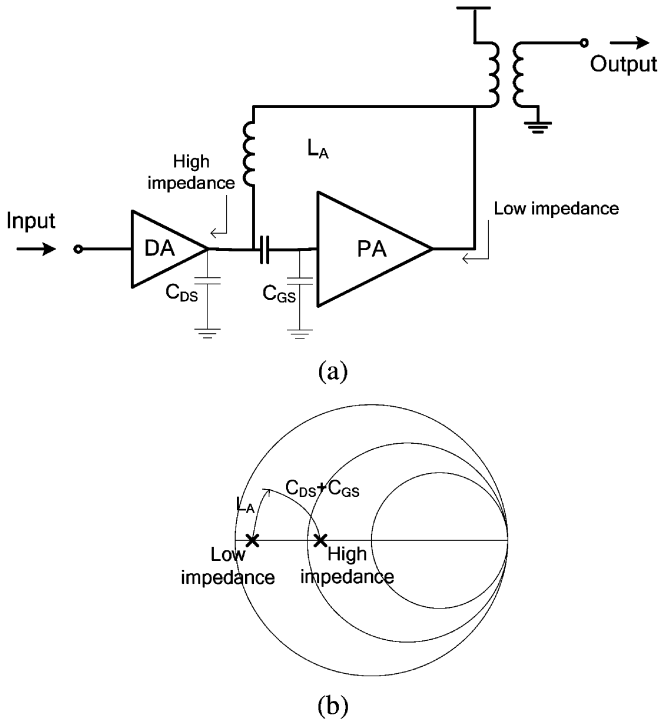

Fig. 8. (a) Load-shared PA with output impedance illustration. (b) Impedance transforming mechanism.

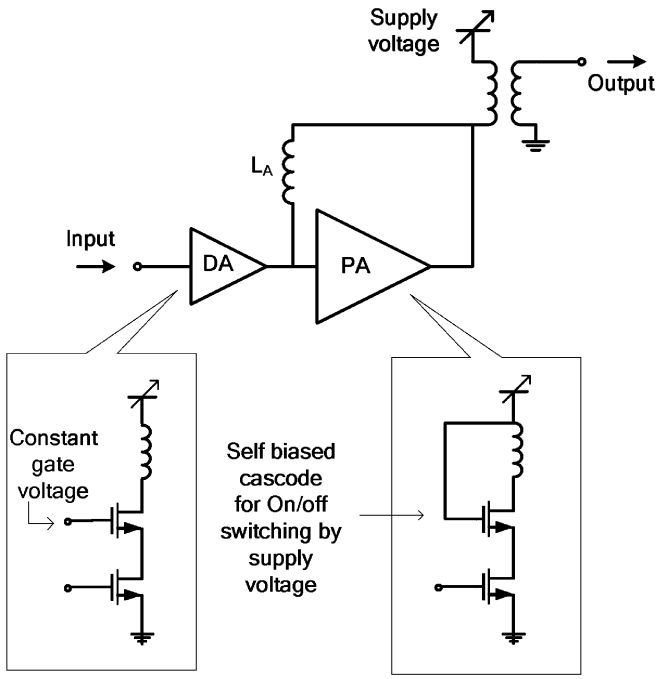

Fig. 9. Load-shared PA using cascode amplifiers.

we can transform the PA output impedance to the DA output impedance. As shown in Fig. 8, a series inductor L_A and shunt capacitors $C_{\rm DS}$ and $C_{\rm GS}$, which are the intrinsic capacitors of the transistors, transform low impedance to high impedance on the Smith chart [19].

The feedback loop between the input and output of the PA may cause the PA to be unstable. This is called mode locking [20], [21]. Mode locking is based on injection-locking oscillators, which feature self-oscillation. The operating frequency is locked with the same frequency as the input signal. Furthermore, the self-oscillation helps to reduce the phase and amplitude errors of differential signals. As a result, the even harmonics, especially the second harmonic, are largely suppressed at the output of the differential structure.

The on/off function of the PA must be operated by the supply voltage for polar transmitters. It is realized with the self-biased cascode amplifier described in Section II. The PA can be turned off naturally as the supply voltage decreases because the series resistance of the CG transistor grows. The DA adopts the constant gate voltage biased cascode amplifier to improve efficiency at low supply voltage, as shown in Fig. 9.

V. Output Transformer Layout and Simulation

The output transformer combines the output power from four differential PAs and DAs with a load-shared configuration. The output transformer is a DAT that has a circular geometry [16]–[18]. Fig. 10 shows a 41-port electromagnetic (EM) simulation layout. Two pairs of PAs are connected to the inner primary winding, and the other two pairs are connected to the

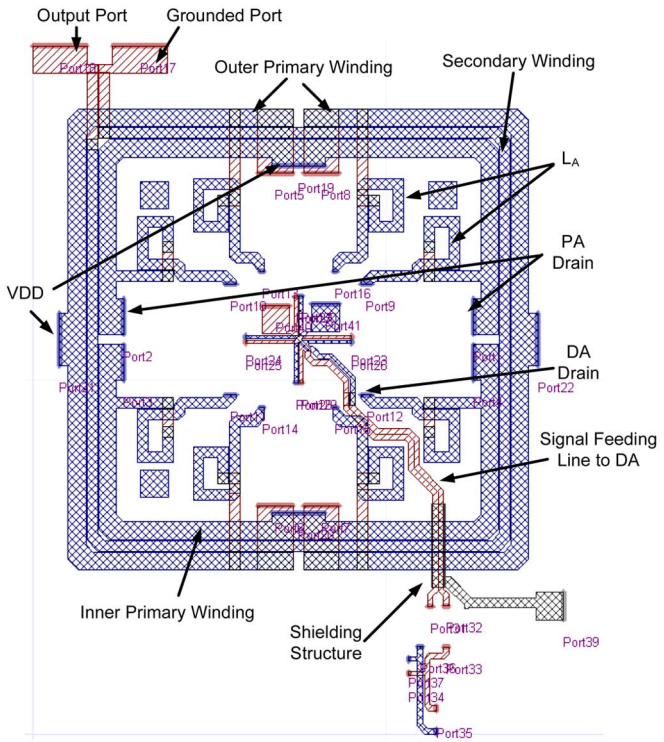

Fig. 10. Output transformer, inductors, and interconnect lines for EM simulation.

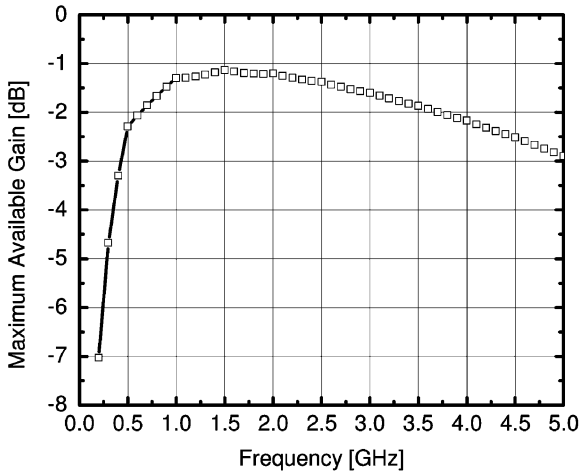

Fig. 11. MAG of output transformer.

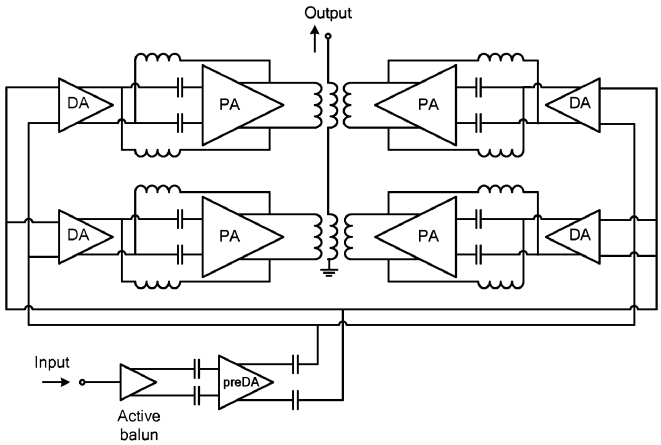

Fig. 12. Total block diagram of the load-shared PA.

outer primary winding, and the secondary winding is the middle metal line with a grounded port. DAs are also connected to the primary winding through L_A's. The four pairs of amplifiers operate symmetrically. The width of the primary winding is 50 μm, the width of the secondary winding is 30 μm, and the spacing between the windings is 3 μm. The lengths of the outer and inner primary windings are 1.2 and 1.13 mm, respectively. The stacked metal, which is stacked with M5 and M6 (top metal) through vias, is used for the DAT to reduce the series resistance. The effective metal thickness is 2.87 μm, which is the sum of the thickness of M5 and M6 excluding the via height because of its vertical current direction through the via.

Accurate EM simulation is crucial to analyze the amplifiers with integrated output transformers. For accurate EM simulation, the physical parameters must first be extracted exactly. The characteristics of the integrated inductors and transformers are determined by the physical and material parameters, including the thickness and conductivity of the metal lines, the permittivity and thickness of the dielectric materials, and the conductivity of the substrate [22]. The inductor implemented on the Si substrate is strongly affected by the substrate parameters, owing to its high substrate conductance. In general, the physical parameters provided by foundries are not sufficient to obtain accurate EM simulation results. We extracted the exact physical parameters by comparing the S-parameters from inductor models with the extracted S-parameters from EM simulation of the inductors. The parameter extraction was performed by using Ansoft Designer, a 2.5-D EM simulator. From the simulation of the DAT, the inductances of the outer and inner primary windings are 1.69 and 1.33 nH, respectively. The secondary winding has 3.58 nH and L_A has 0.32 nH. The minimum passive loss of the DAT is 1.207 dB at 1.88 GHz, which comes from the simulation with maximum available gain (MAG), as shown in Fig. 11.

Finally, the output transformer, additional inductors, L_A, and interconnect lines are simulated excluding any active and passive devices whose models are given by the foundry. Top cell circuits are simulated in Agilent's Advanced Design System (ADS) with the EM simulation data.

VI. Design of Load–Shared PA

A PA for polar transmitters has been designed using 0.18-μm CMOS technology with a 2.34-μm-thick aluminum top metal. A fully differential configuration is used to alleviate some of the issues in CMOS technology. The problem of substrate coupling is relieved because there is less injection of common mode noise into the substrate. Moreover, the greatest benefits of differential structures are the absence of gain degradation and immunity against bond wires [20].

Four pairs of PAs are used to achieve 32-dBm output power for 1.8-GHz polar transmitter applications. For example, GSM requires a dynamic range of 30 dB for power level control. EDGE requires a dynamic range of 47 dB including a peak to minimum ratio (PMR) of 17 dB. The 1.8-GHz GSM band covers from 1850 to 1910 MHz of frequency band.

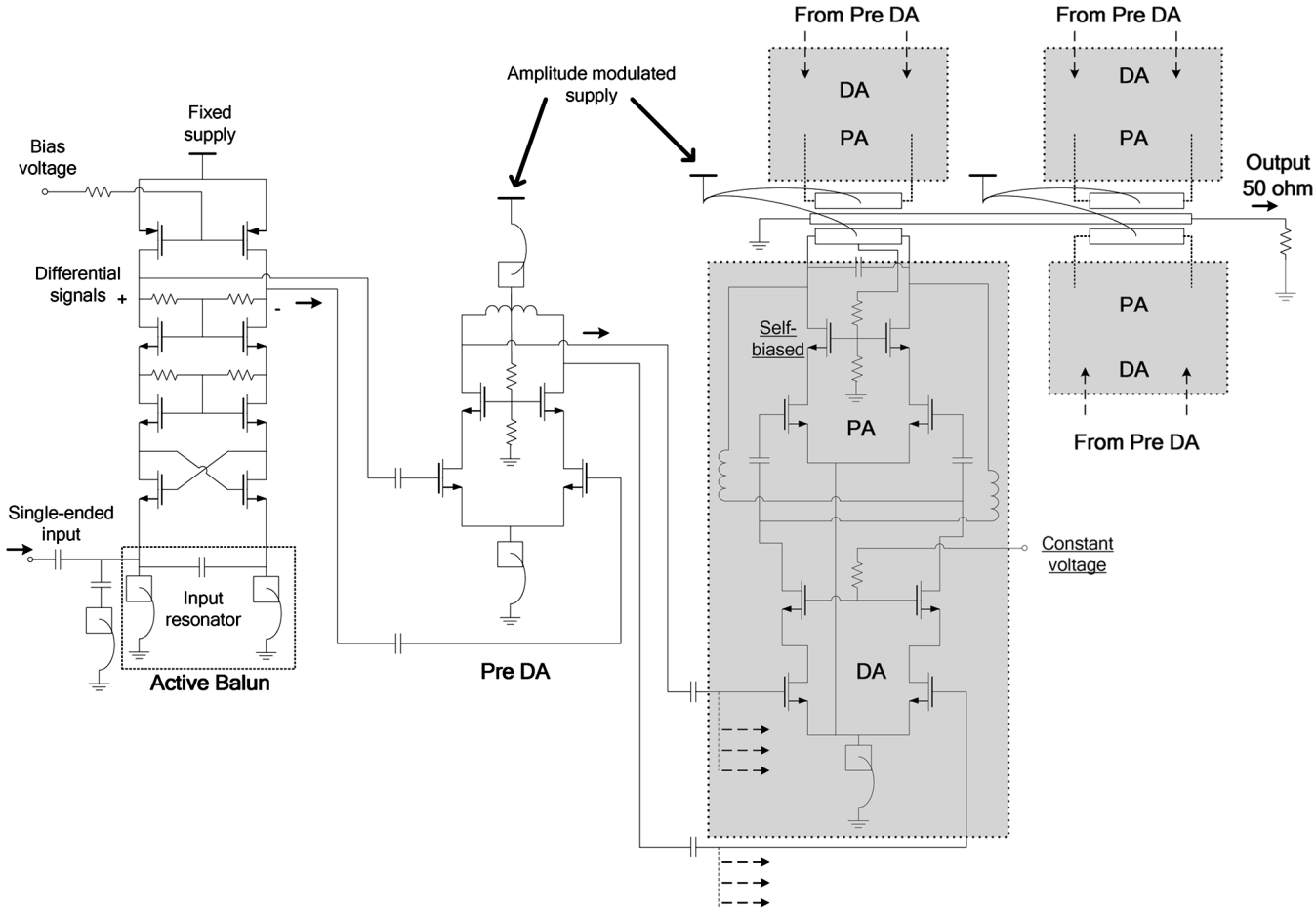

Fig. 13. Schematic of the load-shared PA. Bias conditions and circuits are partially omitted.

The core of the load-shared PA is composed of driver amplifiers (DAs) and PAs with the shared load. To achieve more than 30 dB of power gain, a pre-amplifier (preDA) was added next to an active balun. The entire block diagram is illustrated in Fig. 12. One of the PAs is a differential cascode amplifier having 0.18-μm nMOS CS amplifiers and 0.35-μm-thick oxide nMOS CG amplifiers. The total gatewidth of each device, which is half of one pair, is 4 mm. The four pairs of PAs are identical and the gate of the CG amplifier is self-biased, as described in Section IV. The DA is also a differential cascode amplifier, which is also composed of 0.18-μm nMOS CS amplifiers and 0.35-μm-thick oxide nMOS CG amplifiers, but the gate of the CG amplifier is biased at constant voltage in order to obtain an efficiency boosting effect at a low supply condition.

The preDA is a differential cascode amplifier with an on-chip differential inductor load, and its CG amplifier is self-biased to increase the dynamic range. The active balun is composed of a gate–drain cross-coupled stage and two stacked differential CG amplifiers with an input *LC* resonator using bond wires. The input resonator generates differential signals, and the gate–drain cross-coupled stage amplifies the differential signals and reduces the balance errors with a latch operation. The stacked CG amplifiers increase gain by increasing the output impedance. The measurement results of the active balun showed a gain of 9.3 dB at 1.8 GHz, and phase and amplitude errors of less than 2° and 1 dB, respectively, from 1.0 to 1.96 GHz [23]. A schematic of the load-shared PA is shown in Fig. 13.

Four pairs of PAs and DAs are connected to the DAT, as mentioned in Section V. To meet the symmetric operation condition, the inductance difference between the inner primary winding and the outer primary winding is compensated by shunt capacitors of differential class-E amplifiers. To increase the isolation between the DAT and feeding lines from the preDA, and to prevent redundant feedback, the shielding structure has been adopted under the DAT, as shown in Fig. 14 [24], [25]. The shielding structure shields signal lines (M2) against the DAT (M5–M6) with the upper metal (M3), bottom metal (M1), and via walls (V12–M2–V23). The shielding structure is grounded through a bond wire. The minimum isolation between the feeding lines and the DAT was simulated with MAG. The minimum isolation of the shielded structure is 21.0 dB, while the minimum isolation of the nonshielded structure is 17.3 dB, as shown in Fig. 15. The shielded structure shows a 3.7-dB improvement of the minimum isolation.

VII. Measurement

A microphotograph of the fabricated chip is shown in Fig. 16. The die area is 2×1.5 mm^2 including the output DAT. The PA was measured in two ways. First, the core of the load-shared PA,

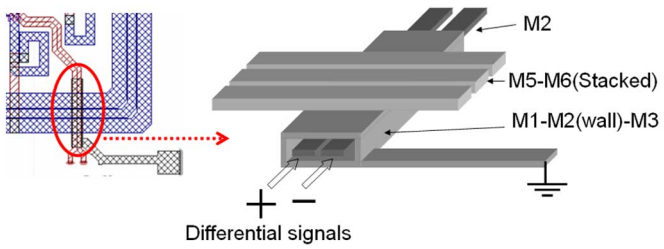

Fig. 14. Shielding structure between the preDA and DAT.

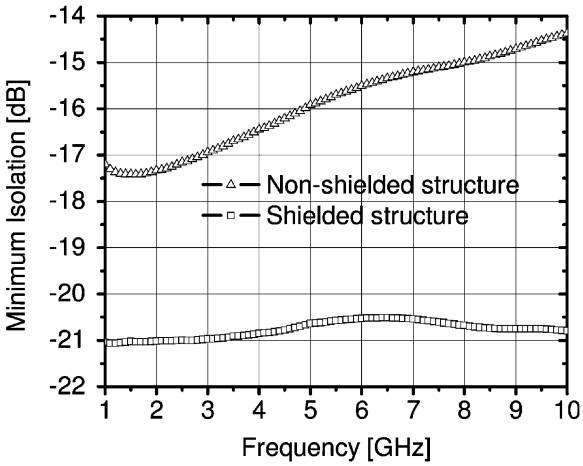

Fig. 15. Minimum isolation comparison between the shielded structure and the nonshielded structure using MAG.

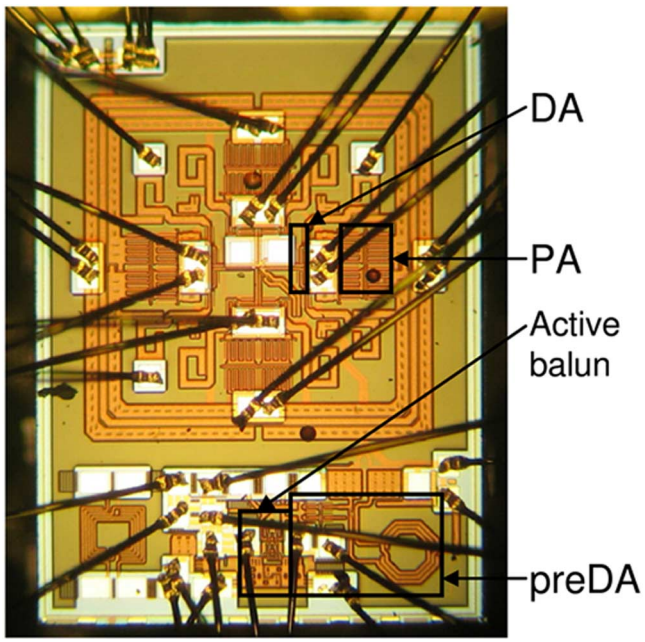

Fig. 16. Microphotograph of the load-shared PA.

which is composed of the DAs and the PAs with an input transformer, is measured in order to verify the efficiency enhancement in the low power range. Second, the total load-shared PA including the active balun and preDA is measured. To prove the efficiency improvement, self-biased amplifiers, where both the

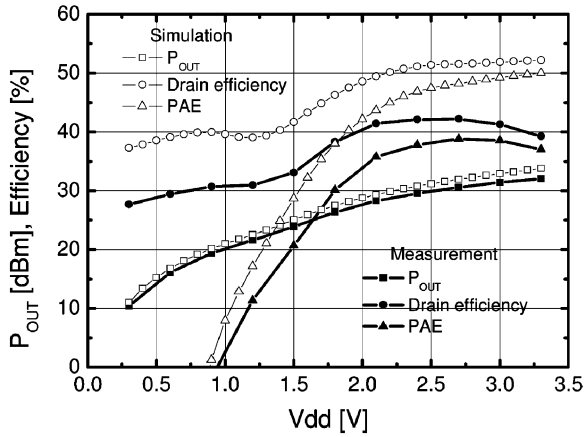

Fig. 17. Measured and simulated P_{OUT}, drain efficiency, and PAE versus V_{DD} for the DA and PA with input transformer (P_{IN} of 20 dBm, operation frequency of 1.88 GHz).

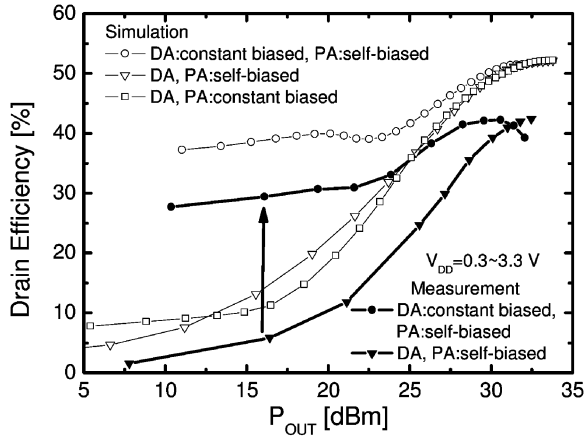

Fig. 18. Measured and simulated efficiency versus P_{OUT} for the DA and PA with input transformer. DAs with a constant voltage biased cascode configuration and PAs with a self-biased cascode configuration (●). DAs with a self-biased cascode configuration and PAs with a self-biased cascode configuration (▼) (P_{IN} of 20 dBm, operation frequency of 1.88 GHz).

DA and PA are self-biased cascode amplifiers, were also measured as a reference.

A. DA and PA With Input Transformer

First, the core amplifier composed of DAs, PAs, and an input passive transformer is measured. The DAs are constant gate voltage biased cascode amplifiers and the PAs are self-biased cascode amplifiers, similar to the load-shared PA. To verify the efficiency boosting phenomenon, the active balun and preDA were excluded in this measurement. The core amplifier was operated at the fully saturated region with 20 dBm of input power. At 1.88 GHz of the personal communications system (PCS) band, the output power, drain efficiency, and PAE versus supply voltage (0.3–3.3 V) were measured, and the results are presented in Fig. 17 with simulation results. The drain efficiency is calculated from the ratio of the output power to the dc power consumption of both the PA and DA. At 1.5-V supply voltage, the PA enters the turn-off mode as the supply voltage decreases, and the DA operates alone. The drain efficiency remains high under 1.5-V supply voltage. The disagreement

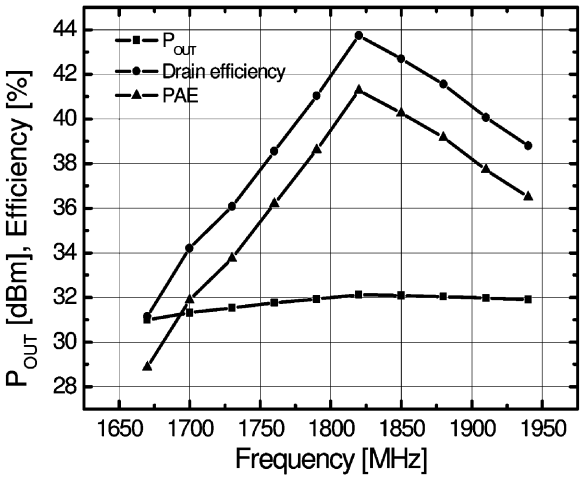

Fig. 19. Measured $P_{\rm OUT}$, drain efficiency, and PAE versus frequency for the DA and PA with input transformer ($P_{\rm IN}$ of 20 dBm).

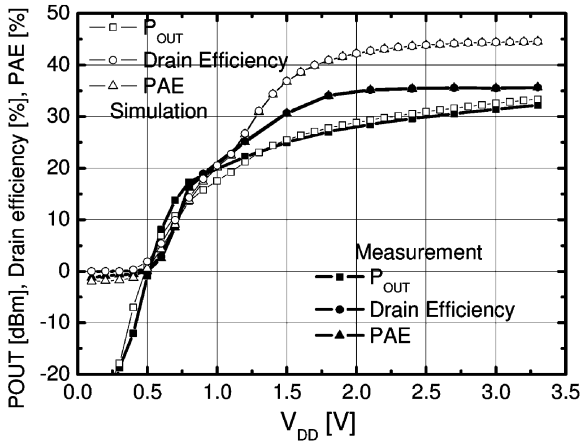

Fig. 20. Measured and simulated $P_{\rm OUT}$, drain efficiency, and PAE versus V_{DD} of the load-shared PA ($P_{\rm IN}$ of 0 dBm, operation frequency of 1.88 GHz).

between the simulation and measurement comes from the DAT EM simulation of which loss have been underestimated by 1 dB. Fig. 18 shows a drain efficiency comparison between the core amplifier of the load-shared PA, the self-biased amplifier, and the constant biased amplifier in simulations and measurements. In the self-biased amplifier, both DAs and PAs have self-biased cascode configurations with the same DAT [11], [12]. In the constant biased amplifier, both DAs and PAs have constant gate voltage biased cascode configurations with the same DAT. From Fig. 18, it is seen that the measured drain efficiency of the load-shared PA at 16 dBm of $P_{\rm OUT}$ was dramatically enhanced from 6% to 30% compared with the self-biased amplifier. Fig. 19 shows $P_{\rm OUT}$, drain efficiency, and PAE versus frequency. The measured peak $P_{\rm OUT}$, peak drain efficiency, and peak PAE are 32.1 dBm, 43.7%, and 41.2%, respectively, at 1.82 GHz.

B. Total Load-Shared PA

Finally, the total load-shared PA, which is composed of DAs, PAs, a preDA, and an active balun, was measured. At 1.88 GHz, the output power, drain efficiency, and PAE versus

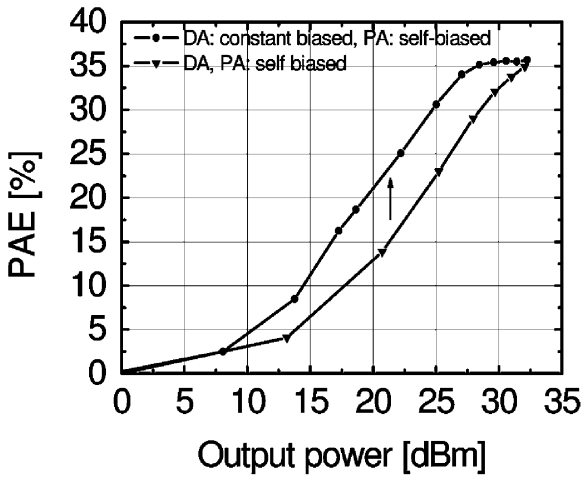

Fig. 21. Measured PAE versus output power comparison. DAs with a self-biased cascode configuration and PAs with a constant voltage biased cascode configuration (•). DAs with a self-biased cascode configuration and PAs with a self-biased cascode configuration (▼) ($P_{\rm IN}$ of 0 dBm, operation frequency of 1.88 GHz).

supply voltage (0.3–3.3 V) were measured, and the results are presented in Fig. 20 with simulation results. The mismatch comes from the 1-dB underestimated DAT loss. The measured peak output power and peak drain efficiency were 32.2 dBm and 35.6%, respectively, at 1.88 GHz with 0-dBm input power. A dynamic range of 44 dB was achieved from 0.4 to 3.3 V of supply voltage. Fig. 21 shows the measured PAEs versus output power for two types of total PAs. One is the load-shared PA, which is composed of DAs with a constant gate voltage biased cascode configuration and PAs with a self-biased cascode configuration, and the other is a self-biased amplifier where both of the DAs and PAs have self-biased cascode configurations. As was verified in Section VII-A, the load-shared PA shows a maximally 8% improved PAE in a wide output power range.

VIII. Conclusion

A fully integrated PA for 1.8-GHz polar transmitters was designed and fabricated using TSMC 0.18-μm CMOS technology. The last two stages of the proposed PA share the load through additional inductors. With the load-shared configuration and a constant gate voltage biasing of a cascode amplifier for a DA, the amplifier has an efficiency boosting characteristic at low output power. To eliminate the bulky input transformer, an active balun using bond wires was incorporated. The core amplifier of the load-shared PA achieves drain efficiency improvement from 6% to 30% at 16 dBm of $P_{\rm OUT}$. Finally, the load-shared PA achieved a 32.2 dBm of $P_{\rm OUT}$, 35.6% of PAE, and a 44-dB dynamic range from 0.4 to 3.3 V of supply voltage. This paper demonstrated that the efficiency boosting technique is applicable to PAs for polar transmitter applications.

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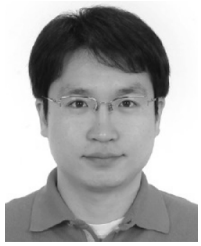

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