

5.8GHz ETC SiGe-MMIC Transceiver

having Improved PA-VCO Isolation with Thin Silicon Substrate

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Abstract — A fully integrated SiGe-MMIC transceiver having a power amplifier (PA), a transmit / receive switch (T/R SW), and a voltage controlled oscillator (VCO) is developed for electric toll collection system (ETC) terminals. To improve the isolation between the PA and the VCO, the back-polish technique of the silicon substrate (127 μ m thickness) is employed. Electro-magnetic simulation shows that a MMIC of 127 μ m thickness achieves the isolation improvement of 12.3dB compared with that of conventional 300 μ m thickness. As a result, the USB/LSB unbalance of the transmitted amplitude shift keying (ASK) signal can be reduced from 4.2dB to 1.2dB at 13dBm output power. The MMIC transceiver fabricated in 0.35 μ m SiGe BiCMOS process achieves the maximum output power of 15.5dBm with the adjacent channel power ratio (ACPR) of -33.5dBc.

Index Terms — MMICs, power amplifiers, silicon, switches, transceivers, voltage controlled oscillators.

I. INTRODUCTION

Since the ETC uses ASK modulation scheme, an on-chip VCO tends to be modulated by the envelope of the transmitted ASK signal. Consequently, the modulated characteristics (i.e. USB/LSB unbalance, ACPR and eye-pattern) are degraded [1]. Even if the shielding grounded-metal with the substrate contact protects the leakage through the channel layer, it is difficult for a MMIC of conventional 300 μ m thickness to achieve the expected modulated characteristics at the 13dBm output power [2]. Therefore, the interference between a 20mW output PA and an on-chip VCO is a problem for the fully integrated single-chip transceiver. To solve the interference problem, the layout approaches, such as shielding grounded-metals and guard rings with deep trench, have been employed [1], [3]-[6]. The uses of high resistivity silicon substrate, silicon-on-insulator, and silicon-on sapphire were also reported [5]-[7].

In the case of a T/R SW integration, single RF interface is desired for the transceiver chip and it requires a single-ended (single RF output) on-chip matching PA. This circuit configuration having single RF interface makes the interference problem tough.

In this paper, the fully integrated SiGe-MMIC transceiver including with a PA, a T/R SW and a VCO is developed for ETC terminals. To suppress the USB/LSB unbalance of the transmitted ASK signal, the isolation between the PA and the

VCO should be improved. The relationship between silicon substrate thickness and the isolation is analyzed based on the electro-magnetic simulation [3]-[6], [8]. The simulated result shows that the MMIC transceiver with thin silicon substrate has higher isolation, and the substrate thickness is determined as 127 μ m with considering of the chip handling easiness. The developed MMIC transceiver achieves the maximum output power of 15.5dBm with the ACPR of -33.5dBc in transmitter (T_x), the input 1dB compression point (P_{1dB}) of -33.1dBm, the DSB NF of 11.2dB and the conversion gain of 22.0dB in receiver (R_x).

II. ARCHITECTURE AND CIRCUIT ISSUE

A. Architecture

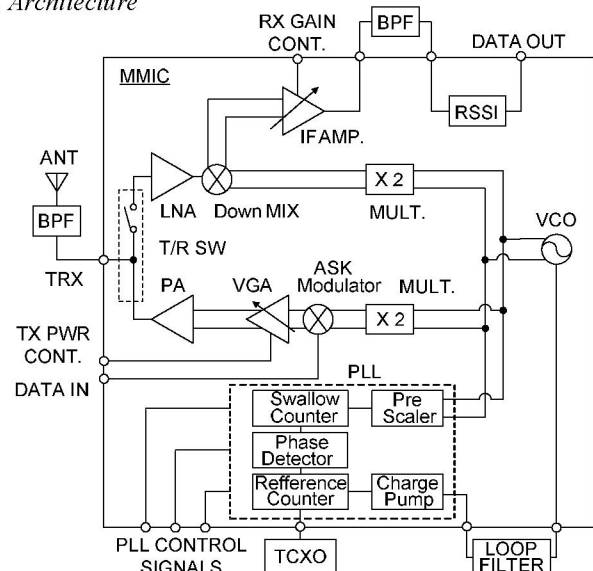


Fig. 1. Architecture of the MMIC transceiver.

Figure 1 shows the architecture of the MMIC transceiver. The T_x path consists of five-stage single-ended PA, variable gain amplifier (VGA), and ASK modulator. The R_x path is

consists of T/R SW, single-input two-stage low noise amplifier (LNA), down mixer, single-ended IF amplifier and RSSI.

B. ASK Modulator

Figure 2 shows the schematic of ASK modulator. The ASK modulator is comprised of a differential transistor pair (Q_1, Q_2) for carrier signal, a lower transistor (Q_3) for base-band signal, and a control section. The control section includes a conversion circuit from voltage to current, a subtracter, and a square circuit. By employment of this control section, the output voltage is proportional to base-band signal, and high control accuracy and high linearity can be realized.

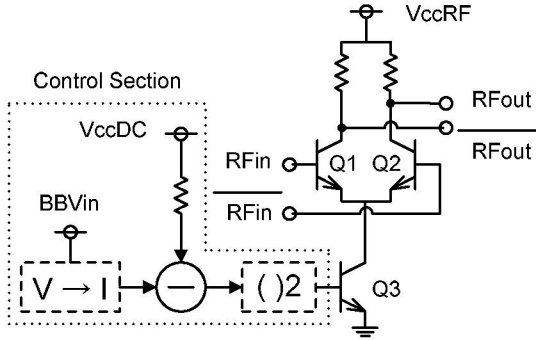


Fig. 2. Schematic of ASK modulator.

Figure 3 shows the measured output voltage (V_{out}) of block with ASK modulator and VGA versus base-band signal (BBV_{in}). It is shown in Fig.3 that V_{out} is proportional to BBV_{in} over the range of 0 to 1V at the all conditions of the VGA control voltage.

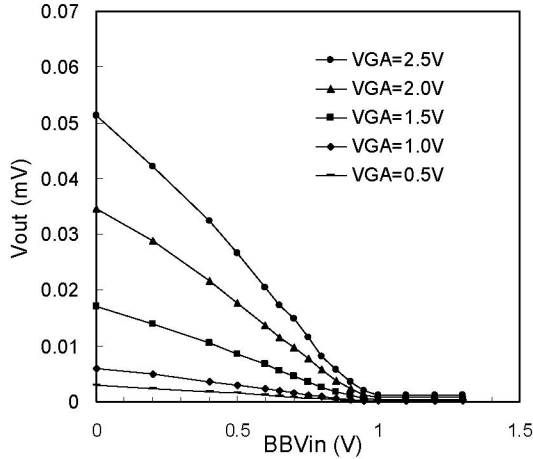


Fig. 3. Measured V_{out} of block with ASK modulator and VGA versus BBV_{in} .

C. PA and T/R SW

Figure 4 shows the block diagram of PA and T/R SW, and Fig.5 shows the schematic of unit amplifier. The T/R SW is comprised of a n-MOSFET and an inverter circuit. When T_x is on-state, the power save voltage (V_{ps}) is 3.3V, and the T/R SW

becomes open-state. The T/R SW is inserted in only R_x path not to increase the output loss in T_x .

The only final-stage PA has single-ended output configuration to connect with the T/R SW, although the almost all the T_x circuits are differential. The differential to single conversion is realized by terminating one of differential signal as shown in Fig.4. The resistor (R_1) for termination is optimized to realize high output power. Moreover the on-chip output matching section, which uses a spiral inductor (L_1, L_1') and two capacitors (C_1, C_2) as shown in Fig.4 and Fig.5, is designed to realize the optimum impedance for both output power in T_x and noise figure (NF) in R_x . The PA employs the emitter-grounded differential amplifier to improve the saturation characteristic as shown in Fig.5. In this circuit configuration, the unbalance of input differential signals is greatly influenced at the view of the linear gain and the output power because the in-phase remove ratio is extremely low. Therefore the resistor feed (R_2, R_2'), which can suppress the effect of unbalance, is employed. The fabricated five-stage PA achieves the output P_{1dB} of 15.8dBm and the linear gain of 30.8dB.

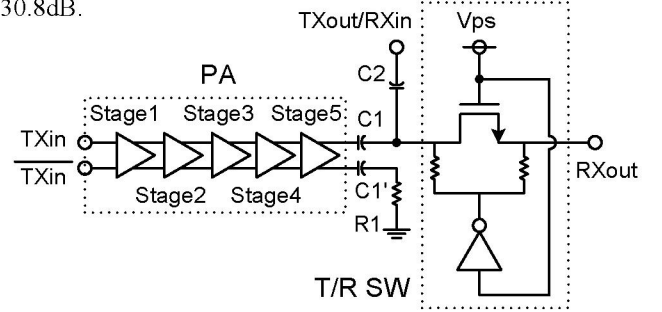


Fig. 4. Block diagram of PA and T/R SW ($C_1 = C_1' = 2.5\text{pF}$, $C_2 = 1.0\text{pF}$, $R_1 = 50\text{ohm}$).

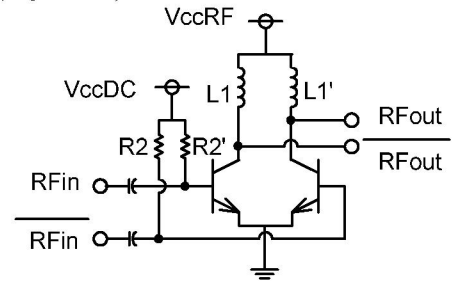


Fig. 5. Schematic of unit amplifier ($L_1 = L_1' = 0.95\text{nH}$).

D. Isolation between PA and VCO

Since the ETC uses ASK modulation scheme with sharply fluctuation of enveloped signal, some techniques to relax the interference problem between the PA and the VCO are needed. Firstly, the 2.9GHz VCO, which is a half of RF, is employed. Secondary, the PA and the VCO are arranged at the orthogonal of the MMIC to separate each other. Thirdly, the shielding ground-metal with the substrate contact is introduced to protect the leakage through the channel layer. However, the interference between the 20mW PA and the on-chip VCO was

still observed due to the leakage through the low resistivity silicon substrate ($10 \Omega\text{-cm}$).

Figure 7 shows the simulated isolation between the PA and the VCO versus the silicon substrate thickness, which is carried out by using the electro-magnetic simulator HFSS. Figure 8 shows the simulated pattern. The chip size is $2.9\text{mm} \times 3.6\text{mm}$, and the electrodes size is $85\mu\text{m} \times 85\mu\text{m}$. Assuming that the shielding grounded-metal protects the leakage of channel layer, the simplified model as shown in Fig.8 is used. As shown in Fig.7, the isolation greatly depends on the silicon substrate thickness. When the silicon substrate thickness is decreased from $300\mu\text{m}$ to $127\mu\text{m}$, the isolation improvement of 12.3dB is realized. With considering chip handling easiness, the silicon substrate thickness of $127\mu\text{m}$ is chosen in this work.

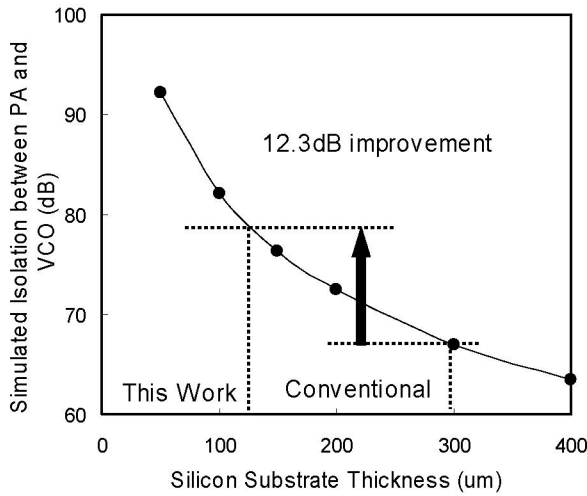


Fig. 7. Simulated isolation between PA and VCO.

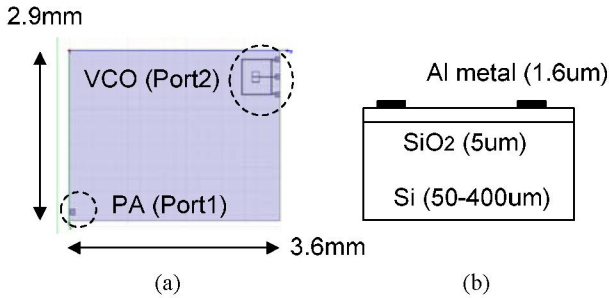


Fig. 8. Simulated pattern. (a) top view, (b) cross section.

III. EXPERIMENTAL RESULTS

The MMIC transceiver was implemented by using $0.35\mu\text{m}$ SiGe BiCMOS process. Figure 9 shows the die photograph. The chip size is $2.9\text{mm} \times 3.6\text{mm}$.

Figure 10 shows the measured T_x characteristics at ASK modulation condition. The output power, the eye-open, the on/off ratio, and ACPR are shown at the temperature range from -40 to 85degC . The supplied voltage is 3.3V , and the RF frequency is 5.8GHz . The MMIC transceiver achieves the

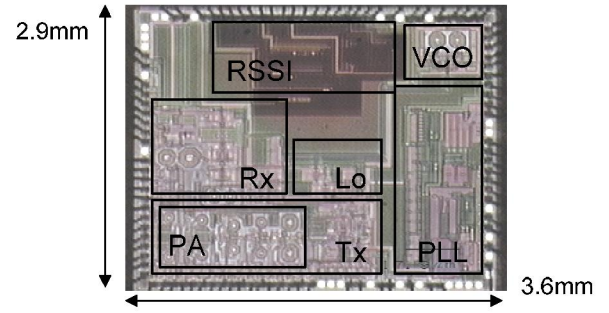


Fig. 9. Die photograph.

output power of more than 13.5dBm , the eye-open of more than 85% , the on/off ratio of more than 25.0dB and the ACPR of less than -31.1dBc .

Figure 11 shows the measured R_x characteristics. The input $P_{1\text{dB}}$, the DSB NF, and conversion gain are shown at the temperature range from -40 to 85degC . The MMIC transceiver achieves the input $P_{1\text{dB}}$ of more than -33.1dBm , the DSB NF of less than 15.6dBm and the conversion gain of more than 18.1dB are achieved.

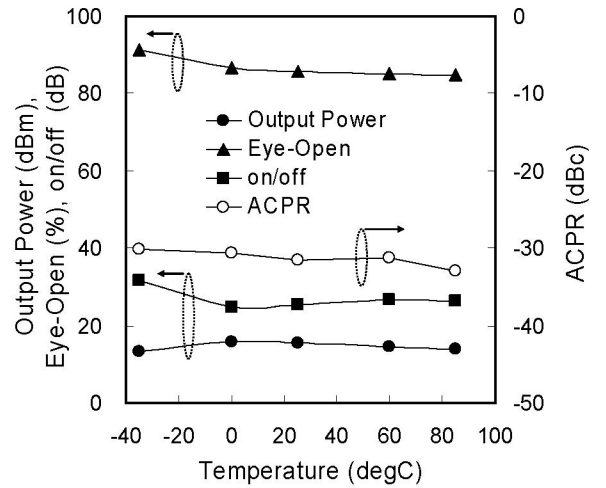
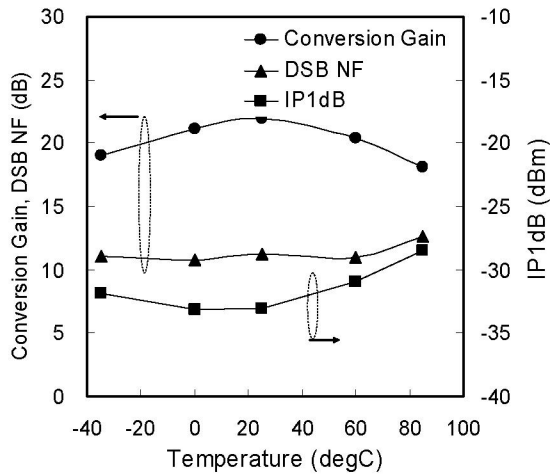


Fig. 10. Measured T_x characteristics at ASK modulation condition.

Figure 12 shows the measured modulation spectrum with the output power of 13dBm at 25degC . Fig.12(a) and (b) present the ones of $300\mu\text{m}$ and $127\mu\text{m}$ thickness, respectively. For the $300\mu\text{m}$ thickness, the VCO is interfered with the PA, and the resultant USB/LSB unbalance of transmitted ASK signal is 4.2dB . On the other hand, for the $127\mu\text{m}$ thickness, the USB/LSB unbalance is 1.2dB . The isolation improvement between the PA and the VCO is realized by employing the thin silicon substrate. Figure 13 shows the measured USB/LSB unbalance versus output power in the each case of $300\mu\text{m}$ and $127\mu\text{m}$ thickness at 25degC . The simulated results are in good agreement with the

Fig. 11. Measured R_x characteristics.

measured results. The output power improvement of 8.7dB is realized under the USB/LSB unbalance of 2dB, and the maximum output power of 15.5dBm is achieved.

Table 1 shows the performance summary of the fully integrated transceiver at 25degC.

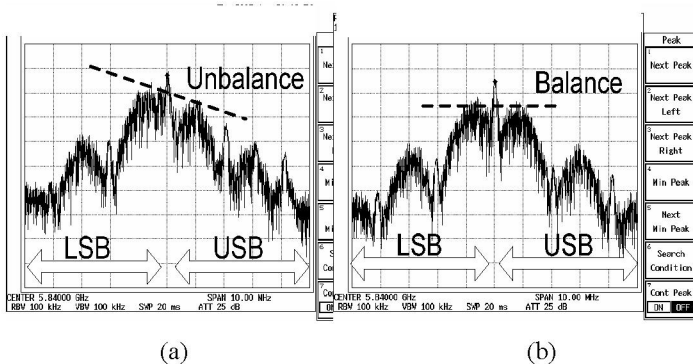


Fig. 12. Measured modulation spectrum with the output power of 13dBm. (a)300μm, (b)127μm.

IV. CONCLUSION

The fully integrated SiGe-MMIC transceiver including with a PA, a T/R SW and a VCO for ETC terminals was developed. To suppress the USB/LSB unbalance of the transmitted ASK signal, the isolation between the PA and the VCO should be improved. The relationship between silicon substrate thickness and the isolation was analyzed based on electro-magnetic simulation. The simulated result shows a MMIC of 127μm thickness achieved the isolation improvement of 12.3dBm compared with that of conventional 300μm thickness. The developed MMIC transceiver achieved the maximum output power of 15.5dBm with the ACPR of -33.5dBc in T_x , the input P_{1dB} of -33.1dBm, the DSB NF of 11.2dB and the conversion gain of 22.0dB in R_x .

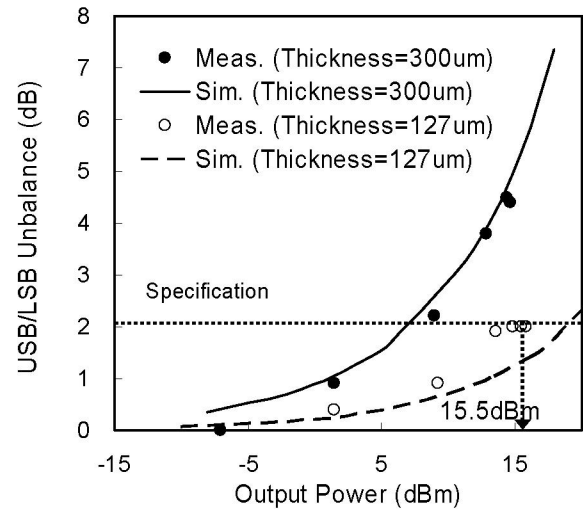


Fig. 13. Measured USB/LSB unbalance versus output power.

Table 1 performance summary.

Tx output power	15.5dBm
Tx ACPR	-33.5dBc
Tx on/off ratio	25.5dB
Tx eye-open	85.7%
Tx VGA dynamic range	20.4dB
Tx current consumption	241.1mA
Rx DSB NF	11.2dB
Rx input P1dB	-33.1dBm
Rx conversion gain	22.0dB
Rx current consumption	65.1mA
Rx phase noise	-106.7dBc/Hz at 1MHz offset

REFERENCES

- [1] Lawrence E. Larson, "Silicon Technology Tradeoffs for Radio-Frequency/Mixed-Signal "Systems-on-a-Chip" ", *IEEE Trans. Electron Devices*, vol.50, pp.683-699, March 2003.
- [2] T. Matsuda, et al., "Single-Chip 5.8GHz ETC Transceiver IC with PLL and Demodulation Circuits using SiGe HBT/CMOS", *ISSCC Dig. Tech. Papers*, pp.96, 449, February 2002.
- [3] T. Blalack, et al., "On-chip RF Isolation Techniques", *Proc. IEEE BCTM*, pp.205-211, 2002.
- [4] S. M. Sinaga, et al., "Circuit Partitioning and RF Isolation by Through-Substrate Trenches", *IEEE Electronic Components and Tech. Conf.*, pp.1519-1523, 2004.
- [5] C. S. Kim, et al., "Deep Trench Guard Technology to Suppress Coupling between Inductors in Silicon RF ICs", *IEEE MTT-s Symp. Digest*, pp.1873-1876, June 2001.
- [6] H-S Kim, et al., "The Importance of Distributed Grounding in Combination With Porous Si Trenches for the Reduction of RF Crosstalk Through p- Si Substrate", *IEEE Electron Device Lett.*, vol.24, pp.640-642, October 2003.
- [7] Y. H. Wu, et al., "Fabrication of Very High Resistivity Si with Low Loss and Cross Talk", *IEEE Electron Device Lett.*, vol.21, pp.442-444, September 2000.
- [8] M. Ono, et al., "Si Substrate Resistivity Design for On-Chip Matching Circuit Based on Electro-Magnetic Simulation", *IEICE Trans. electron.*, vol. E84-C, no. 7, July 2001.