A Fully Integrated CMOS RF Power Amplifier with Tunable Matching Network for GSM/EDGE Dual-Mode Application

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***Abstract* — A fully integrated power amplifier operating at switching and linear mode is implemented using 0.18-μm CMOS technology. To maximize performance for both operation modes, the fundamental load impedances are optimized with a variable capacitor for GSM and EDGE application. For GSM application, 32 dBm of the output power with 45 % of the drain efficiency is achieved at 1.76 GHz. With EDGE modulation signal at 1.76 GHz, error vector magnitude (EVM) has an RMS value of less than 5 % up to 27.5 dBm of the output power, and 28.1 % of modulated PAE is achieved at this power. The output spectrum is confined within the inside of mask up to 27.5 dBm of the output power.**

***Index Terms* — linear PA, power amplifiers, power combining, switching PA, variable capacitor.**

I. Introduction

The RF power amplifiers (PA) in mobile handsets are constantly calling for further miniaturization while its manufacturers require a reduced bill of materials. The PAs operating in dual-mode for GSM and EDGE applications are still required to be as small in size and high efficient as those for a single mode. Addition to the high output power and efficiency which GSM PAs mainly focus on, the PAs for EDGE application are required to meet the stringent linearity requirements such as adjacent channel power ratio (ACPR) and error vector magnitude (EVM). Therefore, the commercial GaAs PAs share their PA stage to operate in different bias conditions for the dual-modes.

Changing bias technique is widely used for multi-mode operation [1], [2]. The technique can only control DC bias to operate in different classes such as class AB and F. However, the output impedances for different modes are changed owing to the different bias conditions. Therefore, the required output matching impedances should be optimized for the operation in the pertinent modes, which means that a tunable matching network is required for further optimized operation in both linear and switching modes.

The efforts for tunable matching network for PA application have been made with some specific processes such as micro-electro-mechanical systems (MEMS), switched capacitors with PIN diodes, silicon-on-insulator (SOI) [3], and silicon-on-glass [4]. Though the tunable capacitor using CMOS technology is generally used, for example, for capacitor bank in voltage-controlled oscillator, its drawbacks are power capability and linearity at a high power level above 20 dBm [3], [5].

In this paper, we present a fully integrated 0.18 μm CMOS PA for GSM/EDGE applications with different optimum output impedances according to the operation modes by using a CMOS high-power variable capacitor. For an efficient power combining, a parallel-combining transformer (PCT) is used [6]. The PA achieves a peak output power of 32 dBm and a peak drain efficiency of 45% at 1.76 GHz for the GSM mode. In addition, the proposed dual-mode CMOS PA is successfully demonstrated to meet the tight specifications of EVM and ACPR up to 27.5 dBm for the EDGE mode, and shows the interoperability for GSM/EDGE applications.

II. Dual-mode Power Amplifier Design

A schematic of a dual-mode CMOS RF PA is shown in Fig. 1(a). It is composed of three parts, (1) input matching network including input balun to convert single-ended signal to differential signal, (2) single stage of PA composed of two pairs of CMOS differential cascode, and (3) tunable output matching network with a variable capacitor and on-chip transformer to change load impedance according to the operation modes.

A. Input Matching with On-Chip Balun

The input matching network consists of symmetric inductors with center-tap for DC biasing and on-chip input balun with input and output capacitors, C_{B1} and C_{B2}. By using the input balun, the single-ended RF signal is converted into differential signal. To reduce the loss due to the inductances of balun, C_{B1} and C_{B2} tunes input inductance and output inductance of balun, respectively.

B. Differential PA design

To avoid the complexity of multi-stage PA and verify the effect of transition of load impedances according to the operation modes, a PA circuit is designed for power stage only. Two pairs of differential cascode topology are used for our dual-mode power amplifier. By using a differential structure, source degeneration due to the bond wire connected to the common source (CS) transistor can be reduced. The

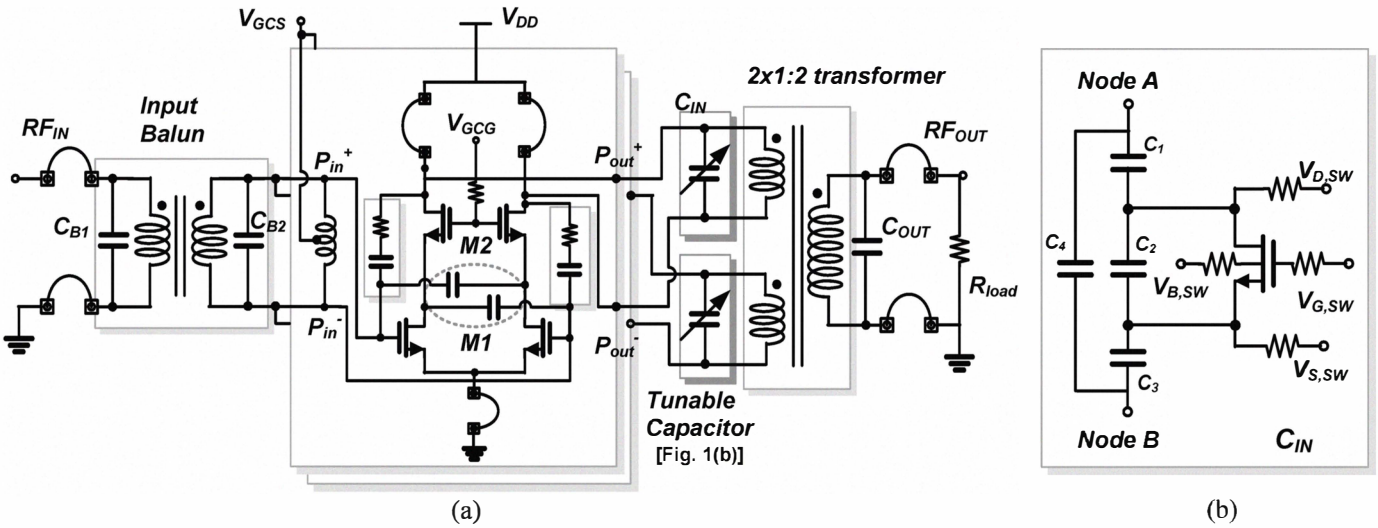

Fig.1. A dual-mode power amplifier. (a) Schematic of single stage power amplifier with a tunable matching network. (b) Structure of a high-power variable capacitor.

CMOS cascode is composed of thick-oxide transistor for common gate (CG) device, M2, and thin-oxide transistor for CS device, M1, to lessen reliability issue due to the high voltage stress at M2 transistor.

To get a higher linearity at a linear operation mode, cross-coupled capacitors are used between the drain of M1 and the gate of M1 at opposite branch in the differential pair. This technique can reduce nonlinear input capacitance at a large-signal circumstance, so called capacitive neutralizaton technique [7]. It also helps to increase gain due to the positive feedback, but can make a circuit unstable. To guarantee the stability and get more linearity, RC feedback is incorporated between the drain of M2 and the gate of M1 – this also helps to reduce the voltage stress of CG device [8].

C. Tunable Output Matching Network

The tunable output matching network used in CMOS PA for dual-mode operation is shown in Fig. 1(a). It is composed of transformer and tunable input capacitors, C_{IN}, and output capacitor, C_{OUT}. The magnetic coupled transformer can provide power combining and impedance transformation simultaneously so that it is suitable for Watt-level CMOS PA design [9]. An on-chip 2x1:2 parallel-combining transformer (PCT) is used for efficient power combining and impedance transformation [6]. It also works as an output balun which converts differential signal to single-ended signal to the load. The role of C_{OUT} is to minimize the loss due to the inductances of transformer by resonating inductance of a secondary winding with C_{OUT} [10].

The variable C_{IN} is adopted to vary the load impedance according to the operation mode, and its structure is shown Fig. 1(b). As CMOS switch transistor is turned on and off, the capacitance between node A and node B can be varied. Because of the large signal at the variable capacitor for Watt-level PA application, it is very important for the variable capacitor to sustain its capacitance value without degrading its linearity.

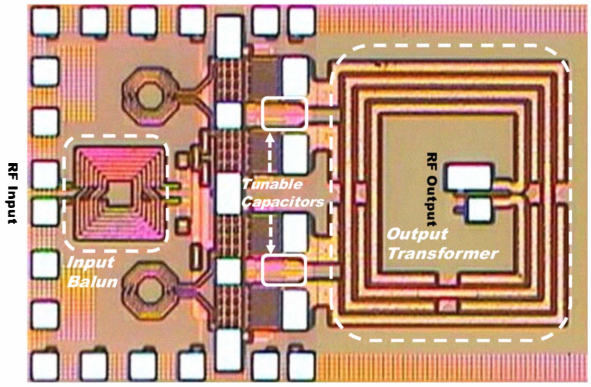

Fig. 2. Microphotograph of fully integrated dual-mode power amplifier with a 2x1:2 transformer.

As the power increases, the increasing voltage swings between terminals of switch transistor can turn on parasitic junction diodes and/or the switch transistor itself. Unlike the conventional variable capacitors, DC voltages can be applied at all terminals of switch transistor through the high resistance resistors in our structure. This can prevent the unwanted turn-on phenomenon and make our variable capacitor sustain high voltage with high linearity. In our design, the peak voltage between variable capacitor terminals can reach up to 9 V at peak power of 32 dBm. The high-power tunable capacitor used in this design does not deteriorate its characteristics up to 10 V.

D. Optimum Load Impedances

For switching mode operation, the optimum output load impedance can be obtained from the output power

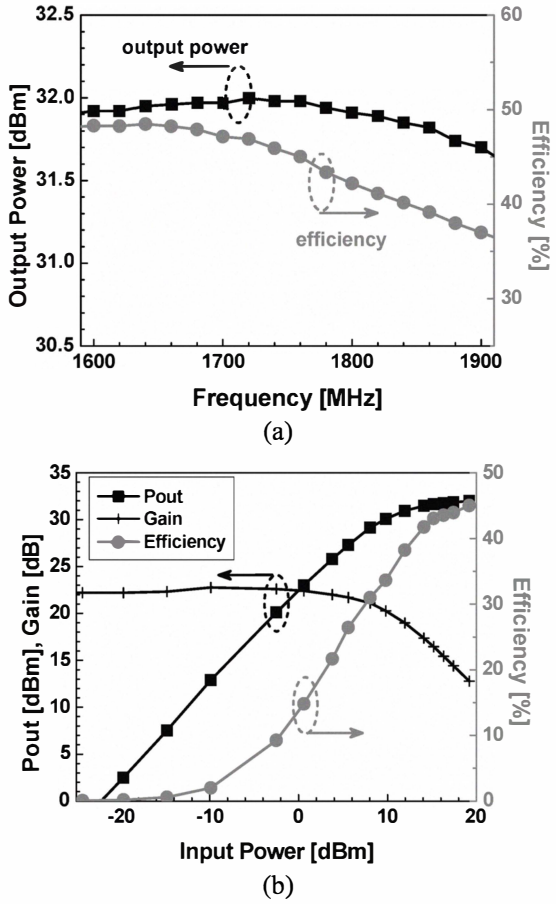

Fig. 3. Measured performances of PA in GSM mode. (a) Output power and efficiency as a function of the operating frequency. (b) Pout, gain and efficiency as a function of the input power at 1.76 GHz operating frequency.

requirements [11]. From this initial solution, optimization is followed using harmonic balance simulations to get the optimum impedance for switching mode.

To find the optimum impedance for linear amplifier operation, load-pull simulations are conducted with changing bias points. For higher efficiency and linearity, bias point is set around class AB operation.

III. Implementation and Measurement Results of GSM/EDGE Dual-mode Power Amplifier

The dual-mode GSM/EDGE PA is implemented with 0.18 μm RF CMOS process. Fig. 2 shows a microphotograph of a chip with a size of 1.7 x 1.1 mm^2 including the on-chip output transformer and all pads. The unable capacitor is implemented with four MIM capacitors and switch transistor, which is the thick oxide transistor of 1.2mm gate width to change the capacitance value according to the operation modes. The chip is assembled on a 2-layer FR-4 evaluation board for the measurement. The loss from the PCB is compensated while that of wire-bonding is included.

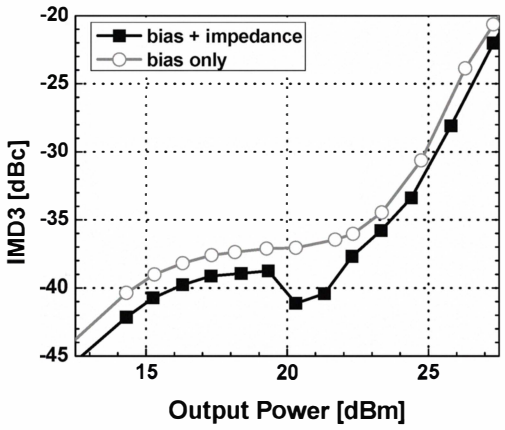

Fig. 4. Measured IMD3 characteristics with 300 kHz tone-spacing two-tone stimulus at 1.76 GHz.

TABLE I
Summary of 1-Tone Measurements in Linear Mode

Parameter	bias only	bias + impedance
S/S power gain	19.8 dB	19.2 dB
P_{1dB}	29.5 dBm	30.5 dBm
P_{sat}	31.5 dBm	31.6 dBm
Efficiency at P_{1dB}	35 %	40 %

For the bias condition of switching mode operation, the idle current is 300 mA with 2.8 V of CG gate bias, and the DC supply is 3.4 V. To set optimum load impedance for GSM operation, switch transistor is biased as "ON" state by applying 3.4 V at the gate and 0 V at the source and drain terminals of switch transistor, respectively. In Fig. 3(a), the power amplifier delivers fairly constant output power over GSM high band frequency more than 31.7 dBm of a output power less than 0.3 dB variation, while the efficiency decreases slightly as the frequency increases. At the GSM input signal of 1.76 GHz frequency, the highest output power is 32 dBm with 45 % of drain efficiency as shown in Fig. 3(b). Due to the gain boosting effect of cross-coupled capacitor, the small signal power gain is 22.2 dB, which is considerably high for the PA with the power stage only.

Different from the switching mode operation, for the better linearity in the linear mode operation, the idle current is set to 120 mA with 2.5 V of the CG gate bias and the same DC supply voltage. By changing the bias of switch transistor as "OFF" state with 0 V at gate and 3.4 V at both source and drain, the power amplifier can operate both at a different bias point and the load impedance which is much closer to the optimized matching point for linear mode operation. Single-tone measurement results of linear mode PA with and without changing impedance are summarized in Table I. Although the saturated powers for both cases are almost the same, PA with changing impedance gets a higher P_{1dB} by 1dB. This implies that load impedance is moved to the better load impedance point in the view point of linear PA.

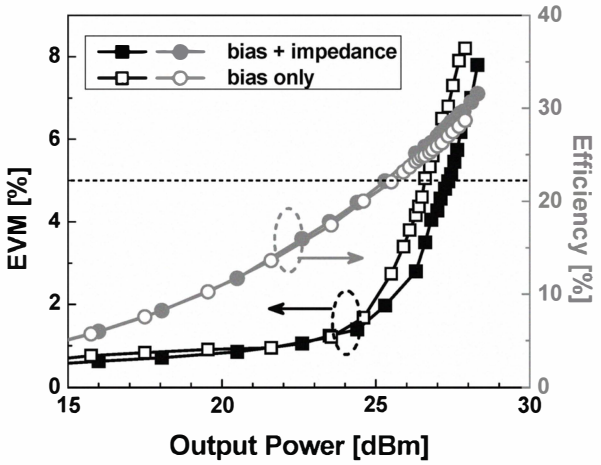

Fig. 5. Measured EVMs and modulated PAEs with EDGE signal for different output impedances.

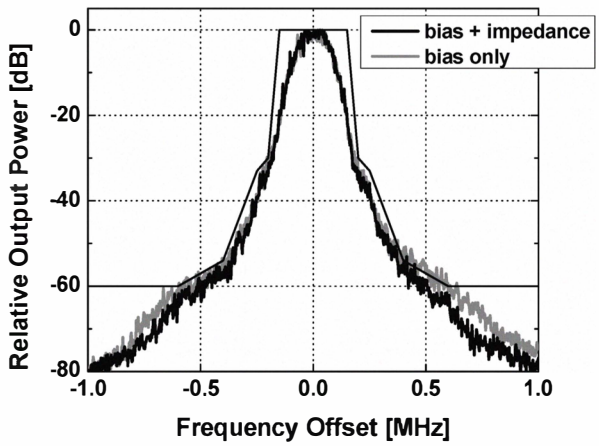

Fig. 6. Measured output spectrum with EDGE modulated signal at 27.5 dBm (freq. = 1.76 GHz).

Fig. 4 shows the comparison of IMD3 according to the impedance change when 300 kHz tone-spacing two tones are stimulated. By changing output impedance, more than 2 dB better IMD3 is achieved up to 26.6 dBm of the output power. Applying the EDGE modulation signal, EVM and output spectrum are measured as shown in Fig. 5 and Fig. 6, respectively. With the new impedance by changing capacitance value, EVM has an RMS value less than 5% up to 27.5 dBm of output power where 28.1 % of modulated PAE is achieved. These values are 1 dB higher in the output power and 3.2 % higher in PAE than those without changing output impedance, respectively. Fig. 6 shows the output spectra with and without changing impedance, and the spectrum is confined within the inside of mask by varying impedance.

IV. Conclusion

In this paper, a dual-mode CMOS PA with a tunable matching network is presented for GSM and EDGE applications. By using a high-power tunable capacitor, the different optimum fundamental load impedances for each mode are achieved. For GSM application, 45 % of the drain efficiency at 32 dBm of the output power is achieved with single tone signal at 1.76 GHz. For EDGE application, IMD3 is better by at least 2 dB up to 26.6 dBm of output power when output impedance is optimized to linear operation mode. With EDGE modulation signal, 27.5 dBm of the output power and 28.1 % of the modulated PAE are achieved at 5 % of EVM. The fully integrated dual-mode CMOS RF PA is successfully demonstrated for GSM/EDGE application by applying variable capacitor in the output matching network.

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