# A Highly Linear and Efficient CMOS RF Power Amplifier With a 2-D Circuit Synthesis Technique

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***Abstract*—A 2-D circuit synthesis technique (2DCST) is introduced that simultaneously linearizes the AM–AM and AM–PM distortions of CMOS RF power amplifiers (PAs). A class-AB nMOS RF PA fabricated in a $0.18-\mu$m CMOS process is reported. With a WCDMA signal, the amplifier achieved 41.6% power-added efficiency (PAE) with $-33$-dBc single-adjacent channel power ratio (ACPR1) and 38.5% PAE with $-40$-dBc ACPR1 at output powers of 24.9 and 24.0 dBm, respectively. This state-of-the-art linearity and efficiency performance is comparable to that of GaAs HBT linear RF PAs. The 2DCST is applicable to a broad range of analog circuits and other semiconductor technologies.**

***Index Terms*—Circuit synthesis, CMOS, linearization, power amplifier (PA), RF.**

## I. Introduction

THE performance of an RF power amplifier (PA) is largely characterized by its power efficiency and linearity. While maximizing performance, a market-competitive RF PA must also minimize design complexity and cost. This is particularly true for portable products. Therefore, circuit-level treatments for linearizing RF PAs are preferred in cost-sensitive markets, as opposed to system-level treatments (e.g., using digital predistortion).

CMOS foundry cost per square millimeter is less than 50% that of a III–V counterpart [1]. CMOS technologies are also better suited to system integration. However, CMOS amplifiers are inherently less linear than GaAs amplifiers and consequently require linearization technologies. Previous circuit-level linearization techniques typically involve "standalone" [2], [3] or "one-to-one" distortion-cancellation-like approaches [4]–[11]. In such techniques, transistor nonlinearity is explicitly identified and a complementary cancellation scheme is devised to neutralize overall distortion. While these techniques are generally simple to implement, the enhancement achievable is restricted by the nonlinear characteristics of the transistor.

Most circuit linearization techniques use a compensating circuit with a nonlinearity inverse to that of the target circuit block. This paper presents a linearization circuit synthesis technique for distortion compensation that does not require an inverse circuit for amplitude correction. Furthermore, the distortion compensation with this circuit synthesis technique can be achieved over a wide dynamic range restricted only by the device breakdown voltage.

Although circuit synthesis techniques exist for low-frequency analog circuits [12]–[14], little has been developed for RF PAs and other large signal RF circuits. For RF circuits, multitanh [15], [16] and derivative superposition [17], among others, can be regarded as 1-D synthesis techniques since either AM–AM or AM–PM distortion is addressed, but not both. Also, their application to PAs is limited due to the use of power intensive differential configurations and/or unsatisfactory linearity performance [18]–[21], despite their successes in analog circuit linearization and with some RF circuits [22]–[24].

Previously the authors presented a synthesis technique for linearizing a class-A tanh cascode cell (TCC) amplifier [25]. This technique was 1-D in the sense that only the in-phase (resistive) characteristic was corrected using a current–voltage transfer characteristic block. In this paper, a 2-D circuit synthesis technique (2DCST) simultaneously addressing both AM–AM and AM–PM distortions is presented. The technique employs flexible current–voltage transfer characteristic blocks and tunable capacitor–voltage characteristic (CVC) blocks. The 2DCST technique can be used with a single-ended topology and therefore is well suited to power-efficient applications, especially RF PAs.

Section II describes the conventional approaches to RF PA linearization. Section III introduces the TCC amplifier as a CMOS circuit implementation for CMOS class-AB amplifier linearization. The performance of the TCC amplifier at low and high frequencies is discussed in Section IV and the complete 2DCST amplifier architecture is introduced. Section V discusses the 2DCST amplifier design procedure for a particular amplifier.

In Section VI, a CMOS WCDMA RF PA, synthesized using 2DCST, is reported with a power-added efficiency (PAE) of 41.6% and single-adjacent channel power ratio (ACPR1) of $-33$ dBc. With backoff, a PAE of 38.5% is reported with an ACPR1 of $-40$ dBc. This amplifier was implemented in the IBM 0.18-$\mu$m 7WL SiGe process (with only CMOS devices used) and is compatible with integrated CMOS circuits combining RF and analog and digital circuits. The performance is state-of-the-art for a CMOS RF PA and rivals that of GaAs RF PAs.

## II. Conventional Approaches

Fig. 1 depicts a conventional circuit-level compensation of RF PA distortion. Fig. 1(a) shows the basic circuit and response of a single-ended RF amplifier. In the classic linearization pro-

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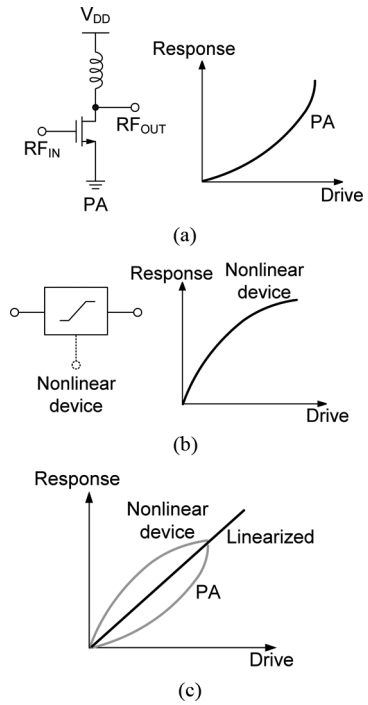


Fig. 1. Conventional linearization technique relying on the nonlinearities of another device. (a) RF PA. (b) Nonlinear device with inverse response. (c) Combined response.

cedure, the strategy is to find a complementary characteristic [see Fig. 1(b)] from available devices to cancel the distortion of the amplifier. The nonlinear device in Fig. 1(b) is put in cascade either before or after the main circuit to obtain the linearized combined response shown in Fig. 1(c). Nonlinear circuits realizing corrections for resistive [4]–[8], [10], [11], [17]–[19] and capacitive nonlinearities [9], or both [21], have been identified. However, typically only the dominant nonlinearity is targeted and a single complementary device is used for distortion cancellation. Although simple and cost effective, these approaches rely on the degree of matching of complementary characteristics, and thus, the linearization achievable ultimately depends on the nonlinear characteristics of the transistor technology. For this reason, linearity improvements with these approaches are usually limited to 10 dB and dynamic range is still dictated by transistor nonlinearities.

## III. Class-AB TCC PA

The synthesis approach introduced in this paper for addressing PA distortion employs circuit-level synthesis where the current–voltage transfer characteristic of a single-ended amplifier is manipulated and a complementary device is not required. The basic requirement is that the amplifier's transfer characteristic is capable of arbitrary manipulation. This concept is illustrated in Fig. 2. To realize our approach for a typical RF PA, a single-ended amplifier with flexible current–voltage transfer characteristics is needed. In [25], the authors introduced the TCC amplifier with the required single-ended flexible characteristics. In this section, the CMOS circuit implementation of the TCC amplifier is used to realize a highly linear class-AB amplifier.

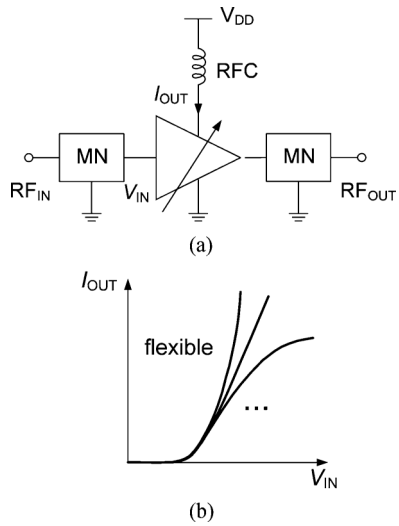


Fig. 2. Conceptual amplifier with flexible current–voltage transfer characteristics to combat amplifier nonlinearities. (a) Schematic with matching networks (MNs). (b) Flexible current–voltage transfer characteristics.

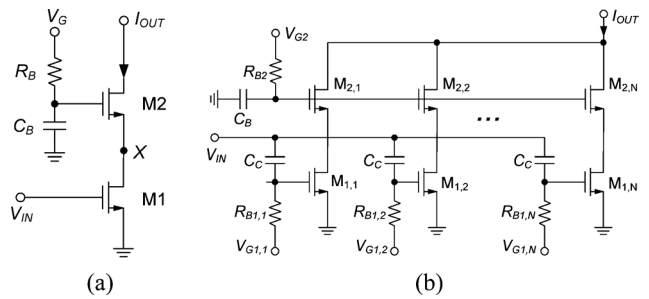


Fig. 3. TCC amplifier as an arbitrary transfer characteristic amplifier [25]. (a) Single cell. (b) Cells in cascade.

### A. TCC Amplifier

Fig. 3 shows the simplified schematic of the TCC amplifier with a single cell [see Fig. 3(a)] having tanh-like current–voltage characteristics resulting from establishing reduced headroom at node $X$. The TCC amplifier [see Fig. 3(b)] parallels $N$ cells. From Fig. 3(b), it is seen that the total output current $I_{\rm OUT}$ is the linear sum of the cell currents, each of which, as will be shown, can be scaled and shifted. For identical TCCs, with each having a tanh-like function $f(V_{\rm IN})$, it can be shown [26] that this summation can be approximately replaced by an integral equivalent to the convolution of $f(V_{\rm IN})$ and the product of a scaling function $A(V_{\rm IN})$ and a shifting function $B(V_{\rm IN})$

$$I_{\rm OUT}(V_{\rm IN}) \propto \int A(\mu)B(\mu)f(V_{\rm IN}-\mu)d\mu. \qquad (1)$$

Thus, the required linear overall characteristic, $I_{\rm OUT}(V_{\rm IN})$, can be synthesized by appropriate scaling and/or shifting of the current–voltage transfer characteristics of individual cells. That is, high linearity can be achieved by deriving and then synthesizing the $A(V_{\rm IN})$ and $B(V_{\rm IN})$ functions. In [25], this capability was demonstrated with a discrete prototype.

Scaling can be accomplished either by device sizing or biasing $(V_{G2})$, and shifting can be attained through threshold

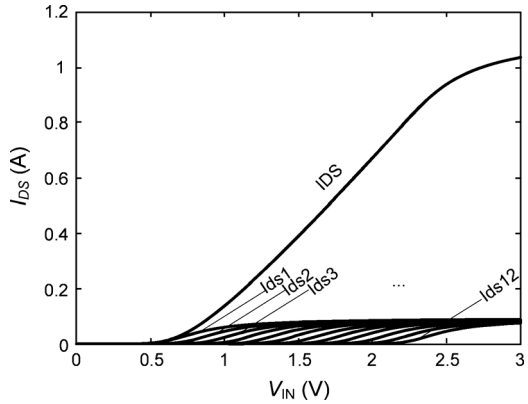


Fig. 4. Simulated dynamic current–voltage transfer characteristics of the TCC amplifier, $I_{\rm DS}$, and of its cells, $I_{dsx}$.

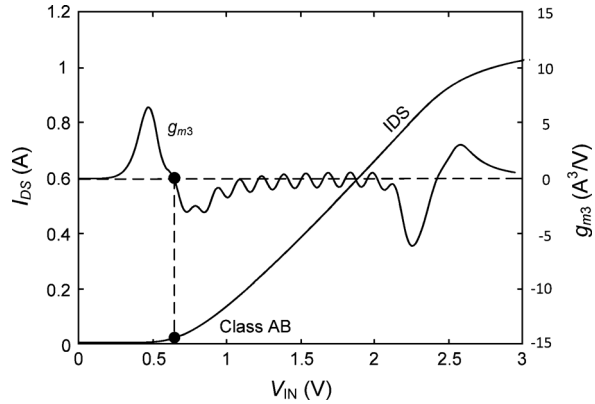


Fig. 5. Simulated small-signal transconductance, $g_{m3}$, of the TCC amplifier considered in Fig. 4.

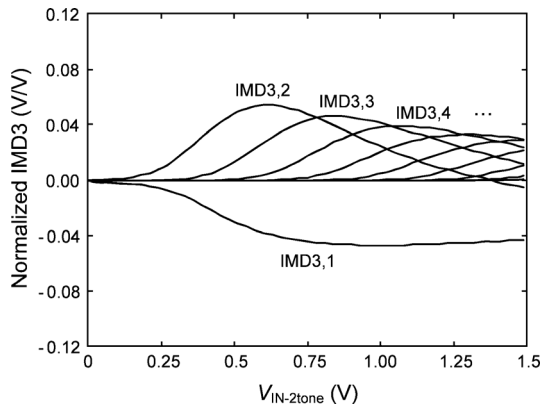


Fig. 6. Simulated and normalized IMD3 of individual TCCs (Fig. 4) biased in class-AB, as shown in Fig. 5.

voltage manipulation, gate biasing, or other means. Although some of these parameters can only be manipulated by device and process engineers, many can be addressed by the circuit designer.

In [25], the high linearity of the synthesized TCC amplifier configured in class-A mode was demonstrated. In this paper, the focus is on the linearity and efficiency of the TCC amplifier configured as a narrowband class-AB PA. It will be shown that in the class-AB mode, the TCC is capable of highly linear and efficient operation.

### *B. AM–AM Distortion Correction*

The overall low-frequency dynamic transfer characteristic of a synthesized TCC amplifier with $N = 12$ identical TCCs tuned for linear transconductance is shown in Fig. 4, together with the responses of individual cells. Each cell is shifted relative to its preceeding cell by changing the gate bias $(V_{G1,x})$ with $V_{G1,1}$ (for cell 1) being the highest bias and $V_{G1,12}$ being the lowest.

To understand the design concept, consider a small input stimulus (i.e., lower power range). Distortion can then be modeled [27] using a Taylor-series expansion of the current–voltage transfer characteristic of the synthesized TCC amplifier

$$I_{\rm DS} = g_{m1}V_{\rm IN} + g_{m2}{V_{\rm IN}}^2 + g_{m3}{V_{\rm IN}}^3 + \cdots. \qquad (2)$$

For a narrowband PA, the primary source of distortion is the third term in (2). Thus, for minimum distortion at low power, the TCC amplifier should have $g_{m3} \approx 0$. The $g_{m3}$ of the CMOS TCC amplifier here is shown in Fig. 5. It is seen that $g_{m3}$ is approximately zero for a broad range of bias voltages. High efficiency, as well as reasonable gain, is obtained for the class-AB point (at $V_{\rm IN} \approx 0.65$ V) indicated in Fig. 5. Here, $g_{m3}$ is suitably small, the slope of the current–voltage transfer characteristic is nonzero, and the bias current is small. That is, for very small input signals, there is negligible third-order intermodulation distortion (IMD3). For a larger input signal, it is necessary to examine the IMD3 level using a two-tone test signal. The IMD3 level of individual cells is shown in Fig. 6 as a function of the peak instantaneous amplitude of the two-tone test signal, i.e., $V_{\rm IN\text{-}2tone}$. In Fig. 6, the IMD3 level is normalized to the amplitude of one of the third-order tones relative to $V_{\rm IN\text{-}2tone}$.

Inspection of Fig. 6 reveals several features. First, the IMD3 of cell 1, the cell with the highest gate bias, is zero at small power levels. Second, this IMD3 becomes increasingly negative and then gradually reduces in magnitude at higher power levels. Third, the IMD3s of other cells are also zero at low power levels and become increasingly positive before eventually decreasing. Since the amplifier's (overall) IMD3 characteristic is the summation of the individual IMD3s of the cells, the sign differences of the IMD3 curves provides an opportunity to obtain zero amplifier IMD3. This can be achieved by shifting and/or scaling of the TCCs (and hence, their IMD3 curves) to eliminate third-order distortion over the entire dynamic range. It is also possible to compensate for AM–AM distortion external to the amplifier. Such distortion can be represented as an additional IMD3 curve in Fig. 6 and it is a simple matter to compensate for it.

## IV. Managing In-Phase and Quadrature Distortion

### *A. Issues at RFs*

In an RF PA, linear and nonlinear reactive effects introduce AM–PM distortion [9], [21]. This can be seen in the simulated IMD3 response of the TCC amplifier of Section III presented in polar form in Fig. 7 (again using voltage/voltage normalization). Here, the in-phase $(I)$ and quadrature $(Q)$ components at low (13.56 MHz) and high (900 MHz) frequencies are presented. It

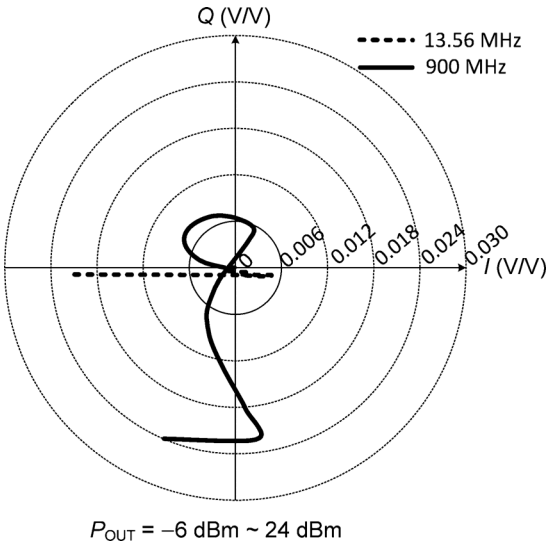


Fig. 7. Polar plot of the simulated and normalized IMD3 of the amplifier at 13.56 and 900 MHz. Output power ranges from −6 to 24 dBm.

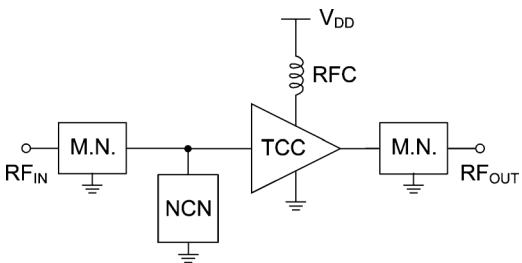


Fig. 8. Architecture of the highly linear and efficient TCC CMOS RF PA with the NCN network.

is seen that the quadrature component of IMD3 is significant at the higher frequency. This is because the IMD3 characteristics of the TCC amplifier can only be optimized for minimum low-frequency (i.e., in-phase) distortion via shifting of the TCCs. Thus, while the in-phase distortion performance is excellent at low frequencies, the quadrature IMD3 at RF is not acceptable (see Fig. 7).

### B. Proposed Architecture

To simultaneously minimize in-phase and quadrature distortion, and hence minimize the corresponding AM–AM and AM–PM distortion, it is necessary to introduce a flexible nonlinear capacitor network (NCN). The NCN completes the architecture of the linear CMOS RF PA (see Fig. 8). The NCN block location and topology relative to the cells of the TCC could be shunt, series, pre- or post- cascade, etc. In this paper, a pre-shunt topology is adopted.

The NCN is synthesized using a concept similar to that used with the TCC amplifier. That is, the CVC of the NCN can compensate the quadrature IMD3 component. Together the TCC and NCN concepts enable circuit synthesis to facilitate a 2-D compensation of RF PA distortion.

### C. NCN

The NCN uses a multiplicity of parallel nonlinear capacitor (varactor) cells synthesized using scaling and shifting. Fig. 9

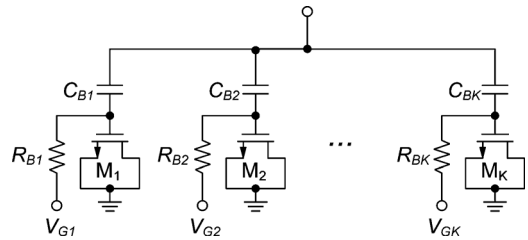


Fig. 9. Simplified schematic of a shunt NCN with nMOS gate varactors.

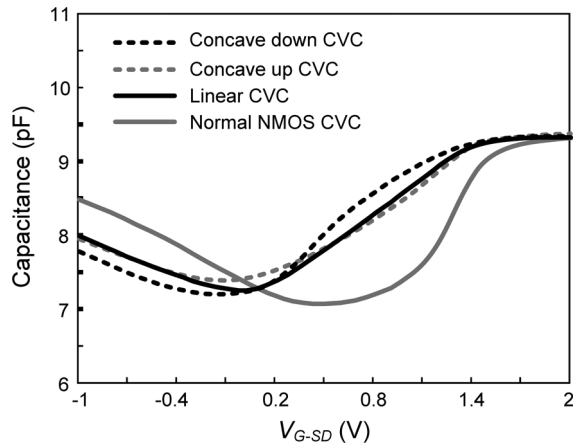


Fig. 10. Measured CVCs of a ten-cell NCN.

illustrates this concept using $K$ parallel varactors, each realized as a gate to drain/source nMOS varactor ($Cg$-$sd$ varactor).

The NCN here was fabricated using 0.4-$\mu$m nMOS $Cg$-$sd$ varactors. Fig. 10 shows measured CVCs of the NCN with different shifting, but equal scaling of the cells. Also shown for comparison is the measured CVC of a conventional nMOS $Cg$-$sd$ varactor. As can be seen, a flexible CVC can be obtained.

## V. Design of the Complete RF PA

### A. Tradeoffs With Number of TCCs

In the design of a TCC amplifier, one of the important decisions to be made is the number of TCCs, $N$. Large $N$ translates to higher resolution since it enables IMD5 and IMD7 to be minimized, as well as achieving low IMD3. Thus, larger $N$ results in better linearity, but diminishing returns are obtained for very large $N$.

A larger $N$ also results in higher dynamic range (the maximum input swing before clipping of the current–voltage transfer characteristic). To understand this, consider Fig. 11, which shows the current–voltage transfer characteristic of a TCC amplifier with cells having identical tanh current–voltage transfer characteristics with each cell biased to have equal relative shift, $V_S$. Inspection of Fig. 11 reveals that the dynamic range is

$$V_{\mathrm{DR}} = (N-1)V_S. \tag{3}$$

Therefore, a large dynamic range is obtained with a large number of cells and is ultimately limited by gate–oxide breakdown.

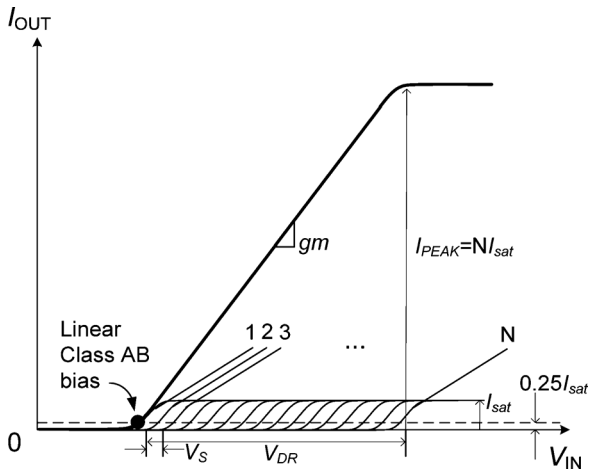


Fig. 11. Current–voltage transfer characteristic of an $N$-cell TCC amplifier with identical tanh current–voltage transfer characteristics.

As will be shown, $N$ is also related to gain and average efficiency.[1] Consider the linear summation of cell currents and the corresponding transconductances for the ideal TCC amplifier of Fig. 4. The quiescent current of the amplifier, $I_Q$, is determined only by the first cell and it is approximately a quarter of the cell's saturation current, $I_{\rm sat}$, at the class-AB bias point

$$I_Q \approx \frac{1}{4} I_{\rm sat}. \tag{4}$$

Also, the peak small-signal transconductance of the TCC amplifier is

$$g_{m\rm TCC,peak} \approx g_{m\rm cell,peak} \tag{5}$$

where $g_{m\rm cell,peak}$ is the maximum $g_m$ of a cell. The overall transconductance of the TCC amplifier at the class-AB point (where $g_{m3}$ of the overall TCC is zero) is half of its maximum value, and thus approximately equal to half of the peak $g_m$ of a cell

$$g_{m\rm TCC,Class\ AB} = \frac{1}{2} g_{m\rm TCC,peak} \approx \frac{1}{2} g_{m\rm cell,peak}. \tag{6}$$

Thus, the gain of the TCC amplifier in the class-AB mode is about 6 dB lower than that of the same TCC amplifier biased in the class-A mode (where overall $g_{m\rm TCC} = g_{m\rm TCC,PEAK}$). Now, the peak current, $I_{\rm PEAK}$, of the $N$-cell TCC amplifier from Fig. 11 is

$$I_{\rm PEAK} = N I_{\rm sat}. \tag{7}$$

Substituting (7) into (4) yields the quiescent current

$$I_Q = \frac{I_{\rm PEAK}}{(4N)}. \tag{8}$$

Since $I_{\rm PEAK}$ is set by the targeted output power then, from (8), a larger number of TCCs results in a smaller $I_Q$ for greater average efficiency due to increased efficiency at low power levels. On the other hand, from inspection of Fig. 12(b), $I_{\rm PEAK}$ is given by

$$I_{\rm PEAK} = \int g_m dV_{\rm IN} \approx g_{m\rm TCC,Peak} V_{\rm DR}. \tag{9}$$

[1]Average efficiency is defined as the statistical long-term mean efficiency of the PA [28].

where $V_{\rm DR}$ is the amplitude of the maximum distortion-free RF input voltage. Assuming $V_S$ to be fixed,[2] and substituting (3) and (6) in (9) yields the average transconductance

$$g_{m\rm TCC,CLASSAB} = \frac{I_{\rm PEAK}}{2(N-1)V_S}. \tag{10}$$

This suggests that for a fixed peak output power, increasing the number of cells reduces the small-signal gain[3] of the PA. This implies a fundamental tradeoff between the gain and average efficiency of the amplifier through the number of TCCs. The complete set of tradeoffs are summarized in Table I. It can be concluded that if the gain of a TCC is inherently high, then PA performances can be improved by increasing the number of cells.

The tradeoffs implies that a suitable design procedure is to optimize the small-signal gain of a cell, and then obtain better average efficiency and linearity by using a large number of TCCs. In practice, the maximum number of TCCs is restricted by gate–oxide breakdown and for the prototype, the number of bias pins available. Here, $N = 12$ TCCs are used as the result of compromise of performance, pin count, and providing a safe oxide breakdown margin.

### *B. TCC Device Sizing, Shifting, and Scaling*

In the design reported in this paper, the TCCs are identical although biased individually. Short channel transistors $(0.18\ \mu{\rm m})$ are used for the common source device [M1 in Fig. 3(a)] to obtain maximum small-signal gain. This choice also reduces the input capacitance, requiring a smaller NCN that translates to lower power loss in the NCN.

A long-channel thick-oxide transistor is used for M2 to increase the breakdown voltage and reduce hot carrier effects. The absolute and relative sizing of M1 and M2 takes into consideration the peak cell current capacity, available headroom, and capacitance at node $X$ and at the output. For example, increasing the relative size of M2 to M1 increases the peak cell current, but also increases the overloading of M1 and adds output capacitance.

For the design reported in this paper, shifting is implemented using voltage biasing of $V_{G1,x}$ (although threshold voltage manipulation, etc., could have been used). Scaling is implemented through absolute/relative device sizing and $V_{G2}$ (biasing of M2).

### *C. NCN Varactors and Number of NCN Cells*

A critical factor that must be considered in the design of the NCN is the shape of the varactor response needed to enable the desired CVC shape to be synthesized. This requirement, however, is somewhat relaxed since a significant amount of flexibility is available from scaling and/or shifting individual cells. For the targeted process, a $Cg$-$sd$ nMOS varactor is used and the $Q$ increases as device scaling reduces [29]. Therefore, a short-channel nMOS device is preferred. However, the short-channel device may limit the dynamic range of the amplifier due to the limited breakdown voltage of gate oxide. Here a 0.4-$\mu$m-thick oxide device is necessary to support the required dynamic range

[2]$V_S$ is largely determined by the need for flexibility in synthesis.

[3]The gain reduction can be recovered by reducing the shifting voltage $V_S$, but minimum $V_S$ is restricted by the flexibility needed to synthesize the desired IV characteristic.

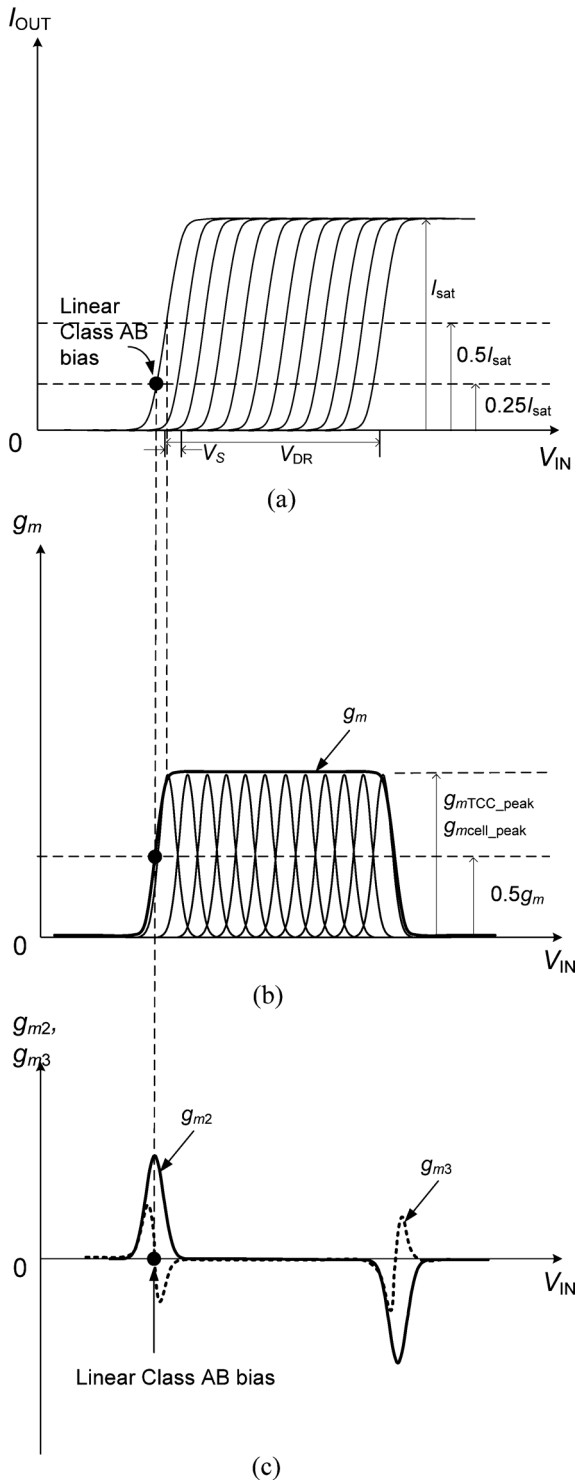


Fig. 12. Linear summation of the tanh current–voltage TCC current and transconductances.

for an RF PA design with 12 TCCs (targeted for 24-dBm output power). Previously, the CVC of the NCN with several shifting conditions was presented in Fig. 10, and the small-signal $Q$'s of these are shown in Fig. 13 and are seen to be acceptable.

To be effective, the capacitive nonlinearities of the NCN must be sufficient to compensate the AM–PM distortion. Therefore, the total (nonlinear and linear) NCN capacitance must be sufficiently large. However, an excessively large NCN reduces the

TABLE I
TRADEOFF BETWEEN NUMBER OF CELLS, $N$, AND AMPLIFIER METRICS

| | Larger $N$ | Smaller $N$ |
|---|---|---|
| Linearity | Improves but diminishing returns | Degrades with very small $N$ |
| Average eff. | Improves | Degrades |
| Gain | Degrades | Improves |
| Dynamic range | Improves | Degrades |

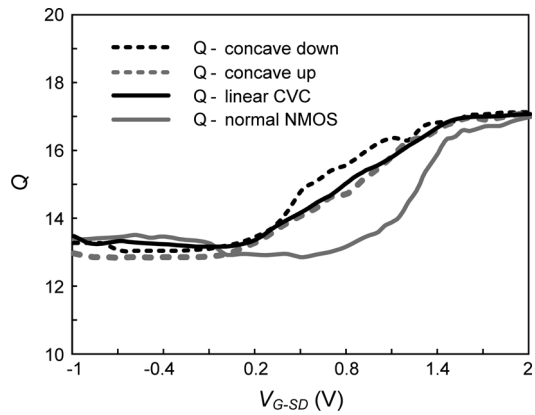


Fig. 13. Measured $Q$ of the NCN CVCs in Fig. 10.

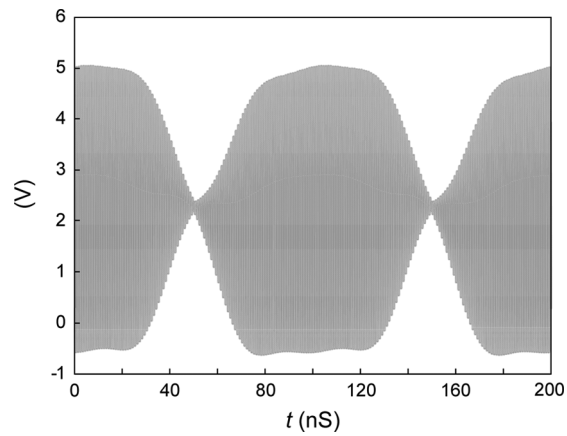


Fig. 14. Drain-to-gate-voltage waveform of the first common source device ($M_{2,1}$ in Fig. 15).

$Q$ factor at the gate input and thus limits the small-signal gain. Experience indicates that for the NCN to be effective, the total NCN capacitance must be comparable to the input capacitance of the TCC.

Similar to that of the TCC, the number of NCN cells required is directly related to the linearity (resolution) and dynamic range that can be achieved. Design of the NCN is thus a task of balancing the oxide breakdown budget, dynamic range, and, for the prototype, pin-count restrictions.

### D. Cascode Advantages and $V_{DD}$ Voltage

The cascode of the TCC differs from other cascoding circuits in that it has a current limit for its current–voltage transfer characteristic (to exhibit a tanh-like current–voltage transfer characteristic), but it has many benefits in common. These include reduction of the Miller effect and thus improvement of bandwidth [30], increase of output to input isolation [31], and hence, increased stability, and increased output impedance. In addition, the absolute and relative device sizing (of $M_1$ and $M_2$) required in synthesis will not compromise dynamic range. The

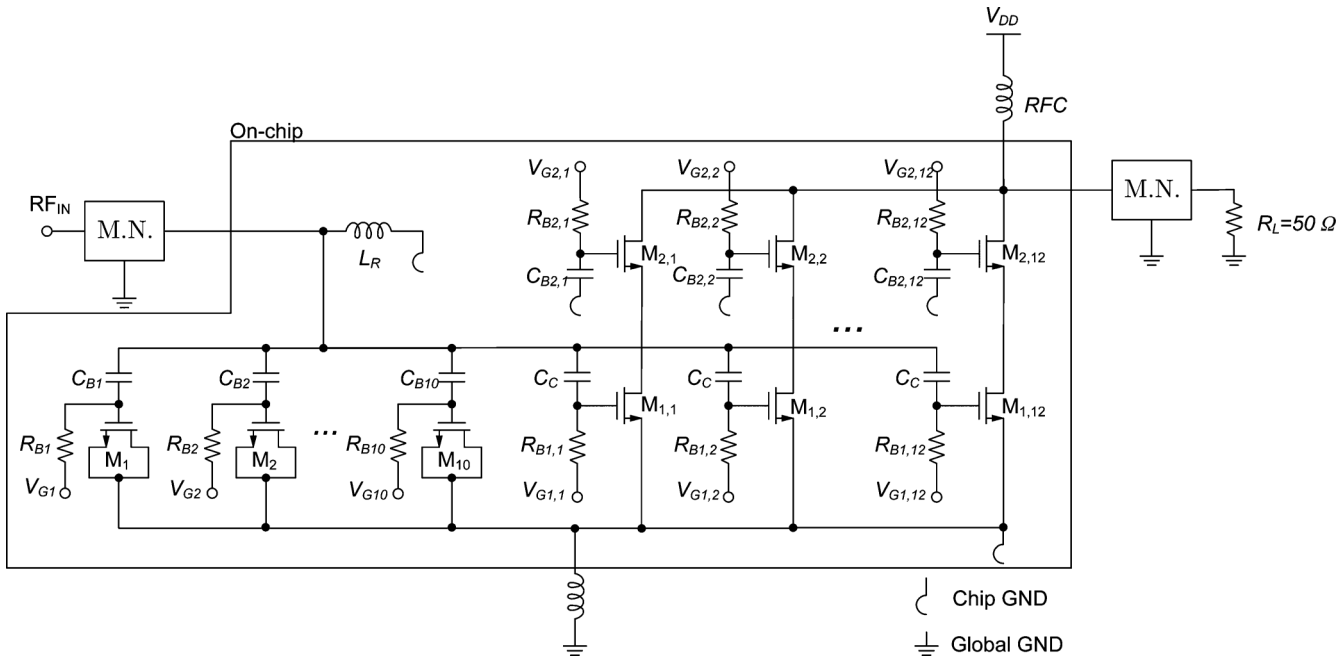


Fig. 15. Simplified schematics of the complete CMOS RF PA and external matching networks (M.N.).

small peak efficiency penalty, if any, can be offset by the improvement of linearity [25].

To ensure reliability, the drain-to-gate (oxide) voltages of the CMOS device should not exceed the recommended dc $V_{DD}$. For analog and digital circuits, this can usually be met without issues. However, for inductively loaded RF PAs, drain voltages can exceed the dc supply. Reports have indicated that an RF PA with peak RF stress equal to or exceeding the dc ratings by 36% [9], [20], [32]–[35] or even 100% [36], [37] can operate without noticeable performance degradation. For RF PAs with cascode configurations [20], [34]–[36], the peak RF stress is typically 1.5–2.0 times the dc rating. The argument made for such high peak RF stress tolerance derives from the low-duty cycle and nonconstant envelope of modern RF signals. Furthermore, it has been argued [36] that hot carrier stress is also less severe in low current density conditions. Here, the cells conduct for, at most, half of the cycle as the amplifier is biased in class-AB mode.

The above arguments lead to the design decision of 3.6 V for $V_{DD}$ while the nominal dc rating is 3.3 V. Each cascode common gate amplifier device is a thick oxide MOSFET to handle the large output voltage swings. Fig. 14 shows the simulated voltage waveforms across the drain and gate of the common gate device of the first cell (which is the one under most stress) for a two-tone signal with 24.1-dBm output. The peak RF stress across the gate to drain of the common gate amplifier with $V_{DD} = 3.6$ V is 5.09 V (1.54 times the recommend maximum dc supply voltage). This factor is similar to or lower than that of many recently reported CMOS RF PAs [9], [20], [32]–[37].

### E. Bias Searching Algorithms

Synthesis of the amplifier here requires searching for the optimum bias voltages. The complexity of the bias assignment problem is reduced by noting that the TCC is primarily responsible for the in-phase distortion component while the quadrature distortion component mainly responds to changes of the NCN. Further simplification is achieved by using IMD3 as the sole measure of distortion. Thus, the optimization goal is independently minimizing in-phase and quadrature IMD3 components. This results in the following interactive biasing algorithm.

1) Initially set equal cell shifting for the TCC (biased at the class-AB point) and NCN.
2) Simulate the complete amplifier and record the IMD3 components at each cell. Then apply the Gauss–Newton algorithm to find the optimum bias for minimum in-phase part of IMD3.
3) Similarly, simulate and record the quadrature IMD3 component and use the Newton–Gauss algorithm to search for optimized NCN biasing to minimize the quadrature components.
4) Repeat 2) and 3) until satisfactory performance is obtained.

The accuracy of the biasing algorithm relies on the accuracy of the circuit modeling. Therefore, to account for the limitations of circuit modeling, manual tuning may be necessary to refine the results from the bias search algorithms to achieve optimized performance at the experimental stage.

## VI. Results

### A. Implementation

Fig. 15 is the simplified schematic of the complete amplifier combining the NCN and TCC amplifier and with input and output matching networks (M.N.). There are 24 biasing controls used to tune in-phase and quadrature characteristics to satisfy experimental verification (to compensate for circuit deviations from simulation and further optimize performance beyond that obtained from the optimization algorithm) and performance (linearity and average efficiency) needs. In the work described here, the bias controls are applied from off-chip, but in the final design will be provided on-chip using on-chip self-calibrating and self-healing control circuit. This technique accommodates

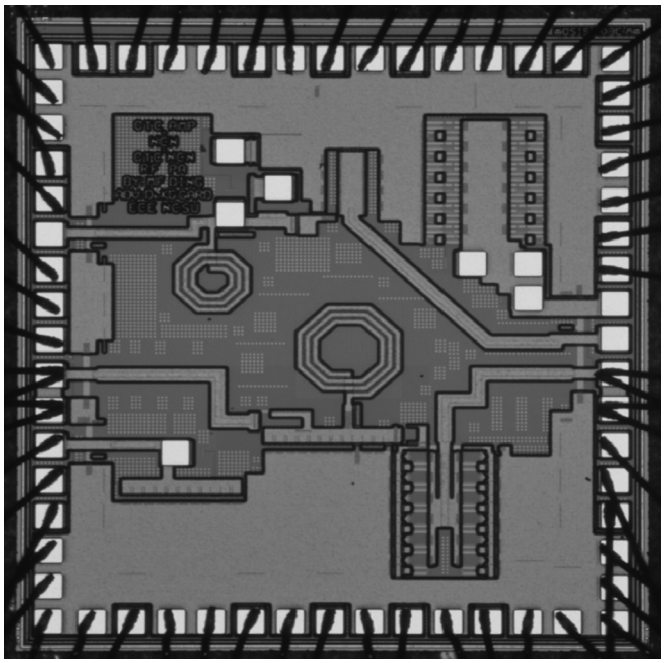

Fig. 16. Die micrograph of the amplifier.

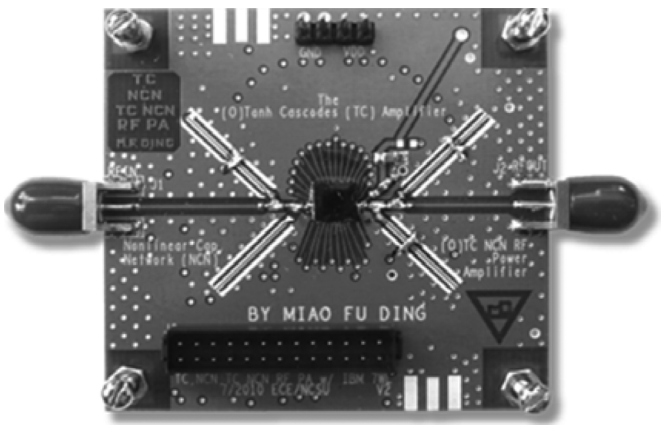


Fig. 17. Evaluation board of the complete TCC NCN RF PA.

for aging effects, and process, voltage, and temperature (PVT) variations.

The active core of the class-AB CMOS RF PA (Fig. 15) was fabricated in the IBM $0.18$-$\mu$m 7WL process. The amplifier was designed for an output power of 24 dBm in the 880–915-MHz band [38] with a supply voltage of 3.6 V. The die, Fig. 16, also includes electrostatic discharge (ESD) devices at the RF input and output pads, independent TCC and NCN circuits, and a conventional CMOS RF PA. $\mathrm{M}_{1,i}$ transistors are identical short channel devices ($W = 570\ \mu$m; $L = 0.18\ \mu$m). $\mathrm{M}_{2,i}$ are identical thick oxide devices in the process ($W = 1400\ \mu$m; $L = 0.4\ \mu$m). $\mathrm{M}_i$ for the NCN network are also identical thick oxide devices in the process ($W = 370\ \mu$m; $L = 0.4\ \mu$m). The resistors and capacitors values are $R_{Bi} = R_{B1,i} = R_{B2,i} = 17.5\ \mathrm{k}\Omega$; $C_{Bi} = 3$ pF; $C_C = 5.8$ pF; $C_{B2,i} = 11$ pF. The conventional CMOS PA is a common source thick-oxide nMOS devices with a length and width of 0.4 and 5548 $\mu$m, respectively. To achieve optimum linearity and efficiency results from this conventional RF PA, it is biased at its sweet spot ($V_{\mathrm{GS}} = 0.75$ V).

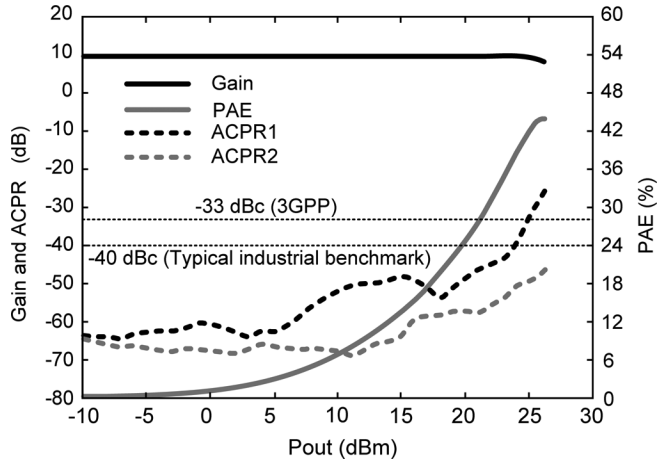


Fig. 18. Measured gain, PAE, ACPR1, and ACPR2 of the TCC/NCN amplfiier in a standard WCDMA test configuration.

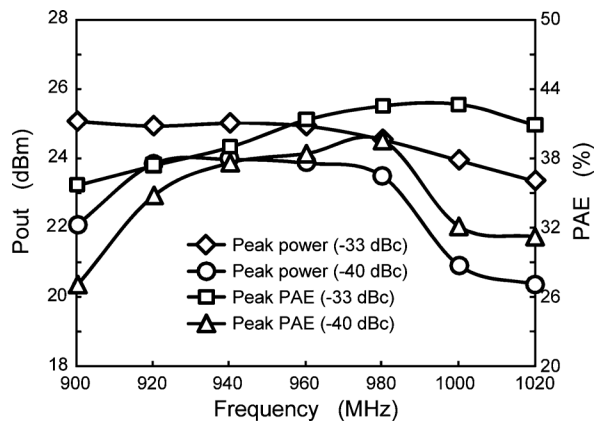


Fig. 19. Measured peak output power and PAE at specified linearity plotted against frequency in a standard WCDMA test configuration.

Critical on-chip EM structures and bond-wires were simulated using Ansoft's HFSS simulator and results used in post-layout simulations. Chip-to-package inductance was minimized using 26 uniformly distributed pads for RF grounding. The effective chip-to-package ground inductance of the bond-wires was simulated to be 0.15 nH. Fig. 17 shows a photograph of the evaluation board.

The off-chip input and output matching networks are both inductor–capacitor–inductor (LCL) $\pi$-network with dc blocking capacitors. The implementation of these networks is for convenience of implementation and tuning for this work. Notice that harmonic terminations are not considered in this work. Following the input matching network is an on-chip high-$Q$ inductor that resonates out the linear input capacitances of the NCN and TCC amplifier.

### *B. Gain, PAE, ACPR for WCDMA*

The performance obtained using a standard WCDMA test at 960 MHz is presented in Fig. 18. A gain of 9.4 dB and PAE of 41.6% at an output power of 24.9 dBm was measured while meeting the 3GPP adjacent channel power ratio (ACPR) specifications of $-33$-dBc ACPR1 and $-43$-dBc double-adjacent

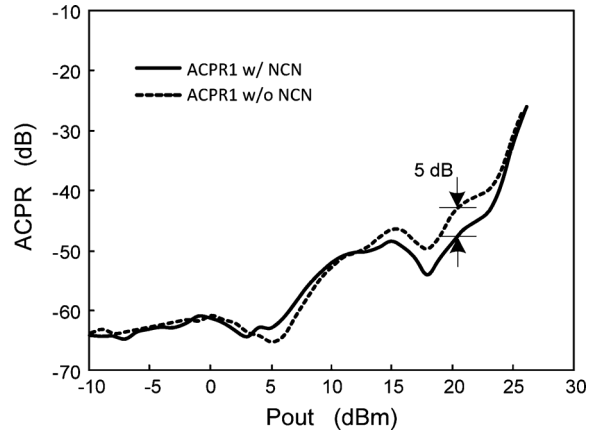


Fig. 20. Measured ACPR1 of the TCC amplifier with and without the NCN network.

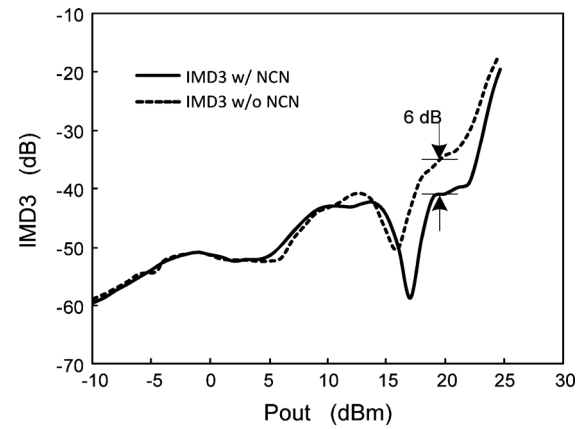


Fig. 21. Measured IMD3 distortion of the TCC amplifier with and without NCN.

channel power ratio (ACPR2). To our knowledge, this is the highest efficiency ever reported for a WCDMA CMOS RF PA. By comparison, the typical benchmark for a commercial GaAs HBT WCDMA PA is a PAE of 40% at an ACPR1 of −40 dBc. From Fig. 18, it is seen that the amplifier achieves a comparable PAE of 38.5% with an ACPR1 of −40 dBc at an output power of 24.0 dBm. Measured peak PAE and output power for a WCDMA signal are shown in Fig. 19. Measurements include bond-wire, package, PCB, and matching network losses up to the SMA connectors.

### C. Effectiveness of the NCN

The effectiveness of the NCN for 2-D linearization is seen by comparing the ACPR performance with and without the NCN (see Fig. 20). The ACPR without NCN correction was obtained by biasing the NCN cells to a high value so that the NCN is virtually a linear capacitor. This experimental trick is valid since the gain and PAE are virtually unchanged, and, to the first order, the third-order distortions are insensitive to the linear portion of the NCN capacitor.[4] As seen in Fig. 20, the NCN improves the ACPR1 by 5–8 dB in the mid and higher power ranges. The measured IMD3 with and without the NCN is compared in Fig. 21, from which a similar difference is observed. Fig. 22

[4]In fact, the linear portion of the total input gate capacitor (NCN and TCC) is resonated out by the gate inductor.

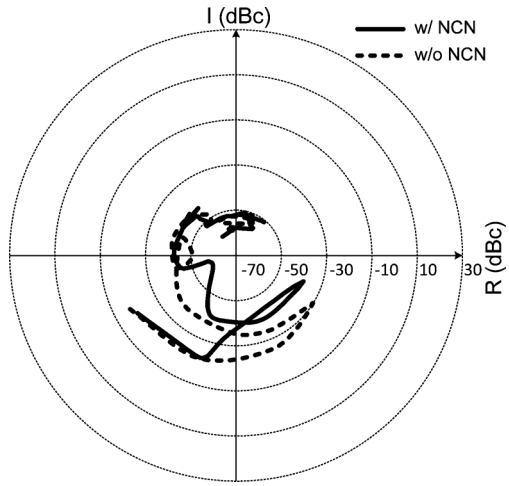


Fig. 22. Measured polar IMD3 of the TCC amplifier with and without NCN for output power ranging from −9.8 to 24.7 dBm.

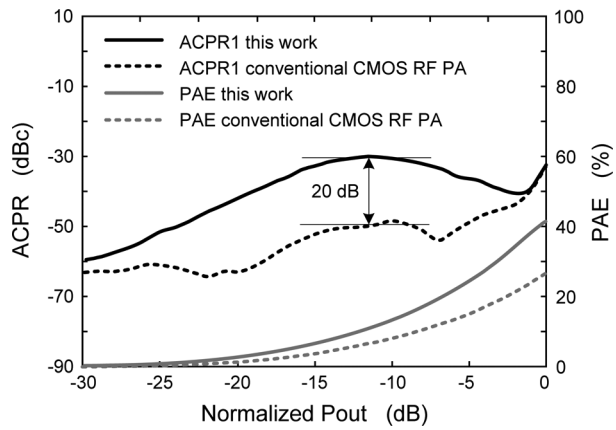


Fig. 23. Comparison of the PAE and ACPR of the new TCC/NCN CMOS PS and a conventional class-AB CMOS RF PA against normalized output power.

is a 2-D representation of the impact of the measured IMD3 with and without the NCN. The effectiveness of the NCN in linearizing the quadrature part of the IMD3 can be clearly observed for mid and higher power levels. Note that the phase of IMD3 is relative to the carrier and detailed measurement setup and procedures can be found in [27] and [39].

### D. Comparison to Conventional Cascode CMOS RF PAs

The advantages of the PA presented here can be appreciated by comparing the linearity and efficiency to that of a conventional common source CMOS RF PA (designed for comparable peak linear output power) on the same die. The conventional CMOS RF PA is biased at its sweet spot [2] (i.e., $g_{m3} = 0$) where in-phase distortion is not significant at low and mid power levels. The measured PAE and ACPR performance of the two PAs are plotted against normalized output power in Fig. 23. Power is normalized to that at −33-dBc ACPR1 so that for a normalized output power of 0 dB, both PAs have an ACPR1 of −33 dBc. The normalized output power of 0 dB corresponds to 23 and 24.9 dBm for the conventional CMOS and TCC/NCN PAs, respectively. That is, compared to a conventional class-AB CMOS PA and for the same distortion level, the new TCC/NCN PA requires approximately 1.9-dB less back-off from the 1-dB

TABLE II
COMPARISON OF THE PERFORMANCES OF THIS PROTOTYPE AND RECENTLY REPORTED RF PAs

| References | | Signal | Pout33/ PAE33 (dBm)/(%) | Pout40/ PAE40 (dBm)/(%) | $Pout_{IMD3}$/ $PAE_{IMD3}$ (dBm)/(%) | Stage/Gain (dB) | VDD (V) | Freq. (MHz) |
|---|---|---|---|---|---|---|---|---|
| This work (with NCN) | CMOS 0.18-0.4 μm | WCDMA | 25/41.6 | 23.8/38.4 | 24/38 | Single/9.4 | 3.6 | 960 |
| This work (without NCN) | CMOS 0.18-0.4 μm | WCDMA | 24.7/40.9 | 23.2/35.2 | 23/36 | Single/9.4 | 3.6 | 960 |
| This work Conventional Class AB CMOS | CMOS 0.4 μm | WCDMA | 7.2/3.5 16.2/12.6 22.6/26 | 3.6/1.7 21.7/23.7 | 22.2/29.5 | Single/16 | 3.3 | 960 |
| Commercial GaAs RF PA | GaAs HBT | WCDMA | 29/42 | 28/40 | N/A | Three/28 | 3.4 | 900 |
| Wang 2004 [9] | CMOS 0.5 μm | WCDMA | 24/29 | 23/25.5 | 25.5/N/A | Two-stage/23.9 | 3.3 | 1750 |
| Presti 2009 [40] | SOI CMOS 0.13 μm | WCDMA/EDGE/ OFDM | N/A | 22.5/40 | N/A | Two/14.5 | 2.1 | 1900 |
| Pornpromlikit 2010 [41] | SOI CMOS 0.13 μm | WCDMA | 29.4/41.4 | 20/12.5 28.4/37.5 | N/A | Single/14.6 | 6 | 1900 |
| Zhang 2009 [42] | InGaP/GaAs HBT | WCDMA | 29/47.5 | 22/22 27/39.5 | 24/N/A (simulated) | Two/29 | 3.4 | 1950 |
| Jeon 2010 [43] | CMOS 0.18 μm | WCDMA | 23.5/40 | 7.5/19.8 | 23/N/A | Two 26 | 3.4 | 1900 |

Pout33/PAE33: $P_{out}$ and PAE for ACPR1=−33 dBc. Pout40/PAE40: $P_{out}$ and PAE for ACPR1=−40 dBc. $Pout_{IMD3}/PAE_{IMD3}$: $P_{out}$ and PAE for IMD3=−25 dBc with a two-tone test.

gain compression point. The PA presented here has a PAE more than 15% greater than that of the conventional PA. The ACPR1 is 20 dB better for sub-mid to high power ranges.

Table II compares the presented linear amplifier performance against recently published CMOS and GaAs HBT amplifier results for WCDMA applications. The presented CMOS amplifier achieves PAE 38.4% at 40-dBc ACLR and 3.6-V supply voltage compared to 37.5% PAE for the best standalone CMOS silicon-on-insulator (SOI) design [41]. The amplifier also compares favorably against the best-in-class CMOS PAE of 40% for an SOI CMOS design [40] that included considerable digital complexity and required DPD correction. Each of these CMOS designs achieved PAE performance comparable to the 40% commercial GaAs HBT designs.

## VII. CONCLUSIONS

A highly linear and efficient CMOS RF PA based on an amplifier with TCCs and NCN cells has been presented. A peak PAE of more than 40% was achieved using a WCDMA test and meeting ACPR specifications. This is the best reported efficiency of a WCDMA CMOS RF PA using only circuit-level linearization techniques. These results are comparable to those of GaAs PAs. Thus, CMOS RF PAs are a viable competitive solution for medium power-range applications such as cellular handset RF PAs.

The significant improvement in linearization is due to a 2DCST that simultaneously linearizes in-phase and quadrature distortion. While the technique was applied to a CMOS amplifier here, it is applicable to a wide variety of analog and RF circuits, especially those with large signals.

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