

2.1 A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications

Song Hu, Fei Wang, Hua Wang

Georgia Institute of Technology, Atlanta, GA

Millimeter-wave fifth-generation (5G) systems will extensively leverage massive multiple-input multiple-output (MIMO) architectures to improve their link performance. These array systems will employ many power amplifiers (PAs) operating at moderate output power (P_{out}), e.g., 16 PAs each with +7dBm P_{out} [1]. The PA energy efficiency is of paramount importance in MIMO systems for improved battery life and thermal management. Due to spectrum-efficient modulations with high peak-to-average power ratios, both PA peak efficiency and power back-off (PBO) efficiency are critical. To achieve 5G Gb/s data-rates with complex modulations, envelope tracking PAs require high-speed/high-precision supply modulators, and outphasing PAs need high-speed baseband computation, both of which pose substantial challenges in practice. Although Doherty PAs support high data-rates, existing silicon mm-wave Doherty PAs exhibit very limited PBO efficiency enhancement, mainly due to inefficient Doherty power combiners and imperfect main/auxiliary PA cooperation [2,3].

In addition, multiple mm-wave frequency bands, including spectra around 28, 37, and 39GHz, have been opened for 5G development. Multiband operations will greatly facilitate MIMO frequency diversity and future cross-network/international roaming. Together with existing wideband antennas, a single multiband PA will enable future ultra-compact multiband massive MIMO 5G systems. However, the carrier bandwidth of a conventional Doherty PA is often limited by the Doherty power combiner.

To address these unmet challenges, we propose a fully integrated 28/37/39GHz multiband Doherty PA for 5G massive MIMO applications. Both PA PBO efficiency and carrier bandwidth are significantly enhanced by a transformer-based Doherty power combiner. Moreover, a power-aware adaptive uneven-feeding scheme provides optimum main/auxiliary PA cooperation. A prototype is implemented in 0.13 μ m SiGe BiCMOS. It achieves +16.8/+17.1/+17dBm peak P_{out} , 18.2/17.1/16.6dB peak power gain, 29.4/27.6/28.2% peak collector efficiency (CE), and 20.3/22.6/21.4% peak PAE at 28/37/39GHz. Its Doherty operation achieves 1.72/1.92/1.62 \times and 3.39/3.86/3.51 \times efficiency enhancement at 5.9/6.6/7.7dB PBO over Class-B and Class-A PAs at 28/37/39GHz, respectively. Amplifying 3Gb/s 64-QAM with high efficiency and linearity is demonstrated in all these three 5G bands.

Figure 2.1.1 shows conventional and proposed Doherty output networks. Most silicon Doherty PAs employ the conventional design with either transmission lines (TLs) [2] or lump elements [4]. Series combining transformer is also used, which, however, exhibits compromised Doherty load modulation and requires additional passive overhead [3]. We propose a transformer-based Doherty output network. It significantly reduces the impedance transformation ratios (ITRs) in PBO while achieving the same peak P_{out} . This directly improves the PBO passive efficiency and enhances the Doherty PA PBO efficiency. Moreover, the reduced ITR broadens the Doherty PA carrier bandwidth due to the decreased loaded quality factor of the passive network [5]. The proposed Doherty output network is designed using on-chip transformers to achieve compactness. Transmission lines TL_1 , TL_2 , and TL_3 are first approximated by low-, low-, and high-pass π -networks, respectively. Then, the four inductors are absorbed into two on-chip transformers. The two shunt inductors from TL_3 form magnetization inductors, and the series inductors from TL_1 and TL_2 are incorporated as leakage inductors. Three $\lambda/4$ TLs are thus realized in a two-transformer footprint. Capacitors C_1 , C_2 , and C_3 absorb PA device or pad parasitics. 3D EM simulations verify the Doherty load modulation behavior with enhanced PBO passive efficiency and carrier bandwidth (Fig. 2.1.2).

For optimum Doherty operation, the auxiliary PA should provide a rapidly increasing current after it is turned on. Conventionally, this is achieved by adaptively biasing the auxiliary PA [3,4]. However, adaptive biasing circuit can become challenging for 5G applications, since it is loaded by large PA transistors, and it needs to track the real-time envelope that has ~3 \times bandwidth expansion over the modulated signal. We propose a power-aware adaptive uneven-feeding scheme (Fig. 2.1.3). The input conductance of the Class-C auxiliary PA increases noticeably for increased input power (P_{in}), while that of the Class-AB main PA

remains almost the same. This effect is leveraged to dynamically modulate the auxiliary driver load and achieve enhanced power gain when P_{in} increases. Thus, compared with the main path, the auxiliary PA final stage is fed by a larger P_{in} in the high-power region. This facilitates the rapid increase of auxiliary PA output current and achieves an optimum Doherty operation without hardware overhead or modulation-rate limitation.

Figure 2.1.4 shows the schematic of the PA. An on-chip differential quadrature hybrid first performs input power split and 90° phase shift. The relative phase of main/auxiliary paths is adjusted using 9-section varactor-loaded TLs to further extend the Doherty PA carrier bandwidth (Fig. 2.1.2) [6]. Different varactor settings are used for 28GHz and 37/39GHz (Fig. 2.1.4). The high-order networks formed by varactor-loaded TLs also ensure wideband input matching for different settings. Each PA path comprises a driver stage and a PA stage. The interstage matching is designed to realize the proposed adaptive feeding scheme.

The PA chip occupies 1.76mm² (Fig. 2.1.7). Measured small-signal S-parameters, saturated P_{out} (P_{SAT}), and P_{1dB} for the two settings show broadband performance (Fig. 2.1.4). The PA achieves a -3dB S_{21} bandwidth of 23.3 to 39.7GHz (52.1%). The -1dB P_{SAT} bandwidth is 27.7% and 33.3% for the two settings, and collectively covers 28-to-42GHz (40%) band. Figure 2.1.5 shows large-signal continuous-wave test results. Owing to the proposed Doherty output network and adaptive feeding scheme, superior PBO efficiency improvements are achieved over Class-B and Class-A PAs in all three 5G bands. Excellent amplitude/phase linearity is also observed. The PA is measured using 500MSym/s 64-QAM (3Gb/s) signals (Fig. 2.1.5). Without predistortion, the EVM and ACPR are better than -27dB and -28.2dBc with average $P_{out}>+9.2$ dBm in all three 5G bands. These 64-QAM tests show substantial PA average efficiency improvements over normalized Class-B and Class-A PAs in all three bands, verifying the multiband Doherty performance in high-speed dynamic operations. The PA also supports 1GSym/s 64-QAM (6Gb/s) at 28GHz as the state-of-the-art demonstrated data-rate for 28GHz silicon PAs. Our PA advances the state of the art for Doherty, wideband, and 5G silicon PAs in mm-wave bands (Fig. 2.1.6).

Acknowledgements:

We thank GlobalFoundries for chip fabrication.

References:

- [1] S. Shakib, et al., "A 28GHz Efficient Linear Power Amplifier for 5G Phased Arrays in 28nm Bulk CMOS," *ISSCC*, pp. 352–353, Feb. 2016.
- [2] A. Agah, et al., "Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45nm SOI CMOS," *IEEE JSSC*, vol. 48, no. 10, pp. 2338–2350, Oct. 2013.
- [3] E. Kaynak, et al., "Transformer-Based Doherty Power Amplifiers for Mm-Wave Applications in 40nm CMOS," *IEEE TMTT*, vol. 63, no. 4, pp. 1186–1192, Apr. 2015.
- [4] K. Onizuka, et al., "A 2.4GHz CMOS Doherty Power Amplifier with Dynamic Biasing Scheme," *IEEE ASSCC*, pp. 93–96, Nov. 2012.
- [5] A. Grebenikov, et al., "A Dual-Band Parallel Doherty Power Amplifier for Wireless Applications," *IEEE TMTT*, vol. 60, no. 10, pp. 3214–3222, Oct. 2012.
- [6] R. Darraji, et al., "Mitigation of Bandwidth Limitation in Wireless Doherty Amplifiers with Substantial Bandwidth Enhancement Using Digital Techniques," *IEEE TMTT*, vol. 60, no. 9, pp. 2875–2885, Sept. 2012.

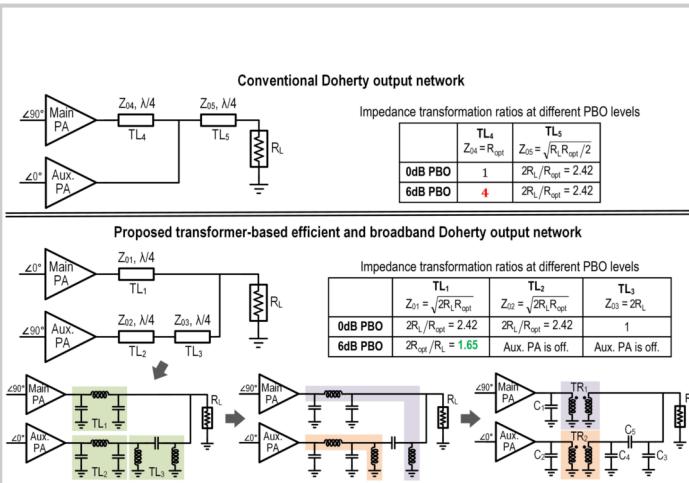


Figure 2.1.1: Proposed transformer-based Doherty power combiner achieving reduced ITRs in PBO with the same peak P_{out} ($R_{opt}=41.3\Omega$).

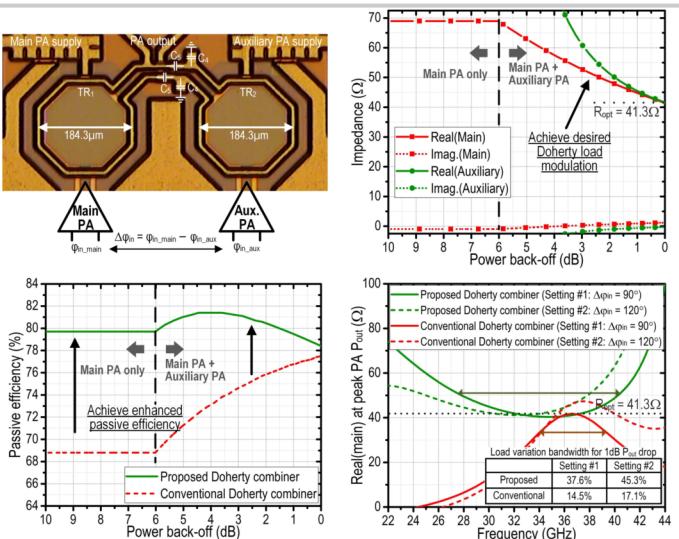


Figure 2.1.2: Compact layout and 3D EM simulation results of the proposed transformer-based Doherty power combiner.

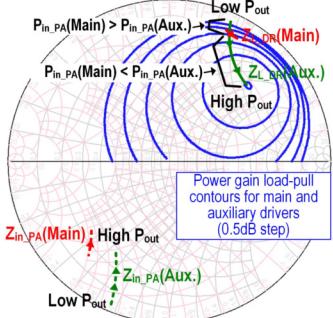
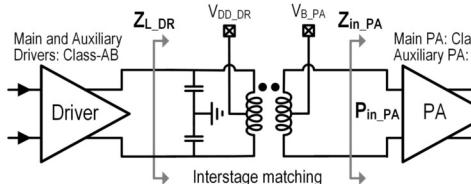


Figure 2.1.3: Proposed power-aware adaptive uneven Doherty PA input feeding scheme.

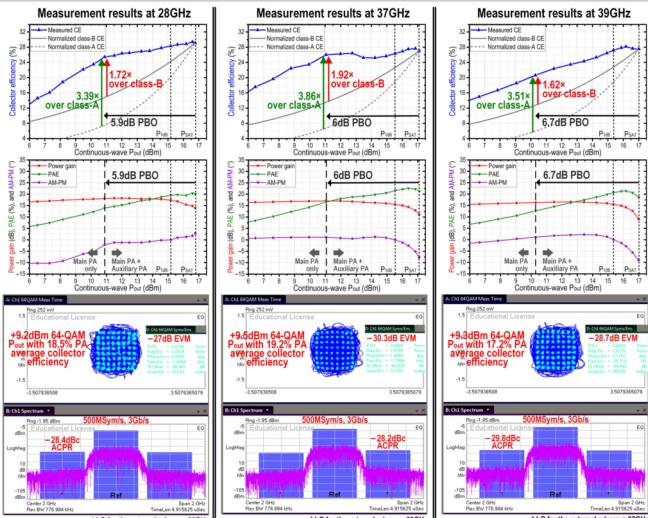


Figure 2.1.5: Continuous-wave and 500MSym/s 64-QAM (3Gb/s) measurement results for the three 5G bands at 28, 37, and 39GHz.

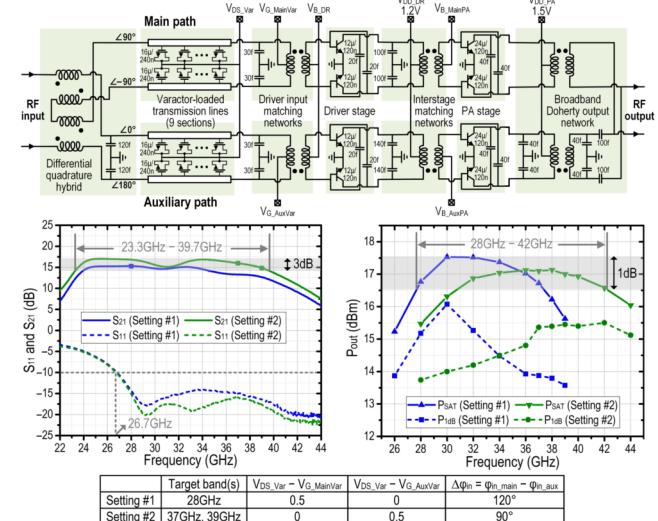


Figure 2.1.4: Schematic together with measured small-signal S-parameters and large-signal P_{SAT}/P_{1dB} results.

		Our work			Mm-wave Doherty PA	Mm-wave wband PA	5G PA
Technology		130nm SiGe			45nm SOI CMOS	40nm CMOS	28nm CMOS
Architecture		Multiband Doherty			Slow-wave CPW Doherty	Doherty	Asymmetric combiner
Supply (V)		1.5			2.5	1.5	1
S ₁₁ -3dB BW (GHz)		23.3-39.7 (52%)			N.A.	60-81 (30%)	40-67 (61%)
P _{SAT} -1dB BW (GHz)		28-42 (40%)			N.A.	58-77 (28%)	40-65 (48%)
Area (mm ²)		1.76			0.64	0.96	0.33
Frequency (GHz)	28	37	39	42	42	55	30
Power gain (dB)	18.2	17.1	16.6	17.2	17.2	18.8	15.7
P _{SAT} (dBm)	+16.8	+17.1	+17	+18	+18	+21	+13.3
P _{1dB} (dBm)	+15.2	+15.5	+15.4	+19.2	+19.2	+19.9	+13.2
Peak η	29.4% CE 13.9% PAE @6dB PBO	27.6% CE 22.4% PAE @6dB PBO	28.2% CE 21.4% PAE @6dB PBO	33% DE 23% PAE @6dB PBO	20.7% DE 13.0% PAE @6dB PBO	27.7% PAE	16% PAE
η @ P _{dB}	26.4% CE 19.8% PAE @6dB PBO	27.1% CE 21.6% PAE @6dB PBO	20.7% PAE 19.3% DE @6dB PBO	17.8% DE [*] 12.4% PAE @6dB PBO	15.7% PAE	14% PAE	34.3% PAE
η @ PBO	26.4% CE 13.9% PAE @6dB PBO	28.2% CE 16.6% PAE @6dB PBO	20.6% CE 12.6% PAE @6dB PBO	11.5% DE [*] 7% PAE @6dB PBO	7% PAE [*] @6dB PBO	5% PAE [*] @6dB PBO	35.5% PAE
Modulation results	64-QAM 500MSym/s +27dB EVM -28.4dBc ACPR	64-QAM 500MSym/s +9.3dBm 18.5% CE	64-QAM 500MSym/s +30.3dB EVM -28.4dBc ACPR	64-QAM 500MSym/s +9.3dBm 19.2% CE	64-QAM 500MSym/s +15.9dBm 7.2% CE	64-QAM 500MSym/s +12.8dBm -25.6dB EVM	64-QAM 250MSym/s +4.2dBm -26.4dBc ACPR 9% PAE

* Read from the reported figures. ** Without pads. † Specially tuned biasing.

Figure 2.1.6: Comparison table.



Figure 2.1.7: Die micrograph.