Broadband CMOS Stacked RF Power Amplifier Using Reconfigurable Interstage Network for Wideband Envelope Tracking

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***Abstract*—In this paper, a two-stage broadband CMOS stacked FET RF power amplifier (PA) with a reconfigurable interstage matching network is developed for wideband envelope tracking (ET). The proposed RF PA is designed based on Class-J mode of operation, where the output matching is realized with a two-section low-pass matching network. To overcome the bandwidth (BW) limitation from the high-Q interstage impedance, a reconfigurable matching network is proposed, allowing a triple frequency mode of operation using two RF switches. The proposed RF PA is fabricated in a 0.32-μm silicon-on-insulator CMOS process and shows continuous wave (CW) power-added efficiencies (PAEs) higher than 60% from 0.65 to 1.03 GHz with a peak PAE of 69.2% at 0.85 GHz. The complete ET PA system performance is demonstrated using the envelope amplifier fabricated on the same process. When measured using a 20-MHz BW long-term evolution signal, the overall system PAE of the ET PA is higher than 40% from 0.65 to 0.97 GHz while evolved universal terrestrial radio access adjacent channel leakage ratios are better than −33 dBc across the entire BW after memoryless digital pre-distortion. To our knowledge, this study represents the highest overall system performance in terms of PAE and BW among the published broadband ET PAs, including GaAs HBT and SiGe BiCMOS.**

***Index Terms*—Broadband, class-J, CMOS, envelope tracking (ET), high-efficiency, long-term evolution (LTE), multiband, power amplifier (PA), silicon-on-insulator (SOI), stacked FET.**

I. Introduction

RAPID development of mobile communication calls for highly efficient RF power amplifiers (PAs) for extended battery life. However, to meet the stringent linearity requirement of the digital modulation signals, a PA should be operated in the back-off region, which results in significant efficiency degradation. The PA efficiency problem has become more serious with the introduction of the fourth-generation long-term evolution (4G LTE) standard, which requires peak-to-average power ratio (PAPR) as high as 6–7 dB. To overcome this problem, an envelope-tracking (ET) technique is widely investigated, and several papers have reported excellent overall system power-added efficiencies (PAEs) using 10-/20-MHz bandwidth (BW) long-term evolution (LTE) signal [1]–[8]. Another challenge of the RF PA for LTE mobile phones is the need to cover a number of highly fragmented LTE bands using a single PA chain. The authors have demonstrated a port-reconfigurable PA using a frequency reconfiguration network (FRN) in the output matching network to cover various frequency bands from a single output port [9]. However, PA reconfiguration for a given output port has limited practicality unless the duplexer filters following the PA can also be made frequency tunable, which is technically difficult at this stage. A more practical approach is to develop a broadband PA followed by a distribution switch to branch out the signals to each of the dedicated-band duplexer filter. Although there have been several reports for broadband PAs, most of studies focused on the design of broadband load matching network for single-stage PAs [4], [10], [11]. However, multiple-stage design is required for the mobile phone PAs due to the high gain requirement. In the multi-stage PA design, the main design challenge for broadbanding may not come from the output load matching, but rather from the interstage matching, which often turns out to be high-Q matching with narrowband characteristics [12], [13].

In this study, a two-stage stacked CMOS RF PA is developed for broadband ET operation to cover the entire low-band LTE frequencies from 0.65 to 1.0 GHz. The output stage is based on a Class-J architecture using the multi-section matching network with integrated Miller capacitors. Broadband matching in the interstage network is realized with a reconfigurable matching network using silicon-on-insulator (SOI) CMOS switches to select desired frequency bands. In this way, the matching BW limitation set by Bode–Fano criteria can be overcome. This paper is an extended version of our previous paper [5], which reported the overall design concept and the first results using a single reconfiguration switch. The extended paper contains a detailed operation principle and design procedure, as well as the updated results with wider RF BW using two reconfiguration switches in the interstage network.

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This paper is organized as follows. Section II gives a basic idea of the proposed broadband Class-J PA with a reconfigurable interstage matching network. In Section III, the detailed design procedure of the proposed PA is presented using SOI CMOS FETs. Also shown in this section is the design of the envelope amplifier (EA) fabricated in an SOI CMOS process. In Section IV, the measured PA characteristics are presented together with the time-domain waveform measurement to verify true Class-J operation. The entire ET PA system performance with a 20-MHz BW LTE signal across the entire frequency range is also demonstrated in this section.

II. Two-Stage Broadband Class-J PA

A. BW Limitation in Multi-Stage PAs and Proposed Solution

Generally, more than two-stage design is required to achieve the gain requirement for the handset RF PAs ($>$ 24 dB). In a two-stage RF PA, the BW limitation may not come from the output matching, but from high-Q interstage matching due to the excessively large input capacitances of the power cell. In other words, the broadband output load matching alone may not be sufficient in meeting the required PA specification in terms of efficiency, gain, and power. For example, if the BW of the interstage matching is small, the drive power to the main stage will not be sufficient at the band edges to meet the overall gain and power target, let alone the efficiency.

To investigate the BW limitation of the interstage matching, we have modeled the input of the power stage transistor as a series combination of a resistor, R, and a capacitor, C, which is a valid equivalent circuit representation of a common-source CMOS FET. For example, a CMOS triple-stacked power cell used in our work has an input capacitance (C) of 36 pF with a series resistance (R) of 1 Ω at 0.85 GHz. The theoretical BW limit of the interstage matching network can be expressed as (1) using the Bode–Fano criteria [14],

$$\int_0^\infty \frac{1}{\omega^2} \ln \frac{1}{|\Gamma(\omega)|} d\omega < \pi RC \tag{1}$$

where $\Gamma(\omega)$ is the reflection coefficient referenced to the optimum load impedance of the driver stage transistor. To estimate the BW limitation, we need to set the allowable mismatch, $|\Gamma(\omega)|$, for the interstage matching.

There can be two criteria in setting the allowable mismatch, $|\Gamma(\omega)|$. First, the overall efficiency of the two-stage PA should remain higher than a certain threshold across the entire BW. Even if the power stage remains unchanged in terms of gain and efficiency across the entire BW, the load mismatch to the driver stage will increase the overall dc current, which is the sum of the driver-stage current and the power-stage current. Fig. 1 shows the load–pull contours of the driver stage only. The red curve (in online version) with cross represents the driver load contour, which results in 50% increase in the driver-stage current while meeting the same output power target compared with the optimum driver-stage load point, shown as a blue dot (in online version). The actual two-stage stacked CMOS PA without the interstage reconfiguration is used in the load–pull simulation. The detailed PA circuit design will be described in Section III.

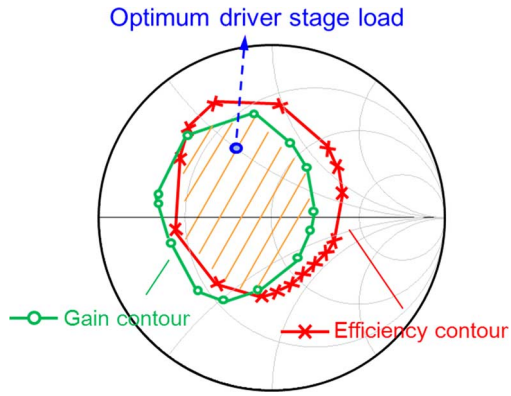


Fig. 1. Simulated driver-stage load–pull contour representing the load contours that generate the same output power as that available from the optimum load impedance shown with the blue dot (in online version). The red curve (in online version) with a cross represents the load contour that increases the driver current by 50%. The green curve (in online version) with a circle represents the load contour that decreases the gain by 6 dB. To meet both gain and efficiency targets, the driver-stage mismatch should stay within the shaded area across the entire BW.

Another criterion is the overall gain. The load mismatch to the driver stage results in the degradation of the driver gain, which should be less than a certain limit so that the overall gain can still meet the predefined system specification across the entire BW. We have used a 6-dB gain window as a criterion. The green curve (in online version) with a circle in Fig. 1 shows the load contour that results in 6-dB gain degradation in the driver stage while meeting the same output power target as that from the optimum load point [blue dot (in online version)]. To meet both gain and efficiency targets for the two-stage PA, the driver-stage load mismatch should stay within the overlap area between these two contours, represented as the shaded region in Fig. 1, across the entire RF BW.

From the circuit simulation of the two-stage PA used in this work, the maximum achievable fractional bandwidth (FB) is only 23.5% (0.75–0.95 GHz) to stay within the shaded region if a single-section matching is used for interstage matching. The BW can increase by employing a larger number of sections, but is still bound by (1), which applies to the case of the infinite number of sections. There is a practical limit in the number of sections for interstage matching in terms of the die size and the associated loss in the matching circuit. It is also worthwhile to note that the driver-stage mismatch analysis presented above is based on the assumption that the power stage is of infinite BW and does not impose any BW limitations, which of course is not always true in the practical PA design. The actual BW of the two-stage PA will be smaller than those predicted in our analysis.

To extend the FB above 40% using the two-stage PA design, which is required to cover all the LTE bands below 1 GHz using a single PA chain, we would need a different design methodology for interstage matching. In this work, a frequency-selective reconfigurable interstage matching network is proposed as a solution. The key idea is to divide the frequency range into several frequency sub-bands and change the matching component values of the interstage matching network according to

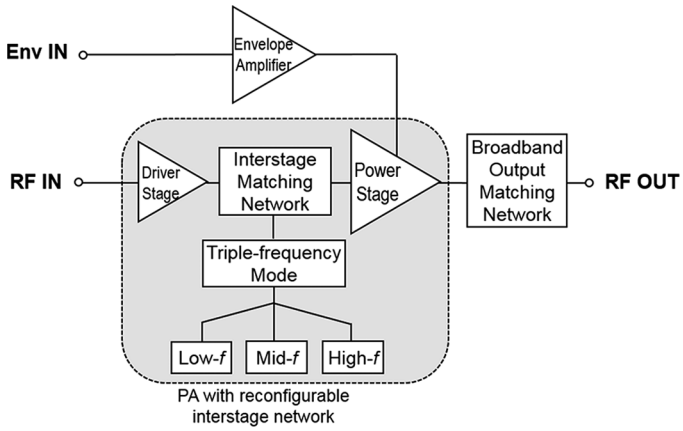


Fig. 2. Basic block diagram of the proposed broadband ET PA with reconfigurable interstage matching.

the sub-divided frequency bands. In this way, the aforementioned BW limitation can be overcome and the optimum load impedance can be presented to the driver stage at each sub-band.

Fig. 2 shows the overall block diagram of the proposed broadband ET PA with a reconfigurable interstage network. Overall efficiency enhancement at the back-off power is achieved through the use of ET, where the envelope signal is amplified by the EA and applied to the drain bias for dynamic bias modulation. The reconfigurable matching network is employed in the high-Q interstage matching network, where the three different modes are selected according the frequencies. Finally, the broadband output matching is implemented through the use of Class-J operation, as will be explained in Section II-B.

B. Output Matching Network

For Class-J operation, the output matching network should provide the optimum impedances at each harmonic frequency as governed by following three equations [15]:

$$Z_1 = \frac{2\sqrt{2}\cdot(V_{DD}-V_k)}{I_{\max}}\angle 45^\circ \tag{2}$$

$$Z_2 = -\frac{3\pi}{4}\cdot\frac{(V_{DD}-V_k)}{I_{\max}}\angle 90^\circ \tag{3}$$

$$Z_n(n>2) = 0. \tag{4}$$

The third condition is typically satisfied by assuming that third-order and higher order harmonic currents are short-circuited through the drain–source capacitance ($C_{\rm ds}$) of the power cell. If $C_{\rm ds}$ of the power cell is not large enough to short third harmonic currents, extra shunt capacitor is needed at the drain node of the power cell. In this work, as shown in Fig. 3(a), a triple-stacked CMOS FET with a unit gate width of 20 mm is used as a power cell, whose $C_{\rm ds}$ is 15.5 pF. The value of $C_{\rm ds}$ of the 20-mm unit transistor is extracted using the device model and confirmed by S-parameter simulation using Advanced Design System (ADS). The detailed equivalent circuit of the output portion of the triple stack cell is shown in Fig. 3(b), where the output capacitors across each FET stack are decomposed to the Miller capacitors. Based on this equivalent circuit, the overall

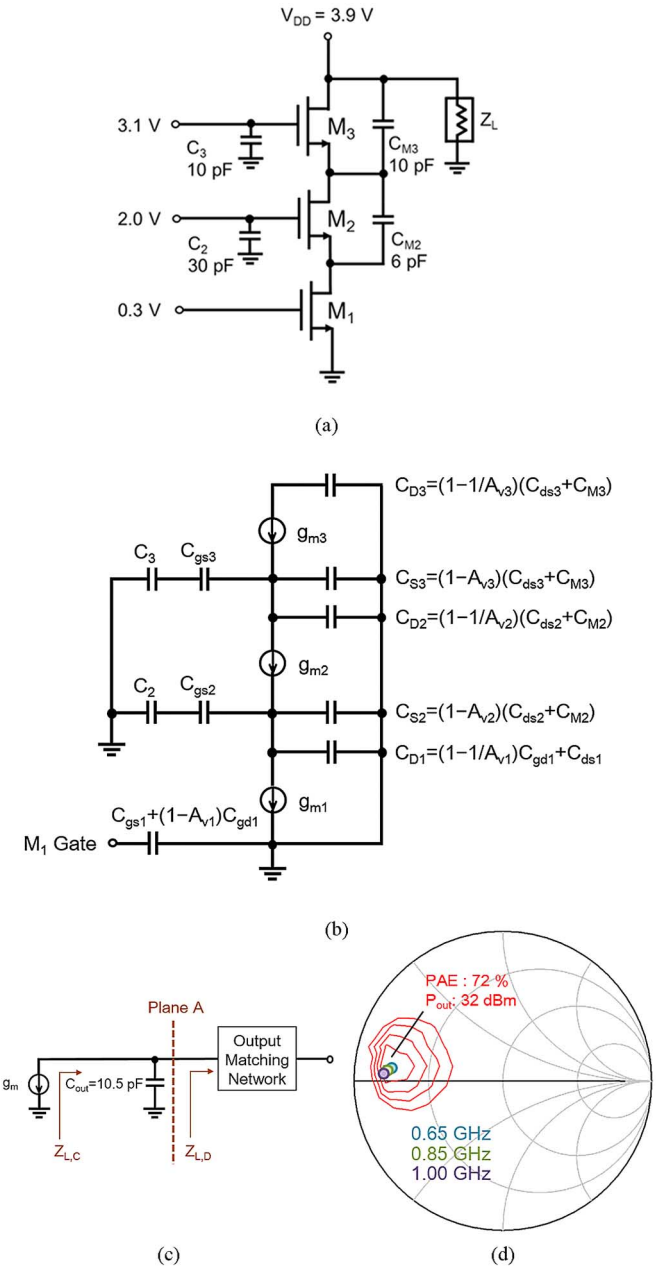


Fig. 3. (a) Schematic of the triple-stack power cell. (b) Detailed equivalent circuit of the power cell with the Miller capacitors decomposed. (c) Simplified equivalent circuit of the power cell. (d) Fundamental load–pull contours of the power cell simulated at plane A for 0.65, 0.85, and 1 GHz.

output capacitor ($C_{\rm out}$) of the triple stack is calculated to be 10.5 pF. The simplified equivalent circuit shown in Fig. 3(c) is used when calculating the load impedance at the current source plane. This overall output capacitance provides a reactance of only $-j6\ \Omega$ at third harmonic frequency (2.55 GHz), which is sufficient to short circuit the third harmonic current.

The load–pull simulation is performed at plane A shown in Fig. 3(c) at 0.65, 0.85, 1 GHz. For the load–pull simulation in Fig. 3, the input power and impedance are fixed at 21 dBm and 50 Ω, respectively, and V_{DD} is 3.9 V. The fundamental load was varied for load–pull simulation while the second harmonic impedance was fixed at the optimum values for PAE.

Fig. 3(d) shows the optimum load impedances for PAE at the plane A fundamental frequencies. The optimum load impedances at the fundamental frequencies are centered around $5.2 + j4.1\ \Omega$ from 0.65 to 1 GHz. It is worthwhile to note that $5.2 + j4.1\ \Omega$ is the impedance at the plane A ($Z_{L,D}$), which does not include the effect of C_{out}. The load impedance seen at the current generator plane ($Z_{L,C}$) is $7.2 + j3\ \Omega$. Even though it is not the ideal Class-J load, it stays within the Class-J load region and provides the optimum performance between the output power and the efficiency, as demonstrated in [16]; slight load tuning helps to increase the output power while achieving the similar level of PAEs. In this case, one then needs to design a broadband load matching circuit to satisfy the intrinsic impedances conditions of (3) and (4) at the harmonic frequencies while hitting the optimum load condition of (2) at the fundamental frequencies. As the optimal fundamental impedances have a low Q factor ($\sim$ 0.79), it can be possible to design the broadband matching network. There are numerous impedance-matching circuit topologies to realize broadband matching with a $1 : n$ impedance transform ratio [14], [17]. In this work, a two-section low-pass network consisting of transmission lines and two shunt capacitors is used to synthesize near-optimum load impedances from 0.65 to 1.0 GHz, corresponding to the FB of $\sim$40%. Detailed design of the load matching circuit and the simulation results are shown in Section III.

C. Reconfigurable Interstage Matching Network

The simulated driver impedances optimum for PAE are shown via dots in Fig. 4 for 0.65, 0.85, and 1.0 GHz. As in the load impedance simulation results in Fig. 4(b), the optimum driver impedances are scattered around $21 + j20\ \Omega$, and the input impedances seen looking into the power cell are around $1.1 - j7.2\ \Omega$. The corresponding Q factor is around 6.5, which is much higher than that of the optimum load impedance of the power cell (0.79) in Fig. 3(d). To show the challenges of a typical interstage circuit to transform the input impedance of the power cell to the optimum driver impedance across the entire frequency range, the impedance trajectory versus frequency with a typical C–L–C interstage matching network optimized at 0.85 GHz is also plotted in Fig. 4(a). It can be noticed from Fig. 4(a) that the driver impedance trajectory sweeps almost half of the Smith chart from 0.65 to 1 GHz, resulting in large impedance mismatches at the band edges. This will lead to the excessive power consumption from the driver stage, and makes it impossible to meet the overall PAE target from the two-stage PA, especially at low- and high-frequency edges.

Instead of a fixed matching network, a reconfigurable interstage matching network is employed in this work to reconfigure the interstage matching according to the frequency of operation. The entire frequency range is divided into three sub-bands, low from 0.65 to 0.8 GHz, mid from 0.8 to 0.9 GHz, and high from 0.9 to 1 GHz. Depending on the frequency of operation, the interstage matching component is reconfigured to provide the optimum matching for each sub-band. In this way, a BW requirement can be reduced. For example, when the RF PA is operated in the mid-frequency sub-band (0.8–0.9 GHz), the interstage matching network remains in the mid-frequency mode (MFM), which is an "as-is" state, to provide the optimum driver

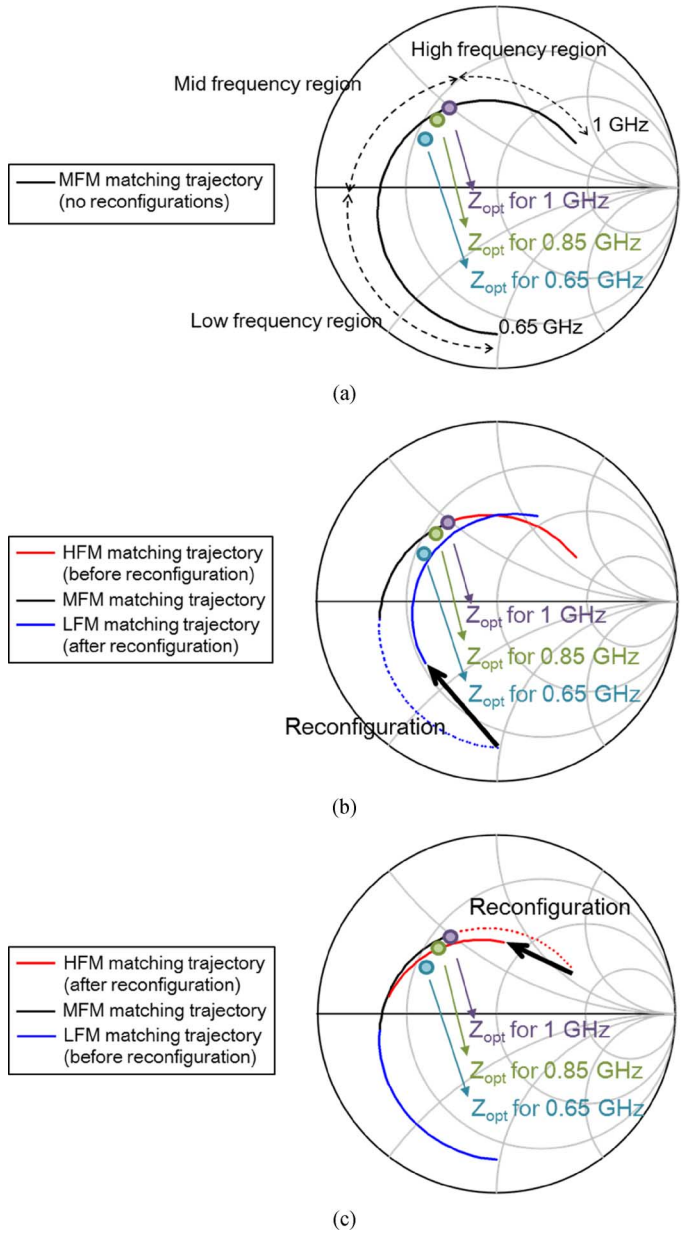


Fig. 4. Simulated optimum load impedances of the driver stage at 0.65, 0.85, and 1 GHz and the driver load trajectory from 0.65 to 1.0 GHz. (a) Without any interstage reconfiguration. (b) With LFM reconfiguration. (c) With HFM reconfiguration.

impedance at the 0.85 GHz, as shown via the black curve in Fig. 4(a). When operated in the low-frequency sub-band, the interstage matching network is reconfigured to the low-frequency mode (LFM), where the matching network components are optimized for 0.75 GHz, as depicted via the blue curve (in online version) in Fig. 4(b). Similarly, for the high-frequency sub-band, the interstage matching network is reconfigured to the high-frequency mode (HFM) for optimum performance at 0.95 GHz, as represented via the red curve (in online version) in the Fig. 4(c). The additional components required for the interstage circuit reconfiguration are two RF switches and extra capacitor and inductor. A detailed design procedure to implement a reconfigurable interstage matching network is presented in Section III.

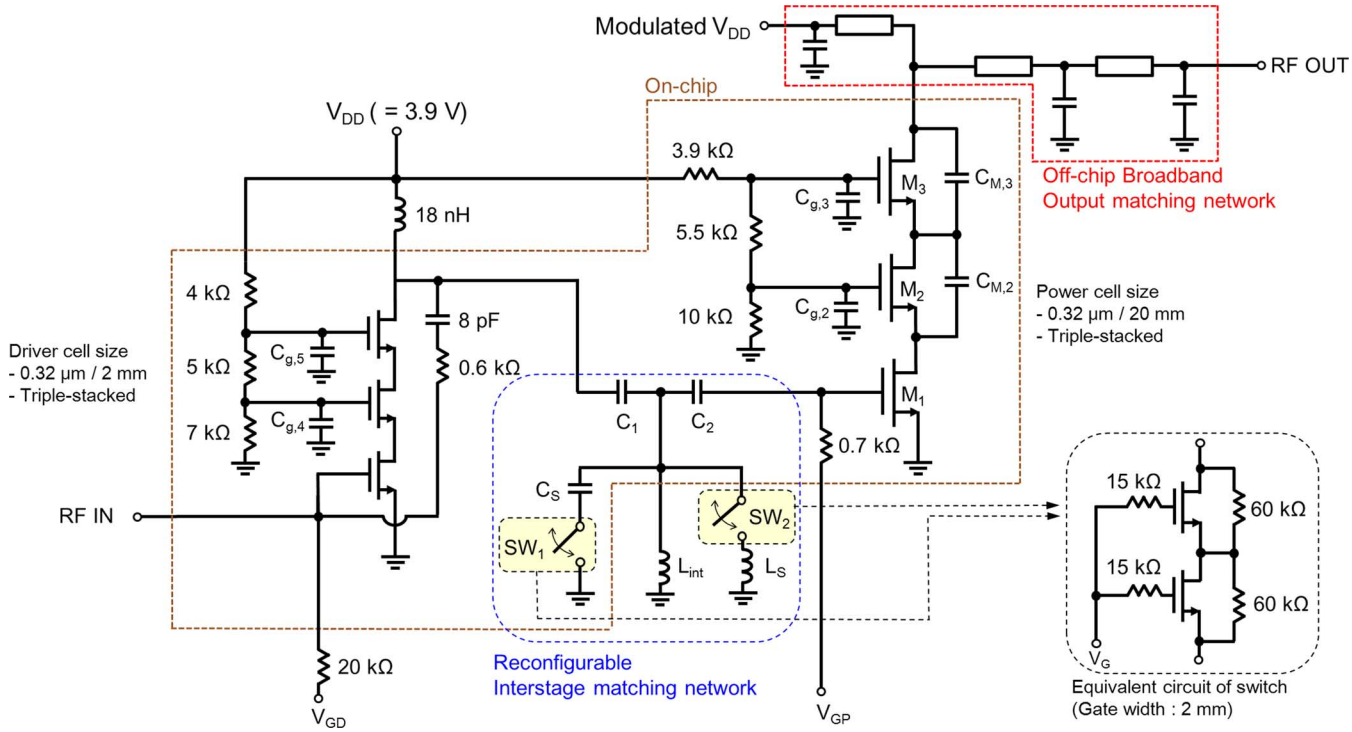


Fig. 5. Detailed circuit schematic of the proposed two-stage CMOS stacked PA with reconfigurable interstage network.

III. Design and Implementation of ET PA

A. PA Design

An overall circuit schematic of a proposed two-stage Class-J CMOS PA is shown in Fig. 5. A triple-stacked FET structure is selected for both stages to overcome the low breakdown-voltage problem of CMOS FETs [18]. The gate widths of the unit FETs are 2 and 20 mm for the driver stage and power stage, respectively. Gate terminal capacitors, $C_{g,5}$, $C_{g,4}$, $C_{g,3}$, and $C_{g,2}$ are designed to 3, 6, 10, and 30 pF, respectively, to ensure that the voltage swing can be evenly distributed to each FET in the stack. As shown in Fig. 5, the gate bias of the common-source FET (M_1) is applied directly through a bias resistor while the gate biases of the common-gate (CG) transistors (M_2 and M_3) are applied using a resistor-based voltage dividing circuit. The gate bias level for the common-source FET is set for Class-B operation to generate the half-sinusoid current, while the biases to the CG FETs are selected to achieve uniform voltage swing between M_2 and M_3. The gate length for all FETs is 0.32 μm, which is selected based on the breakdown requirement.

Two Miller capacitors ($C_{\mathrm{M},3,} = 10$ pF, $C_{\mathrm{M},2} = 6$ pF) are added across M_3 and M_2 to adjust the second harmonic impedance seen at the inner stacks of the power cell. Fig. 6(a) shows the second harmonic load–pull simulation at the drain node of M_2, which was performed in MFM at the drain of M_2, while the output impedance of the entire triple stack was fixed at the optimal load impedance shown in Fig. 3(d). The same conditions were used for V_{DD}, input power, and impedance as the fundamental load–pull simulation shown in Fig. 3. Fig. 6(a) clearly shows that the high-efficiency region is shifted from the capacitive to inductive region due to the reactive effect of C_{ds} in M_2. Unfortunately, the load impedance seen from M_2, which is the input source impedance

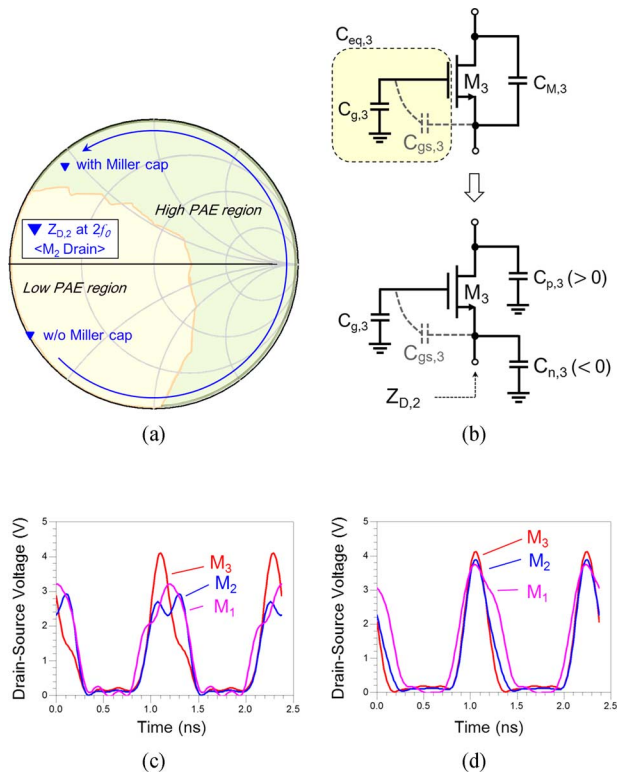


Fig. 6. (a) Simulated load–pull contour and load impedance presented to M_2 drain with and without Miller capacitor. (b) Effect of Miller capacitance. Simulated drain voltage waveforms. (c) Without Miller capacitors. (d) With Miller capacitors.

of M_3, at the second harmonic frequency lies in the capacitive region, resulting in low PAE. This is due to the large input capacitance of M_3 ($C_{\mathrm{eq},3}$), which consists of $C_{\mathrm{g},3}$ and $C_{\mathrm{gs},3}$, where $C_{\mathrm{gs},3}$ is the gate–source capacitances of the M_3. This

problem can be solved by adding a Miller capacitor across the drain and source terminals of M_3, which transforms the second harmonic impedance to the inductive region by adding negative capacitance. As shown in Fig. 6(b), the Miller capacitor can be replaced with two equivalent shunt capacitors at the source ($C_{\mathrm{n},3}$) and drain ($C_{\mathrm{p},3}$) terminals. The shunt capacitor values are expressed as

$$C_{\mathrm{p},3} = \left(1 - \frac{1}{A_{v,3}}\right) \cdot C_{\mathrm{M},3} \tag{5}$$

$$C_{\mathrm{n},3} = (1 - A_{v,3}) \cdot C_{\mathrm{M},3} \tag{6}$$

where $A_{v,3}$ is an intrinsic voltage gain of the CG FET (M_3) and $C_{\mathrm{M},3}$ is the Miller capacitor across the source and drain terminals of the CG-FET. As the CG-FET has positive voltage gain ($A_{v,3}$) greater than unity, the equivalent capacitor at the source node ($C_{\mathrm{n},3}$) has large negative capacitance. The positive term ($C_{\mathrm{p},3}$) can be used as a part of output capacitances for satisfying (4). The negative capacitor ($C_{\mathrm{n},3}$) effectively transforms the second harmonic load impedance of M_2 to the high PAE region by canceling out a portion of $C_{\mathrm{eq},3}$. This effect is shown in the simulated second harmonic load impedance of M_2 in Fig. 6(a). Similar effects can be seen for M_1 harmonic load impedances from Miller compensation applied to M_2.

The effect of Miller capacitors is also verified by the voltage waveform analysis in the power cell. Fig. 6(c) is the simulated drain–source voltage swing of M_1, M_2, and M_3 without Miller capacitors. Unlike the drain–source voltage swing across M_3, which is close to the ideal waveform of half sinusoid, the voltage swing across M_1 and M_2 are heavily distorted due to the effect of capacitive second harmonic load impedance. The effect of Miller capacitances can be clearly observed in the waveform plot of Fig. 6(d), where the same waveform simulation is performed by adding two Miller capacitors. Due to the negative capacitance effect, the overall capacitive loading has been vastly reduced and the voltage swing is now recovered to almost half sinusoid, close to the ideal Class-J operation.

The broadband output matching network is realized using the two-section low-pass matching network with an impedance transform ratio of 1:10 extracted from [17]. The design parameters of the output matching network are shown in Fig. 7(a) while the simulated load impedance trajectory from 0.65 to 1 GHz is shown in Fig. 7(b). The fundamental load impedance from 0.65 to 1 GHz is centered around the target impedance of $5.2 + j4.1\ \Omega$, which was calculated from the load–pull simulation of the power cell shown in Fig. 3(d). After de-embedding the overall output capacitance (C_{out}) of 10.5 pF, the fundamental impedance (Z_{Fund}) and the second harmonic impedance (Z_{H2}) at the current generator plane are calculated as $7.2 + j3\ \Omega$ and $0.11 - j12\ \Omega$, respectively, at 0.85 GHz [see Fig. 7(c)]. These impedances show the typical characteristics of the Class-J PA with the inductive fundamental load and capacitive second harmonic load. Simulated insertion loss of the output matching network at 0.85 GHz is 0.3 dB.

To verify Class-J operation across the entire BW, the voltage and current waveforms have been simulated at the current generator plane of the power cell at $P1$ dB condition. At the center frequency of 0.85 GHz shown in Fig. 8(a), the voltage waveform shows a clean half sinusoid with the corresponding PAE

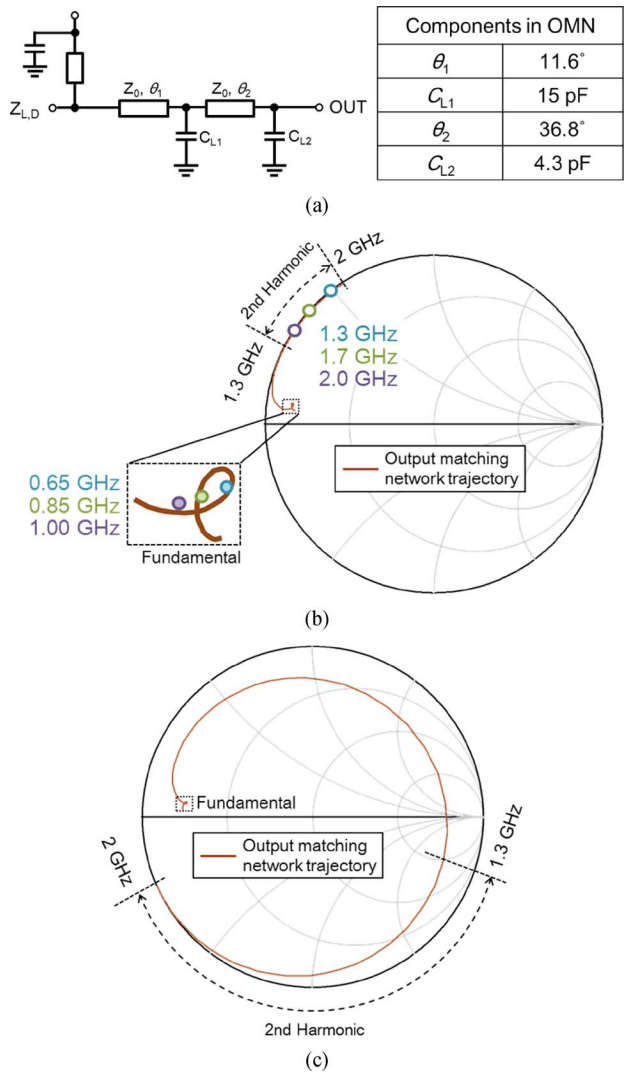


Fig. 7. (a) Circuit schematic of the two-section low-pass matching network used as the output load matching. (b) Optimum load impedance targets from 0.65 to 1.0 GHz and the simulated impedance trajectory of the output load matching circuit at plane A ($Z_{L,D}$). (c) Simulated impedance trajectory of the output load matching circuit at the current generator plane ($Z_{L,C}$).

of 72.3%, which validates optimal Class-J operation. As the operating frequency is lowered, the third harmonic currents are no longer shorted through C_{out} of the power cell, which builds up third harmonic voltage components and distorts the voltage waveform as shown in the simulation results at 0.65 GHz [see Fig. 8(b)]. The distortion in the voltage waveform increases the overlap between the current and voltage waveforms and degrades PAE to 64.4%. On the other hand, as the frequency increases, the peak voltage level decreases since the second harmonic current bypasses through C_{out} and fails to build up the second harmonic voltage, as shown in the simulation results at 1 GHz [see Fig. 8(c)]. The corresponding PAE degradation is around 6% at 1 GHz. This basically shows that there is a practical limit in extending the BW due to the nonideal Class-J operations of the power cell at the band edges. The goal of the reconfigurable interstage matching network is to extend the BW of the entire two-stage PA as wide as the limit set by the power cell and the output matching network used in this work.

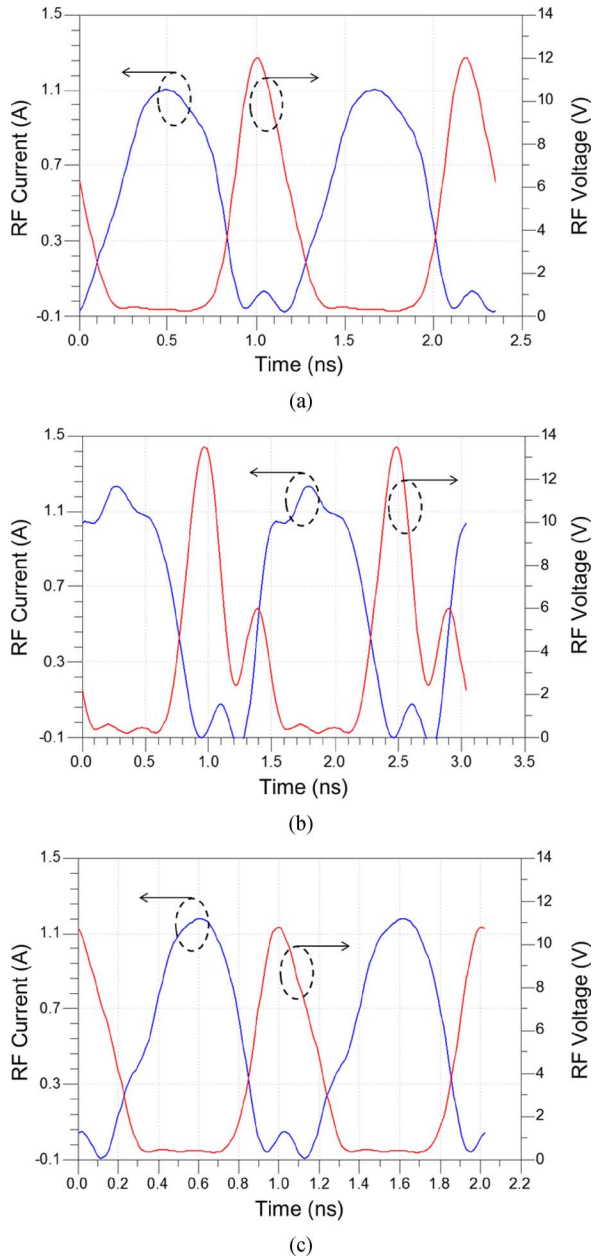


Fig. 8. Simulated voltage and current waveforms at the current generator plane of the power cell at: (a) 0.85 GHz, (b) 0.65 GHz, and (c) 1 GHz.

The reconfigurable interstage network introduced in the previous section is realized using two RF switches, which are fabricated using the same SOI CMOS process. A 2-mm double-stacked N-channel FET (NFET) is used as a switch unit cell. One switch (SW_1) is integrated with the driver and power cell FETs, and the other switch (SW_2) is externally added for the HFM operation, as shown in Fig. 5. The overall interstage matching network is a high-pass network consisting of a series C_1 ($=$ 5 pF), a shunt L_{int} ($=$ 1.5 nH), and a series C_2 ($=$ 20 pF). For matching reconfiguration, the equivalent inductance of L_{int} is changed according to the operation frequency. When the RF PA is operated in the MFM (0.8–0.9 GHz), both switches remain in the off-state to provide the "as-is" shunt inductance ($L_{\mathrm{int}} = 1.5$ nH). This provides the optimum driver load impedance of $21.3 + j19.8\ \Omega$ at 0.85 GHz.

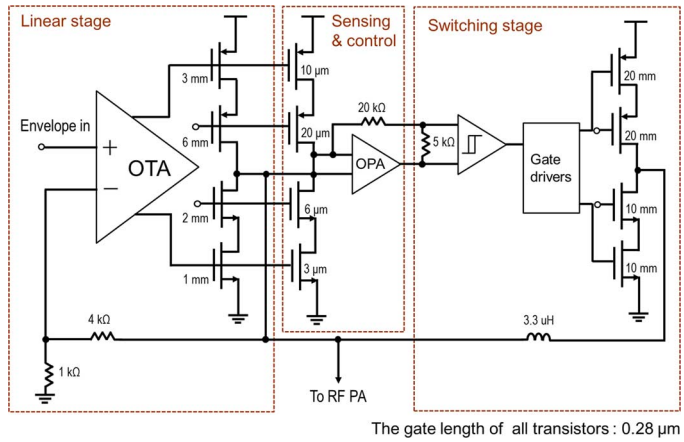


Fig. 9. Schematic of the designed EA.

Therefore, the overall PAE peaks to 72.3% at the 0.85 GHz degrades at the band edges. To boost the efficiencies at lower frequencies, the interstage matching network is reconfigured to the LFM (0.65–0.8 GHz) by turning on SW_1, which effectively adds a shunt capacitance, C_S, and thus increases the equivalent shunt inductance to $L_{\mathrm{int}}/(1 - \omega^2 \cdot L_{\mathrm{int}} \cdot C_S)$. In this case, the optimum load impedance is presented to the driver stage at 0.7 GHz, where PAE improvement as much as 8% is achieved from the simulation. On the other hand, for efficiency boosting in the HFM (0.9–1 GHz), SW_2 is turned on to add a shunt inductance ($L_S = 7$ nH), which reduces the equivalent shunt inductance to $L_{\mathrm{int}} \cdot L_S/(L_{\mathrm{int}} + L_S)$. The simulated PAE improvement by the HFM reconfiguration is as much as 5% at 1 GHz.

B. EA Design

We have also designed an EA to demonstrate the entire ET PA system performance. A typical hybrid type EA is designed to achieve both high efficiency and linearity [1]–[8]. Fig. 9 shows an overall schematic of the designed EA. Output FETs for both stages are cascoded to avoid drain–source voltage breakdown thus operated with 3.9-V V_{DD} supply [19]. According to the small-signal simulation, the gain BW product of the linear stage is 170 MHz with 70° phase margin, which is sufficient to handle 20-MHz BW LTE signal. Fig. 10 shows the shaping function used in the ET testing to avoid the device shut down at the low envelope levels [7]. The measured efficiency of the EA with 20-MHz BW, 6.7-dB PAPR quadrature phase-shift keying (QPSK) LTE envelope signal with 7.5-Ω resistive load is plotted in Fig. 11, showing 74% average efficiency. This efficiency is smaller than the-state-of-the-art results of 86% [20] due to less sophisticated design. However, since the main purpose of this work is to demonstrate the broadband ET PA with a reconfigurable network, all the ET system measurements were taken with the fabricated EA.

IV. Measurement Results

A two-stage stacked-FET PA with the proposed reconfigureable interstage matching network is fabricated using a 0.32-μm SOI CMOS process. Fig. 12(a) and (b) shows die photographs of the fabricated EA and PA, respectively. The chips are mounted on a 400-μm thick, 5 cm × 5 cm sized FR4 PCB ($\varepsilon_r \sim 4.6$, $\tan\delta$

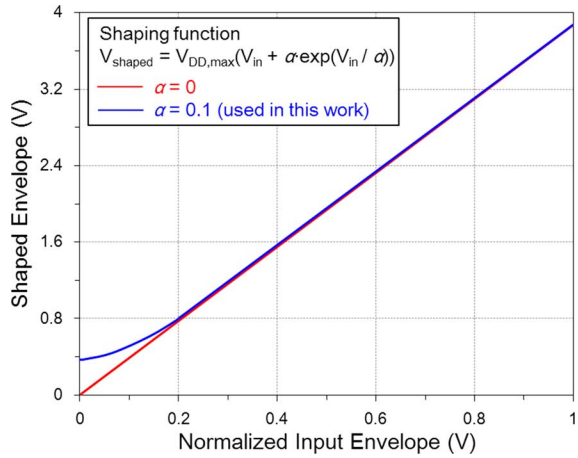


Fig. 10. Envelope shaping function used for ET testing.

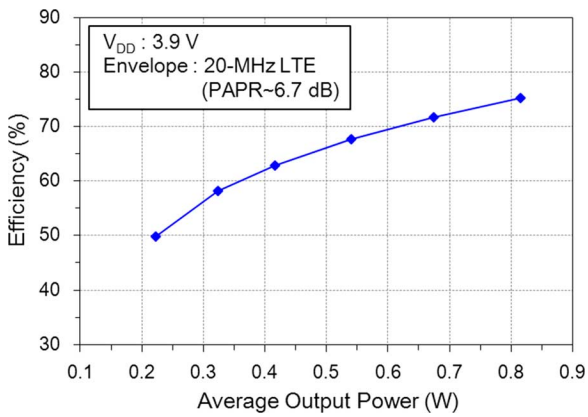
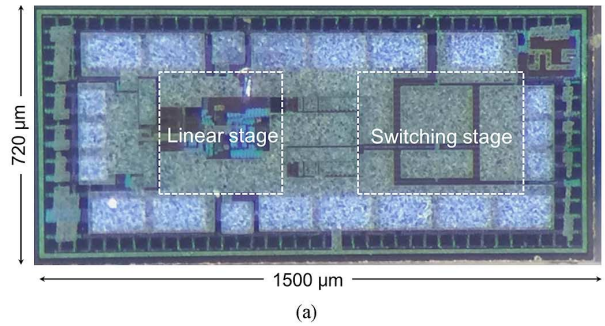
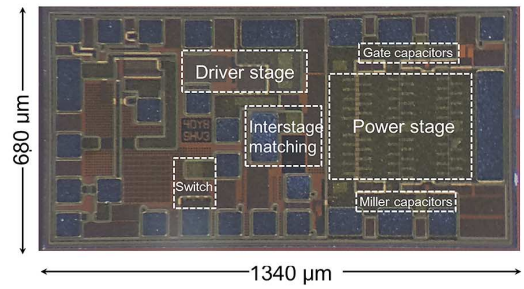


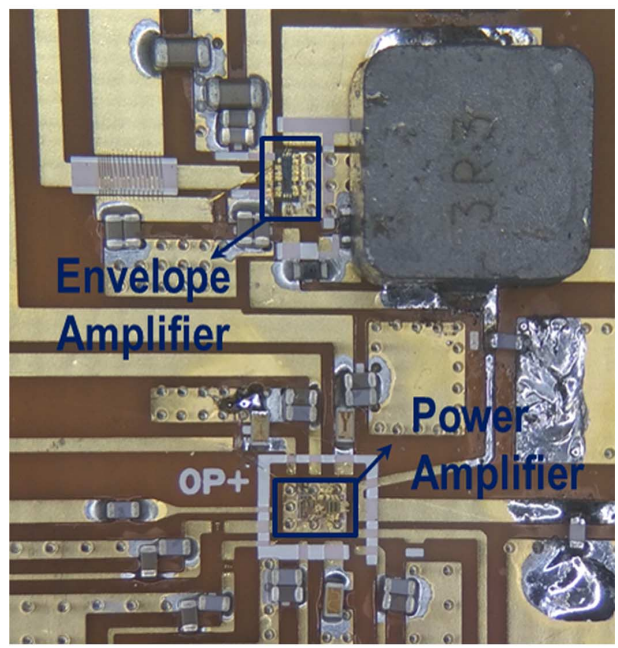
Fig. 11. Measured efficiency of the EA when the input signal is the envelope of 20-MHz BW 6.7-dB PAPR QPSK LTE signal.



(a)



(b)



(c)

Fig. 12. Chip photographs of the fabricated: (a) EA and (b) two-stage PA. (c) Photograph of the test module.

$= 0.025$), where the load matching circuits are realized and external components are mounted. The circuit components outside the dotted box in Fig. 5 are off-chip components mounted on the PCB.

Fig. 13 shows the measured small-signal S-parameters of the fabricated PA module. The PA shows different gain and return-loss profiles according to each frequency mode. Fig. 14 shows continuous wave (CW) power sweep data measured at 0.65 GHz to demonstrate the effect of the interstage reconfiguration. The output power is 29.8 dBm with 52.3% peak PAE without interstage reconfiguration. With interstage reconfiguration, peak PAE improves by ~9%, while the output power and gain increase by 1.2 and 1.9 dB, respectively. $P1$ dB shows similar improvement from 28.6 to 29.7 dBm. Fig. 15 shows the measurement result of the intermodulation distortion (IMD) using two-tone signals with 20-MHz tone spacing.

Broadband CW performance of the PA is measured from 0.65 to 1.05 GHz with and without interstage reconfiguration, as shown in Fig. 16. The applied gate and drain biases for both stages are 0.3 and 3.9 V, respectively, resulting in a total quiescent current of 70 mA, and the CW test was performed at the maximum PAE point at each frequency. As shown in Fig. 16(a), a maximum PAE of 69.2% is observed at 0.85 GHz, which corresponds to the "as-is" state in MFM. Without the interstage reconfiguration, PAEs degrade abruptly at band edges. With the interstage reconfiguration, the peak PAEs maintain higher than 60% from 0.65 to 1.03 GHz, corresponding to an FB of 45%. The efficiency boosting is most pronounced in LFM (0.65–0.8 GHz), showing PAE improvement up to 9%. In HFM (0.9–1 GHz), PAE improvement up to 5% has been achieved. The measured output power over the entire BW ranges from 29.7 to 31.1 dBm while the gain stays between 25.1 and 25.8 dB.

Class-J operation is experimentally verified across the entire frequency BW by measuring the voltage waveform at the drain node of the power stage, as shown in Fig. 17. For this measurement, we used an Agilent N2751A differential probe, which has only 700-fF internal capacitance. Since the output of the power

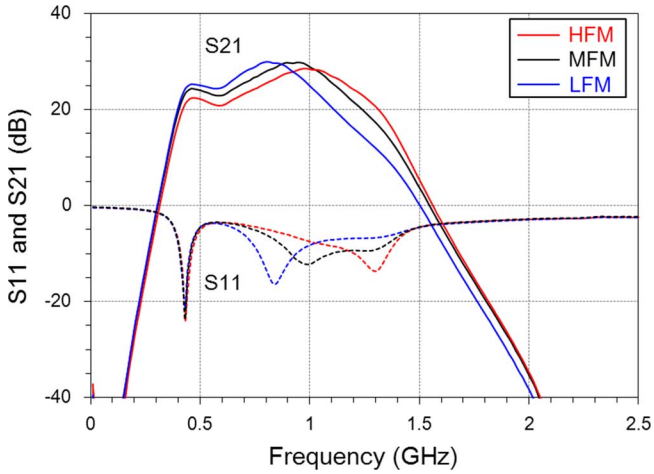


Fig. 13. Measured small-signal S-parameters at three different frequency modes.

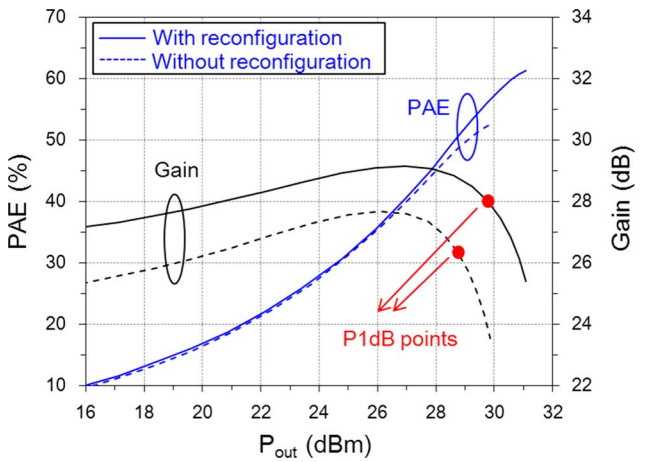


Fig. 14. Measured CW power sweep data of the PA at 0.65 GHz with and without interstage reconfiguration.

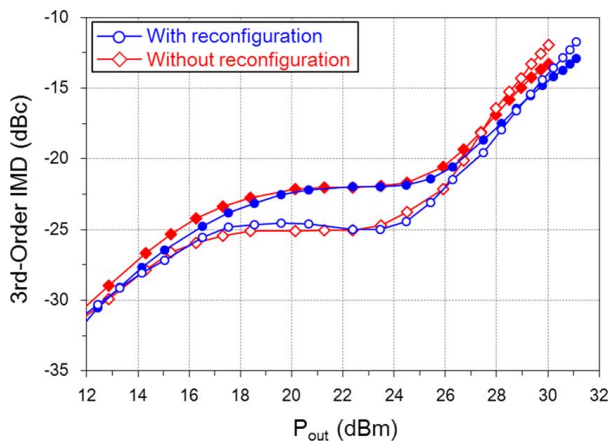


Fig. 15. Measured IMD characteristics of the PA at 0.7 GHz with and without interstage reconfiguration. (filled: lower IMD, hollow: upper IMD).

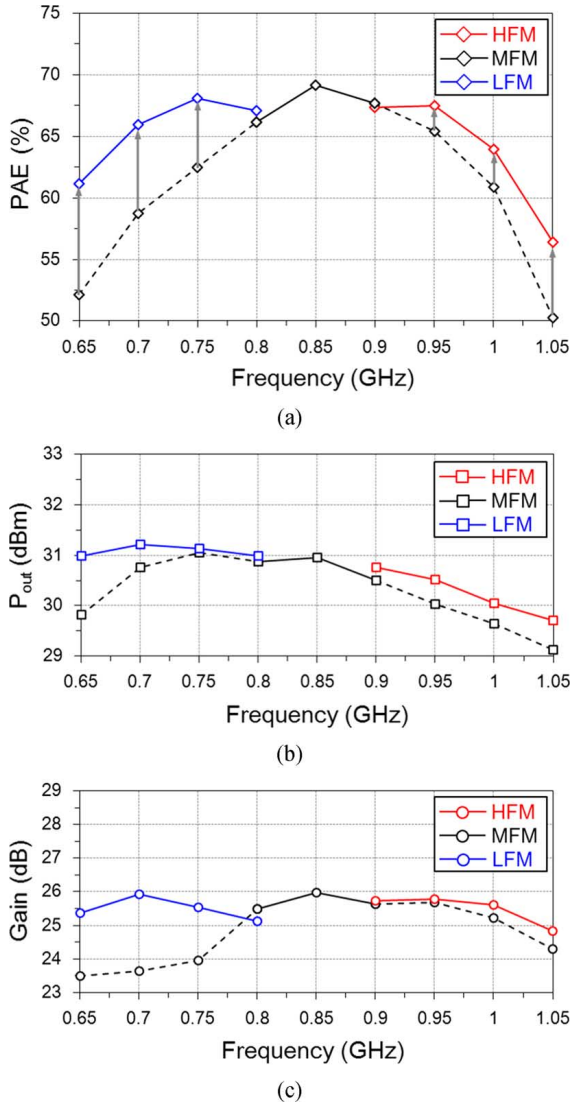


Fig. 16. Measured CW performance of the fabricated PA from 0.65 to 1.05 GHz. (a) PAE. (b) Output power. (c) Gain. The test was performed at the output power that shows the highest PAE at each frequency.

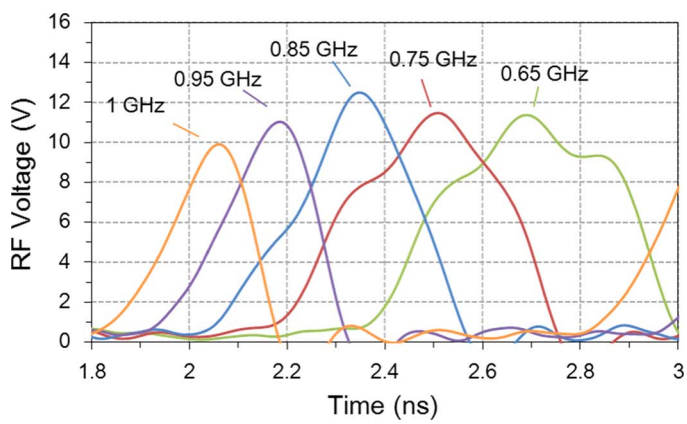


Fig. 17. Measured voltage waveforms at the drain node of the power cell.

cell is heavily loaded by C_{out} of the power cell itself, the additional 700 fF from the differential probe does not significantly affect the output matching. Half-sinusoidal voltage waveforms are well maintained at mid-frequencies, as predicted from the simulation results in Fig. 8(a). Distortions at the low frequencies due to the finite third voltage component, predicted in Fig. 8(b), are also clearly observed in this measurement. Likewise, the reduced voltage peaks are observed at high frequencies, as predicted in Fig. 8(c).

TABLE I
PERFORMANCE COMPARISON TABLE OF BROADBAND HIGH EFFICIENCY (>60% CW PAE) PAs

Reference	Bandwidth (GHz)	Bandwidth (%)	PA Technology	No. of Stage	P_{out} (dBm)	PAE (%)	DE/CE[1] (%)	Gain (dB)	V_{DD} (V)
[22]	1.4~2.0	35	0.28-μm CMOS	Two	23	60~67	62~72[4]	-	2.5
[23]	0.6~0.85	34	65-nm EDCMOS[2]	Two	30	60~65[3]	70~76	16	5
[10]	0.6~0.7	15	0.35-μm SiGe BiCMOS	Single	30.9~31.5	-	60~68.9[3]	10	4.2
[4]	0.65~1.05	47	0.35-μm SiGe BiCMOS	Single	31.5~33.1	61.2~72.1	65~74	12.5	5
This Work	0.65~1.03	45	0.32-μm SOI CMOS	Two	29.7~31.1	60~69.2	62.7~75.6[4]	25.1~25.8	3.9

[1] Drain efficiency/collector efficiency
[2] Extended-drain, thick-oxide device
[3] This result is graphically estimated.
[4] Drain efficiency of the power stage only

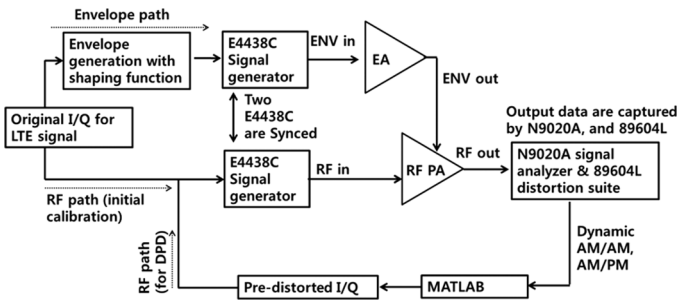


Fig. 18. Measurement setup used for testing ET PA system.

Table I compares CW performance of the published broadband PAs showing PAEs higher than 60%. The PA of this work shows 45% FB (for 60% PAE or higher).

The performance of the entire ET PA system consisting of the fabricated two-stage ET PA and EA is measured using a fully loaded 20-MHz BW 6.7-dB PAPR QPSK-modulated LTE signal. Fig. 18 is a block diagram of the ET PA measurement setup [21]. The input envelope to the EA is generated using original I/Q data of the LTE signal and the exponential shaping function shown in Fig. 10. The input envelope and original I/Q data are then downloaded to two synchronized Agilent E4438C signal generators so that one works as an envelope source while the other works as an RF source. The output of the ET PA is captured using an Agilent N9020A signal analyzer, and the dynamic characteristics are measured using 89604L distortion suite. To correct for the phase distortions in the stacked CMOS RF PA, a simple memoryless digital pre-distortion is used to linearize the ET PA system. The pre-distorted I/Q are re-downloaded to the RF signal generator and then up-converted again to test the ET PA with a pre-distorted signal.

To show the effect of interstage reconfiguration, the ET PA system is measured at 0.7 GHz using 20-MHz BW LTE signals at 0.7 GHz with and without interstage reconfiguration. The power sweep data is shown in Fig. 19. The QPSK-modulated LTE signal shows a PAPR of 6.7 dB with 0.01% probability. The gain and PAE of the standalone RF PA (non-ET, fixed bias mode) is also shown in the same chart as a reference. The overall system PAE at the maximum output power (26 dBm) of the ET PA with interstage reconfiguration is 42.2%, which corresponds to 2.2% efficiency improvement. The overall system PAE includes the power consumption from the EA, RF PA, and loss from matching networks. Compared with the standalone RF PA case, the ET PA shows an efficiency boost up to 4.8%.

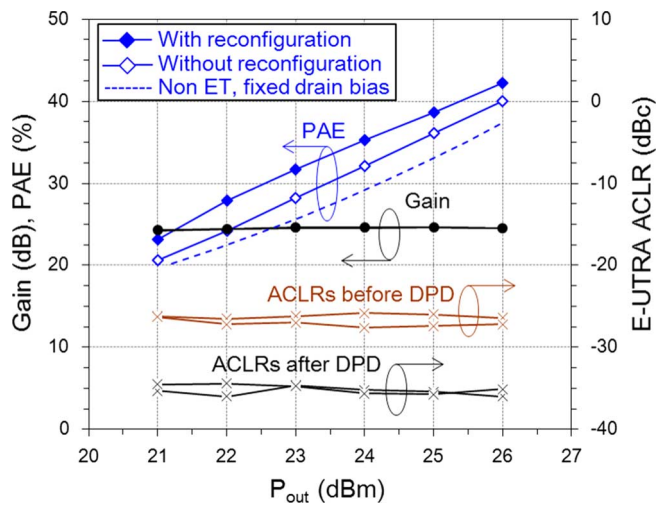


Fig. 19. Measured performance of the overall ET PA system as a function of the output power using 20-MHz LTE signal at 0.7 GHz with and without interstage reconfiguration.

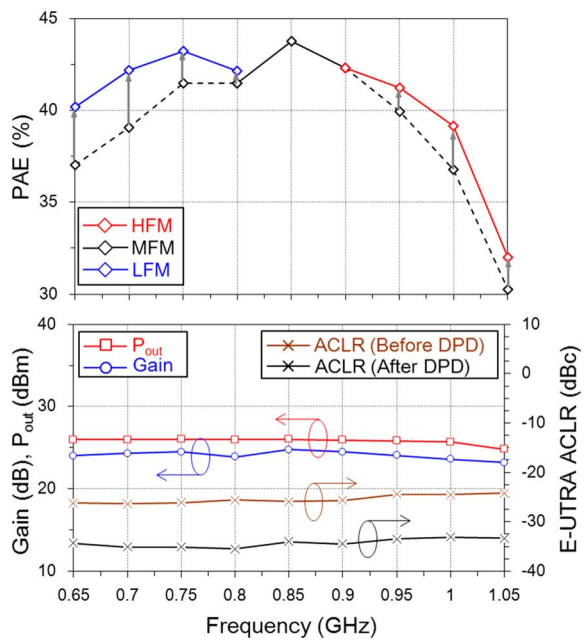


Fig. 20. Measured performance of the overall ET PA system using 20-MHz LTE signal from 0.65 to 1.05 GHz.

The evolved universal terrestrial radio access (E-UTRA) adjacent channel leakage ratio (ACLR) after digital pre-distortion at

TABLE II
PERFORMANCE COMPARISON TABLE OF BROADBAND LTE MOBILE TERMINALS

Reference	Frequency (GHz)	RF FBW[1] (%)	Signal BW (MHz)	PAPR (dB)	PA Technology	P_{out} (dBm)	PAE[2] (%)	E-UTRA ACLR (dBc)	Output matching	V_{DD} (V)
[1]	1.85	16	10	7.5	GaAs HBT	27.8	39	-34	Off-chip	3.4
[2]	1.7	16	10	7.5	GaAs HBT	27	39.5	-33.1	Off-chip	3.4
[3]	1.85	16	10	7.5	0.18-μm CMOS	26	34.1	-34.2	Off-chip	5
[4]	0.7	-	10	7.5	0.35-μm SiGe BiCMOS	27.6	36.4	-	Off-chip	5
			20	7.5	0.35-μm SiGe BiCMOS	27.4	35.6			
[5]	0.85	42	10	6.7	0.32-μm SOI CMOS	25	44	-35.5	Off-chip	3.5
[6]	1.7	16	10	7.5	0.18-μm CMOS	26.5	38.6	-35.3	On-chip	3.5
[7]	2.535	-	20	6.6	GaAs HBT	29	43	-	Off-chip	6
[8]	0.837	-	20	6.7	0.32-μm SOI CMOS	25.9	45.9	-33	Off-chip	3.4
This Work	0.85	47	20	6.7	0.32-μm SOI CMOS	26.1	43.8	-34	Off-chip	3.9

[1] RF signal fractional bandwidth
[2] Peak value within the frequency range

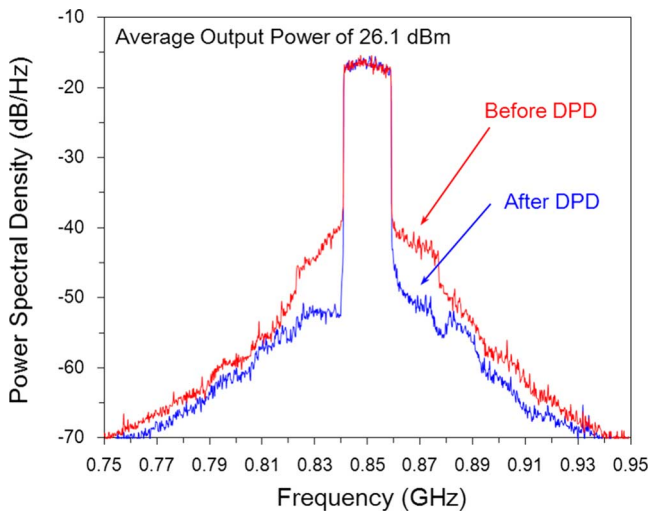


Fig. 21. Measured output power spectrum of the entire ET PA system using 20-MHz LTE signals before and after memoryless digital pre-distortion.

the 26 dBm is measured to −35.1 dBc, which corresponds to a 5.1-dB margin from the system specification.

To show the BW performance, the ET PA system is measured using the same 20-MHz LTE signal while sweeping the carrier frequencies from 0.65 to 1.05 GHz, as shown in Fig. 20. The maximum overall system PAE of 43.8% is achieved at 0.85 GHz with −34-dBc E-UTRA ACLR. With the interstage reconfiguration, the frequency BW showing higher than 40% PAE is extended from 0.225 GHz (27% BW) to 0.32 GHz (40% BW). The gain of the ET PA across the entire BW stays between 23.4 and 24.8 dB while the output power is between 25.4 and 26.1 dBm. The measured E-UTRA ACLRs across the entire test BW is better than −33 dBc.

Fig. 21 is the measured output spectrum of the ET PA at 0.85 GHz with the output power of 26.1 dBm with and without pre-distortion. The digital pre-distortion used in this work improves ACLR by 8.4 dB.

Table II is a performance comparison table for state-of-the-art broadband ET PA system for ET application. Even if a CMOS FET used in this work, our work shows the best system PAE among the published works, including GaAs HBT and SiGe BiCMOS PAs.

V. CONCLUSIONS

In this study, we have developed a broadband two-stage SOI CMOS stacked-FET PA with a reconfigurable interstage matching network for ET application. The power stage is based on a Class-J mode of operation, where output matching is realized using a two-section low-pass network. To guarantee a Class-J mode of operation for the inner stacked FETs as well, Miller capacitors have been added across the drain–source terminals of the CG FETs in the stack.

With the broadband output matching, the practical BW limitation to guarantee high overall gain and PAE over the entire BW comes from high-Q interstage matching. To overcome the BW limitation imposed by Bode–Fano criteria, a reconfigurable matching network is employed between the two stacked FETs. Two RF switches made of the same SOI CMOS process as the PAs have been employed to offer three different matching modes according to the operation frequency. This is achieved by changing the effective inductance value of the shunt inductor in the high-pass C–L–C interstage network. The fabricated PA shows CW efficiencies in excess of 60% from 0.65 to 1.03 GHz. When tested with an EA, the overall ET system efficiency higher than 40% has been achieved using 20-MHz LTE signals from 0.65 to 0.97 GHz. The time-domain waveform measurement shows that the efficiency degradation at the extreme band edges arises from nonideal output matching as the PA deviates from the ideal Class-J mode of operation, as expected from the simulation results. This work represents one of the widest RF BW demonstration for LTE ET PAs for mobile phone applications. As the number of LTE bands increases, the need for PA sharing and wideband operation will ever increase. The proposed idea of reconfigurable interstage matching can provide a practical solution to the BW problems for LTE PAs.

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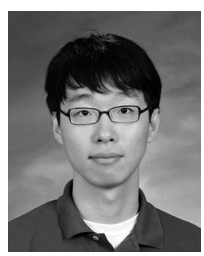

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