A 28/60 GHz Dual-band Power Amplifier

Asad Ali Nawaz[1], John D. Albrecht[2] and Ahmet Cagri Ulusoy[3]
Department of Electrical and Computer Engineering, Michigan State University, USA
[1]nawazasa@msu.edu, [2]jalbrech@msu.edu, [3]ulusoy@msu.edu

***Abstract*— A 0.13-µm SiGe BiCMOS dual-band power amplifier (PA) is developed which can be operated at 28 GHz or 60 GHz. The PA employs an LC tank at the input to perform dual-band impedance matching, while the output is switched from one band to the other using a tunable stub. The stub is made tunable by using an HBT switch, which reduces the stub's length when turned ON shifting the PA between 28 and 60 GHz modes. The switch has 0.7 dB ON- and 0.3 dB OFF-state loss. The measured results exhibit 16.2/11.8 dB small signal gain, 18.4/17.2 dBm saturated output power and 33/21 % peak PAE at 28/60 GHz respectively. The dual-band compact PA has a chip size of 0.55 × 0.52 mm² and consumes a DC current of 11 mA at 3.5 V supply voltage. Within the literature, this is the first demonstration of a 28/60 GHz dual-band PA with performance comparable to dedicated PAs in each band.**

***Keywords*—power amplifier, dual-band, SiGe, 5G, 28 GHz, 60 GHz, switch, Ka band, V band.**

I. Introduction

This paper deals with the design of a Ka/V dual-band power amplifier, which is proposed as one of the sub-blocks in a dual-band transceiver architecture. A dual-band transceiver operating at Ka/V band is of special interest for both radar and wireless communication purposes. The vast unlicensed bandwidth (7 GHz) at V-band can provide multi-Gbps data rate for communications or very high resolution for radar at V-band, whereas the low atmospheric and free-space propagation loss at Ka-band can provide long distance communication or higher range for radar. Furthermore, due to the varying propagation characteristics and capacities among different potential 5G bands, a reconfigurable or multi-band RF transceiver unit is proposed, which can use appropriate frequency band as required by the environment, country or application.

Multi-band frontend electronics has been a topic of interest towards single-chip integration in order to decrease the power consumption and IC area. For example, [1] uses variable inductors or varactors to adjust operational frequency, [2] uses LC tanks in matching network for dual-band operation, [3] uses MEMS switches to change matching network configuration, and [4] uses CMOS switches at both input and output matching networks to shift between frequencies. However, tunable inductors or capacitors give narrow tuning range and MEMS switches add cost and complexity to the fabrication process, while [4] operates at less than 10 GHz.

This paper presents, for the first time, the design of a 28/60 GHz band-switchable power amplifier in 0.13um BiCMOS process. The PA uses cascode as the core amplifier biased in class AB mode. Dual-band operation has been achieved by employing an LC tank in the input matching network and a switchable output matching network. The PA achieve 18.4/17.2 dBm output power and 33/21 % PAE, which is comparable to the state-of-art single-band 28 or 60 GHz PAs, as listed in Table 1. To the authors' knowledge, this PA is the first demonstration of dual-band operation at Ka- and V-band with comparable or better performance to dedicated PAs in each frequency band.

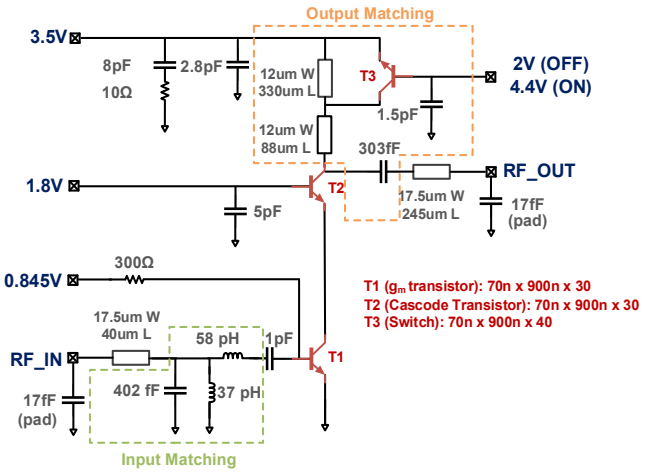

Fig. 1. Schematic of the designed 28/60 GHz PA

II. Circuit Design

The PA is designed in IHP SG13G2 BiCMOS process. The technology features high performance 130 nm HBTs with a specified f_T/f_{max} of 300/450 GHz. The collector-emitter breakdown voltage, BV_{CEO}, equals 1.7 V and collector-base breakdown voltage, BV_{CBO}, equals 4.8 V.

A. Amplifier Design

Fig. 1 shows the circuit diagram of the designed PA. T_1 (g_m transistor) and T_2 (cascode transistor) have been biased in class AB mode. T_2 operates in weak avalanche region with its base terminated with a very low impedance (AC ground). SiGe HBT cascode PAs designed in this fashion with low upper base resistance allow large-signal collector voltage excursions beyond BV_{CEO} without occurrence of catastrophic damage and without impact to long-term hot-carrier reliability [5]. Device sizes and bias current are optimized through load pull simulations to achieve output power around 17 to 18 dBm. The base node of cascode transistor (T_2), which is AC grounded, is very prone to oscillation at mm-wave frequencies. Therefore, large AC ground capacitors have been laid out as close to the base as possible, and EM simulations have been performed to ensure stability. Also, the low-frequency oscillations arising due to RF chokes in the bias paths have been suppressed by shunting the bias paths with proper low-Q capacitors. Fig. 2 shows chip photo and EM simulation model.

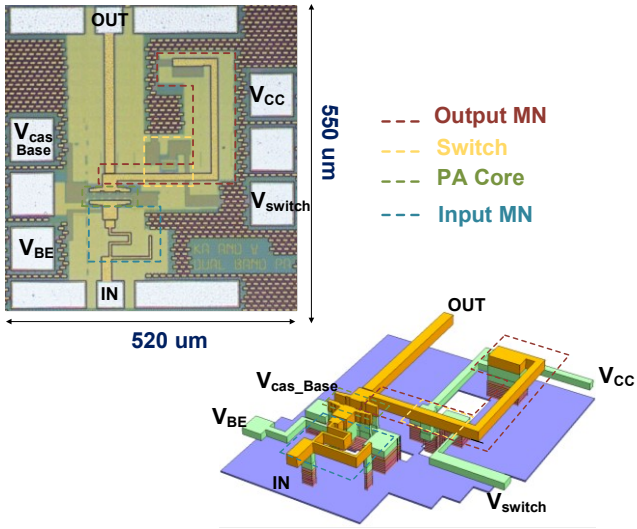

Fig.2. Chip photo and EM model in Sonnet software

B. Matching Network Design

The input of the PA has been dual-band matched at 28/60 GHz by employing a parallel LC tank and a series inductor. This tank resonates around 36 GHz, thereby providing positive reactance below 36 GHz and a negative reactance above 36 GHz. Therefore, the LC tank behaves as an inductor at 28 GHz and as a capacitor at 60 GHz. In essence, it's an L-type matching network with a L_{shunt}-L_{series} topology at 28 GHz and a C_{shunt}-L_{series} topology at 60 GHz, as shown in Fig. 3 (a).

The output of the PA has been dual-band matched at 28/60 GHz by using a shunt stub and series capacitor. The shunt stub is a thin film microstrip line (TFML) with an HBT switch used to tune its length. When the switch is turned OFF, the RF signal sees a longer stub length and PA switches to the 28 GHz mode. When the switch is turned ON, it shorts a part of the stub to the ground, effectively reducing the length of the TFML, as shown in Fig.3 (b). Therefore, RF signal sees a shorter stub length and the PA switches to the 60 GHz mode.

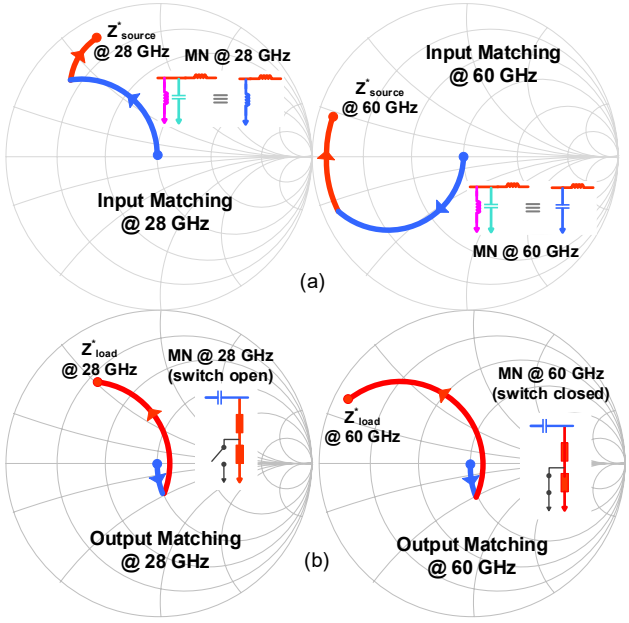

Fig. 3. Dual-band matching networks (MNs). (a) Input matching network with parallel LC resonator for 28/60 GHz match, (b) Output matching network with tunable shunt stub using switch.

C. Switch Design

The loss incurred by the switch in the TFML can be minimized by reducing the product I^2R_{sw}, where I is the current through the shunt stub and R_{sw} is the switch ON resistance. The current, I, depends upon multiple factors including electrical length of the stub, characteristic impedance of the stub and the location of the stub. In general, if a stub is connected to a high impedance node in the matching network, the loss would go down with a higher electrical length and higher characteristic impedance. Since the length and the placement of the stub are dictated by the matching network, they cannot be controlled.

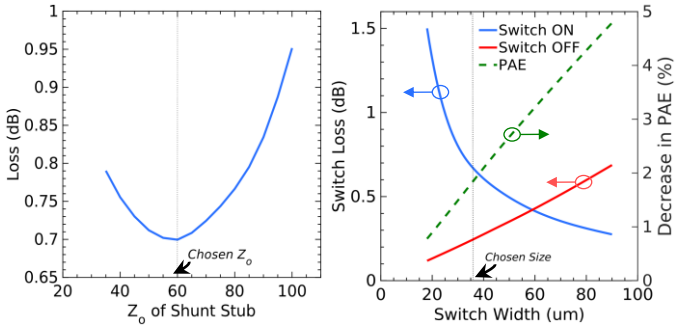

Fig. 4. Tradeoffs between switch loss, switch width and characteristic impedance of the stub. (a) Dependence of loss on characteristic impedance of the stub, (b) 36um wide transistor switch achieves as low as 0.7dB ON loss, 0.3dB OFF loss and 2% additional decrease in PAE due to switch bias current

However, the characteristic impedance of the stub can be optimized. Fig. 4 (b) shows dependence of the switch loss on the characteristic impedance of the stub. As we move to low characteristic impedances, input impedance of the shunt stub decreases, which increases the switch loss; whereas for high characteristic impedances metallic loss through conductor dominates (as physical width of the conductor decreases). Therefore, there exists an optimum where the loss is minimum. Fig. 4 (b) shows this is Z_0=60 Ω in our case. Therefore, while designing the shunt stub a 60 Ω characteristic impedance is chosen, and the length is then determined according to the matching network requirement.

As for the switch ON resistance, R_{sw}, it can be minimized by increasing the switch size. However, there is a trade-off between the ON resistance, OFF resistance and OFF capacitance. Since the transmission line itself is a distributed element, the capacitance of the switch in the OFF state can be absorbed into the transmission line, allowing for much larger transistors to be used with lower ON resistance. After a certain size, the reduction in insertion loss in ON state (due to decrease in ON resistance) becomes insignificant whereas the increase in insertion loss in OFF state (due to proportional decrease in OFF resistance) becomes significant. Also, at large switch size, there is additional drop to PAE due to the switch bias current. Fig. 4 (a) captures these tradeoffs. Based on these tradeoffs,

switch size of 0.09 x 36 mm^2 is chosen which results in 0.7dB loss in ON state, 0.3dB loss in OFF state and 2% additional decrease in PAE due to switch bias current.

An additional concern is the linearity of the switch. This is critical in the OFF state, as the AC voltage present at the TFML (the collector of T_3 in Fig. 1), leaks to the base of the switch and develops a base-emitter differential, which may self-actuate the switch. This can be alleviated by applying a reverse bias on the switch. Fig. 5 plots 1-dB compression point of the switch against reverse bias applied to it. The reverse emitter-base breakdown limit for HBT in this process is -1.6V, therefore we use a V_{BE} of -1.5V, which gives 23 dBm compression point which is far higher than the PA 1dB output compression point of 15.5 dBm. Therefore, the linearity of the PA is not affected, and switch is not operated beyond its breakdown limit. It should be noted that a negative bias of -1.5 V is achieved by applying an OFF-state voltage of 2 V, because the emitter is connected to a supply of 3.5 V, therefore no actual negative potential is required.

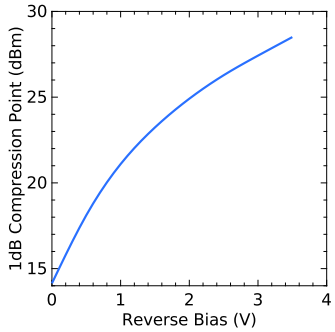

Fig. 5. 1-dB compression point of switch against reverse bias applied to the switch during OFF state

III. Measurement

Small signal measurements have been performed using Keysight N5227A PNA network analyzer which is calibrated using SOLT standards from 0.1MHz to 67 GHz range. Fig. 6 (a) and (b) shows measured and simulated s-parameters at 28 GHz and 60 GHz respectively. Measured gain at 28/60 GHz is 16.2/11.8 dB and measured input return loss is -8/-19 dB. To measure the output power, input of the PA is excited using a Keysight E8257D analog signal generator and the output is measured using Keysight N9010B EXA signal analyzer. Fig. 6 (c) shows measured and simulated PAE at 28/60 GHz and Fig. 6 (d) shows measured and simulated output power at 28/60 GHz. Due to the measurement setup, there is measurement uncertainty of ± 0.2 dB in the output power which also adds uncertainty of ± 1.5 % to the peak PAE. The PA shows simulated P_{sat} of 18/16.5 dBm and simulated peak PAE of 32/22 % at 28/60 GHz whereas the measured Psat is 18.4/17.2 dBm and measured peak PAE is 33/21 % at 28/60 GHz.

Table 1 compares this PA with the most recent single-band and wideband PAs around 28/60 GHz frequencies. The designed PA shows state of the art performance in terms of PAE and output power. The very promising dual-band performance is achieved by minimizing switch loss, while maintaining high linearity as described in this paper. To the authors' knowledge, this is the first demonstration of dual-band PA at 28 GHz and 60 GHz.

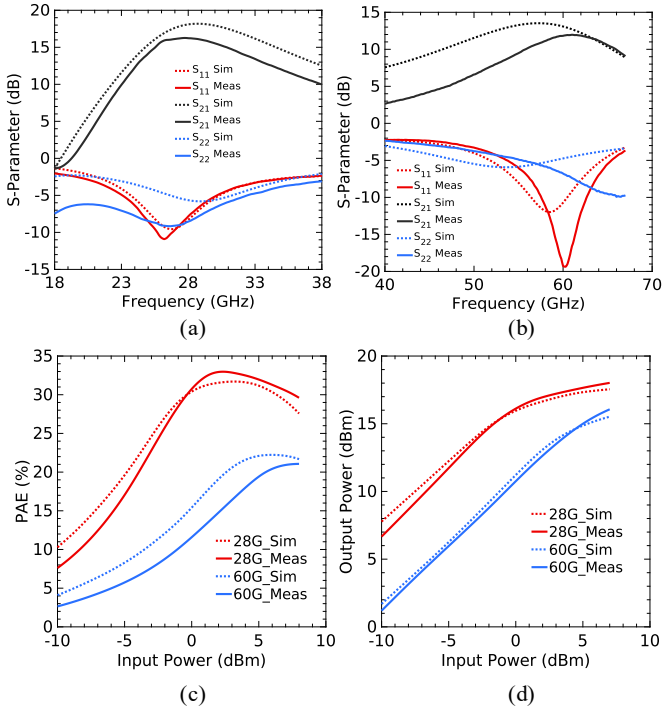

Fig. 6. Simulated and measured results. (a) 16 dB gain and -8dB input return loss at 28 GHz, (b) 11.8 dB gain and -19 dB input return loss at 60 GHz, (c) 33/21 % peak PAE at 28/60 GHz, (d) 18.4/17.2 dBm saturated output power (extrapolated from plots) at 28/60 GHz

IV. Conclusion

A dual-band PA operating in 28 GHz and 60 GHz mode is presented. The PA employs cascode topology, LC tank at input matching network and tunable stub at the output matching network to shift the frequency of operation between 28 GHz and 60 GHz. Performances in each band are comparable to single band state of the art PAs. The designed PA is suitable for 5G transceivers or dual-band phased array radars.

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Table 1. Comparison with Recent 28GHz and 60GHz PAs

Reference		Technology	Topology	Frequency (GHz)	P_{sat} (dBm)	Peak PAE (%)	Gain (dB)	Core Area (mm^2)
Dual-band PA	This Work	130 nm SiGe	Class AB Cascode	28	18.4	33	16.2	0.1
				60	17.2	21	11.8	
Dedicated Single Band PAs	2017 ISSCC [6]	45 nm SOI	Cascode w/ Output Combiner	60	16.7	28.3	24	0.067
	2018 MWCL [7]	45 nm SOI	Cascode w/ Output Combiner	60	18.5	25.5	15	0.12
	2016 ISSCC [8]	130 nm SiGe	Cascode w/ Output Combiner	60	23.6	27.7	24	0.55*
	2015 ISSCC [9]	28 nm CMOS	Doherty	60	18.2	21	15.2	0.16
	2017 TMTT [10]	130 nm SiGe	Class AB Harmonically Tuned	28	18.8	35.3	15.5	0.27
	2018 MWCL [11]	45 nm SOI	Doherty	28	22.4	40	10	0.25*
	2018 RFIC [12]	45 nm SOI	Hybrid Class F/F^{-1}	28	18.6	45.7	11.4	0.14
	2018 RFIC [13]	90 nm CMOS	Cascode w/ Output Combiner	28	26	34	16.3	0.4
	2016 JSSCC [14]	28 nm CMOS	CS w/ Source Degen.	28	14	35.5	15.7	0.155
Wideband PAs	2011 TMTT [15]	130 nm SiGe	Distributed	DC-77	17.5	13	10	2.2#
	2018 PAWR [16]	130 nm SiGe	Distributed	12-40	21.5	20.1	14	1.2#
	2016 JSSC [17]	90 nm SiGe	Distributed	14-105	15&	9.7	12	1.51#
	2017 MWCL [18]	180 nm CMOS	Distributed	2-22	14.5&	10	11.9	1.7#

*estimated from figures in paper &OP1 dB #total chip area

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