24.1 A 24-to-30GHz Watt-Level Broadband Linear Doherty Power Amplifier with Multi-Primary Distributed-Active-Transformer Power-Combining Supporting 5G NR FR2 64-QAM with >19dBm Average P_{out} and >19% Average PAE

Fei Wang, Hua Wang

Georgia Institute of Technology, Atlanta, GA

The continuous worldwide demand for multi-Gb/s data-rate has driven the rapid development and standardization of 5G New Radio (NR) specifications in the mmwave bands [1-3]. As a result, there is a surge of interest in high-performance yet compact mm-wave 5G front-end chipsets to enable large-aperture phased arrays. In User Equipment (UE) devices, the limited form factor restricts the number of antenna array elements, e.g., 2×2, which dramatically increases the output power (P_{out}) requirement per element [1,4]. For base stations, although some applications require only moderate element P_{out} and high antenna gain, high P_{out} capabilities allow array-divisions/sub-arrays for concurrent multi-stream mm-wave links.

However, generating high Pout at mm-wave necessitates high-efficiency power amplifiers (PAs) and judicious power combining in low-breakdown silicon processes. A few silicon high-power (>26dBm P_{out}) mm-wave PAs have been reported but with limited linearity and average efficiency (PAE_{avo}) due to the unbalanced impedance across ports and/or limited passive efficiency [4-8]. In parallel, high-speed spectrally efficient modulation schemes, e.g., high-order QAM, OFDM, and carrier-aggregation (CA), will be widely used in 5G, leading to high peak-to-average power ratio (PAPR) waveforms [1-4,9-11]. This makes both PA peak and back-off efficiency values highly critical. To support 5G multi-Gb/s high-PAPR signals, outphasing PAs require substantial baseband computation and DPD overhead [9]. Although Doherty PAs potentially support large modulation bandwidths with low baseband overhead, existing mm-wave Doherty PAs in silicon exhibit limited efficiency and Pout mainly due to lossy and complex on-chip Doherty output networks [2,3]. Hence, mm-wave silicon PA solutions with high power, high linearity, and high peak/back-off efficiency still remain elusive. To address these challenges, we introduce a fully integrated watt-level broadband linear Doherty PA with multi-primary distributed-active-transformer (DAT) powercombining to efficiently support multi-Gb/s 5G NR signals.

Figure 24.1.1 shows the design of the proposed broadband power-combined multi-primary DAT Doherty output network. The equivalent network and the transmission matrix show that a transformer can be designed as an inductive impedance inverter after the capacitive loadings resonate out the remaining inductances ($L_{12}M/L_s$ and $L_{12}M/L_p$), resulting in an impedance inverter with the characteristic impedance of $Z_0=1/Y_0=\omega L_{12}$. Schematic simulations verify that this one-transformer network indeed achieves ideal Doherty active load modulation. We propose a multi-primary distributed active transformer to achieve simultaneous series/parallel multi-way power combining. It achieves series power combining between Primary #1 and #2 as well as between Primary #3 and #4; meanwhile, it achieves parallel power combining between Primary #1 and #3 as well as between Primary #2 and #4. Furthermore, to enable multi-primary DAT power combining in both main/auxiliary paths and broaden the carrier bandwidth, an impedance scaling network, composed of two impedance inverters, i.e., one transformer-based and one capacitor-based, is inserted in the auxiliary (Aux) path. In practice, the two negative capacitors (-C₁) are absorbed in the two shunt physical capacitors (C_{S1} and C_{S2}). Finally, the one-transformer Doherty output network is extended to the proposed multi-primary DAT configuration at both main/auxiliary paths, achieving high-efficiency power combining and desired Doherty active load modulation simultaneously. Four differential main PAs (Main 1 to 4) and four differential auxiliary PAs (Aux 1 to 4) are respectively combined in a DAT fashion with series/parallel power combining. The layout of a multiprimary transformer is shown in Fig. 24.1.1, where the multi-primary coils are implemented using two top metals and the secondary coil uses the second top metal. It also simplifies DC supply feeding and layout integration with PA cells.

Figure 24.1.2 shows 3D EM simulation results of the proposed broadband power-combining multi-primary DAT Doherty output network including custom MOM capacitors (the layout is shown in Fig. 24.1.3). Simulation results (f_c =28GHz)

verify that the proposed network achieves highly desired Doherty active load modulation, in that all the single-ended complex loads for all 8 main/auxiliary differential PAs are well balanced and symmetric across all power levels. This achieves the multi-way power combining and desired Doherty active load modulation with >81% total passive efficiency (<1dB loss) at 28GHz. Simulations also show that the proposed DAT Doherty network supports broadband symmetrical operations for all 16 main/auxiliary ports over 24 to 34GHz at both OdB (peak Pour) and 6dB back-off. More than 80% total passive efficiency (<1dB loss) is maintained at 0dB and 6dB back-off over the entire Doherty load modulation over 23.8 to 29.2GHz.

The proposed broadband power-combined multi-primary DAT Doherty PA is prototyped in a standard 0.13 μ m SiGe BiCMOS process (Fig. 24.1.3). The PA and driver stages employ common-emitter amplifiers with sizes of 2×6×8 μ m and 2×2×12 μ m, respectively. Neutralization capacitors are used at the PA (55fF) and driver (32fF) for gain and stability improvement. RC pairs at the inputs of the PA and driver further enhance stability. Figure 24.1.7 shows the die micrograph. The PA occupies 4.19mm² total chip size and the core area is only 1.35mm².

The chip is wirebonded to an Aluminum PCB and probed for measurement. Figure 24.1.4 shows the small-signal S-parameters and large signal continuous-wave (CW) measurement results. The peak S_{21} is 23.2dB at 24GHz with a 3dB bandwidth from 22.0 to 28.5GHz. The input matching is <-10dB from 23.2 to 34.0GHz. The PA CW tests demonstrate Doherty back-off efficiency enhancement over the 23 to 31GHz $P_{\rm sat}$ 1dB bandwidth. At 24GHz, the PA achieves 37.8% peak PAE (PAE_{\rm max}) with 28.2dBm $P_{\rm sat}$ and 37.8% PAE at 26.6dBm $P_{\rm 1dB}$ and 27.8% PAE at 6dB back-off from $P_{\rm sat}$. At 28GHz, the PA achieves 30.4% PAE_{\rm max} with 28.3dBm $P_{\rm sat}$ and 30.2% PAE at 26.8dBm $P_{\rm 1dB}$ and 21.2% PAE at 6dB back-off from $P_{\rm sat}$.

Figure 24.1.5 shows modulation tests using single-carrier 64-QAM signals and FR2 5G NR signals. For 200MSym/s (1.2Gb/s) single-carrier 64-QAM signal, the PA achieves 21.3/20.9dBm average P_{out} (P_{avg}) and 24.6/18.4% average PAE (PAE_avg) with -25.4/-25.0dB rms EVM at 24/28GHz. For 200MHz 1-CC FR2 5G NR 64-QAM signal (9.64B PAPR), the PA achieves 19.1/18.1dBm P_{avg} and 19.0/13.8% PAE_avg with -25.2/-25.1dB rms EVM at 24/28GHz. For 200MHz 2-CC FR2 5G NR 64-QAM signal (11.84dB PAPR), the PA achieves 17.9/17.5dBm P_{avg} and 16.2/12.9% PAE_avg with -25.6/-25.5dB rms EVM at 24/28GHz. Moreover, for 800MHz 2-CC FR2 5G NR 16-QAM signal (11.78dB PAPR), the PA achieves 18.2/18.7dBm P_{avg} and 17.4/16.6% PAE_avg with -19.3/-19.4dB rms EVM at 24/28GHz.

In summary, the proposed watt-level broadband linear Doherty power amplifier with multi-primary DAT power-combining achieves high P_{out} and high peak/back-off efficiency simultaneously. The prototype PA demonstrates the highest P_{out} among reported 28GHz Doherty/outphasing silicon PAs in [12] and the highest PAE at peak/back-off among mm-wave high-power silicon PAs in both CW and modulation operations in [12].

Acknowledgement:

This work was in part supported by Qorvo. The authors would like to thank K. Kobayashi, B. Nelson, Dr. M. O'Neal, B. Peterson and Dr. G. Burra from Qorvo for technical discussions. They also thank GLOBALFOUNDRIES for chip fabrication and Keysight for measurement equipment support.

References:

[1] "3GPP 5G-NR specifications"

Accessed in Sept., 2019, http://www.3gpp.org/DynaReport/38-series.htm. [2] F. Wang et al., "A Highly Linear Super-Resolution Mixed-Signal Doherty Power Amplifier for High-Efficiency mm-Wave 5G Multi-Gb/s Communications," *ISSCC*, pp. 88-90, Feb. 2019.

[3] S. Hu et al., "A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications," *ISSCC*, pp. 32-33, Feb. 2017.
[4] K. Dasgupta et al., "A 26 dBm 39 GHz Power Amplifier with 26.6% PAE for 5G Applications in 28nm bulk CMOS," *IEEE RFIC*, pp. 235-238, June 2019.

[5] H. Nguyen et al., "A 60GHz CMOS Power Amplifier with Cascaded Asymmetric Distributed-Active-Transformer Achieving Watt-Level Peak Output Power with 20.8% PAE and Supporting 2Gsym/s 64-QAM Modulation," *ISSCC*, pp. 90-92, Feb. 2019.

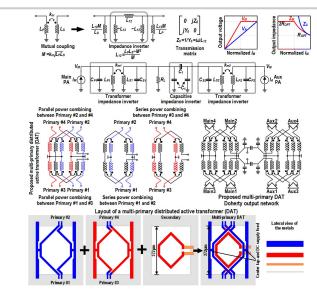


Figure 24.1.1: Design of the multi-primary DAT Doherty output network.

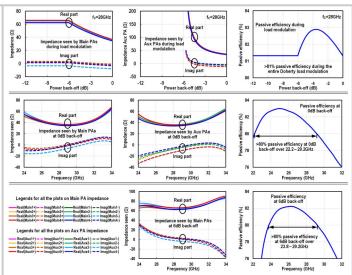


Figure 24.1.2: 3D EM simulation results of the multi-primary DAT Doherty output network.

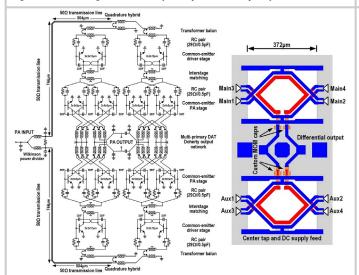


Figure 24.1.3: Top schematic of the prototype PA and layout of the multiprimary DAT Doherty output network.

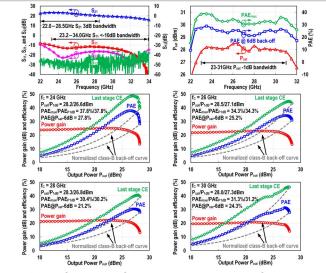


Figure 24.1.4: Small-signal S-parameters and large-signal CW measurement results. Comparison with recently reported mm-Wave PAs in silicon

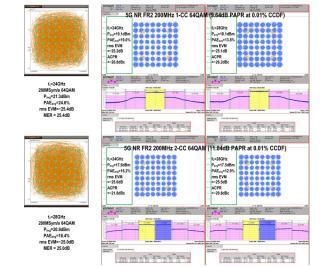


Figure 24.1.5: Modulation measurement results with single-carrier 64-QAM and FR2 5G NR signals.

	This work		mm-Wave High Power PAs				mm-Wave Doherty/Outphasing PAs			5G PAs	
			[4] Dasgupta, RFIC '19	[5] Nguyen, ISSCC '19	[7] Bhat, TMTT '15	[8] Datta, ISSCC '15	[2] Wang, ISSCC '19	[3] Hu, ISSCC '17	[9] Rabet, ISSCC 18	[11] Li, ISSCC '18	[10] Shakib, ISSCC '17
Technology	0.13μm SiGe		28nm CMOS	45nm SOI CMOS	45nm SOI CMOS	0.13µm SiGe	45nm SOI CMOS	0.13µm SiGe	0.13µm SiGe	0.13µm SiGe	40nm CMO
Architecture	Multi-Primary DAT Doherty		DAT	Cascaded Asymmetric DAT	4-stacked 8-way Combined	Digital 8-way Dynamic Load Modulated	Mixed- Signal Doherty	Multiband Analog Doherty	Triaxial Balun Outphasing	Continuous Class F-1	Dual- Resonano Transforme
Supply (V)	2.0		2.2	2.0	4.8	5	2.0	1.5	4	1.9	1.1
Freq. (GHz)	24	28	39	60	42.5	46	27	28	28	28.5	27
Gain (dB)	23.6	20.5	38.0	24.7	19.4	13	19.1	18.2	14.0	20	22.4
P _{sat} (dBm)	28.2	28.3	26	30.1	27.2	28.9	23.3	16.8	23	17	15.1
P _{1dB} (dBm)	26.6	26.8	21.5	26.5	24.0*	N.A.	22.4	15.2	N.A.	15.2	13.7
PAEmex	37.8%	30.4%	26.6%	20.8%	10.7%	18.4%	40.1%	20.3%	41.4%†	43.5%	33.7%*
PAE _{P1dB}	37.8%	30.2%	13.6%	15.4%	7.5%	N.A.	39.4%	19.5%	N.A.	39.2%	31.1%*
PAE@ 6dB back-off	27.8%	21.2%	10%	7.0%*	4.5%	11%	33.1%	13.9%	34.7% [†]	22%*	15.1%
Modulation scheme	64-QAM		64-QAM	64-QAM	N.A.	ASK	64-QAM	64-QAM	64-QAM OFDM	64-QAM	64-QAN OFDM
Data rate (Gb/s)	1.2	1.2	0.6	6.0	N.A.	N.A.	6	6	0.48	9	4.8
EVM(dB)	-25.4	-25.0	-28.5*	23.4	N.A.	N.A.	-25.3	-26.6	-30.5	-26.8	-25
DPD	NO	NO	Yes	NO	N.A.	N.A.	NO	NO	Yes	NO	NO
P _{avg} (dBm)	21.3	20.9	19.0	23.0	N.A.	N.A.	15.9	7.2	14.3	10.7	6.7
PAE _{avg} (%)	24.6%	18.4%	8.3%*	5.2% PAE	N.A.	N.A.	29.1% PAE	14.4% CE**	25.3% PAE†	21.4%	11%
Area (mm²)	4.19 (1.35‡)		2.96 (0.945‡)	6.6#	4.16	13.7	2.87 (0.52‡)	1.76	0.56	0.29‡	0.23#

*graphically estimated **last stage CE †1-stage PA ‡core area

Figure 24.1.6: Comparison table with recently reported mm-wave PAs in silicon.

ISSCC 2020 PAPER CONTINUATIONS

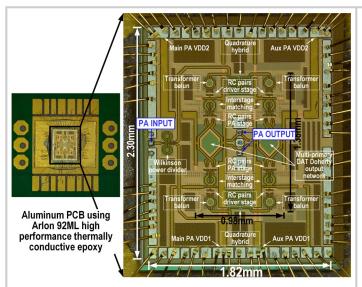


Figure 24.1.7: Die micrograph.

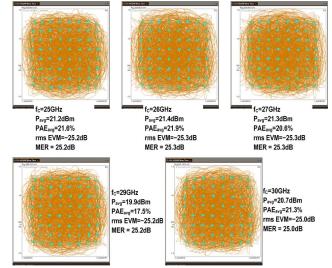


Figure 24.1.S2: Modulation measurement results with 200MSym/s singlecarrier 64-QAM signals.

Additional References:

[6] T. Chi et al., "A 60GHz On-Chip Linear Radiator with Single-Element 27.9dBm P_{sat} and 33.1dBm Peak EIRP Using Multifeed Antenna for Direct On-Antenna Power Combining," *ISSCC*, pp. 296-297, Feb. 2019.

[7] R. Bhat et al., "Large-Scale Power Combining and Mixed-Signal Linearizing Architectures for Watt-Class mmWave CMOS Power Amplifiers," *IEEE TMTT*, vol. 63, no. 2, pp. 703-718, Feb. 2015.

[8] K. Datta and H. Hashemi, "A 29dBm 18.5% Peak PAE mm-Wave Digital Power Amplifier with Dynamic Load Modulation," *ISSCC*, pp. 46-47, Feb. 2015.

[9] B. Rabet and J. Buckwalter, "A High-Efficiency 28GHz Outphasing PA with 23dBm Output Power Using a Triaxial Balun Combiner," *ISSCC*, pp. 174-176, Feb. 2017

[10] S. Shakib et al., "A Wideband 28GHz Power Amplifier Supporting 8×100MHz Carrier Aggregation for 5G in 40nm CMOS," ISSCC, pp. 44-45, Feb. 2017.

[11] T. Li et al., "A Continuous-Mode Harmonically Tuned 19-to-29.5GHz Ultra-Linear PA Supporting 18Gb/s at 18.4% Modulation PAE and 43.5% Peak PAE," ISSCC, pp.410-412, Feb. 2017.

[12] H. Wang et al., Power Amplifiers Performance Survey 2000-Present. Accessed in Sept. 2019, http://gems.ece.gatech.edu/PA_survey.html.

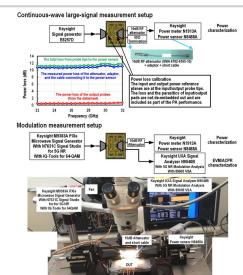


Figure 24.1.S1: Large-signal CW measurement and modulation measurement setups.

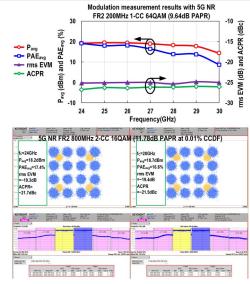


Figure 24.1.S3: Modulation measurement results with 5G NR FR2 signals.