2.5 A High-Efficiency Multiband Class-F Power Amplifier in 0.153µm Bulk CMOS for WCDMA/LTE Applications

Jenwei Ko, Xiaochuan Guo, Changhua Cao, Saravanan Rajapandian, Solti Peng, Jing Li, Wenchang Lee, Narayanan Baskaran, Caiyi Wang

MediaTek, Austin, TX

Rapid growth in LTE smart phones has increased the demand for multiband power amplifiers (PAs) that have low cost and high efficiency. This paper describes a multiband WCDMA/LTE PA fabricated in a low-cost 0.153µm (85% shrink of 0.18µm) bulk CMOS process that has the highest PAE among published CMOS WCDMA/LTE PAs in [1-6]. Notably, the PA implemented a Class-F output matching network (MN) that maximizes P_{sat} and PAE at P_{sat} and improves linearity.

Figure 2.5.1 shows the block diagram of the multiband CMOS PA for 824 to 849MHz (B5), 880 to 915MHz (B8), 1850 to 1910MHz (B2), and 1920 to 1980MHz (B1). B5 and B8 share a low-band (LB) path, while B1 and B2 share a high-band (HB) path. Each path consists of a single-ended-to-differential input MN, a driver-stage amplifier, an inter-stage MN, an output-stage amplifier, and a differential-to-single-ended output MN. Directional couplers at the output of LB and HB paths are daisy-chained for power detection. All circuit blocks are controlled through a MIPI interface.

The output-stage amplifier uses a cascode structure with a high-voltage MOS transistor (M_2) to improve the drain breakdown voltage and to reduce the voltage swing at the drain of the NMOS transistor (M_1). This decreases the Miller effect on gate-to-drain capacitance (C_{gd}). In addition, a cross-coupled capacitor C_1 neutralizes the C_{gd}. Non-linearity from gate-to-source capacitance (C_{gs}) and any un-neutralized C_{gd} of M_1 is linearized by a PMOS varactor (M_3) biased in the moderate-inversion region [1]. The overall amplifier size, gate bias voltages, and load impedance are optimized for maximum efficiency at 28dBm output power.

The PA implements a Class-F output MN that not only limits the maximum drain voltage swing but also improves the drain efficiency, P_{sat}, and output-stage linearity. The MN terminates the fundamental and the 3rd-harmonic impedances at the drain to values determined from a load-pull analysis. It is easier to realize specific impedance at the 3rd harmonic at LB compared to HB due to the significant non-linear drain capacitance (C_{dd}) observed in the CMOS process. The MN realizes a short for the 2nd harmonic. This limits the drain voltage swing to 2×VDD at the matched condition and also reduces the device breakdown-voltage requirement under VSWR conditions. Realizing specific impedances at harmonics higher than the 3rd gives marginal improvement in efficiency at the expense of area and complexity.

In Fig. 2.5.2, C_{2H}(C_{2L}), L_{2H}(L_{2L}), and L_{2CM} are used to realize the 2nd-harmonic trap. Optimal values for C_{1H}(C_{1L}), C_{3H}(C_{3L}) and the transformer inductance in conjunction with the 2nd-harmonic trap help realize specific impedances at the fundamental and 3rd harmonic with minimal loss. Large frequency difference between HB and LB leads to different MN implementations.

The driver-stage-amplifier (driver) design along with inter-stage matching network is critical for overall PA linearity and to drive the output-stage amplifier to its fullest. Increasing the ratio (n) of the step-down inter-stage transformer in Fig. 2.5.3 improves the driver efficiency at the expense of driver linearity. This PA implements a 3:1 inter-stage transformer to optimize the efficiency-and-linearity trade-off. As a result, the driver is very efficient and consumes only 3% of the output-stage quiescent current. The driver uses a cascode structure for good linearity and isolation with the input. Furthermore, a 2nd-harmonic short is implemented at the driver output to improve its linearity.

The input matching network matches the PA to 50Ω using a 1:3 transformer, which provides an additional 9.5dB voltage gain. A tuning capacitor at the primary is used to keep S_{11} < -10 dB across the various frequency bands.

Although the Class-F operation and the HVMOS improve reliability significantly, real-time voltage-stress monitoring (VSM) is implemented on each of the output-stage amplifier drains to indicate the voltage stress and to protect the PA under severe conditions. The VSM circuit in Fig. 2.5.3 comprises of series diodes, a capacitor, and a resistor divider. The diodes and the capacitor track the peak drain voltage. The divided voltage is compared with the reference voltage (V_{ref}) to signal the stress on the device.

Figure 2.5.7 shows the micrograph of the 0.153µm CMOS die and the 0.18µm IPD die in a 3.0×4.2×0.6mm³ LGA package. The performance of the packaged PA is measured on an evaluation board. Figure 2.5.4 shows linearity, PAE, and gain versus output power for an LTE 20MHz 100RB 16-QAM signal with *V*DD=3.4V. Measured LB (HB) PAE are 37.3% (34.7%) at 27.5dBm (28.1dBm) linear output power (P_{max}) while meeting the 3GPP specification with a 2dB margin. Lowering VDD and the bias voltage enhances PAE at the mid- and low-power outputs (Fig. 2.5.5). At 19dBm and 9dBm output power, HB PAEs are 21% and 8%, which are higher than the Doherty PA in [6]. The high temperature operation life (HTOL) test is performed with 16 samples in each band at 85°C and 28dBm modulated signal for 520 hours. The ruggedness test is carried out under a VSWR of 10:1 for various phases. No performance degradation is observed after the HTOL and the ruggedness tests. The PA passes both HBM 2kV and machine-model (MM) 300V ESD tests.

Figure 2.5.6 shows a summary of the performance comparison of this PA with the state-of-the-art CMOS PAs for the WCDMA and LTE 20MHz 16-QAM signals. This Class-F linear PA has the best efficiency and the least power back-off (P_{sat}-P_{max}), compared to other PA architectures in [2-6]. The lower power back-off demonstrates the high linearity of this PA.

In conclusion, this Class-F PA achieves the highest efficiency among the published CMOS PAs in Fig. 2.5.6 and closes the performance gap between CMOS and GaAs PAs, especially, at LB frequencies.

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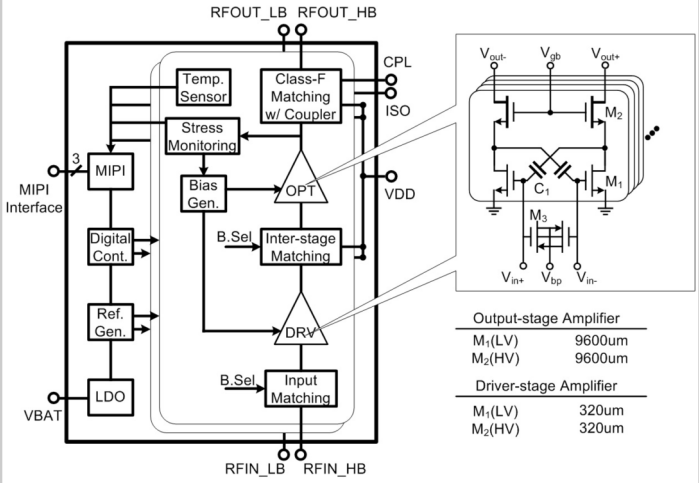

Figure 2.5.1: Top block diagram and unit PA schematic.

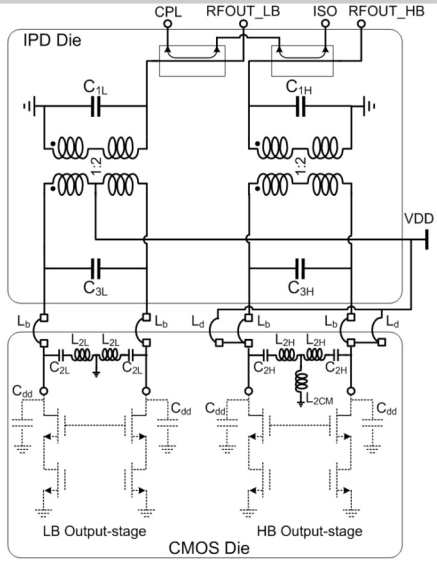

Figure 2.5.2: LB and HB Class-F output matching networks.

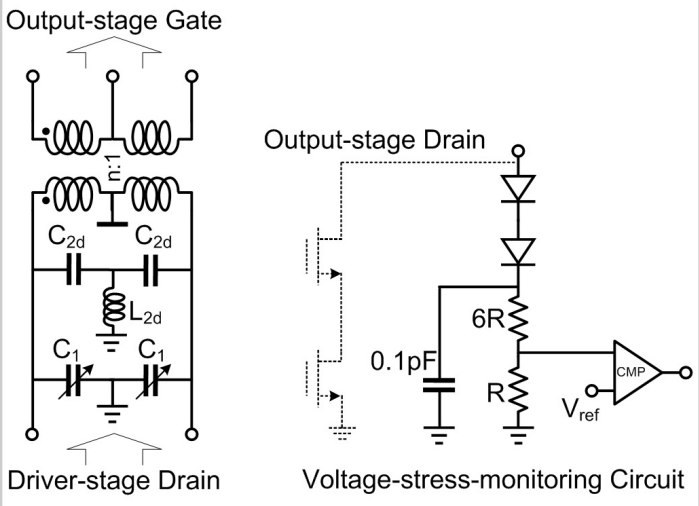

Figure 2.5.3: Inter-stage matching network and voltage-stress-monitoring circuit.

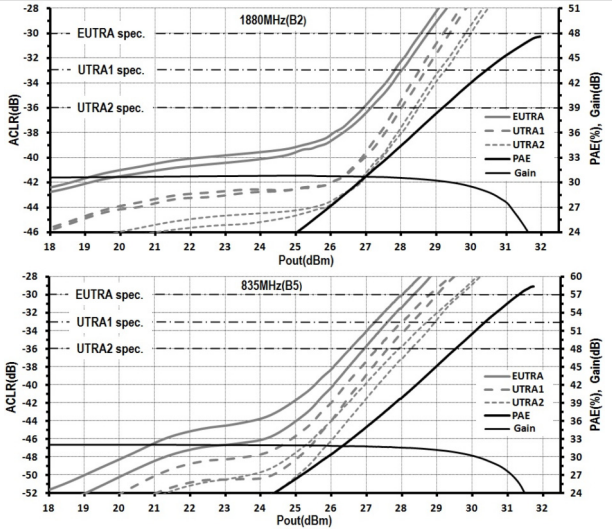

Figure 2.5.4: LTE 20MHz, 100RB, 16-QAM measurement results with V_{DD}=3.4V.

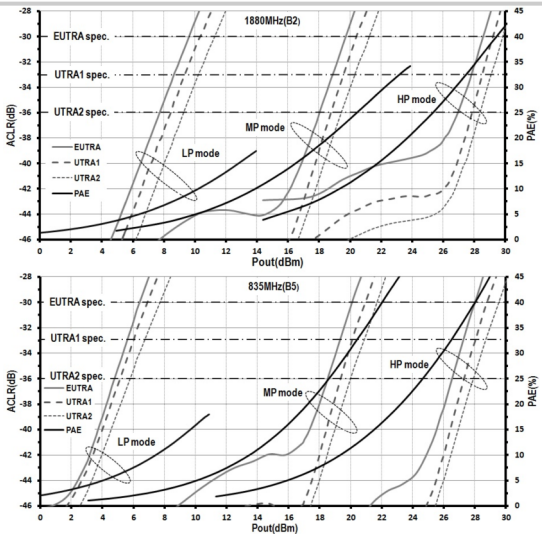

Figure 2.5.5: LTE 20MHz, 100RB, 16-QAM measurement results at power modes.

3G WCDMA PA	ISSCC'12[2]	ISSCC'12[3]		This work			
CMOS Technology	0.18 µm	90 nm		0.153 µm			
Package	no	LGA 3.5 x 4 x 0.7 mm³		LGA 3.0 x 4.2 x 0.6 mm³			
VDD (V)	3.4	3.5		3.4			
Frequency (GHz)	1.95	0.837	1.95	0.835 (B5)	0.898 (B8)	1.88 (B2)	1.95 (B1)
Psat (dBm)	30.5	-	-	31.7	31.9	32	31.9
PAEpeak (%)	42.1	-	-	58.9	55.6	47.6	46.5
Pmax (dBm)	28	28.2	27.4	29.4	29.4	29.8	29.5
PAE (%) @Pmax	36.4	31.2	28.5	47	44.4	40.8	39.6
ACLR1 (dB) @Pmax *	-35	-34	-34	-36	-36	-36	-36
ACLR2 (dB) @Pmax *	-	-	-	-50.5	-52	-50	-49.8
Gain (dB) @Pmax	23.7	28.5	28.5	30.4	31.7	30.5	31.1
EVMrms (%) @Pmax *	-	-	-	4	4.1	3.5	4.2
Power back-off (dB)	2.5	-	-	2.3	2.5	2.2	2.4

* 3GPP spec. ACLR1 < -33 dB, ACLR2 < -43 dB, EVMrms < 17.5%

4G LTE PA	EuMIC'12[4]	ISSCC'14[5]	ISSCC'15[6]	This work			
CMOS Technology	0.18µm	40nm	0.13µm	0.153µm			
Package	no	no	32-QFN	LGA 3.0 x 4.2 x 0.6 mm³			
Output matching	off-chip	on-chip	off-chip	on-chip (0.18µm IPD)			
VDD (V)	4.5	1.5	3.3	3.4			
Modulation	LTE 10M 16QAM	LTE 20M 16QAM	LTE20M 16QAM	LTE 20M 16QAM ***			
Frequency (GHz)	1.85	1.9	2.4	0.835 (B5)	0.898 (B8)	1.88 (B2)	1.95 (B1)
Psat (dBm)	-	28	31.6	31.7	31.9	32	31.9
PAEpeak (%)	-	34	39.6	58.5	55.6	47.6	46.3
Pmax (dBm)	26	23.4	27	27.5	27.7	28.1	27.7
PAE (%) @Pmax	31.5	23.3	22.2	37.3	36.5	34.7	33.3
EUTRA (dB) @Pmax **	-32	-30	-32.1	-32.1	-32.1	-32	-32
UTRA1 (dB) @Pmax **	-	-	-	-35.2	-35.4	-35	-35
UTRA2 (dB) @Pmax **	-	-	-	-37.8	-37.9	-37	-37.1
Gain (dB)@Pmax	11	21.3	9.6	31.7	32	30.5	31.1
EVMrms (%) @Pmax **	-	7.1	2.3	6.2	6.2	6	6
Power back-off (dB)	-	4.6	4.6	4.2	4.2	3.9	4.2

** 3GPP spec. EUTRA < -30 dB, UTRA1 < -33 dB, UTRA2 < -36 dB, EVMrms < 12.5%
*** CCDF 0.1% LTE 20M 16QAM / WCDMA = 6.4 dB/ 3 dB

Figure 2.5.6: Performance comparison with the state-of-the-art WCDMA/LTE CMOS PAs.

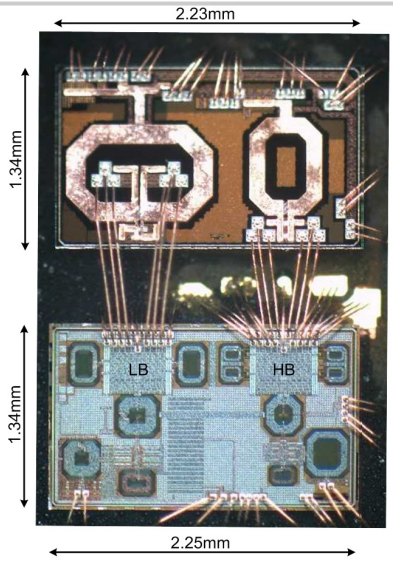

Figure 2.5.7: CMOS and IPD die micrograph.

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