A Monolithic Voltage-Boosting Parallel-Primary Transformer Structures for Fully Integrated CMOS Power Amplifier Design

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***Abstract* — In this paper, a novel monolithic voltage-boosting parallel-primary transformer is presented for the fully integrated CMOS power amplifier design. Multiple primary loops are interweaved in parallel to combine the AC currents from multiple power devices while the higher turn ratio of a secondary loop boosts AC voltages of the combined primary loops at the load of the secondary loop. The proposed interweaved structure is much more compact and separable from power devices, avoiding potential instability. To verify the feasibility of this power combining method, the fully integrated CMOS switching power amplifier was implemented in a standard 0.18-μm technology. The power amplifier successfully demonstrated a measured output power of 1.3 W and a measured power added efficiency (PAE) of 41% to a 50-Ω load with a 3.3-V power supply at 1.8 GHz operation.**

***Index Terms* — Voltage-boosting, parallel-primary, transformer, CMOS, power amplifier.**

I. Introduction

With the significant increase of the mobile phone market and the rapid advances in semiconductor technology, there is a tremendous demand for low-cost RF components for the wireless/mobile terminal. Accordingly, full integration of digital, analog, and even RF functions into the same substrate has been an inevitable task in the modern wireless communication industry. The most cost-effective solution for such an integration is possible by using a CMOS platform that is already a dominant way of implementation with baseband digital, analog, and RF transceiver circuits [1].

However, even such a promising CMOS technology has not yet been sufficiently exploited in the implementation of RF front-end blocks such as RF power amplifiers (PAs) and RF switches because standard CMOS technology has intrinsic drawbacks such as a low quality factor (Q) of passive components, lossy substrate, and low breakdown voltage. Therefore, a modular integration of a PA and an output matching structure has been preferred rather than a fully integrated PA [2]. Recently, a fully integrated output matching and combining technique has been proposed and has presented quite successful results [3]. This work, however, is based on a circular structure causing a cross-coupling between the input and output power that may result in instability of the amplifier circuit [4]. Also, a strong magnetic coupling from the power combining structure is inseparable from the power devices because of its generic circular geometry. Furthermore, the relatively bulky power combining structure compared to the active device area primarily determines the total die size, which is not desirable for an efficient cost model.

In this paper, various monolithic transformers for a CMOS PA are proposed that consist of multiple primary loops in parallel and a secondary loop with a higher turn ratio in an interweaved structure with a compact dimension. The magnetically induced currents caused by primary loops in parallel are combined in the secondary loop, while the increased turn ratio from primary loop to secondary loop boosts the AC voltage at the load. With the proposed structure, the transformer can be spatially separable from the power devices so that the input and output of the PA can be decoupled for a more stable operation. Moreover, the interweaved primary and secondary loops can make the transformer compact. For verification of the proposed transformer in the CMOS PA design, a fully integrated class-E PA was implemented in a standard 0.18-μm CMOS technology for wireless applications. The PA achieves an output power of 1.32 W (31.2 dBm) and a power-added efficiency (PAE) of 41% with a 3.3-V power supply at a 1.8 GHz range.

II. Voltage-Boosting Parallel-Primary Transformer

A. Parallel-Primary Transformer

PAs used in cellular applications usually require watt-level output power. However, it is unrealistic to achieve such a high output power from just one large-size power device in a fully integrated CMOS PA. Consequently, several power devices should be combined efficiently until a required power level is achieved.

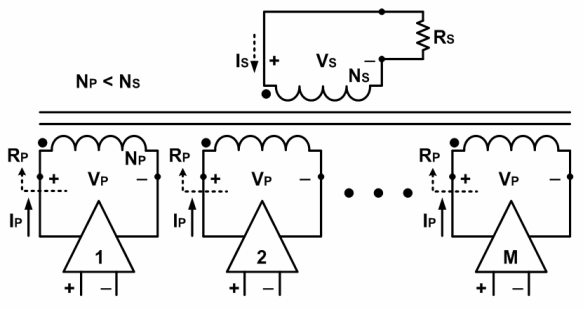

Fig. 1. Schematic diagram of the voltage-boosting parallel-primary transformer for power amplifier system.

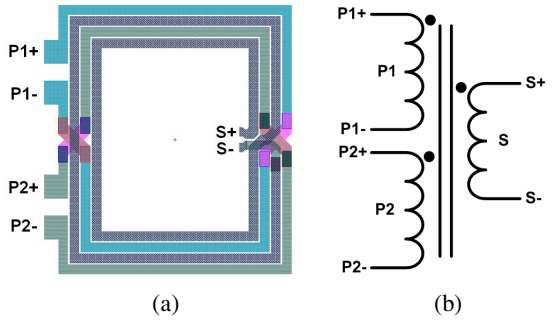

Fig. 2. 2×1:2 Transformer. (a) Physical layout. (b) Schematic diagram.

As shown in Fig. 1, the proposed voltage-boosting parallel-primary power combining structure consists of the number of M separate transformers with the relation of $M \times N_P:N_S$ [*M : number of primary loops, N_P : number of primary turns, N_S : number of secondary turns*]. Each of the power devices is coupled to each of the $N_P:N_S$ ratio transformers, in which all primary loops are combined in parallel, and the single multi-turn secondary is shared with all primary loops. The turn ratio of primary and secondary loops is defined such that it always satisfies $N_P < N_S$, which boosts the AC voltage from primary loops to the secondary loop. Assuming an ideal coupling coefficient case, the magnetically induced currents are added together into the secondary loop in the same phase as follows:

$$\begin{aligned} V_S / V_P &= N_S / N_P \\ I_S / I_P &= M \cdot N_P / N_S \end{aligned} . \tag{1}$$

Also, the impedance seen by each power device is calculated as follows:

$$R_P = M \cdot \left(\frac{N_P}{N_S} \right)^2 \cdot R_S . \tag{2}$$

By distributing the burden of total turn ratios to multiple primary loops, the impedance looking into the transformer from the drain, R_P, is higher than that of a single 1:N high turn ratio transformer. Therefore, a large size of a power device is not necessary, which ensures a more stable PA operation.

B. Implementation of 2×1:2 Transformer

Fig. 2 shows a physical layout and the equivalent schematic diagram of the simplest example, a 2×1:2 transformer. Two single-turn primary loops (*P1, P2*) and a single two-turn secondary loop (*S*) are employed. The transformer is designed such that the currents of the primary loops are always in the same direction with neighboring traces to prevent self-cancellation [4].

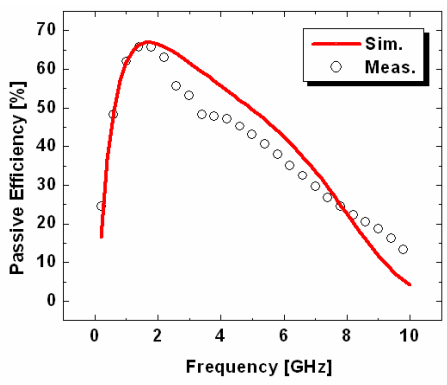

Fig. 3. Passive efficiency of the optimized transformer.

The key design parameters to optimize the passive efficiency performance are the width and thickness of metal traces, the spacing between adjacent metal traces, and an outer dimension of the transformer. The width and thickness of metal traces are directly related to the passive Q, which is the key factor to determine the insertion loss of the transformer. Another important design factor is to guarantee a large enough inductance for sufficient inductive coupling by narrowing the width to some extent that still keeps the passive Q reasonably high for low insertion loss. The widths of the primary and secondary loops are optimized to be 30 μm. There also exists an optimal spacing between adjacent metal traces that determines a dominant coupling mechanism between magnetic coupling and capacitive coupling. When capacitive coupling dominates, the passive loss can be increased. This optimization has to be considered in advance; otherwise, such a loss effect cannot be easily eliminated even by adding tuning capacitances in the output ports [5]. In our design, the spacing between adjacent metal traces is determined to be 5 μm. The outer dimension is also optimized to have minimum loss at the desired frequency range. The optimized transformer size for the best performance at 1.8 GHz is 850 μm × 730 μm.

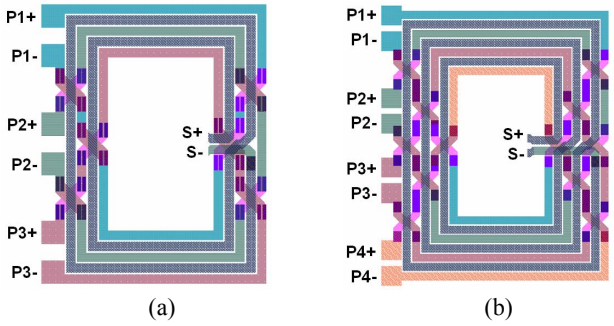

Fig. 4. Layout examples of extended transformer. (a) 3×1:2 transformer. (b) 4×1:3 transformer.

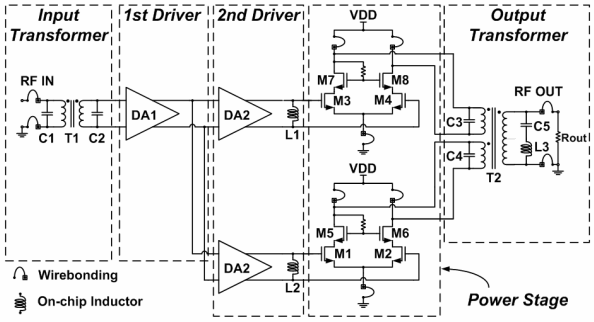

Fig. 5. Schematic diagram of class-E power amplifier.

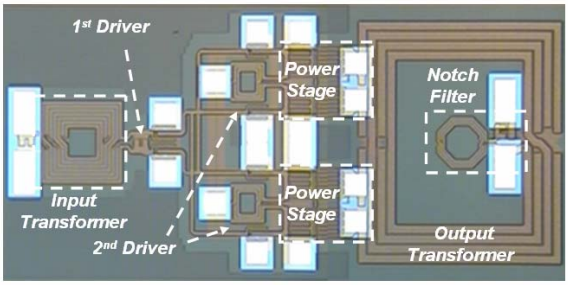

Fig. 6. Microphotograph of the class-E power amplifier with a 2×1:2 transformer.

The transformer is implemented in a standard 0.18-μm CMOS process with an aluminum top-metal thickness of 2.34 μm. Several sub-metal layers with a thickness of 0.53 μm are also used for interweaving metal traces through vias.

Passive efficiency of the optimized transformer is shown in Fig. 3. The simulated and measured insertion losses at the 1.8 GHz range are -1.74 dB (67%) and -1.83 dB (65.6%), respectively. The EM simulation results using Agilent ADS Momentum are well matched to the measured results. The achieved passive efficiency is close to the upper limit of 68% that the generic transformer can achieve in an ideal case [2].

C. Implementation of $M\times N_1{:}N_2$ Transformer

The proposed transformer structure can be extended to combine more than two power devices. To decouple the input and output power for stability purposes, the input ports are aligned on one side, while the output port is positioned on the other side. For a better inductive coupling, the secondary loop is designed to be guarded by two primary loops on both sides. Therefore, the total primary and secondary loops can be seen to be spatially overlapped so that their virtual centers are close to each other to maximize magnetic coupling [4]. Fig. 4 shows the layout examples of a 3×1:2 transformer and a 4×1:3 transformer according to the given design methodology.

The generalized advantages of the proposed transformer are summarized in Table I.

TABLE I
BENEFITS OF PROPOSED TRANSFORMER

Design Methodology	Benefits
Separation of transformer and power devices	Good stability Compact size
Decoupling of input and output	Good stability
Interweaved primary and secondary loops	Compact size Higher coupling

III. CLASS-E POWER AMPLIFIER DESIGN WITH A 2×1:2 TRANSFORMER

A class-E CMOS PA is designed to verify the feasibility of the proposed transformer. The schematic diagram of the designed CMOS PA is shown in Fig. 5. The PA consists of five key-cascaded functional blocks, (1) an input balun transformer, (2) a 1st stage driver, (3) a 2nd stage driver, (4) a class-E power amplifier stage, and (5) an output transformer. The input balun transformer (*T1*) functions as a DC block and a balun converting a single-ended input signal into a differential signal. Two driver amplifiers (*DA1, DA2*) are designed using an inverting amplifier topology with a stacked PMOS and NMOS. The power amplifier stage incorporates a cascode topology to overcome the susceptible voltage stress of submicron CMOS devices. Each of the unit power devices has a stack configuration of 0.18-μm common-source (*M1-M4*) and 0.35-μm common-gate (*M5-M8*). The gold wires bonded to the drain of the common-gate transistors work as a finite DC-feed inductance having the effect of increasing efficiency and reducing voltage stress [6]**.** DC biasing through the center tap of the output transformer (*T2*) should be avoided because of the voltage drop caused by large current drawing along the metal traces of the output transformer. Output RF powers from two power

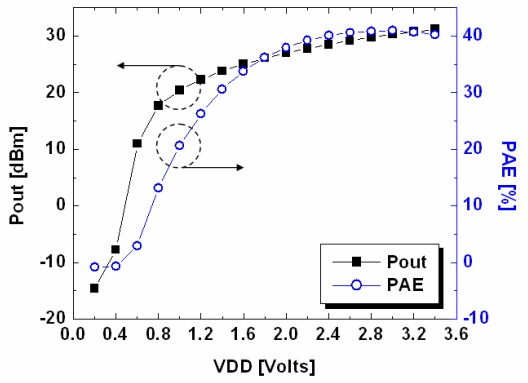

Fig. 7. Measured output power and PAE as a function of the supply voltage (Input power of 5 dBm).

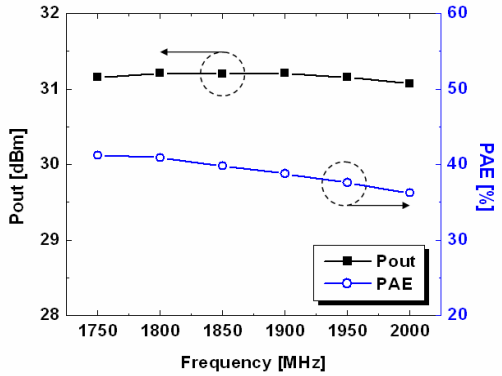

Fig. 8. Measured output power and PAE as a function of the operation frequency.

devices are combined through the 2×1:2 output transformer which is implemented according to the proposed design methodology. At the output port in the secondary loop, a series resonating *LC*-notch filter (*L3, C5*) is added to eliminate the 3rd harmonic component. The circuit simulation is verified by using Agilent ADS, and all passive structures and interconnections are heavily simulated by both Agilent Momentum and Ansoft HFSS.

Fig. 6 shows the microphotograph of the fabricated CMOS power amplifier in a 1-poly 6-metal standard 0.18-μm CMOS technology. The total die area is 0.96 mm × 2.04 mm.

The measured output power and PAE of the power amplifier along with the supply voltage at the 1.8 GHz range are shown in Fig. 7. At the supply voltage of 3.3 V, the power amplifier delivers an output power of 1.32 W (31.2 dBm) to a 50-ohm load with a power gain of 26.2 dB, and a PAE of 41%. Fig. 8 shows the output power and PAE of the power amplifier over cellular applications. The output power is fairly constant throughout the entire GSM high band with more than 31 dBm of output power, while the PAE slightly decreases as the frequency increases. Therefore, it can be derived from the result that the operating frequency range of the proposed transformer is wide enough for cellular applications. The proposed monolithic transformer can be a good candidate for watt-level CMOS PA applications.

V. Conclusion

A novel monolithic voltage-boosting parallel-primary transformer is proposed as a new power combining method for the fully integrated CMOS PA design. The structure offers voltage-boosting effect by increasing the turn ratio from primary loops to the secondary loop, while the multiple primary loops interweaved in parallel provide increased current in the secondary loop. By increasing both voltage and current in the secondary loop, the more efficient method of power combining can be realized monolithically. The structure has a compact geometry and moreover, it is spatially remote from power devices to avoid possible instability issues. A fully integrated CMOS power amplifier fabricated in 0.18-μm CMOS technology was presented using the proposed transformer structure. The measurement results demonstrate that the PA can deliver an output power of 31.2 dBm and a PAE of more than 40% with a 3.3-V power supply at a 1.8 GHz range.

Acknowledgement

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