A Highly Efficient GSM/GPRS Quad-band CMOS PA Module

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***Abstract* — The highly efficient CMOS Power Amplifier Module (PAM) is designed for quad-band cellular handsets comprising GSM850, EGSM, DCS, PCS and supports Class 12 General Packet Radio Service (GPRS) multi-slot operation. This module integrates an input matching network, a complete power control, and a thermal, over current, and load mismatch protection in a standard RF CMOS process and also contains a high-*Q* integrated passive device (IPD) for an output-matching network. The modular integration of the IPD makes it easier to manufacture PA module and also guarantees higher power-added efficiency (PAE) when compared with PAM products based on other technologies.**

***Index Terms* — CMOS PA, class-E, cascode, breakdown, power amplifier, transformer.**

I. Introduction

Recently, the demand for CMOS power amplifiers (PA) has been dramatically increased for the fully integrated IC solution for baseband, power management, and transceiver RF in wireless terminal. Though there are several successful demonstrations for watt-level PAs [1], it is still a very challenging task to implement a high output power CMOS PA with high efficiency. Switching PAs, class-E topology in particular, are widely used since they provide high efficiency and circuit simplicity [2]-[4]. Fig. 1 shows the circuit schematic of a typical class-E PA with an output network. A magnetically coupled transformer is an attractive solution for the output network because it can provide the impedance transformation and power combining at the same time for watt-level output power. Therefore, a class-E PA using a finite DC-feed inductance combined with the magnetically coupled transformer is a good solution for on-chip CMOS PA integration. Recently, several papers have been published for class-E or class-E/F PAs using a finite DC-feed inductance integrated with transformers [5]-[8]. When a transformer is combined with a class-E PA, the impedance of the transformer can be a part of a class-E load network, thereby minimizing the number of elements and maximizing efficiency. However, the silicon (Si) substrate used in a traditional CMOS process is conductive, which increases RF loss and severely degrades the performance of passive circuit elements. Accordingly, there is a need for novel CMOS PA designs that include integrated passive devices (IPD) on high resistive substrates so that the quality (*Q*) factor of passive device is not the bottleneck of overall PA performance.

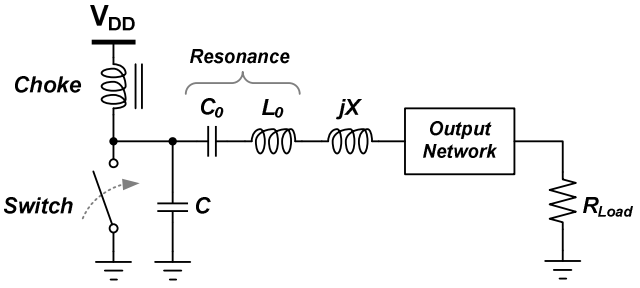


Fig. 1. Schematic of a class-E PA with an output network.

In this work, we demonstrated the implementation of the highly efficient GSM/GPRS quad-band CMOS PA module which meets all the 3GPP standards. By using the high-*Q* integrated passive devices and module technology, the PA achieves power added efficiency levels that are among the highest in the GSM PA reported. This paper also demonstrated the integration techniques that allow the multi-band PA core and the power controller to be implemented in a single die with a standard silicon CMOS technology bringing the cost advantage of true CMOS integration. The integrated 50Ω input and output matching circuitry in the standard 5×5 leadless plastic package enables to significantly minimize the bill of material.

II. Class-E PA Design with Parallel Power Combining

The schematic diagram of the designed CMOS PA is shown in Fig. 2. For the low-band (GSM/EGSM) PA, three parallel stages of power devices are incorporated for its high power requirement, while two parallel power stages are used for high-band (DCS/PCS) PA design. The 2nd driver stage and the power stage can be extended further by adding the same blocks in parallel to increase the output power level based upon the power requirement. For the single-ended input and output connection, two balun functions are implemented at the input and output. For the driver amplifiers, differential inverters are used as shown in Fig. 2. These driver amplifiers provide the signals to the power stage with maximum swing from the ground to the supply voltage without using inductor bias feeding, resulting in compact design with simplification. Between the 2nd driver stage and the power stage, each unit power cell has its own interstage matching inductor (L_1) to

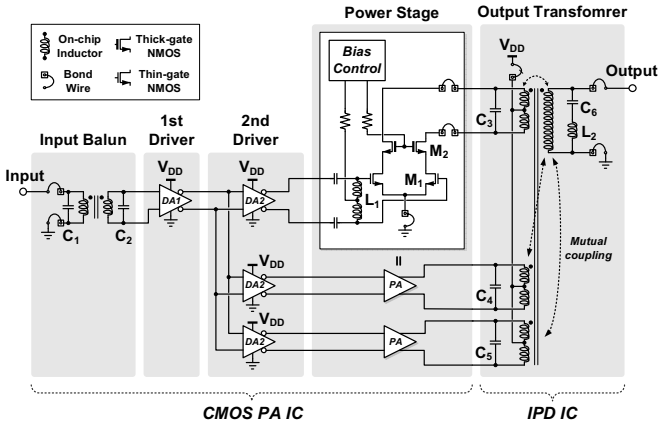


Fig. 2. Schematic diagram of the proposed CMOS cascode class-E PA with IPD transformer.

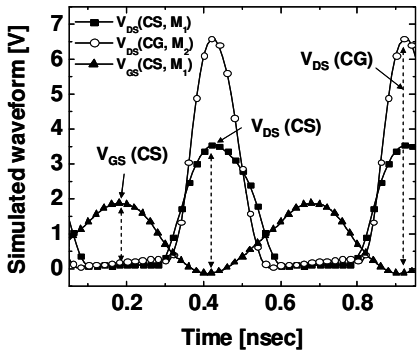


Fig. 3. Output waveform of power stage.

resonate out the gate capacitance. Since a unit power cell is a parallel connection of transistors, there exists an unwanted large capacitance that hinders driving of the power stages.

For high efficiency, a topology of the class-E switching PA family [9] is used in the power stage. Because of high voltage stress of class-E PAs that occurs from drain to gate, and from drain to source, a protection scheme is required. Generally, a CMOS device can sustain only twice of a given supply voltage [7]. Therefore, to avoid voltage stress of CMOS devices, a cascode topology is used particularly for the power stage, as M_1 and M_2 in Fig. 2. In simulation, stacking of the thick-oxide 0.35μm common-gate (CG) and thin-oxide 0.18μm common-source (CS) can endure up to around 10V, distributing the voltage stress to the CG and CS stacks as 6.2 V and 3.6 V, respectively as shown in Fig. 3 [2].

To transform impedance from the low impedance of switching network to 50Ω load, a transformer with multi-segment primary and multi-turn secondary was designed. Multi-turn secondary transforms the impedance while multi-segment primary increases the magnetic coupling [10], therefore minimizing passive loss. There have been several efforts to realize the function of power combining and impedance transformation at the same time by using

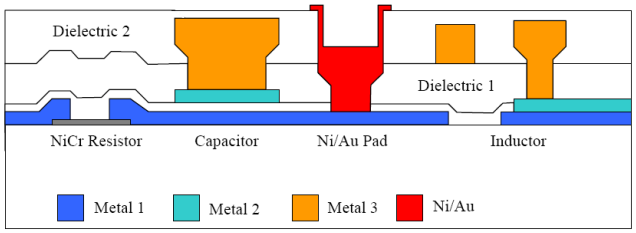


Fig. 4. Layer Configuration of integrated passive device.

transformer-type output networks. They can be categorized as series-combining transformers (SCTs) [5] and parallel-combining transformers (PCTs) [7] according to their ways of voltage and current combining at the load.

Because PCTs enable efficient power combining with a good passive characteristic and less output driving as well as its adaptability to the separated high-Q passive solution, we incorporated PCTs using IPD technology. The turn ratio of the transformer is chosen within a proper range, if possible, of low values to avoid unnecessary complexity. To minimize the loss, a process with low metal resistance, low substrate conductivity, and larger distance between the metal and substrate is preferred [11]. From this point of view, a general standard CMOS process is not considered as a good candidate for on-chip transformers in terms of material quality. Therefore, in this design, IPD was incorporated for better power combining and impedance transforming. Fig. 4 shows the vertical structure of Samsung's own IPD technology. The thickness of the top metal is 10μm copper, while that of 0.18μm RF CMOS process is 2.34μm aluminum, thus the parasitic resistance of the transformer is much lower than that of conventional RF CMOS processes. Moreover, the increased edge-side coupling due to the thicker metal line can raise the coupling factor of transformers. The Q factors of the designed transformers are high up to 20.

To implement the proposed transformers, there are several design guidelines to follow. First, adjacent metal traces should belong to different windings to decrease self inductance and increase mutual inductance [11]. Second, the length of each primary winding is adjusted until all the primary windings have equal phase delays from the inputs of the primary windings to the ports of the secondary winding to avoid destructive current coupling. Hence, primary metal traces need to be interweaved to have equal electrical length. Third, the distance between opposite edges should be as far as possible to suppress negative magnetic coupling, that is, the shape should be close to a regular polygon. Fourth, the ports of primary windings are aligned at one edge of the layout for easy connection to unit power cells, while the secondary port is positioned at the opposite side to maximize the isolation between the input and output. In addition, physical specifications such as the outer dimension, the width of metal traces, and the spacing between metal traces are key design parameters to optimize the performance. Outer dimension is closely related to the inductance for mutual coupling, and

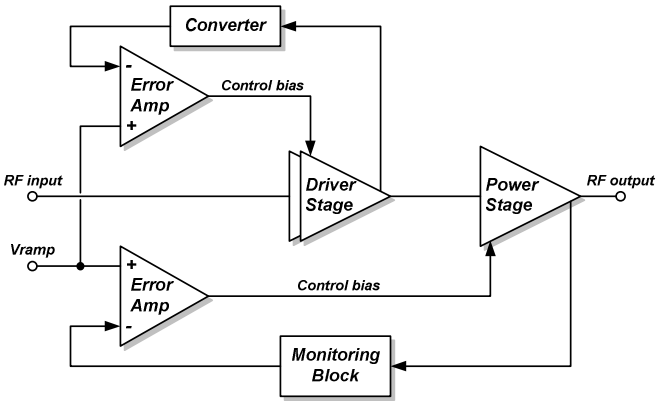


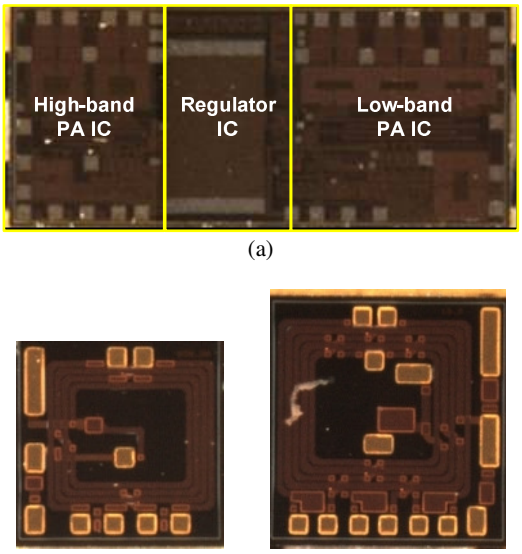
Fig. 5. Closed-Loop power control blocks.

width and thickness determine the Q of metal traces while the spacing is determined between capacitive coupling and magnetic coupling. Based on these design guidelines and parameters, two transformers, a 2×1:2 for high-band transformer and a 3×1:2 for low-band transformer, are designed as shown in Fig. 6 (b) and (c), respectively. The overall dimension is optimized considering the size of the die and the frequency band of interest. At the output port, a notch filter (C_6, L_2) is attached in parallel to suppress the third order harmonic component.

With an advance of recent wide variety of mobile communication standards, the technical demand for more accurate and more efficient control of output power of the mobile transmitter system has emerged. The control of output power is required from various reasons such as a) to prevent one cell from interfering with the reception of other neighboring cells, b) minimizing output to reduce the power consumption from the limited source of energy while keeping the communication capability. As shown in Fig. 5, the PA system include driver stages and a power stage that are operative to receive the input signal and generate an output signal, and a feedback loop that receives the power control signal and generates a control bias signal for adjusting an operation of the PA. The feedback loop includes a sensing block that detects a parameter associated with the output signal of PA, and a comparator that compares the detected parameter or a variation of the detected parameter to the received power control signal, wherein based upon the comparison, the comparator generates a compensation signal. The power controller also integrated various protection features such as over temperature, over current, and load mismatch.

IV. Implementation and Measurement Results

Fig. 6 (a) shows the microphotograph of the fully integrated quad-band PA and power controller fabricated in a 1P6M 0.18μm CMOS technology. The die area is 2.64mm×1.15mm. Fig. 6 (b) and (c) shows the high-band transformer and low-band transformer, respectively, implemented in IPD



(a)

(b) (c)

Fig. 6. Microphotographs of (a) CMOS PA IC, (b) High-band transformer IPD IC, and (c) Low-band transformer IPD IC.

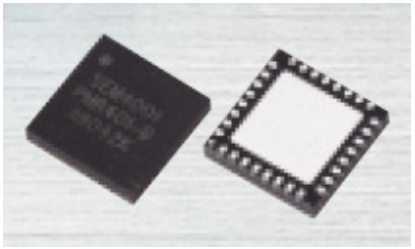
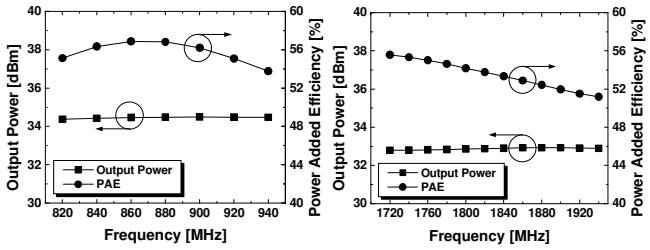


Fig. 7. Photograph of packaged PA module.



(a) (b)

Fig. 8. Measured output power and PAE in (a) Low-band PA, (b) High-band PA.

technology of Samsung Electro-Mechanics. Those dies are packaged in 5×5 32-pins standard leadless plastic package. The input and output of the package part are 50Ω matched so there is no need for any off-chip matching components, except bias bypass capacitors, which can dramatically reduce the overall BOM cost. The front and back sides of CMOS PA package part are shown in Fig. 7.

Fig. 8 shows the measured output power and PAE versus frequency in (a) low-band and (b) high-band of interest. The 34.5dBm of output power with 55% PAE is demonstrated in low-band PA, while 32.5dBm of output power with 52% of

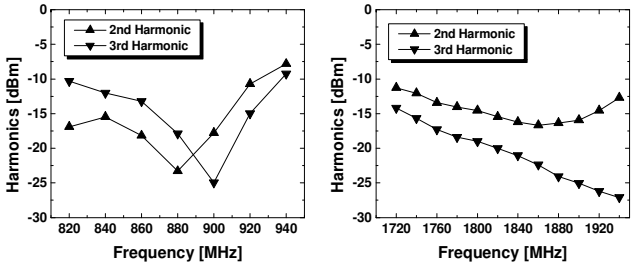


Fig. 9. Measured harmonics in (a) Low-band PA, (b) High-band PA.

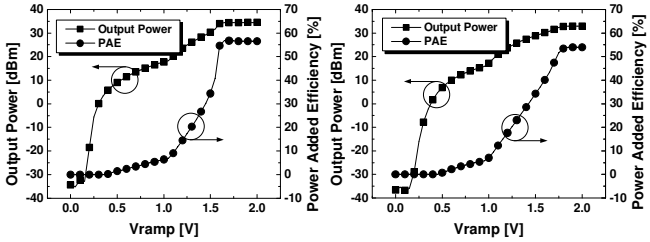


Fig. 10. Measured gain control in (a) Low-band PA, (b) High-band PA.

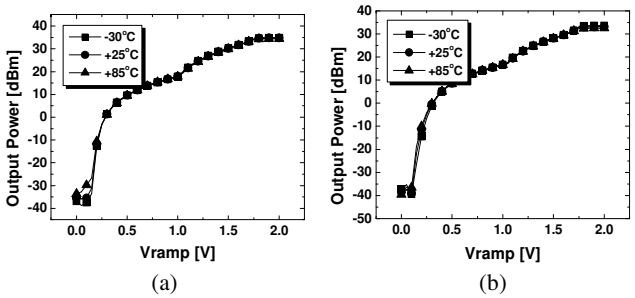


Fig. 11. Measured temperature variation of gain control in (a) Low-band PA, (b) High-band PA.

PAE is generated in high-band PA when 3.4V power supply and 0 dBm RF input are supplied.

Fig. 9 shows the 2nd and 3rd harmonics performance of (a) low-band PA and (b) high-band PA. Less than -10dBm of harmonics power are observed over the band of interest. Fig. 10 shows the power control performance in both low and high bands. More than 60 dB of dynamic range was achieved with control slope of less than 100dB/V. Fig. 11 shows the power control variation depends on various temperatures. With the aid of closed-loop compensation, the power control variation is within +/-0.5dB range.

V. Conclusion

In this paper, the highly efficient CMOS PA module is demonstrated for quad-band Class-12 GPRS applications. This module integrates an input matching network, a complete power control circuitry, and a thermal protection, an over-current protection, and load mismatch protection in a standard RF CMOS process and also contains a high-*Q* IPD for an output-matching network. Experimental results demonstrate the output power of 34.5dBm with 55% of PAE in GSM/EGSM band and 32.5dBm of output power with 52% of PAE in DCS/PCS band. This CMOS PA module also meets all the required specification from 3GPP. The high-*Q* modular integration solution for CMOS PA guarantees higher power-added efficiency (PAE) when compared with PAM products based on other semiconductor technologies.

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