A 1-Watt Doubly Balanced 5GHz Flip-Chip SiGe Power Amplifier

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Abstract — **A doubly balanced 5GHz flip-chip SiGe power amplifier with Low Temperature Co-Fired Ceramic (LTCC) matching networks is described. A doubly balanced amplifier features two balanced amplifiers connected in a push-pull configuration using 180-degree hybrids[1]. The amplifier achieves a saturated output power and power added efficiency (PAE) of 31.5dBm and 24% respectively. At its 1dB compression point, the amplifier delivers 29.6dBm to a 50Ω load, and has a PAE of 18.5%. At 5GHz, the amplifier's small-signal gain is 20.6dB, with input and output return losses in excess of 10dB. The amplifier's 1dB power bandwidth is 700MHz.**

I. Introduction

In recent years frequencies at 4.9GHz to 5.9GHz have been allocated for data transmission systems such as IEEE 802.11a, HIPERLAN II, and public safety systems. Each of these systems requires a power amplifier (PA) as part of the transceiver hardware, and they each allow a different maximum output power from the transmitter. For example, HIPERLAN II allows a maximum of 29dBm to be transmitted while IEEE 802.11a has different limits depending on whether the transmission occurs in the lower (5.15GHz-5.35GHz) or the upper band (5.725GHz-5.875GHz). In the U.S. a public safety band has been recently allocated at 4.9GHz covering a 50MHz bandwidth (4.94GHz-4.99GHz), with a proposed modulation format similar to IEEE 802.11a. The public safety band is a licensed band, and a proposed transmitter output power from the base station is near 1W.

Traditionally, power amplifier circuits at high frequencies have been and currently are implemented in GaAs processes. Recently, interest in developing SiGe HBT based power amplifiers has increased. To date, the SiGe power amplifiers that have been described in the literature are directed at frequencies lower than 5GHz [1], [2]. SiGe power amplifiers intended for IEEE 802.11a-like applications have been described in industry journals but complete specifications are not available [3]. In contrast, the SiGe PA circuits described in this paper deliver at least 9dB more linear output power than the SiGe PA described in [3].

SiGe devices capable of operating at 5GHz have a low collector-emitter breakdown voltage, making it difficult to extract high output power from a single transistor. The doubly balanced configuration, allows one to quadruple the output power of a single transistor amplifier. To this end we describe a 1-Watt doubly balanced SiGe power amplifier suitable for use in the public safety band transceivers.

The amplifier employs SiGe HBTs available in Motorola's 0.35μm BiCMOS process [4], [5]. The SiGe HBTs have a peak f_T and a peak f_{max} of 48GHz and 86GHz respectively. The process provides metal-insulator-metal (MIM) capacitors, a variety of poly-silicon resistors, and spiral inductors fabricated in 10μm thick copper [4], [5]. The silicon die contains the SiGe HBTs for PA service, a base bias voltage generator with a bias tee implemented using a MIM capacitor and a copper spiral inductor. Each device pair needed to implement a balanced amplifier [6] was fabricated on the same die. For flexibility in test and evaluation, this implementation of the doubly balanced amplifier combines two separate balanced amplifiers using external 180-degree hybrids.

The paper is organized as follows: Section II provides an overview of the doubly balanced power amplifier topology, Section III presents the design methodology, Section IV presents the measured results, and Section V presents the summary and conclusions.

II. Overview of the Doubly Balanced Amplifier

A doubly balanced amplifier described here combines the concepts of a microwave balanced amplifier [6], and an integrated circuit differential (or push-pull) amplifier. Two balanced amplifiers are combined in push-pull to form a doubly balanced amplifier as shown in Fig. 2.1. In addition to quadrupling the power from a single amplifier, the doubly balanced power amplifier topology allows one to implement an antenna switch suitable for time division duplex (TDD) systems without any additional components. Furthermore, the implemented antenna switch does not degrade the intermodulation (IM) performance of the system. While an antenna switch using hybrids has been described in the literature [7], the doubly balanced configuration, in addition to providing an antenna switch, allows one to maintain a fully differential transceiver architecture, and provides a convenient port to monitor the output power of the amplifier. The block diagram in Fig. 2.1 shows the connections to the receiver front end, represented by an LNA, and the power meter port.

[1] Patent Pending.

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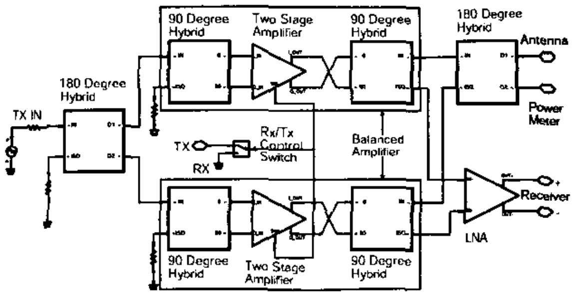

Fig. 2.1. Doubly Balanced Transceiver Topology.

III. Design Methodology

The design technique employed makes use of load-pull simulations using a commercially available Harmonic Balance (HB) simulator to estimate the HBT's emitter area. In these simulations, the HBTs were described by foundry-supplied nonlinear models. After completing the layout, the on-silicon metallization pattern is simulated using a commercially available 2.5D electromagnetic (EM) simulator to obtain its multi-port s-parameters. The foundry-supplied active device model is embedded in the obtained multi-port s-parameters to form a "composite" device model. Then, this composite device model is subjected to a second round of load-pull simulations to plot a set of constant output power and PAE contours. The HB simulator also allows one to run a two-tone load pull simulation where the third order IM power contours can be overlaid on the output power and PAE contours. The choice of optimum load impedance is a compromise between these three conditions.

The matching networks and the Lange couplers needed for a two-stage balanced amplifier topology were designed using commercially available LTCC material. Each dielectric layer has a thickness of 96.5μm and a relative dielectric constant of 7.8. The metallization is silver and has a conductivity of $4.6x10^7$ S/m. The output-matching network was designed to show the collectors of the active device the load impedance determined through load-pull simulation using the composite device model described earlier. The designed matching network was simulated using the 2.5D EM simulator over a wide range of frequencies that covers the passband and parts of the stopband above and below the passband. Similarly, the interstage matching network was designed to transform the conjugate of the input impedance seen looking into the final stage to the desired load impedance of the driver, and lastly, the input matching network was designed to provide a conjugate match at the input port of the driver stage. As in the case of the matching networks, the Lange couplers needed to implement the balanced amplifier were simulated using the EM simulator. Upon completion of each design, a two stage balanced amplifier was described in the HB simulator using the composite device model and the multi-port s-parameters of the matching networks, and Lange couplers obtained from EM simulations.

The Lange couplers and all the matching networks needed to implement the balanced amplifier (from here on referred to as a singly balanced amplifier) were fabricated in LTCC at an in-house prototype facility. The flip-chip assembly was also done at an in-house facility. A photograph of an assembled singly balanced amplifier is shown in Fig. 3.1. The photograph shows two separate die, one for the driver and one for the final stage. From this figure it is clear that the number of connectors needed to test the amplifier limits the minimum size of the LTCC.

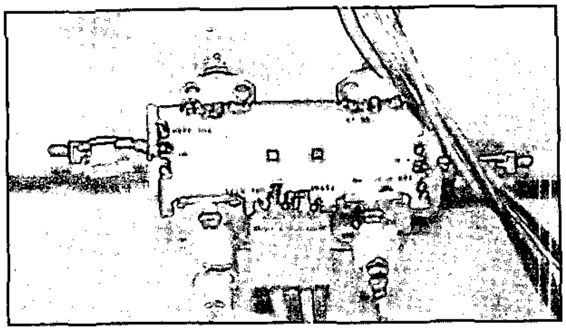

Fig.3.1. Photograph of the Singly Balanced, Two Stage Power Amplifier.

IV. Measurement Results

In this section we present the measurement results obtained with one pass of the silicon and the LTCC. We present three test results for the singly balanced amplifier, followed by the measured results of the doubly balanced amplifier. Fig. 4.1 shows the small-signal s-parameters of the two singly balanced amplifier units used to implement the doubly balanced amplifier. As it can be seen the two units have essentially identical s-parameters.

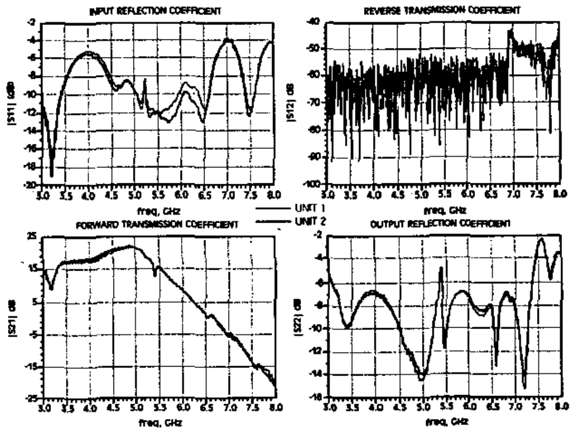

Fig. 4.1. Measured Small-Signal S-Parameters of Each Singly Balanced Amplifier.

From the data in Fig. 4.1, we find that at 5GHz the amplifier provides a small-signal power gain of 21.5dB, an isolation of 57dB, and the input and output return losses are better than 10dB. The measured 1dB bandwidth of the amplifier covers 4.45GHz to 5.15GHz. Two resonances that can be seen in the measured s-parameters at approximately 5.25GHz and 5.4GHz are potential causes for not having yet a wider 1dB bandwidth. At this time the causes of these two resonances are unknown.

Fig. 4.2 presents the single-tone compression characteristics and the PAE of the singly balanced amplifier. From the data in this figure, we find that the 1dB compressed output power of the singly balanced amplifier is approximately 26.9dBm into a 50Ω load. At this output power the PAE of the singly balanced amplifier is 21.5%. The two-tone compression characteristics of the singly balanced amplifier are shown in Fig. 4.3. From this figure we find that a third order IM suppression of 35dBc is obtained for an output power slightly better than 19dBm per tone, or 22dBm peak envelope power (PEP).

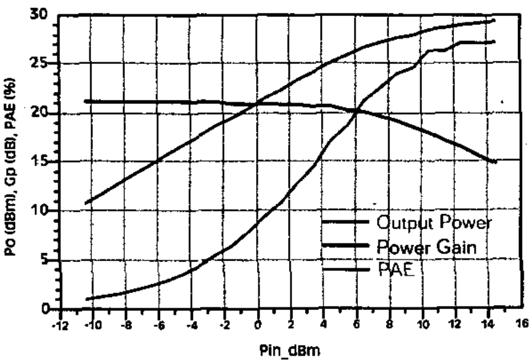

Fig. 4.2. Measured One-Tone Compression Characteristics and Power Added Efficiency of the Singly Balanced Amplifier.

We have shown the small-signal responses of each singly balanced amplifier unit used in the implementation of the doubly balanced amplifier, and for purposes of brevity only the results of one amplifier unit obtained from the compression tests. From our measurements, we have found that each of the two amplifiers used to implement the doubly balanced configuration exhibit nearly identical results as will be seen from the results presented next.

The test setup of the doubly balanced amplifier is shown in the photograph in Fig. 4.4. As it can be seen from Fig. 4.4, two short segments of cable and two external 180-degree hybrids were needed in the assembly. Each hybrid and cable segment contributes a loss of approximately 0.3dB and 0.2dB, respectively, for a total loss of 1dB as compared to the singly balanced amplifier. Of course, the final system will include both singly balanced amplifiers on one LTCC substrate, thereby eliminating the cable losses and raising the gain of the amplifier by 0.4dB.

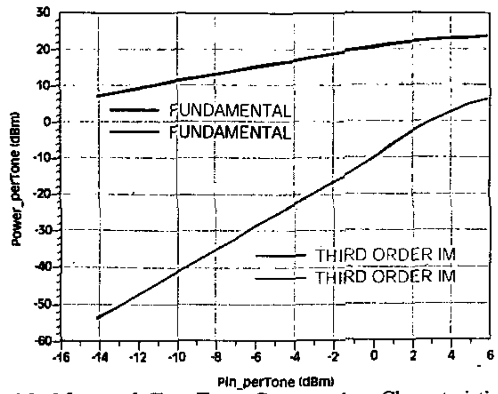

Fig. 4.3. Measured Two-Tone Compression Characteristics of the Singly Balanced Amplifier (Each Tone).

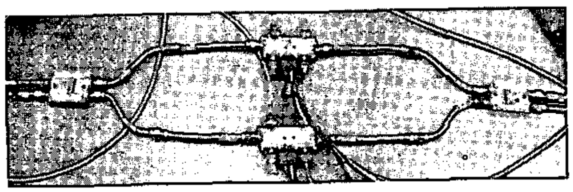

Fig. 4.4. Test Setup of the Doubly Balanced Power Amplifier.

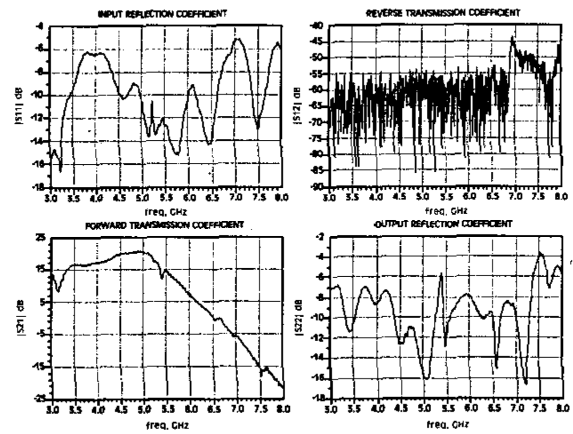

Fig. 4.5. Measured Small-Signal S-Parameters of the Doubly Balanced Power Amplifier.

The measured small-signal s-parameters of the doubly balanced amplifier are presented in Fig. 4.5. From this data we find that the small-signal gain is 20.6dB, or approximately 1dB lower than the singly balanced amplifier, as expected. If the cable losses described earlier can be recovered, then the gain would become 21dB.

The one-tone compression characteristics of the doubly balanced power amplifier are shown in Fig. 4.6. In this test, for identical amplifiers, we expect the 1dB compression point to be approximately 2.7dB (3dB minus the output hybrid's loss) higher than that of the singly balanced amplifier. From the data in Fig. 4.6, we find that the output power at the 1dB compression point is approximately 29.6dBm, 2.7dB higher than the 1dB compressed output power of the singly balanced amplifier, as expected. This result suggests again that the two singly balanced amplifier units have essentially identical compression characteristics. In Figs. 4.7 and 4.8 we present the two-tone compression characteristics of the doubly balanced power amplifier. Fig. 4.7 shows the fundamental and third order intermodulation (IM_3) product powers (each per tone), while Fig. 4.8 shows the output power spectrum with the drive level adjusted for an IM_3 rejection of 35dBc. From the measurement results shown in Fig. 4.7 and 4.8, it can be seen that at this IM_3 rejection, the doubly balanced power amplifier delivers 22dBm per tone, or 25dBm PEP, to the 50Ω load. The output referred third order intercept is computed to be 39.1dBm.

V. Summary and Conclusions

We presented a 1Watt doubly balanced SiGe power amplifier suitable for use in 4.9GHz safety-band applications. The active devices were flip-chip assembled onto a multilayer LTCC that contains all matching networks, and Lange couplers needed to implement a balanced amplifier. Some of the measured parameters are summarized in Table 5.1, along with other 5GHz SiGe and InGaP based power amplifiers available in the industry.

Table 5.1 Power Amplifier Parameters.

Parameter	This Work	MAX2841 [3]	LX5503 [8]
Power Gain	20.6dB	22.8dB	22dB
$P_{o,1dB}$	29.6dBm	18dBm	25dBm
PAE @ $P_{o,1dB}$	18.5%	N/A	N/A
$P_{o,sat}$	31.5dBm	N/A	> 26dBm
PAE @ $P_{o,sat}$	24%	N/A	N/A
Device Process	SiGe	SiGe	InGaP

As it can be seen from Table 5.1, the SiGe power amplifier described in this work delivers more output power than the amplifiers in [3], and [8], while providing comparable power gain. The doubly balanced amplifier has sufficient bandwidth to cover the IEEE 802.11a and HIPERLAN II bands, if the response of the amplifier is shifted up in frequency. This may be accomplished with a redesign of the matching networks. To our knowledge, this is the first 5GHz SiGe power amplifier that is capable of delivering 1W to a 50Ω load.

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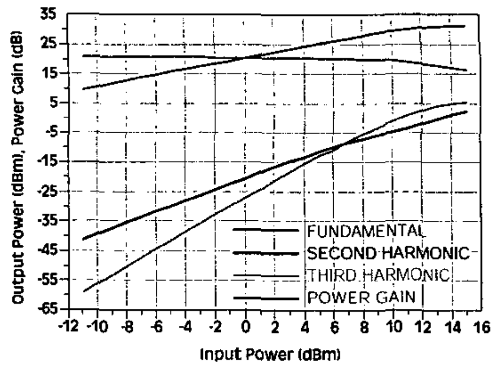

Fig. 4.6. Measured One-Tone Compression Characteristics of the Doubly Balanced Power Amplifier.

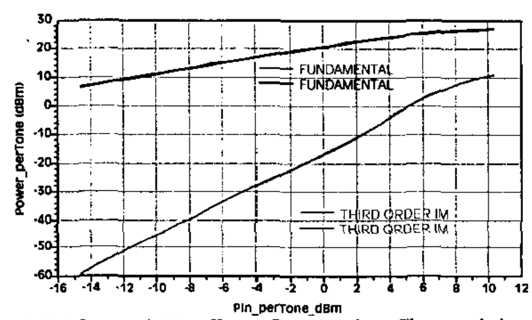

Fig. 4.7. Measured Two-Tone Compression Characteristics of the Doubly Balanced Power Amplifier.

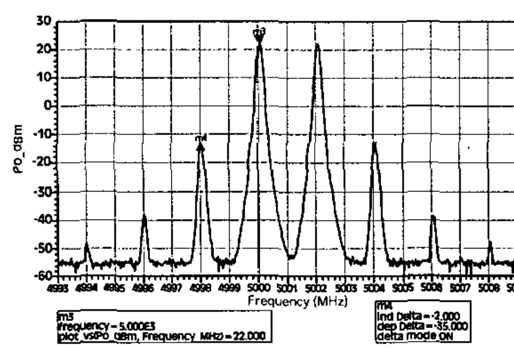

Fig. 4.8. Measured Two-Tone Output Spectrum of the Doubly Balanced Power Amplifier.