A Novel CMOS Transmitter Front-end for Mobile RFID Reader

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***Abstract* — Aiming at the specified protocol of EPC global Class-1 Generation-2, design considerations are expatiated to a novel structure of transmitter front-end for mobile RFID reader with 0.18um CMOS process. The transmitter front-end consists mainly of an up-conversion mixer, a linear power amplifier (PA) and a non-linear PA. Controlled by the reader's working status, the implemented scheme can transmit high efficient carrier or linear ASK-modulation data at separate periods. The linear PA can provide a power gain of 16.3dB and a 1dB output power of 19dBm. The non-linear PA can achieve 1dB output power of 20.6dBm and a maximum power-added efficiency (PAE) of 44%. The output waveform and spectrum are tested to verify the feasibility of the designed transmitter.**

***Index Terms* — CMOS, power amplifier, RFID reader, transmitter**

I. Introduction

As the worldwide RFID market has been growing tremendously, potential applications of RFID are currently driving hardware developers to merge RFID readers into mobile devices such as PDAs and cell phones, which will enable individual customers to acquire product information through their own RFID readers.

In the integrated-circuit (IC) design field, CMOS-based solutions are very competitive in power consumption and large scale integration, but it is placed at a disadvantageous position in output power and tx-rx isolation. Great efforts are engaged to develop a fully-integrated CMOS single-chip solution for an RFID system. Although several successful examples come forth on the integration of RFID reader with CMOS process [1-3], there is still no real power amplifier (PA) module in the CMOS-based RFID reader chip. It is a great challenge to fulfill a fully-integrated CMOS reader with PA module.

A typical RFID system is comprised of reader, tags and communication system. Communication between reader and tags is half duplex. A reader first sends a modulated wave to tags, if tag lies within the interrogation range of the reader. When the reader waits replies, it must transmit the un-modulated carrier continuously in order to provide the power energy for tag's operation. After the reader receives information from tags, it verifies errors, determines their validity, and sends them to computer for further process. This paper demonstrates a novel configuration of transmitter front-end in mobile RFID reader for the protocol of EPC global Class-1 Generation-2 [4]. In the scheme, a linear PA and a non-linear PA is used to amplify the transmitted signal separately. The linear PA amplifies the modulated wave and the non-linear PA amplifies the un-modulated carrier. The designed transmitter was fabricated in 0.18um CMOS process. Test results verify the feasibility of the proposal structure.

II. Transmitter Architecture

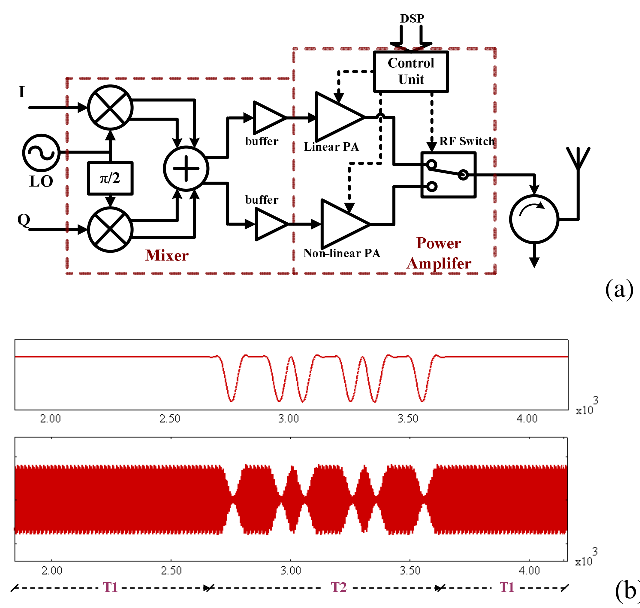

Fig. 1. (a) Block diagram of the transmitter front-end in RFID reader (b) baseband and RF output waveform at different period.

To a RFID reader, it is obviously that the reader transmits and receives signals at the same time with the same frequency. The working time of reader can be divided into two periods. At one period, the reader receives the tags' signal. Meanwhile it transmits the un-modulated carrier to supply the tag's energy. Within the other period, the reader sends ASK-modulated data to tags. Thus linear PA and non-linear PA can be applied respectively to amplify the different RF signal at different period, leading to a high linear and high efficient scheme.

Fig. 1 shows a block diagram of the proposed transmitter front-end for mobile RFID reader. The transmitter is made of on-chip modules and external components such as decoupling capacitor and RF switch. The main on-chip modules are an active up-conversion mixer, two buffers, a linear PA, a non-linear PA and digital control units. A linear PA is utilized to amplify the ASK-modulated RF signal for the demand of linearity. The non-linear PA is applied to amplify the un-modulated carrier on account of its high efficiency. At any time, there is only one PA be selected in amplifying mode and the other PA is turned off to enhance the overall efficiency. The main circuit modules in Fig. 1 are discussed as follow.

A. Direct Up-conversion Mixer and buffer

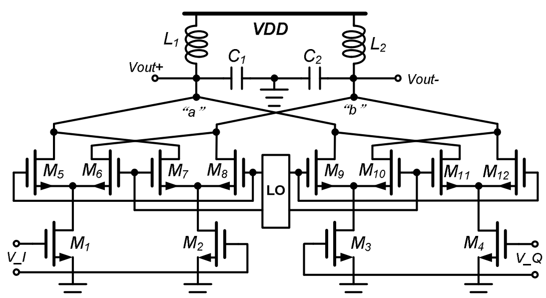

Fig. 2. Direct Up-conversion Mixer Architecture.

Fig. 2 shows the schematic of the differential active mixer. The mixer is realized as Gilbert cells with their outputs added in the current domain. The voltages of the differential I and Q baseband signals are converted to currents by the transconductors, M1-M4. These current signals are then added at points 'a' and 'b' in Fig.2. The other transistors, M5-M12, act as switches driven by external differential LO signals. Two inductors, L1 and L2, along with the capacitors C1, C2, and the parasitic capacitors of transistors M5-M12, form the LC tank for the differential RF output. Inductor loads are used for high frequency output to increase the output voltage swing. By the way, the desired modulation depth can be efficiently set through the DACs before the mixer in DSP unit.

The function of the buffers in Fig. 1 is to amplify the modulated RF signal from mixer and provide a larger input power to PAs. In the design, a common-source stage amplifier is selected to implement the buffer.

B. Linear Power Amplifier

In the design, a Class-AB PA is adopted to amplify the ASK-modulated RF signal in order to satisfy the linearity demand from the protocol of EPC global Class1 Generation2 [4]. The implemented 2-stage PA is shown in Fig. 3. The gate bias voltage of M3 and M1 is 0.85V and 0.9V to ensure that the 2 stages work at class A and class AB, respectively.

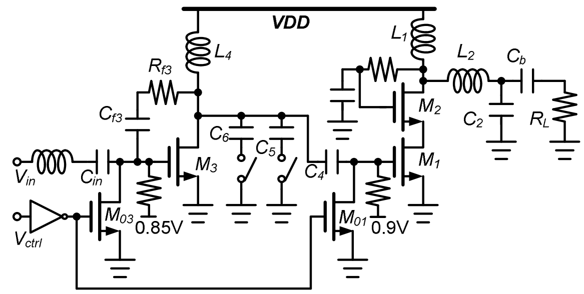

Fig. 3. Schematic of Class-AB PA.

In the output stage, a self-biased cascode structure along with thick gate-oxide transistor M2 is adopted to enhance the supply voltage and protect the transistors [5]. In the design, M1 is 0.18um transistor and M2 is 0.34um ones. With supply voltage VDD of 3.3V, the maximum gate-drain voltage does not exceed 2V even at the input signal power as high as 3dBm and the oxide breakdown doesn't occur.

In the input stage, resistor R_{f3} and capacitor C_{f3} comprise to a series feedback to increase the overall stability. Two switch-selectable capacitors C5 and C6 are added to the drain of M1 to improve the performance of inter-stage matching circuits.

Two output impedance-variable transistors M01 and M03 are added to the gate of M1 and M3, individually. When the control bit $Vctrl$ is "1", M01 and M03 are off and its equivalent effect is to add small capacitance to the gate of M1 or M3. When $Vctrl$ is "0", M01 and M03 work as a low-value resistance operating in deep triode region. Thus the equivalent resistance of M01 or M03 is equal to

$$R_{on} = \frac{1}{\mu_N \cdot C_{ox} \cdot (W/L) \cdot (V_{GS} - V_{TH})} \tag{1}$$

From the equation, a low value of R_{on} is maintained as long as the value of W/L and ($V_{GS} - V_{TH}$) is adequately large. Thus the gate voltage of M1 and M3 is near zero, leading to a null output and zero energy consumption.

C. Non-Linear Power Amplifier

Aiming at the high efficient demand of RFID reader, a Class-E PA is selected for its circuit simplicity and high frequency performance. The implemented 2-stage PA is shown in Fig. 4. The gate bias voltage of M1 and M3 is 0.52V and 0.85V to ensure that the 2 stages work at class E and class AB, respectively.

In the output stage, a self-biased cascode structure along with thick gate-oxide transistor M2 is adopted to enhance the supply voltage and protect the transistors. M1 is 0.18um transistor and M2 is 0.34um ones. The supply voltage of $VDD2$ is 3.3V and $VDD1$ of 2.8V.

Two switch-controllable transistors M02 and M04 are added to the gate of M1 and M3, whose function is the same as M01 and M02 in Fig. 3. Controlled by the same control bit $Vctrl$ from DSP, both functions of the controllable transistors in class-E and class-AB PA ensure only one PA in amplifying mode at any time. Meanwhile the other PA is in off mode.

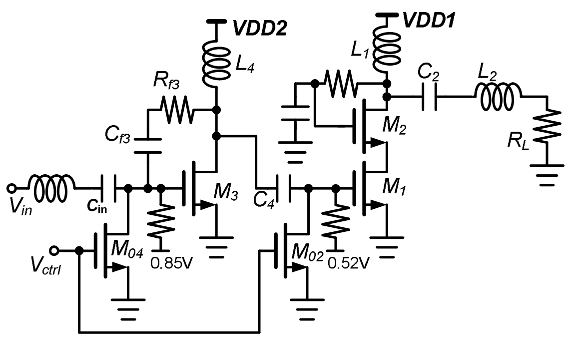

Fig. 4. Schematic of Class-E PA.

III. Experimental Results

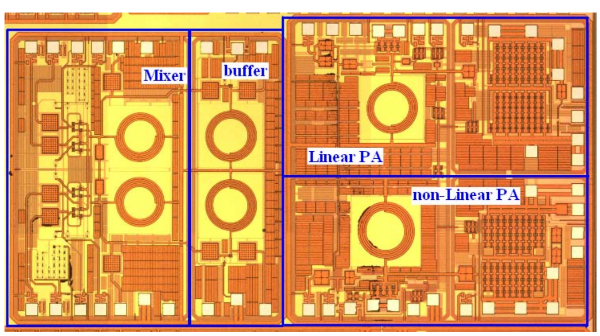

Fig. 5. Die photo of transmitter front-end.

The designed transmitter IC was fabricated in 0.18um 1P6M CMOS process. The die photograph is shown in Figure 5. It takes $3.1\times1.65mm^2$ silicon area including pads. A printed circuit board (PCB) for testing the chip is also fabricated. The chip is directly glued to the PCB board using an electrically and thermally conductive adhesive. Ground pads of the chip and the signal pads were wire-bonded to the gold-plated metal lines on the PCB.

The output power and gain of the designed active mixer including buffers are shown in Fig. 6. From the figure, the active mixer provides a conversion gain of 10.1dB and a 1dB output power of 3dBm.

The measured output power and PAE efficiency of linear class-AB PA is shown in Fig. 7. With the supply voltage of 3.3V and gate bias voltage of 0.9V in output stage and 0.85V in the driver stage, the linear PA can provide a power gain of 16.3dB. The 1dB output power is 19dBm and the maximum output power can be 21.8dBm. Small-signal gain flatness over the full UHF RFID band (860M-960MHz) is less than 2dB.

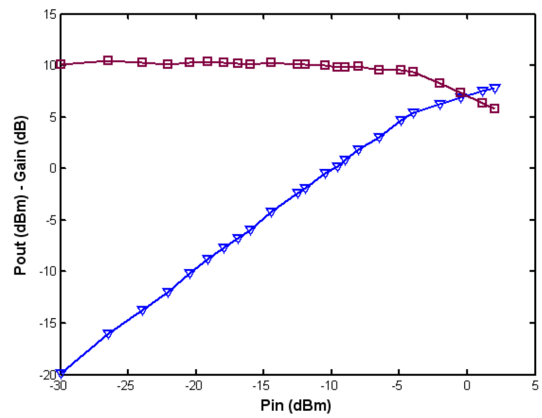

Fig. 6. Output power and gain vs. input power of mixer.

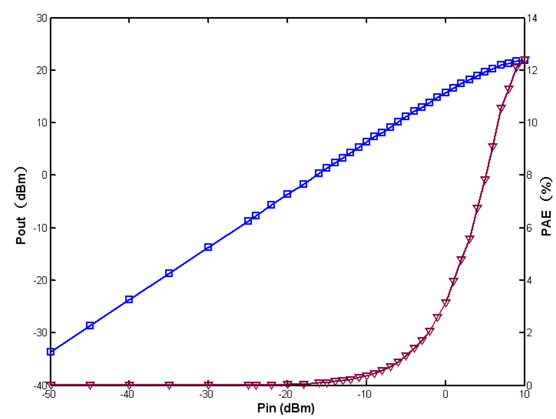

Fig. 7. Measured output power and PAE of Class-AB PA.

The measured output power and PAE efficiency of non-linear class-E PA is shown in Fig. 8. With the supply voltage of 3.3V and 2.8V, and gate bias voltage of 0.52V in output stage and 0.85V in the driver stage, the PA provides a power gain of 22.8dB. The 1dB output power is

20.6dBm and the corresponding PAE efficiency is 35.4%. The maximum PAE efficiency can be 44.0%. Small-signal gain flatness over the full UHF RFID band (860M-960MHz) is about 2dB.

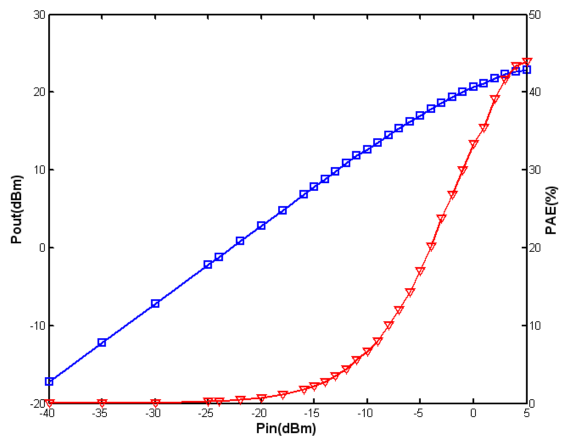

Fig. 8. Measured output power and PAE of Class-E PA.

An important characteristic of an RFID reader is the temporal envelope-shaping constraints. The reader needs to transmit a waveform with well-defined temporal characteristics to aid the tags in demodulating the signal. These time-domain constraints include envelope rise/fall time, envelope ripple, bit period, and modulation depth etc. Fig. 9 demonstrates the transmitted signal envelope of the DSB-ASK modulated waveform with the data rate of 80kbps.

Fig. 9. Measured waveform of baseband and output RF signal.

Another important characteristic of an RFID reader is the transmitted spectral requirements. Fig. 10 illustrates the measured output spectrum with the input signal of DSB-ASK modulation and Tari = 12.5us. The spectrum at the transmitter output satisfies the required spectrum mask in the multiple-reader environment condition of EPC global Class-1 Generation-2 standard.

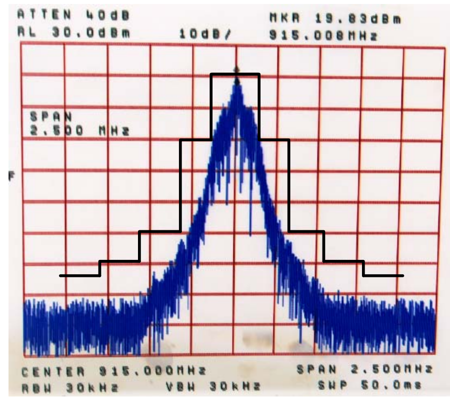

Fig. 10. Measured transmitter output spectrum and spectral mask for multiple reader environment.

IV. CONCLUSION

In this paper, a novel transmitter front-end for mobile RFID reader is proposed to obtain a high efficiency and high linearity output. The main highlight is a linear PA amplifies the modulated wave and a non-linear PA amplifies the un-modulated carrier, separately. The function of the scheme is verified with 0.18um CMOS process. The linear PA can provide a 1dB power of 19dBm. The non-linear PA can provide a 1dB power of 20.6dBm and a maximum PAE efficiency of 44%. Finally, transient wave and spectral are tested for the specified protocol of EPC global C1 G2.

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