An ESD protected RFIC Power Amplifier Design

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Abstract **— This paper presents the development of Electrostatic Discharge (ESD) protection circuitry for a three-stage Power Amplifier (PA) designed for 1.9 GHz Digitally Enhanced Cordless Telephone (DECT) applications. Through careful RF and ESD circuit co-design, good RF performance and ESD immunity are achieved. The PA features a high gain of 26dB at an output power of 25dBm, which remained unaffected due to the inclusion of ESD circuitry. The circuit's Power Added Efficiency (PAE) is also relatively unaffected, remaining at around 43%. The circuit is fabricated using a commercial 0.5µm SiGe-HBT process. The design is capable of protecting the PA from –4kV to +1.5kV Human Body Model (HBM) ESD stresses.**

Index Terms **— Electrostatic Discharge, Human Body model, LC-Tank, Power Amplifier, Radio Frequency Integrated Circuit (RFIC).**

I. INTRODUCTION

There is tremendous demand for increasing the electrostatic discharge (ESD) robustness of Radio Frequency Integrated Circuits (RFICs) in wireless communications applications, since such devices, typically handheld, are much more prone to ESD-induced damages. However, ESD protection structures also introduce parasitic effects that can adversely affect the performance of the core circuitry. Providing sufficient ESD protection for RFICs in wireless systems poses a major design and reliability challenge. ESD protection for digital ICs is relatively mature; however, ESD protection of RF circuits is still in its infancy and is the topic of significant research and development activities. No standard methodologies exist yet for RF ESD protection. Standalone PA's are of particular concern since they are currently not embedded in large System on Chips (SOC), but are more likely to be packaged in separate PA modules.

This paper reports on the development of a fully ESD protected 3 stage SiGe-HBT Power Amplifier designed for DECT application. It features novel ESD protection schemes optimized for RF performance that protect the PA from -4kV to +1.5kV standard HBM pulses (JESD22-A114-B [1]). These schemes can be straightforwardly extended to PA designs for other applications.

II. ESD PHENOMENON

When two objects at different electrostatic potentials are brought into close proximity such that their electric field lines interact, transfer of electrostatic charges between the two objects can occur. This process is called electrostatic discharge (ESD).

ESD events can be catastrophic to the IC if proper protection methods are not implemented. Internal methods require integration of on-chip protection devices, which are intended to provide an explicitly robust path for ESD currents between any pair of pins [2]. The protection circuit generally discharges the ESD strike by providing a low impedance path to ground, thereby shunting most, if not all of the transient away from the sensitive core circuits. The protection circuit should also clamp the pad voltage to a sufficiently low level during the ESD event.

A typical on-chip protection circuit is placed between the signal pin and the main circuit (Fig. 1) [3]. The diodes shunt excessive voltage applied to the signal pin towards V_{CC} or GND to divert the ESD strike from reaching the main circuit. An ESD protection circuit need not necessarily be based on diodes; depending on the available technology, it may alternatively be comprised of various devices such as thick field oxide (TFO) clamps, Silicon controlled rectifiers (SCRs), spark gaps, or transistors [4].

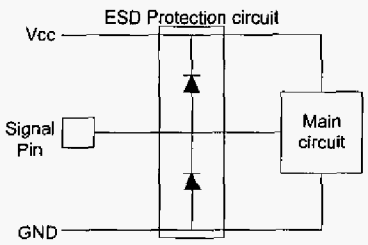

Fig. 1. A Simple ESD protection structure [3]

III. POWER AMPLIFIER DESIGN

This work focuses on developing ESD protection circuitry that does not adversely impact the performance and cost for high performance amplifiers. The starting

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amplifier features a high gain of 26 dB for output power ranges of 24dBm to 28dBm and a good Power Added Efficiency (PAE) of about 43%. All three stages of the amplifier are biased Class AB (first stage is more class A to obtain higher linearity) so as to increase the overall efficiency. The allowable supply voltage range varies from 1.6 to 4V; maximum current drawn is less than 400 mA with a standby leakage current of 3μA. The PA chip is fabricated using a commercial 0.5μm SiGe-HBT process with high Q on-chip inductors. It is packaged in a 3mm PQFP 12 Lead package.

The incorporation of an ESD protected structure requires careful RF/ESD co-design. For example, if the PA's RF input design accounts for the presence of the ESD structure, the designer can take advantage of the parasitic loading into the design of the RF input matching circuit. In this work, the input off-chip matching network was replaced with a shunt L – series C on chip matching network. The RF/ESD co-design is divided into two sections, control and supply lines, and RF input and output. The overall ESD protection design is discussed in the following section.

IV. ESD PROTECTED PA DESIGN

A. ESD diodes

The fabrication technology supports two non-scalable ESD diode structures that have been qualified against the HBM test. Zener based diodes have a breakdown voltage of about 7V while the HBT based collector-base (CB) junction diodes have a breakdown voltage of about 22V. The CB diode has a lower parasitic capacitance (Table 1) because of its smaller size. All diodes have a cut-in voltage (V_{on}) of approximately 0.7V. ESD diodes were characterized on-chip using pulsed IV (Accent DIVA D265) and S-parameter measurements.

TABLE I
ESD DIODE CAPACITANCES

	Capacitance @ 0 V, f = 1.91 GHz		
	Area μm^2	C (simulated) pF	C (measured) PF
Zener	50x30	2.46	2.291
CB	20x20	0.329	0.305

B. Control and Supply line protection (V_{en} and V_{cc})

Two approaches were investigated for protecting the control and bias lines. Fig.2(a) represents a diode ring approach [4]. Multiple diodes are used to prevent actuation under normal operating conditions (3V). The size of the diodes used for protecting control pin(s) is important, as the total capacitance at the pin must be charged/discharged during PA cycling. Their size is not important if used to protect supply pin(s), as it simply adds to the decoupling capacitance at the pin.

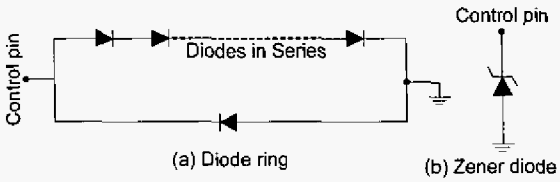

Fig. 2. (a) CB Diode Ring and (b) Zener diode approaches

The second approach uses just one reverse biased Zener diode [Fig.2 (b)] between the voltage line and ground and is therefore more area efficient. This approach utilizes both forward and reverse bias characteristics of the diode unlike the above approach, which utilizes only the forward characteristics of the diode. Zener diodes were used because of their lower reverse breakdown voltages. It should be noted that this approach is more immune to stronger negative HBM pulses. For a positive ESD strike the diode breaks down at about 7V, providing a slight overshoot for a very short period of time (few ns). For a negative strike, the Zener (acts in forward bias) turns on at its V_{on} providing a much lower voltage overshoot. To make the device indifferent to the positive and negative ESD strikes, we can either design Zener diodes with comparatively lower breakdown voltages (which is typically not an option for IC designers) or use the diode string approach. However, the single Zener approach is more area efficient as compared to the diode string approach especially given that there is more than one control line to protect.

C. Input and Output protection (RF_{in} and RF_{out})

ESD currents typically have a lower frequency spectrum as compared to the desired RF signals. Therefore the protection circuit should essentially act like a low pass filter. The basic electrical component with such a characteristic is an inductor. Therefore, an on chip shunt inductor used at an RF port can divert the ESD strike to ground. Where a normal ESD protection structure adds parasitics to the device, this inductor not only tunes out the parasitics at the input (or output) but also provides matching capability. On the other hand, the inductor acts like a shunt path to ground at ESD frequencies. An external capacitor may be added to obtain a more realizable value of on-chip inductance. The transmission loss of the low pass circuit must be as low as possible so that the circuit does not significantly degrade the input/output signal levels. Inductors with a higher Q-factor will reduce the transmission loss. However, the Q-factor

should also be low enough so as to increase the bandwidth. Hence an optimum value of inductance (2n H) was chosen so as to achieve lower loss and a reasonable bandwidth.

In this amplifier, the output match is realized off-chip for performance and cost savings. The protection of the RF output circuitry was realized using a shunt protective diode and the capacitance of the loading diode is incorporated as a part of the output match. A simplified functional schematic of the protected amplifier with the surrounding circuit board components is shown in Fig.3.

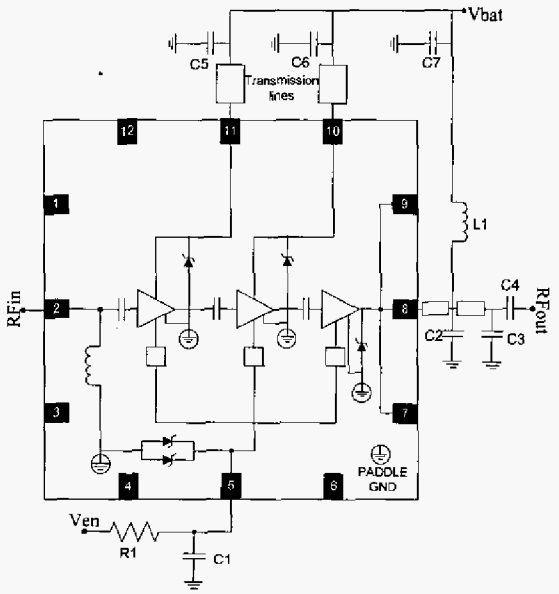

Fig. 3. Functional schematic of the fully ESD protected PA

Table. II presents a comparison of the large signal simulations for the fully protected PA with and without ESD protection. As can be seen, the PA performance is virtually unaffected by the addition of the ESD protection circuitry.

TABLE II
LARGE SIGNAL SIMULATION COMPARISON

	Without ESD	With ESD
Gain (dB)	27.511	27.805
Pout (dBm) (at Pin = -2dBm)	25.511	25.805
PAE (%)	43.137	42.820
Return Loss	0.041	0.017
Current (mA)	343	370
Harmonics 2^{nd}, 3^{rd}(dBc)	-52.9, -62.2	-55.4, -67.8

Fig.4 shows the large signal, small signal and transient simulation results for the fully protected PA. The PA's performance is largely unaffected. It also shows the circuit's response to +1.5kV and –4kV HBM pulses (with respect to the package PADDLE). For a positive ESD strike on 'V_{en}' pin, the voltage rises to a maximum of 11V for a few nanoseconds. For a similar ESD strike on 'V_{en}' and 'RF_{in}' pins, the protection structure limits the voltage to a lower value. The final settling voltages in the cases of 'V_{en}' and 'V_{cc}' strikes are around 7V, which is the reverse breakdown voltage of the Zener. As mentioned earlier, the simulations show that even for a –4kV HBM strike, the voltage overshoot is limited to a lower value for strikes on 'RF_{out}', 'V_{en}' and 'V_{cc}'. The surge on RF_{in} is slightly higher than on the other pins but this lasts only for a very short period of time.

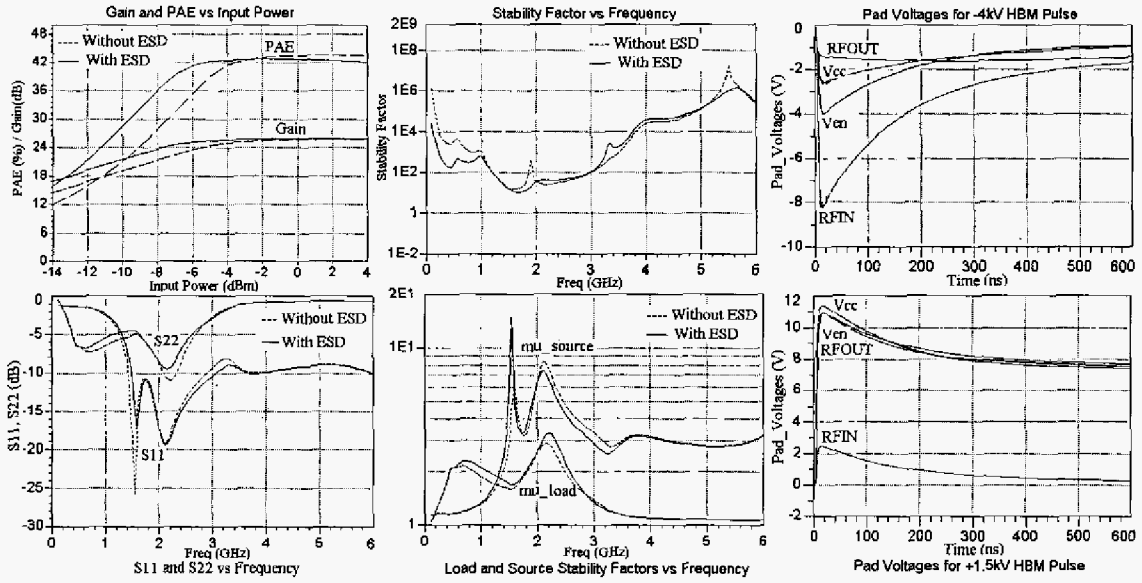

Fig. 4. Large signal, Small signal and Transient simulation results for the fully protected PA design

IV. LAYOUT AND MEASUREMENT

Measurements were performed on a prototype partially protected power amplifier. The design has two separate 'V_{en}' pins. Only the 'RF_{in}', 'V_{en1}' and 'V_{en2}' pins of this PA were protected. RF_{in} was protected using L-C tank approach [5]. In this case, the inductor was not used as a part of the input-matching network unlike the fully protected PA. Rather, it was used to tune out the parasitic capacitance present at the input, minimizing the impact of the L-C tank on the RF performance. An external capacitor was included to obtain a reasonable value of inductance (1.6 nH). The 'V_{en}' pins were protected using string of diodes (five forward biased and one reverse biased). The traditional multiple diodes approach was used to prevent zapping under normal operating conditions. The diode string was used instead of the Zener diode approach so as to make the device indifferent to positive and negative ESD strikes.

The SiGe HBT PA chip had a die area of 1.15mm x 0.75mm. A picture of the ESD circuitry portion of the amplifier is shown in Fig.5.

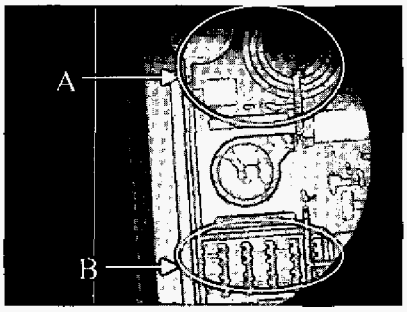

Fig. 5. (A) RF input and (B) control line protection circuitry

Measured Gain and P_{out} of the prototype PA design are shown in Fig.6. There is a slight degradation in the gain and compression point of the PA due to the addition of the L-C tank and diode string. This degradation has been corrected in the fully protected PA design (See Fig 4).

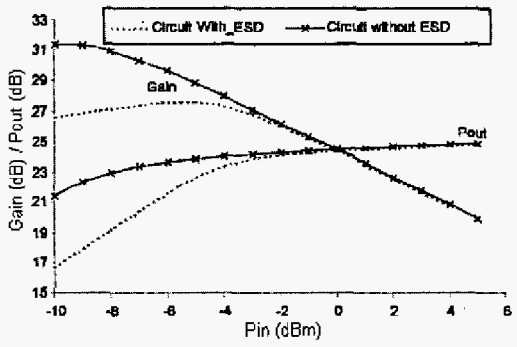

Fig. 6. Measured Gain and Pout Comparison

The partially protected PA was tested up to ±1kV HBM pulses. The pre/post ESD RF performance results are shown in Fig.7 for a number of sample circuits. The results show no degradation in RF output power after the ±1kV ESD pulse testing.

IV. CONCLUSION AND FUTURE WORK

This paper presents the design of a high performance SiGe HBT RFIC Amplifier with ESD protection. The PA's design incorporates ESD protection schemes, which are capable of protecting the PA from –4kV to +1.5kV HBM pulses. This demonstrates that excellent RF PA performance can be maintained while at the same time providing more than 1kV ESD protection. . Additional measurements are on going and will be incorporated in the final paper. The fully protected SiGe HBT PA design is planned for fabrication in the near future.

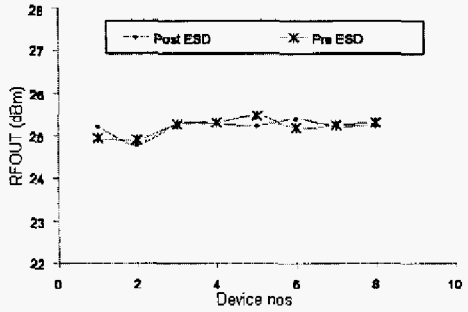

Fig.7. Measured RF performance pre/post ±1kV HBM pulsing

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