A 900MHz GSM PA in 250nm CMOS with Breakdown Voltage Protection and Programmable Conduction Angle*

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Abstract—**A three-stage 900MHz GSM power amplifier implemented in 2mm^2 in 250nm CMOS outputs 2W and 1.5W with 30 and 43% drain and power-added efficiencies with 3.0 and 2.5V power supply voltages, respectively. A cross-coupled self-biased cascode configuration reduces maximum voltage stress in the class-E driver stage to 1.6V_{DD} without the use of additional bias voltages. A programmable conduction angle technique is also introduced and demonstrated.**

Index Terms—**Power amplifier, class-E power amplifier, programmable conduction angle, GSM.**

I. Introduction

CMOS is an attractive technology for system-on-chip solutions for wireless devices. Consequently, many front-end RF circuits with impressive performance have been successfully designed and fabricated using deep sub-micron CMOS devices. Although short-channel devices are efficient in high-frequency small-signal applications, their use in large-signal monolithic power amplifiers (PA) requiring high output power and efficiency along with immunity to breakdown voltage and hot electron effects is problematic. Also, concepts for digitally programming the conduction angle of a PA for optimum performance have not been reported.

There are two basic PA types determined by the digital modulation method employed: linear (class-A, class-C, etc.) and non-linear (class-D, class-E, etc.). While high data rates are obtained using digital modulation standards such as QAM, PSK, etc., the required linear PA generally exhibits low drain and power-added efficiency values. Conversely, a high efficiency PA is achievable using non-linear modulation techniques such as GMSK, MSK, etc., at the expense of lower data rates. The GSM standard uses GMSK modulation.

The basic class-E non-linear power amplifier concept was introduced by Sokal and Sokal in 1975 [1]. It uses a passive LC filter to achieve high efficiency by reducing the power consuming overlap times between the drain current and voltage waveforms. Hence, a compelling feature of the class-E PA approach is its theoretical 100% drain efficiency. In terms of the continued voltage scaling outlined in the *International Technology Roadmap for Semiconductors*, however, a potential roadblock looms ahead; namely, the maximum drain voltage in the conventional class-E PA (~3.3V_{DD}) portends breakdown voltage and hot electron long-term reliability problems. New solutions to these problems are proposed in this paper and applied to a class-E PA for GSM applications.

Gate oxide rupture and drain-substrate junction breakdown are potential failure mechanisms in CMOS. In fact, in sub-micron short-channel devices, gate oxide breakdown and hot electron effects are critical because they generally occur at lower voltages than junction breakdown; moreover, they are not reversible. The ubiquitous cascode configuration (Fig. 1) alleviates these problems. However, since the maximum output voltage in a conventional class-E stage is ~3.3V_{DD}, a cascode device with its gate biased at V_{DD} sees a maximum V_{DG} of ~2.3V_{DD}. Yoo and Huang [2] use a cascode biased at ~1.4V_{DD} to reduce the maximum V_{DG} to ~1.9V_{DD}.

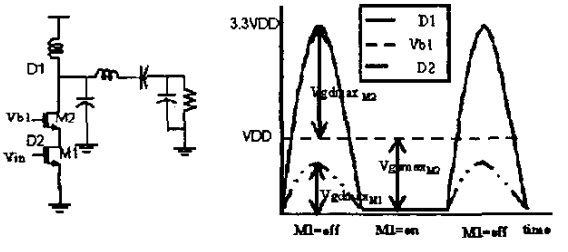

Fig. 1. Conventional class-E power amplifier and associated drain-gate voltage waveforms. $V_{b1} = V_{DD}$.

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Fully integrated power amplifiers with high efficiency and output power levels are desirable, and to assure long-term reliability in high-volume manufacturing, circuit techniques that protect against gate oxide breakdown and hot electron effects are required. In Section II, a differential class-E PA topology that addresses these requirements is introduced. Measurement results from a prototype in 250nm CMOS are presented in Section III and conclusions are given in Section IV.

II. Differential Class-E PA Topology

The differential three-stage PA of Fig. 2 protects against oxide breakdown and hot electron effects without requiring additional package pins or bias voltages.

The first stage is fixed class-B, the second is digitally programmable class-B, and the third is the fully differential class-E topology. Its gate oxide breakdown and hot electron protection techniques are described in Section II.1, and the digitally programmable conduction angle method is introduced in Section II.2.

II.1. Gate Oxide Breakdown Protection Technique

Figure 3 shows the fully differential class-E third stage and its critical voltage waveforms. The self-biasing concept of Sowlati and Leenaerts [3] is applied using the parasitic capacitance at node X and resistors R1 and R2 to create low pass transfer functions. Consequently, the maximum V_{DG} is reduced to ~$1.6V_{DD}$ for all devices. However, when switching device M1 is ON, the gate drive of cascode device M2 is reduced. Hence, drain efficiency is reduced due to the increased series resistance. The overall ON resistance of the cascode is reduced paralleling M3 with increased gate drive in a modification of the cross-coupled configuration of Tsai and Gray [4]. Stability of the positive feedback loop is assured since the loop gain is less than one. Hence, the class-E stage allows a high output voltage without excessive device stresses.

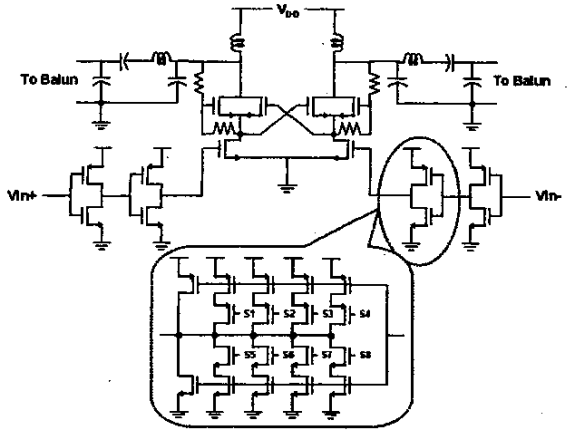

Fig. 2. Three-stage PA with gate oxide breakdown, hot electron protection, and programmable conduction angle.

II.2. Digitally Programmable Conduction Angle

Figure 4 shows the conventional analog and proposed digital methods of controlling the conduction angle of a PA. Traditionally, a dc bias voltage is coupled into the driver stage to set the conduction angle as shown Fig. 4 (top). In the standard approach, however, large dc blocking capacitors C_B are required between stages to minimize signal losses associated with the large C_{gs} capacitances of the very wide NMOS switching devices. The technique introduced in Fig. 4 (bottom) eliminates the need for dc blocking capacitors, and enables digital programming of the conduction angle of the PA as desired in nascent reconfigurable RF system-on-chip solutions. The first stage of the three-stage PA is a fixed class-B stage, and the second is a programmable class-B stage. The programming concept is based on the fact that as the effective ratio of PMOS to NMOS device strengths is changed under digital control, the duty cycle of the square switching waveform driving the third stage is varied. Consequently, the dc value of the driving waveform is changed so that the conduction angle is also controlled as shown.

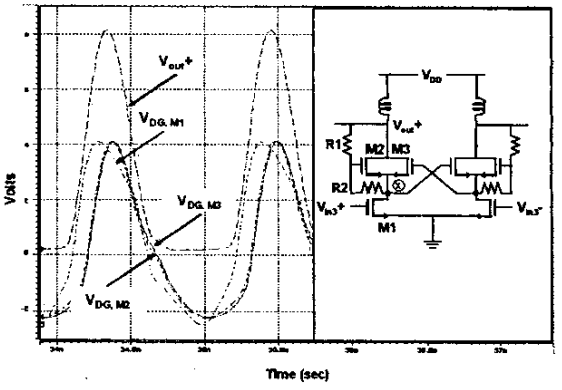

Fig. 3. Fully differential class-E PA stage with gate oxide breakdown, hot electron protection circuitry, and waveforms of the critical drain-to-gate voltages.

The method described above for programming the conduction angle has several advantages. First, it eliminates the requirement for large coupling capacitors, which saves considerable on-chip area. Second, it is a reliable solution for the driver stage transistors in terms of breakdown voltage limitations. If conventional class-B amplifiers with inductor loads are used as the driver stages, the maximum drain voltage is 2 times V_{DD}, which may cause transistor voltage breakdown problems. However, the breakdown voltage concern is eliminated in the proposed method wherein the maximum output voltage is limited to V_{DD}.

The theoretical limit on the variation of the conduction angle (θ) of the circuit is

$$\theta(\text{deg}) = \frac{V_{DD} - 2V_t}{V_{DD}} \cdot 360 \qquad (1)$$

For example, with V_{DD} = 2.5V and V_t = 0.4V, the maximum conduction angle range is ~230° (65°-295°). Since the intent was proof of concept only, the conduction angle in this design was designed to vary only about 20°. This digitally programmable RF PA presents an interesting alternative for optimizing PA performance for non-linear and possibly linear PA designs.

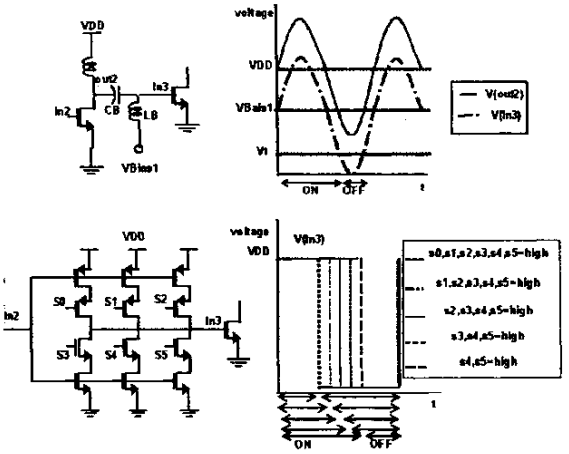

Fig. 4. Conventional method using a dc bias voltage for changing the conduction angle of a PA. The digitally programmable conduction angle concept and variable duty cycle waveforms (bottom).

III. Measurement Results

Prototype three-stage PA circuits have been fabricated in a 250nm CMOS process. Figure 5 shows a packaged die and associated bond wires. High-Q bond wires are used for the critical inductors; note that the bond wire lengths are adjusted slightly by modifying the location of the chip on the package header. To handle the high output power levels, several bond wires are connected in parallel to the outputs.

The measured output power and drain efficiency (η) with an input power of 10dBm versus V_{DD} is displayed in Fig. 6. With V_{DD} = 2.5V, Pout = 1.45W, η = 43%, and PAE = 43%, and with V_{DD} = 3.0V, Pout = 2.0W, η = 30%, and PAE = 30%.

Figure 7 displays the measured output power and drain efficiency vs. frequency. At 900MHz, output power is maximum (32 dBm) with a drain efficiency of 45% using a single 2.5V power supply.

Figure 8 shows measured output power and drain efficiency (η) with an input power of 10dBm and V_{DD} = 2.2V versus programmed conduction angles for 7 digital codes. The overall conduction angle variation in this proof-of-concept implementation is ~20°.

Figure 9 shows the measured GSM spectral emission mask (in dBc) at an output power level of 1.3W obtained using a resolution bandwidth of 30kHz with BT=0.3. The output spectrum exceeds the GSMK spectral emission mask requirements. An amplified GMSK modulated signal with BT = 0.3 was used for the test.

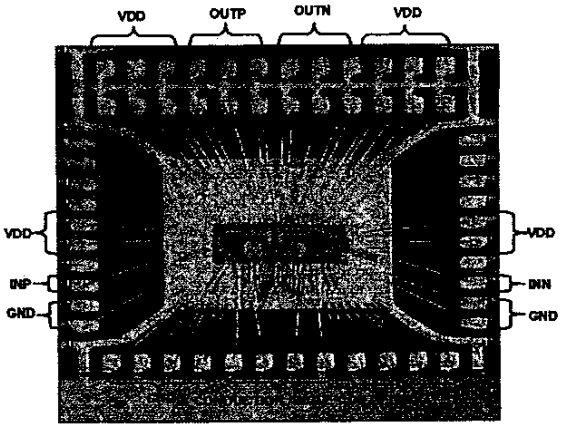

Fig. 5. Die photo of the power amplifier with bond wire inductors and package. Die area is 2mm^2 in 250nm CMOS.

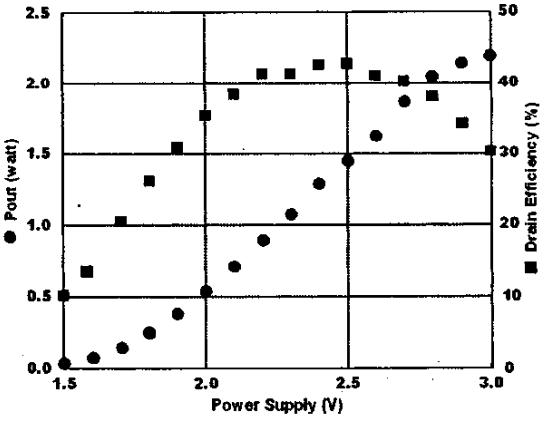

Fig. 6. Output power and drain efficiency vs. power supply voltage. Input power = 10dBm.

IV. Conclusions

To overcome reliability concerns relating to CMOS RF power amplifiers such as breakdown voltage and hot

electron limitations, several RF CMOS power amplifier design techniques are proposed, and validated with fabricated and tested chip results. A digitally programmable conduction angle circuit is also described and demonstrated. The power amplifier topology is attractive for reducing the high voltage stresses on CMOS devices as well as improving the performance of the PA.

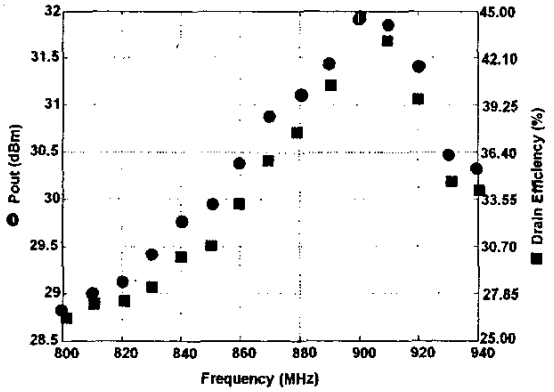

Fig. 7. Output power and drain efficiency vs. frequency.

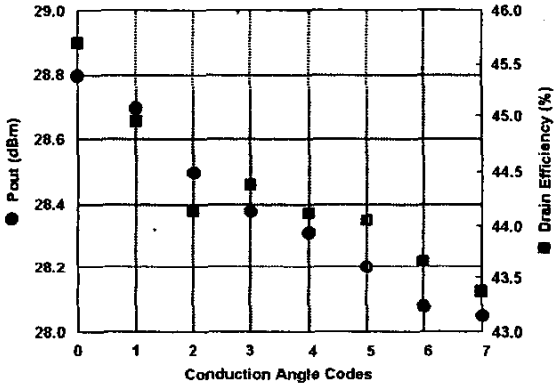

Fig. 8. Measured output power and drain efficiency vs. conduction angle variations (~20°).

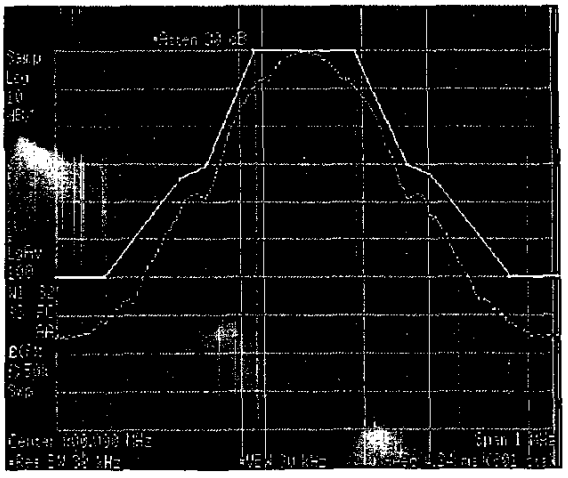

Fig. 9. Amplified GMSK modulated signal (BT = 0.3) and measured GSM spectral emissions relative to the specified limits.

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