1-W, High-Gain, High-Efficiency, and Compact Sub-GHz Linear Power Amplifier Employing a 1:1 Transformer Balun in 180-nm CMOS

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***Abstract*— This letter presents a fully integrated two-stage monolithic microwave integrated circuit (MMIC) power amplifier (PA) with a 1:1 transformer balun in Taiwan Semiconductor Manufacturing Company (TSMC) 180-nm CMOS process. To optimize the performance of PA, an on-chip 1:1 turn spiral transformer balun (STB) was used with a high supply power through the cascode topology. The proposed PA achieved a 40–43-dB gain and a saturation power (P_{sat}) of 29.9–30.3 dBm with a 40%–45% of power-added efficiency (PAE) in the frequency range of 820–1000 MHz. Using the antiphase biasing technique, the PA achieves a linear output power of 25 dBm with 29.5% PAE in 20-MHz spacing two-tone measurement, which satisfies $IMD_3 < -25$ dBc. The measured 1-dB compression point was 28.1 dBm. Furthermore, the proposed PA occupied a core area of 3.3 × 0.86 mm^2.**

***Index Terms*— Antiphase technique, cascode, distributed active transformer (DAT), monolithic microwave integrated circuit (MMIC), power amplifier (PA), spiral transformer balun (STB).**

I. Introduction

TO DATE, the reported watt-level subgigahertz CMOS power amplifiers (PAs) use distributed active transformers (DATs) for their output matching network, which enable simultaneous impedance matching and power combining with a reduced power loss [1]–[4]. However, DATs exhibit several problems; they occupy a significant volume, exhibit voltage swing asymmetries due to the crossed input feed line, and have the stability issue due to the poor isolation characteristics between the input feed line and the transformer [4]. In contrast, the on-chip spiral transformer balun (STB) can be constructed in a relatively compact volume and has the balanced voltage swing in differential amplifier. However, as the optimum impedance (R_{opt}) at lower supply voltage has a lower impedance, the multiturn ratio between the primary and secondary loops is required for transforming the output impedance (50 Ω) to R_{opt}, which leads to a disparity of inductance and physical size between the primary and secondary inductors [2], [3]. Therefore, the effective quality factor (Q-factor) of the STB decreases. In previous works, to prevent this problem, a 1:1 or 1:2 turn transformer was used through an nth array power combining [4], [5]. However, such transformers require a complex structure with a lot of via connection to combine nth array transistors pair, which increase the internal resistance significantly. Therefore, a proper approach is required for achieving relatively higher output power and efficiency, while maintaining the preexisting advantages of the STB.

In this letter, we demonstrated a watt-level PA with a 1:1 turn STB in the 180-nm CMOS process. To achieve the relatively better performance in the output transformer, a 1:1 turn STB with the cascode configuration was used with a physically equal coupling line length and an equal inductance.

II. Circuit Design

A. Optimum Impedance and 1:1 STB

To achieve a watt-level output power with a higher efficiency in the PA, the output matching loss should be kept minimal. In the on-chip STB, the output matching losses are generated by the internal resistance and extreme 1:n turn ratio between the primary and secondary loops, eddy and displacement currents in the highly doped silicon substrate, low permeability of the core material, and the magnetic field leakage in planar geometry. Among these factors that increase the output matching loss, the turn ratio, the line length, and the width of the STB can be controlled. From [2] to [5], an optimum turn ratio of the STB was reported for 1:1, which resulted in lowest coupling loss compared with other 1:n turn STBs. However, to use the 1:1 turn STB with optimum performance, a higher $R_{opt} = \mathrm{VDD}^2/2P_{out}$ is required. If a higher voltage is supplied, R_{opt} increases. Consequently, a higher supply voltage supports the use of a 1:1 turn STB for the output matching network. Fig. 1 depicts the equivalent model of the STB and the locus of the proposed 1:1 turn STB with the shunt capacitor at the input and output. In addition, it also provides R_{opt} according to the supply voltage. The 1:1 turn STB with the shunt capacitor helps transform the 50 Ω into the desired impedance on the constant admittance circle. Moreover, the shunt capacitors help adjust the input and output reactance of the STB to the desired value, which further reduces the output matching loss. However, to use a proposed matching network, R_{opt} is required to be located near the constant admittance circle. If R_{opt} is located far from the constant admittance circle due to a lower or higher supply voltage, the consequent higher or lower impedance transformation with the 1:n turn STB would be required, which would increase the loss significantly. Therefore, an appropriate supply voltage helps use the 1:1 turn STB by locating R_{opt} at the desired point. Furthermore, the device has a lower breakdown voltage in the CMOS process,

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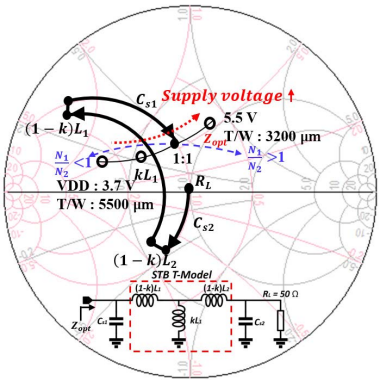
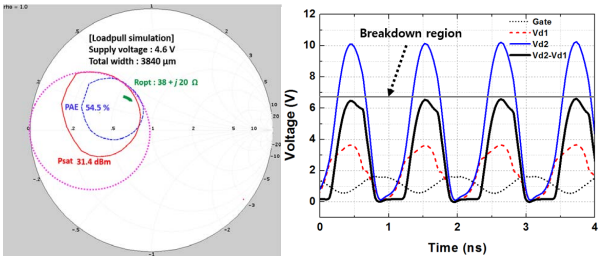


Fig. 1. Matching mechanism with a 1:1 turn STB and Z_{opt} according to the supply voltage (N_1, N_2, and k are the number of turn of the primary loop, number of turn secondary loop, and coupling factor, respectively).



(a) (b)

Fig. 2. (a) Load pull simulation with a supply voltage of 4.6 V and (b) transient simulation at the drain to gate of the cascode topology.

due to which, the cascode or n-stack topology is required to endure the voltage stress of the device. Therefore, according to the obtained supply voltage, an appropriate number of stacked devices could be determined [6].

B. Circuit Implementation

The power cell was implemented with a differential push–pull structure to achieve a higher output power and stability. According to the previous methodology, by adjusting the supply voltage, we can locate R_{opt} located in the intersection of the power contour, power-added efficiency (PAE) contour, and the constant admittance circle. To achieve a watt-level saturation output power (P_{sat}) with a higher PAE, the total width of the power stage was optimized by applying the optimum supply voltage, which was obtained from the load pull simulation. The optimized output impedance, the supply voltage, and the total width of the power stage are $38+j20\ \Omega$, 4.6 V, and 3840 μm, respectively, as shown in Fig. 2(a). According to the simulated supply voltage, the cascode structure was implemented to prevent the breakdown. Fig. 2(b) shows the transient simulation between the drain and the source with a 4.6-V supply voltage. We observed that the supply voltage was increased, and the device breakdown had primarily occurred at the drain and source; therefore, consideration of the voltage stress becomes indispensable. Fig. 3 depicts the full schematic of the proposed two-stage PA. As shown, we used metal stack-up (1-poly 6-metal) for the 180-nm CMOS process. Fig. 4 details a proposed matching network with a shunt capacitor and an electromagnetic (EM) structure of a 1:1 turn ratio STB. Moreover, as shown in Fig. 4(a), L_1, L_2, $C_{\text{out}-1}$, and $C_{\text{out}-2}$ are 3.7, 3.9 nH, 8.5, and 3.8 pF, respectively. Metal–insulator–metal (MIM) capacitor was used for all the capacitors used in these circuits. Fig. 4(b) depicts the EM structure of the 2:2 turn STB. The top metal (M6) of 4.6-μm thickness was

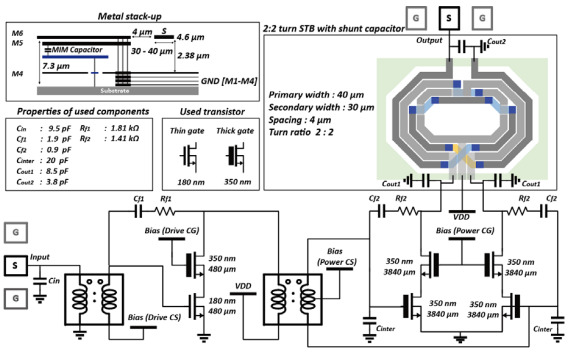
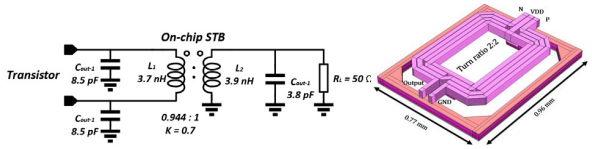
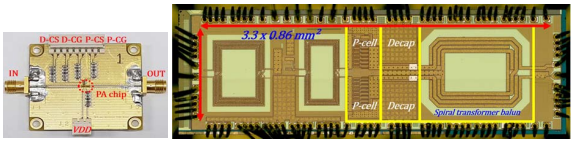


Fig. 3. Schematic and metal stack-up of the proposed PA.



(a) (b)

Fig. 4. (a) Proposed matching network and (b) EM structure of a proposed 1:1 turn STB.



(a) (b)

Fig. 5. (a) Test PCB of the PA chip and (b) microphotograph of the PA chip and wire bond.

used for the signal line, and M1–M4 metals were used for the ground metal. The structure of the STB was carefully optimized to ensure that the design of the 1:1 turn ratio STB provided a relatively higher performance and had a relatively compact volume. As the turn of the STB is a tradeoff between the internal resistance and the coupling length, the STB was optimized with a 2:2 turn. To minimize the internal resistance, the line widths of the primary loop and secondary loops were ensured to be 40 and 30 μm with a spacing of 4 μm, respectively. The inner area and the distance between the signal line and the ground plane are 550×346 μm^2 and 70 μm, respectively. The size of the on-chip transformer balun is 0.96×0.77 mm^2. $\eta = S_{21}^2/(1-S_{11}^2)$ is the ratio of the power delivered to the load across the output matching network. The simulated maximum power transfer efficiency is 76.3%, which is comparable with the DAT efficiency reported in [2]. The drive stage was implemented with a single-ended topology for an increased efficiency. The total width of the drive stage was maintained at 480 μm. The drive stage and the power stage were connected with a 3:2 turn STB between the primary and secondary loops, in addition to a shunt capacitor (C_{inter}) of 20 pF. The input stage was implemented with a 3:4 turn STB between the primary and secondary loops in addition to a shunt capacitor (C_{in}) of 9.5 pF to achieve a wider matching.

III. Measurement Results

Fig. 5 depicts the printed circuit board (PCB) on which the PA chip was tested in addition to a microphotograph of the PA chip and bonding wire. No additional off-chip matching components and drive amplifiers were considered herein. Fig. 6(a) provides the simulated and the measured S-parameters. For supply voltage of 4.6 V, drive stage common source (D-CS): 0.7 V (class A), drive stage common

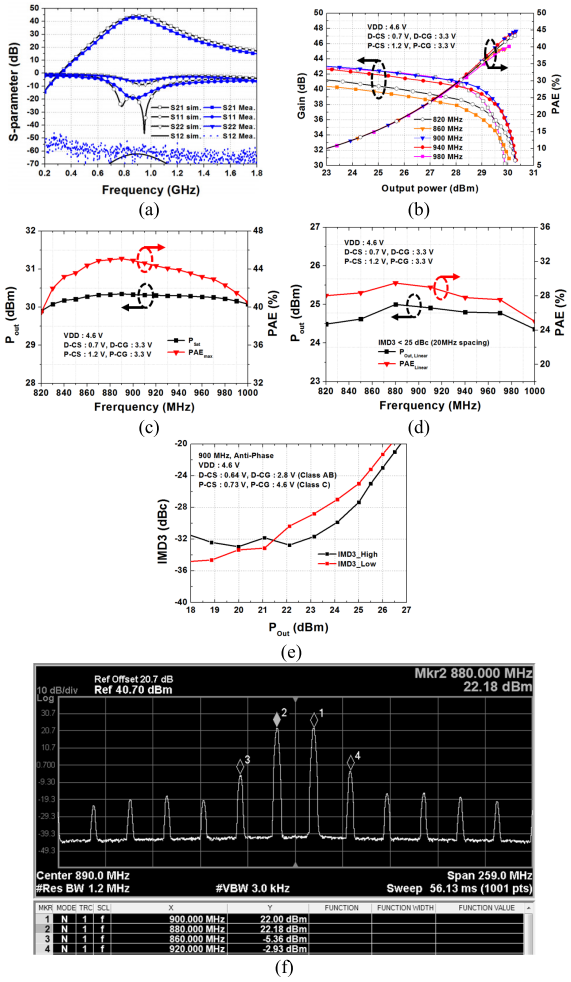


Fig. 6. Measured results: (a) S-parameter, (b) one-tone measurement, (c) P_{sat} and PAE_{max}, (d) P_{linear} and $\text{PAE}_{\text{linear}}$ measured at $\text{IMD}_3 - 25$ dBc, (e) IMD_3, and (f) spectrum of the two-tone measurement with 20-MHz tone spacing.

gate (D-CG): 3.3 V, power stage common source (P-CS): 1.2 V (class AB), and power stage common gate (P-CG): 3.3 V were applied for these measurements. The observed input matching (S_{11}), output matching (S_{22}), and input–output isolation (S_{12}) are < -14.1, -5.2, and -53.7 dB, respectively, in the frequency band of 820–1000 MHz. Moreover, the peak gain was found to be 43 dB at 900 MHz. Fig. 6(b) and (c) shows the one-tone measurement. The measured value of P_{sat} and PAE_{max} is 29.9–30.32 dBm and 39.4%–45.0%, respectively, in the frequency band of 820–1000 MHz. Fig. 6(d)–(f) details the two-tone measurement result with 20-MHz tone spacing. To optimize the linear performance, the antiphase biasing technique was used [7]. For a supply voltage of 4.6 V, D-CS: 0.64 V (class AB), D-CG: 3.3 V, P-CS: 0.74 V (class C), and P-CG: 4.6 V were applied for the two-tone measurement. The linear output power (P_{linear}) and linear efficiency ($\text{PAE}_{\text{linear}}$) were measured with satisfying IMD_3 and $\text{IMD}_5 < -25$ dB. The measured P_{linear} and $\text{PAE}_{\text{linear}}$ are >24.3–25 dBm and 24.5%–29.5% shown in Fig. 6(d), respectively. The measured P_{sat} and PAE_{max} were 29.1 dBm and 41.6% at 900 MHz, respectively. The measured 1-dB compression point (P1dB) was 28.1 dBm. Fig. 6(e) and (f) shows the measured IMD_3 and output spectrum at 900 MHz, respectively. Table I provides a comparison between the reported watt-level subgigahertz state-of-the-art PAs. It can be seen that the proposed PA

TABLE I

PERFORMANCE COMPARISON OF STATE OF ARTS

	This work		[1]	[3]	[8]	[9]
Frequency [MHz]	820 - 1000		920	900	930	700-1000
Class	AB	AB	AB	A	AB	AB
Type of output matching network	On-chip STB		DAT	DAT	DAT	On-chip
Power gain	43	32.4	16.8	12	28	27-29
P_{sat} [dBm]	30.3	29.1	28	29.5	29.4	32
PAE_{max} [%]	45	41.4	32	34.5	25.8	35-38
P_{linear} [dBm]		25	NR	NR	25.1	23-25
PAE_{linear} [%]		29.5	NR	NR	15	NR
Supply [V]		4.6	1.8	3.6	2	5
FOM	89	77	59	56	71	75
Core size [mm^2]	2.66		3.3	3.3	3.3	64
Technology	180nm CMOS		90nm CMOS	90nm CMOS	90nm CMOS	GaAs HBT

NR : Not Reported

achieved the highest values for gain, PAE_{max}, and $\text{PAE}_{\text{linear}}$. The figure of merit (FOM) calculation is as follows:

$$\text{FOM} = P_{\text{sat}}\,[\text{dBm}] + \text{Gain}\,[\text{dB}] + 20\log(f_c\,[\text{GHz}]) + 10\log(\text{PAE}_{\text{max}}\,[\%]). \quad (1)$$

The proposed PA achieved the highest FOM among the reported subgigahertz CMOS PAs [1], [3], [8], [9]. Furthermore, the core size (3.309×0.866 mm^2) of the proposed PA was observed to be the smallest among the reported PAs.

IV. CONCLUSION

The fully integrated two-stage PA with a 1:1 turn STB was demonstrated using the 180-nm CMOS technology. The on-chip 1:1 turn STB with high performance and a significantly compacted size was used with the cascode topology. The proposed PA exhibited a performance of 1 W P_{sat} at a bandwidth of 820–1000 MHz, with over 45% PAE_{max} and a gain of 43 dB. The measured values of P_{sat}, PAE, and gain were the highest when compared with those obtained for the reported fully integrated CMOS subgigahertz linear PAs.

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