A 28 GHz Single-Input Linear Chireix (SILC) Power Amplifier in 130 nm SiGe Technology

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***Abstract*— This article presents an integrated high-efficiency 28 GHz power amplifier (PA) employing a combination of Chireix outphasing and Doherty architectures in order to simultaneously achieve power back-off efficiency and linearity with a single RF input signal and no predistortion. The amplifier consists of a dual-input high-efficiency outphasing PA and a simple input network which serves as a power splitter and feeds the same signal to the inputs of the main and auxiliary PA cells that are biased in class-AB and class-C regions, respectively, similar to the Doherty architecture. The operation of the PA cells together with the Chireix combiner result in back-off efficiency enhancement plus systematic AM-AM and AM-PM variations which are used to correct the distortions caused by transistors, resulting in a linear response. The implemented PA demonstrates 19 dBm saturation power (Psat) with 34.4% peak power-added efficiency (PAE) and 6 dB back-off PAE of >23% at 27.5 GHz. The modulated signal performance using a 100 MHz 64QAM OFDM signal shows an average output power of 11.9 dBm with PAE >20%, EVM <5%, and ACLR < −33 dBc without using predistortion.**

***Index Terms*— 5G mobile communication, BiCMOS integrated circuits, millimeter wave (mm-wave) integrated circuits, power amplifiers (PAs).**

I. Introduction

THE low distortion levels required for spectrally efficient complex modern communication signals with high peak-to-average power ratio (PAPR) put strict requirements on the linearity of wireless transmitters. The average efficiency, mostly determined by the power amplifier (PA) performance at peak and back-off power levels, is another significant criterion, particularly for battery-powered devices. For emerging 5G applications employing mm-wave phased arrays with multiple PA units on the same die, the importance of linearity and efficiency escalate further, since implementing individual digital predistortion (DPD) for each unit is not practical and heating of the PAs, densely placed next to each other, can be a problem. Therefore, the PA units must be inherently linear and efficient.

Chireix outphasing [1] and Doherty [2], the two popular active load modulation techniques used at RF frequencies for PA efficiency enhancement, are currently being investigated for mm-wave applications. Both methods, in their original forms, utilize two PA cells connected to a nonisolating three-port passive network, which serves as a power combiner and provides the desired load modulation during operation.

In theory, outphasing offers a better efficiency profile than Doherty [3], and in practice, there are a variety of creative ways to implement the Chireix combiner with low loss (e.g., two-element L-C [4], offset transmission lines [5], on-antenna outphasing [6], [7], and triaxial balun [8]). Also, contrary to most Doherty implementations, the PA cells in outphasing have the same size, are biased similarly, and see the same magnitude of fundamental load modulation. These features make the dual-input implementations of outphasing [8] more advantageous than the dual-input implementations of Doherty (with analog [9], [10] or digitally assisted mixed-signal [11] PAs) in that the two inputs for outphasing are symmetric (they have the same amplitude with opposite phases, i.e., complex conjugate in baseband signal domain).

On the other hand, a major advantage of the Doherty architecture, which has historically made it a more common choice than outphasing, is the simplicity of implementing its input signal splitter that feeds the two PA cells from a single RF input source, without the need for an extra IQ modulator and the bandwidth expansion problem associated with dual-input realizations.

In recent years, there have been successful proposals for novel architectures within the Doherty-outphasing continuum, in order to garner the best advantages of both methods in one circuit [12], [13]. The primary emphasis in these works has been placed on efficiency improvement for single RF input amplifiers, leaving the linearity to be addressed with DPD. This article presents a method that not only improves the back-off efficiency while requiring a single RF input but also corrects the nonlinearity of the PA cells, eliminating the need for predistortion. It relies on the use of the Chireix combiner and is termed here the single-input linear Chireix (SILC) PA. In the following, the design principles of the SILC PA are first discussed, and an experimental implementation with SiGe HBTs is then described. The measurement results with a 64QAM OFDM signal appropriate for 5G applications are reported, showing an average output power of 11.9 dBm and power-added efficiency (PAE) >20%, which to the authors' best knowledge is among the highest PAE reported to date for an OFDM signal without DPD (or other forms of digital enhancement) at power levels of interest for 5G transmitters.

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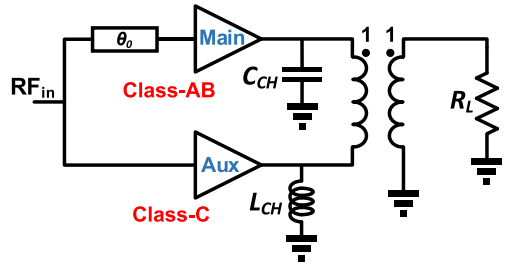

Fig. 1. Proposed PA architecture with the main and auxiliary PA cells biased in class-AB and class-C, respectively.

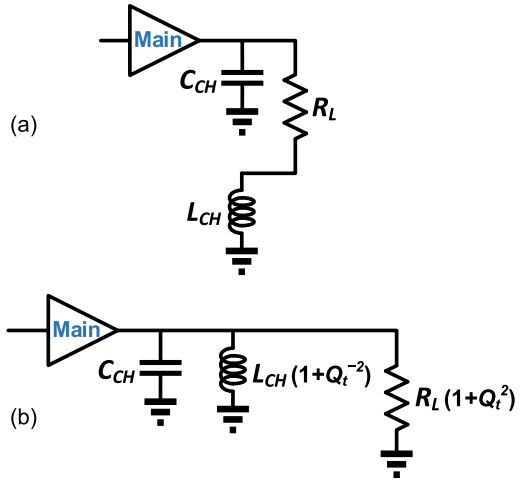

Fig. 2. Equivalent circuit at low power when the auxiliary amplifier is off. (a) R_L moved to the primary side of the transformer and (b) series-to-parallel impedance transformation applied.

II. Proposed Architecture

A. Schematic

Fig. 1 shows the proposed topology that consists of a standard Chireix PA with Doherty-like biases and a simple input network providing a constant phase shift (θ_0) to the main path. Depending on the type of the Chireix combiner and characteristics of the PA cells, the delay line can be placed at the input of either amplifier for proper operation. Here, the unit PA cells are regarded as current sources, and the shunt compensating elements with susceptances of $\pm B_{CH}$ (C_{CH} and L_{CH}) are chosen in accordance with outphasing principles [14].

Analysis of the circuit is carried out by splitting the operation into low-power and high-power regions.

B. Low-Power Region

At low input power levels, the auxiliary amplifier is off, and the main amplifier works as a standalone class-AB PA. The equivalent circuit for this mode of operation is depicted in Fig. 2(a).

The load impedance seen by the main PA at low power (Z_A) can be calculated by performing a series-to-parallel impedance transformation, as shown in Fig. 2(b). The quality factor of this transformation (Q_t) is equal to inverse of $B_{CH}R_L$, which is a design parameter for Chireix combiners determining the back-off efficiency profile of the outphasing PAs. For example, $B_{CH}R_L$ equal to 0.6 and 0.86 result in back-off peak efficiency points at 10 dB and 6 dB, respectively, and therefore, Q_t is typically a value in the 1.16–1.66 range. Additionally, C_{CH} is tuned out, although not completely, by the resulting parallel inductance, keeping the reactive part of the load impedance low for high efficiency. The residual capacitance, $C_{CH}/(1+Q_t^2)$, causes modest efficiency and gain reduction due to a nonunity power factor (PF_A) ranging between 0.75 and 0.85. Equation (1) shows the relation between the PF_A and Q_t:

$$PF_A = \frac{\text{real}\{Y_A\}}{|Y_A|} = \frac{\frac{1}{R_L(1+Q_t^2)}}{\sqrt{\left(\frac{1}{R_L(1+Q_t^2)}\right)^2 + \left(\frac{B_{CH}}{1+Q_t^2}\right)^2}} = \frac{1}{\sqrt{1+(B_{CH}R_L)^2}} = \frac{Q_t}{\sqrt{1+Q_t^2}}. \quad (1)$$

One can design a modified Chireix combiner to avoid any excess reactance [13]; however, the degraded symmetry of the circuit is not desirable for the high-power mode of operation described below.

The PA should be designed such that the auxiliary amplifier remains off up to the input power where the main amplifier starts saturating and exhibits nonlinear behaviors including gain compression and AM-PM distortion. In principle, the efficiency should reach its maximum class-AB value scaled by PF_A (0.75 − 0.85), and the gain should be lower than the class-AB gain by $PF_A/2$ (3.7 − 4.25 dB). The extra 1/2 for the gain ratio is due to the fact that in this mode of operation, the input power going to the auxiliary amplifier is wasted.

C. High-Power Region

As the auxiliary amplifier turns on and begins providing power, a variety of mechanisms influence the output, of which some are due to the topology itself (i.e., load modulation, systematic AM-AM and AM-PM variations), some are due to the device nonidealities (i.e., gain compression and AM-PM distortion), and some result from combination of both topology and device nonidealities (i.e., self-outphasing), as discussed below.

The endpoint of this region, where the PA provides its highest output power, is considered first. Both amplifiers work with their full power at this point, with a constant phase shift (θ) between them, resulting from the delay line at the input network (θ_0), as well as phase imbalance (θ_I) coming from the nonequal input impedances of the PA cells due to their bias difference ($\theta = \theta_0 + \theta_I$). If a standard combiner is used, this operation point can be designed to lie in a high-efficiency area (PF = 1) of the impedance trajectories provided by the Chireix method [5] shown in the Smith chart of Fig. 3. There are two candidates for this point, one close to the center of the Smith chart with a lower impedance value associated with higher output power and the other one at "outphasing back-off," providing higher load impedance appropriate for low-power operation. The design parameter that determines the impedance of choice is the phase shift θ between the two amplifiers.

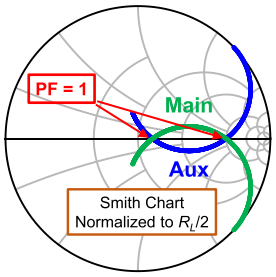

Fig. 3. Impedance trajectories provided by the Chireix combiner in standard outphasing operation. The high-efficiency points with unity PF are marked.

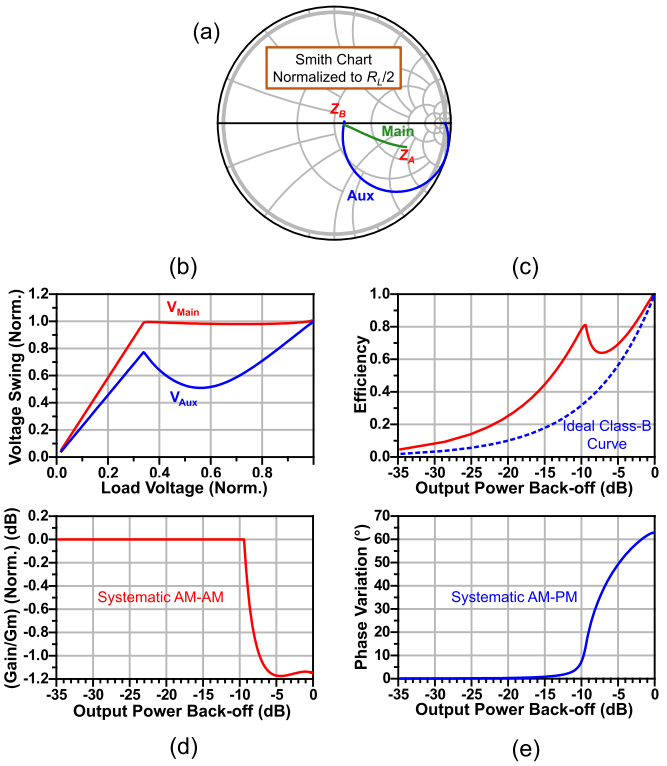

Fig. 4. Simulation of an example design with a low, purely resistive impedance at peak power, using the idealized transistor model (a VCCS with knee voltage). (a) Impedance trajectories seen by the amplifiers, (b) output voltage magnitudes of the amplifiers normalized to the main supply voltage, (c) normalized overall efficiency, (d) systematic AM-AM, and (e) systematic AM-PM.

Note that for standard outphasing operation, equal fundamental voltage amplitudes are required at the ports of the Chireix combiner. This approach is also followed here at full power; since the auxiliary amplifier is biased in class-C and has lower gain, it is set to have a higher supply voltage than the main amplifier in order to match the voltage swings at maximum power.

To further investigate the different possible design approaches, simulations with an idealized transistor model (voltage-controlled current source (VCCS) with knee voltage, described in Appendix A) and an ideal balun have been done. Fig. 4(a) shows the impedance trajectories seen by the main and auxiliary amplifiers for an example design, where the endpoint impedance at maximum power is chosen to be the lower value of the two options mentioned above. With $B_{CH}R_L$ of 0.8 ($Q_t = 1.25$), the fixed phase shift between the amplifiers is calculated accordingly based on the standard Chireix equations [5] ($\theta = \sin^{-1} B_{CH}R_L = \sin^{-1} Q_t^{-1} = 126.9°$). Theory predicts that the trajectory of impedance seen by the main amplifier starts at

$$Z_A = \left[R_L(1+Q_t^2)\right] \| \left[\frac{1+Q_t^2}{jB_{CH}}\right] = R_L\left(Q_t^2 - jQ_t\right) \quad (2)$$

and ends at

$$Z_B = R_L Q_t^2\left(1-\sqrt{1-Q_t^{-2}}\right) = \frac{R_L}{2\cos^2\frac{\theta}{2}}. \quad (3)$$

These values are supported by the simulation results shown in Fig. 4(a). The output power variation due to load modulation ratio (LMR) for the main amplifier is

$$LMR_{Main} = \frac{\text{Real}\left\{\frac{1}{Z_B}\right\}}{\text{Real}\left\{\frac{1}{Z_A}\right\}} = \left(1+Q_t^2\right)\left(1+\sqrt{1-Q_t^{-2}}\right) \quad (4)$$

which corresponds to 4.1 (6.1 dB) in this design. For the overall output power, the contribution of the auxiliary amplifier is then taken into account, by doubling the value for the main amplifier (adding 3 dB), since at the maximum power both amplifiers see the same impedance [Fig. 4(a)] and have the same output voltage swing [Fig. 4(b)]. The back-off peak efficiency is, therefore, expected to be at a power level 9.1 dB below the maximum power with a value reduced by PF_A (0.78) relative to the peak efficiency. These numbers are in good agreement with the simulations shown in Fig. 4(c). The slight difference between the theory and simulation is due to the presence of knee voltage and saturation of the PA cells. Note that in Fig. 4(a), the impedance seen by the auxiliary amplifier goes outside of the Smith chart for a small region at the beginning of its operation. This condition is not an indicator of instability; it only shows that a small portion of the power generated by the main amplifier is consumed by the auxiliary amplifier.

These results are favorable in terms of efficiency, but the linearity aspects of the PA need to be addressed as well in order to achieve a design that does not require DPD. The goal is to have systematic AM-AM and AM-PM changes that are in the opposite direction of the gain compression and AM-PM variation caused by the device nonidealities, so that the overall response is distortion free. For an overdriven amplifier, the gain compression characteristics and resultant AM-AM distortion are in general dependent on the choice of power transistor (SiGe HBT, CMOS, LDMOS, and pHEMT) and bias conditions. The corresponding AM-PM distortion, associated with the change of device input and output capacitance as well as the impedance matchings, is often a critical determinant of the overall amplifier linearity in this regime.

D. Systematic AM-AM and AM-PM Variations

The net amount of systematic AM-AM results from two features. The first one is the $PF_A/2$ ratio that was mentioned above. Contrary to the low-power mode of operation, at high-power, the PF rises to unity and the input power going

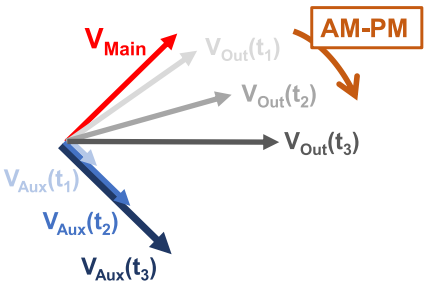

Fig. 5. Simplified phasor diagram describing the systematic AM-PM of the load voltage in the high-power mode of operation.

to the auxiliary amplifier is not wasted, therefore the gain increases by $2/PF_A$. The second feature is that the load modulation decreases the gain, if the transconductance (gm) is considered to be constant for the PA cells. This gain variation is captured by looking at the change in the magnitude of impedance seen by the main amplifier ($|Z_A|/|Z_B|$), thus the overall systematic AM-AM can be calculated as shown below:

$$\begin{aligned} \textit{Overall Systematic } AM-AM &= \frac{2}{PF_A}\times\frac{|Z_B|}{|Z_A|} \\ &= 2\times\left(1-\sqrt{1-Q_t^{-2}}\right)=4\sin^2\frac{\theta}{2}. \end{aligned} \tag{5}$$

Equation (5) in this example results in ~ -1 dB, meaning that for a design with low value impedance at peak power, the systematic AM-AM aggravates the device gain compression problem rather than fixing it. In order to capture the systematic AM-AM in simulation, the variation in large signal Gm is de-embedded from overall gain variation, as shown in Fig. 4(d).

Next, the systematic AM-PM and the mechanism that causes it are described by looking at the combiner port voltages. Fig. 5 shows a simplified phasor diagram illustrating the output voltages of the main (V_{Main}) and auxiliary (V_{Aux}) amplifiers as well as the load voltage (V_{Out}). A vector sum (instead of subtraction) is depicted here for the sake of convenience, even though the actual combiner is differential. We use the simplifying assumptions that V_{Main} and the phase difference between the two vectors (θ) stay constant in this region. As V_{Aux} increases, the magnitude and phase of V_{Out} vary simultaneously, and it is clear from the figure that the overall amount of this systematic AM-PM is equal to half of θ, because eventually V_{Aux} approaches the same magnitude as V_{Main}. In practice, the assumptions made here are not accurate, because the main and auxiliary amplifiers see reactive loads in the middle points [Fig. 4(a)]. However, since at the endpoint both of them see a purely resistive impedance, the overall systematic AM-PM change captured by this analysis, as given by (6), remains a very good approximation. A more detailed calculation, which takes into account the differential nature of the combiner and the effects of C_{CH} and L_{CH}, is presented in Appendix B.

$$\begin{aligned} \textit{Overall Systematic } AM-PM &\cong \frac{\text{total input phase shift }(\theta)}{2} \\ &= \frac{\sin^{-1} Q_t^{-1}}{2} \end{aligned} \tag{6}$$

The simulation result shown in Fig. 4(e) verifies this analytical approach. The AM-PM obtained in this example is not particularly favorable for an overall linear amplifier, because the relatively large amount ($\sim$50° over a 5 dB power variation and $\sim$63° in total) is significantly greater than typical device-related phase distortions.

In this example design, it was seen that a remarkable back-off efficiency profile is achievable with a simple outphasing PA topology that has an asymmetric bias and a constant phase shift between the two input RF signals feeding the PA cells. The phase shift was chosen such that the load impedance at maximum power was relatively low, and therefore, the efficiency had a second peak at a deep back-off, but the linearity in terms of AM-AM and AM-PM was not good. As a result, this design can be a strong candidate for applications where predistortion is available. Modifications are needed, however, for applications where inherent linearity is required.

A similar design is now examined that at peak power has the higher impedance

$$Z_B = R_L Q_t^2\left(1+\sqrt{1-Q_t^{-2}}\right)=\frac{R_L}{2\sin^2\frac{\theta}{2}} \tag{7}$$

with unity power factor, achieved by changing the input phase shift to the other answer of the trigonometric equation $\theta = \sin^{-1} Q_t^{-1}$, which is 53.12° (for $B_{CH}R_L = 0.8$). The simulation results, obtained by using the same transistor model, are shown in Fig. 6. Compared to the previous example, here the amount of load modulation for the main amplifier is minor [Fig. 6(a)] and

$$LMR_{Main} = \frac{\text{Real}\left\{\frac{1}{Z_B}\right\}}{\text{Real}\left\{\frac{1}{Z_A}\right\}} = \left(1+Q_t^2\right)\left(1-\sqrt{1-Q_t^{-2}}\right) \tag{8}$$

is only 0.11 dB. Also, the output voltage of the main amplifier continues to increase (deep saturation) even after the auxiliary amplifier turns on [Fig. 6(b)]. The efficiency profile, shown in Fig. 6(c), is not as good as the previous example, but it is still better than an ideal class-B and has a back-off peak at $\sim$4.4 dB, with a value that is lower than the peak efficiency by PF_A (0.78) as found for the previous case. Note that if the efficiency curve was plotted versus absolute power (rather than normalized power), the back-off efficiency peak would be at the exact same output power in both example designs, but the peak power would be different. The systematic AM-AM expression needs to be modified too, since Z_B has increased. The new expression is:

$$\begin{aligned} \textit{Overall Systematic } AM-AM &= \frac{2}{PF_A}\times\frac{|Z_B|}{|Z_A|} \\ &= 2\times\left(1+\sqrt{1-Q_t^{-2}}\right)=4\cos^2\frac{\theta}{2} \end{aligned} \tag{9}$$

that results in $\sim$5 dB [Fig. 6(d)], which can compensate the device-related gain compression coming from the considerable amount of effective Gm reduction due to the deep saturation experienced by the main amplifier. (As it will be discussed later, the deep saturation of the main amplifier can be avoided in a practical design by adjusting the bias condition of the auxiliary amplifier.) The equation for the systematic AM-PM

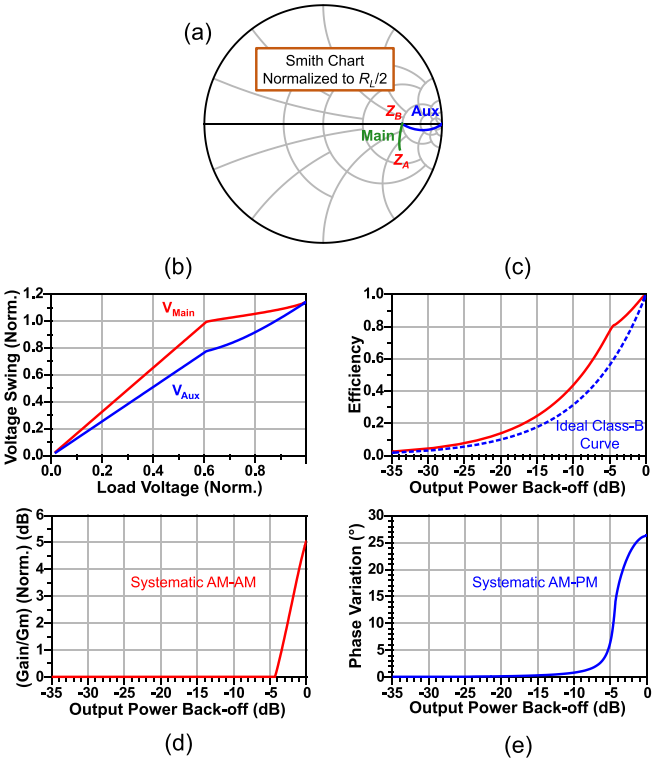

Fig. 6. Simulation of an example design with a high, purely resistive impedance at peak power, using the idealized transistor model (a VCCS with knee voltage). (a) Impedance trajectories seen by the amplifiers, (b) output voltage magnitudes of the amplifiers normalized to the main supply voltage, (c) normalized overall efficiency, (d) systematic AM-AM, and (e) systematic AM-PM.

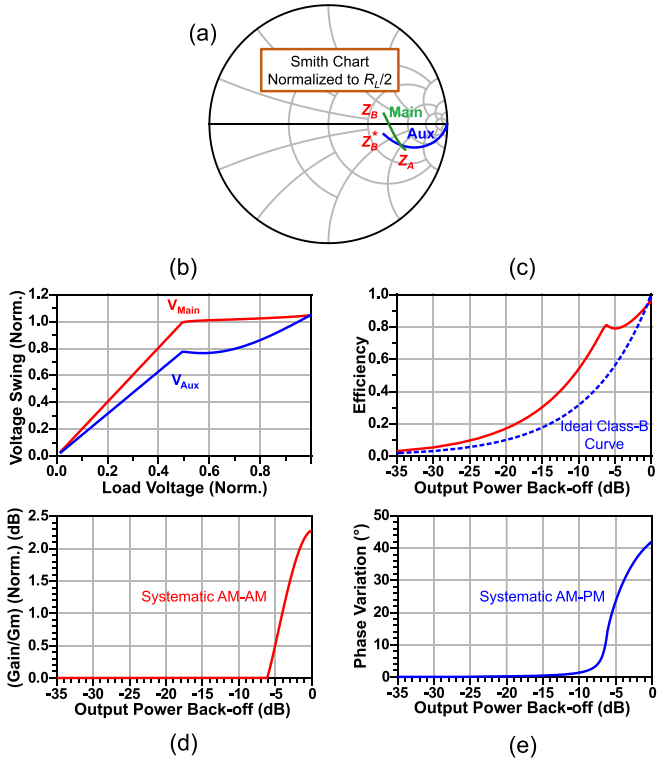

Fig. 7. Simulation of an example design with 90° phase shift at the input, using the idealized transistor model (a VCCS with knee voltage). (a) Impedance trajectories seen by the amplifiers, (b) output voltage magnitudes of the amplifiers normalized to the main supply voltage, (c) normalized overall efficiency, (d) systematic AM-AM, and (e) systematic AM-PM.

is the same as (6) and results in ∼26.6°. The simulation result shown in Fig. 6(e) is in good agreement with the calculation.

It is also possible to have an intermediate design between the two previous examples. As shown in Fig. 3, if a phase shift other than the two values suggested by $\theta = \sin^{-1} Q_t^{-1}$ is applied to the input signals, the peak power impedances seen by the main and auxiliary amplifiers will be complex conjugates of each other and not purely resistive (Z_B and Z_B^*). As a result, the peak efficiency will slightly drop due to the nonunity power factor of Z_B (PF_B), but other than that the PA will work in a manner similar to the previous examples. Fig. 7 shows the simulation results for a case with phase shift of 90° applied at the input. There is an appreciable amount of load modulation for both PA cells [Fig. 7(a)], and the main amplifier is less driven into deep saturation [Fig. 7(b)]. The efficiency peaks at a back-off power of 6.2 dB [Fig. 7(c)], and the overall systematic AM-AM, capture by simulation, is ∼2.2 dB [Fig. 7(d)]. A more general form of the equations can be applied in this case:

$$\begin{aligned} \textit{Overall Systematic AM} - \textit{AM} &= 2 \times \frac{\text{Real}\{Z_B\}}{\text{Real}\{Z_A\}} \\ &= 2 \times \frac{PF_B}{PF_A} \times \frac{|Z_B|}{|Z_A|} \end{aligned} \tag{10}$$

$$LMR_{Main} = \frac{\text{Real}\left\{\frac{1}{Z_B}\right\}}{\text{Real}\left\{\frac{1}{Z_A}\right\}} = \frac{PF_B}{PF_A} \times \frac{|Z_A|}{|Z_B|}. \tag{11}$$

Note that since the PA cells operate in current mode and at the maximum power, they see different reactive loads and experience different amounts of saturation, the actual voltage phase shift at the combiner ports is not 90°, therefore the systematic AM-PM shown in Fig. 7(e) is slightly lower than the expected value of ∼45° suggested by the first line of (6).

The aforementioned behavioral characteristics of this intermediate design are in between those of the two previous ones; therefore by changing the input phase shift, a certain design goal (e.g., a required amount of systematic AM-PM) can be achieved, although the other specifications (e.g., the systematic AM-AM) will vary as well, in a manner that may result in an undesirable outcome. An additional control knob, with a somewhat independent influence, is useful to make the PA work in a more favorable fashion. The bias condition of the PA cells, especially the auxiliary amplifier, can provide such a control parameter. Since in practical devices the gm is usually bias dependent, as the bias voltage of the auxiliary amplifier is varied, both the turn-on input power level and the gm change, affecting the overall AM-AM behavior as well as the back-off efficiency profile of the PA (similar to what happens in the Doherty architecture). For example, if the auxiliary amplifier is set to have a low bias voltage (deep class-C), it will turn on at a higher input power level and even after that, it will have a low gm (soft turn-on). This condition will lead the main amplifier to go to deep saturation which is beneficial in terms

of back-off efficiency, but it is problematic in terms of linearity since the reduced Gm at saturation drops the gain. In contrast, a higher bias for the auxiliary amplifier will result in a higher overall gain and a lower efficiency peak at back-off.

An additional feature of this architecture results indirectly from the AM-PM variation caused by the device nonideality and impacts the impedance trajectories seen by the unit PA cells. As noted above, the device-related AM-PM mostly arises from the voltage-dependent capacitance variation at the input and output nodes. The onsets of this phenomenon for the individual main and auxiliary PA cells are at different power levels, due to their bias and supply voltage differences. As a result, there is a power-dependent phase variation between the individual PAs, which together with the Chireix combiner result in "self-outphasing" that slightly changes the impedance trajectories at the intermediate power levels. To capture this effect in simulation, a realistic device model is needed; the effect is shown in the simulated results for the experimental SiGe PA discussed below.

The design methodology for the SILC PA adopted in this work is to linearize the overall PA response by appropriately choosing the input phase shift θ_0 and the auxiliary bias condition, such that the best AM-AM and AM-PM are obtained.

III. Implementation and Simulation

A previously reported 28 GHz high-efficiency dual-input outphasing PA, implemented in 130 nm SiGe BiCMOS (GlobalFoundries 8HP) process [8], is used in this work as the core PA [Fig. 8(a)]. The combiner is implemented as a "triaxial balun" with electrical length of $\sim\lambda/15$ using the top three metal layers of the process, achieving an exceptionally low loss of ~0.5 dB at 28 GHz (determined in a back-to-back balun measurement). A detailed model for the triaxial balun is proposed in [8]. The unit amplifiers employ a cascode cell with a smaller size top device to achieve the low output capacitance needed for the Chireix operation. The bias voltages have been modified in accordance with the desired mode of operation (i.e., class-C bias and higher V_{CC} for the auxiliary amplifier). Base biases were provided through 100 Ω on-chip resistors and the transistors drew 33.4 mA and 38.8 mA, measured at maximum power, from supply voltages of 3.7 V and 4.3 V for the main and auxiliary PA cells, respectively.

The postlayout simulation of this PA, fed by a pair of phase-shifted RF signal sources, confirms the predicted behavior in terms of efficiency and linearity. As shown in Fig. 8(b), if the auxiliary amplifier is completely turned off, the main amplifier by itself introduces a noticeable amount of AM-PM distortion toward its saturation. A proper bias of the auxiliary amplifier together with appropriate phase shift result in a flat AM-PM response (over-compensation is also possible and must be avoided).

Based on the simulations, in this design, the signal phase shift due to the input impedance difference of the PA cells is sufficient for the desired operation ($\theta = \theta_1$) and there is no need for an explicit delay line at the input ($\theta_0 = 0°$). Therefore, the same RF signal is fed to both inputs of the core PA, via DC blocking caps that are necessary because of the difference in the base bias of the PA cells. A back-to-back

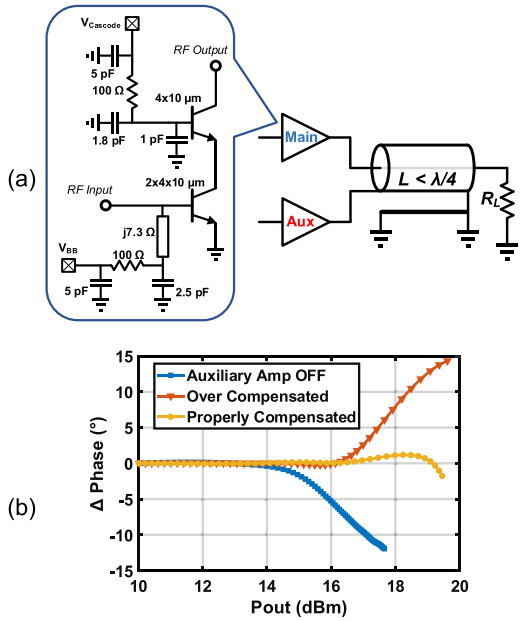

Fig. 8. (a) Schematic of the core PA [8]. (b) Postlayout simulation of the overall AM-PM response at 28 GHz.

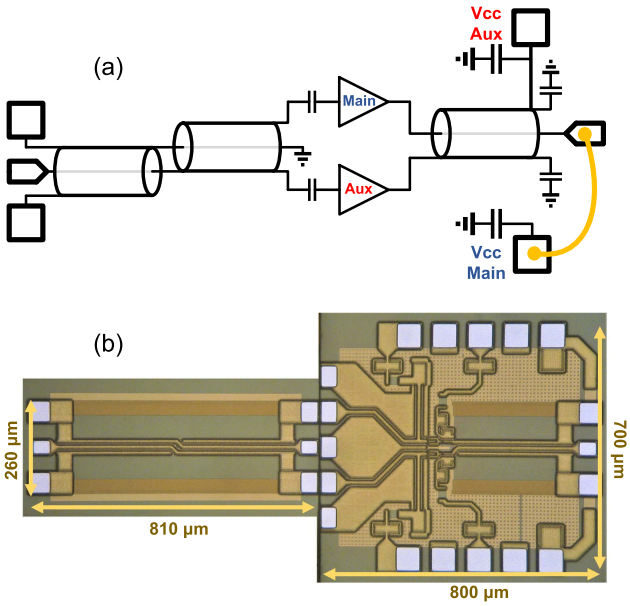

Fig. 9. (a) Schematic of the overall PA. (b) Die photo (before wirebonding).

triaxial balun (fabricated to be tested separately) is used for this purpose. The core PA and the input signal splitter chips are attached next to each other on a board and connected via very short wirebonds, forming the overall PA (Fig. 9). The effect of the wirebonds is included in the simulations by using series inductors.

The postlayout simulation results of the overall PA, while being driven from a single 28 GHz RF source, are shown in Fig. 10. By manually de-embedding the 85 fF device output capacitance, the impedance variations seen by the internal current sources of the main and auxiliary amplifiers are captured [Fig. 10(a)]. The trajectories shown here (with the Smith chart normalized to R_L) are slightly more curved

TABLE I
COMPARISON WITH STATE-OF-THE-ART

	This Work	[15]	[16]	[17]/[19]	[18]/[19]	[20]	[21]
Frequency (GHz)	27.5	28	26.75	27	26	30	27
Technology	130 nm SiGe	45 nm CMOS-SOI	45 nm CMOS-SOI	45 nm CMOS-SOI	45 nm CMOS-SOI	28 nm CMOS	40 nm CMOS
Topology	SILC	Doherty	2-stack	2-stack	4-stack	2-stage Diff.	3-stage Diff.
Psat (dBm)	19	22.4	18.9	19.5	23.6	15.3	15.1
Peak PAE (%)	34	40	40.5	46.7	32	36.6	33.7
6 dB PBO PAE (%)	23	28	23	24	17	18	15.1
Gain (dB)	9.7	10	12	10*	11.5	16.3	22.4
Modulation Type	64QAM OFDM	64QAM OFDM	64QAM OFDM	64QAM OFDM	64QAM OFDM	64QAM OFDM	64QAM OFDM
Signal BW (MHz)	100	800	800	800	800	250	800
Predistortion	No	No	No	No	No	No	No
Average Pout (dBm)	11.9	13	9.8	9.2	15	5.3	6.7
EVM (%)	4.9	5.5	5.5	5.5	5.5	5.6	5.6
Average PAE (%)	20.2	16.8	14.8	17	14	9.6	11

* Gain at maximum PAE

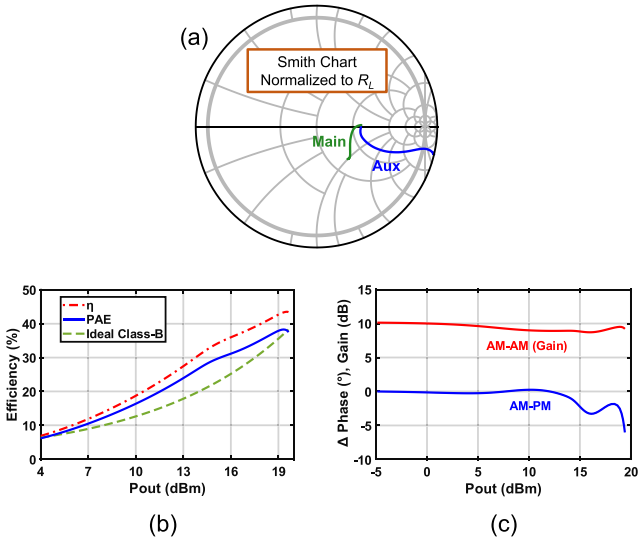

Fig. 10. Full PA postlayout simulation at 28 GHz. (a) Trajectories of impedance seen by the internal current sources of the main and auxiliary amplifiers. (b) Efficiency. (c) Gain and AM-PM.

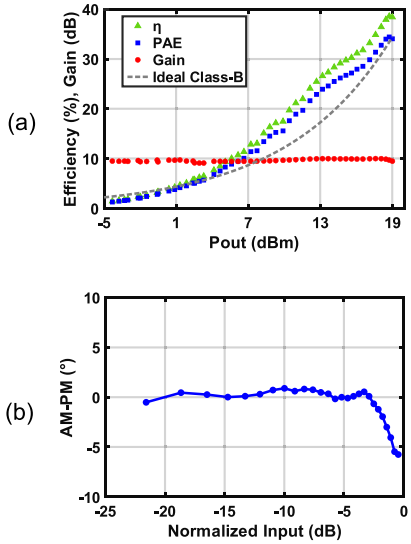

Fig. 11. (a) CW measurement at 27.5 GHz showing efficiency and gain. (b) AM-PM obtained from the modulated signal measurement under the same bias condition.

than those in the idealized simulations of Figs. 6 and 7, due to the "self-outphasing" phenomenon mentioned in the previous section. The insertion loss of the output balun is the expected value of 0.5 dB and stays constant with respect to the output power. Fig. 10(b) shows that the PAE at 6 dB back-off is improved by 34% compared to an ideal Class-B, while Fig. 10(c) shows the gain is flat to within 1 dB and the phase variation is below 5° up to 19 dBm output power. The AM-AM and AM-PM variations remain in these ranges at least for 1 GHz of bandwidth, under the nominal bias condition.

IV. MEASUREMENT RESULTS

Measurements are carried out at 27.5 GHz (instead of 28 GHz) due to the presence of a slight mistuning in the circuit. Fig. 11(a) shows the continuous wave (CW) test result demonstrating more than 19 dBm Psat with peak PAE of 34.4% and 6 dB back-off PAE of greater than 23% that corresponds to 34% improvement over ideal Class-B back-off behavior. The gain is also shown on the same plot; it is flat to within ±0.3 dB of 9.7 dB. The AM-PM shown in Fig. 11(b) is obtained from the modulated signal measurement under the same bias condition and has ±3.3° variation.

A 100 MHz 64QAM OFDM signal (generated with Keysight M8195A Arbitrary Waveform Generator and up-converted to 27.5 GHz) is used to evaluate the dynamic performance of the PA (with output signal captured using Agilent DSO80604B 6 GHz 40 GS/s real-time oscilloscope

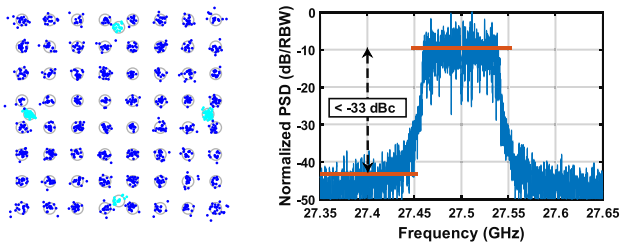

Fig. 12. (a) Constellation and (b) spectrum of the PA output for a 100 MHz 64QAM OFDM signal centered at 27.5 GHz with no DPD.

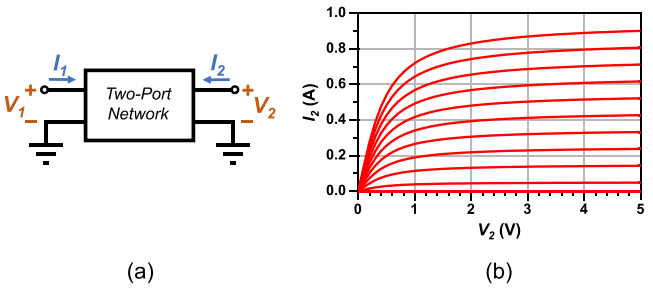

Fig. 13. (a) Generic two-port network that is used to create the VCCS transistor model. (b) I-V curves of the model described by (12) with $V_{th} = 0.5$, $gm = 0.1$, and $\alpha = 2.5$, while V_1 is swept from 0 to 10 V with 1 V steps.

after down-conversion to 2.5 GHz). The average collector efficiency of 22.9% and the average PAE of 20.2% are obtained for 11.9 dBm output power. Linear equalization has been applied to the complete setup including the DUT (using Keysight VSA software), and with no DPD, EVM of 4.9% and ACLR better than −33 dBc (at 100 MHz offset from the carrier frequency) are achieved. Fig. 12 shows the resulting constellation and spectrum of the output signal.

Table I summarizes the SILC PA performance and compares it to the recently published state-of-the-art PAs that modulate OFDM signals without employing digital enhancement. Given these constraints, this work presents the highest reported average efficiency for a silicon-based integrated PA. Better results can be achieved by utilizing dual-input PAs and digital enhancement techniques [7]–[11].

V. Conclusion

SILC, a new method for simultaneously improving back-off efficiency and linearity of PAs is presented. The circuit consists of a Chireix outphasing topology with asymmetric biases for the PA cells and a simple input signal splitter creating a phase shift between them. The implemented mm-wave integrated circuit achieves an average PAE greater than 20% while modulating a 64QAM OFDM signal with 100 MHz bandwidth and 11.9 dBm average output power at 27.5 GHz. Without using DPD, EVM less than 5% and ACLR better than −33 dBc are obtained, demonstrating the potential for emerging 5G applications. Additional improvements may be possible in future work by using different device sizes for the two branches.

Appendix A
Idealized Transistor Model

A mathematically defined two-port network [Fig. 13(a)] is used to create the transistor model as a VCCS with knee voltage. The set of conditions and equations that are used to define the transistor-like behavior are given in the following equation:

$$\begin{cases} I_1 = 0 \\ \text{if } [(V_1 - V_{th}) \le 0] \text{ or } [V_2 \le 0] \text{ then } I_2 = 0 \\ \text{else } I_2 = gm \times (V_1 - V_{th}) \times \dfrac{\arctan(V_2/\alpha)}{\pi/2}. \end{cases} \quad (12)$$

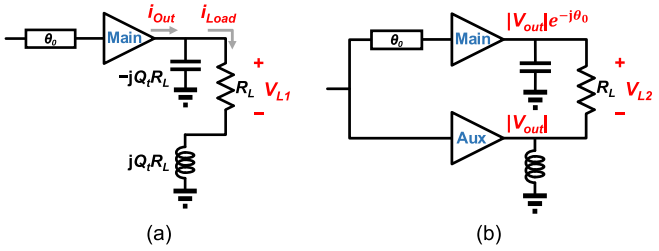

Fig. 14. Equivalent circuits to calculate the phase of the load voltage at (a) low power and (b) peak power.

V_{th} and gm model the transistor's threshold voltage and forward conductance, respectively, while α sets the value of the knee voltage. Fig. 13(b) shows a set of I-V curves obtained by using this transistor model with $V_{th} = 0.5$, $gm = 0.1$, and $\alpha = 2.5$. In this simulation, V_1 is swept from 0 to 10 V with 1 V steps.

Appendix B
Derivation of the Systematic AM-PM Equation

In order to calculate the overall systematic AM-PM, the phase of the load voltage at low power (V_{L1}) and at peak power (V_{L2}) is subtracted from each other. Fig. 14(a) shows the equivalent circuit at low power when the auxiliary amplifier is off, with the corresponding currents annotated. It is obvious that the phase of V_{L1} is the same as the phase of i_{Load} in this mode of operation. By writing KVL and KCL at the output node of the main amplifier, it can be shown that $i_{Load} = i_{Out} \times (-\mathrm{j}Q_t)$, and since i_{Out} itself has θ_0 degrees delay, the phase of V_{L1} is calculated to be $-(\theta_0 + 90°)$.

Fig. 14(b) shows the equivalent circuit at peak power. If the PA is designed such that at this point the main and auxiliary amplifiers see a purely resistive (PF = 1) impedance and have the same voltage swing ($|V_{Out}|$), V_{L2} would be equal to $|V_{Out}| \times [\exp(-\mathrm{j}\theta_0) - 1]$. In that case, it can be shown that the phase of V_{L2} is equal to $-(\theta_0/2 + 90°)$.

The overall phase variation from low power to peak power is equal to phase of V_{L2} minus phase of V_{L1}, which results in $\theta_0/2$, as it was suggested by (6).

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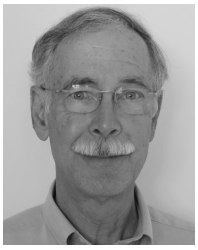

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