A Compact Dual-Band Digital Polar Doherty Power Amplifier Using Parallel-Combining Transformer

Yun Yin, *Member, IEEE*, Liang Xiong, Yiting Zhu, Bowen Chen, Hao Min, and Hongtao Xu, *Senior Member, IEEE*

***Abstract*— This paper presents a dual-band high-power digital polar Doherty power amplifier (PA). A current-mode parallel-combining transformer (PCT) power combiner is introduced for Doherty operation, which realizes simultaneous dual-band coverage, high output power, and backoff efficiency enhancement with an ultra-compact single-transformer footprint. The PA is implemented in 55-nm CMOS and occupies 1.11 mm^2 die area. It achieves 28.9-dBm peak P_{out} with 36.8% PAE in low band (LB) and 27.0-dBm peak P_{out} with 25.4% PAE in high band (HB). For 12-subcarrier 180-kHz bandwidth cellular narrowband Internet-of-Things (NB-IoT) signals, the peak P_{avg} of 24.4 dBm with average PAE of 29.5% at 850 MHz and the peak P_{avg} of 23.0 dBm with average PAE of 17.9% at 1.7 GHz are obtained with −21.6-dB error vector magnitude (EVM). Moreover, the PA achieves 20.8-dBm P_{avg}, 22.7% average PAE, and −30.5-dB EVM for 20-MHz 256-QAM WLAN signal.**

***Index Terms*— CMOS, digital, Doherty, dual-band, narrowband Internet-of-Things (NB-IoT), parallel-combining transformer (PCT), power amplifier (PA).**

I. Introduction

CELLULAR narrowband Internet-of-Things (NB-IoT) [1] have become an important branch of Internet of Everything (IoE). Based on existing wireless networks, NB-IoT provides better coverage for thing-to-thing communications, supports massive connections, and lowers power consumption. It enables easy access and interaction with a variety of devices in different domains, such as home appliance, mobile health care, industry automation, smart grids, and so on. However, NB-IoT specifies stringent emission mask to compatible with guard-band or in-band scenarios, supports multiple operation bands over 699–915 MHz [low band (LB)] and 1710–1980 MHz [high band (HB)], and requires at least 23-dBm maximum output power for long-range communication.

For cost reduction, longer battery life, and fast time to market, the integration of high-power high-efficiency power amplifiers (PAs) on-chip is greatly demanded, albeit it is quite challenging in low-cost digital processes given the low supply voltage and metal stack optimized for digital routing. To benefit from advanced CMOS technology, the digital polar transmitter has become the most attractive architecture for IoT applications, and so on, due to its high output power and efficiency [2]–[6]. In addition, in order to simultaneously support dual bands for user flexibility, traditional solutions usually employ either separately optimized PAs [7]–[9] or a single PA with tuning load impedance [10], [11], which increases design complexity and die area. Park *et al.* [12] propose an ultra-compact single-transformer-based passive network, which provides parallel power combining and optimum load transformation simultaneously at two operation bands without any tuning elements or band selection switches.

Furthermore, high peak-to-average-power-ratio (PAPR) multi-subcarrier modulation scheme is adopted in NB-IoT to achieve higher throughputs and better spectral efficiency, which requires the PA to be efficient not only at peak power but also at power backoff (PBO) to extend battery lifetime. Many techniques have been developed to enhance PA PBO efficiency, including envelope tracking [13], [14], outphasing [15]–[17], Doherty [18]–[21], and so on. Envelope tracking improves the average efficiency by modulating the supply voltage according to signal envelope, but the supply modulator presents stringent tradeoffs among speed, efficiency, and dynamic range. In an outphasing architecture, the input signal is decomposed into two constant components and combined through efficient switching-mode PAs. By using proper power combiners, the outphasing technique also enhances the PBO efficiency. However, constant power consumption from drivers and short-circuit current often degrade overall efficiency, especially at deep PBOs. Doherty PAs utilize main/auxiliary sub-PAs to perform load modulation and boost PBO efficiency without costly computation of input signals. However, several key challenges exist in Doherty PAs, such as poorly coordinated main/auxiliary paths, large and lossy high-order passive networks, and limited RF bandwidth, which result in compromised performance for the traditional analog Doherty PAs.

Alternative analog Doherty PA architectures using a serial-combining transformer (SCT) have been proposed to perform power combining and load modulation while achieving wide bandwidth [22], [23]. These passive networks typically require the use of large switches or tuning capaci-

Manuscript received August 20, 2018; revised December 19, 2018; accepted January 20, 2019. Date of publication February 18, 2019; date of current version May 24, 2019. This paper was approved by Associate Editor Waleed Khalil. This work was supported in part by the National Science and Technology Major Projects of China under Grant 2018ZX03001005-004 and in part by the National Natural Science Foundation of China under Grant 61604043 and Grant 61874153. *(Corresponding author: Hongtao Xu.)*

The authors are with the State Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China (e-mail: hongtao@fudan.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2896407

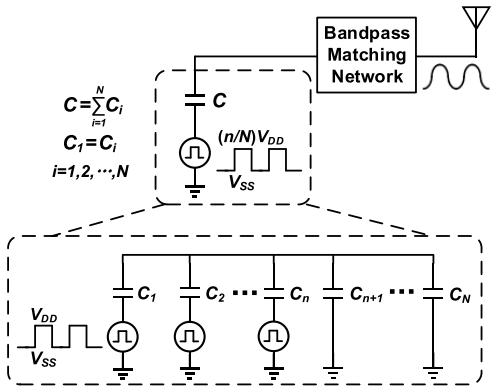


Fig. 1. Block diagram of a typical single-ended SCPA [27].

tors, which increases backoff insertion loss and would cause gain/phase discontinuities. Recently, transformer-based digital Doherty PAs have gained extensive attention owing to the well-cooperated main/auxiliary paths, superior PBO efficiency enhancement, and broadband operation. Compared with current-mode counterparts [24], the voltage-mode digital Doherty PA utilizing switched-capacitor PAs (SCPAs) is proposed in [25], which shows good linearity and intrinsic low impedance at OFF state, thus eliminating the use of large switches. However, two transformers are needed in all above-mentioned transformer-based Doherty PAs and occupy a large area. In our work, a high-power digital Doherty PA is proposed for NB-IoT applications, which introduces an ultra-compact single-transformer-footprint parallel-combining transformer (PCT) power combiner for simultaneous dual-band coverage and PBO efficiency enhancement [26].

This paper is organized as follows. In Section II, theoretical operations of Doherty SCPA with ideal SCT/PCT and non-ideal PCT power combiners are discussed. Section III describes the detailed circuit implementation. Section IV shows the measured results, with conclusions drawn in Section V.

II. Theory of Operation

The digital PA plays a dominant role in digital transmitters, which performs digital-to-analog conversion, frequency up-conversion, and power amplification all-in-one. Intensive studies have been directed toward voltage-mode Class-D-based SCPAs [25]–[32], which are more amenable to CMOS scaling and have good linearity and efficiency due to precision capacitor ratios and fast low-loss switches.

As shown in Fig. 1, a typical single-ended SCPA comprises an array of N unit capacitors and a bandpass matching network. Digital codes proportional to the input amplitude select the corresponding number of n capacitors, whose bottom plates are switched between V_{DD} and V_{SS} at the RF frequency, while the unselected $(N - n)$ capacitors are connected to ground. Thus, an equivalent square-wave voltage is generated that is quantized depending on the ratio of selected capacitors to total numbers. The bandpass matching network filters the square wave to sinusoidal output by resonating with the total capacitance C and provides the load transformation to generate high output power.

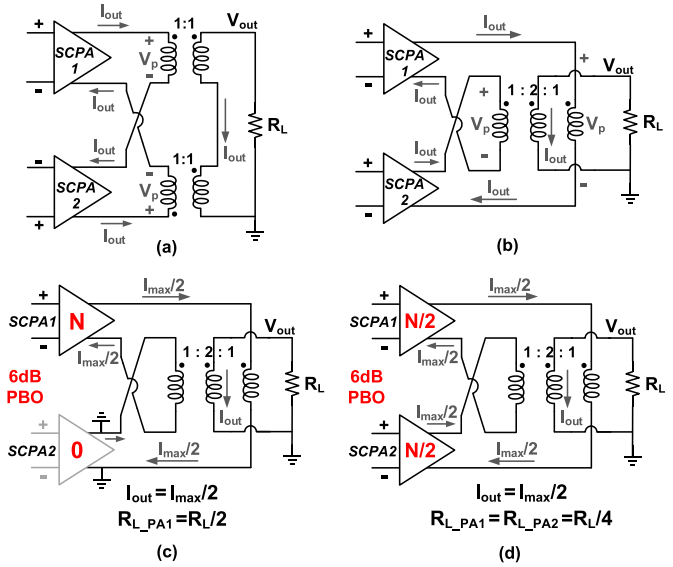


Fig. 2. SCPA architectures using (a) SCT and (b) PCT power combiners. PCT-based SCPAs at 6-dB PBO: (c) Doherty and (d) symmetrical configurations.

A. Doherty SCPA With Ideal SCT/PCT Power Combiner

As shown in Fig. 2(a), SCT-based Doherty SCPAs have been proposed to perform power combining and load modulation [25], [30], where two ideal transformers with 1:1 turn ratios bridge between the two identical sub-PAs to collect their outputs and provide proper matching. In our work, an ultra-compact single-transformer-based Doherty SCPA using PCT power combiner is proposed, as shown in Fig. 2(b). The voltage-mode and current-mode combining are employed in SCT and PCT power combiners, respectively. For an SCT power combiner, each primary coil is coupled to its own secondary coil, and the two secondary coils are in series to combine the output voltages at load from the two primaries. While for the proposed PCT power combiner, the two primary coils are both coupled to the same secondary coil, and their output currents are finally combined at load in the secondary coil.

With the same primary and secondary inductances as the SCT combiner [Fig. 2(a)], the turn ratio of the proposed PCT power combiner is 1:2:1. Then, it can be derived that this PCT Doherty SCPA will perform the same load impedance, output voltage, and output power as the SCT counterpart, but with an ultra-compact implementation. Here, the three-coil current-mode PCT combiner acts as a four-way power combiner, where the two primary coils are driven by two differential sub-PAs. The configuration of the PCT power combiner maintains both sub-PA pairs quasi-differential and close to each other, which is critical to minimize differential mismatch and reduce effective ground parasitics.

In the polar architecture, SCPA1 and SCPA2 are in-phase. With input power increased, they are turned on in sequence. At peak power, both sub-PAs are fully switched on and the single-ended impedance R_{L_PA} seen by each sub-PA is $R_L/4$. With output power decreased, SCPA2 is gradually switched off and the impedance seen by SCPA1 increases until it reaches $R_L/2$. An efficiency peaking at 6-dB PBO is achieved due to Doherty

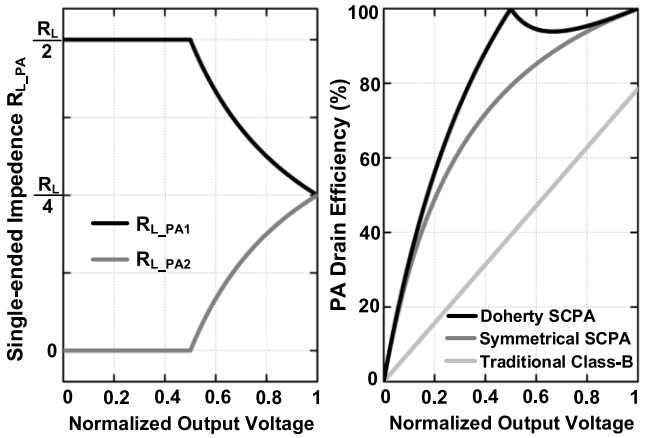


Fig. 3. Single-ended impedance RL_PA seen by sub-PAs of the SCT/PCT-based Doherty SCPAs and PA drain efficiency comparisons ($Q_{\mathrm{Load}} = 3$ assumed).

load modulation when the SCPA2 is completely turned off, as shown in Fig. 2(c). Compared with the case that two sub-PAs are controlled synchronously (called symmetrical SCPA), as shown in Fig. 2(d), the load impedance of each sub-PA stays constant when the output power is gradually backoff from peak and it does not perform efficiency enhancement at PBOs. Then, for both SCT- and PCT-based Doherty SCPAs, with n ($0 \le n \le 2N$) unit cells being switched, the fundamental components of the primary voltage V_{p}, PA output voltage V_{out}, and output power P_{out} are as follows:

$$V_{\mathrm{p}} = \frac{2}{\pi}\left(\frac{n}{N}\right) V_{\mathrm{DD}} \tag{1}$$

$$V_{\mathrm{out}} = \frac{4}{\pi}\left(\frac{n}{N}\right) V_{\mathrm{DD}} \tag{2}$$

$$P_{\mathrm{out}} = \frac{8}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{\mathrm{DD}}^2}{R_L}. \tag{3}$$

The load modulation of the Doherty SCPA is shown in Fig. 3, which can be derived as

$$R_{L\_\mathrm{PA1}} = \begin{cases} \dfrac{R_L}{2}, & 0 \le n \le N \\ \left(\dfrac{N}{n}\right)\dfrac{R_L}{2}, & N \le n \le 2N \end{cases} \tag{4}$$

$$R_{L\_PA2} = \begin{cases} 0, & 0 \le n \le N \\ \left(\dfrac{n-N}{n}\right)\dfrac{R_L}{2}, & N \le n \le 2N. \end{cases} \tag{5}$$

Then, the dynamic power P_{SC} required to charge/discharge the capacitor arrays and the PA drain efficiency η_{PA} are given by

$$P_{\mathrm{SC}} = \begin{cases} \dfrac{2n(N-n)}{N^2} C V_{\mathrm{DD}}^2 f, & 0 \le n \le N \\ \dfrac{2(n-N)(2N-n)}{N^2} C V_{\mathrm{DD}}^2 f, & N < n \le 2N \end{cases} \tag{6}$$

$$\eta_{\mathrm{PA}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{SC}}} = \begin{cases} \dfrac{2n}{2n + \frac{\pi(N-n)}{Q_{\mathrm{Load}}}}, & 0 \le n \le N \\ \dfrac{2n^2}{2n^2 + \frac{\pi(n-N)(2N-n)}{Q_{\mathrm{Load}}}}, & N < n \le 2N \end{cases} \tag{7}$$

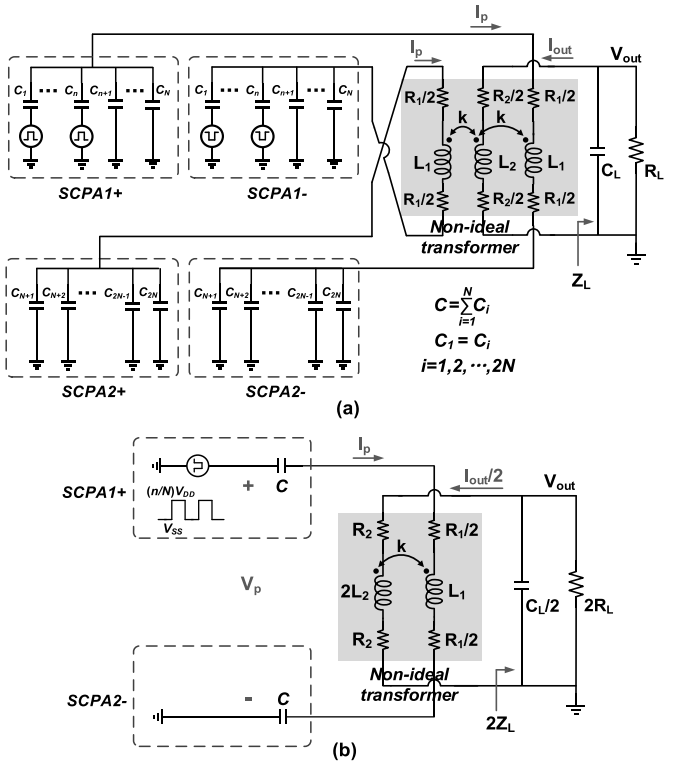


Fig. 4. (a) Detailed schematic of Doherty SCPA using the non-ideal PCT power combiner. (b) Simplified single-primary equivalent circuit.

$$Q_{\mathrm{Load}} = \frac{1}{2\pi f C R_L/4} = \frac{2}{\pi f C R_L} \tag{8}$$

where Q_{Load} is the loaded quality factor of the series resonant network. As shown in Fig. 3, the proposed Doherty SCPA has two efficiency peakings due to the load modulation, which is superior to the symmetrical SCPA and traditional Class-B PAs.

B. Doherty SCPA With Non-Ideal PCT Power Combiner

Fig. 4(a) shows the detailed schematic of a Doherty SCPA using non-ideal PCT power combiner. The network highlighted in gray represents a non-ideal transformer with both parasitic resistances and leakage inductances. To maximize the power combiner efficiency, the output capacitance C_L should resonate with the secondary inductance L_2 at the operating frequency

$$\mathrm{Im}(Z_L) = -\omega L_2. \tag{9}$$

Fig. 4(b) shows the simplified single-primary equivalent circuit. The maximum efficiency of the transformer can be achieved when the primary inductance L_1 and load impedance Z_L satisfy [33], [34]

$$\omega L_1 = \frac{2A \cdot R_L}{\alpha^2\left(1 + A^2\right)} = \frac{2A}{\alpha^2}\mathrm{Re}(Z_L) \tag{10}$$

$$A = \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2}k^2}} = \omega C_L R_L \tag{11}$$

where α is the effective turn ratio ($\alpha^2 = 2L_2/L_1$). Q_1 and Q_2 are the quality factors of primary and secondary

coils ($Q_1 = \omega L_1/R_1$, $Q_2 = \omega L_2/R_2$), and k is the coupling coefficient ($k = M/(2L_1L_2)^{1/2}$). R_L is typically 50 Ω. Then, the transformer maximum efficiency $\eta_{\max\_TF}$ is only determined by Q_1, Q_2, and k [33]

$$\eta_{\max\_\mathrm{TF}} = \frac{1}{1 + \frac{2}{Q_1Q_2k^2} + 2\sqrt{\frac{1}{Q_1Q_2k^2}\left(1 + \frac{1}{Q_1Q_2k^2}\right)}}. \quad (12)$$

The relationships between fundamental voltages and fundamental currents in the PCT power combiner can be simplified and calculated by using two-port Z-parameters [Fig. 4(b)]

$$\begin{bmatrix} V_p \\ V_{\mathrm{out}} \end{bmatrix} = \begin{bmatrix} \frac{2}{j\omega C} + j\omega L_1 + R_1 & j\omega M \\ j\omega M & 2(j\omega L_2 + R_2) \end{bmatrix} \begin{bmatrix} I_p \\ \frac{I_{\mathrm{out}}}{2} \end{bmatrix} \quad (13)$$

$$V_{\mathrm{out}} = -I_{\mathrm{out}}Z_L. \quad (14)$$

To obtain the optimal resistive load impedance for the two sub-PAs, the total capacitance of differential arrays should resonate with the primary inductance at the operating frequency, i.e., $2/(\omega C) = \omega L_1$. Thus, the secondary fundamental current I_{out} and PA fundamental output power P_{out} are derived as

$$I_{\mathrm{out}} = \frac{2B}{\pi}\frac{\alpha}{R_L}\left(\frac{n}{N}\right)V_{\mathrm{DD}} \quad (15)$$

$$B = \frac{kQ_1Q_2(1+A^2)}{k^2Q_1Q_2A + Q_2 + A} \quad (16)$$

$$P_{\mathrm{out}} = \frac{1}{2}I_{\mathrm{out}}^2\mathrm{Re}(Z_L) = \frac{2B^2\alpha^2}{\pi^2(1+A^2)R_L}\left(\frac{n}{N}\right)^2V_{\mathrm{DD}}^2. \quad (17)$$

It indicates that the Doherty PA performs linear power amplification with the non-ideal PCT power combiner. Here, the SCPA is assumed as ideal voltage sources and its nonlinearity is not included.

For PA drain efficiency calculation, the odd-harmonic power losses should be counted since the load transformation is no longer high impedance at 3rd/5th/7th…harmonic frequencies as the ideal PCT power combiner. In our work, the matching network should have wideband frequency response to support both LB and HB operations, thus the odd-harmonic impedances have similar levels as the fundamental impedance. Then, the third-order harmonic power is about 1/9 of the fundamental power while other higher order harmonic powers are negligible.

Thus, the PA drain efficiency η_{PA} can be estimated by

$$\eta_{\mathrm{PA}} = \frac{P_{\mathrm{out}}}{(10/9)P_{\mathrm{out}}/\eta_{\max\_\mathrm{TF}} + P_{\mathrm{SC}}} = \begin{cases} \dfrac{18B^2n}{\frac{20B^2n}{\eta_{\max\_\mathrm{TF}}} + \frac{9\pi(1+A^2)^2}{A}(N-n)}, & 0 \le n \le N \\ \dfrac{18B^2n^2}{\frac{20B^2n^2}{\eta_{\max\_\mathrm{TF}}} + \frac{9\pi(1+A^2)^2}{A}(n-N)(2N-n)}, & N < n \le 2N. \end{cases} \quad (18)$$

The PA drain efficiency η_{PA} is closely related to the transformer parameters k, Q_1, and Q_2, as presented in Fig. 5, where Q_1 shows a greater influence on η_{PA} than k and Q_2 at all power levels. However, in order to achieve high output power, the primary inductance L_1 is usually much smaller than the secondary L_2 to perform a large load transformation ratio, which results in decreased Q_1 and degraded drain efficiency η_{PA}. In this paper, the magnetic enhancement is introduced in the design of PCT power combiner to improve the primary quality factor, which will be explained in Section III-B. In addition to (18), other power losses owing to switch ON-resistance, switch drivers, and clock distribution parasitics can be included by estimating the transistor ON-resistance and gate capacitance being driven [27].

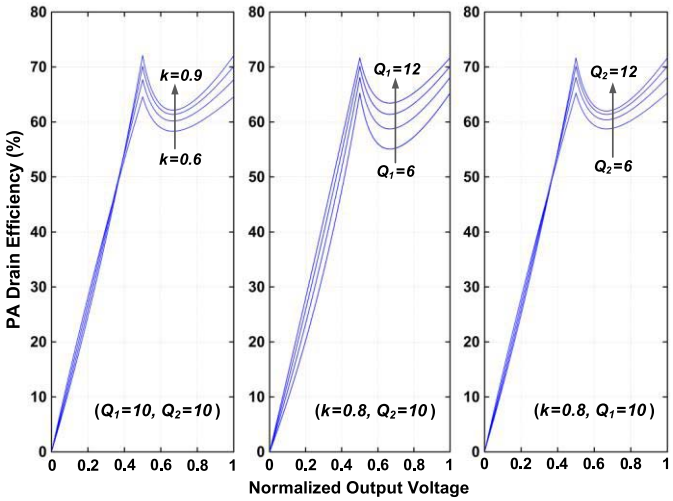


Fig. 5. Drain efficiency η_{PA} of Doherty SCPA using the non-ideal PCT power combiner with different k, Q1, and Q2 values.

III. Circuit Implementation

A. Digital Doherty PA and Floorplan

Fig. 6 shows the block diagram and floorplan of the proposed dual-band digital Doherty PA using PCT power combiner. The polar SCPA architecture is employed due to its high efficiency and good linearity. To meet stringent NB-IoT emission mask, a total resolution of 10 bits is adopted. Here, PA1 and PA2 are two identical 9-bit sub-PAs, which are controlled by the lower nine amplitude bits (AM8-0) while the highest amplitude bit (AM9) performs the Doherty operation between two sub-PAs. In order to mitigate performance variations introduced by binary cells, each sub-PA is constructed using a hybrid unary/binary array. The sub-PA is divided into 16 groups controlled by AM8-5, and each group consists of seven thermometer-coded cells decoded by AM4-2 and 2-bit LSB binary-coded cells. Therefore, the process, voltage, and temperature (PVT) mismatches of binary bits are distributed to each group and finally averaged with output power.

As shown in Fig. 6, in the unit PA cell, a cascode inverter Class-D topology is employed to distribute $2 \times V_{\mathrm{DD}}$ supply voltage stress among four transistors and provide high output power. The single-ended phase modulation (PM) signal is first converted by a single-ended-to-differential (S-to-D) block to generate the differential signals and then further level shifted to two voltage domains. Here, non-overlapping clocks with 52% and 48% duty-cycle control are adopted for PMOS and

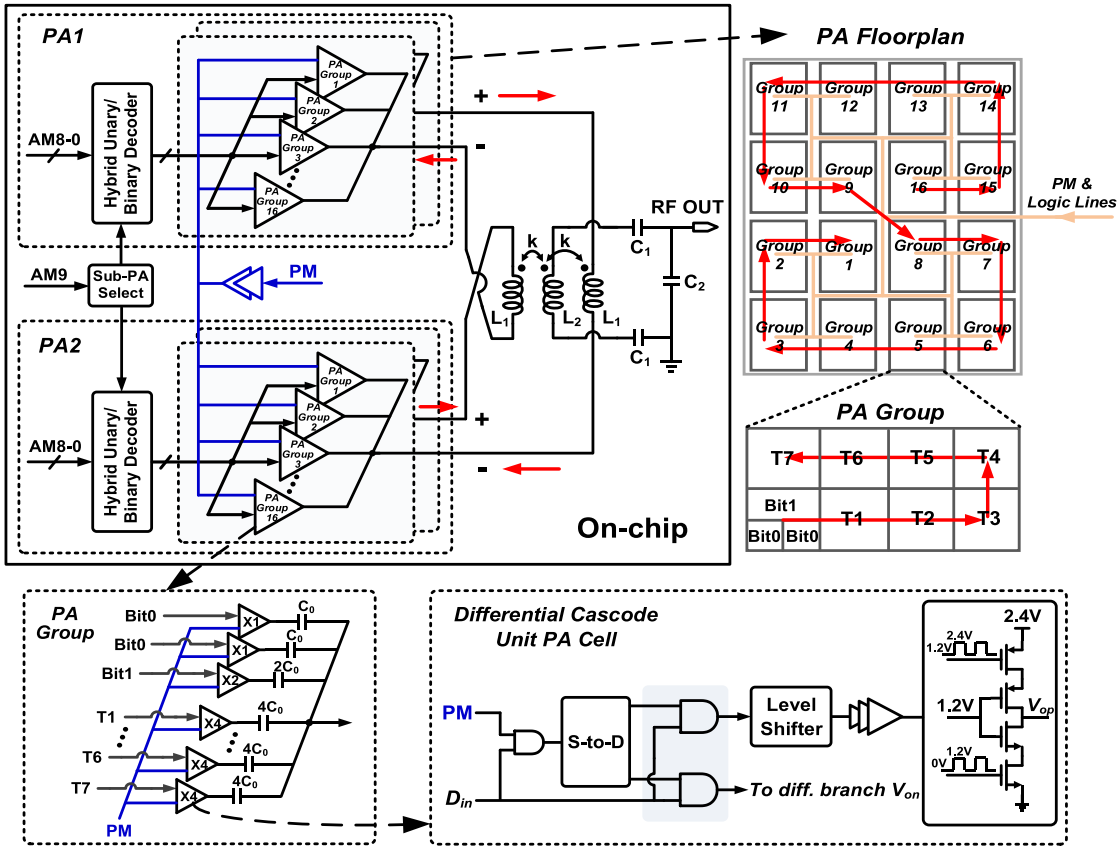


Fig. 6. Block diagram and floorplan of the proposed dual-band digital Doherty PA using PCT power combiner.

NMOS transistor chains, respectively, which help to reduce the crowbar current. At the OFF-state, the differential outputs (V_{op} and V_{on}) of the unit PA cell are both connected to ground so as to reduce different fluctuations between supply and ground. In addition, metal-oxide-metal (MOM)-switched capacitors formed by middle metal layers are laid on the top of devices to reduce capacitive parasitics while saving area.

In the floorplan, each sub-PA is arranged in order of 16 groups (Group16–1), and each group comprises seven thermometer-coded cells (T7–1) and three binary-coded cells (Bit1–0). As shown in Fig. 6, the "eight-figure" movements are performed end-to-end among groups, which shows better center symmetry to mitigate layout PVT variations and improve differential nonlinearities (DNL) [35]. Moreover, the distribution of PM and logic lines to each unit cell is routed like H-trees to minimize delay mismatches. The local oscillator (LO) gating technique that gates PM signal with input codes using AND gates is also employed to scale down LO distribution power at low output power.

B. Dual-Band Matching Network

Fig. 7 presents the implementation of the proposed single-transformer-based PCT power combiner. The three-coil PCT is implemented within an ultra-compact single-transformer footprint with seven turns, where two turns are the two primary inductances and the other five turns are the secondary inductance. In the design, the PCT power combiner

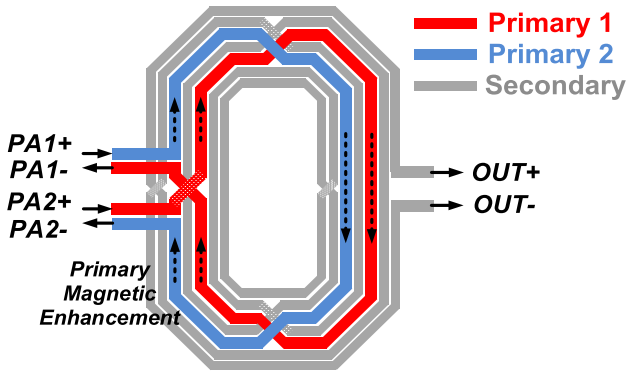


Fig. 7. Implementation of the proposed single-transformer-based PCT power combiner.

is optimized to occupy a compact die size while maintaining a high quality factor and coupling coefficient to improve the power transfer efficiency. The PCT combiner only occupies an area of 340 × 500 μm^2, and its self-resonant frequency is 3.6 GHz which is much higher than the dual-band operation frequencies. Here, PA1 and PA2 are placed at the same side of the PCT combiner to maintain good differential symmetry. Moreover, the output currents from PA1 and PA2 flow in the parallel direction in the two primary coils, which achieves magnetic enhancement and increases the effective primary inductance and quality factor, thus contributing to further size reduction and lower loss. This is especially important for on-chip matching design at the sub-GHz band.

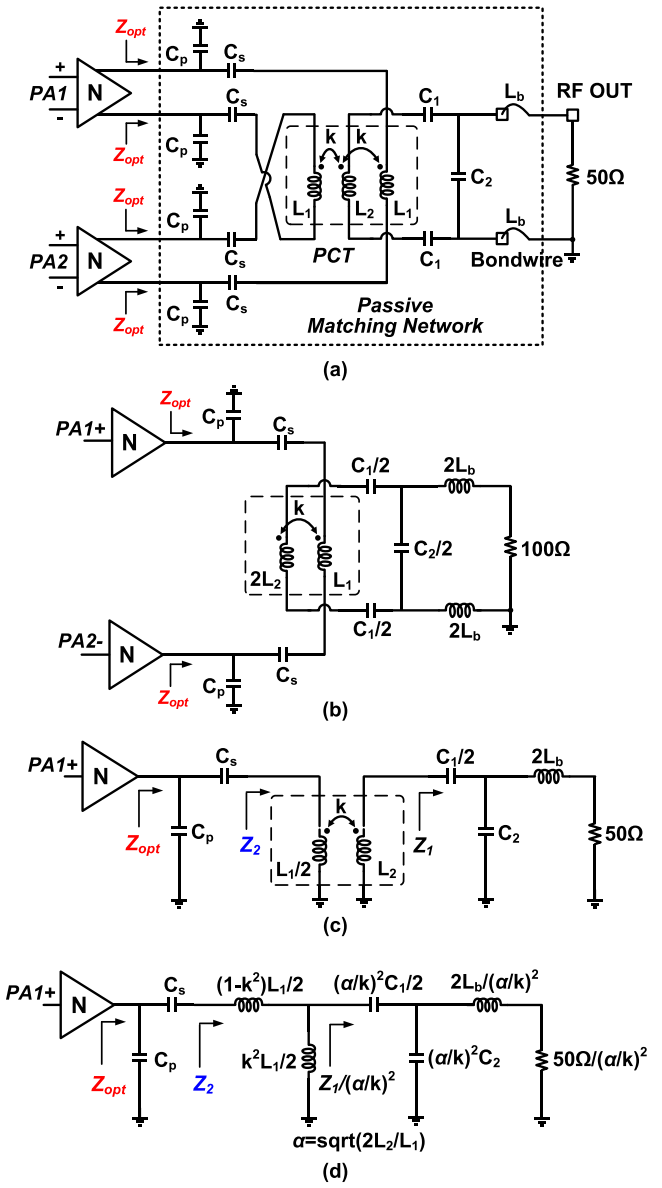


Fig. 8. (a) Lumped model equivalent circuit of the proposed passive matching network, (b) its single-primary equivalent circuit, (c) single-PA equivalent half circuit, and (d) simplified single-PA equivalent half-circuit.

Fig. 8(a) shows the lumped model equivalent circuit of the dual-band passive matching network. It consists of the PA device output capacitance $C_{\rm p}$ (which comes from the large size of the switch transistors and the routing parasitic capacitance), switched capacitors $C_{\rm s}$, a three-coil transformer, capacitors C_1 and C_2 as well as bondwires $L_{\rm b}$. The balun function is implemented on-chip with a single-ended output pad. At peak power, it transforms the optimum load for two sub-PAs. For the sake of analysis, first, the single-primary equivalent circuit is depicted in Fig. 8(b), where all the impedances of components at the secondary coil are doubled due to the parallel power combining. Then, it is further simplified to a single-PA equivalent half-circuit as shown in Fig. 8(c). Finally, the non-ideal transformer is simplified using the ideal 1:(α/k) transformer, and the antenna impedance, bondwires, and capacitors at the secondary coil are transformed to the primary side with the impedance scaling factor, as depicted in Fig. 8(d). Thus, the transformed single-ended load impedance $Z_{\rm opt}$ can be expressed as

$$\begin{aligned} Z_{\rm opt} &= \left\{ \left[(Z_{L,\rm eq} + sL_{b,\rm eq}) \left\| \frac{1}{sC_{2,\rm eq}} + \frac{1}{sC_{1,\rm eq}} \right. \right] \right. \\ &\quad \left. \left\| \frac{sL_{1,\rm eq}}{2} + \frac{s(L_1 - L_{1,\rm eq})}{2} + \frac{1}{sC_{\rm s}} \right\} \right\| \frac{1}{sC_{\rm p}} \\ Z_{L,\rm eq} &= 50/(\alpha/k)^2, \quad L_{b,\rm eq} = 2L_b/(\alpha/k)^2 \\ C_{2,\rm eq} &= (\alpha/k)^2 C_2, \quad C_{1,\rm eq} = (\alpha/k)^2 C_1/2 \\ L_{1,\rm eq} &= k^2 L_1. \end{aligned} \tag{19}$$

In the design, the device output capacitance $C_{\rm p} = 15$ pF, the output pad capacitance $C_2 = 0.1$ pF, and the bondwire $L_{\rm b} = 1$ nH. Here, the maximum output power of the PA active part is

$$P_{\rm out,max} = \frac{8}{\pi^2} \frac{V_{\rm DD}^2}{\rm Re(Z_{opt})}. \tag{20}$$

With the power supply of $V_{\rm DD} = 2.4$ V and the matching network loss of ~1.5 dB, the real part $\rm Re(Z_{opt})$ of the single-ended optimal load impedance is about 3 Ω to obtain watt-level output power and $\rm Im(Z_{opt})$ should be zero to achieve high efficiency

$$\rm Re(Z_{opt}) \text{ at LB} = 3\ \Omega, \quad Im(Z_{opt}) \text{ at LB} = 0\ \Omega \tag{21}$$

$$\rm Re(Z_{opt}) \text{ at HB} = 3\ \Omega, \quad Im(Z_{opt}) \text{ at HB} = 0\ \Omega. \tag{22}$$

Based on (19)–(22), the values of components L_1, L_2, $C_{\rm s}$, and C_1 in the matching network can be derived versus different coupling coefficients k. Fig. 9 shows the calculated optimal complex load impedance $Z_{\rm opt}$ with the coupling coefficient k varying from 0.75 to 0.9, where the band separation increases with the larger coupling coefficient k. It can be seen that the optimal complex load impedance $Z_{\rm opt} = 3$ Ω can be achieved over dual bands with k between 0.85 and 0.9. This design method is similar to the way of converting a bandpass network to the proposed output matching topology across a wide frequency range [36], [37].

By optimizing the matching network, a wideband frequency response is obtained with $L_1 = 1.3$ nH, $L_2 = 10.7$ nH, $k = 0.87$, $C_{\rm s} = 60$ pF, $C_{\rm p} = 15$ pF, $C_1 = 7$ pF, $C_2 = 0.1$ pF, and $L_{\rm b} = 1$ nH while offering the optimum load impedance for the two sub-PAs. Fig. 10 shows the load transformation trajectories on the Smith chart from 0.7 to 2.0 GHz, which can be divided into three steps: first, the capacitors C_1 and C_2 are designed to resonate the inductance of bondwires and transform antenna impedance to a capacitive impedance Z_1; then, the impedance Z_1 is scaled to $Z_1/(\alpha/k)^2$ and slightly up-transformed by the primary parallel and leakage inductances, which achieves a convergent reactive impedance Z_2; finally, the impedance Z_2 is almost completely resonated by the switched capacitor $C_{\rm s}$ and parasitic capacitor $C_{\rm p}$, resulting in the desired resistive impedance $Z_{\rm opt}$ over the operation band.

Moreover, in order to verify the layout symmetry of the proposed PCT power combiner, magnitude and phase responses of the passive matching network are simulated from each input of PA1+/− and PA2+/− to RF output, as presented

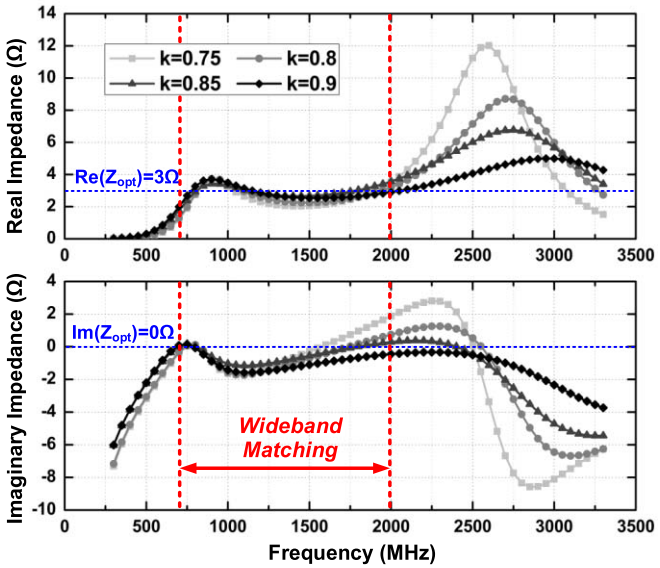


Fig. 9. PA single-ended optimal complex load impedance Z_{opt} versus different coupling coefficients k based on the equivalent model in Fig. 8(d).

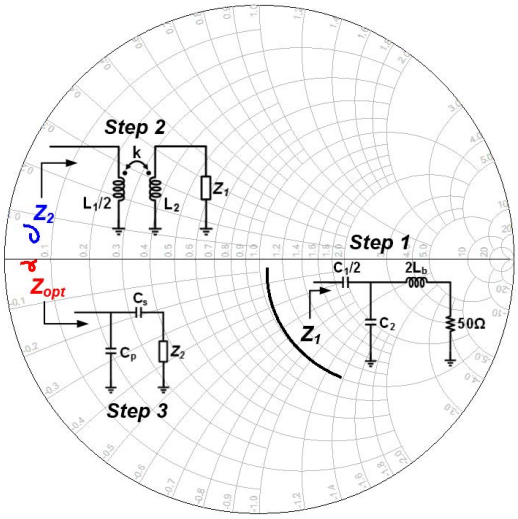


Fig. 10. Load transformation trajectories on the Smith chart from 0.7 to 2.0 GHz.

in Fig. 11, which shows little gain or phase mismatches among the four ways over the frequency. With the proposed matching network, the digital Doherty PA realizes two power peaks over LB and HB, as shown in Fig. 12, and the total passive loss from the two sub-PAs to 50-Ω load is less than 1.6 dB in the wide frequency range. In this paper, a total of 1.2-nF de-Q decoupling capacitors are integrated on-chip to attenuate supply and ground ringing while improving the linearity and noise performance.

IV. Measurement Results

The proposed dual-band digital Doherty PA is implemented in 55-nm CMOS process. As shown in Fig. 13, the chip occupies an area of 1.26×0.88 mm^2 including all decoupling capacitors and electro-static discharge (ESD) I/O pads. The PA is packaged in a quad flat no-lead (QFN) package and surface mounted on an evaluation PCB board with a single-ended

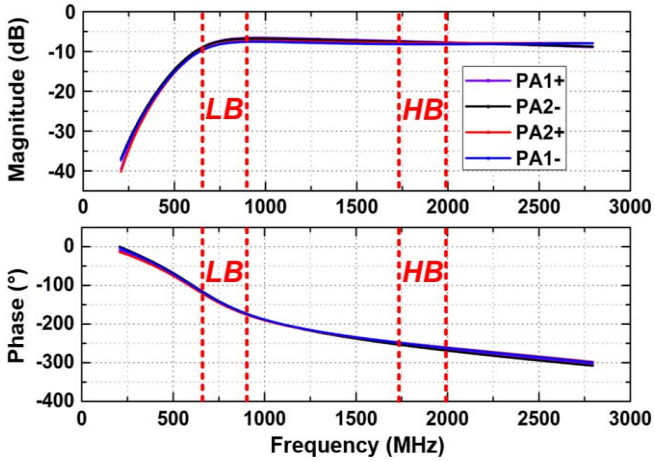


Fig. 11. Simulated magnitude and phase responses of the matching network from each input of PA1+/− and PA2+/− to RF output.

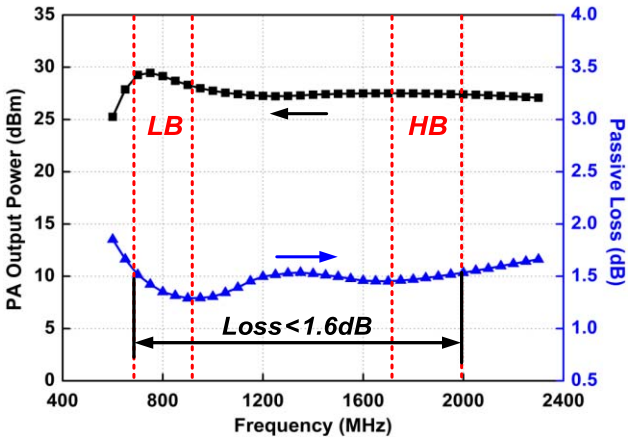


Fig. 12. Simulated PA peak output power and passive loss of matching network.

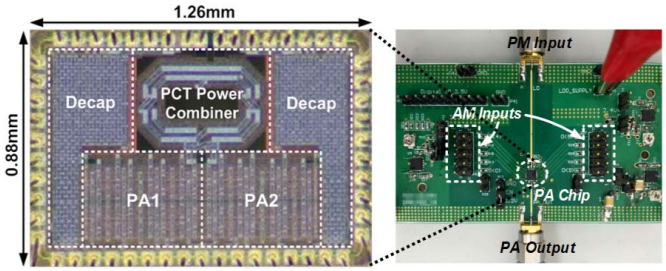


Fig. 13. Chip microphotograph and evaluation PCB board.

LO input and an RF output. The PA operates with dual power supplies of 2.4 and 1.2 V. In the PAE calculation, the power consumption of IO buffers, LO distribution drivers, logic blocks, and PAs is all included, which is equivalent to the system efficiency. In the measurement, the AM and PM signals are exported from a digital pattern generator and an arbitrary waveform generator (AWG), respectively. The AM–PM synchronization is performed by using a 10-MHz reference combined with a trigger signal from the AWG.

The measured dual-band continuous-wave (CW) results are shown in Fig. 14, where the LB achieves 28.9-dBm peak output power with 36.8% peak PAE, and the HB obtains

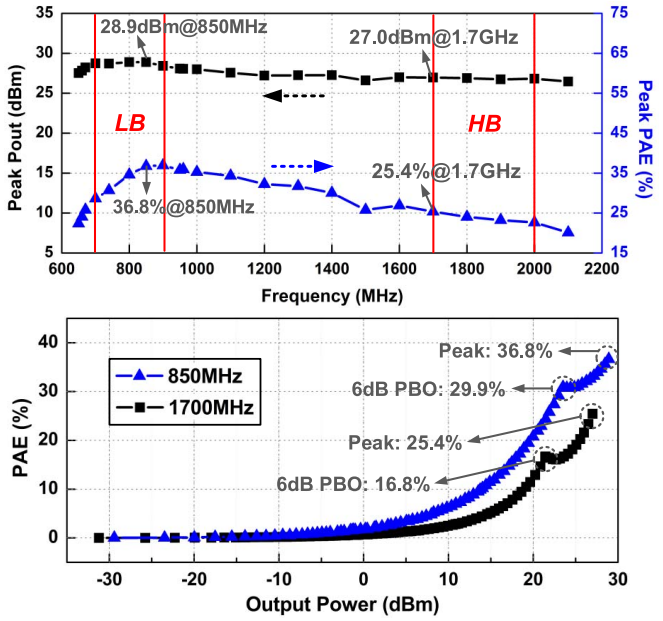


Fig. 14. Measured dual-band CW results of output power, PAE, and frequency response.

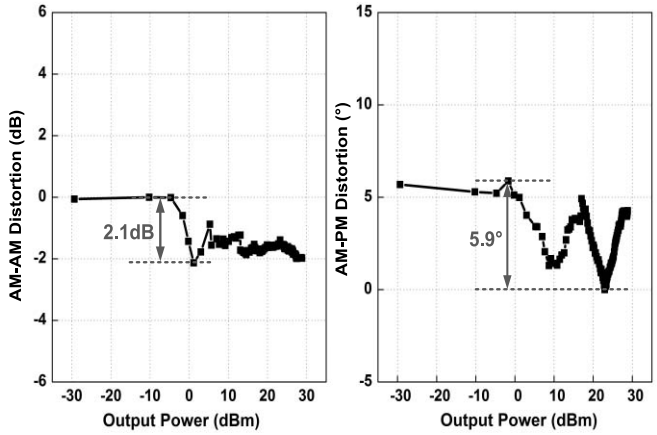


Fig. 15. Measured PA AM–AM and AM–PM nonlinearities at 850 MHz.

27.0-dBm peak power with 25.4% peak PAE. In addition, the relatively flat output power is achieved over LB and HB, respectively, with the maximum power deviations of 0.3 and 0.2 dB within the frequency bands. Owing to the Doherty load, the PAE of 29.9% and 16.8% is achieved at 6-dB PBO for 850 MHz and 1.7 GHz, respectively, showing the average efficiency enhancement. The reason why the HB performance is worse than the LB can be explained from two aspects: first, due to the higher switching frequency, the driving power and rising/falling time of HB are much larger than those of LB; second, the passive loss of HB is ∼0.2 dB larger than LB, thus resulting in the output power and efficiency degradation. Fig. 15 shows the measured AM–AM and AM–PM nonlinearities versus output power at 850 MHz. The PA obtains 2.1-dB AM–AM distortion and 5.9° AM–PM distortion, which are mainly due to the performance variations among the PA groups since the PA core occupies a relatively large area in 55-nm CMOS, and these nonlinearities are correctable by digital predistortion (DPD).

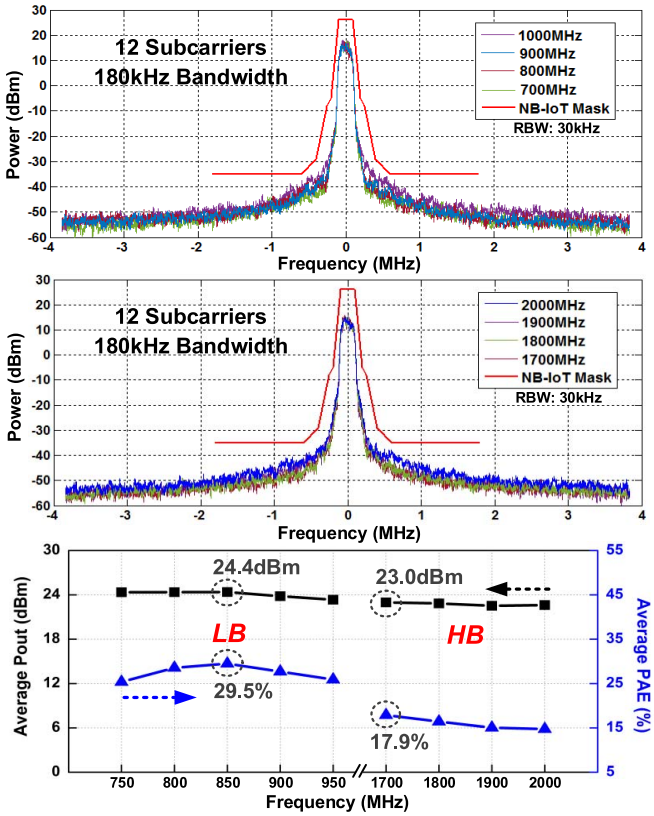


Fig. 16. Measured PA output spectrum, average P_{out}, and average PAE of the 12-subcarrier NB-IoT signal versus frequency.

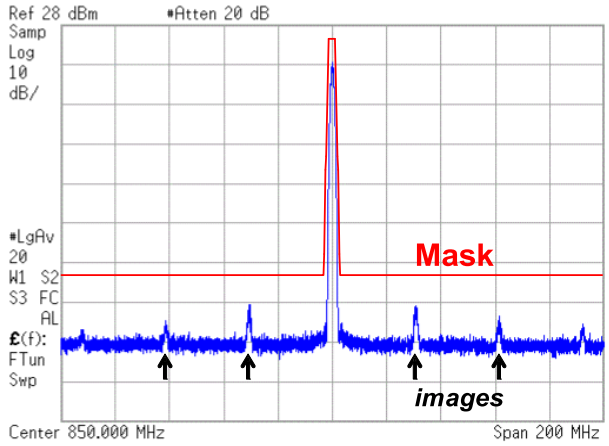


Fig. 17. Measured PA far-out spectrum of the 12-subcarrier NB-IoT signal.

In modulation tests, memoryless DPD look-up tables are used to linearize the PA. For 12-subcarrier 180-kHz bandwidth NB-IoT signals, with 4.5-dB clipping PAPR and −21.6-dB error vector magnitude (EVM), the PA output spectrum, average output power, and average PAE over the frequency are shown in Fig. 16. The PA meets the stringent NB-IoT emission mask requirements across both LB and HB bands, and it achieves P_{avg} of 24.4 dBm with average PAE of 29.5% at 850 MHz and P_{avg} of 23.0 dBm with average PAE of 17.9% at 1.7 GHz. Fig. 17 shows the PA far-out NB-IoT spectrum with 30.72-MHz up-sampling rate. As spectral images are attenuated by the sinc function associated with the zero-order hold, they can be further reduced by increasing the up-sampling rate.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

Index	This work		TCAS-I 2017 [2]†	ISSCC 2015 [7]	JSSC 2016 [12]*	JSSC 2015 [20]*	JSSC 2017 [25]*	JSSC 2017 [31]
Architecture	PCT-based digital Doherty SCPA		Current-mode digital PA	Transistor-stacked analog PA	PCT-based current-mode digital PA	Current-mode digital Doherty PA	SCT-based Class-G digital Doherty SCPA	Digital Doherty SCPA
On-chip Balun	Yes (1 transformer)		No (Off-chip matching)	Yes (2 transformer)	Yes (1 transformer)	Yes (2 transformer)	Yes (2 transformer)	No (Off-chip Matching)
Freq. (GHz)	0.85/1.7		0.891	0.95/1.95	2.6/4.5	3.82	3.5	0.9
Peak Pout (dBm)	28.9/27.0		23.2	32	28.1/26.0	27.3	25.3	24
Peak PAE (%)	36.8/25.4		44.5	-	35/21.2	32.5 (DE)	30.4	45
6dB PBO PAE (%)	29.9/16.8		-	-	-	22 (DE)**	25.3	34
Modulation Signal	12-subcarrier 180kHz NB-IoT	20MHz 64QAM/256QAM WLAN	Single Carrier, 3.75kHz NB-IoT	HSPA	8MS/s 256QAM	500kS/s 16QAM	32Carriers, 10MHz 256QAM	40MHz 256QAM 802.11ac
Carrier Freq. (GHz)	0.85/1.7	0.8	0.891	0.95/1.95	2.35/4.7	3.82	3.5	0.9
Pavg (dBm)	24.4/23.0	22.9/20.8	18.87	>26/>26	20.37/18.53	21.8	19.0	14.7
Average PAE (%)	29.5/17.9	26.1/22.7	33.4	23.7/23.8	16.26/13.42	22.1 (DE)	24.0	22
EVM (dB)	-21.6	-25.3/-30.5	-28.2	-26.6/-23.2	-36.3/-34.6	-25.0	-35.0	-34.8
Supply (V)	1.2/2.4		2	3	1.5/3	1.2/3	1.2/2.4	1.2/2.4
Chip Size (mm^2)	1.11		1.75	3‡	2.25	2.09	1.2	1.62
CMOS Technology	55nm		180nm	65nm	65nm	65nm	45nm SOI	65nm

†Results from the second prototype. ‡Estimated total area of RF DACs, LB PA and HB PA from chip micrograph.

*Results measured with GSG probe. **Estimated from Fig. 13 in [20].

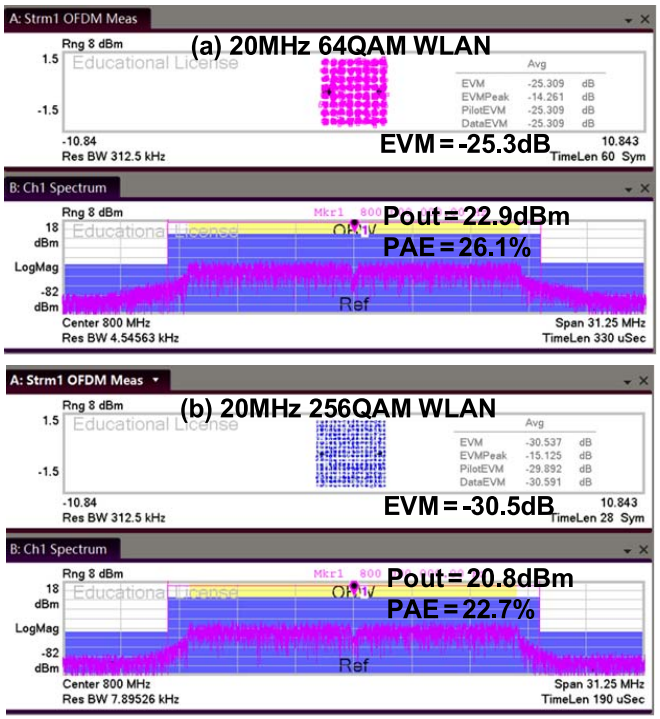


Fig. 18. Measured PA-demodulated 20-MHz 64-QAM/256-QAM WLAN signals.

Moreover, this PA can be applied to wideband communication, such as WLAN and long-term evolution (LTE). As shown in Fig. 18, the PA obtains 22.9-dBm P_{avg}, 26.1% average PAE, −25.3-dB EVM, and 20.8-dBm P_{avg}, 22.7% average PAE, −30.5-dB EVM for 20-MHz 64-QAM and 256-QAM WLAN signals, respectively. Table I gives the summary of the measured performance and the comparison with prior works. Our work delivers a close-to-watt-level peak output power and obtains the best average PAE with on-chip matching at the sub-GHz band. By utilizing a PCT power combiner, the dual-band frequency coverage, high output power, and back-off efficiency enhancement are achieved simultaneously with the smallest footprint, thereby well-fitting low-cost NB-IoT applications.

V. CONCLUSION

In this paper, we have demonstrated a fully integrated dual-band digital Doherty PA. A PCT power combiner is introduced for dual-band coverage, backoff efficiency enhancement, and ultra-compact implementation. The wide-band impedance transformation, power combining, and load modulation are realized using a single-transformer footprint. The PA achieves the state-of-the-art performance of watt-level output power, best average efficiency, and smallest die size. This digital Doherty PA is suitable for system-on-chip (SoC) integration for low-cost and low-power wireless applications.

REFERENCES

[1] *Technical Report for BS and UE Radio Transmission and Reception (Release 13)*, document 3GPP TR 36.802, Jun. 2016.

[2] Z. Song, X. Liu, X. Zhao, Q. Liu, Z. Jin, and B. Chi, "A low-power NB-IoT transceiver with digital-polar transmitter in 180-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2569–2581, Sep. 2017.

[3] D. Lachartre *et al.*, "A TCXO-less 100Hz-minimum-bandwidth transceiver for ultra-narrow-band sub-GHz IoT cellular networks," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 134–135.
[4] A. Ba *et al.*, "A 1.3nJ/b IEEE 802.11ah fully digital polar transmitter for IoE applications," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 440–441.
[5] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.
[6] M. Hashemi, Y. Shen, M. Mehrpoo, M. S. Alavi, and L. C. N. de Vreede, "An intrinsically linear wideband polar digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3312–3328, Dec. 2017.
[7] J. Moreira *et al.*, "A single-chip HSPA transceiver with fully integrated 3G CMOS power amplifier," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[8] X. Yu *et al.*, "A fully-integrated reconfigurable dual-band transceiver for short range wireless communications in 180 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2572–2590, Nov. 2015.
[9] K. Kanda *et al.*, "A fully integrated triple-band CMOS power amplifier for WCDMA mobile handsets," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 86–88.
[10] S. Hu, S. Kousai, and H. Wang, "A compact broadband mixed-signal power amplifier in bulk CMOS with hybrid class-G and dynamic load trajectory manipulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1463–1478, Jun. 2017.
[11] O. Oliaei *et al.*, "A multiband multimode transmitter without driver amplifier," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 164–166.
[12] J. S. Park, S. Hu, Y. Wang, and H. Wang, "A highly linear dual-band mixed-mode polar power amplifier in CMOS with an ultra-compact output network," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1756–1770, Aug. 2016.
[13] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho, and B. Kim, "Optimization for envelope shaped operation of envelope tracking power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 7, pp. 1787–1795, Jul. 2011.
[14] M. Hassan, L. E. Larson, V. W. Leung, and P. M. Asbeck, "A combined series-parallel hybrid envelope amplifier for envelope tracking mobile terminal RF power amplifier applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1185–1198, May 2012.
[15] P. Madoglio *et al.*, "A 20 dBm 2.4 GHz digital outphasing transmitter for WLAN application in 32nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 168–170.
[16] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani, and K. Soumyanath, "A flip-chip-packaged 25.3 dBm class-D outphasing power amplifier in 32 nm CMOS for WLAN application," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596–1605, Jul. 2011.
[17] Z. Hu, L. C. N. de Vreede, M. S. Alavi, D. A. Calvillo-Cortes, R. B. Staszewski, and S. He, "A 5.9 GHz RFDAC-based outphasing power amplifier in 40-nm CMOS with 49.2% efficiency and 22.2 dBm power," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 206–209.
[18] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.
[19] D. Kang, J. Choi, D. Kim, and B. Kim, "Design of Doherty power amplifiers for handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 8, pp. 2134–2142, Aug. 2010.
[20] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "Design of a transformer-based reconfigurable digital polar Doherty power amplifier fully integrated in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1094–1106, May 2015.
[21] Y. Shen *et al.*, "A fully-integrated digital-intensive polar Doherty transmitter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 196–199.
[22] D. Chowdhury, C. D. Hull, O. B. Degani, Y. Wang, A. M. Niknejad, "A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4G WiMax applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393–3402, Dec. 2009.
[23] E. Kaymaksut and P. Reynaert, "A dual-mode transformer-based Doherty LTE power amplifier in 40 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 64–65.
[24] L. Ye, J. Chen, L. Kong, P. Cathelin, E. Alon, and A. Niknejad, "A digitally modulated 2.4 GHz WLAN transmitter with integrated phase path and dynamic load modulation in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 330–331.
[25] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "A class-G voltage-mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3348–3360, Dec. 2017.
[26] Y. Yin, L. Xiong, Y. Zhu, B. Chen, H. Min, and H. Xu, "A compact dual-band digital Doherty power amplifier using parallel-combining transformer for cellular NB-IoT applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 408–410.
[27] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.
[28] W. Yuan, V. Aparin, J. Dunworth, L. Seward, and J. S. Walling, "A quadrature switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1200–1209, May 2016.
[29] H. Jin, D. Kim, and B. Kim, "Efficient digital quadrature transmitter based on IQ cell sharing," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1345–1357, May 2017.
[30] Y. Zhu *et al.*, "A compact 2.4 GHz polar/quadrature reconfigurable digital power amplifier in 28 nm logic LP CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[31] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "Voltage mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1295–1304, May 2017.
[32] E. Bechthum *et al.*, "A CMOS polar single-supply class-G SCPA for LTE NB-IoT and cat-M1," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp. 30–33.
[33] G. Liu, P. Haldi, T.-J. K. Liu, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600–609, Mar. 2008.
[34] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.
[35] M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, "A wideband 2×13-bit all-digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 732–752, Apr. 2014.
[36] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.
[37] C.-H. Li, C.-N. Kuo, and M.-C. Kuo, "A 1.2-V 5.2-mW 20–30-GHz wideband receiver front-end in 0.18-μm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3502–3512, Nov. 2012.

Yun Yin (S'13–M'16) received the B.S. degree in micro-electro-mechanical systems and the Ph.D. degree in micro-electronics from Tsinghua University, Beijing, China, in 2010 and 2015, respectively.

Since 2015, she has been a Research Faculty Member with the School of Microelectronics, Fudan University, Shanghai, China. Her research interests focus on analog/RF circuit design, including multi-mode transceiver and high-efficiency CMOS power amplifier (PA) for wireless communications.

Liang Xiong received the B.S. degree from Xidian University, Xi'an, China, in 2016. He is currently pursuing the master's degree with the School of Microelectronics, Fudan University, Shanghai, China.

His research interests focus on high-power CMOS digital power amplifiers (PAs) with deep back-off efficiency enhancement.

Yiting Zhu received the B.S. degree in microelectronics from Sun Yat-sen University, Guangzhou, China, in 2016. She is currently pursuing the M.S. degree with the Institute of Microelectronics, Fudan University, Shanghai, China.

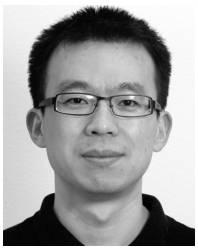
Her research interests focus on high-efficiency mixed-signal CMOS power amplifier (PA) and transmitter design.

Bowen Chen received the B.S. degree from Chongqing University, Chongqing, China, in 2013, and the M.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2016. He is currently pursuing the Ph.D. degree with the School of Microelectronics, Fudan University, Shanghai, China.

His research interests focus on wideband phase-locked loop (PLL).

Hao Min received the Ph.D. degree from Fudan University, Shanghai, China, in 1991.

From 1995 to 1998, he was a Visiting Associate Professor with Stanford University, Stanford, CA, USA, where he was involved in CMOS image sensors technologies. He was a Consultant at a number of IC design companies in Silicon Valley. From 1998 to 2005, he served as the Director of the State Key Laboratory of ASIC and System, Fudan University. From 1998 to 2006, he was the General Manager of Shanghai Huahong Integrated Circuits Company Ltd., Shanghai, where his team developed the first contact-less smart card chip that was successfully applied to the Shanghai Public Transportation System and designed the chip for the second-generation ID cards of China. He is the Co-Founder of Shanghai Quanray Electronics, Shanghai. He is currently the Vice Dean of the School of Microelectronics and the Research Director of the AUTO-ID Lab, Fudan University. He has authored or co-authored over 80 papers. He holds 20 authorized or pending patents. His current research focuses on Internet-of-Things technologies which include high-energy efficiency wireless transceiver, high-efficiency large dynamic range power management, and so on.



Hongtao Xu (S'03–M'06–SM'14) received the B.S. degree in electronic engineering from Fudan University, Shanghai, China, in 1997, the M.A. degree in economics, and the Ph.D. degree in electrical and computer engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2003 and 2005, respectively.

He was with the Intel Labs, Hillsboro, OR, USA. In 2015, he joined the School of Microelectronics, Fudan University, as a Full Professor. He has authored or co-authored more than 40 journal and conference papers. He holds 12 U.S. patents in the areas of RF transceiver and front-end module. His technical interests include innovative analog/RF/millimeter-wave circuits and wireless system for communication and sensing.

Dr. Xuis a Steering Committee Member and the Technical Program Committee Member for the IEEE Radio Frequency Integrated Circuits Symposium (RFIC).