A 1.4 GHz - 2 GHz wideband CMOS class-E Power Amplifier delivering 23dBm peak with 67% PAE

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Abstract — **The design of CMOS Power Amplifiers (PA) is still a challenging issue. Efficiency is one of the key requirements, but it is usually obtained at the expense of large device stress. The latter can be reduced by introducing a cascode solution, which features an efficiency penalty due to dissipative mechanisms associated to MOS capacitive parasitics, overlooked up to date. The class-E PA, proposed in this paper, allows simultaneously high efficiency and reduced stress by means of an integrated inductor tuning out the parasitic. Prototypes, realized in a 0.13μm CMOS technology demonstrate 67% PAE while delivering 23 dBm peak power at 1.7 GHz. PAE is still above 60% within the range 1.4GHz-2GHz.**

Index Terms — **CMOS power amplifier, switching amplifier, radio-frequency (RF) circuits, Class-E, wireless communications.**

I. Introduction

Today, the research effort is continuously pushing toward highly integrated transceivers, but the design of CMOS Power Amplifiers (PA) is still challenging. In applications requiring medium to large delivered powers, such as cellular phones, increasing the efficiency even by a small amount is fundamental to save battery life, as the power amplifier is the block of the overall transceiver contributing the most significant power consumption. For this reason, much research has recently focused on switched power amplifiers [1-6], particularly on class E and F ones, as class D PAs are commonly believed as not suited to RF operations.

The major advantage of class F PAs is given by the low peak voltage and rms current, that is very beneficial from the device stress point of view. However, although class-F PAs feature a 100% efficiency in the ideal case, they require several inductors to perform correct harmonic terminations, i.e. several spirals of metal in integrated fashion, resulting in lower efficiencies and large area consumption [5].

On the contrary, conventional class-E power amplifiers offer several advantages compared to class-F PAs. First, class-E PAs allow strong switching operations and Zero Voltage Switching (ZVS) conditions, which permits to strongly reduce capacitance discharge losses [6]. Second, their circuit, incorporating the transistor output capacitance in the circuit topology, is very simple and easy to implement (especially compared to class-F one). Unfortunately, class-E PAs feature high peak voltage and rms current waveforms, that constitute a serious stress for the devices. For this reason, the supply voltage is usually lowered compared to its maximum to assure safe operating conditions, thus degrading the overall efficiency because a lower load resistance should be matched for the same output power.

The class E PA, based on a cascode topology, has been introduced to allow a higher supply voltage without enhancing the device stress [4]. The benefit on the efficiency is actually doubtful because new mechanisms of dissipation are introduced. They are associated to charging and discharging transients of capacitance Cp, the parasitic loading the drain of the input device, M1 in Fig. 1. In this paper, we identify and discuss each of the mechanisms. A simple circuit solution, with an inductor tuning out the capacitive parasitic, is proposed. In this way, the efficiency is higher, for the same device stress, than the conventional common source and cascode based topologies.

II. Class-E PA: Efficiency And Reliability

When designing PAs, efficiency is the primary concern. On the other hand, also reliability is a crucial issue, more and more important in scaled CMOS implementations. To maximize efficiency, the most straightforward way is increasing the amplifier supply. But this makes the solution less reliable. A well identified figure of merit taking into account both efficiency and reliability does not exist. Even more, the device voltage values able to assess the reliability level of a power amplifier are not unanimously recognized when switching is at radio-frequency. To assure a reasonable device life time the

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attention is set on the maximum high-field stress (V_{GD}, V_{DS}) undergone by MOS devices.

Usually, the maximum V_{DS} is considered the parameter quantifying the device stress level, which accounts for drain junction reliability and hot carrier effects. In addition, also the maximum V_{GD}, which often exceeds V_{DS}, must be considered, and should be kept as low as possible to avoid gate oxide breakdown. Quantitatively, the maximum V_{DS} and V_{GD} must not exceed the Absolute Maximum Rating (AMR), the DC voltage limit beyond which the device unrecoverable damage occurs, set equal to $2V_{MAVS}$, V_{MAVS} being the maximum allowed voltage supply.

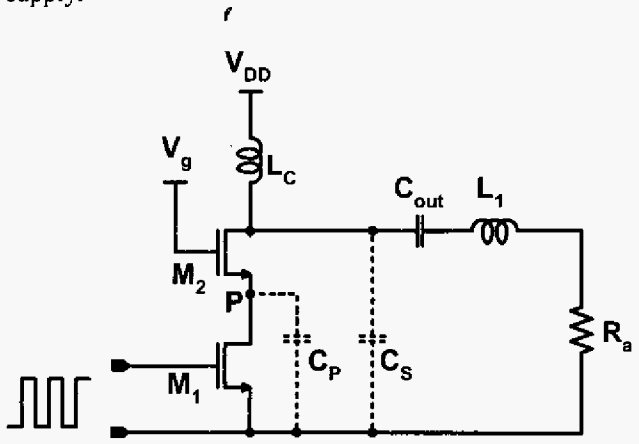

Fig. 1. Schematic of the class E PA based on a cascode topology.

In conventional common-source class E PAs delivering medium to high power level with a reasonable PAE, V_{GD} (usually more than V_{DS}) exceeds AMR because drain and gate voltage waveforms are out-of-phase. Compared to the conventional solution, the cascode class E PAs topology allows both V_{GD} and V_{DS} to be significantly reduced: V_{GD}, because the gate is positively biased at V_{DD}; V_{DS}, because the total drain voltage drops on the series of transistors M1 and M2 [4]. Therefore, being the V_{GD} and V_{DS} stresses on both transistors lower, the voltage supply (V_{DD}) can be increased compared to the conventional common source solution. For given output power, the required actual load resistance R_a is larger, thus reducing the impact on power efficiency of fixed parasitics, such as those associated with inductor Lc, output matching network, and evaluation board. Furthermore, the transistor dissipation due to the on-resistance is usually made negligible by selection of large aspect ratio devices [4].

The use of cascode topologies is thus extremely attractive especially at large delivered powers, where relatively low drain efficiencies are achieved and the improvement is approximately proportional to the increase in load resistance. On the other hand, a new intrinsic dissipative mechanism typical of the cascode topology is introduced, which might even make the cascode solution ineffective.

III. Cascode PA Dissipative Mechanisms

To gain insight into the typical dissipative mechanisms of cascode PAs, Fig. 2 shows drain and source voltage waveforms of the common gate device, M2, assuming a square wave voltage drive, together with its instantaneous power dissipation. The dissipative mechanism stems from the charging and discharging of the parasitic capacitance associated with node P. This capacitance is charged and discharged once a period and during these transients the active devices dissipate.

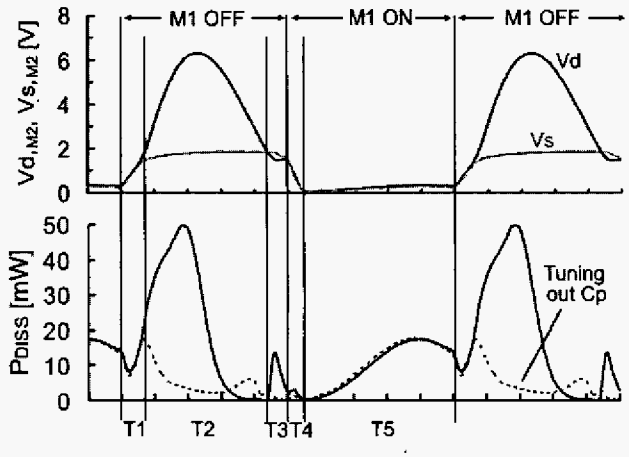

Fig. 2. Drain and source voltage waveforms and instantaneous power dissipations, P_{DISS}, of M2 with and without the inductor tuning out C_P.

At turn off, C_p starts charging and transistor M_2, in its triode region of operation, provides the current. During time interval T1, the dissipated power is thus proportional to the device on resistance r_{on}. With increasing the source voltage due to C_P charging, the MOS approaches weak inversion/sub-threshold region of operation and the drain to source voltage difference increases. Therefore, during T_2, the capacitance charges at a relatively low current (proportional to $C_p \cdot dV_S/dt$). Nonetheless, the power dissipated is not negligible at all because of the relatively large drain to source voltage, as evident from Fig. 2. During T3, M_2 reverts its operation and C_p discharges through M2 and resistor R_a. At the end of T3, M_1 turns on, and both C_p and C_S are discharged to ground, dissipating the stored energy. Finally, during T_5, the two transistors

operate in their triode region and dissipation is only due to their non zero on resistances.

Notice that the only mechanism accounting for transistor dissipation in a common source class E takes place during T_5, whereas all the others are proper of the cascode implementation. Assuming r_{on} = 330mΩ, C_P = 3.6pF as typical values for a 23 dBm design, simulations show that power dissipation due to C_P is ~5 times that due to r_{on}. Furthermore, the power dissipated by the transistor is not negligible when compared to dissipative mechanisms associated to passive components. Several designs performed for output powers in the 20dBm to 30dBm range suggest the latter represents roughly 30% of the total dissipation, assuming typical passive component resistive parasitics. This identified contribution to circuit dissipation can be minimized by means of an inductor, tuning out the capacitive parasitics. The dotted line in Fig. 2 shows the simulated power dissipation when C_P is tuned out.

III. Design

The circuit topology we propose is shown in Fig. 3, where both the power and driver stages are reported. A 0.13μm CMOS technology, provided by STMicroelectronics, has been adopted. The 50Ω load resistance is down-converted by means of the L_{match} C_a network, C_a being an off chip capacitor. All the inductors are bond wires for maximum quality factor, i.e. minimum dissipation. L_S is a spiral because its quality factor is not critical.

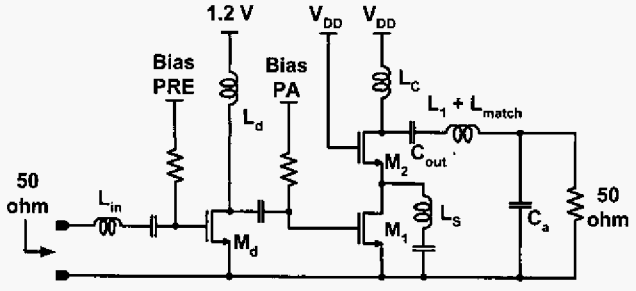

Fig. 3. Schematic of Driver and Power stages.

A relatively low quality factor has been selected both in the driver load and PA output network to allow a wide frequency range of operation. Furthermore, a low quality factor in the output network Q_{out} brings also the following advantages: 1) higher efficiency, since reducing the output network quality factor corresponds to reducing L_1, i.e. its parasitic resistance; 2) the optimum operation point of the power amplifier is less sensitive to component variations, thus allowing the PA efficiency to remain high over a wider frequency range.

All the transistors have a thick gate oxide to maximize the allowed voltage, V_{MAVS} = 2.8V. The common gate, a 3000/0.28 μm/μm width device, sustains the maximum voltage stress. To minimize V_{GD} and also to improve the efficiency, the gate of M_2 is tied to V_{DD}. From simulations, the maximum V_{GD} has been derived as ~ $2.2 \cdot V_{DD}$. Assuming that the maximum tolerable gate-drain voltage for non destructive PA operation is $V_{GD,MAX} \sim 2 \cdot V_{MAVS}$, sets the maximum voltage supply at 2.5V. The aspect ratio of the common source transistor is set to 1800/0.28 μm/μm. An higher aspect ratio would not improve the efficiency of the output stage while increasing the power consumption of the driving stage.

The transistor of the driving stage is biased in class-C. The gate capacitance of M1 is tuned out by means of L_d. L_d can be an on-chip spiral, but in this design a bondwire has been selected to save chip area. Despite a small penalty in PAE, to comply with the high operation bandwidth of the output stage and to make the circuit insensitive against component variations, the quality factor of the inter-stage resonator (L_d-$C_{GS,M1}$) has been purposely reduced to about 3. The supply voltage of the driving stage is set to 1.2V, resulting in a maximum V_{ds} voltage across M_d of about 2.4V.

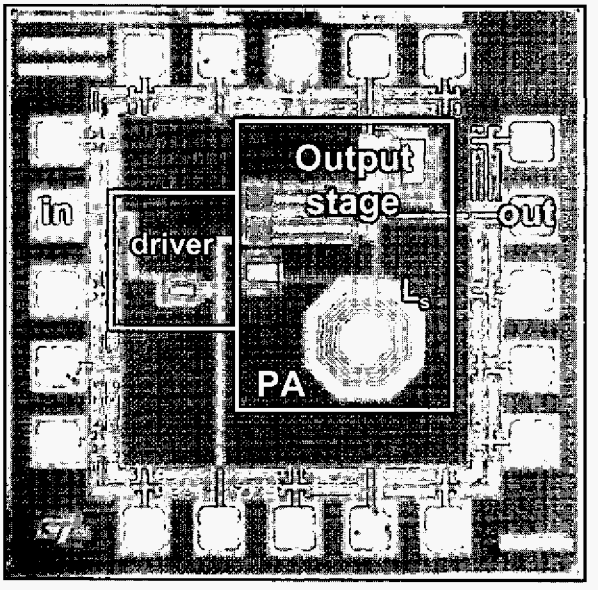

Fig. 4. Chip photomicrograph.

IV. Results

Fabricated prototypes have been characterized bonding dies directly on PCB. The photomicrograph of the realized

circuit is reported in Fig. 4. The die area, including bond pads, is 0.9 mm^2. Measured S_{11} is plotted in Fig. 5. The minimum is achieved at 1.76 GHz. The input is well matched in the 1.4 GHz – 2.1 GHz range, where S11 is below -10dB.

The delivered output power for V_{DD}=2.5V is 23 dBm, where drain efficiency (DE) and Power Added Efficiency (PAE) are 71% and 67%, respectively. The measured PAE and drain efficiency (DE) curves are plotted in Fig. 6 versus V_{DD}. The driver dissipates 11.2 mW and the PA 292 mW when V_{DD}=2.5V. As shown, both DE and PAE curve are quite flat, and the power amplifier exhibits a 59% PAE at -6dB back-off.

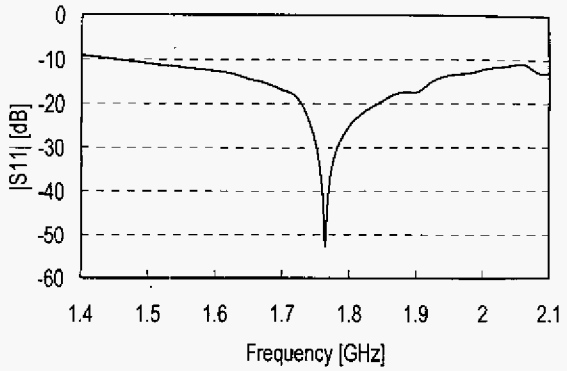

Fig. 5. Measured S11.

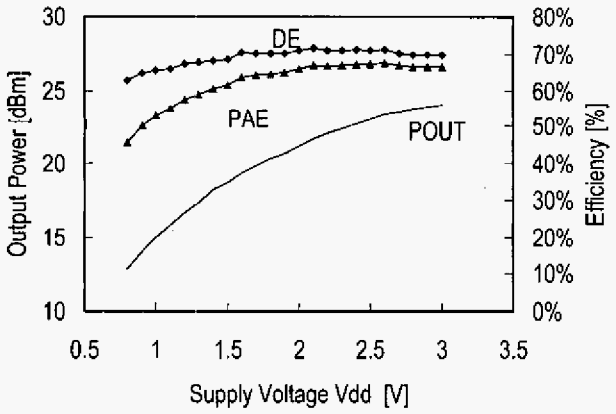

Fig. 6. Output Power (Pout), PAE and Drain Efficiency (DE) versus V_{DD} measured.

Fig. 7 shows output power, PAE and drain efficiency versus frequency. Due to the low quality factor of the output network, the PAE is above 60% in the 1.4 GHz - 2 GHz band, lending the power amplifier to operate efficiently in a wide-band.

VII. Conclusion

The cascode class-E power amplifier proposed in this paper showed reduced device stress and high efficiency, compared to a conventional common-source solution. A dissipative mechanism associated to capacitive parasitics, overlooked up to date, have been discussed and minimized by an integrated inductor. Prototypes, realized in a 0.13μm CMOS technology, have demonstrated 67% PAE when delivering 23 dBm output power at 1.7 GHz and a PAE higher than 60% over the 1.4 – 2 GHz frequency band.

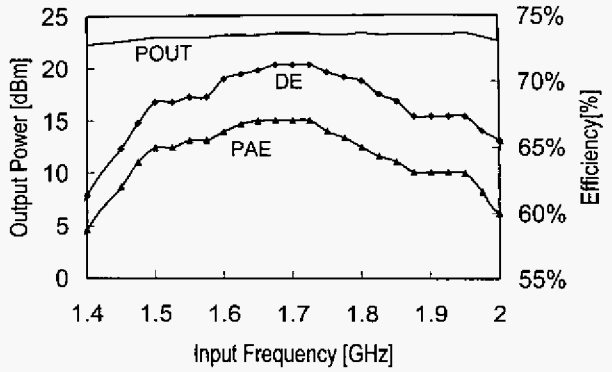

Fig. 7. Measured Output Power (Pout), PAE and Drain Efficiency (DE) versus frequency.

Acknowledgement

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