A Broadband 4.5–15.5-GHz SiGe Power Amplifier With 25.5-dBm Peak Saturated Output Power and 28.7% Maximum PAE

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***Abstract*—This paper presents the design of a broadband power amplifier (PA) in 130-nm SiGe BiCMOS technology. First, a single-stage broadband single-cell PA covering the 4.5–18-GHz frequency band is introduced. In this frequency range, this single cell achieves a measured gain, saturated output power ($P_{\rm sat}$), output 1-dB compression point ($P_{\rm 1dB}$), and power-added efficiency (PAE) in the range from 12.8 to 15.7 dB, 18.8 to 23.7 dBm, 16.7 to 19.5 dBm, and 11.4 to 31.9%, respectively. Its peak saturated output power and maximum PAE are both obtained at 8.5 GHz. Second, to increase the output power, a PA consisting of two parallel broadband cells with a power combination is presented. This PA operates in the 4.5–15.5-GHz frequency range with measured gain, $P_{\rm sat}$, $P_{\rm 1dB}$, and PAE in the range from 11 to 16.6 dB, 21.3 to 25.5 dBm, 18.7 to 21.7 dBm, and 11.9 to 28.7%, respectively. It achieves its peak saturated output power of 25.5 dBm at 8.5 GHz and its maximum PAE of 28.7% with an associated output power of 23.6 dBm at 6.5 GHz. Each of those two PAs achieves better performances than the state-of-the-art in broadband SiGe technology when comparing the output power level and efficiency.**

***Index Terms*—BiCMOS SiGe technology, broadband power amplifier (PA), integrated transformer, power combiner.**

I. Introduction

THE LAST developments of SiGe BiCMOS technologies provide the capability to be competitive with III–V compounds for applications over the S- to Ku-band frequency range [1]. SiGe technology offers the advantage of being low cost and having a high integration level. However, the main problem is achieving high RF power, due to the low breakdown voltages. In parallel, there is a strong need to develop power amplifiers (PAs) with high output power and high efficiency over a large frequency range, using low-power supply voltages. For wideband applications, [2] describes a multi-octave (2–18 GHz) distributed amplifier, which was fabricated using conventional thin-film microwave integrated circuit (MIC) technology. That PA achieves a gain level above 26 dB, an output power of 25 dBm, and an average power-added efficiency (PAE) of 27%. The HMC451 from Hittite is a GaAs monolithic microwave integrated circuit (MMIC) pseudomorphic HEMT (pHEMT) PA, which operates between 5 and 20 GHz [3]. This amplifier provides 18–22 dB of gain and up to 23 dBm of saturated output power ($P_{\rm sat}$). The GaN PA reported in [4] achieves 40 dBm of $P_{\rm sat}$, 38% of peak PAE, and 12 dB of gain. All these demonstrators or products are fabricated with III–V technologies, which are high cost and require high voltage supplies (from 5 to 40 V). With SiGe technology and for narrowband application [2 GHz of bandwidth (BW)], a 10-GHz SiGe PA described in [5] typically achieves 29.3 dBm of output power, 18% of PAE, and 13.5 dB of gain, using 4.5 mm^2 of area. Reference [6] also introduces a narrowband differential two-stage amplifier operating in the 11–13-GHz frequency range with 21.2 dB of gain, 23.4 dBm of output power, and 25%–37.3% of PAE. For wideband applications, [7] introduces a transformer-based 75 GHz-f_T SiGe PA operating in the 7–18-GHz frequency band with 17.5 dBm of $P_{\rm sat}$, 10.1% of PAE, and 15 dB of gain using 0.72 mm^2 of area. Reference [8] describes a distributed PA operating over 1–15 GHz, with 16 dBm of output power, 10% of PAE, and 10 dB of gain, using 1.45 mm^2 of area. The distributed PA reported in [9] operates over 1–12 GHz, with 22.1% of PAE at 2 GHz and 12 dB of gain, using 2.1 mm^2 of die area. A broadband distributed CMOS PA achieving a $P_{\rm sat}$ as high as 19 dBm, a gain of 8.3 dB, and a peak PAE of 25% at about 5 GHz is demonstrated in [10]. In the 20.5–30-GHz frequency range, [11] shows a CMOS PA achieving a gain, maximum output power, and PAE of 15 dB, 17.5 dBm, and 10.1%, respectively. Reference [12] reports a 90-nm CMOS PA operating in the 5.2–13-GHz band with up to 25.2 dBm of $P_{\rm sat}$ and 21.6% of PAE. Finally, [13] presents a CMOS 45-nm silicon-on-insulator (SOI) PA providing up to 23.7 dBm of $P_{\rm sat}$ and 20.5% of PAE with a gain of 5–6 dB in the 6–26-GHz range.

The main challenge addressed in this paper is to deliver a high output power over a wide frequency band (4.5–15.5 GHz) with the low-cost BiCMOS9MW SiGe technology (f_T of 280 GHz) from STMicroelectronics [14]. Due

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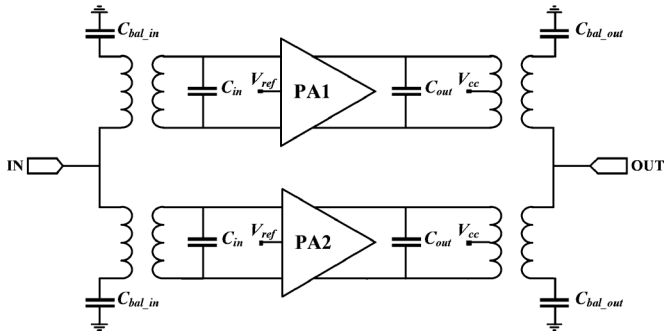

Fig. 1. Parallel differential PA with input splitter and output power combiner.

to the output power requirements, a PA architecture has been designed with a cascode topology, a differential structure, two power cells in parallel, and a broadband low-loss power combiner. With the proposed configuration, the output combiner is able to preserve the signal magnitude and phase while introducing less than 2.3 dB of losses over the 2–18-GHz frequency range. The large BW PA delivers up to 25.5 dBm of peak output power and 28.7% of maximum PAE. The SiGe die area of the PA using two cells in parallel is 1.96 mm^2 (including the pads). Compared to broadband SiGe PA reported in literature, the proposed transformer-based PA provides higher saturated output power and PAE.

II. Broadband PA Architecture

The PA structure is based on a parallel topology, where the power combination is realized through a power combiner, as illustrated in Fig. 1. The PA combines two differential PAs in parallel to achieve both high output power and good linearity performance. This structure is composed of input and output broadband transformers associated with techniques for current splitting at the input and current combining at the output. This intrinsically provides a large frequency range conversion mode (single-to-differential and differential-to-single) and impedance transformation. This power-combination technique allows to achieve a saturated output power in SiGe technology in the range of 21.3–25.5 dBm in the 4.5–15.5-GHz frequency band with a PAE of 11.9 to 28%. This is an improvement compared to [9] reporting the highest performances found in literature for a broadband SiGe PA. This PA operates over 1–12 GHz with a PAE in the range of 10.3%–22.1% for an output 1-dB compression point ($P_{1\mathrm{dB}}$) between 16.2 to 19.5 dBm.

For each differential power cell (PA1 and PA2 in Fig. 1), class-AB operation is preferred since this specific application provides the best tradeoff between output power and efficiency. The input and output of those cells are based on transformers providing balanced-to-unbalanced transformation, impedance matching, and dc biasing [11], [15]. Regarding passive components, the back-end of the six-metal layer technology (+Alucap) is well adapted for high currents since it contains two thick metal levels far from the silicon substrate. The design of wideband transformer-based matching networks is described in Section III-C. The on-chip power combiner structure will be adapted from loop inductors to constitute the different primary windings and the secondary winding. Its design will focus on transformer sizing for power combining integrated into a bandpass network.

TABLE I
BiCMOS9MW Extrinsic Transistor Parameters for $L_E = 15\ \mu$m and $N_{BE} = 5$

	W_E (μm)	NPN	J_C@peak f_T (mA/μm²)	BV_{CE0} (I_b = 0A) (V)	BV_{CB0} (V)	f_T (GHz)	f_{max} (GHz)
BiCMOS9MW SiGe:C 0.13 μm	0.27	MV	1.5	2	7.5	150	280
		HS	7.5	1.6	5.5	230	280

III. BiCMOS SiGe Broadband Single Power Cell

A. Power Transistor

The BiCMOS9MW design kit from STMicroelectronics provides two NPN transistors compared in Table I. In order to choose the suitable SiGe power transistor (medium voltage: MV or high speed: HS), each transistor is considered.

For both transistors, a multi-finger NPN transistor configuration is used to increase the maximum collector current I_c given by

$$I_C = J_C \times W_E \times L_E \times N_{BE} \tag{1}$$

where J_c is the current density, W_E and L_E are the emitter finger width and length, respectively, and N_{BE} is the number of emitter fingers. To avoid the self-heating effect, a ballast on the emitter fingers is used.

Transistor supply voltages are limited by the breakdown voltages BV_{CB0} and BV_{CE0} (given for $I_b = 0A$). If the transistor base is driven by a low source impedance, the breakdown voltage BV_{CE} increases and a higher supply voltage V_{cc} can be used.

The MV transistor allows a relatively high V_{cc} given by

$$V_{cc\_\mathrm{typ}} = 4\ \mathrm{V} < V_{cc} < V_{cc\_\mathrm{max}} = 7.5\ \mathrm{V}. \tag{2}$$

Compared to the MV transistor, the HS transistor allows a slightly lower supply voltage given by

$$V_{cc\_\mathrm{typ}} = 3.2\ \mathrm{V} < V_{cc} < V_{cc\_\mathrm{max}} = 5.5\ \mathrm{V}. \tag{3}$$

In Fig. 2, the f_T and $f_{\max}$ of the intrinsic MV and HS transistors are compared versus the collector current I_c. It can be observed that the MV transistor allows a relatively low density current at its peak f_T of $J_c = 1.5$ mA/μm^2 while the HS transistor allows a much higher density current at its peak f_T of $J_c = 7.5$ mA/μm^2.

Compared to the MV transistor, the HS transistor provides gain at high frequency with a much higher collector current for a slightly lower supply voltage. Therefore, for PA design, the HS transistor is more suitable to achieve high output power at high frequencies. It is selected for the design of the proposed broadband PA.

The transistors T_1 and T_3 in Fig. 3 are built with $N_{BE} = 5$ fingers of $L_E = 15\ \mu$m length. They are biased in class AB with collector currents $I_{c1} = I_{c3} = 19$ mA to achieve a low quiescent consumption while achieving a high gain (Fig. 2). For

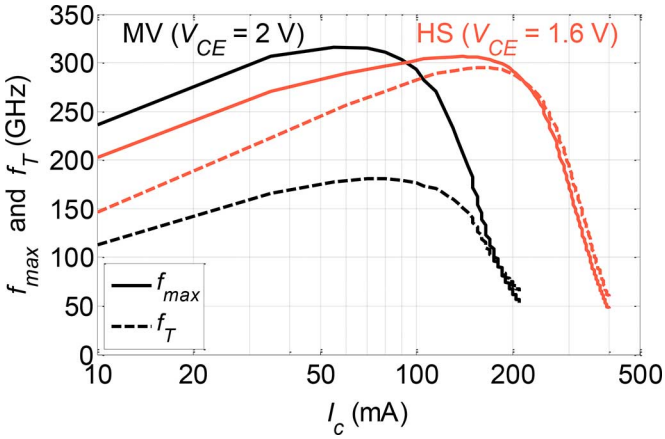

Fig. 2. $f_{\max}$ and f_T of the intrinsic MV and HS transistors versus collector current I_c for $L_E = 15$ μm, $W_E = 0.27$ μm, $N_{BE} = 5$.

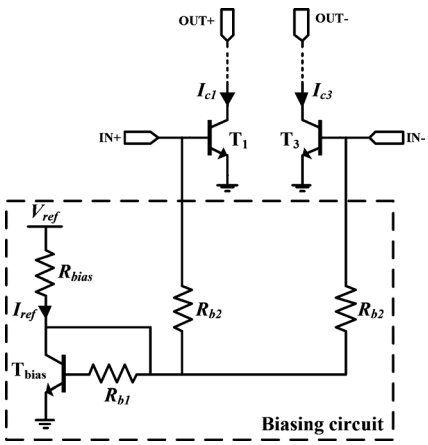

Fig. 3. On-chip biasing circuit of the power cell.

strong input signal, the two transistors will be able to drive I_c currents as high to about 200 mA with high gain (Fig. 2).

On-chip integrated active biases are used to provide an optimum condition for the power cell (Fig. 3). A current mirror biasing circuit is used on the transistor base to ensure reliability when delivering saturated output power. The differential PA consumes a total quiescent current I_c of 38 mA for a voltage supply *Vcc* of 3.6 V. The I_c current is the sum of the collector current (I_{c1} and I_{c3}). The I_{ref} current is adjusted by the 400-ΩR_{bias} resistor. To reduce the consumption of the bias circuit, a current ratio greater than one is selected. This ratio is applied to size the transistors with a T_{bias} emitter area of 4 μm^2 and T_1 and T_3 areas of 20 μm^2. The base resistors R_{b1} and R_{b2} are 1000 and 200 Ω, respectively.

B. Input and Output Transformers

Special attention must be paid to the input and output transformers. They must provide a broadband impedance matching and balanced-to-unbalanced mode conversion while occupying a small silicon area. The transformer designs are achieved as follows.

1) Determination of the optimal transistor input and output impedances over the frequency range of interest using a source– and load–pull simulation.

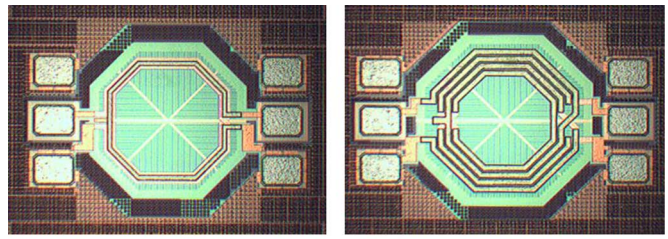

Fig. 4. Fabricated: (a) input and (b) output transformers.

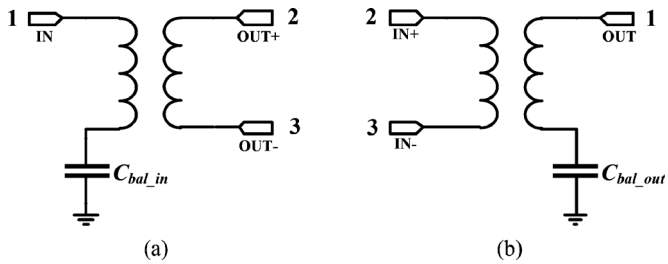

Fig. 5. (a) Input and (b) output transformers with $C_{\text{bal\_in}}$ and $C_{\text{bal\_out}}$ transformer imbalance capacitances.

2) Synthesis of the input and output impedances using transformer equivalent circuits.
3) Determination of the transformers' geometric parameters based on fundamental equations [16].
4) Determination of the equivalent dielectric permittivity of consecutive dielectric levels of the technology stack [17] to efficiently employs an electromagnetic (EM) simulator such as Momentum from Keysight Technologies for verification of the transformer characteristics.
5) Comparison between simulations using the equivalent circuit and S-parameters obtained from EM simulation. If the achieved performances of the EM model are not satisfactory, return to 3).

In order to present the optimum input and output impedances to the parallel PAs over a large frequency range, the more appropriate transformer topology is selected (stacked or interleaved) and the k coupling coefficient of each transformer is adjusted. Reference [18] has demonstrated that a large coupling factor in an RF transformer is necessary to minimize attenuation and maximize the BW. Also, a patterned ground shield (PGS) is used to prevent from electric field leakage into the silicon substrate.

For the input transformer [see Fig. 4(a)], a stacked topology [19], [20] is adopted. Its primary presents two turns with a 255-μm outer diameter, 10-μmtrace width, and 3-μm line spacing. Its secondary presents one turn with 242-μm diameter and 10-μm trace width. The output transformer is formed by multi-turn coils in an interleaved configuration on the same metal level [see Fig. 4(b)]. Its primary uses two turns with a 302-μm outer diameter, 12-μm trace width, and 3-μm line spacing. Its secondary uses two turns with a 272-μm outer diameter, 12-μm trace width, and 3-μm line spacing.

Series capacitances $C_{\text{bal\_in}}$ and $C_{\text{bal\_out}}$ are, respectively, added in the primary of the input transformer [see Fig. 5(a)]

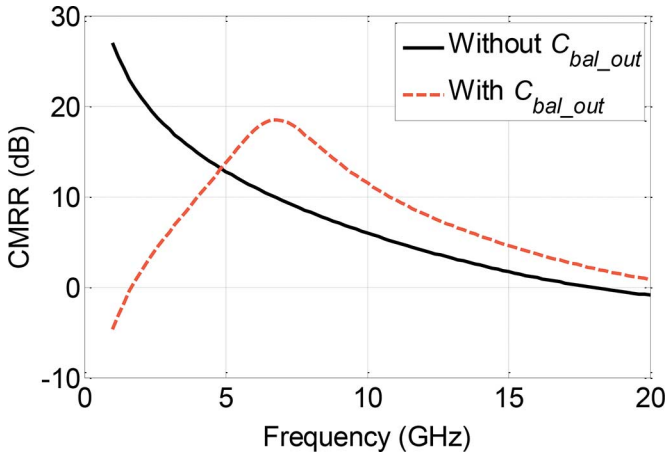

Fig. 6. Impact of the $C_{\mathrm{bal\_out}}$ capacitance on the output transformer CMRR.

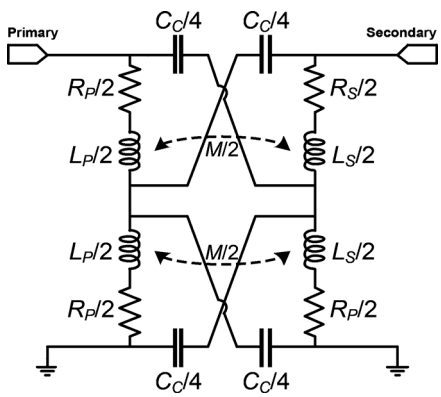

Fig. 7. Transformer equivalent circuit.

and in the secondary of the output transformer [see Fig. 5(b)] to improve the common mode rejection ratio (CMRR).

The CMRR is used to evaluate single-to-differential mode conversion performance. Those two capacitances compensate the transformers imbalance due to an asymmetry in electric field distribution for each coil [21]. The CMRR improvement calculated using S-parameters in (4) is illustrated in Fig. 6,

$$\mathrm{CMRR} = \left| \frac{S_{31} - S_{21}}{S_{21} + S_{31}} \right|. \tag{4}$$

Fig. 7 describes the transformer model with electrical parameters suitable in circuit computer-aided design (CAD) tools. This equivalent circuit is a simplified version of the model proposed in [16]. L_p and R_p are the primary inductance and resistance, L_s and R_s are the secondary inductance and resistance, M is the mutual inductance between the two conductors, k is the coupling coefficient, and C_c is the coupling capacitance between the primary and secondary coils. They are summarized in Table II.

To validate the simulation model of the transformers, the output and input transformers of the power cell were fabricated with open and short de-embedding elements to access their

TABLE II
TRANSFORMER ELECTRICAL PARAMETERS

Element	Input transformer			Output transformer		
	Meas.	EM Sim.	Model	Meas.	EM Sim.	Model
L_p (nH)	1.68	1.7	1.71	1.88	1.89	1.96
L_s (nH)	1.49	1.45	1.47	0.613	0.593	0.631
R_s(Ω)	0.83	0.95	1.09	1.1	1	1.09
R_p (Ω)	0.85	0.9	0.77	0.48	0.56	0.46
k	0.66	0.73	0.7	0.72	0.78	0.78
M (nH)	1.14	1.06	1.06	0.760	0.829	0.914
C_c (fF)	-	227	195	-	271	300

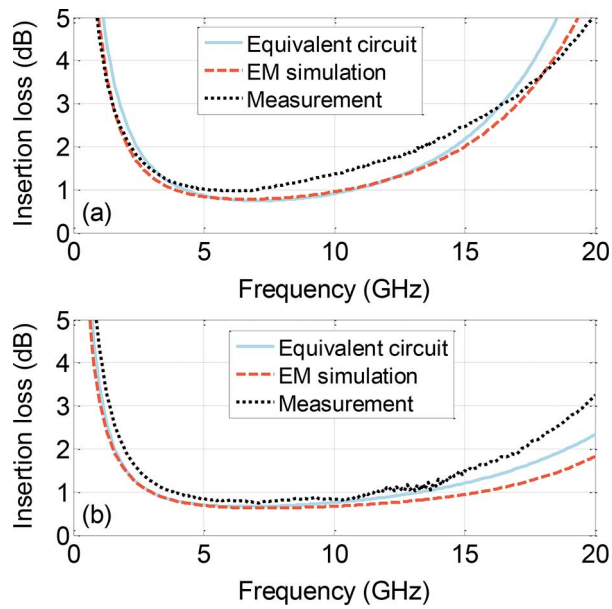

Fig. 8. Measured and simulated insertion loss of: (a) input and (b) output transformers.

intrinsic parameters. On-wafer S-parameter measurements were accomplished using an Agilent E8361A network analyzer covering frequencies up to 110 GHz, ground–signal–ground (GSG) probes ($|Z|$ probes from Cascade Microtech), and a through-reflect-line (TRL) calibration. Fig. 8 depicts the measured and simulated (using the equivalent model and also Momentum 2-D EM simulation tool) mixed-mode S-parameter results for both transformers between dc and 20 GHz. Good agreement is achieved for both differential and common-mode S-parameters over the entire frequency band. Insertion loss of the input and output transformers are in the range of 0.97 to 3.7 dB and 0.75 to 2.3 dB in the 4.5–18-GHz frequency range.

C. Power Cell Topology

The limited voltage swing available in advanced silicon devices is a critical issue to achieve high output power. To overcome this problem, one of the conventional strategies is to use a cascode topology allowing a higher supply voltages V_{cc} in the

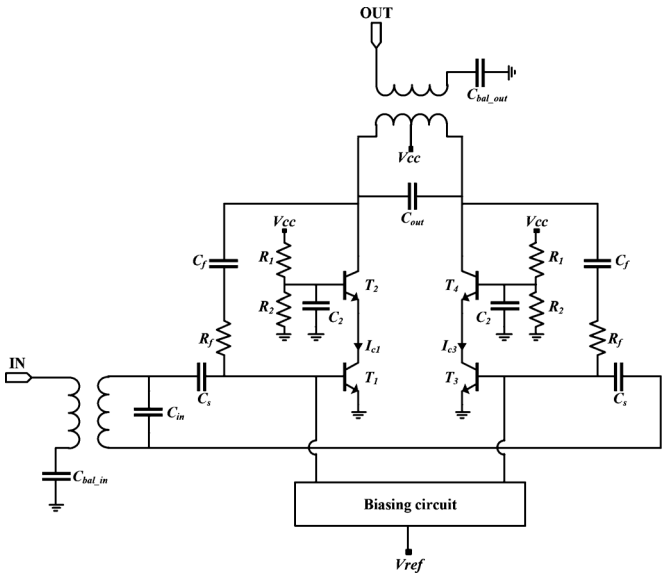

Fig. 9. Pseudo-differential cascode elementary cell in a feedback configuration.

TABLE III
PSEUDO-DIFFERENTIAL CASCODE CELL COMPONENTS

C_{in} (pF)	C_{bal_in} (pF)	C_f (pF)	C_1 (pF)	C_{out} (pF)	C_{bal_out} (pF)	C_s (pF)	R_f (Ω)	R_1 (kΩ)	R_2 (kΩ)
0.5	0.55	1.2	2	0.14	0.55	4	220	1	4

range of 3–5 V. Moreover, to reach higher output power, a differential structure is employed. Hence, the power cell is composed by two stacked transistors and the voltage swing is distributed across T_1 and T_2 on one side and T_3 and T_4 on the other side (Fig. 9).

Table III gives the component values of the pseudo-differential cascode elementary cell. At the output, the choke inductor is included as part of the transformer. The broadband power cell uses a feedback circuit (composed of R_f and C_f) between the input and output of the cascode power transistor to obtain a flat gain over the frequency band of interest. The feedback circuit consists of a resistor connected in series with a capacitive element to improve the broadband stability. Impedance-matching BWs of input and output transformers are improved using the C_{in} and C_{out} capacitors (Fig. 9). This topology also needs transistors with high *gm* transconductance, leading to a small transistor size.

D. Measurement Results

The chip micrograph of the fabricated single power cell is shown in Fig. 10. The pseudo-differential PA occupies an area of 1.2 mm × 0.6 mm (0.72 mm^2) including the pads. Four pads are used for dc biasing with $V_{\text{ref}} = 1.8$ V and $V_{cc} = 3.6$ V.

Table IV gives the dc biasing comparison between transistor models and measurement. The HICUM L0 model simulation gives a very good agreement with the current measurements.

1) Small-Signal Performances: The small-signal parameters of this fabricated broadband single-cell PA were measured on-wafer using GSG probes for RF input and output, dc probes

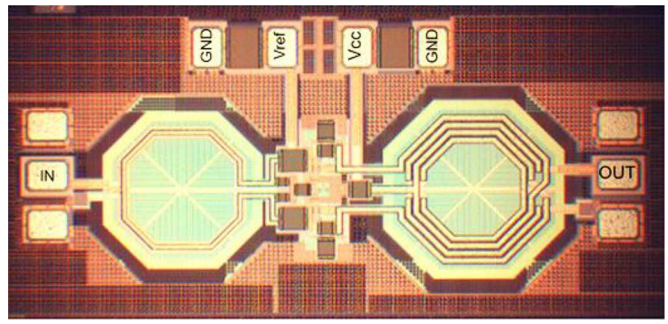

Fig. 10. Fabricated SiGe single power cell.

TABLE IV
SINGLE POWER CELL PA DC BIASING

Voltage supply	I[HICUM L2]	I[HICUM L0]	I[Meas.]
V_{ref} = 1.8V	2.3 mA	2.3 mA	2.2 mA
V_{cc} = 3.6V	45 mA	38 mA	38 mA

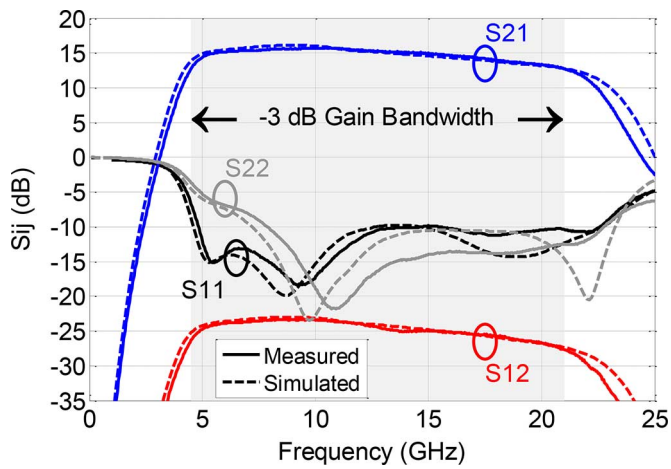

Fig. 11. Measured and simulated S-parameters of the single power cell PA.

for biasing, and a TRL calibration. Fig. 11 compares the simulated and measured S-parameters with a very good agreement between simulation and measurement results. This single power cell PA achieves a measured return loss ($S11$) better than −10 dB from 4.8 to 22.5 GHz (129%). The maximum measured gain ($S21$) is 15.7 dB with a −3-dB BW going from 4.5 to 21 GHz (129%). Over this frequency range, the isolation ($S12$) is better than 23 dB and the output return loss ($S22$) is better than −4 dB. On Fig. 12, the small-signal gain ($S21$) is reported. A thermally controlled chuck has been used to achieve this measurement. When the temperature changes from 70 °C to 100 °C, the measured maximum gain variation is 0.1 dB in the 4.8–19-GHz band.

2) Stability: The measured Edwards–Sinsky stability factor μ of the single power cell PA is illustrated on Fig. 13 for 70 °C and 100 °C. A good agreement is obtained with the simulated μ-factor. The unconditional stability ($\mu > 1$) [22] of the single-cell PA can be observed. From 70 °C to 100 °C, the μ-factor has a very small variation.

Before sending the layout in fabrication, the large-signal stability of this PA has been tested in simulation by the injection

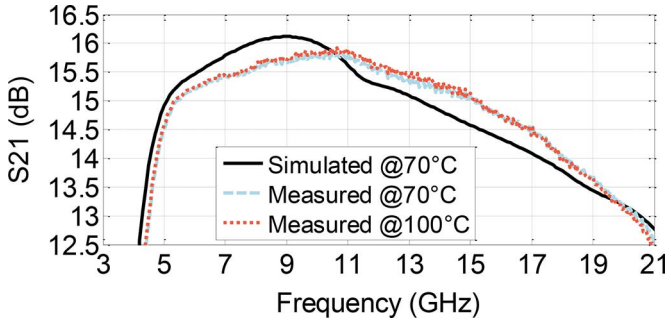

Fig. 12. Measured and simulated small-signal gain ($S21$) versus frequency at 70 °C and 100 °C.

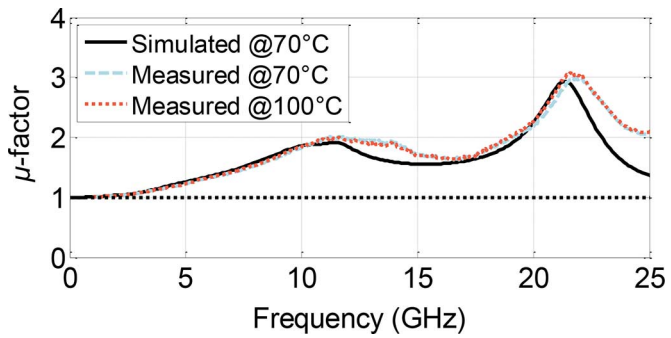

Fig. 13. Measured and simulated μ-factor versus frequency at 70 °C and 100 °C.

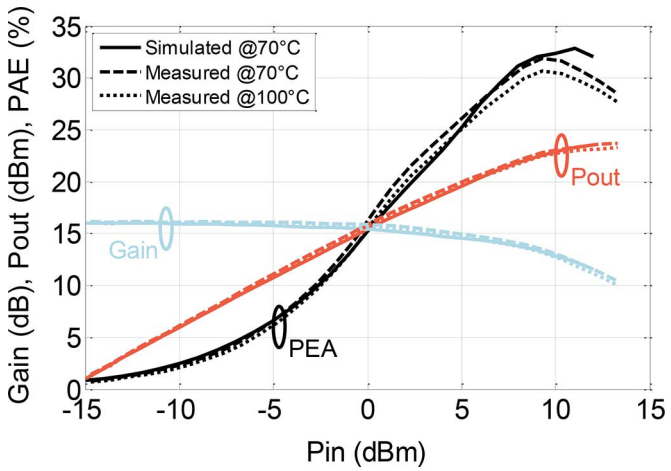

Fig. 14. Measured and simulated gain, Pout, and PAE of the single power cell PA at 8.5 GHz.

of short pulses on the dc supply connection [23]. The stabilization of the output signal following the pulses injection has been verified.

3) Large-Signal Performances: Large-signal performances has been measured on-wafer with GSG and dc probes and 50-Ω input and output loads. The measurement setup consists of an RF generator SMF100A from Rohde&Schwarz and an E4418B power meter from Agilent, both controlled by the Load–Pull Explorer software from Focus Microwave. The simulated and measured large-signal results are compared at 8.5 GHz for temperatures of 70 and 100°C on Fig. 14. This figure shows a very good agreement between measurement and simulation results. Between 70 °C and 100 °C, the maximum gain, $P_{\rm sat}$, and PAE decreases from 16.14 to 16.07 dB, 23.72 to 23.27 dB, and 31.86% to 30.64%, respectively.

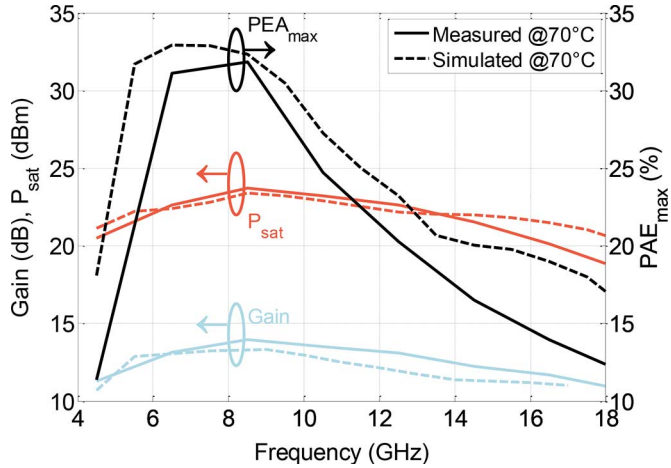

Fig. 15. Measured and simulated small-signal gain, $P_{\rm sat}$ and maximum PAE of the single power cell PA versus frequency.

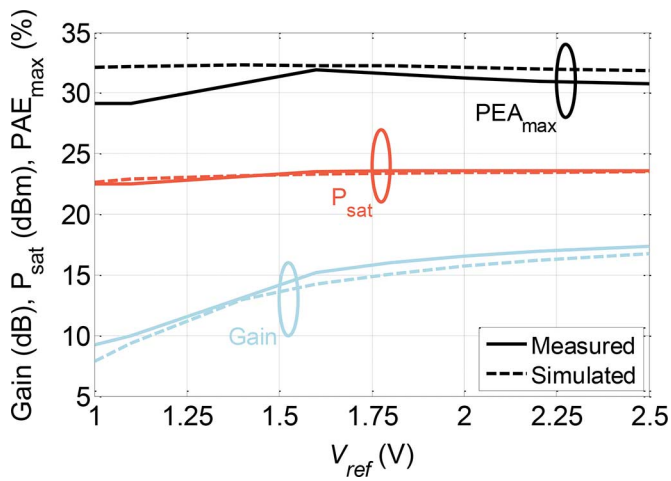

Fig. 16. Measured (solid lines) and simulated (dashed lines) small-signal gain, $P_{\rm sat}$, and maximum PAE of the single power cell PA versus $V_{\rm ref}$ at 8.5 GHz and 70 °C with $V_{cc} = 3.6$ V.

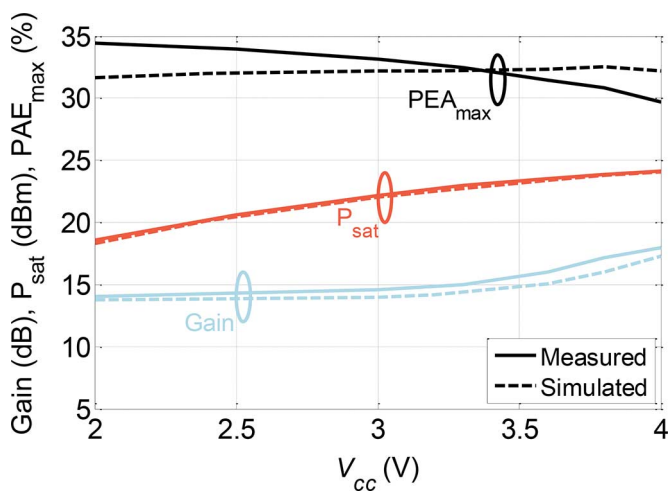

Fig. 17. Measured (solid lines) and simulated (dashed lines) small-signal gain, $P_{\rm sat}$, and maximum PAE of the single power cell PA versus V_{cc} at 8.5 GHz and 70 °C with $V_{\rm ref} = 1.8$ V.

Fig. 15 shows that the single-cell PA achieves in the 4.5–18-GHz band a saturated output power and a PAE in the range of 18.8–23.7 dBm and 11.4%–31.9%, respectively.

TABLE V
TWO-PARALLEL-CELL PA COMPONENT VALUES

C_{in} (pF)	C_{bal_in} (pF)	C_f (pF)	C_1 (pF)	C_{out} (pF)	C_{bal_out} (pF)	C_s (pF)	R_f (Ω)	R_1 (kΩ)	R_2 (kΩ)
0.6	0.8	1.2	2	0.18	0.5	4	250	1	4

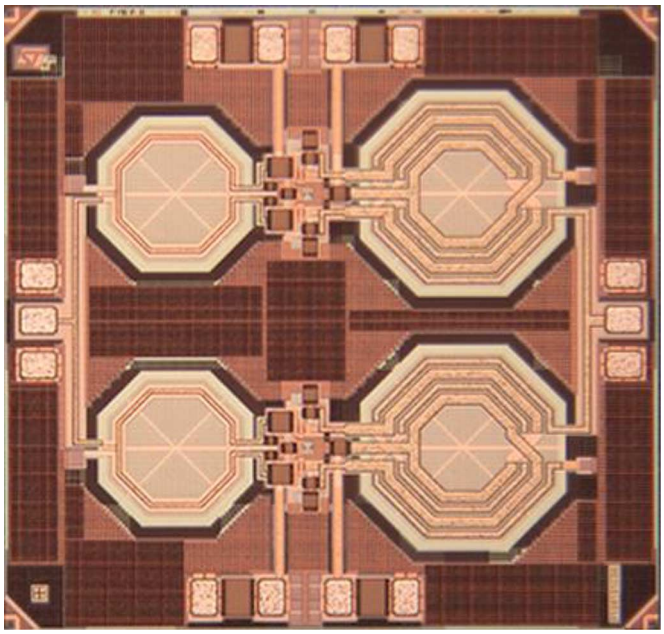

Fig. 18. Broadband BiCMOS SiGe two-parallel-cell PA (1.44 mm × 1.36 mm).

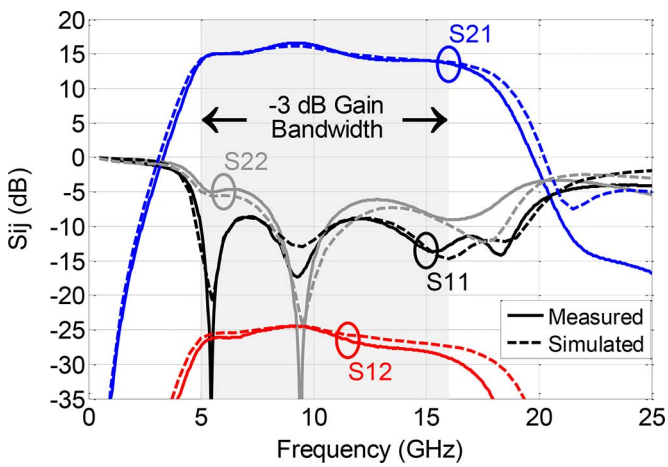

Fig. 19. Measured and simulated S-parameters of the two-parallel-cell PA.

4) Performances Versus Supply Voltages: The small-signal gain, $P_{\rm sat}$, and PAE at 8.5 GHz versus the $V_{\rm ref}$ and V_{cc} supply voltage are illustrated in Figs. 16 and 17, respectively. Both figures shows a good agreement between simulation and measurement.

$V_{\rm ref}$ mostly impacts the small-signal gain while the maximum PAE and $P_{\rm sat}$ are relatively constant. A $V_{\rm ref}$ of 1.8 V represents a good compromise between the achieved gain and quiescent consumption.

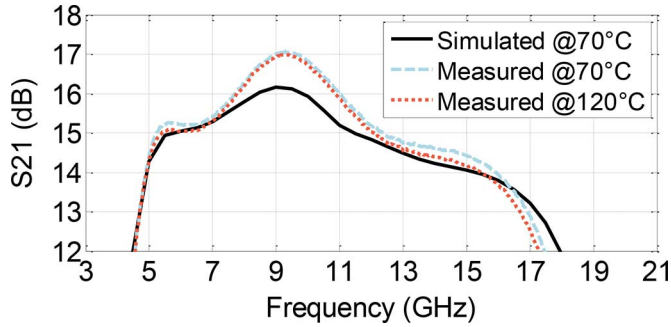

Fig. 20. Measured and simulated small-signal gain ($S21$) versus frequency at 70 °C and 120 °C.

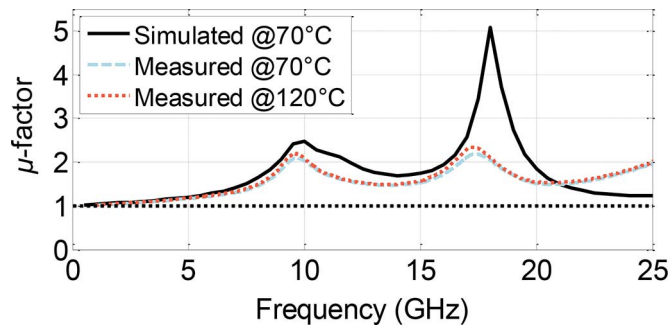

Fig. 21. Measured and simulated μ-factor versus frequency at 70 °C and 120 °C.

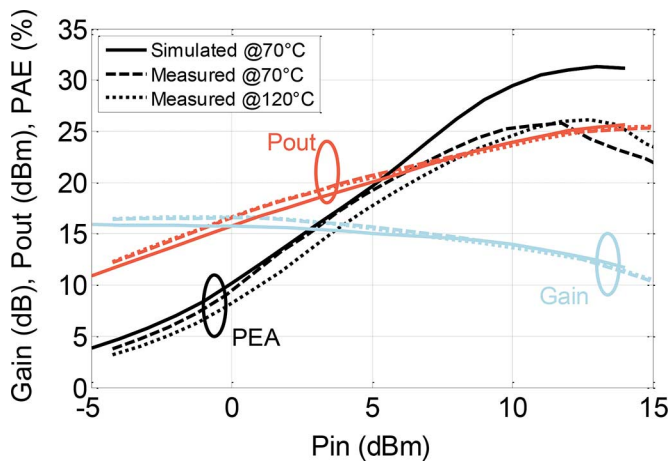

Fig. 22. Measured and simulated gain, Pout, and PAE of the two-parallel-cell PA at 8.5 GHz.

V_{cc} has a small impact on the PAE, but increases the gain and $P_{\rm sat}$. A V_{cc} of 3.6 V is selected to offer a good compromise between the achieved $P_{\rm sat}$ and gain and the PA reliability.

These results validate the modeling of the active and passive elements and demonstrate the capability of the BiCMOS SiGe to achieve a broadband power cell.

IV. BROADBAND TWO-PARALLEL-CELL PA

In this section, in order to increase the output power, the combination of two of the broadband power cells is described to target a minimum of 10% PAE over the 4.5–15.5-GHz frequency range.

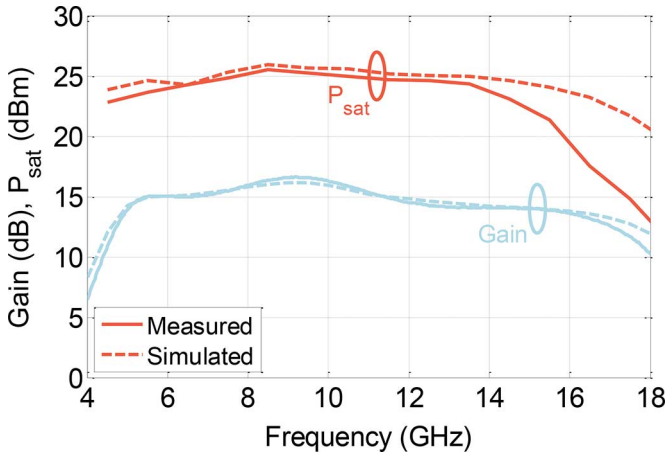

Fig. 23. Measured and simulated saturated output power and small-signal gain of two-parallel-cell PA.

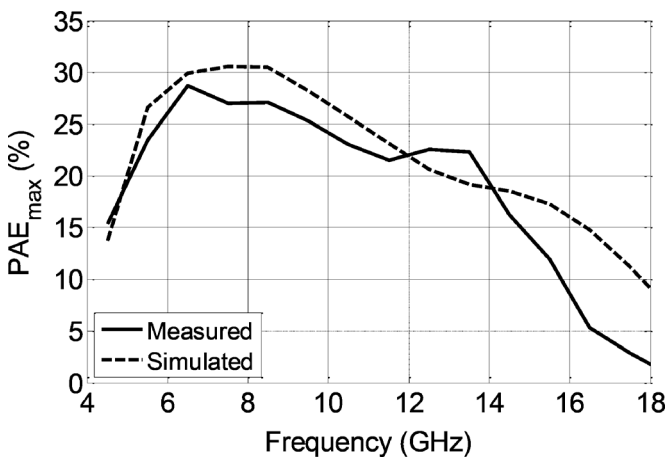

Fig. 24. Measured and simulated maximum PAE of two-parallel-cell PA.

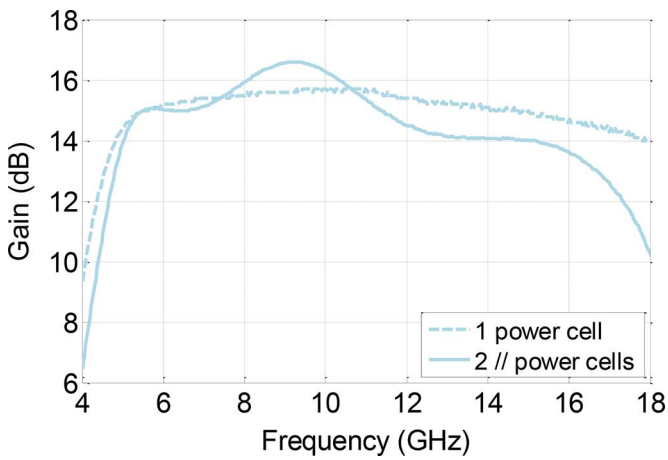

Fig. 25. Measured small-signal gain comparison between single-cell and two-parallel-cell PA.

Fig. 1 shows the schematic of the broadband PA composed of two power cells in parallel. The input power splitting and output power combining are achieved using T-combiners. This implementation requires the redesign of the transformers to achieve the 50-Ω input and output matching. This parallel architecture needs a new configuration of element values for each parallel power cell. Based on Fig. 9, the new component values are given in Table V.

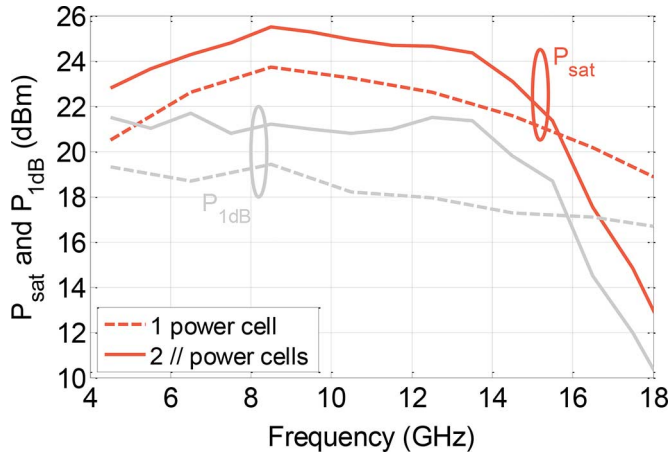

Fig. 26. Measured saturated output power $P_{\rm sat}$ and $P_{\rm 1dB}$ comparison between single-cell and two-parallel-cell PA.

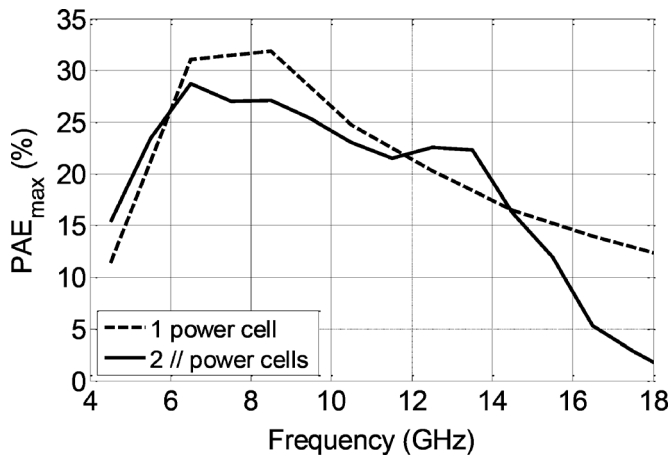

Fig. 27. Measured maximum PAE comparison between a single-cell and two-parallel-cell PA.

TABLE VI
COMPARISON OF THE ACHIEVED MEASURED PROPERTIES FOR A SINGLE-POWER CELL AND TWO-PARALLEL CELLS AT 8.5 GHz

8.5 GHz	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE max (%)
single cell PA	15.6	23.7	19.5	31.9
2-parallel cell PA	16.5	25.5	21.2	27.1

A current mirror biasing circuit (Fig. 3) has been used on each parallel power cells to provide an optimum condition for the power device as function of temperature and output power. The biasing circuit achieves a 2.3-mA quiescent current ($I_{\rm ref1} = I_{\rm ref2}$) under 1.8-V bias voltage ($V_{\rm ref1} = V_{\rm ref2}$) for each power cell. Each cascode has a quiescent current of 19 mA for a 3.6-V dc supply.

Fig. 18 shows the chip micrograph of the BiCMOS SiGe broadband two-parallel power cell PA. It occupies an area of 1.44 mm × 1.36 mm (1.96 mm^2) including the RF and dc pads.

1) Small-Signal Performances: The simulated and measured S-parameters of the two-parallel-cell PA are shown in Fig. 19.

The measurement is achieved on-wafer using GSG probes for RF input and output, dc probes for biasing, and a TRL calibration. A good agreement between measured and simulated results

TABLE VII
COMPARISON OF INTEGRATED BROADBAND SiGe, CMOS, AND III–V PAs

Reference	Technology	Frequency (GHz)	Gain (dB)	P_{sat} (dBm) Min/Max	P_{1dB} (dBm) Min/Max	PAE (%) Min/Max	Supply (V)	Chip area (mm²)
This work (1 cell)	**SiGe 0.13 µm**	**4.5-18**	**12.8-15.7**	**18.8 / 23.7**	**16.7 / 19.5**	**11.4 / 31.9**	**3.6**	**0.7**
This work (2 parallel cells)	**SiGe 0.13 µm**	**4.5-15.5**	**11-16.6**	**21.3 / 25.5**	**18.7 / 21.7**	**11.9 / 28.7**	**3.6**	**1.96**
[7]	SiGe 0.35 µm	7-18	15	- / 17.5	- / -	- / 10.1	2.4	0.72
[8]	SiGe 0.25 µm	1-15	9.5 ± 0.5	- / 16.2	12 / 14	9.9 / 13.8	4.1	1.45
[9]	SiGe 0.25 µm	1-12	11 ± 1	- / -	16.2 / 19.5	10.3 / 22.1	2.6	2.1
[25]	SiGe 0.25 µm	2-12	9 ± 0.5	- / 16	13 / 14	6.5 / 9.5	5	1.16
[26]	SiGe 0.13 µm	1-110	10 ± 3	- / 17.5	- / 16.7	- / 13.2	3	2.18
[10]	CMOS 0.18 µm	3.7-8.8	8.3	16 / 19	13 / 15.6	7 / 25	-	2.8
[11]	CMOS 0.13 µm	20.5-31	8.4	10.7† / 13	- / -	1.4† / 13.2	1.5	1
[12]	CMOS 90 nm	5.2 - 13	15.5-18.5	18.5 / 25.2	14 / 22.6	6 / 21.6	2.8	0.7*
[13]	CMOS 45 nm SOI	6 - 26	5-6	17.6 / 21.7	12.9 / 18.5	8 / 20.5	4.5	0.52
			-	18.6 / 23.7	10.5 / 19.2	4.8 / 17.5	5.4	
[3]	GaAs	5-20	18-22	20 / 23	19 / 21	24	5	1.61
[4]	GaN 0.25 µm	2-18	12	38 / 42.2	36 / 39	10 / 39	30-40	15.34

†graphically estimated
*core area

is obtained. The −3-dB gain BW is achieved from 5 to 16 GHz (104%). In the 4.5–15.5-GHz band, a measured gain, input and output reflection coefficients, and isolation of better than 11 dB, −5, −2.3, and 24.4 dB are achieved, respectively. In Fig. 20, the measured small-signal gain ($S21$) is reported at 70 °C and 120 °C. The measured maximum gain variation over temperature is 0.2 dB in the 4.5–15.5-GHz band.

2) Stability: The μ-factor of the two-parallel-cell PA is illustrated in Fig. 21 for 70 °C and 120 °C. The unconditional stability of the design can be observed. From 70 °C to 120 °C, the μ-factor has a very small variation. For this two-parallel PA, the large-signal stability has also been tested in simulations before fabrication.

3) Large-Signal Performances: Fig. 22 shows the measured and simulated gain, output power (Pout), and PAE in function of the input power (Pin) at 8.5 GHz for temperatures of 70 °C and 120 °C. The laboratory setup described for the characterization of the single power cell PA section is also used. This figure shows a good agreement between measurement and simulation results. Between 70 °C and 120 °C, the maximum gain, Pout, and PAE increase from 16.52 to 16.64 dB, 25.3 to 25.5 dB, and 25.84% to 26.1%, respectively.

Figs. 23 and 24 depict the measured and simulated small-signal gain, $P_{\rm sat}$ and maximum PAE over 4.5–18 GHz. A fair agreement is obtained between simulated and measured results. In the band of interest (4.5–15.5 GHz), a measured small-signal gain, $P_{\rm sat}$ and PAE of 11.0–16.6 dB, 21.3–25.5 dBm, and 11.9%–28.7% are obtained, respectively. The maximum peak output power of 25.5 dBm and peak PAE of 28.7% are achieved at 8.5 and 6.5 GHz, respectively.

V. DISCUSSIONS

A. Single-Cell and Two-Parallel-Cell PA Comparison

Figs. 25–27 compare the measured small-signal gain, the saturated output power, and the PAE for a single power cell and two-parallel power cells. It can be observed that there is no significant difference in gain as it could be expected. Also, using two-parallel power cells, the output power is increased by a mean value of 2 dB over the 4.5–15.5-GHz frequency range. However, this improvement is obtained at the cost of a decrease by about a few percent in PAE.

Table VI summarizes the measured results at 8.5 GHz. At this frequency, compared to the single-cell PA, the two-parallel-cell PA saturated output power is enhanced by 1.8 dB, while its maximum PAE is decreased by 4.8%.

Table VII compares the proposed PA with other broadband SiGe, CMOS, and III–V PAs reported in the literature.

Compared to [9] presenting a broadband SiGe PA, the single-cell PA achieves at higher frequency a similar $P_{\rm 1dB}$ for a higher gain and PAE with a significantly reduced size. The two-parallel-cell PA also provides a saturated output power that is higher than the state-of-the-art in the broadband SiGe PA.

When comparing with CMOS technology, the proposed single-cell PA achieves better gain, $P_{\rm sat}$, and PAE for a similar area than the 45-nm SOI PA reported in [13]. The two-parallel PA also has an equivalent gain and $P_{\rm sat}$ than the 90-nm CMOS PA introduced in [12], but it operates over a larger BW and provides a better PAE.

The proposed SiGe PA provides good performances comparable to commercialized GaAs medium output power PA [3] for

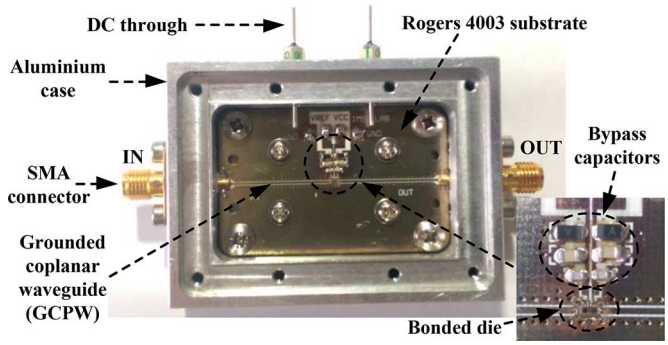

Fig. 28. Packaged single-power-cell PA die.

a lower supply voltage. This work in SiGe technology represents an alternative solution to III–V-based PAs. It allows to avoid using a costly system-in-package (SiP) scheme to design a low-cost fully integrated system-on-chip (SoC) requiring medium output power.

B. Die Bonding

The proposed PA can be implemented in a low-cost integrated transceiver as one of the advantages of the SiGe HBT technology is its compatibility with CMOS to achieve low-cost integrated systems.

This PA can also be used in standalone. To achieve high performances, the PA die must be bonded using a thermally conductive adhesive or eutectic soldering on a highly thermally conductive base (usually copper) attached to a heat sink. The RF input and output pads can be wire bonded using either a ball or wedge bonder to a printed circuit board (PCB). For higher RF performances, the wire bond must be as short as possible to avoid parasitic effect. The PCB input and output transmission lines should be placed as close to the die as possible to minimize bond wire length. Therefore, the base must be designed such that the surface of the die is coplanar with the surface of the PCB substrate [3]. To minimize parasitic inductance, a ribbon instead of a wire can be used to connect the RF pads. Ribbon bonding with rectangle-shaped wire provide lower inductive and impedance at higher frequency than round wire [24]. Fig. 28 shows a single-cell PA die (Fig. 10) bonded using thermally conductive glue to a copper base and bonded to a 254-μm-thick Rogers 4003 PCB. The dc and RF pads are wire bonded using a 23-μm-diameter wire. Surface mount bypass capacitors are used to shunt noise and other high-frequency interference to ground.

VI. Conclusion

Theoretical, simulated, and experimental studies of two SiGe fully integrated PAs, based on a single cell and two cells in parallel, have been presented in this paper. The single-cell PA achieves a measured gain, saturated output power, and PAE in the range from 12.8 to 15.7 dB, 18.8 to 23.7 dBm, and 11.4% to 31.9% over the 4.5–18-GHz frequency band for a die area of only 0.7 mm^2. To achieve a higher output power, a PA combining two cells in parallel is reported. It achieves a similar measured gain, saturated output power, and PAE in the range from 11 to 16.6 dB, 21.3 to 25.5 dBm, and 11.9% to 28.7% over the 4.5–15.5-GHz band for a die area of 1.96 mm^2. Compared to medium-power SiGe-based broadband PAs found in the literature, these achieved results show a significant improvement in terms of gain, maximum output power, and PAE. In circumstances where medium power is desired, such as for radar transmit/receive (TR) modules, these proposed broadband SiGe PAs represent a low-cost alternative solution to integrated PAs using III–V technologies.

Acknowledgment

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