24.4 An EDGE/GSM Quad-Band CMOS Power Amplifier

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Although Si CMOS PAs for mobile applications have demonstrated specification-compliant performance over the last several years, Si CMOS has not been widely employed in cellular PA applications due to certain inferior properties of its power capability, PAE, and breakdown to its counterparts such as GaAs and SiGe BJTs [1]. However, research conducted in the past decade has enabled commercially available cellular switching CMOS PAs for constant envelope modulation such as GSM applications [2,3]. This successful implementation of a GSM PA called forth a demand for a combination of linear EDGE operation with GSM operation in order to increase data rate up to 384kb/s while using legacy infrastructures [1,4]. The challenges of implementation of a dual-mode CMOS PA arise from required linearity for high peak-to-average-power ratio, which forces the PA to operate at power back-off from the P_{1dB} and results in inevitable low efficiency. Although a CMOS EDGE/GSM PA was reported in the past, the application was intended for Class-E3 operation [5]. The presented PA is an EDGE/GSM dual-mode, quad-band CMOS cellular application PA satisfying the requirement for power Class-E2 operation [4].

A CMOS quad-band RF PA module (PAM) for wireless GSM/EDGE applications has been designed with two integrated passive devices (IPDs) on a high-resistivity Si substrate. Figure 24.4.1 shows the schematic diagram of the two-stage PAs with IPD-based transformers. The PA IC comprises two RF PAs for the low-band (GSM850/EGSM) and the high-band (DCS/PCS), a programmable power LDO shared by both paths, two LDOs for the driver stages, an RF power controller, four reference voltage (Vref) generators for adaptive bias circuitry (ABC) of the driver and power stages for both bands, and two input baluns in a substrate. Three and two parallel units of power stages for both bands, respectively, are combined by parallel combining transformers (PCTs) for efficient power transfer and impedance transformation using Samsung's proprietary IPD technology, which is well described in [3].

The differential driver and power stages are designed in a cascode topology to prevent excessive voltage stress on the devices for a supply voltage up to 4.5V. Each power stage depicted in Fig. 24.4.2 is a stack of 0.4μm thick-oxide transistors and 0.18μm thin-oxide transistors with parallel-capacitive feedback. The driver stage with a differential inductor load has the same structure as the power stage, and is connected to the power stage through an inter-stage matching network.

In a CMOS linear PA, AM-PM distortion is caused by the gate-drain capacitance (C_{gd}) as well as the gate-source capacitance (C_{gs}) when the input signal is large enough to constantly turn devices on and off. This work is focused on reducing the nonlinearity of C_{gd} in the CG stage since the signal is largest at the output node, which periodically puts the CG stage into the triode and saturation regions. For a normal differential cascode amplifier, the gate of its common-gate (CG) stage is virtually grounded due to its generic differential nature. Therefore, C_{gd} seen from the output node is C_{gd} itself and is highly nonlinear in a high power range. To prevent the gate node of the CG stage from a virtual ground, the transistor M5 is turned off for linear mode, and MIM capacitances C1 and C2 (less than 1pF) are added to the gate as shown in Fig. 24.4.2. The effective capacitance seen from the output is a series capacitance of C_{gd} and C1, which is much more linear than C_{gd}. As a result, the AM-PM distortion in a high output power range can remarkably decrease.

To reduce AM-AM distortion and power back-off from the P_{1dB} for EDGE application, an ABC is proposed. The ABC boosts up the dc bias voltage to the gate of the CS stage as the input signal increases, thus increasing the PAE for a given linearity requirement. As shown in Fig. 24.4.3, the presented ABC consists of two diode-connected NMOS transistors in series connected between a reference voltage (Vref) and ground, respectively. The dc bias of Vbias is determined by the sizes of diodes and Vref when the RF input signal is small enough or not applied. When the RF signal is large enough to turn off the Mu and Md, it begins operation in the same way as a charge pump in a PLL. For the lower half cycle of the RF signal, the upper transistor, Mu, charges C_{gs} of the CS stage in the amplifier, while Md is turned off. For the upper half cycle, Md discharges C_{gs}, while Mu is turned off. If the size of Mu is larger than that of Md, Vbias will increase as the RF signal level increases, since the charging current is larger than the discharging one. Carefully optimizing the size of Mu and Md, and Vref controls the dc level of Vbias in the low power range and the increasing slope in high power operation. It should be noted that the sizes of Mu and Md are carefully chosen so that the ABC consumes under 0.5mA at an output power of 28.5dBm for each branch.

In order to minimize the performance variation from environmental change such as PVT, the Vref voltage that is used to set the dc operating point of the ABC is produced from the circuit depicted in Fig. 24.4.3. The circuit is comprised of a replica of the ABC, a replica of the CS stage in the amplifier, a current mirror, and an op-amp. A PTAT current, I_{ptat}, is supplied as the reference current to reduce the gain variation depending on temperature. The width of the CS stage in the main amplifier is M times that of the replica, while the replica of the ABC is the same size as that of the original. Therefore, Vref can be determined and supplied to each ABC such that the dc current in the power stage, I_{PA}, is calculated as $M \times N \times I_{ptat}$. The values of R1 and R2 are carefully chosen because of the channel-length modulation effect of the PMOS current mirror and the replica of the CS stage. Another noteworthy point of the design of the block is bandwidth. The bandwidth has to be optimized between the factors of RX band noise and AM bandwidth.

In the GSM mode of Class-E PA operation, it is required to control the output power from the PA with a dynamic range of more than 30dB and a tolerance of ±2dB. In this work, the power control scheme is implemented using gate voltage control of the driver stage and closed-loop current control of the power stage. As shown in Fig. 24.4.4, two different Vramp shaping circuits with a temperature compensation feature are used for the driver and power stages to have a gentle slope of power output versus Vramp. In the power stage control, the current through the power PMOS is sensed by a replica of the PMOS and a resistive component to be compared with the output of the power cell control shaped Vramp signal. The result of the comparison, which is the error amplifier output, goes to the gate of the power amplifier core cell and adjusts the current from the power PMOS.

The active IC is implemented in a 0.18μm CMOS technology. Measured RF performance for low-band is shown in Fig. 24.4.5. The right figure is the output power and PAE for GSM mode, and the other is for EDGE mode. Figure 24.4.6 gives a summary of PAM performance. The measured PAM efficiency is 23% in EDGE mode and 48 to 55% in GSM mode depending on the band. The receiver Band noise with a 100kHz RBW at 20MHz offset is -82 and -86dBm for GSM and EDGE modes, respectively. Figure 24.4.7 shows the micrograph of the PAM with the transformers assembled in a 32-pin QFN package.

References:

[1] H. S. Bennett, et al., "Device and Technology Evolution for Si-Based RF Integrated Circuits," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp.1235-1258, July 2005.

[2] I. Aoki, et al., "A Fully-Integrated Quad-Band GSM/GPRS CMOS Power Amplifier," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp 2747-2758, Dec. 2008.

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[5] P. Reynaert, M. Steyaert, "A 1.75GHz GSM/EDGE polar modulated CMOS RF power amplifier," *ISSCC Dig. Tech.Papers*, pp. 312-313, Feb. 2005.

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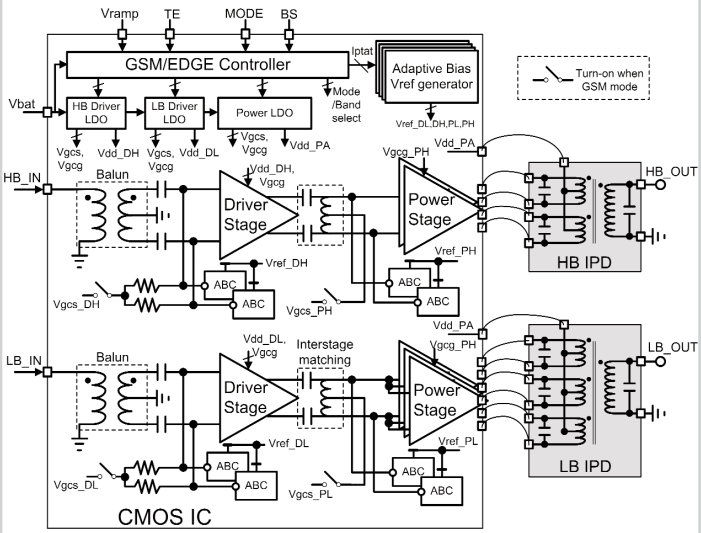

Figure 24.4.1: Block diagram of GSM/EDGE Quad-band CMOS PA Module.

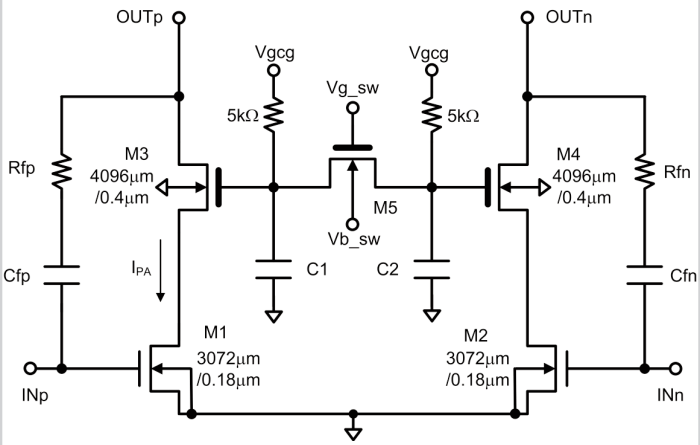

Figure 24.4.2: Simplified circuit schematic of PA stage.

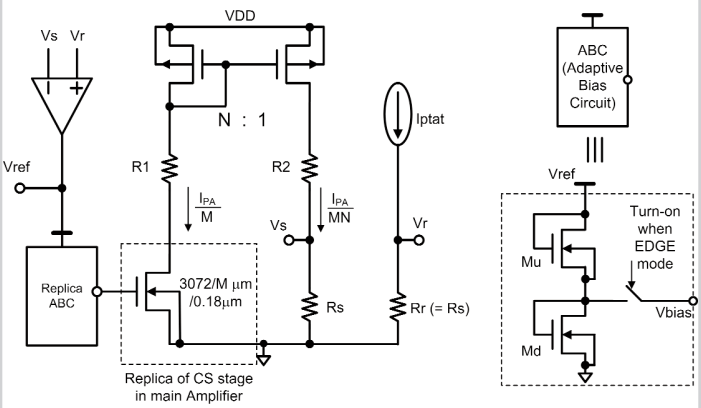

Figure 24.4.3: Simplified circuit schematic of reference voltage generator for adaptive bias circuitry.

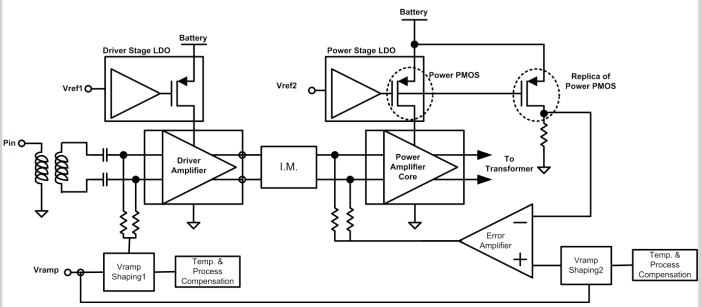

Figure 24.4.4: Power control scheme of driver stage and closed loop current control of power stage for GSM mode.

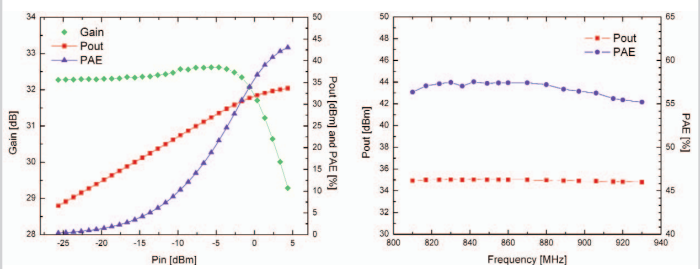

Figure 24.4.5: Measured RF performance for low-band. The right figure is the output power and PAE for GSM mode, and the other is for EDGE mode.

			This work	[5]
Technology			0.18μm CMOS & IPDs	0.18μm CMOS
Silicon Area [mm^2]			1.1×2.8, 1.1×1.2, 1.5×1.4	1.8×3.6
Package size [mm^2]			5×5	-
Supply Voltage [V]			3.0-4.2	-
EDGE	GSM/EGSM	average linear Pout [dBm]	28.5	-
		average PAE [%]	22	-
		ACPR [dBc] @ 400kHz	-57	-
		ACPR [dBc] @ 600kHz	-75	-
		EVM-rms [%]	1.6	-
		Rx band noise @ 20MHz offset	-86 dBm/100kHz	-
	DCS/PCS	average linear Pout [dBm]	27.5	23.8
		average PAE [%]	23	22
		ACPR [dBc] @ 400kHz	-56	-56.7
		ACPR [dBc] @ 600kHz	-74	-64
		EVM-rms [%]	2.5	1.67
		Rx band noise @ 20MHz offset	-86 dBm/100kHz	-
GSM	GSM/EGSM	Input power [dBm]	0~+6	-
		Output power [dBm]	34.5	-
		PAE [%]	55	-
		Rx band noise @ 20MHz offset	-82 dBm/100kHz	-
	DCS/PCS	Input power [dBm]	0~+6	-3
		Output power [dBm]	32.5	27
		PAE [%]	48	34
		Rx band noise @ 20MHz offset	-82 dBm/100kHz	-

-Unless otherwise specified: Vbat=3.5V, Pin=+3dBm, Duty Cycle=25%, Zin=Zout=50Ω, Tc=25℃, Vramp=1.8V

Figure 24.4.6: PAM measurement summary for low bands and high bands.

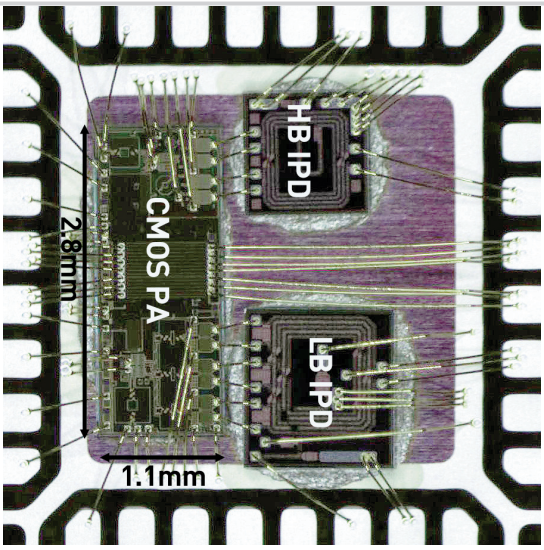

Figure 24.4.7: Micrograph of PA IC with IPD-based transformers assembled in a 32-pin QFN package.

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