A 2.4 GHz SiGe HBT High Voltage/High Power Amplifier

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***Abstract*—Two- and three- stage high voltage/high power (HiVP) amplifiers have been designed, implemented, and measured using a 0.12 μm SiGe HBT process. The HiVP is a circuit configuration that allows for very large output voltage swings, leading to high output power when used in a power amplifier. This letter describes the first implementation of a HiVP circuit using Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs). The intent of this letter is 1) to illustrate practical design steps for implementing a HiVP circuit in silicon-based technologies and 2) to report measurements of this HiVP implementation in 0.12 μm SiGe. At 2.4 GHz, $\mathrm{Psat} = 16.67\ \mathrm{dBm}$ and $\mathrm{Psat} = 18.55\ \mathrm{dBm}$ are achieved for the two- and three-stage SiGe-HBT HiVP amplifiers, respectively.**

***Index Terms*—Germanium compounds, heterojunction bipolar transistor (HBT), power amplifiers (PAs), silicon germanium (SiGe), silicon, silicon alloys.**

I. Introduction

SILICON GERMANIUM (SiGe) BiCMOS and RF-CMOS technologies offer the advantage of greater *integration* compared to III-V technologies. Integrating all of the components of a transceiver onto a single-chip has been accomplished in silicon [1], [2], but always through a series of compromises. The power amplifier is the component that often experiences the greatest compromise in terms of output power, efficiency, and gain in the aspiration of integration.

In an effort to obtain higher $\mathrm{f_T/f_{MAX}}$ in SiGe and Si processes, process scaling, among other techniques, is typically employed. Scaling in the form of shortening channel length for FETs or base width for bipolar devices, to decrease carrier transit time, reduces breakdown voltages from one process generation to the next [3]. Reduced breakdown voltages effectively decrease the output voltage swing and output impedance of devices. For power amplifiers made from such devices, this results in reduced RF output power and more complex matching circuitry to operate in a 50 Ω system.

A commonly used technique to increase RF output power is to place transistors in parallel, increasing the output current swing of an amplifier, but reducing the output impedance. This makes matching more difficult for the designer. A less commonly used technique is device stacking; of which cascoding is an example. An original device stacking technique known as the HiVP (High Voltage/High Power) configuration offers a unique approach that not only allows the designer to customize the dc bias of their amplifier, like a cascode, but increases the output voltage swing, improves efficiency, and raises the output impedance, greatly simplifying matching. Originally implemented in GaAs FETs [4], it has recently been implemented using Silicon FETs [5] and InGaP HBTs [6]. In this work we used the original HiVP architecture, provided a novel biasing technique, and extended it for use with SiGe Heterojunction Bipolar Transistors.

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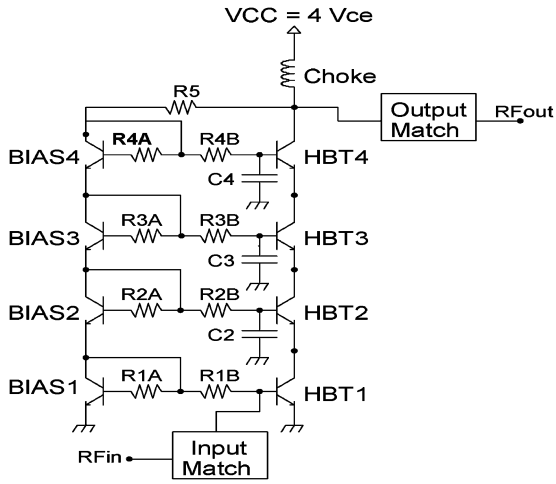

Fig. 1. Four Stage HiVP where HBT devices are in series both in dc and RF.

II. SiGe HBT-HiVP Concept

Fig. 1 shows a HiVP implementation using a stack of four SiGe HBTs. $HBTs$ 1-4 are identical in emitter area size. $\mathrm{V_{CC}}$ is set to four times a single transistor's $\mathrm{V_{CE}}$ bias value. The HBT labeled $BIAS1$, along with resistors $R1A$ and $R1B$, serves as a ratioed current mirror for $HBT1$; this is true for $BIAS$ 2-4 for $HBTs$ 2-4 as well. $R5$ serves a dual purpose: negative feedback and variable dc bias control. As the RF output signal swings up and down, R5 changes the reference current to each current mirror. This adjusts the base current to each HBT 1-4, preventing device breakdown—a key and necessary feature of the SiGe HBT-HiVP configuration.

From an RF perspective, $HBTs$ 1-4 behave as an RF power combiner. RF enters through the base of $HBT1$, travels up the stack of HBTs, and exits through $HBT4$'s collector. What differentiates this configuration from a classic cascode configuration is the creation of optimum power match conditions for each transistor. Capacitors $C2 - C4$ enable the designer to tune the

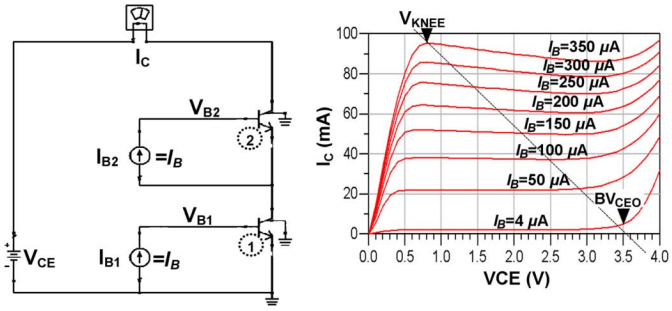

Fig. 2. Two Stack (a) doubles IV-Curve's (b) C-E breakdown $(\mathrm{BV_{CEO}})$.

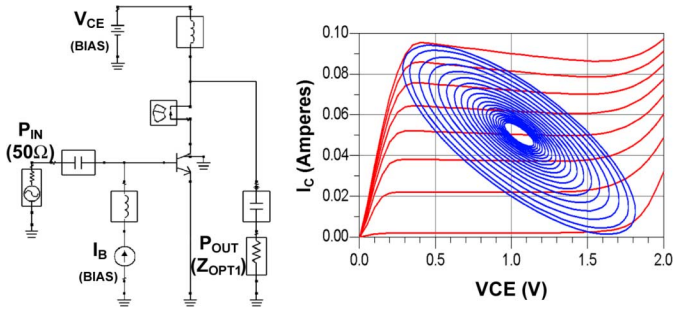

Fig. 3. Bottom Stage of HiVP (a) and its H.B. dynamic load line (b).

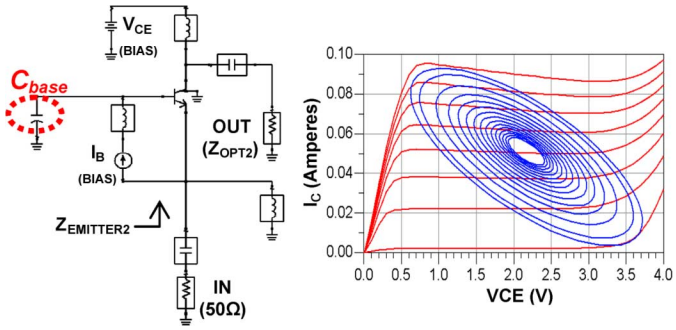

Fig. 4. S-parameter test bench for second stage of two-stack HiVP (a), Harmonic balance dynamic load line for two-stack HiVP (b).

input impedance of each HBT's emitter. By tuning the capacitor on the base of an HBT, the optimal load impedance can be presented to the preceding HBT's collector. The relationship between a capacitor at the base of an HBT and its effect on the HBT's small signal emitter impedance is derived from Ezzeddine and Wu [4], [5] through the following equation:

$$Z_{emitter} \approx \left(\frac{1}{g_m}\right)\left(1+\frac{C_{be}}{C_{base}}\right). \tag{1}$$

Equation (1) shows that by adjusting a capacitor attached to the base of an HBT, the emitter's impedance can be altered. The goal is to adjust C_{base} so that the emitter's impedance becomes the optimal load impedance for the preceding HBT's collector. Thus, RF power can be transferred from one HBT stage to the next, effectively using the stack of HBTs as an RF power combiner.

III. Two Stack HiVP Simulation & Design

As a proof of concept, both two- and three-stack HiVP devices were designed, fabricated, and measured. This section discusses the design and simulation technique used for the two-stack implementation, which was then expanded for the three-stack implementation.

To properly size the devices in the HiVP, a mixture of DC, harmonic balance, and S-parameter simulations are used, iteratively. Each HBT in the HiVP stack is a four-finger IBM High-$\mathrm{f_T}$ $18\ \mu\mathrm{m} \times 0.12\ \mu\mathrm{m}$ SiGe HBT in double-stripe CBEBC configuration. Each HBT in the current mirror stack is a single-finger HBT of identical emitter area and configuration.

A. DC Simulation-IV Curves and Initial Calculations

The first step of the design process is to generate an IV-Curve ($\mathrm{I_C}$ versus $\mathrm{V_{CE}}$) for a two HBT stack. The unusual configuration shown in Fig. 2(a) is used to generate the IV-Curves in Fig. 2(b). The key to this simulation is to have the bottom terminal of the current source, supplying the second HBT, tied to the first HBT's collector as opposed to ground. This allows the voltage of the top HBT's base to be $\mathrm{V_{B2}} = \mathrm{V_{BE2}} + \mathrm{V_{CE1}}$ at all times during the dc simulation. The current sources are set to a common variable name (I_B), so that each device's base current remains the same for each parametric sweep. Fig. 2(b) shows the two HBT's $\mathrm{BV_{CEO}} = 3.5\ \mathrm{V}$ nearly doubling a single HBT's $\mathrm{BV_{CEO}}$ of only 1.8 V. The IV-curves of a single HBT are shown in Fig. 3(b).

B. Harmonic Balance—Determining Optimal Impedances

Next we determine the optimal load impedance for the first stage of the HiVP stack (the bottom HBT). The inverse of the slope of the single HBT's load-line provides a first order approximation of the real component of the optimal load impedance for the first stage $(\mathrm{R_{OPT1}})$. In this case, the single four-finger HBT has $\mathrm{R_{OPT1}} \approx 30\ x\Omega$. A harmonic balance simulation is used to determine the optimal load's reactive component and more precisely determine $\mathrm{R_{OPT1}}$.

The bottom HBT is configured as shown in Fig. 3(a). An RF signal at 2.4 GHz (center frequency of interest) is applied to the base; the input power of the 2.4 GHz signal is swept into compression (−20 dBm to 5 dBm), allowing the device to range from its linear region of operation into saturation. The dc bias for a single transistor is set for class AB operation (in our case, $\mathrm{V_{CE}} = 1.05\ \mathrm{V}$, $\mathrm{I_B} = 157\ \mu\mathrm{A}$). RF choke inductors and dc blocking capacitors are shown in boxes in Fig. 3(a). The load attached to the collector of the device is set as a tunable variable, $Z_{\mathrm{OPT1}} = \mathrm{R_{OPT1}} + \mathrm{j} * \mathrm{Z_{IMG1}}$; initially $\mathrm{R_{OPT1}} = 30\ \Omega$, while $\mathrm{Z_{IMG}} = 0$.

Fig. 3(b) shows the results of a tuned harmonic balance simulation overlaid with the results of a dc simulation for a single HBT. The designer can adjust the variable $\mathrm{R_{OPT1}}$ and $\mathrm{Z_{IMG1}}$ until the ellipse fills the entire dc IV-curve. An ellipse reaching the boundaries of the IV-curve indicates that the load presented to the device yields the maximum output voltage and output current swing. One must also ensure that the load presented ensures the highest PAE of the device for the class of operation. The load of $\mathrm{Z_{OPT1}} = 12.5 + \mathrm{j}11.5\ \Omega$ produces the ellipse shown in Fig. 3(b) for a single SiGe HBT.

C. S-Parameter Simulation

Using (1), the goal is to make the input impedance of the second stage equal $\mathrm{Z_{OPT1}}$. An S-parameter simulation is performed on the second stage of the HiVP to determine its emitter impedance, as shown in Fig. 4(a).

Fig. 4(a) shows the top stage of the 2 stack HiVP device. An input terminal is placed at the emitter (as port 1), and a second

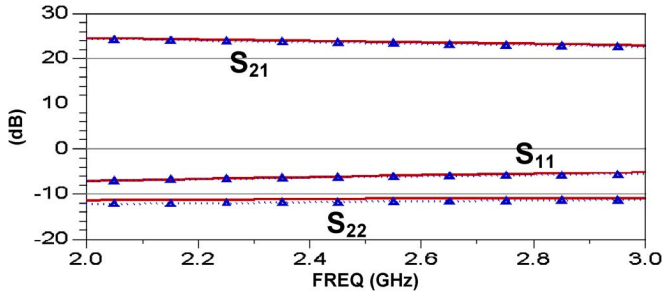

Fig. 5. S-parameters—*unmatched*—2 stack HiVP (*sim.* versus *mes.*).

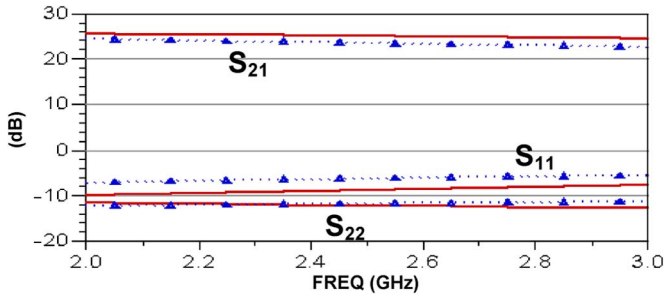

Fig. 6. S-parameters—*unmatched*—3 stack HiVP (*sim.* versus *mes.*).

terminal (as port 2) is attached to the device's collector. The optimal impedance of the second stage is estimated at twice the first stage's optimal load ($\mathrm{Z_{OPT2}} \approx 2 * \mathrm{Z_{OPT1}} = 25 + \mathrm{j}23\ \Omega$). This serves as a valid first order approximation and will be refined in a harmonic balance simulation. The dc bias found in dc simulation is applied to the transistor ($\mathrm{VCE} = 1.05$ V, $\mathrm{IB} = 157\ \mu$A). RF chokes and dc blocks are added as shown.

In this simulation, C_{base} is attached to the base of the HBT, as shown in Fig. 4(a) and is initially set to 0 F. A Smith chart plot of S11 reveals that as C_{base} is increased, the emitter's input impedance $\mathrm{Z_{EMITTER2}}$ (at 2.4 GHz) decreases from $32.7 + \mathrm{j}7.2\ \Omega$ to $12.6 + \mathrm{j}11.7\ \Omega$, as (1) predicts. With C_{base} tuned, $\mathrm{Z_{EMITTER2}} \approx \mathrm{Z_{OPT1}}$, so the second stage is now equal to the optimal impedance for the first stage. The two stages can be interconnected, as they are now optimally matched.

D. Harmonic Balance—Stacking of Stages

The final step is to interconnect stage 1 and the tuned stage 2 of the HiVP. As done for a single HBT, a harmonic balance simulation is performed to find the optimal load impedance ($\mathrm{Z_{OPT2}}$) that must be presented to the two-stage stack.

Once the optimal impedance for the two-stage HiVP is determined, the simulations are repeated. Because the HBTs are non-unilateral, $\mathrm{Z_{OPT2}}$ changes emitter impedance of the second stage, so prior simulations for the second stage must be repeated to properly find C_{base}. Fig. 4(b) shows the dynamic load line for a properly matched two-stack device.

Due to the sensitivity of the SiGe HBT to base-emitter voltage, resistor ratioed current mirrors replace the ideal current sources used in simulation. Ratioed mirrors allow one to use smaller HBTs for BIAS 1-4 in Fig. 1. The size of R5 is determined by calculating the dc supply current needed in the bias stack. Attention in layout is required to keep the feedback path through the bias stack to a fraction of the wavelength of interest, to avoid any potential phase-shifts in the HiVP stack. The simulator was used to verify that R5 provides the correct bias current and that the phase of feedback path phase is small.

IV. Measurements

Both two- and three-stack HiVPs have been fabricated using the IBM 8HP SiGe HBT 0.12 μm process, and have been measured. The total layout area for the $\mathrm{two-stack} = 0.013\ \mathrm{mm}^2$; the area for the $\mathrm{three-stack} = 0.016\ \mathrm{mm}^2$. For the two- and three-stack devices, supply voltage ($\mathrm{V_{CC}}$) is 2.17 V and 3.2 V, respectively. S-parameters for the unmatched two- and three-stack devices are shown in Figs. 5 and 6, respectively. Large signal characteristics, for both unmatched devices, are in Fig. 7.

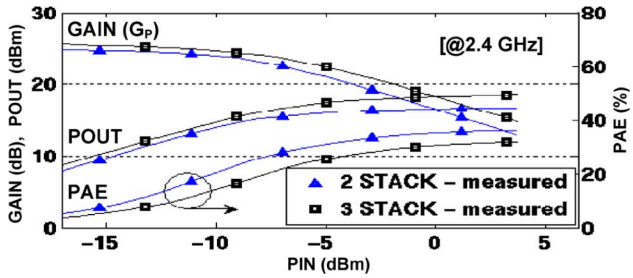

Fig. 7. $\mathrm{Psat} = 16.67$ dBm, $\mathrm{Psat} = 18.55$ dBm, 2 & 3 stack HiVP resp. (*mes.*).

The measurements show a strong agreement with simulated values, as a variance of only 1.5 dB is observed. The power measurements in Fig. 7 show a more than 50% increase in Psat with the addition of the third stage—a big benefit for a small increase in area. It is important to note that a large transistor of similar total periphery would have a narrower bandwidth, S11 and S22 would not be as flat across the band, and Zout would be much lower. Due to success at low frequencies, SiGe HBT-HiVP two-, three-, and four-stage mm-wave implementations have been designed and sent out for fabrication.

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