A 1.75-GHz Polar Modulated CMOS RF Power Amplifier for GSM-EDGE

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***Abstract*—This work presents a fully integrated linearized CMOS RF amplifier, integrated in a 0.18-μm CMOS process. The amplifier is implemented on a single chip, requiring no external matching or tuning networks. Peak output power is 27 dBm with a power-added efficiency (PAE) of 34%. The amplitude modulator, implemented on the same chip as the RF amplifier, modulates the supply voltage of the RF amplifier. This results in a power efficient amplification of nonconstant envelope RF signals. The RF power amplifier and amplitude modulator are optimized for the amplification of EDGE signals. The EDGE spectral mask and EVM requirements are met over a wide power range. The maximum EDGE output power is 23.8 dBm and meets the class E3 power requirement of 22 dBm. The corresponding output spectrum at 400 and 600 kHz frequency offset is −59 dB and −70 dB. The EVM has an RMS value of 1.60% and a peak value of 5.87%.**

***Index Terms*—EDGE, linearized power amplifier, polar modulation.**

I. Introduction

TO INCREASE their data rate, recent wireless systems like EDGE, WCDMA, CDMA2000, and WLAN, also allow amplitude or envelope variations of the phase modulated RF carrier. In contrast to constant envelope systems like GSM and Bluetooth, these envelope variations require either a linear or a linearized power amplifier (PA). A linear power amplifier, such as a Class A or AB amplifier, has the drawback of lower efficiency and hence reduced battery lifetime. Furthermore, all RF stages preceding the amplifier must have the same amount of linearity to avoid degradation of the output spectrum. This overall linearity requirement will increase the power dissipation, not only of the PA stage itself, but of the entire transmitter as such.

Nonlinear switching or saturated power amplifiers are easier to integrate and consume less power since the driver stages do not have to be linear. Furthermore, since the amplifier works in compression, it is less sensitive to shifts in the operating point that might be caused by technology variations.

Especially in CMOS, switching amplifiers have been integrated with great success since a CMOS technology basically is a digital (switching) technology. However, in order to meet the linearity requirements of EDGE, WCDMA, WLAN, and others, these constant envelope PAs need to be linearized. As digital signal processing is widely available at a relatively low power and low cost in CMOS, it is advantageous to use this *DSP power* to linearize a constant envelope PA.

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In this paper, a fully integrated CMOS nonlinear Class E amplifier is linearized based upon a polar modulation scheme. The amplifier is optimized for transmitting EDGE signals at 1.75 GHz. The output matching network, RF inductors and the amplitude modulator are all integrated on a single 0.18-μm CMOS die. To the authors' knowledge, this is the first reported fully integrated linearized CMOS RF PA, based on polar modulation.

This paper is organized as follows. First, the principle of Polar Modulation is reviewed. Section III describes the procedure to design a fully integrated switching CMOS RF PA. In Section IV, the design of the amplitude modulator is discussed, followed by a discussion of the distortion mechanisms. The measurement results are discussed in Section V and final conclusions are given in Section VI.

II. Polar Modulation

The basic idea of polar modulation is depicted in Fig. 1. At digital baseband, the RF output signal is represented by an in-phase voltage $I(t)$ and a quadrature voltage $Q(t)$. The relationship between the baseband signals and the RF output voltage is given by

$$v_{\mathrm{RF}}(t) = I(t) \cdot \cos(\omega t) + Q(t) \cdot \sin(\omega t). \tag{1}$$

This cartesian representation of the RF output signal can be rewritten in polar coordinates, resulting in the baseband signals $A(t)$ and $\theta(t)$

$$v_{\mathrm{RF}}(t) = A(t) \cdot \cos\left(\omega t + \theta(t)\right). \tag{2}$$

The conversion from cartesian to polar coordinates can be done by a digital CORDIC, implemented in the DSP [1].

The signal $\cos(\omega t + \theta(t))$ is an RF signal with a constant envelope. Hence, it can be amplified by a switching or saturated amplifier. In these amplifiers, the amplitude relationship between the RF input signal and RF output signal is lost. However, the output voltage is linearly dependent on the supply voltage. Therefore, if the supply voltage is modulated by $A(t)$, the envelope is recovered at the antenna output, as clarified in Fig. 1.

The polar modulation architecture clearly consists of two signal paths: 1) a constant envelope phase path consisting of an up-converter mixer and PLL, and 2) an envelope path, carrying the envelope signal $A(t)$ and consisting of an amplitude modulator that delivers the supply voltage of the RF PA. This architecture can be considered as an extension to existing constant envelope GSM and Bluetooth architectures, since the RF signal is still a phase modulated and constant envelope signal.

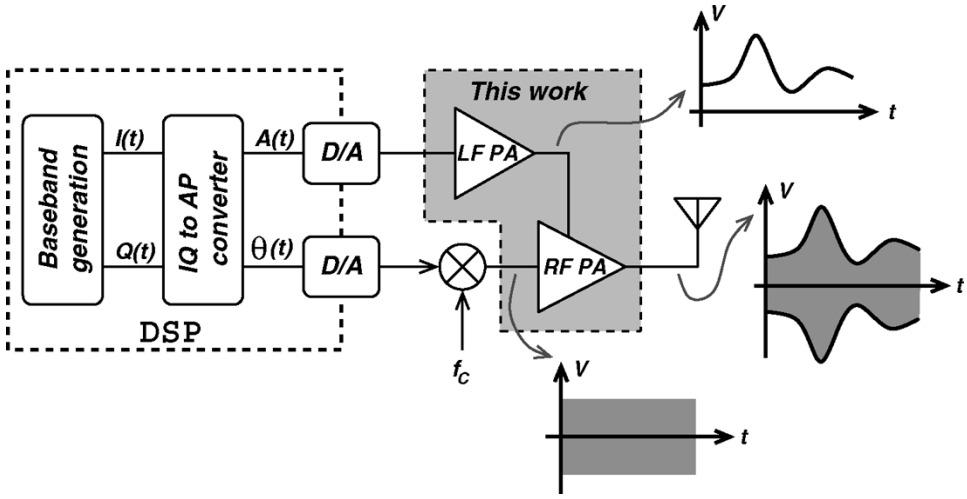

Fig. 1. Block diagram of a polar modulated power amplifier.

In a polar modulated PA, the amplitude linearity requirement is completely shifted to the envelope path and the phase path only needs to have phase linearity [2], [3]. Since the entire envelope path operates at baseband, linearity is easier to achieve at a lower power consumption. The main causes of linearity degradation in a polar modulated power amplifier are: 1) a differential delay between $A(t)$ and $\theta(t)$; 2) low-pass filtering of the envelope signal $A(t)$; and 3) AM-PM distortion. These topics will be discussed in more detail in Section IV. In the next section, the design of the RF power amplifier in CMOS is discussed.

III. RF PA Design in CMOS

A. Class E Power Amplifiers

The key idea behind any high efficiency power amplifier is to reduce the overlap of current conducting through the transistor and voltage across the transistor. This will result in less dissipation in the transistor and hence increases the efficiency of the amplifier. A second idea is to use the transistor not as a current source, but as a switch. A further efficiency enhancement is obtained by minimizing the voltage across the switch when it is closed, the so-called *zero-voltage switching* criteria (ZVS). All these requirements are present in the Class E amplifier [4], [5].

In Class E, the voltage-current separation and ZVS is obtained by using a tuned LC network. The switch is closed at the instant where both the switch voltage and its first derivative are zero. The requirement of a zero first derivative makes the amplifier less sensitive to component variations. This leads to the well-known Class E conditions as stated by Sokal [4]:

$$\text{Class E} \Leftrightarrow \begin{cases} v_{sw}(t_1) = 0 \\ \frac{dv_{sw}}{dt}\big|_{t=t_1} = 0 \end{cases}$$

where t_1 represents the instant at which the switch closes, and $v_{sw}(t)$ represents the switch voltage.

Fig. 2 depicts a circuit that can satisfy the Class E requirements, provided that the correct component values are chosen. If the nMOS transistor is driven by a square wave, it can be seen as a voltage controlled switch with a nonzero on-resistance R_{on}.

The six passive components of Fig. 2 are constrained by following general considerations. The combination of L_m, C_{m1} and C_{m2} forms an impedance matching network that converts the load impedance of 50 Ω toward a lower impedance R_{eq} to increase the output power. This network also acts as a filter, rejecting the harmonics of the Class E waveform at the drain of the nMOS switch. The value of the *equivalent load impedance* R_{eq} will mainly be determined by the desired output power. In the original Class E design of Sokal, L_1 is made very large so it acts as a current source. Since the Class E working conditions are given by two equations, two components of the circuit can be chosen in such a way that the amplifier fulfills the Class E working conditions. For the circuit of Fig. 2, these two components are the capacitor C_1 and the inductance L_X. In this way, all components are determined.

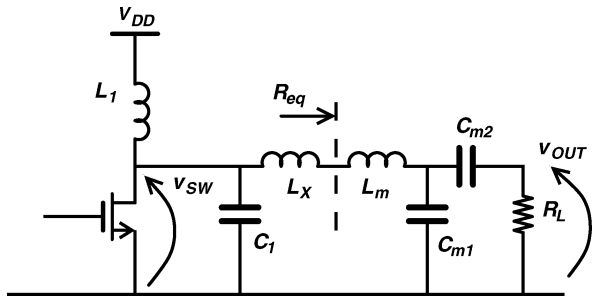

Fig. 2. Class E power amplifier.

B. Implementation in CMOS

When the circuit of Fig. 2 is implemented in CMOS, several loss mechanisms will degrade the performance. If a fully integrated solution is aimed for, the design of the inductors becomes critical. Especially the loss of the matching network becomes excessive for low values of R_{eq} [6]. When inductor L_1 is integrated, it can no longer be considered as infinitely large. Actually, when losses are taken into account, reducing the value of L_1 will increase the efficiency of the amplifier. The amplifier can still operate in class E mode, if the value of L_X is also reduced. This technique is demonstrated in [7]. Reducing the value of L_1 will also result in an increase of the shunt capacitor C_1 in order to meet the Class E conditions. This increase facilitates the design of the nMOS transistor since the parasitic

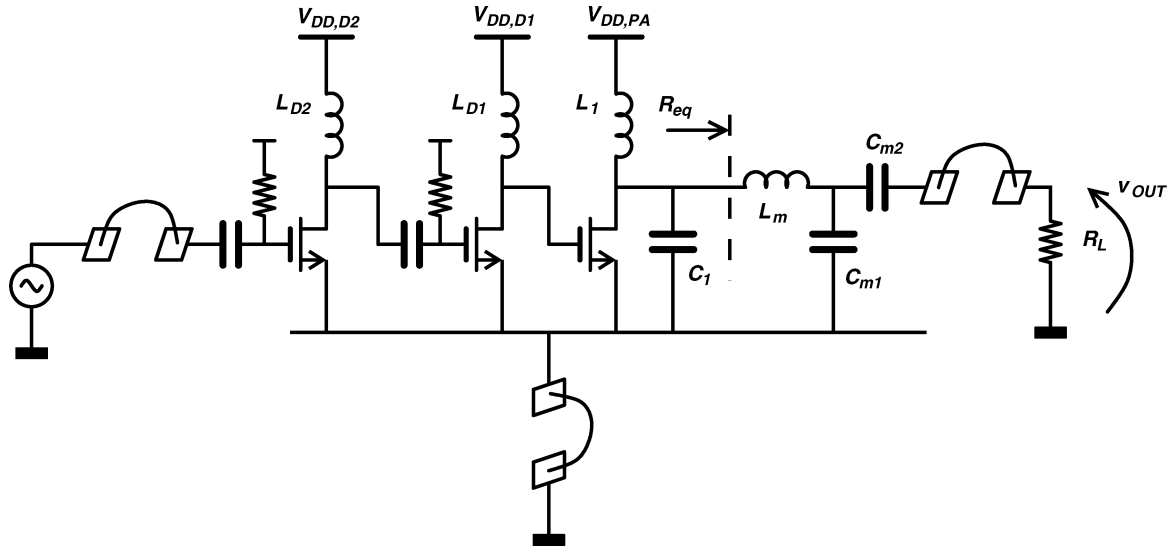

Fig. 3. Class E power amplifier and driving stages.

drain-bulk capacitance and parasitic wiring capacitance can all be included in capacitor C_1.

The size of the nMOS switch is mainly constrained by two loss mechanisms. First, making the switch larger will be beneficial for the output stage itself since the on-resistance is reduced. Once the series loss of the switch can be neglected compared to the other losses in the network, making the switch larger has no benefit. On the other hand, a large nMOS transistor increases the input capacitance which must be driven by the driver stages. If a Class D driver stage is used, the required drive power is determined by

$$P_{\mathrm{DRV}} = \frac{1}{2} \cdot f \cdot C_{\mathrm{nMOS}} \cdot V_{\mathrm{DD}}^2 \tag{3}$$

with C_{nMOS} denoting the input capacitance of the nMOS switch. This capacitance not only includes the gate-source capacitance C_{gs} but also the gate-drain capacitance C_{gd} which is amplified by the Miller effect. To lower the required drive power, the input capacitance of the PA can be tuned by an inductor L_{D1} as indicated in Fig. 3. Since the inductor L_{D1} has some series resistance R_S, the impedance seen by the driver stage at resonance becomes

$$R_{\mathrm{DRV}} = R_S \cdot \left(1 + Q_{L_{D1}}^2\right) \tag{4}$$

in which

$$Q_{L_{D1}} = \frac{L_{D1} \cdot \omega_o}{R_S}. \tag{5}$$

If R_S is approximated as proportional to L_{D1}

$$R_S = \alpha \cdot L_{D1} \tag{6}$$

(4) becomes

$$R_{\mathrm{DRV}} \approx R_S \cdot Q_{L_{D1}}^2 \approx \frac{1}{\alpha \cdot C_{\mathrm{nMOS}}} \tag{7}$$

with $\omega_o = 1/\sqrt{L_{D1} C_{\mathrm{nMOS}}}$. Although the input capacitance is tuned by an inductor, a larger switch still requires more driver power which will degrade the overall efficiency of the amplifier.

In deep-submicron technologies, the low breakdown voltage will require a low value of R_{eq} to achieve the same amount of output power. The lower R_{eq}, the higher the losses of the matching network alone [6] and thus it will decrease the efficiency of the amplifier. This mechanism, together with the power dissipation in the switch and the losses of inductor L_1, will make the Class E solution no longer the optimal solution in terms of efficiency and output power. The performance of a Class E amplifier can therefore be improved by using an overall optimization method that takes all these losses into account [8].

C. Design and Optimization for GSM-EDGE

The GSM-EDGE Class E3 specifications require an average output power of 22 dBm. Since the peak-to-average power ratio for EDGE is 3.4 dB, the RF amplifier must be able to transmit a peak power of at least 25.4 dBm. To increase both the reliability and output power, a thick gate-oxide transistor with an oxide thickness of 6.5 nm and a drain-bulk breakdown voltage of 9 V was chosen for the nMOS switch in the output stage. Another advantage of using a thick-gate transistor in the output stage is the reduced AM-AM distortion which will be discussed in Section III-D. The thick gate-oxide transistor comes with the RF technology option that enables to integrate the inductors. The matching network is designed to transform the 50 Ω antenna impedance to 12 Ω. Together with the thick gate-oxide transistor, this will meet the output power requirement.

Two driving stages are added to the circuit of Fig. 2 in order to achieve sufficient gain and to lower the input capacitance seen by the upconverter. Since the main task of the driver stages is to deliver gain, the corresponding transistors are minimum gate-length 0.18-μm transistors that benefit from the higher f_T. A single-ended version of the complete RF amplifier circuit is

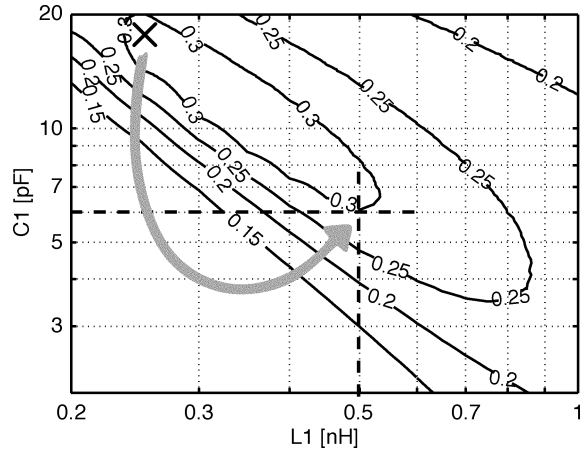

Fig. 4. Contour plot of single ended output power (in Watt) for L_1 and C_1.

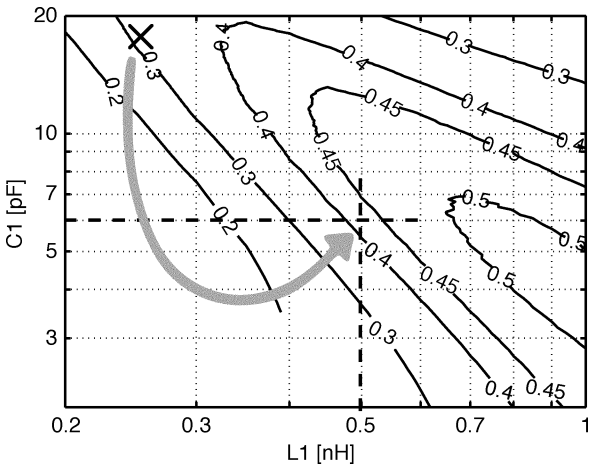

Fig. 5. Contour plot of PA efficiency for L_1 and C_1.

shown in Fig. 3. The amplifier is made fully differential to increase the output power, to reduce the required on-chip decoupling capacitance and to reduce the influence of the parasitic ground inductance present in the package.

As stated in Section III-B, the Class E operating point is not the optimal point regarding efficiency and output power because of the breakdown voltage restriction and the losses in the circuit. To investigate this effect, both the values of L_1 and C_1 are varied, the circuit is simulated and the output power and efficiency are calculated. The result of this optimization process is given in Figs. 4 and 5. The initial Class E operating point is obtained with $L_1 = 0.25$ nH and $C_1 = 18$ pF and is indicated by an x in the upper left corner of the contour plot. In this point, the output power is indeed high (300 mW) but the efficiency is far from the maximal obtainable efficiency. Therefore, in this design L_1 is chosen to be 0.5 nH and C_1 equals 6 pF, resulting in a single-ended output power of almost 300 mW and an efficiency of 42.5%. From these simulations, it is clear that deviating from Class E can result in better performance. The contour plots given in Figs. 4 and 5 were calculated for several transistor widths. A width of 3000 μm results in a maximal power-added efficiency (PAE) and was therefore chosen in this design. The resulting on-resistance is 0.5 Ω at a gate voltage of 3.3 V. The

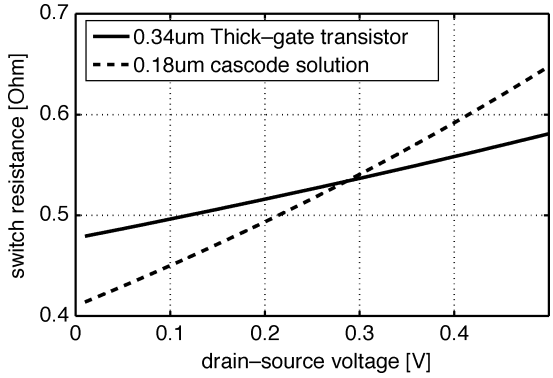

Fig. 6. Linearity of the nMOS switch resistance.

corresponding input capacitance of the PA, taking into account the Miller effect, is 11.5 pF.

The RF amplifier is integrated in a 0.18-μm CMOS technology with a 4-μm top-metal aluminum layer. All inductors required to tune the class E waveform and to perform the output impedance matching, are integrated on-chip. This will result in a solution that is less sensitive to the used package. Furthermore, since no off-chip striplines or inductors are required, the total board area is reduced. Inductors L_1, L_{m1}, and L_{D1} have a quality factor Q_L of about 11. The simulations predict a peak output power of 600 mW or 27.8 dBm with a drain efficiency of 42.5%. To drive the 11.5-pF capacitance of the nMOS switch, the driver stages consume a total DC power of 140 mW. The RF input power to the first driver stage is only -3 dBm. The upconverter can thus directly be connected to the power amplifier. In Fig. 3, $V_{\mathrm{DD,D2}}$ is equal to 1.4 V and $V_{\mathrm{DD,D1}}$ is equal to 1.56 V. In the implementation, these voltages are derived from an on-chip voltage regulator.

D. Reliability Issues

In a Class E power amplifier, the current and voltage waveforms are separated in time. Besides the increased efficiency, this also results in a better reliability regarding hot electrons. Hot electrons occur when both a large gate-drain voltage and a large drain current are present in the transistor. When the transistor is switched off, no current flows in the drain and therefore the drain voltage is allowed to surpass the nominal supply voltage of the technology. In fact, in the off-state the drain voltage is only limited by the oxide breakdown and the drain-bulk junction breakdown. During the on-state, the voltage across the transistor is very low because it acts as a switch and hence no hot electrons are present.

When L_1 and C_1 are modified to achieve a higher efficiency, the ZVS requirement is no longer fulfilled. Therefore, a nonzero drain voltage will be present when the switch is closed. This voltage must be kept below the nominal supply voltage to avoid hot-electrons.

The thick gate-oxide transistor used in this design has another advantage compared to a stacked device solution [9]. Since the RF PA will be linearized by changing the supply voltage of the last stage, the average on-resistance of the nMOS will also change. As a comparison, Fig. 6 depicts the on-resistance of the

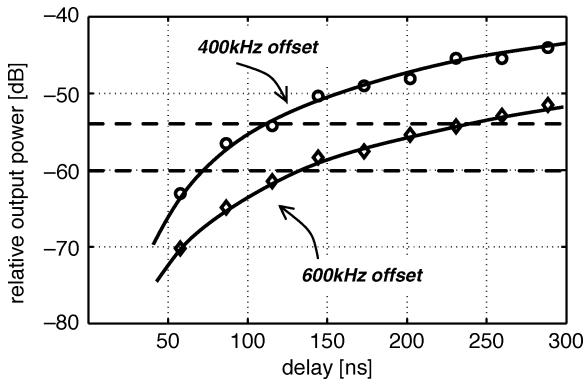

Fig. 7. Simulated spectral mask versus delay.

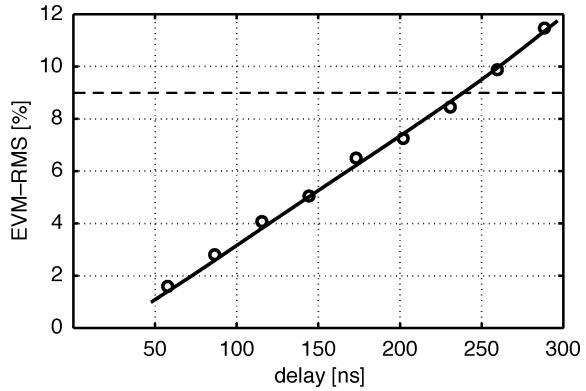

Fig. 8. Simulated EVM versus delay.

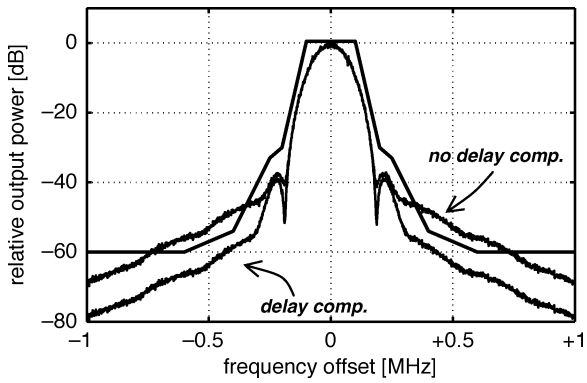

Fig. 9. Simulated output spectrum for a 1-MHz envelope filter, with and without delay compensation.

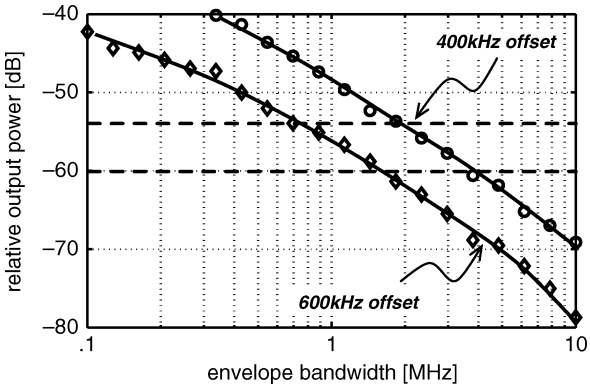

Fig. 10. Simulated spectral mask versus envelope bandwidth.

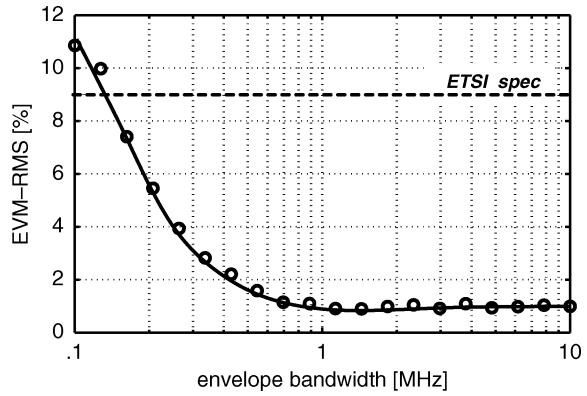

Fig. 11. Simulated EVM versus envelope bandwidth.

used thick gate-oxide transistor and an alternative stacked device solution. It can clearly be seen that the on-resistance of the thick gate-oxide transistor is more constant and hence, if used in an RF PA, it will be more linear if the supply voltage is modulated.

IV. Amplitude Modulator

The switching RF amplifier is linearized by modulating the supply voltage. Because of the linear relationship between the output envelope and the supply voltage of the last stage, the amplitude linearity can be recovered at the output. The driving stages are kept at a fixed supply voltage to ensure that the RF PA always operates as a switching amplifier. If the supply voltage of the driving stages is modulated, excessive AM-AM and AM-PM distortion would be introduced and an amplitude and phase feedback loop would be mandatory [3].

The ETSI specifications pose two linearity requirements that must be fulfilled by the transmitter. First, the transmitted spectrum should not exceed a spectral mask. A second requirement is given by the error vector, defined as the deviation between the actual transmitted constellation point and the ideal constellation point. For the mobile station, the RMS value of the error vector should be lower than 9% and its peak value should be below 30%.

A. Differential Delay

A source of distortion in this architecture is a delay that might occur between the amplitude and phase path. Such a delay will result in a misalignment when amplitude and phase are recombined in the RF power amplifier. The distortion resulting from a differential delay was calculated for a two tone test by Raab in [10]. Actually, it is the group delay of the two signal paths that must be matched. If a second order type-II PLL is assumed in the phase path, the group delay in the phase path for low frequencies is almost zero [11]. In order to have a zero group delay in the envelope path, the amplitude modulator must be designed with a wide enough bandwidth. Fig. 7 shows the output spectrum at 400 and 600 kHz frequency offset, which are the critical points of the spectral mask. The relative output power at these offsets should be -54 dB and -60 dB, respectively. In Fig. 8, the simulated EVM-RMS is given. From the EVM requirement,

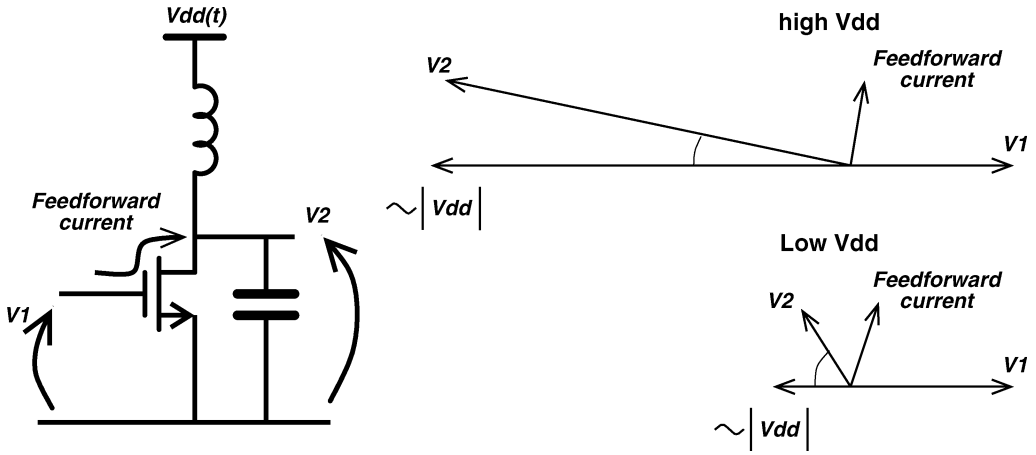

Fig. 12. AM-AM and AM-PM distortion due to the Miller capacitance.

a delay of 240 ns can be tolerated. The more stringent spectral mask requirement however, requires a delay of less than 100 ns.

B. Finite Envelope Distortion

An important design specification is the required bandwidth of the amplitude modulator. The envelope signal $A(t)$ will have a much wider bandwidth compared to the bandwidth of the complex RF output signal $v_{\rm RF}(t)$ [2], [11]. Fig. 9 shows the simulated RF output spectrum when the envelope signal is filtered by a first-order Butterworth low-pass filter with a -3-dB frequency of 1 MHz. The output spectrum at 400 and 600 kHz frequency offset are the most critical points and at these points the spectral mask is violated. The corresponding EVM is 1.7%, which is well below the required 9%. Fig. 10 shows the mask margin and Fig. 11 depicts the EVM-RMS, both versus the bandwidth of the amplitude modulator. Regarding the EVM requirement, a bandwidth of only 150 kHz would be sufficient. However, the more stringent spectral mask requirement sets the bandwidth to at least 2 MHz.

The distortion due to envelope filtering can partially be overcome by adding an additional delay in the phase path. This will result in a better match between the group delay of the envelope filter and the delay of the phase path. As an example, Fig. 9 shows the output spectrum for a 1-MHz envelope filter and a delay of 173 ns in the phase path. This value was obtained by a simple optimization algorithm. With this *optimal* delay, the spectral mask is completely met. This technique is further explored in Section V.

C. AM-AM and AM-PM Distortion

AM-AM distortion is the difference between the baseband envelope signal $A(t)$ and the envelope of the RF output voltage. Such a difference might be caused by distortion in the amplitude modulator or by a nonlinear relationship between the supply voltage $V_{\rm DD}$ and the envelope of the RF output signal. Distortion in the amplitude modulator is relatively easy to control since this block operates at baseband with a relatively low bandwidth. AM-AM distortion in the RF PA itself can be kept low if the last stage is always operated as a switching amplifier. In other words, the supply voltage of the driver stage will be kept high to ensure the switching nature of the amplifier. Besides AM-AM, AM-PM distortion will also be present in this architecture. This distortion is an unwanted phase modulation of the RF output carrier due to the modulation of the supply voltage.

A feedforward current through the relatively large gate-drain capacitance C_{gd} of the nMOS switch is a cause of both AM-AM and AM-PM. This can be understood from the model depicted in Fig. 12. Without the feedforward current, the voltage at the gate will be 180 degrees out of phase from the voltage at the drain. Due to the Miller capacitance C_{gd}, a feedforward current will be present equal to

$$i_{\rm FF} = (v_1 - v_2) \cdot j\omega C_{gd}. \tag{8}$$

The feedforward current $i_{\rm FF}$ will be converted to a voltage at the drain of the nMOS switch and will slightly rotate the voltage v_2. When the supply voltage of the last stage is reduced, v_2 will decrease but the feedforward current will remain high since the supply voltage of the driver stage is not modulated. Therefore, the unwanted rotation of the carrier will be more pronounced when the supply voltage of the PA is reduced.

It is also important to realize that the feedforward signal is only phase modulated and, hence, it has a wide bandwidth [11]. Therefore, not only the AM-PM rotation will affect the linearity and the spectral mask, but the feedforward signal itself will also broaden the output spectrum.

D. Implementation of the Amplitude Modulator

Fig. 13 shows the simplified circuit of the amplitude modulator. For the design of this block, the RF PA is first simulated for different values of $V_{\rm DD,PA}$, the supply voltage of the last stage of the amplifier. From these simulations, the equivalent DC load resistance of the amplifier $R_{\rm equiv,DC}$ can be derived. $R_{\rm equiv,DC}$ is related to the efficiency of the switching amplifier. In the ideal case, the efficiency of the RF PA is independent of the supply voltage $V_{\rm DD,PA}$ and therefore $R_{\rm equiv,DC}$ should remain constant. In a practical implementation however, the equivalent DC load resistance is not constant and this variation will cause AM-AM distortion of the RF output signal. To reduce this distortion, the amplitude modulator is be designed to have a very low output resistance, which is controlled by the loopgain and

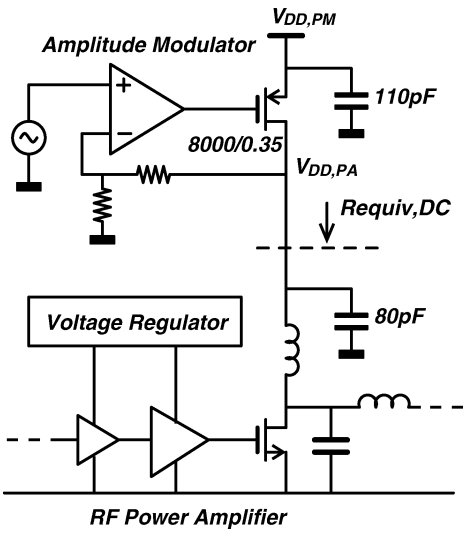

Fig. 13. Simplified circuit of the amplitude modulator.

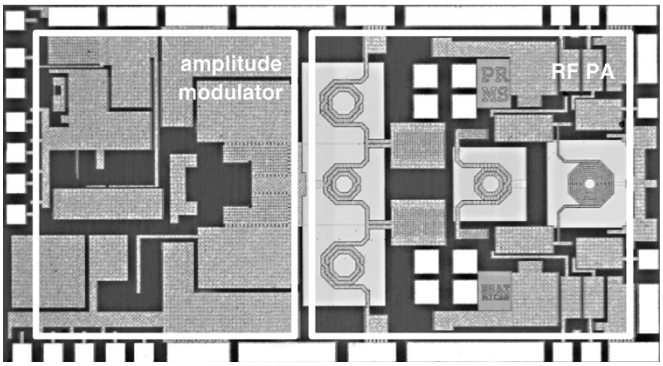

Fig. 14. Microphotograph of the linearized EDGE PA.

the output conductance of the large pMOS. From the simulations, the equivalent DC load resistance of the RF amplifier is 9 Ω and the output resistance of the amplitude modulator is only 0.2 Ω.

The supply voltage of the amplitude modulator is equal to 3.3 V. When EDGE signals are transmitted at maximum output power, the actual supply voltage of the RF PA, $V_{\mathrm{DD,PA}}$ in Fig. 13, has a peak value of 2.9 V, an average value of 1.9 V, and a minimal value of 0.4 V.

The amplitude modulator is integrated on the same chip as the RF PA. Fig. 14 shows a microphotograph of the fully integrated linearized amplifier. The total chip area including bonding pads is 1.8×3.6 mm^2. Wide bonding strips are used for ground and supply voltage connections. Sufficient decoupling is integrated on-chip to ensure stability and to provide a low impedance for the AC supply currents of the RF PA.

V. Measurements

A. Output Power and Efficiency

The measured constant envelope RF output power is 27 dBm. For DCS1800 power class 2, the required constant envelope output power in GSM mode is 24 dBm. Therefore, the presented solution can also be used as a class 2 GSM PA. The input power

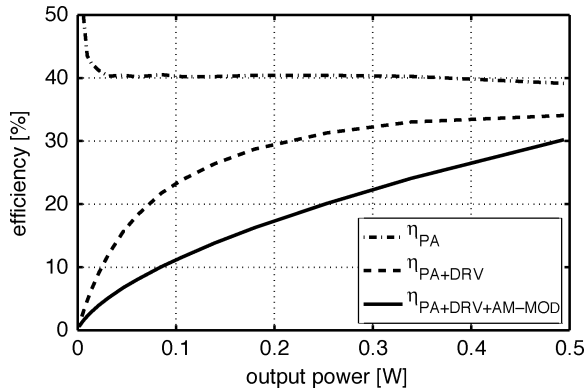

Fig. 15. Measured efficiency versus output power.

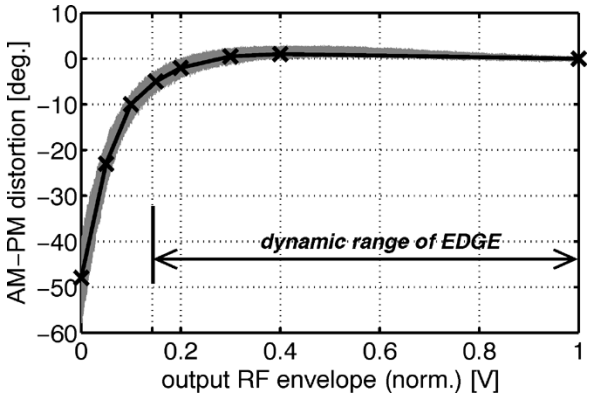

Fig. 16. Measured AM-PM distortion of the RF amplifier.

is −3 dBm, resulting in a power gain of 30 dB, and it enables that the upconverter can directly be connected to the linearized amplifier. Fig. 15 shows the measured PAE of the amplifier for various levels of P_{OUT}. This graph is obtained by applying a DC voltage at the input of the amplitude modulator. The class E amplifier itself (η_{PA}) maintains its high efficiency of 40% over the entire power range. When the power consumption of the RF driver stages is taken into account $(\eta_{\mathrm{PA+DRV}})$, the efficiency drops to 34%. Due to the voltage drop across the amplitude modulator $(\eta_{\mathrm{PA+DRV+AM-MOD}})$, the efficiency becomes 30%.

B. AM-PM Distortion

Fig. 16 shows the measured AM-PM distortion of the amplifier. In this measurement, an unmodulated carrier is applied to the RF amplifier and the envelope signal is slowly varied. The RF output voltage is captured by a vector analyzer and from the raw I and Q data, the phase information can be derived. As can be seen, the AM-PM distortion becomes severe as the supply voltage goes to zero, as explained in Section IV-C. The AM-PM distortion has been measured for different samples and temperatures ranging from 20 °C to 70 °C. All this data is plotted on Fig. 16, but only little variation can be noticed. Therefore, it is justified to apply this data for predistortion. To make digital predistortion feasible, the measured AM-PM distortion has been averaged and is modeled by a piece-wise linear approximation, which is also indicated in Fig. 16 by the solid line.

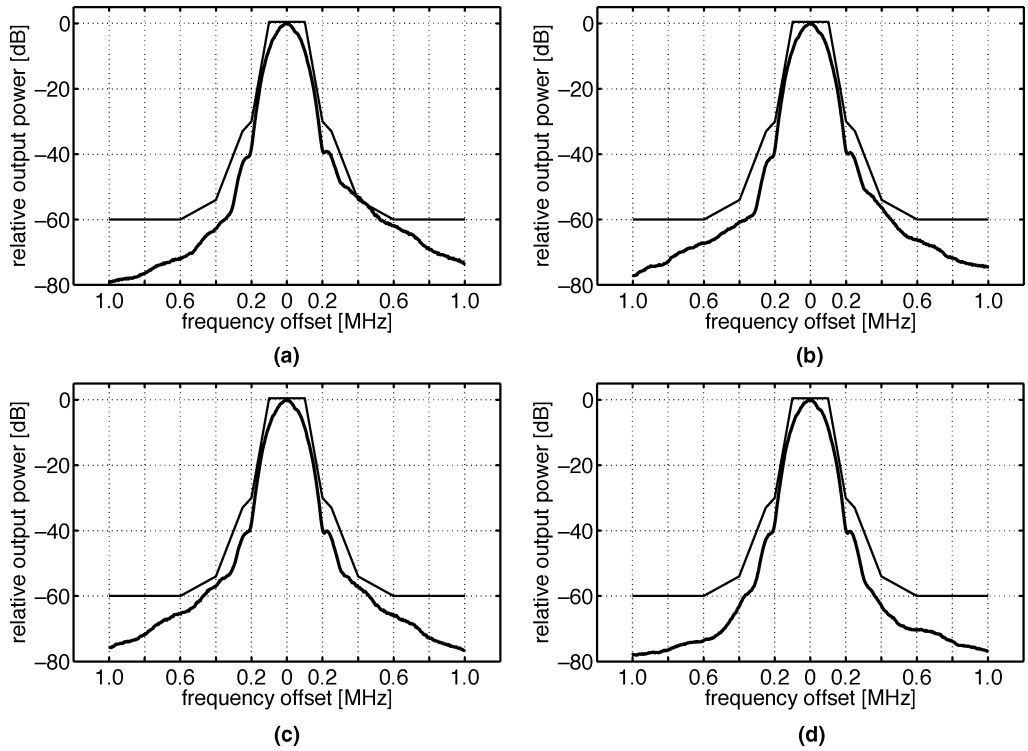

Fig. 17. Output spectra at 23.3 dBm average output power: (a) no compensation, $\mathrm{EVM} = 1.15\%$; (b) AM-PM predistortion $\mathrm{EVM} = 1.14\%$; (c) delay compensation, $\mathrm{EVM} = 1.00\%$; (d) AM-PM predistortion + delay comp. $\mathrm{EVM} = 1.06\%$.

C. EDGE Modulation

In EDGE, the peak-to-average power ratio is 3.4 dB. Since the RF amplifier has a peak output power of 27 dBm, the maximum average output power is about 23.8 dBm or 240 mW.

Fig. 17 shows several EDGE output spectra at 23.3 dBm average output power. It is interesting to note how AM-PM distortion together with a delay between the amplitude path and the phase path can generate an asymmetric output spectrum. In Fig. 17(a), no predistortion or delay compensation is applied. It can be seen that the spectral mask margin is very small at 400 kHz offset. Furthermore, the output spectrum exhibits a large amount of asymmetry. When the eight piece-wise linear predistortion is applied [Fig. 17(b)], the mask is easily met and the asymmetry has almost disappeared. However, the predistortion has little influence on the EVM. If the delay between amplitude and phase is completely compensated, the spectrum is again symmetrical. Now, the EVM is further reduced. Applying both AM-PM predistortion and delay compensation, Fig. 17(d), results in a large margin at both 400 and 600 kHz offset.

Figs. 18 and 19 show the value of the output spectrum at 400 and 600 kHz offset versus average output power. Both the upper and lower spectral values are given to indicate an asymmetry of the output spectrum. In Fig. 18, the spectral mask at $+400$ kHz offset is not met if no predistortion or delay compensation is applied. The spectral mask at -400 kHz offset is much lower which corresponds to a large asymmetry of the output spectrum. When delay compensation is applied, both curves fall together, indicating a symmetrical output spectrum. With the predistortion, the spectral mask margin can be further increased as

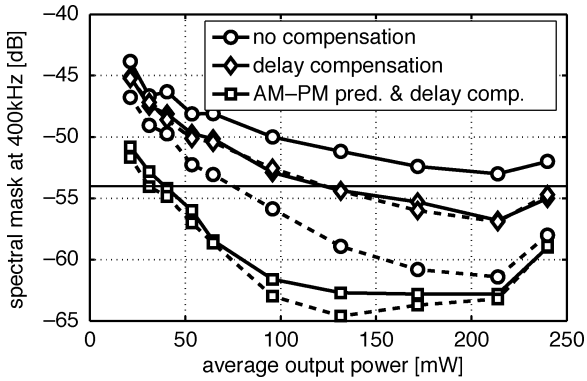

Fig. 18. Measured output spectrum at $+400$ kHz (solid line) and -400 kHz (dashed line) frequency offset.

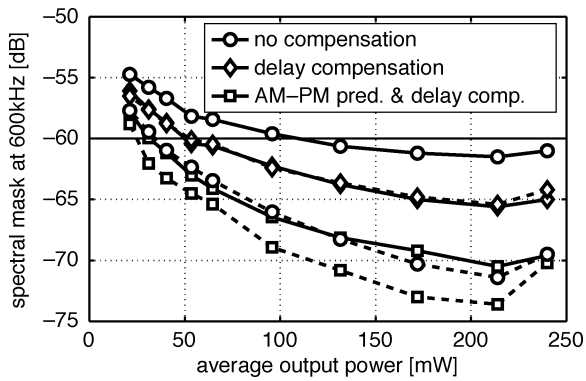

Fig. 19. Measured output spectrum at $+600$ kHz (solid line) and -600 kHz (dashed line) frequency offset.

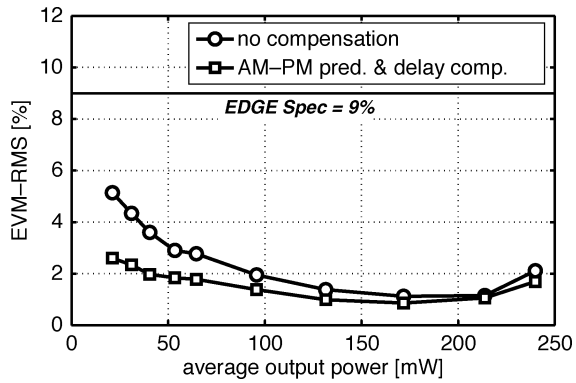

Fig. 20. Measured EVM-RMS versus average output power.

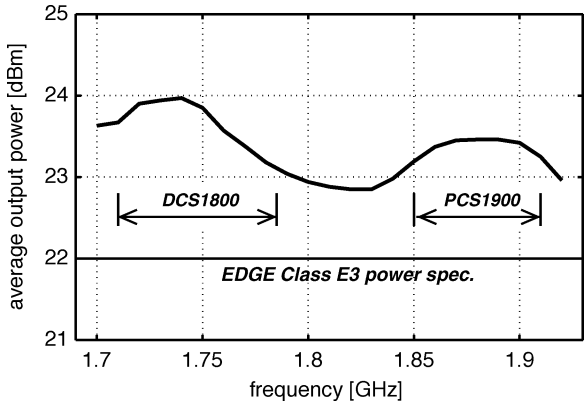

Fig. 21. Measured average output power in EDGE mode.

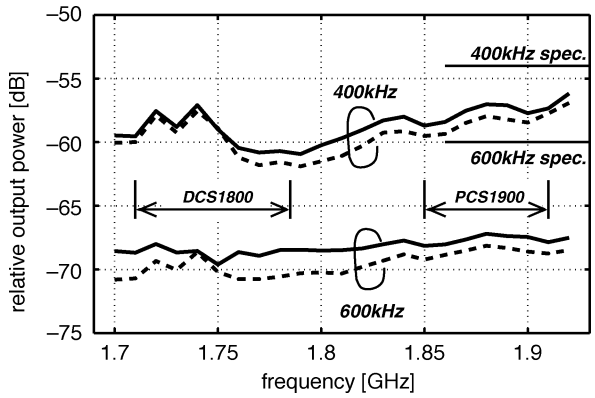

Fig. 22. Measured output spectrum versus frequency for both 400 and 600 kHz frequency offset.

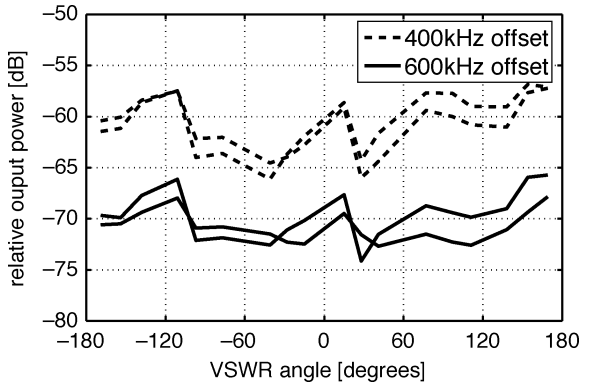

Fig. 23. Measured output spectrum for a 1:3 VSWR.

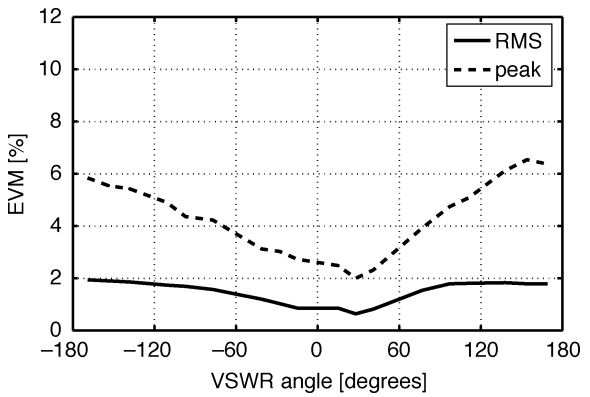

Fig. 24. Measured EVM for a 1:3 VSWR.

well as the power range over which the mask is met. The spectral mask margin is high enough to allow some degradation in the upconverter. For a lower average output power, the AM-PM becomes larger and therefore linearity will decrease. At maximum output power, the spectral mask margin is reduced because of additional AM-AM distortion in the amplitude modulator. To achieve the spectral mask specifications over a wider power range, a more agressive feedforward should be applied, based on a look-up table that can be updated periodically. Fig. 20 shows the measured EVM-RMS versus average output power. The EVM is well below the required 9% specification and is mainly reduced by the delay compensation. In Figs. 17–20, a delay of 52 ns is applied between amplitude and phase, to compensate for the delay of the external upconverter.

Figs. 21 and 22 show the performance of the linearized amplifier versus frequency. The output power and spectral mask specifications are met for both the DCS1800 band ranging from 1.710 to 1.785 GHz and the PCS1900 band from 1.850 to 1.910 GHz.

The EDGE performance has also been measured for a VSWR mismatch of 1:3, as specified by ETSI. The resulting spectral mask and EVM is given in Figs. 23 and 24. Both the spectral mask and EVM requirements are met over the entire range of VSWR angles.

D. Envelope Filtering

To demonstrate how delay compensation can alleviate the required envelope bandwidth, Figs. 25 and 26 show the measured spectral mask at ± 400 and ± 600 kHz offset for different values of the envelope bandwidth. From the simulated results (Fig. 10) it was found that the bandwidth should be at least 2 MHz to meet the spectral mask at 400 kHz. This clearly matches the measurement of Fig. 25. If delay compensation is applied, the envelope bandwidth could be reduced for the same spectral mask margin.

E. Performance Summary

To conclude, Table I shows the performance summary of this single chip linearized PA. Table II compares the performance with the EDGE system requirements.

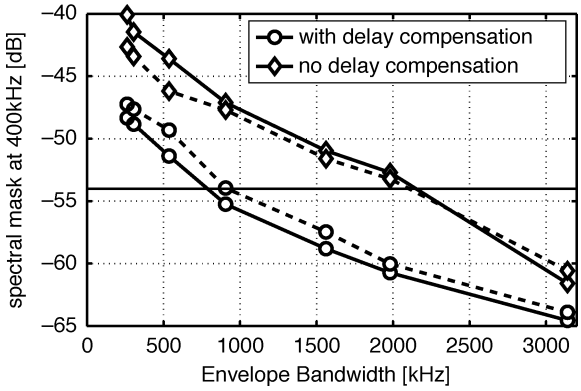

Fig. 25. Influence of envelope filtering on the measured output spectrum at +400 kHz (solid line) and −400 kHz (dashed line) frequency offset.

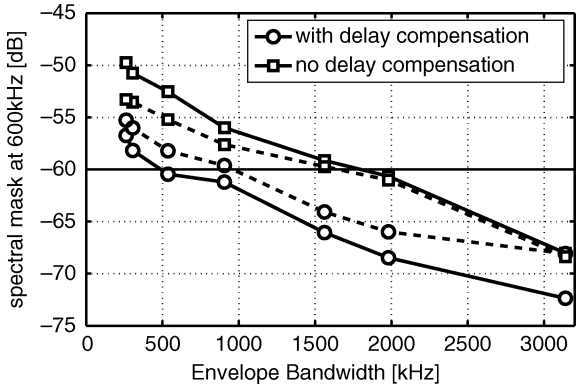

Fig. 26. Influence of envelope filtering on the measured output spectrum at +600 kHz (solid line) and −600 kHz (dashed line) frequency offset.

TABLE I
MEASURED PERFORMANCE AND PROCESS SPECIFICATIONS

Parameter	
technology	.18 μm CMOS
supply voltage	1.8 V and 3.3 V
area	1.8x3.6 mm^2
frequency	1.75 GHz
Parameter	Measured
peak output power (constant envelope)	27 dBm
input power	−3 dBm
power added efficiency	34%
DC power consumption at peak output power	
RF PA	1250 mW @ 3.3 V
RF Driver	186 mW @ 1.8 V
amplitude modulator	33 mW @ 3.3 V

TABLE II
MEASURED PERFORMANCE AND ETSI SPECIFICATIONS

Parameter	Measured	EDGE E3 Specs.
average output power	23.8 dBm	22 dBm
power added efficiency	22%	
modulation spectrum		
400kHz offset, 30kHz RBW	−59 dB	−54 dB
600kHz offset, 30kHz RBW	−70 dB	−60 dB
RMS EVM	1.69%	9%
Peak EVM	5.87%	30%

VI. CONCLUSION

In this paper, a fully integrated CMOS RF power amplifier is linearized for GSM-EDGE at 1.75 GHz. The linearization is based on polar modulation scheme. The amplifier meets the Class E3 EDGE requirements regarding output power, error vector magnitude and spectral mask margin. This fully integrated CMOS solution will reduce the required board area and enables a single chip or single technology EDGE transceiver.

A piece-wise linear predistortion model allows the PA to meet the spectral mask requirements over a wide power range. Delay compensation is suggested as a means to reduce the bandwidth of the amplitude modulator and to further increase the linearized performance.

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