24.5 A 15b Quadrature Digital Power Amplifier with Transformer-Based Complex-Domain Power-Efficiency Enhancement

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With CMOS processes scaling down, digital transmitters (TXs) align with Moore's law to provide compact die area, better interface to digital back-end, and higher power efficiency due to the faster switching nature of core devices even in face of reduced supply voltages. Moreover, the integration of high-power high-efficiency digital power amplifiers (DPAs) on-chip is highly desired for cost reduction, longer battery life, and fast time to market. Recently, digital polar and quadrature TXs have become very attractive architectures [1-7]. Compared with polar TXs, quadrature TXs do not need CORDIC, phase modulators, or time-synchronization circuits, showing good compatibility with wideband communication systems, but the I/Q combination limits the output power and efficiency. To support most wideband applications while enhancing the power efficiency, several techniques have been explored in quadrature DPAs, such as Class-G [1], IQ cell-sharing [2,3], Doherty techniques [4], etc. Besides, wide dynamic power range is often required in wireless standards, like LTE and WLAN, to accommodate various communication environments. In this work, a transformer-combined 15b quadrature DPA with Complex-Domain load modulation and cell sharing is proposed, which achieves wide dynamic power range and high average efficiency even compared with polar DPAs while only occupying a single-transformer footprint.

Figure 24.5.1 illustrates the operation principles of proposed transformer-combined quadrature DPA with IQ cell sharing and load modulation. Here, DPA1 and DPA2 are two identical sub-DPAs, which are controlled by the input I/Q signals. Besides, the cell-sharing technique is adopted in each sub-DPA to enhance output power and efficiency. In state A, i.e., [I, Q] = [±N, 0] or [0, ±N], which are the maximum power points on the orthogonal axes, the transformer combiner is driven by the two sub-DPAs in anti-phase at full amplitude, and the impedance seen by each DPA is $R_L/2$. With output power decreased, the unit cells of DPA2 are gradually turned OFF until they reach state C, which is located at [I, Q] = [±N/2, 0] or [0, ±N/2]. In state C, the DPA2 is completely switched OFF and the impedance seen by DPA1 increases to R_L, thus enhancing the back-off efficiency with load modulation at 6dB power back-off (PBO). Furthermore, in state B, i.e., [I, Q] =[±N/2, ±N/2], input I/Q quadrature signals are fed into DPA1/DPA2 individually and finally vector combined through the transformer combiner for linear power amplification. In state B, the transformer performs as a non-isolating power combiner and introduces an interaction between I/Q paths to reduce power consumption, where another efficiency peaking is obtained at 3dB PBO. Therefore, with the cell sharing and load modulation techniques, this quadrature DPA realizes a total of 12 efficiency peaks (i.e., A/B/C states) in the I/Q complex plane and effectively enhances the average efficiency.

Figure 24.5.2 shows the block diagram of the proposed 15b quadrature DPA. The switched-capacitor PA is adopted due to its good linearity and efficiency [3]. To support most wireless standards with wide-dynamic-power-range requirements, a total of 15b resolution is employed where DPA1 and DPA2 are two identical 14b sub-DPAs. In order to minimize layout mismatch and further improve the resolution, hybrid unary and binary arrays are introduced in each sub-DPA. First, the I/Q_{15} bits determine the corresponding quadrant in the I/Q complex plane. Second, the two sub-DPAs controlled by $I/Q_{14\text{-}0}$ are split into 127 unary cells and 7b LSB binary cells. Here, each sub-DPA consists of 16 hybrid groups (Group0 to 15) with 4b MSBs ($I/Q_{13\text{-}10}$) and 1 binary group (Group16) with 7b binary LSBs ($I/Q_{6\text{-}0}$). Besides, for each hybrid group (Group0 to 15), it is composed of 7 thermometer-coded cells decoded by $I/Q_{9\text{-}7}$ and 2b binary-coded cells ($I/Q_{6\text{-}5}$). Due to the cell-sharing operation, LOI and LOQ signals are fed into both sub-DPAs. Finally, a current-mode parallel-combing-transformer power combiner is adopted to collect the DPA outputs and provide proper impedance matching. In the unit PA cell, the differential cascode inverter topology is employed to improve output power, and the logic circuits are utilized to select the corresponding state of each unit PA for I/Q cell sharing. In the design, redundant buffers are added in Group16 to adjust delay mismatch of binary cells so as to achieve the synchronization with other Group0 to 15. In the floorplan, the "snake"-traverse movement is performed among groups to improve the differential nonlinearity (DNL), which is indicated as the colored arrow lines. The I/Q signals have inverse movements for cell sharing and demonstrate good symmetry in the switching sequence.

Figure 24.5.3 shows the implementation of the proposed single-transformer-footprint parallel-combining-transformer power combiner [6]. Here, DPA1 and DPA2 are placed at the same side of the transformer combiner to maintain good differential symmetry. The pick-up network from each sub-DPA to the primary coils achieves good symmetry by flipping the output polarities of DPA2. Moreover, the output currents from DPA1 and DPA2 flow in parallel directions in the two primary coils, which achieves magnetic enhancement and increases the effective primary inductance. This is especially important for an on-chip matching design at sub-GHz to reduce the area cost. With this transformer power combiner, simulation results show that the DPA achieves the maximum output power of 29.3dBm on the maximum points of orthogonal axes (i.e., state A) where the cell sharing is performed. The output power in state B and state C is 26dBm and 23.1dBm, respectively, which are 3dB and 6dB lower than state A as expected. Moreover, owing to load modulation, the efficiency in state B and C is effectively improved, thus enhancing the average efficiency.

The proposed transformer-combined quadrature DPA was fabricated in a 55nm CMOS process (Fig. 24.5.7) and occupies $1.15\times1.04mm^2$ die area including the two DPA cores, decoders, and transformer power combiner. The chip is tested in a QFN package and powered by two power supplies of 1.2V and 2.4V. In the PAE calculation, the power consumption of all I/O buffers, LO distribution drivers, decoders, and DPAs is counted. The DPA achieves 29.3dBm measured peak output power with 43.1% peak PAE. Figure 24.5.4 shows the measured AM-AM/AM-PM distortion in four quadrants. Besides, the DPA achieves good average linearity performance owing to the elaborated floorplan and symmetrical signal distributions.

Finally, modulation signals are directly tested through the DPA without the need for any digital pre-distortion (DPD). Figure 24.5.5 shows the DPA output spectrum of an LTE 10MHz 64-QAM signal. With -25.6dB EVM, this quadrature DPA achieves 23.6dBm average output power with 24.4% average efficiency, and its output spectrum satisfies the emission mask with enough margin. Moreover, the DPA with 15b resolution realizes wide dynamic output power range from -5dBm to 23.6dBm while still meeting the EVM and mask requirement. Compared with prior-art DPAs in Fig. 24.5.6, the proposed quadrature DPA achieves the highest resolution, highest average power with the best average efficiency when compared with other efficiency-enhanced quadrature or polar DPAs; besides, it supports wide dynamic power range and does not need any DPD for various wireless communications.

Acknowledgement:
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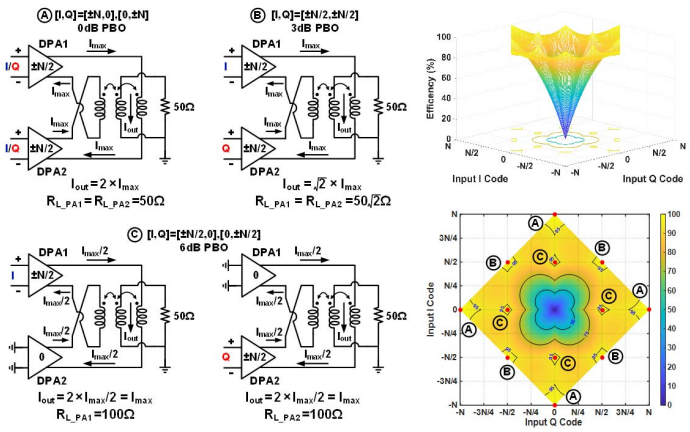

Figure 24.5.1: Operation principles of proposed transformer-combined quadrature DPA with cell sharing and load modulation.

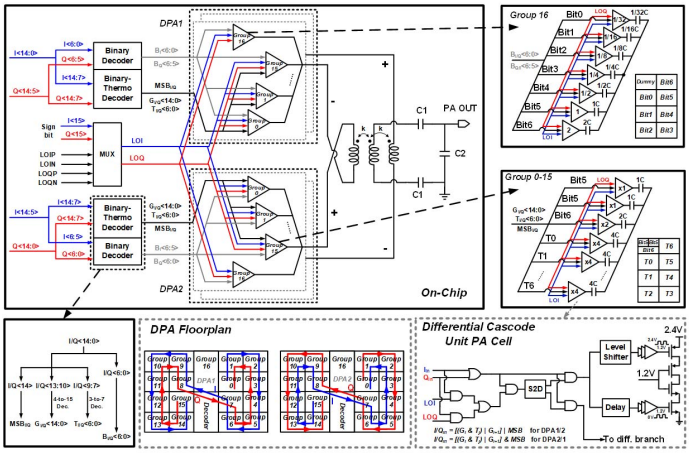

Figure 24.5.2: Block diagram of proposed quadrature DPA and its floorplan.

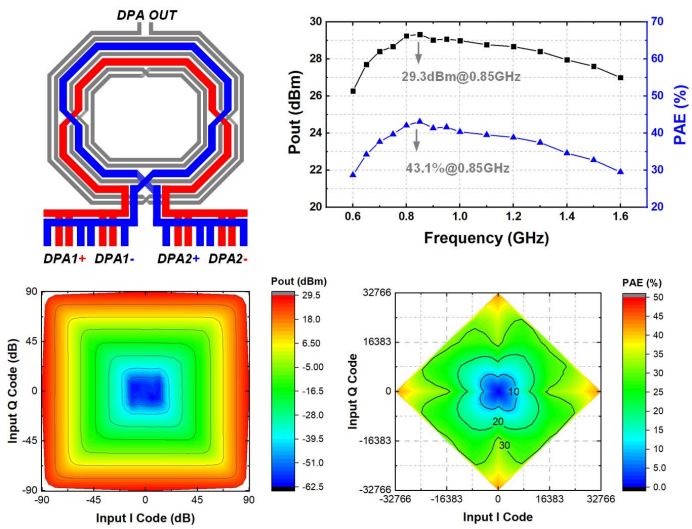

Figure 24.5.3: Layout of the transformer combiner and the measured results of frequency response, peak output power, and PAE.

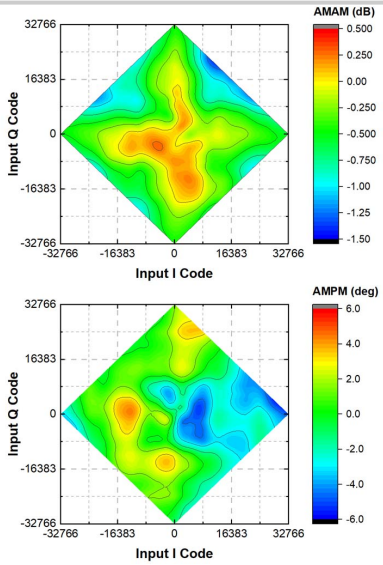

Figure 24.5.4: Measured DPA AM-AM/AM-PM in four quadrants.

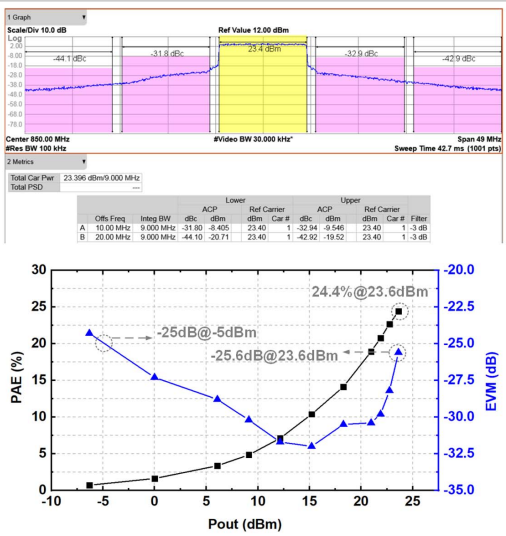

Figure 24.5.5: Measured DPA output spectrum of LTE 10MHz 64-QAM signal at 0.85GHz.

	This Work	JSSC 2016 [1]	JSSC 2017 [2]	ISSCC 2017 [3]	RFIC 2019 [7]
Architecture	Quadrature with Complex-Domain load modulation	Class-G Quadrature	Quadrature with IQ sharing	Quadrature with IQ sharing	Quadrature with Class-G Doherty
On-chip Balun	1 transformer	No	No	1 transformer	2 transformers
Frequency (GHz)	0.85	2.0	0.8	2.5	2.2
Resolution (bit)	15	7	6	11	12
Peak Pout (dBm)	29.3	20.5	13.9	28.6	27.8
Peak PAE (%)	43.1	20	40.4	35	32.1
Modulation Signal	LTE 10MHz, 64QAM	LTE 10MHz, 64QAM	LTE 10MHz, 16QAM	WLAN 20MHz	20-MHz SingleCarrier 1024 QAM
Pavg (dBm)	23.6	14.5	6.97	17.3	21
PAE (%)	24.4	12.2	29.1	11	18.4
EVM (dB)	-25.6	-28.9	-25.9	-27.3	-43
W/ DPD	No	Yes	Yes	No	Yes
Supply Voltage (V)	1.2/2.4	1.2/2.4	1.1	1.1	2.55/1.25
Die Area (mm²)	1.15×1.04	1.75×1	1.66×0.66	1×1	1.07*0.845
Technology	55nm CMOS	65nm RF CMOS	28nm CMOS	28nm CMOS	65nm CMOS

†Results measured with a 50ohm GSG probe.

Figure 24.5.6: Performance summary and comparison with prior-art DPAs.

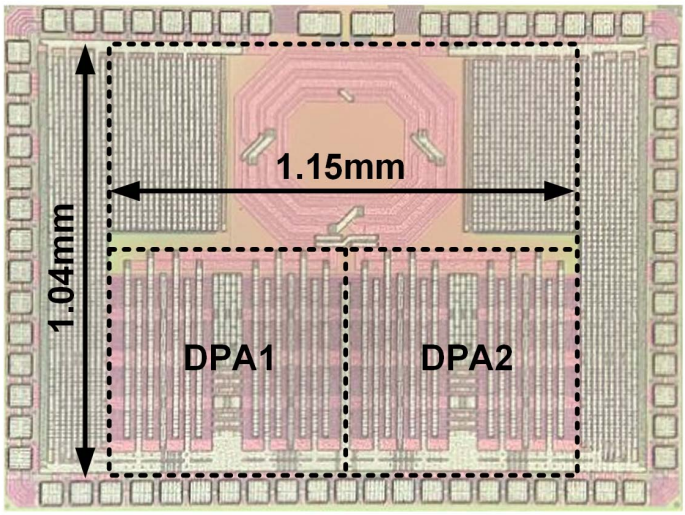

Figure 24.5.7: Die micrograph.

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