A 1.8-GHz CMOS Power Amplifier Using a Dual-Primary Transformer With Improved Efficiency in the Low Power Region

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***Abstract*—A 1.8-GHz CMOS power amplifier for a polar transmitter is implemented with a 0.18-μm RF CMOS process. The matching components, including the input and output transformers, were integrated. A dual-primary transformer is proposed in order to increase the efficiency in the low power region of the amplifier. The loss induced by the matching network for the low-output power region is minimized using the dual-primary transformer. The amplifier achieved a power-added efficiency of 40.7% at a maximum output power of 31.6 dBm. The dynamic range was 34 dB for a supply voltage that ranged from 0.5 to 3.3 V. The low power efficiency was 32% at the output power of 16 dBm.**

***Index Terms*—Class-E, dynamic range, global system for mobile communication (GSM), load impedance, mode locking, polar transmitter, transformer, variable load.**

I. Introduction

GENERALLY, a power amplifier only achieves its peak efficiency at a maximum output power. The efficiency usually degrades seriously at low-output power. Since statistically the transmitted power in a wireless system is below the maximum for most of the transmission times, the average power efficiency is far below its maximum [1]. It is, therefore, essential to maintain a high efficiency over a wide rage of output power to enhance the average power efficiency [1]–[4]. One of the key issues to do this is to improve the efficiency in the low-output power region. Accordingly, methods to improve the efficiency in the low power region are being studied intensively [5]–[7].

A power amplifier with a switched gain stage [8] bypasses an output transistor in low power operation with the aid of additional switches, which are located at the input and output sides of the output power transistor. As a result, the driver transistor alone generates output power with increased efficiency in the low power mode. However, the loss induced by the additional switches degrades the efficiency improvement in the low-output power region. Another method to improve the efficiency in the low-output power region is to vary the output load [9]. In the low power mode, the load impedance of the amplifier is increased. Recently, a stage-convertible structure, in which the merits of the amplifier with a switched gain stage and that with a variable load are utilized, was reported [10], [11]. In previous studies [10], [11], the transmission line transformers are used to design the stage-convertible structure effectively. The stage-convertible power amplifier has multiple load impedances for the high and low power modes. However, a large inductance is needed to design a high load impedance for the low power mode. The parasitic resistance of the large inductance degrades the improvement of the efficiency in the low power region.

In this study, a dual-primary transformer is proposed to remove the degradation of the efficiency improvement in the low-output power region for polar transmitters. Since the transformer has dual-primary parts, which have different inductances, capacitances, and different impedance transformation ratios, the transformer has dual load impedances for the high and low power modes. The transformer is used for power combining and impedance matching in the stage-convertible power amplifier.

In Section II, the efficiency of the power amplifier for polar transmitter applications is explained. In Section III, the structure of the stage-convertible power amplifier and problems of the structure are presented. Section IV presents the output transformer, and the operation of the dual-primary transformer is explained. In Section V, the structure of the power amplifier is explained and the merit of the proposed amplifier is shown. In Section VI, the measurements are shown.

II. Efficiency of Power Amplifier for Polar Transmitters

Generally, the input signal of a power amplifier for polar transmitters is split into two signals: an amplitude signal and a phase signal. The amplitude signal is used in a power amplifier as a supply voltage. The amplitude of the RF phase input of the power amplifier always remains constant. The output power of the power amplifier is determined by the supply voltage. Thus, the gain of the amplifier for polar transmitters varies according to the supply voltage.

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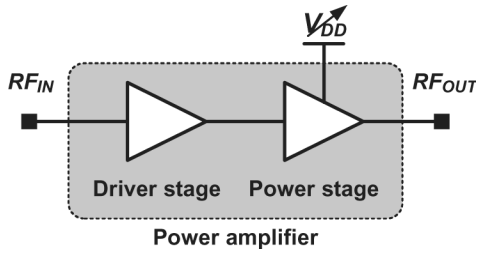

Fig. 1. Block diagram of a conventional power amplifier for polar transmitters.

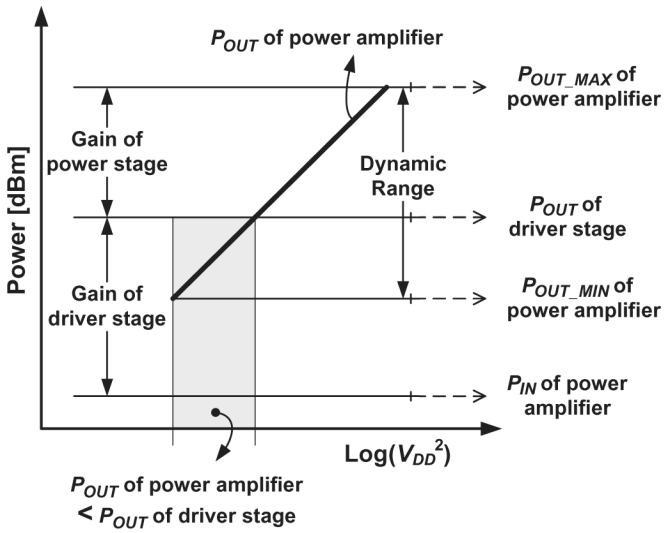

Fig. 2. Output power versus $\mathrm{Log}(V_{DD}^2)$ of a conventional power amplifier.

A conventional power amplifier for polar transmitters is shown in Fig. 1. The supply voltage of the driver stage is fixed in Fig. 1. The output power of the driver stage is, therefore, always constant. While the supply voltage of the power stage varied to control the output power of the power amplifier, a region where the output power of the driver stage is higher than that of the power stage may be encountered, as shown in Fig. 2. The efficiency of the low-output power region is, therefore, degraded seriously. To improve the average power efficiency of the polar transmitter, the efficiency at the low-output power must be improved.

One of the most popular methods to improve the efficiency is the variable load technique, as shown in Fig. 3 [9]. For the high power mode, the variable load becomes low impedance. For the low power mode, the load becomes high impedance. Thus, the variable load power amplifier has high maximum output power at the high output power mode and high efficiency at the low-output power mode. However, although the method is very effective for linear power amplifiers, the same problem with the conventional power amplifier still exists in the variable load power amplifier for the polar transmitter.

To overcome the low efficiency during low-output power, the topology of split power amplifier was studied, as shown in Fig. 4 [12]. However, the split power amplifier requires an additional power stage to improve low efficiency in the low-output power region. Thus, the complexity of the split power amplifier is higher than that of the conventional power amplifier.

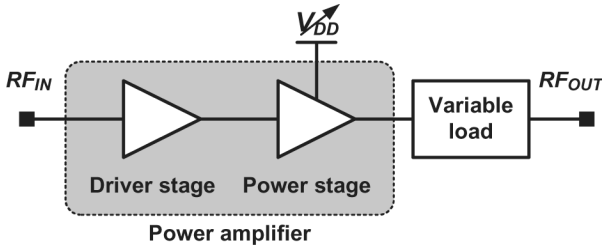

Fig. 3. Block diagram of a variable load power amplifier for polar transmitters.

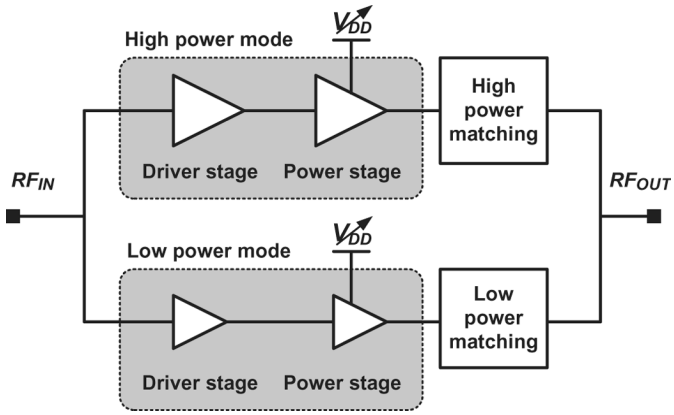

Fig. 4. Block diagram of a split power amplifier for polar transmitters.

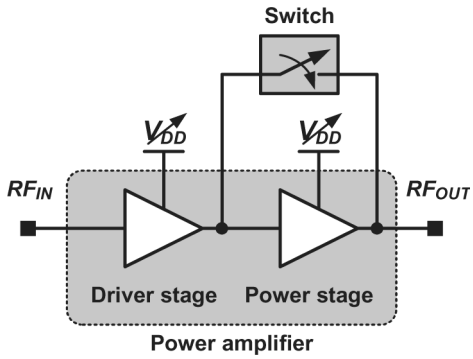

Fig. 5. Block diagram of an amplifier with a switched gain stage for polar transmitters.

A possible solution to improve the efficiency in the low-output power region is an amplifier with a switched gain stage [8]. The topology does not require an additional power stage for the low power mode to increase the efficiency. Fig. 5 shows the power amplifier with a switched gain stage for the polar transmitter. At the low power mode, the power stage is turned off and is bypassed. The output of the amplifier is determined by the driver stage. The driver stage alone then generates the output power. Thus, the dc power loss at the power stage is removed. As a result, the efficiency could be increased. Thus, the topology uses the driver stage as a driver stage for the high power mode and as a power stage for the low power mode. The output power of the driver stage must also be varied for polar transmitters. Thus, the supply voltage of the driver stage becomes one of the inputs for the polar transmitters. However, the loss induced by the additional switch degrades the efficiency improvement of the low power mode.

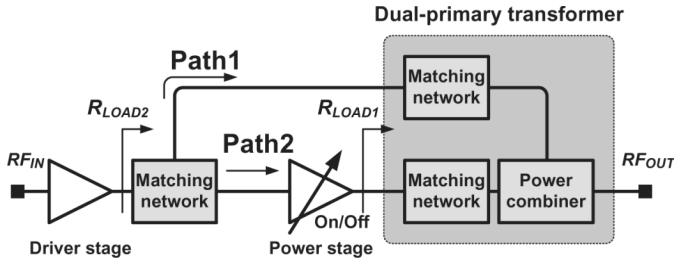

Fig. 6. Block diagram of the stage-convertible power amplifier for polar transmitters (after [10] and [11]).

III. Structure of Proposed Power Amplifier

A. Stage-Convertible Power Amplifier

Fig. 6 shows the topology of a stage-convertible power amplifier [10], [11]. The topology is a modified version of the power amplifier with a switched gain stage. The switch is replaced by matching networks. The output impedance R_L of the stage-convertible power amplifier must be low to get high maximum output power [10], [11]. The output impedance R_H of the amplifier must be high due to the matching network, which is located between the output and input of the power stage.

1) High Power Mode: In the high power mode, the driver stage functions as a driver amplifier of the power stage. The power generated in the power stage and the power transmitted through path 1 are combined at the power combiner shown in Fig. 6. However, the power generated in the power stage is much higher than the power transmitted through path 1. Thus, the output power of the power amplifier is almost the same as the output power of the power stage.

2) Low Power Mode: In the low power mode, the driver stage functions as a power stage because the power stage is turned off and the output power of the driver stage is transmitted to the output of the power amplifier through the matching network and the power combiner. Since the driver stage generates low-output power, the R_H may be increased. The matching network located between the input of the power stage and the output of the driver stage includes the parasitic capacitances of the power stage. The efficiency of the low power mode could then be increased with the high value of R_H [10], [11]. Additionally, the dc power loss at the power stage is removed during the low power mode. As a result, the efficiency could be substantially increased.

The stage-convertible power amplifier has no additional stages or switches on the signal path to change the mode of a power amplifier. Simply turning on or off the power stage is enough to change the mode of the power amplifier. The topology is, therefore, more efficient than that of a power amplifier with a switched gain stage and a split power amplifier. In this study, the matching networks and power combiner are designed with a proposed dual-primary transformer.

B. Problems of Phase Difference in the Power Combiner

One of the most important design issues of a stage-convertible power amplifier is the combining of the powers through paths 1 and 2, as shown in Fig. 6. The phase difference between the signals of paths 1 and 2 degrades the output power and efficiency

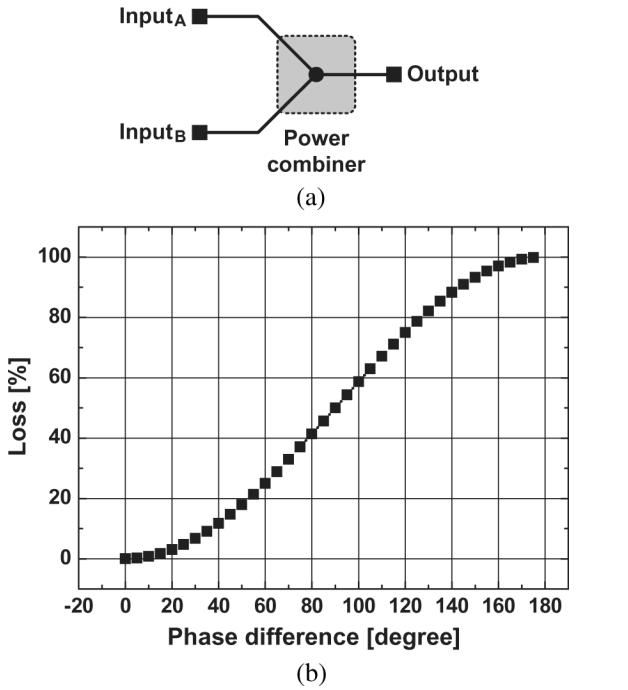

Fig. 7. Simulated loss induced by phase difference. (a) Schematic for the simulation. (b) Simulation results.

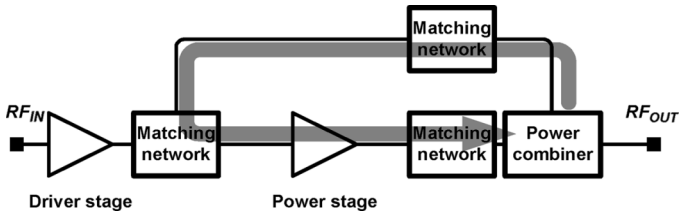

Fig. 8. Feedback loop of the stage-convertible power amplifier.

of the stage-convertible power amplifier. Fig. 7 shows the simulated loss induced by the phase difference between two paths. If the phase difference between the two paths is 20°, 97% of input power is transferred into the output of the power amplifier. In the design of the stage-convertible power amplifier, the target of the phase difference was lower than 10°. Under 10° of phase mismatch, the loss is negligible, as shown in Fig. 7.

C. Stability Issues

As shown in Fig. 8, the feedback loop is made in the stage-convertible power amplifier. The arrow indicates the feedback loop. The feedback loop can create serious problems for linear power amplifier applications because the output power must be determined by the input power. However, the output power may not be controlled by the input power since the amplifier oscillates. Thus, to apply the stage-convertible topology to linear power amplifier applications, careful precautions must be taken to prevent the oscillation. However, the stability problems induced by the feedback loop may not be serious for nonlinear power amplifiers. In the polar transmitter, they can use a nonlinear amplifier. The RF input power of the power amplifier is, therefore, always constant. The output power of the amplifier is controlled not by the input power, but by the supply voltage of

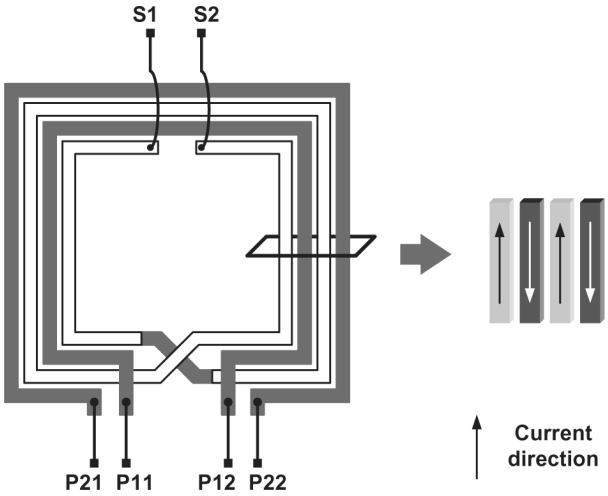

Fig. 9. Simplified structure of the proposed dual-primary transformer.

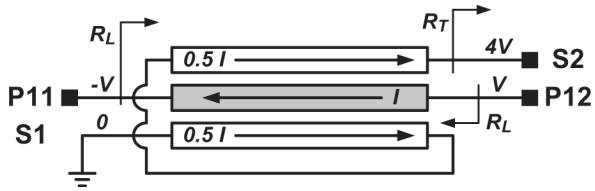

Fig. 10. Equivalent structure of the dual-primary transformer for low load impedance.

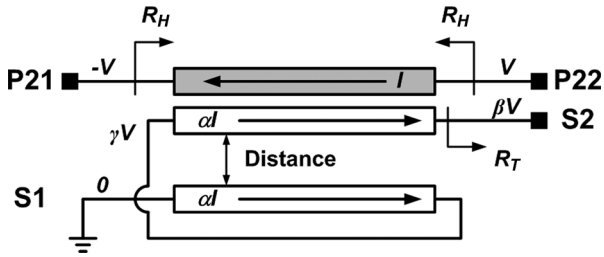

Fig. 11. Equivalent structure of the dual-primary transformer for high load impedance.

the amplifier. Generally, the RF input power $(\mathrm{RF_{IN}})$ of the amplifier for global system for mobile communication (GSM) and EDGE applications is between 0–5 dBm. Under these RF input powers, the oscillation does not occur and unwanted frequency components induced by the oscillation can be eliminated.

IV. Design of the Proposed Power Amplifier

A differential structure is applied to the proposed power amplifier to create a virtual ground, which prevents gain reductions due to wire bonding to grounds. Another important advantage of the differential structure is that load impedance R_{LOAD} can be two times larger than that of a single-ended structure. A dual-primary transformer is used as the output transformer. With the parasitic capacitance of the power transistor and an additional metal–insulator–metal (MIM) capacitor, the output matching network is completed.

A. Proposed Dual-Primary Transformer

A dual-primary transformer is proposed to implement a stage-convertible power amplifier. The dual-primary transformer is used as matching networks and a power combiner. The simplified structure of the dual-primary transformer is shown in Fig. 9. The transformer consists of a secondary part and two primary parts. One of the two primary parts is connected to the power stage. The other primary part is connected to the driver stage. In the physical structure of the transformer, the turn number of the secondary part is 2 and those of the two primary parts are 1, as shown in Fig. 9. The current directions of the two primary parts are designed to be the same. According to the basic theory of the transformer, the current direction of the secondary part is opposite to those of the primary parts. The secondary part is located in both sides of the inner primary part. However, the secondary part is located at only one side of the outer primary part, as shown in Fig. 9. Note that the ports of the inner primary part are connected to the power stage for high power mode. The ports of the outer primary part are connected to the power stage for the low power mode.

Figs. 10 and 11 show the operation of the proposed dual-primary transformer. The outer primary part is removed in the analysis of the relationship between the secondary part and inner primary part to simplify the analysis of the transformer. Similarly, the inner primary part is removed in the analysis of the relationship between the secondary part and outer primary part. In Fig. 10, the inner primary part and secondary part of Fig. 9 are simplified. If the current (I) flows from P12 to P11, the current flowed through the secondary part is 0.5 I. If the voltage drop between P11 and P12 is 2 V, as shown in Fig. 9, the voltage drop between S1 and S2 is 4 V. We assumed that the port S1 is connected to the ground and the port S2 is connected to the 50-Ω terminal. The equivalent resistance R_L and R_T can then be calculated by

$$R_L : R_T = \frac{V}{I} : \frac{4\ \mathrm{V}}{0.5\ I} = 1 : 8 = 6.25\ \Omega : 50\ \Omega \qquad (1)$$

where R_L is R_{LOAD} for the high power mode and R_T is the impedance of the terminal. If the parameter T is defined as the ideal impedance transformation ratio R_T/R_L, T of the transformer, shown in Fig. 10, is eight. To ports P11 and P12, the differential power stages are connected. The power generated by each power stage can be calculated by

$$P_{\mathrm{OUT}} \propto \frac{V_{DD}^2}{R_{\mathrm{LOAD}}} \qquad (2)$$

where P_{OUT} is the output power of the amplifier, V_{DD} is the supply voltage, and R_{LOAD} is the load impedance of the power stages. In this case, the R_{LOAD} is R_L. If the parameter N is defined as the number of power stages, N is 2 for the inner primary part. Thus, the total output power is the summation of the powers generated by the two power stages. Additionally, the power generated by the power stage is related with R_{LOAD}. If the terminal impedance of the power amplifier is 50 Ω, R_{LOAD} can be calculated by 50 Ω/T. Thus, the total output power generated by the multipower stages can be explain as

$$P_{\mathrm{OUT}} \propto N \cdot \frac{V_{DD}^2}{R_{\mathrm{LOAD}}} = N \cdot \frac{V_{DD}^2}{50/T} = (N \cdot T) \cdot \frac{V_{DD}^2}{50}. \qquad (3)$$

As shown in (3), $N \times T$ must be increased to obtain high output power. In the transformer, which is made by the secondary part and the inner primary part, $N \times T$ is 16.

In Fig. 11, the outer primary part and secondary part of Fig. 9 is simplified. In the analysis of the relationship between the outer primary part and secondary part, the secondary part can be considered as two parts. One of the parts is the secondary part, which adjoins the outer primary part. The other part is the secondary part, which is located away from the outer primary part. The magnetic coupling between the primary part and secondary part, which is located away from the outer primary part, is expected to be very weak. If the current I flows from P21 to P22, the current flowed through the secondary part can be assumed as αI. α is almost 1. β is almost 2, and γ is almost 0, as followed by

$$0.5 < \alpha < 1 \tag{4}$$

$$2 < \beta < 4 \tag{5}$$

$$0 < \gamma < 2 \tag{6}$$

$$\therefore\ 2 < \frac{\beta}{\alpha} < 8. \tag{7}$$

T of the transformer, shown in Fig. 11, is, therefore, close to two. The equivalent resistance R_H and R_T can then be calculated by

$$R_H : R_T = \frac{V}{I} : \frac{\beta V}{\alpha I} = 1 : \frac{\beta}{\alpha} \approx 1 : 2 = 25\,\Omega : 50\,\Omega \tag{8}$$

where R_H is R_{LOAD} for the low power mode. In the transformer, which is made by the secondary part and the outer primary part, $N \times T$ is almost 4. Thus, if we assumed perfect magnetic coupling and no loss of the metal lines, the power generated by the power stage is four times higher than that by the driver stage.

We need a very low level of R_{LOAD} to ensure that the maximum output power in a power amplifier reaches a high level. However, for the low power mode, we must increase the R_{LOAD} of a power amplifier in order to achieve high efficiency. As shown in the following equation, if the R_{LOAD} increases, we can increase the efficiency under low-output power:

$$\text{Efficiency} \propto \frac{R_{\mathrm{LOAD}}}{R_{\mathrm{ON}} + R_{\mathrm{LOAD}}} \tag{9}$$

where R_{ON} is the on resistance of power transistors. Thus, to simultaneously get a high maximum P_{OUT} in the high power mode and a high efficiency in the low power mode, we need to have dual load impedances. The value of parameter T must be decreased to get a high load impedance using the transformer. As shown in (1) and (8), the T for the low power mode is lower than that for the high power mode. Thus, R_H is higher than R_L. The dual-primary transformer can, therefore, be used to increase the efficiency at the low-output power region of the power amplifier.

B. Structure of the Power Amplifier Using a Dual-Primary Transformer

The dual-primary transformer is used as a power combiner, and a matching network, as shown in Fig. 12, is used to improve

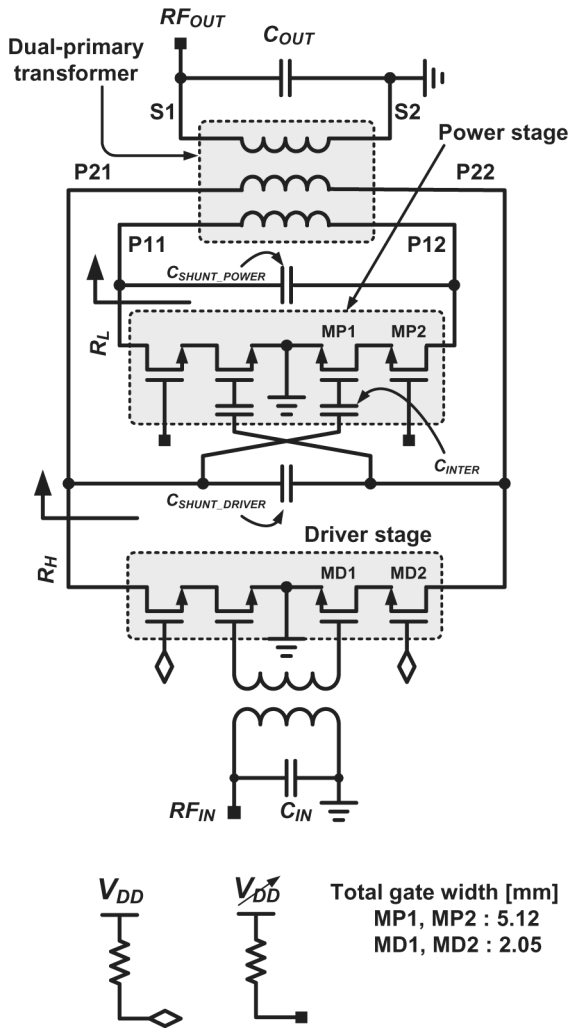

Fig. 12. Schematic of the designed power amplifier using a dual-primary transformer.

the efficiency in the low-output power region. Fig. 12 shows the simplified schematics of the proposed power amplifier. The output of the driver stage is connected to the gate of the power stage through the capacitor and to the dual-primary transformer. The phase difference between P21 (or P22) and P11 (or P12) was minimized using the inductances of the dual-primary transformer and the capacitances including a MIM capacitor and the parasitic capacitance of a MOS transistor. At maximum output power conditions, the power stage and driver stage work as class E to increase the efficiency.

In Section IV-A, simplified models of a transformer are used for the intuitions of the low power and high power modes of the designed power amplifier. However, the impedance transformation ratios shown in Section IV-A will change in an actual case due to the various parasitic components of the transformer. Accordingly, the S-parameters of the designed transformer were simulated to confirm the actual impedance transformation ratio. Figs. 13 and 14, respectively, show the simulated R_L and R_H results of Fig. 12. The dual primary transformer used in Fig. 12 was designed using a 2.5-D electromagnetic (EM) simulator. The simulated real part of R_L is 7.9 Ω at 1.8 GHz, as shown in

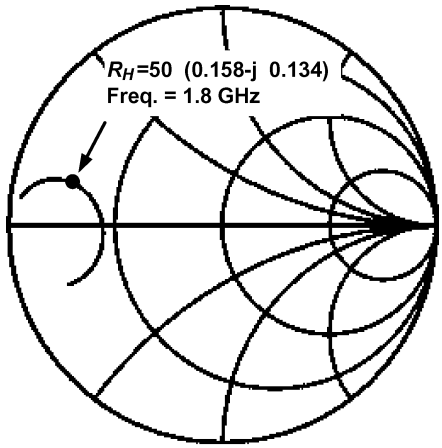

Fig. 13. Simulated S-parameter to check R_L of Fig. 12.

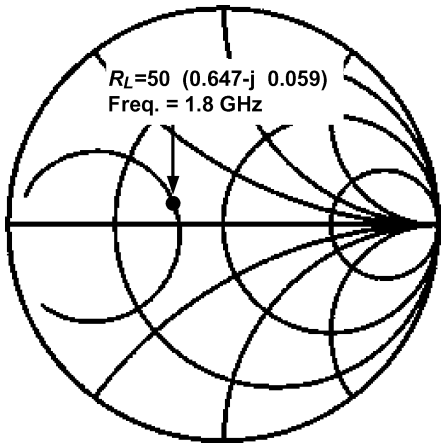

Fig. 14. Simulated S-parameter to check R_H of Fig. 12.

Fig. 13. The simulated real part of R_H is 32.35 Ω at 1.8 GHz, as shown in Fig. 14.

With the additional MIM capacitors, the parasitic capacitance of power transistors, and the inductances of input and output transformer, an input and output matching to 50 Ω load was achieved. The inductance of the primary part of the input transformer is cancelled out with $C_{\rm IN}$. The inductance of the secondary part of the input transformer was cancelled out with the parasitic gate–source capacitance of the MD1. The output voltage waveform of driver stage is controlled with the inductance of the high load impedance primary part of the dual-primary transformer and $C_{\rm SHUNT\_DRIVER}$. The voltage waveform of the drain of the power stage is controlled with inductance of the low load impedance primary part of the dual-primary transformer and $C_{\rm SHUNT\_POWER}$. With $C_{\rm INTER}$, the power, which is transferred to path 2 of Fig. 12, is controlled. $C_{\rm OUT}$ and the inductance of the dual-primary transformer form a low-pass filter. The low-pass filter suppresses the harmonic components of the amplifier. An additional notch filter may be helpful to suppress the harmonic components.

Fig. 15 shows the circuit configurations of the high power mode, low power mode, and auto-switching mode [1]. Since the output power of the power amplifier has to be determined by the driver stage in the low power mode, the supply voltage of

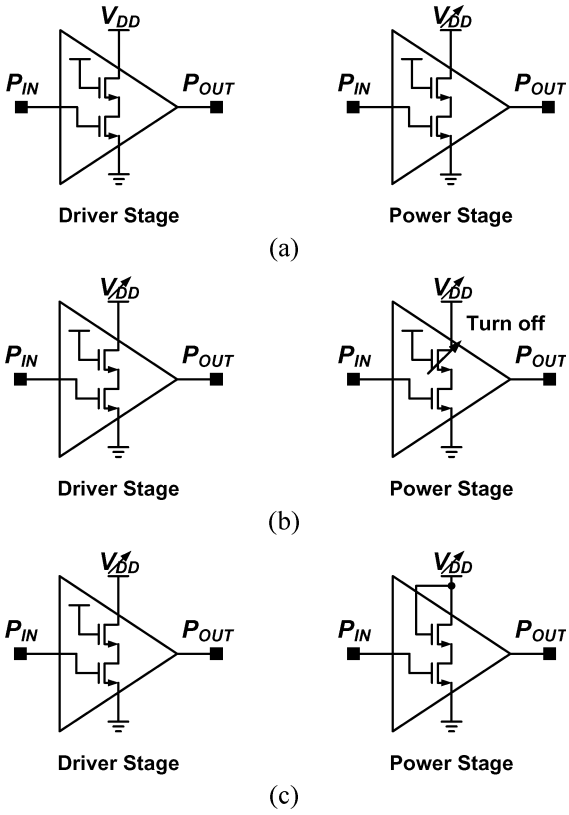

Fig. 15. Circuit configuration of: (a) high power mode, (b) low power mode, and (c) auto-switching mode (after [11]).

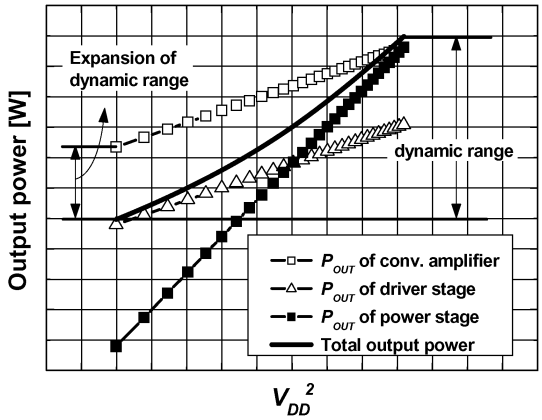

Fig. 16. Output powers of the driver stage and power stage during auto-switching mode.

the driver stage also varies. In the high power mode, all of the stages are turned on. In the low power mode, the power stage is turned off using the common-gate power transistors of cascode structures. In the auto-switching mode, the gate voltages of the common-gate power transistors of the cascode structure of the power stage are bound to the variable supply voltage.

Fig. 16 shows the simulated output powers of the driver stage, power stage, and power amplifier in the auto-switching mode. As a reference, the output power of a conventional power amplifier, as shown in Fig. 1, is shown in Fig. 16. As the supply voltage is decreased, the output power of the driver stage decreases. The output power of the power stage decreases more

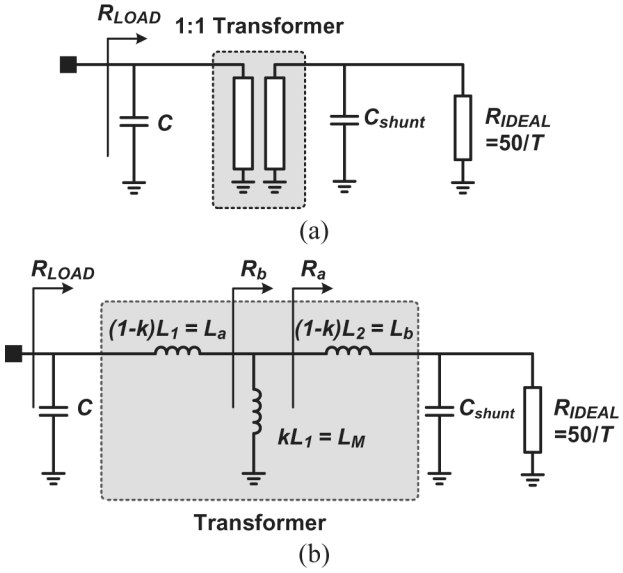

Fig. 17. (a) Output matching network. (b) Equivalent circuit for the output matching network (after [11]).

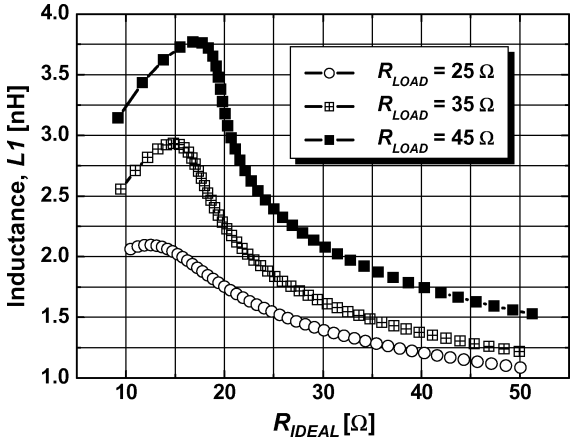

Fig. 18. Calculated inductance for a low power mode matching network.

rapidly as the supply voltage is decreased because the input power of the power stage also decreases as the supply voltage decreases. However, the input power of the driver stage is constant. The output power of the power amplifier is the summation of the output powers of the power stage and the driver stage, as shown in Fig. 16, in the auto-switching mode. Thus, all of the stages are turned on in the auto-switching mode. However, in the low supply voltage region, the output power of the amplifier is almost the same as that of the driver stage. In the high supply voltage region, the output power of the amplifier is almost the same as that of the power stage. Thus, there is no abrupt change point in the output power of the amplifier in the auto-switching mode.

C. Efficiency Improvement in Low Power Mode

As described in Section IV-A, to improve the efficiency in the low-output power region, the ideal impedance transformation ratio "T" must be decreased. The ideal impedance transformation ratio "T," described in Section IV-A, is calculated under the assumption of ideal transformation characteristics. However, in real transformers, there exist parasitic components, e.g., parasitic inductances, parasitic capacitances, and parasitic resistances. Thus, the real impedance transformation ratio may be changed because of the parasitic components of the transformer.

From a previous study [11], the impedance transformation using a transformer and additional capacitor is analyzed as in Fig. 17. In Fig. 17, T is the ideal impedance transformation ratio. The transformer is modeled using the coupling factor (k), mutual inductance (L_M), self-inductance of the primary part (L_1), and self-inductance of the secondary part (L_2).

In [11], the relationship between the parameters are derived as

$$L_b = \frac{R_{\mathrm{IDEAL}}^2 C_{\mathrm{shunt}}}{1 + (\omega R_{\mathrm{IDEAL}} C_{\mathrm{shunt}})^2} \tag{10}$$

$$\therefore\ C = \frac{\omega^2 L_a L_M^2 + R_a^2 (L_a + L_M)}{\omega^4 L_a^2 L_M^2 + \omega^2 (L_a + L_M)^2 R_a^2} \tag{11}$$

$$R_{\mathrm{LOAD}} = \frac{\omega^2 R_a L_M^2}{R_a^2 \left[1 - \omega^2 C (L_a + L_M)\right]^2 + \omega^2 L_M^2 (1 - \omega^2 L_a C)^2}. \tag{12}$$

Using the equations, the relationship between L_1 and R_{LOAD} can be calculated according to the values of 50 Ω/T, as shown in Fig. 18. To improve the efficiency in the low power region, high load impedance is needed. In (12), R_{LOAD} denotes the load impedance of the amplifier. The value of R_{LOAD} must be increased, therefore, in the low power mode. As shown in Fig. 18, the higher the value of T, the needed inductance, the higher L_1 must be to get the same R_{LOAD}. If the value of L_1 is increased, the length of the primary part must also be increased. If the length of the primary part is increased, the parasitic resistance of the primary part is also increased. The high inductance of the primary part means high resistance associated with the primary part. Thus, to reduce the resistance induced by the primary part, the value of T must be reduced.

D. Comparison of the Efficiency Improvement With Previous Work

In [11], to improve the efficiency in the low-output power region, a three-port asymmetric transmission line transformer was used. In that study, two differential pairs of power stages were needed for the watt-level maximum output power. Accordingly, the same number of differential pairs of driver stages was required to remove the phase differences between the power and driver stages due to the characteristic of the three-port asymmetric transmission line transformer. In that study, to achieve the high load impedance for low power mode, high inductance of the primary part is needed. That means the losses induced by the primary part for low power mode degraded the improvement of the efficiency at the low-output power region. Fig. 19 shows the simplified schematics of the previous study [11]. The high power stages are turned off and only the low power stages work at the low power mode. A simplified schematic for the low power mode in the referenced work [11] is shown in Fig. 20(a). From the relationship of the voltage and current between the

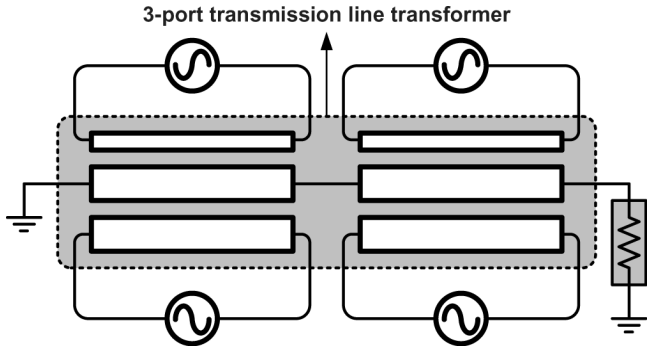

Fig. 19. Simplified structure of the three-port asymmetry transformer (after [11]).

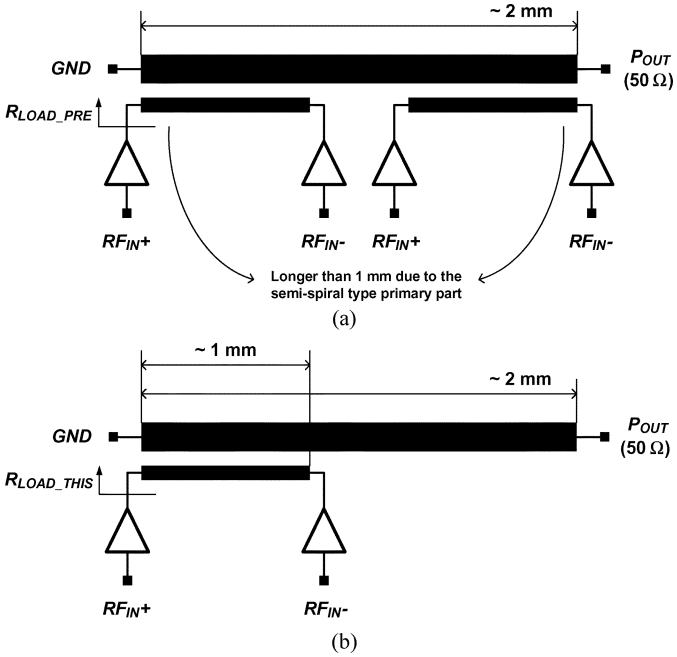

Fig. 20. Simplified equivalent circuits of low power modes for: (a) the previous study [11] and (b) this study.

secondary part and primary part for the low power mode, the $R_{\mathrm{LOAD\_PRE}}$ value can be calculated by

$$R_{\mathrm{LOAD\_PRE}}(\mathrm{ideal}) : R_T = \frac{V}{I} : \frac{4\ \mathrm{V}}{0.5\ I} = 1:8 = 6.25\ \Omega : 50\ \Omega \tag{13}$$

where $R_{\mathrm{LOAD\_PRE}}(\mathrm{ideal})$ is the ideal $R_{\mathrm{LOAD\_PRE}}$ and R_T is the terminal impedance of Fig. 20(a). The R_T value is assumed 50 Ω in (13). Thus, the ideal impedance transformation ratio T is 4 for the amplifier of the previous study. For the low power mode, the ideal output power $P_{\mathrm{OUT\_PRE}}(\mathrm{ideal})$ of this earlier study can be calculated by

$$P_{\mathrm{OUT\_PRE}}(\mathrm{ideal}) = 1.365 \frac{V_{DD}^2}{R_{\mathrm{LOAD\_PRE}}(\mathrm{ideal})} \times 4 \times \eta \tag{14}$$

where 4 is the number of driver stages and η is the efficiency of the amplifier.

However, the ideal impedance transformation ratio T becomes 2 for the low power mode in this study, as calculated in (8). For the low power mode, the output power in the this study can be calculated by

$$P_{\mathrm{OUT\_THIS}}(\mathrm{ideal}) = 1.365 \frac{V_{DD}^2}{R_{\mathrm{LOAD\_THIS}}(\mathrm{ideal})} \times 2 \times \eta \tag{15}$$

where 2 is the number of driver stages and η is the efficiency of the amplifier.

Ideally, if the terminal impedance R_T is 50 Ω, the $R_{\mathrm{LOAD\_PRE}}(\mathrm{ideal})$ value is 12.5 Ω and the $R_{\mathrm{LOAD\_THIS}}(\mathrm{ideal})$ value is 25 Ω, as calculated by (13) and (8), respectively. However, the load impedances of the stages can be designed by the length, width, and structure of the primary part, as mentioned in Section IV-C. Assumed here is that $P_{\mathrm{OUT\_THIS}}(\mathrm{req})$ and $P_{\mathrm{OUT\_PRE}}(\mathrm{req})$ are the required output powers for the low power modes of this and the earlier referenced work, respectively. In this case, if $P_{\mathrm{OUT\_THIS}}(\mathrm{req})$ and $P_{\mathrm{OUT\_PRE}}(\mathrm{req})$ are equal for a given V_{DD}, the relationship between $R_{\mathrm{LOAD\_THIS}}(\mathrm{req})$ and $R_{\mathrm{LOAD\_PRE}}(\mathrm{req})$ can be calculated by

$$P_{\mathrm{OUT\_PRE}}(\mathrm{req}) = P_{\mathrm{OUT\_THIS}}(\mathrm{req}) \tag{16}$$

$$\frac{V_{DD}^2}{R_{\mathrm{LOAD\_PRE}}(\mathrm{req})} \times 4 = \frac{V_{DD}^2}{R_{\mathrm{LOAD\_THIS}}(\mathrm{req})} \times 2 \tag{17}$$

$$2 \cdot R_{\mathrm{LOAD\_THIS}}(\mathrm{req}) = R_{\mathrm{LOAD\_PRE}}(\mathrm{req}). \tag{18}$$

If the 0.4 W of output power is desired while V_{DD} is 3.3 V and η in (14) and (15) is 50%, the required $R_{\mathrm{LOAD\_PRE}}$, $R_{\mathrm{LOAD\_PRE}}(\mathrm{req})$, is 74.25 Ω and the required $R_{\mathrm{LOAD\_THIS}}$, $R_{\mathrm{LOAD\_THIS}}(\mathrm{req})$, is 32.16 Ω. Thus, $R_{\mathrm{LOAD\_PRE}}(\mathrm{ideal}) = 12.5\ \Omega$ must be transferred into $R_{\mathrm{LOAD\_PRE}}(\mathrm{req}) = 74.25\ \Omega$ and $R_{\mathrm{LOAD\_THIS}}(\mathrm{ideal}) = 25\ \Omega$ must be transferred into $R_{\mathrm{LOAD\_THIS}}(\mathrm{req}) = 32.16\ \Omega$. The ideal load impedances and required load impedances for this and the preceding work are summarized in Table I.

TABLE I
SUMMARY OF IDEAL AND REQUIRED LOAD IMPEDANCES

Configuration	*Ideal* R_{LOAD} [Ω]	*Required* R_{LOAD} [Ω]
Previous work [11]	12.5	74.25
This work	25.0	32.16

R_T is assumed to be 50 Ω.

In conclusion, the required parasitic inductance of the primary part in the earlier referenced study is, therefore, higher than that of the present study, as described in Section IV-B and Fig. 18. Accordingly, the required length of the primary part in the earlier study is, therefore, longer than that in this study, as described in Section IV-B. The inductance and losses of the primary part for the low power mode can, therefore, be reduced in the present study compared to those in the earlier study. Thus, the degradation of the efficiency improvement induced by the associated resistance of the primary part in the low power mode is reduced compared to that in the earlier study.

However, the resistive loss induced by the secondary part in this study is nearly identical to that in the earlier work, as the length and width of the secondary part in the present investiga-

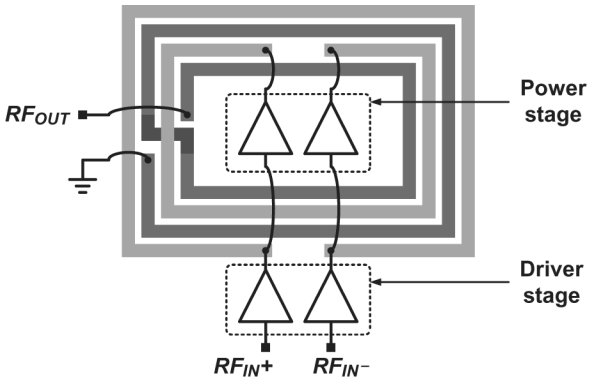

Fig. 21. Simplified structure of the dual-primary transformer.

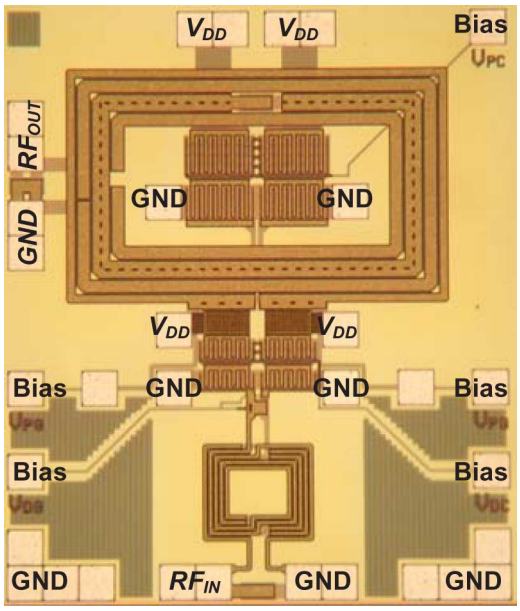

Fig. 22. Chip photograph of the implemented power amplifier.

tion are nearly identical to those in the earlier work, as shown in Fig. 20.

V. Implementation and Measurement Results

A. Implementation

The proposed power amplifier is implemented using a 0.18-μm RF CMOS process. The input and output transformers are implemented with 2.35-μm-thick top metal. The spacing between the primary and secondary parts of the output transformer is 3 μm. The width of the primary part for the low load impedance is 50 μm, and the width of the primary part for the high load impedance is 10 μm. The width of the secondary part is 30 μm. The size of the output transformer is 0.85×0.53 mm^2. The total gate lengths of MP1, MP2, MD1, and MD2 are 5120, 5120, 2048, and 2048 μm, respectively. The simplified structure of the proposed power amplifier is shown in Fig. 21. Fig. 22 shows a photograph of the designed power amplifier. The total chip size is 1.1×1.3 mm^2 including all the signal pads, dc pads, and test pads. To reduce the chip size, the power stage of the

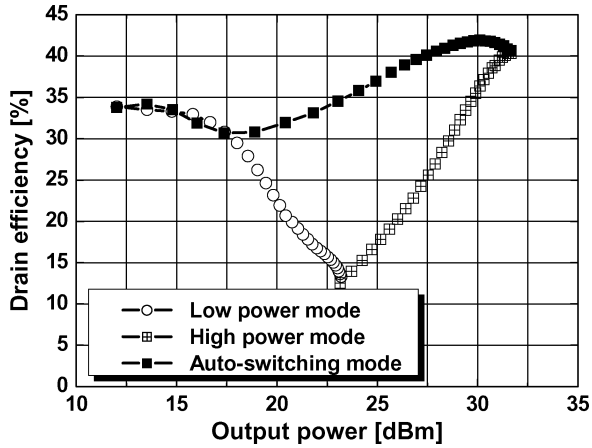

Fig. 23. Measured output power and efficiency of the low power, high power, and auto-switching modes.

proposed power amplifier is located in the output transformer. The fill patterns are removed around the output transformer to prevent the efficiency degradation of the output transformer. To predict the interactions between transformers, pads, and interconnect lines, the 2.5-D EM simulator is used. All of the metal lines used in the implementation of the proposed power amplifier are included in the 2.5-D EM simulation. Using 2.5-D simulation, the operation frequency of the designed circuit was predicted with very high accuracy. There was no frequency difference between simulation and measurement results. However, a 10% difference existed between the efficiencies between the 2.5-D simulation and measurement results. The reason for the difference is the higher Q factor of the 2.5-D simulation than that of the measurement.

The designed chip is glued directly to a gold-plated brass heat sink using conductive adhesive to allow enough thermal dissipation. The chip ground pads are wire bonded to the heat sink. The input and output are wire bonded to 50-Ω microstrip lines on a printed circuit board. The voltage supply and gate bias pads are also wire bonded. The inter-stage matching network is completed with a wire-bonded inductor between the MOS gates of the differential power stage.

B. Measurement Results

The input power of the power amplifier is fixed at 10 dBm since the power amplifier is designed for the polar transmitter applications. All the losses due to the bond wires are included in the measured results.

Fig. 23 shows the measured drain efficiency versus P_{OUT}, while V_{DD} varies from 0.5 to 3.3 V and the operation frequency is fixed at 1.8 GHz. Fig. 24 shows the frequency response under the maximum output power conditions. The single-ended output power is higher than 31 dBm over a frequency range of 1.68$\sim$2.00 GHz. Fig. 25 shows the measured second and third harmonics under auto-switching mode.

Fig. 26 shows a comparison graph between the drain efficiency in the previous work and that of the present study. The maximum output power in the present work is similar to that in the previous study [11]. However, the efficiency at 16 dBm in this study is higher than that in the previous work [11]. Thus,

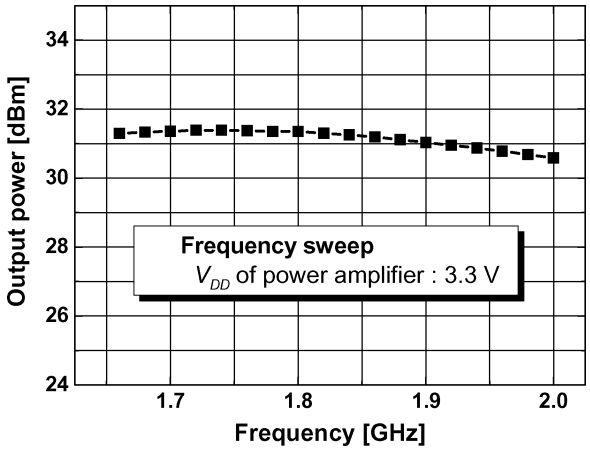

Fig. 24. Measured frequency response under maximum output power conditions.

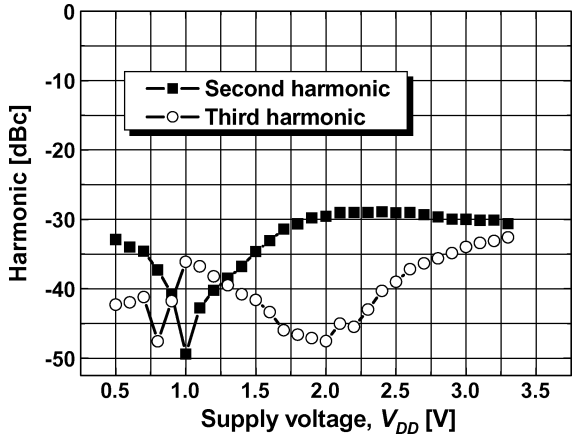

Fig. 25. Measurement results of harmonic components under auto-switching mode.

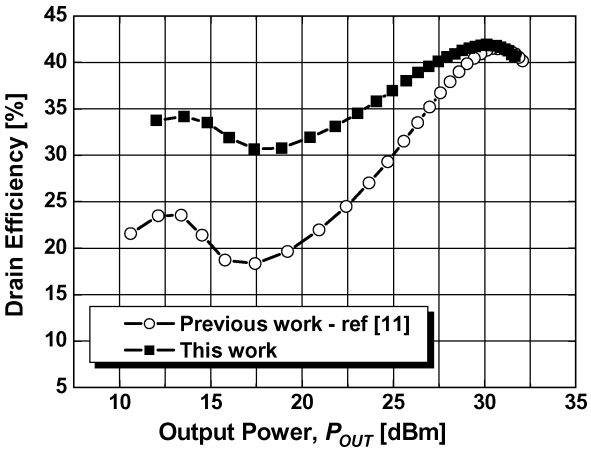

Fig. 26. Comparison graph: drain efficiencies of [11] and this study.

the degradation of the efficiency improvement in the low-output power region is reduced compared to the earlier study.

VI. Conclusion

A 1.8-GHz CMOS power amplifier for polar transmitters was implemented with a 0.18-μm RF CMOS process. The matching components, including the input and output transformers, were integrated. A dual-primary transformer is proposed in order to increase the efficiency in the low-output power region. The amplifier achieved a drain efficiency of 40.7% at a maximum output power of 31.6 dBm. The measured dynamic range was approximately 34 dB for a supply voltage that ranged from 0.5 to 3.3 V. The low power efficiency was 32% at an output power of 16 dBm.

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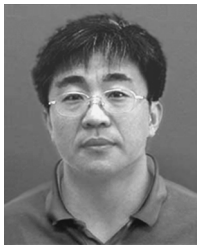

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