Voltage-Combined CMOS Doherty Power Amplifier Based on Transformer

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***Abstract*— This paper presents a voltage-combined CMOS Doherty power amplifier (PA) based on a transformer. The dynamic load modulation of the two-way transformer is analyzed in detail. A comparison between the current- and voltage-combined Doherty PAs shows that the Doherty PA based on a voltage-combining method delivers a broad bandwidth (BW) with a larger load tolerance. The proposed Doherty PA achieves close to ideal load modulation without additional offset line by manipulation of the output capacitances. For demonstration purposes, the PA and output combining transformer are implemented using a 0.18-μm CMOS process and an FR4 printed circuit board, respectively. The PA is tested at 880 MHz using a fully loaded long-term evolution signal with 16-quadrature amplitude modulation, 7.5-dB peak-to-average power ratio, and 10-MHz BW. The PA delivers a gain of 13.3 dB, a power-added efficiency of 47.4%, an error vector magnitude of 3.85%, and E – UTRA$_{\mathrm{ACLR}}$ of −33 dBc at an average output power of 27 dBm. This simple voltage-combined Doherty PA without any additional circuitry achieves good performance. These results show that the proposed CMOS Doherty PA is suitable for handheld PA applications.**

***Index Terms*— CMOS, Doherty, handset, long-term evolution (LTE), load modulation, power amplifier (PA), series combining, transformer, voltage combining.**

I. Introduction

RECENT wireless communication standards use complex modulation techniques to meet the demand for a high data rate within limited spectrum resources. Because spectrally efficient modulations are employed, the signals have high peak-to-average power ratios (PAPR) and wide channel bandwidths (BWs). Power amplifiers (PAs) for such systems should be efficient at the back-off output power as well as at the maximum rated power due to the large PAPR of the signals. PAs, one of the largest power consumers in handheld devices, should the efficiently operated to decrease heat dissipation and provide longer battery life.

To achieve high efficiency at the average output power level of the high PAPR signal, Doherty PA is an attractive choice [1]. The Doherty PA utilizes load modulation to provide the optimum load impedances for high efficiencies at the 6-dB power back-off (PBO) and the maximum rated output power. Doherty [1] introduced two amplifier configurations. One involved a shunt-connected load and the other involved a series-connected load. The first one is a well-known architecture because of its ease of construction [2], [3], and many studies of the shunt Doherty PA have been published [4]–[9].

Recently, series Doherty PAs were introduced. Kawai *et al.* [10] and Watanabe *et al.* [11] proposed series-connected Doherty PAs that used a lumped-element balun for base-station applications. Distortion analysis and miniature design of the series-connected Doherty PAs are described based on a lumped-element balun. For mobile applications, series Doherty PAs that use CMOS devices have been introduced [12]–[14]. These papers propose a Doherty PA based on a four-way structure and focus on an optimized design of the four-way transformer for combining power efficiently.

For proper Doherty operation, with high efficiency at the PBO, the load modulation is the most important element. In this paper, we analyze the basic load modulation principles of a series Doherty PA based on a two-way transformer. In Section II, through an ideal simulation using ideal current sources to represent transistors, we derive fundamental analyses of dynamic load modulation based on the voltage equation. With dynamic load modulation, the output voltages of the carrier and peaking amplifiers are properly combined by the transformer. The advantages of Doherty PAs based on a voltage-combining method are the large load tolerance and BW compared with the current combined structure; we describe these advantages in Section III. For the design of a CMOS Doherty PA, the series type is well-suited because the voltage combining method is advantageous for CMOS PAs [15]–[19]. The low breakdown and the low power density problems of the CMOS device are solved by increasing the output load impedance through the series modulation realized with an output transformer. We discuss implementation of a voltage-combined CMOS Doherty PA using a two-way transformer and then the linearity of the Doherty operation in Section IV. In Section V, we describe the experimental results.

II. Analysis of Voltage-Combined Doherty PA

Doherty introduced two types of concepts for the amplifier configuration. One involved a shunt-connected load and the other involved a series-connected load. In this section, we

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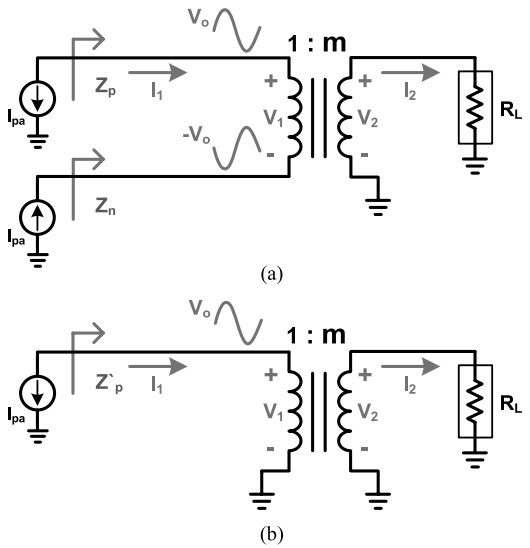

Fig. 1. Operational diagram of transformer-based (a) differential and (b) single-ended PAs.

analyze the load modulation principles of the series Doherty PA based on a two-way transformer.

A. Characteristics of Transformer With Static Load Modulation

Recently, we proposed a static load modulation PA based on the characteristics of a transformer [20]. We briefly review this work to analyze the dynamic load modulation of a Doherty PA. Fig. 1 shows a conceptual diagram of the transformer architecture. I_{pa} represents the current source of an amplifier. The transformer transforms the 50-Ω load impedance into a lower impedance at the primary for a power match to each unit amplifier and combines the output power from each unit amplifier at the secondary, using 1:m ratio. Based on the basic transformer theory

$$V_2 = m \cdot V_1 \tag{1}$$

$$I_2 = \frac{1}{m} \cdot I_1. \tag{2}$$

In the differential PA case shown in Fig. 1(a), the impedances are given by

$$R_L = \frac{V_2}{I_2} = \frac{2m^2 \cdot V_o}{I_1}, \quad \text{where } V_2 = 2m \cdot V_o \tag{3}$$

$$Z_p = Z_n = \frac{V_o}{I_1} = \frac{R_L}{2m^2}. \tag{4}$$

The turn ratio m can be designed to make Z_p and Z_n optimal. However, in the single-ended PA case shown in Fig. 1(b), the impedances are

$$R_L = \frac{V_2}{I_2} = \frac{m^2 \cdot V_o}{I_1}, \quad \text{where } V_2 = m \cdot V_o \tag{5}$$

$$Z'_p = \frac{V_o}{I_1} = \frac{R_L}{m^2}. \tag{6}$$

The optimum impedance Z'_p is two times larger, and the power cell size is one-half of the differential case. Therefore, by shorting one of the two halves of the PA, peak efficiency occurs at the 6-dB PBO under the single-ended operation with $2Z_p$ conditions. The transformer can modulate the load seen by each unit amplifier, and this load modulation principle can be extended to continuous dynamic load modulation in a Doherty PA.

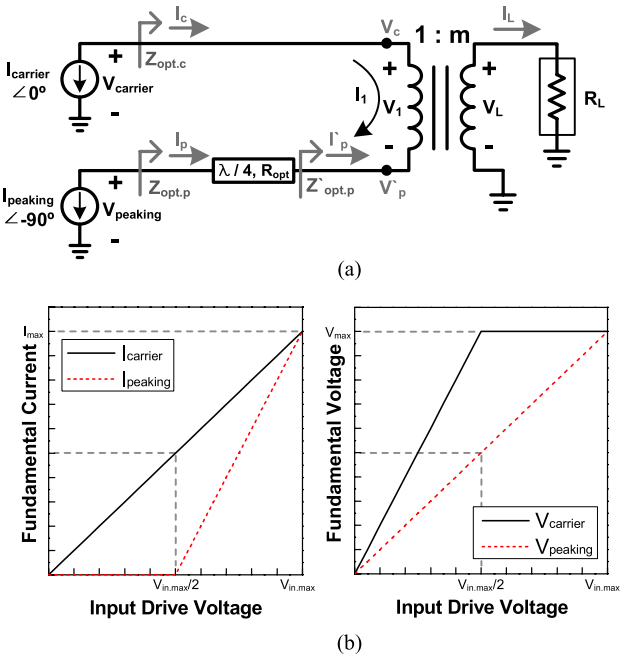

Fig. 2. (a) Operational diagram of voltage-combined Doherty PA with a two-way transformer. (b) Magnitudes of the fundamental current and voltage versus the input drive voltage.

B. Voltage-Combined Doherty PA With Dynamic Load Modulation

Fig. 2(a) shows a series Doherty PA based on a transformer. I_{carrier} and I_{peaking} are the carrier and peaking transistor's output current sources, respectively. It is assumed that each current source is linearly proportional to the input voltage signal after it is turned ON, operating as a class-AB or class-B amplifier with harmonic short circuits. Fig. 2(b) shows the fundamental current and voltage amplitudes according to the input drive voltage. As shown in Fig. 2(b), the peaking amplifier is designed to turn ON at one-half of the maximum input voltage. A phase-adjusting line should be inserted into the input side of the carrier or peaking amplifier to compensate for the output quarter-wave transformer. When two antiphased voltage signals are applied to the primary ports of the transformer, such as a differential pair, the two signals can be properly combined at the secondary output port.

In the low-power region (0 to $V_{\text{in.max}}/2$), the peaking amplifier remains in the cutoff state, and the load impedance of the carrier amplifier is two times larger than that of the conventional amplifier. The operation is the same as the single-ended operation explained in Section II-A. The peaking amplifier's output impedance is infinity due to the open states. The quarter-wave transformer inserted at the output of the peaking amplifier transfers it to a short condition at the V'_p node. However, the parasitic output capacitor disturbs the

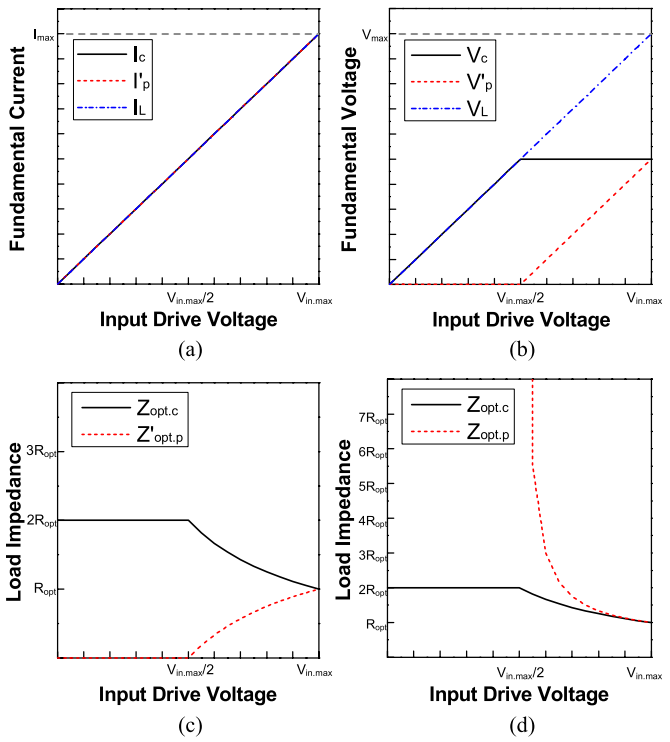

Fig. 3. (a) Magnitudes of the fundamental output current and (b) voltage at the combining nodes of transformer versus input drive voltage. (c) Load impedances at the primary ports of the transformer. (d) Load impedances of the Doherty transistors.

ideal operation, and the practical operation will be discussed in Section IV.

In the high-power region ($V_{\text{in.max}}/2$ to $V_{\text{in.max}}$), where the peaking amplifier is conducting, the voltage level of the peaking amplifier plays an important role in determining the load modulation of the Doherty amplifier. Assuming that the transconductance (gm) of the peaking amplifier is two times larger than that of the carrier amplifier, the current and voltage swings of the peaking amplifier increase in proportion to the input voltage level, and the voltage swing reaches the maximum voltage swing of $V_{\max}$ only at the maximum input voltage. The load impedance seen by the carrier and peaking amplifiers can be calculated using (1) and (2), and are given in (7) and (9), respectively (where $V_p' = 0$ to $-V_c$)

$$Z_{\text{opt.c}} = \frac{V_c}{I_c} = \frac{R_L \cdot V_c}{m^2\left(V_c - V_p'\right)}, \quad \text{where } I_c = I_1 \tag{7}$$

$$Z'_{\text{opt.p}} = \frac{V_p'}{I_p'} = \frac{R_L \cdot V_p'}{m^2\left(V_p' - V_c\right)}, \quad \text{where } I_p' = -I_1 \tag{8}$$

$$Z_{\text{opt.p}} = \frac{m^2 \cdot R_{\text{opt}}^2\left(V_p' - V_c\right)}{R_L \cdot V_p'}. \tag{9}$$

Therefore, the load impedance of each amplifier is dynamically modulated according to the input power level. Since the load impedance of the peaking amplifier depicted by $Z_{\text{opt.p}}$ should be decreased as the input voltage increases, the quarter-wave inverter is needed for proper modulation.

When $R_L = 2R_{\text{opt}}$ and $m = 1$ are assumed for a simple analysis, the calculated idealized results are shown in Fig. 3.

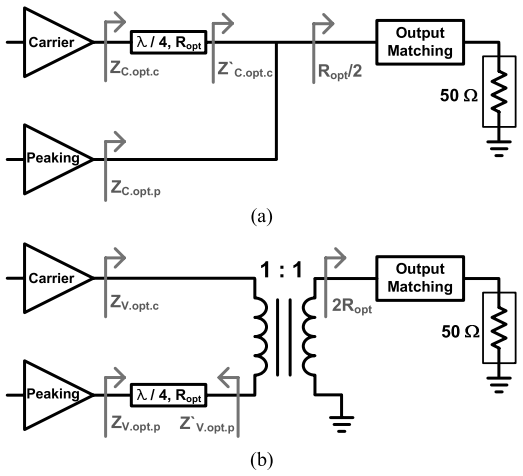

Fig. 4. Block diagrams of (a) current-combined Doherty PA and (b) voltage-combined Doherty PA based on a 1:1 transformer.

The magnitudes of the output currents I_c and I_p' at the primaries are the same as the I_L at the secondary (where $I_c = -I_p' = I_1$ and $I_L = I_1$) as shown in Fig. 3(a). The generated output voltages from the primaries are combined at the secondary of the transformer as shown in Fig. 3(b). In the low-power region, the load impedance of $Z'_{\text{opt.p}}$ at the combining node is maintained at zero, thanks to the quarter-wave inverter as shown in Fig. 3(c), and the carrier amplifier with the load impedance of $2R_{\text{opt}}$ achieves a peak efficiency at 6-dB PBO under the single-ended operation. In the high-power region, through (7) and (9), the transformer with the quarter-wave inverter properly modulates the load impedance seen by the each carrier ($2R_{\text{opt}}$ to R_{opt}) and peaking (∞ to R_{opt}) amplifiers as shown in Fig. 3(d).

III. Comparison Between Current- and Voltage-Combined Doherty PA

Fig. 4 shows current- and voltage-combined Doherty PAs. In theory, the junction impedance (R_{junction}) should be $R_{\text{opt}}/2$ for current-combined Doherty PAs to eliminate the matching circuits at the two amplifiers. Likewise, R_{junction} should be $2R_{\text{opt}}$ for the voltage-combined Doherty PAs for the same reason. The output capacitance effects can be embedded in the circuit element design as described in Section IV-A. This Doherty circuit topology provides the advantage of size for handset PAs. Therefore, the compact structures of the two Doherty PAs as shown in Fig. 4 are compared. A circuit node Q_n and a loaded Q_L for the output matching network are defined by

$$Q_n = \sqrt{\frac{R_L}{R_{\text{junction}}} - 1}$$
$$Q_L = \frac{Q_n}{2} = \frac{f_o}{\text{BW}} \tag{10}$$

where R_L and R_{junction} are the 50 Ω and the junction impedance, respectively. BW is inversely proportional to Q_n, and the smaller impedance transformation ratio results in a larger BW. If the R_{opt} is lower than 50 Ω, the output matching network of the voltage-combined case has an inherently larger

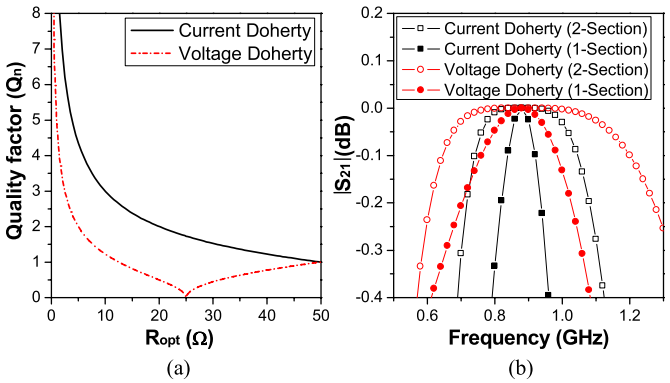

Fig. 5. (a) Quality factor (Q_n) of the output matching network versus the R_{opt}. (b) BW of the output network of one-section and two-section matching circuits using the lumped L, C elements (where $R_{\text{opt}} = 8\ \Omega$).

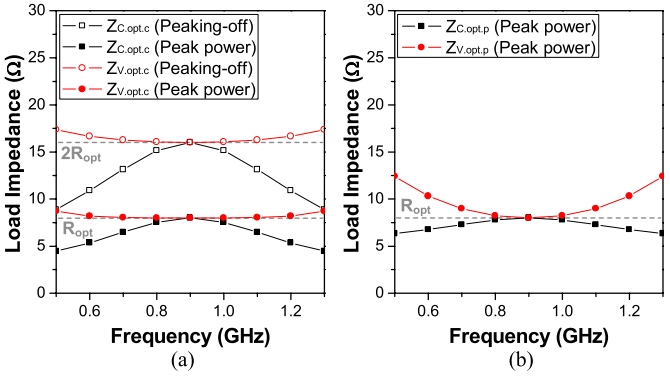

Fig. 6. (a) Magnitudes of the load impedances of the carrier amplifier at the low-power-region and the peak power region. (b) Magnitudes of the load impedance of the peaking amplifier at the peak power region.

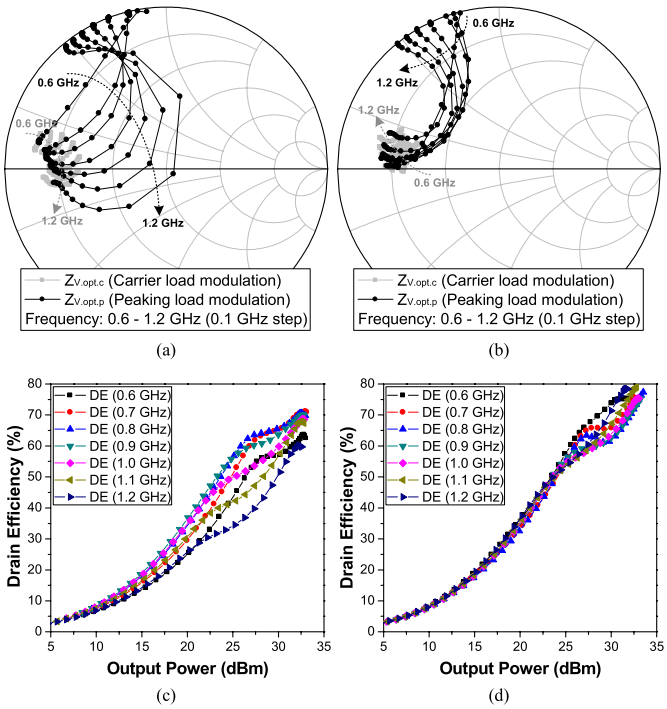

Fig. 7. Load impedance traces of (a) current-combined Doherty PA and (b) voltage-combined Doherty PA according to the frequency and the input power. Drain efficiency of (c) current-combined Doherty PA and (d) voltage-combined Doherty PA according to the frequency and the output power.

BW than the other, as shown in Fig. 5(a). In general, the R_{opt} of the watt-level handset PA is lower than 10 Ω. When the R_{opt} is 8 Ω, Fig. 5(b) illustrates the BW characteristics of each case using one-section and two-section (bandpass filter type having the lowest Q_n) output matching networks. The voltage-combined Doherty with a two-section matching network has a 64% fractional BW at a voltage standing wave ratio of 1.5, i.e., a 570-MHz BW at a 900-MHz center frequency. Furthermore, the 1:1 transformer and the output matching network can be merged into the output transformer that has a 1:m ratio, and the BW of the output transformer can be increased by the broadband technique of a transmission-line transformer [21].

To investigate the load sensitivity as well as the BW characteristic of the Doherty stage, except for the output matching network, an ideal simulation is conducted using the ideal current sources and the quarter-wave transmission line as shown in Fig. 2. R_{junction} as shown in Fig. 5(a) and (b) is given by the ideal load terms of $R_{\text{opt}}/2$ and $2R_{\text{opt}}$, respectively. The R_{opt} is 8 Ω and the center frequency is 900 MHz. In this simulation, only the quarter-wave transmission line can affect the load modulation of the Doherty PA according to the frequency variation. The simulation results are shown in Fig. 6. The load impedance of the carrier amplifier in the voltage-combined Doherty PA maintains almost $2R_{\text{opt}}$ and R_{opt} in the low- and high-power regions, respectively, while that of the current-combined Doherty PA deviates significantly. Since the $Z'_{\text{V.opt.p}}$ maintains the near short condition by the quarter-wave impedance inverter at the pinch-off state, the $2R_{\text{opt}}$ condition for the carrier amplifier in the low-power region is barely affected by the frequency variation. The peaking amplifier of the voltage-combined Doherty PA has a slightly larger load variation than the current-combined Doherty PA as shown in Fig. 6(b) because the quarter-wave transmission line that is inserted at the peaking amplifier output path directly affects the load condition of the peaking amplifier. To verify the ideal results, a harmonic balance simulation is conducted using a real CMOS transistor model (two-stacked power cell as shown in Fig. 9) instead of the ideal current sources and the results as shown in Fig. 7. The output- and input-matching variations are not considered for this simulation. The voltage-combined Doherty PA shows the proper load modulation trace over a broad BW compared with the current-combined Doherty PA as shown in Fig. 7(a) and (b). The transistors' output currents are influenced by the load conditions, differently from the ideal current sources. The load impedance of the carrier amplifier is dependent on the current level of the peaking amplifier and vice versa. Since the load condition of the peaking amplifier is affected by the load variation of the carrier amplifier, the peaking amplifier's load-trace variation of the voltage-combined Doherty PA is smaller than the current-combined Doherty PA, differently from the simulation that used ideal current sources. The voltage-combined Doherty PA delivers constant drain efficiency for a broader frequency band compared with the current-combined Doherty PA as shown in Fig. 7(c) and (d). Especially, the proposed Doherty PA shows almost the same efficiency at the low-power region,

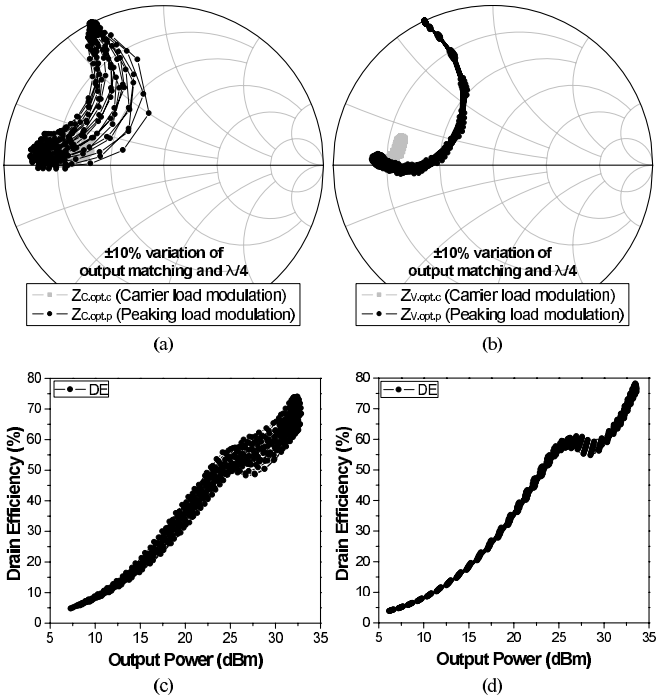

Fig. 8. Load impedance traces of (a) current-combined Doherty PA and (b) voltage-combined Doherty PA. Drain efficiency of (c) current-combined Doherty PA and (d) voltage-combined Doherty PA according to ±10% variation of both the output matching network and the phase of quarter-wave transformer.

because the carrier amplifier does not have the quarter-wave inverter and the load impedance is properly matched across the broad BW. Fig. 8 shows the simulation results for ±10% variation of both the output matching circuit and the phase of quarter-wave inverter. The voltage-combined Doherty PA has better ruggedness over the ±10% variation compared with the current-combined Doherty PA.

The voltage-combined Doherty PA has a low impedance transformation ratio from 50 Ω to $2R_{\text{opt}}$ instead of from 50 Ω to $R_{\text{opt}}/2$. The carrier amplifier that plays an important role in the Doherty operation is barely affected by the variation in the quarter-wave transmission line inserted at the peaking output path. Furthermore, when the peaking amplifier is turned OFF, the load impedance of the carrier amplifier easily maintains the $2R_{\text{opt}}$ condition by $Z'_{\text{V.opt.p}}$ with near short impedance for the frequency sweep. Therefore, the voltage-combined Doherty PA has an inherently larger load tolerance and a larger BW compared with the current-combined Doherty PA. The total BW of the voltage-combined Doherty PA is determined by the designed BW of the 1:m output transformer.

IV. Implementation of Proposed CMOS Linear Doherty PA

A. Design of Proposed Voltage CMOS Doherty PA

In general, the normal class-AB CMOS PA frequently employs the output transformer for voltage-combining method [15]–[19]. Therefore, the series combining is well suited for a CMOS Doherty PA. The low breakdown and low-power density problems of a CMOS device are alleviated by the Doherty amplifier's increased output load impedance (R_{junction} as shown in Fig. 5). R_{opt} of the carrier and peaking amplifiers can be easily modulated with an output transformer.

The schematic of the proposed CMOS Doherty PA including the output transformer is shown in Fig. 9. Thick-oxide 0.4-μm transistors are used in the common gate (CG) stage for reliable high power, and thin-oxide 0.18-μm transistors are used in the common-source (CS) stage to enhance the gm and gain. The total gate width of the thin and thick devices are 4800 and 9600 μm, respectively. The second harmonic short circuit implemented by a metal-insulator-metal capacitor and the inductance of a down-bonding wire are provided at the source of the CS stage to improve linearity by suppressing the series feed-backed second harmonic terms [17], [18]. The R_{CG}–C_{CG} bias circuits are inserted to control the voltage swing at the gates of the CG stages [19]. The $L_{\text{in.c}}$ and $L_{\text{in.p}}$ of the input matching networks transform the input impedance of the transistors to pure resistance of 12 Ω. A −90° high-pass T-type lumped quarter-wave transformer is inserted at the input path of the peaking amplifier to compensate for the phase of the output quarter-wave inverter.

The offset line is often employed to compensate for the output capacitance effect of the transistors since the Doherty modulation circuit handles real impedance only [4], [6]–[8]. However, the additional offset line in the conventional Doherty PA enlarges the chip and reduces the BW. Therefore, the output capacitances are de-embedded in the Doherty network components without generating any phase. Fig. 10(a) shows the output matching network of the proposed practical CMOS Doherty PA. The output capacitance of the two-stacked power-cell is nonlinear, varied with V_{DD} [22]. The average output capacitances of the carrier amplifier ($\overline{C_{\text{out.c}}}$) and the peaking amplifier ($\overline{C_{\text{out.p}}}$) are de-embedded in Z_{opt}s so that the loadline becomes purely resistive. Fig. 10(b) illustrates how to manipulate the output capacitances of the transistors without using offset lines. The overall circuit is shown in Fig. 9.

The $\overline{C_{\text{out.p}}}$ is merged into the quarter-wave inverter, a low-pass π-type, considering compact implementation. Thus, the first shunted capacitor (C_{p1}) of the lumped inverter is obtained by

$$C_{\text{inverter}} = \frac{1}{\omega R_{\text{opt}}} \tag{11}$$

$$C_{p1} = \frac{C_{\text{inverter}} - \overline{C_{out.p}}}{L_{\text{down}}(C_{\text{inverter}} - \overline{C_{\text{out.p}}})\omega^2 + 1} \tag{12}$$

where L_{down} is the inductance of the down-bonding wire of shunted C_{p1}.

Since the center tap of the output transformer is used as a biasing point for compact implementation, the $\overline{C_{\text{out.c}}}$ should be merged into the output transformer with C_1 and C_2 to eliminate the offset line for the carrier amplifier. The $\overline{C_{\text{out.c}}}$ can be manipulated by C_1 and the second shunted capacitor (C_{p2}) of the lumped inverter as shown in Fig. 10(b). The capacitances are obtained using a mathematical equation based on the simplified model shown in Fig. 11 [15]. L_1 and L_2 are the self-inductances of the transmission-line transformer,

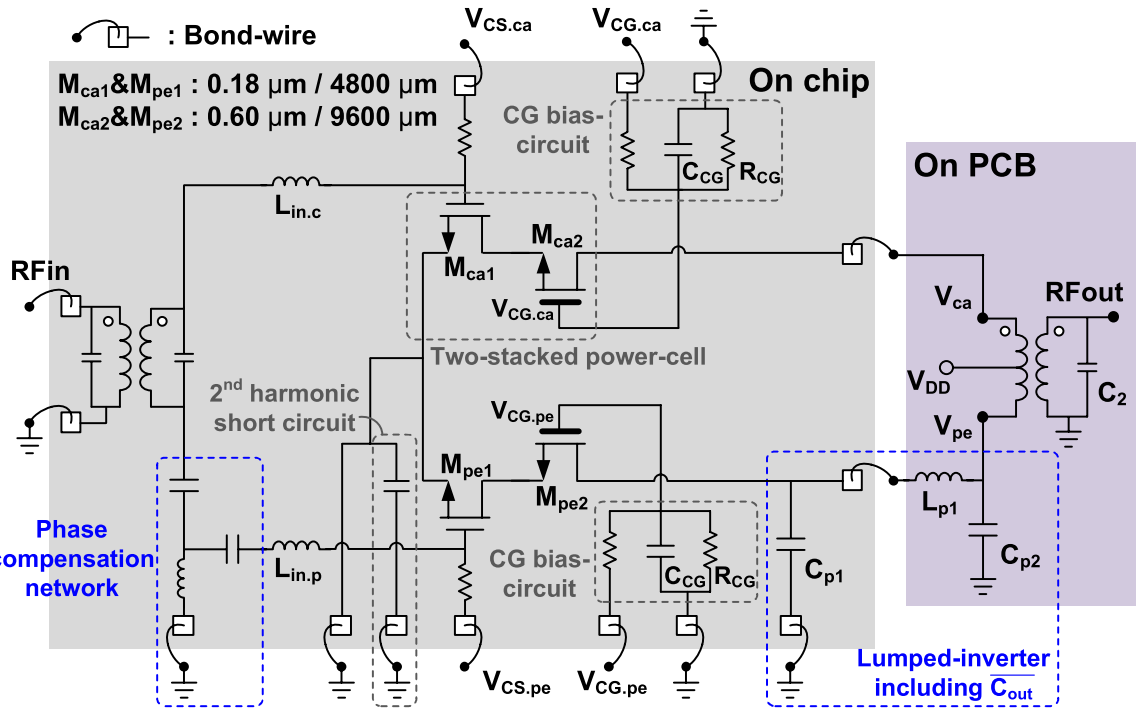

Fig. 9. Schematic of a voltage-combined CMOS Doherty PA based on the transformer.

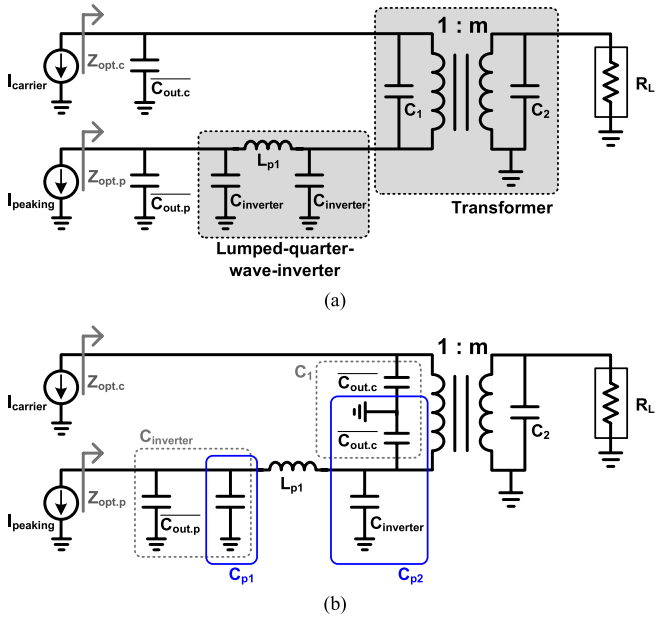

Fig. 10. (a) Practical output matching network with the transmission-line transformer, including C_1 and C_2. (b) Manipulation of the output capacitances without additional offset lines for the voltage-combined Doherty PA.

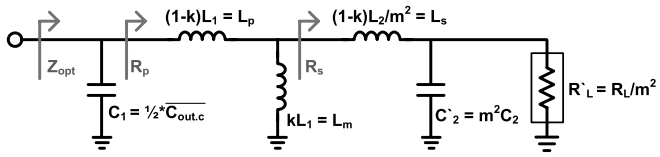

Fig. 11. Equivalent circuit model of the output transformer.

and L_m is the mutual inductance. k is the coupling coefficient determined by the spacing between the primary and secondary windings. The series loss of the transmission line is ignored to simplify the calculation. C_1 and C_2 are calculated as follows:

$$R_s = \frac{R'_L}{\left(wR'_L \cdot C'_2\right)^2 + 1} \tag{13}$$

$$C'_2 = \frac{R'_L - \sqrt{R'^2_L - 4w^2L_s^2}}{2w^2 \cdot R'_L \cdot L_s}$$

$$C_2 = \frac{C'_2}{m^2} \tag{14}$$

where the imaginary part of R_s is equal to zero because L_s is tuned out by C_2. R_p and Z_{opt} are given by

$$R_p = \frac{w^2R_s \cdot L_m^2}{R_s^2 + w^2L_m^2} + jw\frac{w^2L_p \cdot L_m^2 + R_s^2(L_p + L_m)}{R_s^2 + w^2L_m^2} \tag{15}$$

$$Z_{\text{opt}} = \frac{w^2R_s \cdot L_m^2}{R_s^2\{w^2C_1(L_p + L_m) - 1\}^2 + w^2L_m^2(w^2L_p \cdot C_1 - 1)^2} \tag{16}$$

where the imaginary part of Z_{opt} is also equal to zero by C_1 and can be expressed as

$$C_1 = \frac{\overline{C_{out.c}}}{2} = \frac{w^2L_p \cdot L_m^2 + R_s^2(L_p + L_m)}{w^4L_p^2 \cdot L_m^2 + w^2R_s^2(L_p + L_m)^2}. \tag{17}$$

As a result, C_{p2} is determined by

$$C_{p2} = C_{\text{inverter}} + \overline{C_{\text{out.c}}} = C_{\text{inverter}} + 2C_1. \tag{18}$$

Using elaborate manipulation of the output capacitances, the load modulation circuit is directly attached to the current sources of the carrier and peaking transistors without any help from the offset lines.

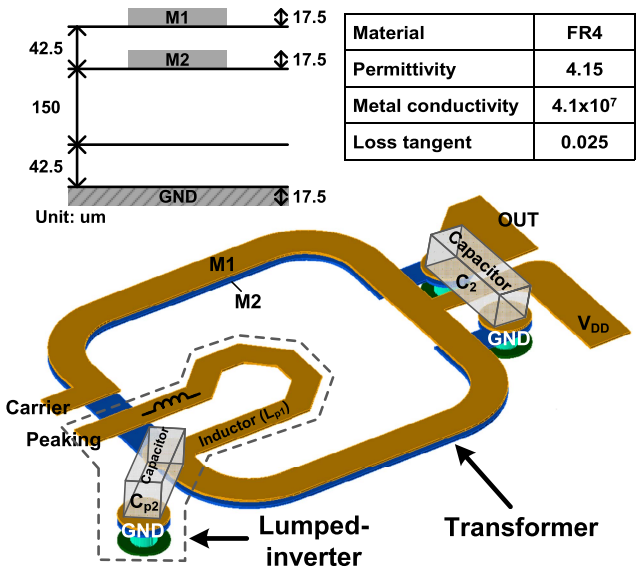

Fig. 12. Layer information of the PCB used for the PA module and 3-D view of the implemented output transformer including a partially lumped quarter-wave inverter.

B. Design of Output Transformer for Doherty PA

Fig. 12 depicts the layer information of the generic four-layer evaluation printed circuit board (PCB), and a 3-D view of the implemented output transformer, including a partial lumped quarter-wave inverter. The use of the two metal layers generates stronger coupling and has the advantage of size [23]. The L_{p1} and C_{p2}, which are parts of the lumped inverter, are also implemented on the PCB using the metal line and the external capacitor, respectively. The external capacitor C_2 is used for impedance matching with the small inductance of the secondary trace. The insertion loss of the output transformer including the C_2 is 0.32 dB at 880 MHz. In this paper, the CMOS process that has aluminum metals only without thick-copper metal is used. The on-chip output transformer using a thick-copper metal option can be used for full integration and for minimizing the size, but there is a tradeoff in the size and the insertion loss of the on- and off-chip transformers [18].

C. Simulation Results of Designed Doherty PA

Fig. 13 shows the simulation results of the designed voltage-combined Doherty PA described in Sections IV-A and IV-B. The magnitudes of the output current I_c and I_p' at the primaries are slightly different as shown in Fig. 13(a) due to the loss of transformer and asymmetry. In the practical case, the peaking cell cannot abruptly turn-ON due to the class-C bias operation different from the ideal case as shown in Fig. 2(b). Therefore, the output voltage of V_p' is increased early before the 6-dB PBO region as shown in Fig. 13(b). For a high-power region, the output voltage of the carrier amplifier at the combining node is maintained having the peak voltage level like the ideal simulation result as shown in Fig. 3(b). The class-C biased peaking amplifier generates lower fundamental output current compared with the carrier amplifier. For this reason, the output voltage of the peaking amplifier is slightly lower than that of the carrier amplifier at the peak output power region. In the low-power region, the load impedance of $Z'_{\text{opt.p}}$

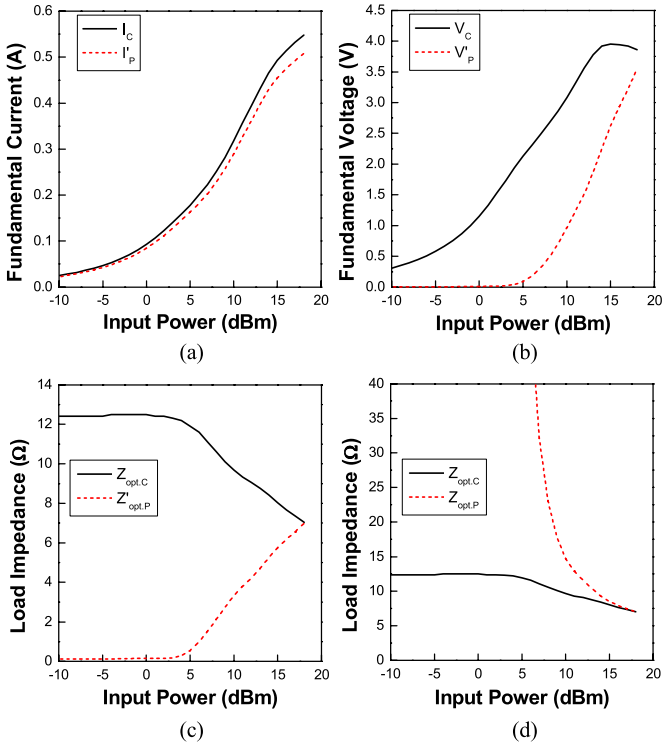

Fig. 13. Simulation results of (a) magnitudes of the fundamental output current and (b) voltage at the combining nodes of transformer versus input power. (c) Load impedances at the primary ports of the transformer. (d) Load impedances of the Doherty transistors.

at the combining node is maintained at near zero thanks to the quarter-wave inverter as shown in Fig. 13(c), and the load impedance of carrier amplifier is maintained with 2Ropt delivering a high efficiency at 6-dB PBO under the single-ended operation. In the high-power region, the transformer with the quarter-wave inverter properly modulates the load impedance seen by each carrier and peaking amplifier as shown in Fig. 13(d). These simulation results are well matched with the ideal concept described in Section II.

D. Linear Doherty Operation

Under ideal conditions, the output voltage swing of an ideal class-B PA with an output load of $2R_{\text{opt}}$ is two times larger than that of a comparable PA with R_{opt}. When the output voltage swings are identical, the input voltage of the former is halved. Therefore, the class-B PA under the load condition of $2R_{\text{opt}}$ achieves 3-dB higher power gain compared to the amplifier with the R_{opt} case. In a Doherty PA design, a class-AB or deep class-AB type is preferred for the carrier amplifier, and in the carrier amplifier, there is a power gain difference of about 3 dB between the $2R_{\text{opt}}$ and R_{opt} load conditions [3].

However, in the practical design of a Doherty PA, the gain modulation is affected by nonlinear capacitors with the C_{dg} feedback effect. Moreover, the gains of the carrier amplifier with the R_{opt} and $2R_{\text{opt}}$ loads are almost the same [7], [8]. Therefore, the carrier amplifier is saturated in Doherty operation with about 3-dB gain compression at the maximum output power because the input power to the carrier amplifier

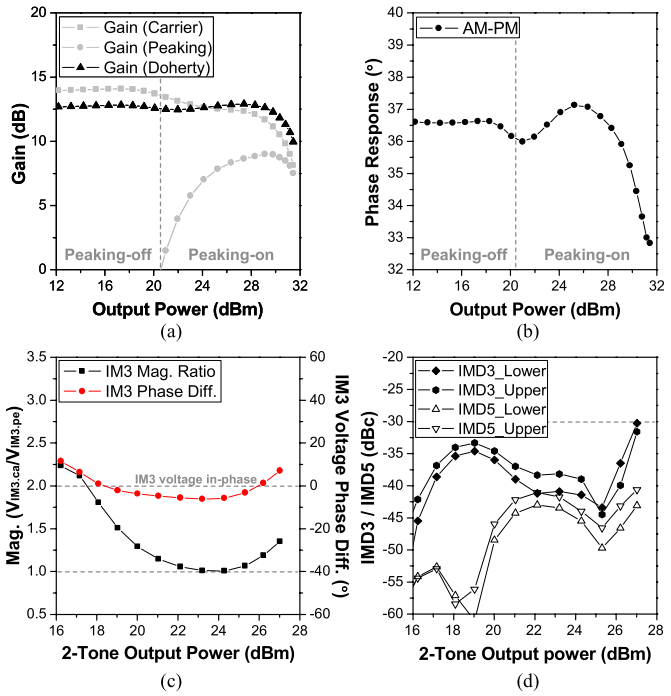

Fig. 14. CW simulation results of (a) gain and (b) AM–PM curves of the Doherty PA. (c) Two-tone simulation results for the magnitude and phase differences in the IM3 voltages between the carrier (V_{ca}) and peaking (V_{pe}) amplifiers versus the power sweep. (d) IMD curves versus the power sweep.

is too high for a linear operation. The lower gain of the carrier amplifier compensates for the low gain of the peaking amplifier and aids the Doherty operation with a constant gain as shown in Fig. 14(a) [8]. In the high-power region, not only the AM–AM response but also the AM–PM response of the carrier amplifier is compensated for by the peaking amplifier resulting in a flat AM–PM curve as shown in Fig. 14(b). For the linear operation, the third-order intermodulation distortion (IMD3) from the carrier and peaking amplifiers should cancel each other with lower fifth-order IMD (IMD5). The canceling can be achieved by adjusting the large-signal third-order transconductance coefficient (gm3), which is achieved by the proper gate biases of the two amplifiers [4] and by an additional phase delay line to compensate for the phase delay mismatch caused by the memory effects [7].

The efficiency and linearity at the 6-dB PBO region are closely related to the turn-ON timing of the peaking amplifier. Since the peaking amplifier cannot abruptly turn ON, it should be turned ON early to compensate for the AM–AM, AM–PM, and IMD3 distortions of the carrier amplifier for achieving high linearity at the 6-dB PBO, but the early turn-ON means that the load modulation starts early, which decreases the peak efficiency at the 6-dB PBO. Fig. 14(c) shows the magnitude and phase differences of the third-order intermodulation (IM3) voltages between the carrier (V_{ca}) and peaking (V_{pe}) amplifiers, and Fig. 14(d) shows the IMD curves of the proposed linear Doherty PA.

V. Measurement Results

To validate the proposed CMOS Doherty PA, the PA was fabricated using a 0.18-μm CMOS process, and the total chip area including pads is 1.2×1.1 mm^2 as shown in Fig. 15.

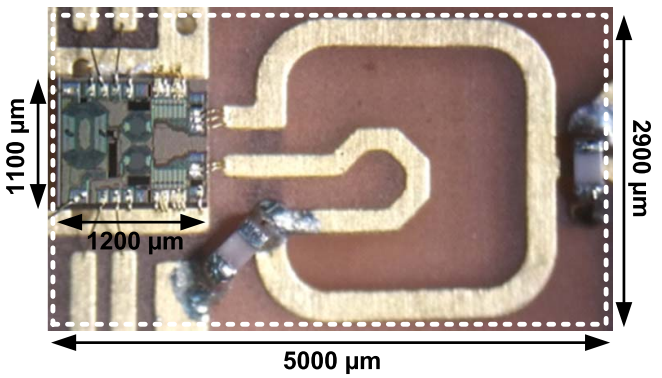

Fig. 15. Photograph of the voltage-combined CMOS Doherty PA module that includes the PA chip in a 0.18-μm CMOS process.

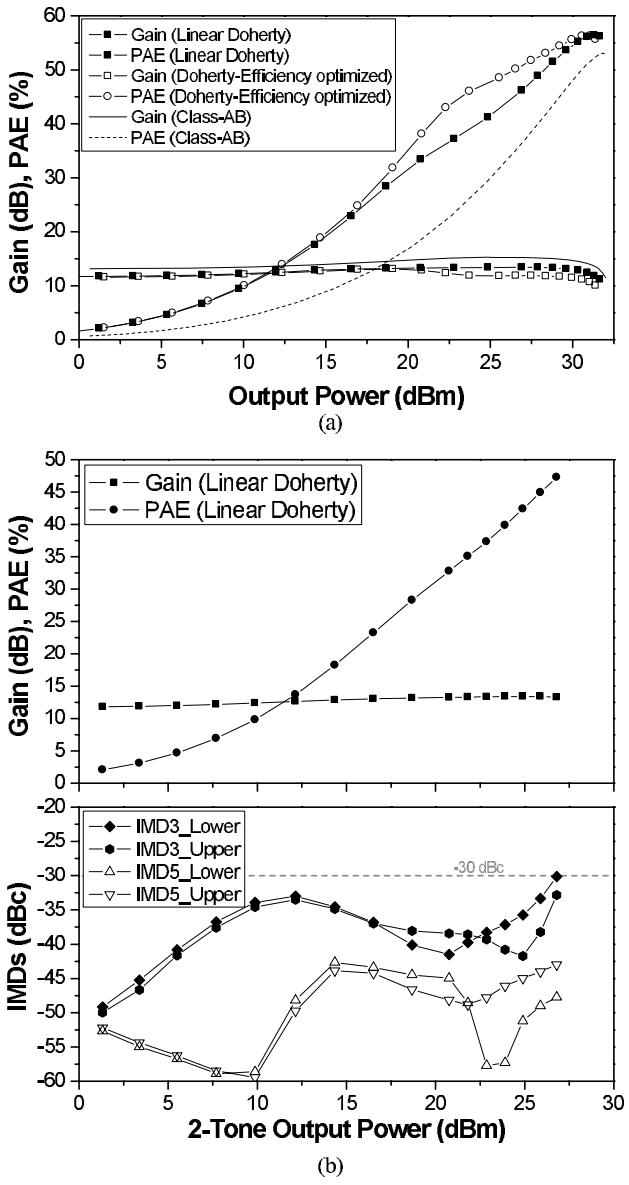

Fig. 16. Measured performance of the proposed Doherty PA with 4.0 V V_{DD}. The gain, PAE, and IMD performances versus the power sweep for (a) CW signal and (b) two-tone signal.

The output combining transformer including the partially lumped inverter is implemented on an FR4 PCB board, and the total PA module is 5.0×2.9 mm^2. Fig. 16 shows the measured

TABLE I
PERFORMANCE COMPARISON OF RECENTLY REPORTED MOBILE LTE PAs

Ref.	Freq. (MHz)	Signal/BW/PAPR (–/MHz/dB)	Technology	Characteristic	P_{out} (dBm)	Gain (dB)	PAE (%)	ACLR* (dBc)	V_{DD} (V)	Output matching
MWCL 2014 [24]	900	LTE/10/7.5	0.32-μm SOI CMOS	Phase Linearized PA	26.3	28.3 2-stage	36.5	-35.5	4	off-chip
JSSC 2013 [25]	700	LTE/10/7.5	0.35-μm SiGe BiCMOS	ET PA	27.6	17.0 1-stage	36.4	N/A	5	off-chip
MWCL 2015 [26]	1850	LTE/10/7.5	0.18-μm CMOS	Adaptive Biased ET PA (2 chips)	27.5	14.2 1-stage	44.5	-33.6	4	off-chip
TMTT 2014 [27]	837	LTE/10/6.7	0.32-μm SOI CMOS	Dynamic Stack ET PA (2 chips)	25.7	26.6 2-stage	47.5	-35†	3.4	off-chip
MWCL 2014 [28]	847	LTE/10/7.6	0.18-μm CMOS	Current Combined Doherty PA (2 chips)	25.2	27.2 2-stage	43.6	-34.1	N/A	off-chip
This Work	880	LTE/10/7.5	0.18-μm CMOS	Voltage Combined Doherty PA	25.5 26	12.7 1-stage	45.5 46.7	-34.2 -33	3.5	off-chip
					26.5 27	13.3 1-stage	46.1 47.4	-34.2 -33	4	

*LTE specifications: $E-UTRA_{ACLR} <$ -30 dBc.
†With DPD but the power consumed by DPD is not included.

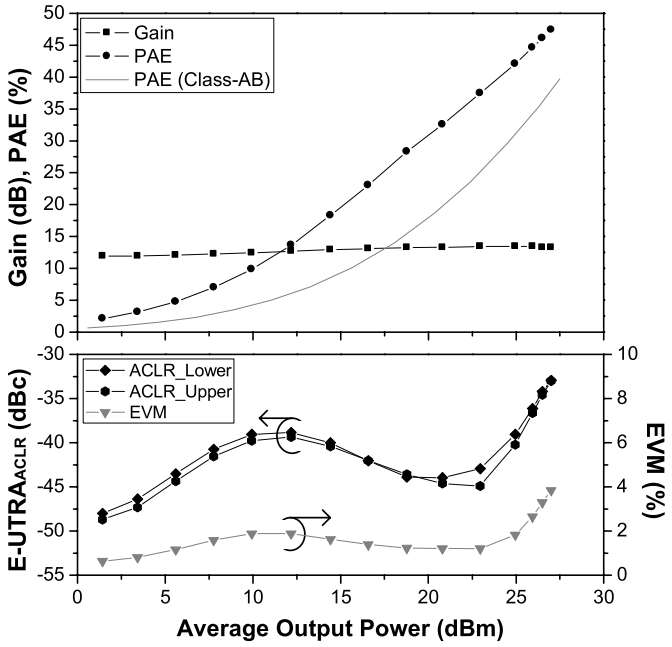

Fig. 17. Measured performance of the proposed PA with the 16-QAM 7.5-dB PAPR LTE signal. The gain, PAE, EVM, and $E-UTRA_{ACLR}$ performances versus the power sweep.

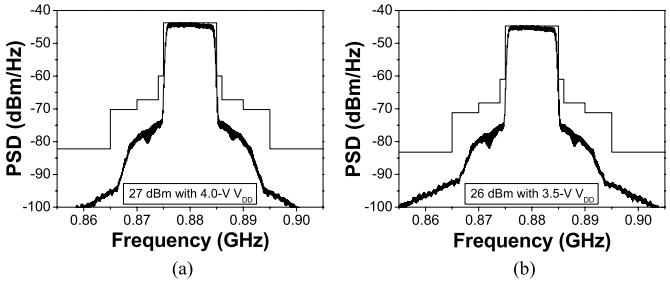

Fig. 18. Measured LTE spectra of the PA at (a) average output power of 27 dBm with 4.0-V V_{DD} and (b) average output power of 26 dBm with 3.5-V V_{DD}.

performance of the PA with a supply voltage of 4.0 V at the 880-MHz frequency band. The first peak efficiency at the 6-dB PBO can be optimized by adjusting the CS gate bias of the peaking amplifier as described in Section IV-C. However, the gate bias with optimized efficiency leads to gain distortion that deteriorates the linearity as shown in Fig. 16(a). For the linear Doherty PA, the CS gate bias of the peaking amplifier is chosen to make the flat AM–AM and AM–PM. With the proper CS gate biases and the additional phase delay line merged into the input phase compensation network, the Doherty PA achieves good IMDs as shown in Fig. 16(b).

The proposed linear PA is tested at 880 MHz using a 10-MHz BW, 16-quadrature amplitude modulation (QAM), and 7.5-dB PAPR long-term evolution (LTE) signal as shown in Fig. 17. The PA delivers a gain of 13.3 dB, a power-added efficiency (PAE) of 47.4%, an error vector magnitude (EVM) of 3.85%, and an access adjacent channel leakage ratio ($E-UTRA_{ACLR}$) of -33 dBc at an average output power of 27 dBm. For a high PAPR signal, such as LTE, these results demonstrate convincingly that Doherty operation is effective in achieving high efficiency with good linearity at the peak output power as well as at the PBO regions. Fig. 18 shows the measured spectra, satisfying the standard spectrum mask at an average output power of 27 dBm with a supply voltage of 4.0 V and 26 dBm with a supply voltage of 3.5 V. Fig. 19 depicts the measured dynamic AM–AM and AM–PM responses for the LTE signal.

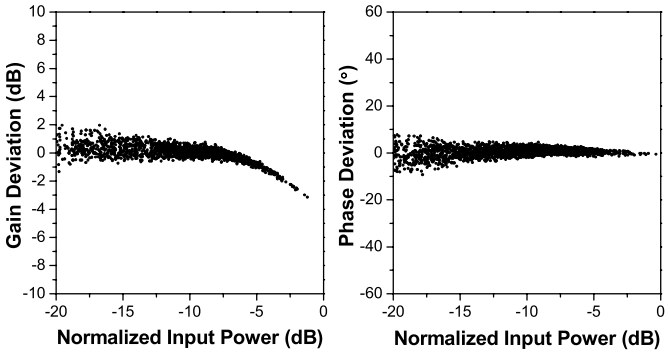

Fig. 19. Measured dynamic (a) gain deviation and (b) phase deviation at an average output power of 27 dBm with a supply voltage of 4.0 V for the LTE signal.

Table I summarizes the comparison of the measured results with state-of-the-art handset PAs for LTE terminals. Without any complex circuitry, our work shows, using the envelope tracking (ET) technique with additional chip [25]–[27], and digital predistortion [27], that the efficiency of the Doherty PA based on a voltage-combining method is comparable to that of the state-of-the-art LTE PAs. In particular, the efficiency demonstrated in the proposed Doherty PA based on a voltage-combining method is higher than that of the Doherty PA based on a current-combining method using an additional chip for the auxiliary bias control circuit [28].

VI. Conclusion

A voltage-combined linear CMOS Doherty PA based on a two-way transformer has been developed. Based on the transformer theory, the load modulation characteristics of the transformer were investigated. Furthermore, a detailed analysis of the dynamic load modulation using the two-way transformer with a quarter-wave inverter was investigated to realize the Doherty PA based on a voltage-combining method. The comparison between the current- and voltage-combined Doherty PAs shows that the voltage-combined Doherty PA has a larger load tolerance and a larger BW compared with the Doherty PA based on a current-combining method. The proposed Doherty PA achieved close to the ideal load modulation without an additional offset line by de-embedding of the output capacitances to the Doherty network.

A voltage-combined linear CMOS Doherty PA was designed and fabricated using a CMOS process for operation at 880 MHz. The combining transformer was implemented on the PCB module. Full LTE characterization was performed using a fully loaded LTE signal with a 16-QAM, a 7.5-dB PAPR, and a 10-MHz BW. The PA provided a gain of 13.3 dB, a PAE of 47.4%, an EVM of 3.85%, and E − UTRA$_{\mathrm{ACLR}}$ of −33 dBc at an average output power of 27 dBm. This simple voltage-combined Doherty PA without additional circuitry delivers a comparable performance among the state-of-the-art ET PAs reported.

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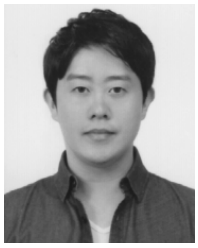

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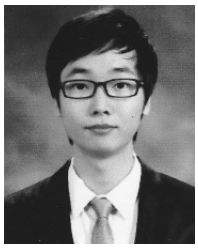

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