Design of a K-Band Power Amplifier for High Gain, Output Power and Efficiency on 0.18-µm SiGe BiCMOS Process

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***Abstract* — The design of a K-band power amplifier (PA) on a 0.18 µm SiGe BiCMOS process for high gain, output power and power-aided efficiency (PAE) is presented. The designed PA is composed of a drive amplifier, two identical main amplifiers, and lumped-element Wilkinson power divider and combiner. The PA achieves 37.5-39.5 dB of small-signal gain, 18.6-20.6 dBm of saturated output power, and 18-29% of PAE over the entire K-band (18-26.5 GHz). Specifically at 24 GHz, it achieves 19.4 dBm output power, 22.3% PAE, and 37.6-dB gain.**

Index Terms — CMOS/BiCMOS power amplifier, lumped Wilkinson power divider/combiner, power amplifier, RFIC.

I. Introduction

The K-band (18-26.5 GHz) is a viable spectrum for radar and satellite communications. Especially, its 24 GHz has been adapted for ISM applications and vehicle radar. A power amplifier (PA) is a crucial component in transmitters. It is challenging to achieve high gain and output power with decent PAE simultaneously across wide frequency ranges for silicon-based PAs. This is due to the fact that silicon devices have low breakdown voltage, causing low power gain, and silicon substrates are highly conductive and hence very lossy at high frequencies, leading to reduced gain and output power. Many works on silicon-based PAs operating in K-band have been reported [1]-[5].

In this paper, the design of a broadband PA over the whole K-band for high gain, high output power, and high PAE on a 0.18-µm SiGe BiCMOS process is presented. The PA consists of a drive amplifier and two identical amplifiers in parallel integrated with lumped-element Wilkinson power divider and combiner. It achieves good performance with output power of 18.6-20.6 dBm, gain of 37.5-39.5 dB, and PAE of 18-29% across the entire K-band. Specifically, at the widely used frequency of 24 GHz, the PA achieves 19.4-dBm output power, 22.3% PAE, and 37.6-dB gain. The employed power combiner/divider possesses low-pass filtering characteristic, enabling harmonic suppression and improving bandwidth that help achieve good performance over the whole K-band frequency range.

II. Power Amplifier Design

Fig. 1 shows the schematic of the developed PA, which includes a drive amplifier, two identical main amplifiers, and Wilkinson power divider and combiner. The cascode structure is utilized to obtain high gain and reverse isolation. This enables large device size ratio between the transistors of the main and drive amplifiers, resulting in less burden for the drive amplifier. Coplanar waveguide (CPW) on the topmost metal layer is employed for the spiral inductors, input and output transmission lines, and interconnections for low conductor loss. The common ground plane for the CPW is extended over the whole PA chip to provide continuous ground plane as well as to isolate the inductors from nearby elements, which helps reduce the coupling effects. These components were designed and simulated using the EM simulator IE3D [6].

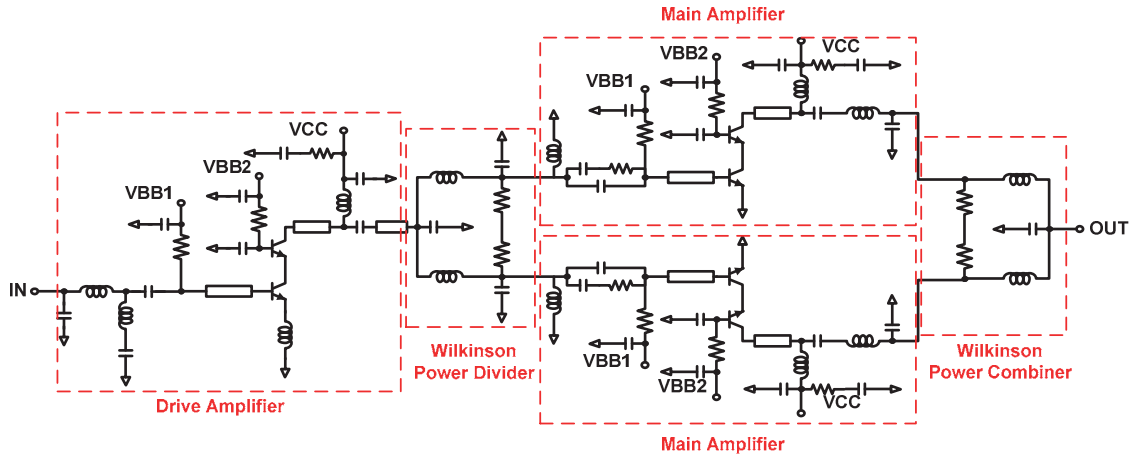


Fig. 1. Schematic of the proposed PA.

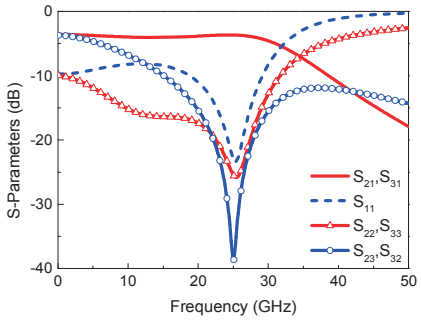


Fig. 2. Simulated S-parameters of lumped-element Wilkinson power divider/combiner.

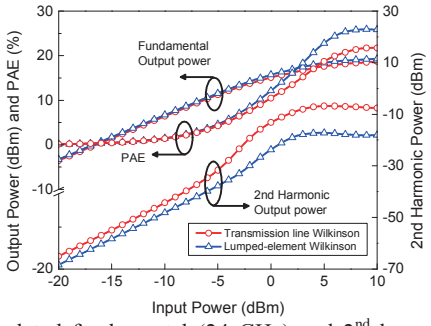


Fig. 3. Simulated fundamental (24 GHz) and 2nd harmonic output power and PAE of PAs with lumped-element and transmission line Wilkinson power divider/combiner.

A. Main Amplifier Design

Each transistor employed in the main amplifier is determined based on load-pull simulations for high output power under class AB bias point and consists of four transistors, each having 0.15µm emitter width and 10.16µm emitter length. The large transistors in PAs make them more vulnerable to instability. To improve the PA stability and achieve unconditional stability at lower frequencies, series RC circuit with shunt capacitor [1] is connected to the input of the main amplifier as shown in Fig. 1. This RC network produces resistive loss at low frequencies to reduce excessive gain of the devices at lower frequencies, thereby resulting in improved stability. A 4.2pF bypass capacitor connected in parallel with a small 5Ω resistor in series with a larger 13.2 pF bypass capacitor are used at the collector's DC supply node (VCC) to enhance the low-frequency stability further. The simulated stability factor (K) of the amplifier is greater than 30 from DC to 60 GHz.

B. Lumped-Element Wilkinson Power Divider/Combiner

The traditional Wilkinson power divider/combiner occupies a large chip area since two quarter-wavelength transmission lines are used, making it not desirable for silicon RFICs operating in the K-band region. To minimize the chip size, lumped-element based Wilkinson power divider/combiner [7], [8] is implemented. The conventional quarter-wavelength transmission line is replaced with a pi-network as shown in Fig. 1. The inductance and capacitance of the pi-network can be derived as $L=Z_0/2\pi f_0$ and $C=1/2\pi f_0 Z_0$, respectively, where Z_0 is the transmission line's characteristic impedance and f_0 is the design frequency. The simulated S-parameters of the designed lumped-element Wilkinson power divider/combiner are shown in Fig. 2. At 24 GHz, the insertion loss is 0.66 dB and its second harmonic is rejected by more than 16 dB. As can be seen, the simulation results demonstrate that the designed power divider/combiner exhibits low-pass filtering response over a wide bandwidth. This is due to the fact that each of its two pi-networks functions like an artificial transmission line, which works as a wideband low-pass filter up to a cut-off frequency. This wideband low-pass filtering behavior helps suppress undesired harmonics, which cannot be suppressed with transmission-line based Wilkinson power dividers/combiners. Two PAs designed with lumped-element and transmission-line Wilkinson power dividers/combiners are simulated to demonstrate the differences in harmonic suppression and PAE. Fig. 3 shows the simulated output powers of the 24-GHz fundamental and 48-GHz second-harmonic signals and the PAE. As can be seen, more suppression of the second harmonic with slightly higher fundamental output power and higher PAE are provided by the PA with the lumped-element Wilkinson power divider/combiner.

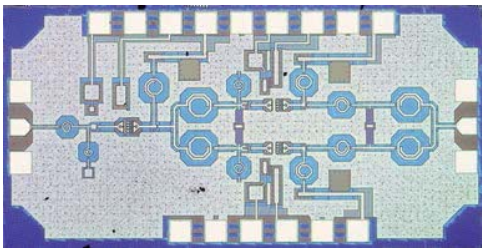


Fig. 4. Photograph of the fabricated PA.

C. Driver Amplifier Design

The driver amplifier is designed to produce the necessary input power for the main amplifiers. Each device of the driver amplifier combines four transistors each having 0.15µm emitter width and 4.52µm emitter length. The device size ratio of the driver amplifier and the combined two main amplifiers is larger than 4:1. Inductive degeneration, simulated with a short transmission line, is used at the emitter of the common-emitter part of the cascode structure to introduce negative series feedback and enable broadband input matching.

III. Simulation and Measurement

Fig. 4 shows a photograph of the designed PA fabricated using Jazz 0.18-µm SiGe BiCMOS process [9]. The chip area is 2×1 mm^2 with the RF and DC pads. The PA was measured on-wafer and the DC current of the driver and main amplifiers were 30 mA and 65 mA with 2 V of VCC respectively. Fig. 5 shows the measured and simulated S-parameters of the designed PA, showing good agreement. The measured gain is 37.5-39.5 dB between 18 and 26.5 GHz and the 3-dB gain bandwidth is from 16.5 to 28 GHz, which is larger than the

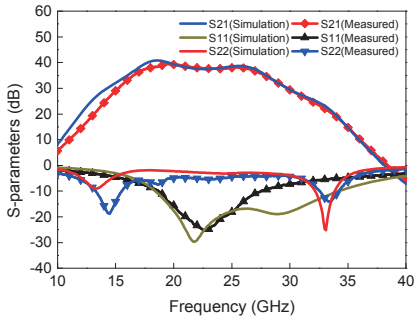
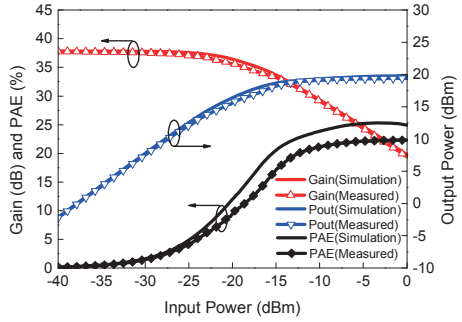
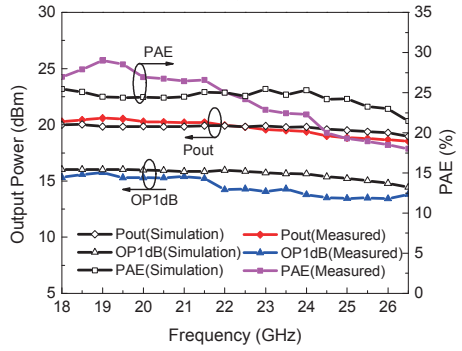


Fig. 5. Measured and simulated S-parameter of the designed PA.



(a)



(b)

Fig. 6. Measured and simulated (a) power gain, output power, and PAE at 24 GHz, and (b) saturated output power, OP1dB, and PAE.

whole K-band. At 24 GHz, the measured gain is 37.6 dB. The measured input return loss is greater than 10 dB over the K-band. Fig. 6(a) shows the results of power gain, output power, and PAE with respect to input power at 24 GHz. The saturated output power is 19.4 dBm with peak PAE of 22.3%, and the output power at 1-dB compression point (OP1dB) is 13.8 dBm. Fig. 6(b) shows the saturated output power, OP1dB, and PAE from 18 to 26.5 GHz. As can be seen, the measured saturated output power is highest at 20.6 dBm at 19 GHz and 18.6-20.6 dBm between 18 and 26.5 GHz. Furthermore, the measured PAE is 18-29% within this band. To the best of our knowledge, the designed PA's performance is among the best reported silicon PA's in K-band, and its 3-dB operating bandwidth of 16.5-28 GHz is the largest.

IV. Conclusion

A power amplifier with high gain, high output power and good PAE working across the entire K-band was designed using a 0.18-µm SiGe BiCMOS process. The PA achieves 37.5-39.5 dB of small-signal gain and output power of 18.6-20.6 dBm with 18-29 % of PAE from 18 to 26.5 GHz. At 24 GHz, the measured output power is 19.4 dBm with peak PAE of 22.3%. By incorporating a lumped-element Wilkinson power divider/combiner having low-pass filtering response, high-performance wide-band PAs can be designed for silicon RFICs. Moreover, it also demonstrates that it is possible to incorporate a filtering function in RFIC's constituent elements to enhance the performance. .

Acknowledgement

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