A Monolithic 24 GHz, 20 dBm, 14% PAE SiGe HBT Power Amplifier

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Abstract— **A monolithic 24 GHz SiGe HBT power amplifier (PA), with an output 1 dB compression point of 20 dBm, is presented. The circuit is biased from a 5.1 V supply in a class AB mode of operation, resulting in a power added efficiency (PAE) of 14 % at the 1 dB compression point. The SiGe PA has a small-signal gain of 12 dB at 24 GHz, and a return loss of 9.6 dB and 16 dB at the input and output ports, respectively. This SiGe PA leverages the increased voltage swing capabilities associated with the common-emitter / common-base configuration for SiGe HBTs incorporated in a cascode architecture.**

Index Terms- Power Amplifier, PA, Silicon-Germanium, SiGe HBT.

I. Introduction

Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT) technology is becoming increasingly prevalent in commercial RF and microwave applications due to its attractive combination of high speed, low noise, low power, high integration level, and low cost. There has been significant recent research on SiGe HBT transceiver building blocks, and the benefits of SiGe technology for general wireless applications [1], [2], [3].

Recently there have been several studies investigating SiGe circuits operating in the 22-29 GHz band for local multi-point distribution (LMDS) systems [4], wireless communication transceivers [5], and automotive radar applications [6]. However, there has been very limited work examining the capabilities of SiGe power amplifiers at these frequencies. The work presented in [7] investigated device level optimization of single HBT power cells, while [8] and [9] have reported SiGe BiCMOS or CMOS microwave power amplifiers (PA), but with modest output powers (< 15 dBm), and limited efficiency.

The present work investigates the efficacy of SiGe HBT power amplifiers targeting higher power and moderate efficiencies at 24 GHz. This SiGe HBT PA is based on a cascode architecture, and exploits the bias dependence of breakdown voltage in SiGe HBTs. This configuration enables the circuit to operate with a significantly larger output voltage swing, resulting in an output 1-dB compression point (OP_{1dB}) of 20dBm and a power added efficiency (PAE) of 14% at 24 GHz. The input and output ports of the amplifier are matched on-chip to 50 Ω, with a corresponding small-signal gain of 12 dB.

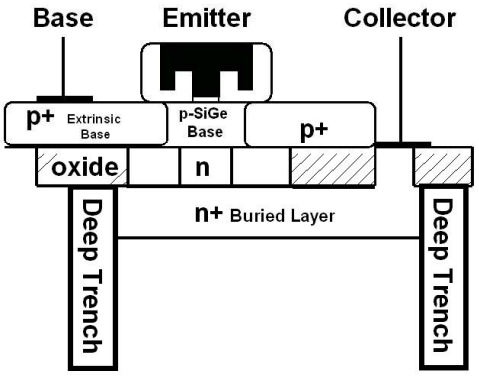

Fig. 1. Schematic cross-section of the SiGe HBT.

TABLE I
Characteristics of Jazz SiGe-120 HBT BiCMOS technology.

	f_T	f_{max}	BV_{CEO}
Device Type	GHz	GHz	V
High Speed	150	170	2.2
Medium Speed	75	130	3.5
Low Speed	34	60	6.0

II. SiGe HBT BiCMOS Technology

The SiGe BiCMOS technology used in this study is the commercially-available Jazz SiGe-120 process, which offers a maximum unity-gain cut-off frequency (f_T) of 150 GHz[10]. This SiGe technology also features 6 layers of metalization, 180 nm CMOS devices, high-Q spiral inductors, and high-Q MIM capacitors [10]. The process utilizes shallow- and deep-trench isolation and a self-aligned emitter-base structure for the SiGe HBT (Fig. 1), resulting in both low base resistance and reduced capacitive parasitics [10].

In addition to high-speed SiGe HBTs, the technology also offers devices targeting higher breakdown voltages (BV_{CEO})[11], as shown in Table I. As expected, this increase in breakdown voltage comes at the expense of frequency response, as well as collector current density (J_C) at which peak f_T occurs. These multiple device options, however, allow designers to selectively incorporate both high-speed and high-breakdown transistors in critical circuit applications to leverage all of the performance capabilities of the technology, greatly enhancing design flexibility.

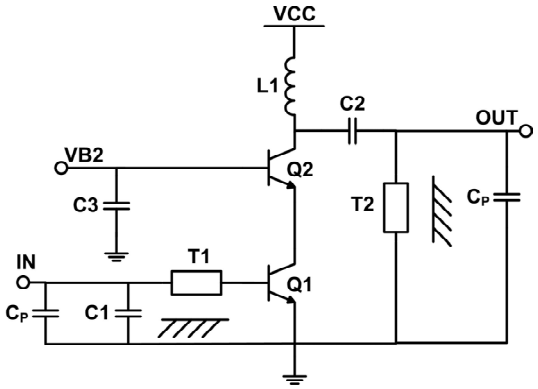

Fig. 2. Schematic of the 24 GHz SiGe power amplifier.

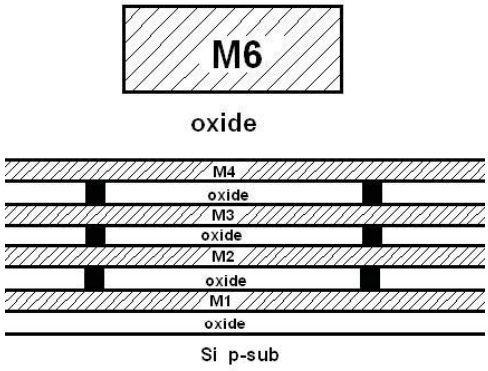

Fig. 3. Schematic cross-section of the thin-film microstrip transmission line.

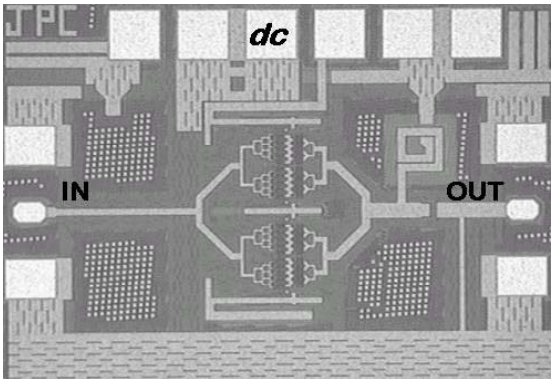

Fig. 4. Die photo of the 24 GHz SiGe power amplifier (0.85 x 1.2 mm^2).

III. Power Amplifier Design

A cascode architecture was used for the power amplifier topology, as shown in Fig. 2. The cascode topology provides high isolation between the output and the input ports, and allows for an increase in the available operating voltage for the circuit. This topology also allows the designer to utilize higher breakdown transistors for Q2, increasing the available voltage swing at the output. Higher speed (and therefore higher gain) transistors can still be utilized for the driving transistor (Q1) to simultaneously achieve both high gain and high output power for the power amplifier.

The available voltage swing at the output of Q2 is also significantly increased due to the *dc* biasing associated with the cascode architecture [12]. That is, the practical breakdown voltage for the SiGe HBT is dependent on the type of *dc* source used to bias the circuit. For instance, when the HBT is biased in a common-emitter topology with high input impedance, BV_{CEO} represents the usable (worst case) breakdown voltage. However, when the emitter is driven with a current source and the base is biased with a voltage source, the breakdown voltage is actually closer to BV_{CBO} (which is approximately twice as large as BV_{CEO}). This increase in voltage swing correlates to larger output power for a given bias current, thus improving the PA's efficiency.

The driving transistor (Q1) consists of 20 single-stripe high-speed (150 GHz f_T) 0.20x10.16 μm^2 HBTs, resulting in a total emitter area (A_E) of 40.64 μm^2. The top transistor (Q2) consists of 16 multi-stripe medium-breakdown (75 GHz f_T and 3.5 V BV_{CEO}) HBTs with a total emitter area of 113.8 μm^2. The significant increase in A_E for Q2 results from the decrease in current density for the medium-breakdown transistor (as compared to the high-speed transistor).

The matching for the amplifier is accomplished with on-chip passives consisting of MIM capacitors, spiral inductors, and thin-film microstrip transmission lines. The microstrip transmission lines utilize the top-metal (M6) for the signal path, with the lower metals (M4-M1) shorted with vias, creating a low resistance return path (Fig. 3). These transmission lines were designed and modeled using ADS and Momentum simulators, in conjunction with the SiGe-120 design kit. Different types (i.e., high-pass and low-pass) of matching networks are used for the input and output of the amplifier to improve the broadband stability. Additional de-coupling capacitors were also placed on chip at the base of Q2 and at V_{CC} to achieve a good on-chip RF short at high frequencies.

The simulated circuit was biased at 5.1 V, and dissipated 56 mA for nominal *dc* operation. The simulated gain of the amplifier was 12.2 dB, with an OP_{1dB} of 22 dBm, and a peak PAE of 14 %. The simulated circuit also demonstrated a return loss greater than 10 dB for both the input and output ports at 24 GHz.

A. Measured Results

The 24 GHz SiGe power amplifier (Fig. 4) was fabricated and measured at the die level with an Agilent 8510C VNA, a 8565E spectrum analyzer, a 4419B power meter, a 8485A power sensor, and two frequency sweepers. The circuit was biased from a 5.1 V *dc* power supply, with 1.9 V applied to the base of Q2, and 0.88 V applied to the base of Q1, resulting in a nominal I_{CC} of 38mA.

The amplifier was biased in a class-AB mode of operation, allowing the I_{CC} *dc* current to increase with the

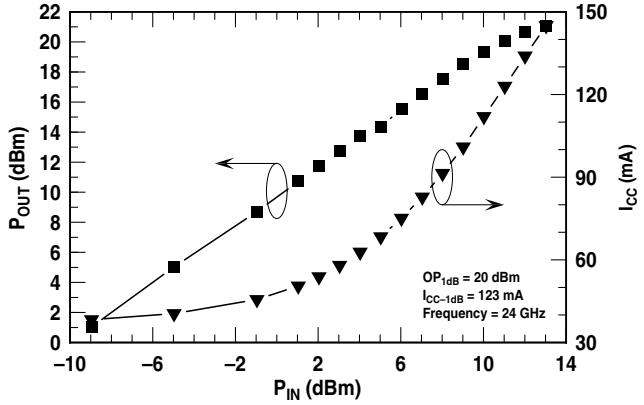

Fig. 5. Output power and I_{CC} versus input power for the 24 GHz power amplifier.

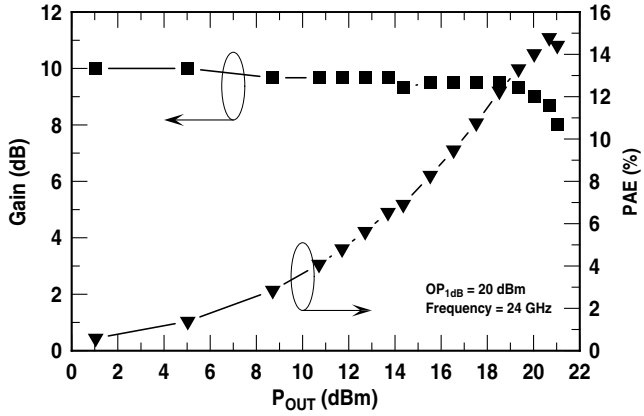

Fig. 6. Gain and power added efficiency versus output power for the 24 GHz power amplifier.

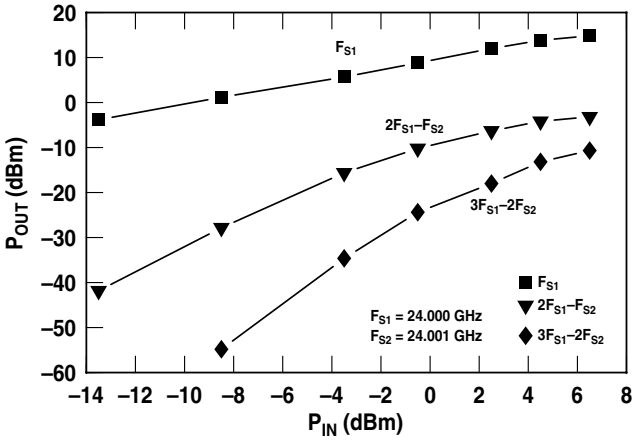

Fig. 7. Output power and intermodulation products versus input power for the 24 GHz power amplifier.

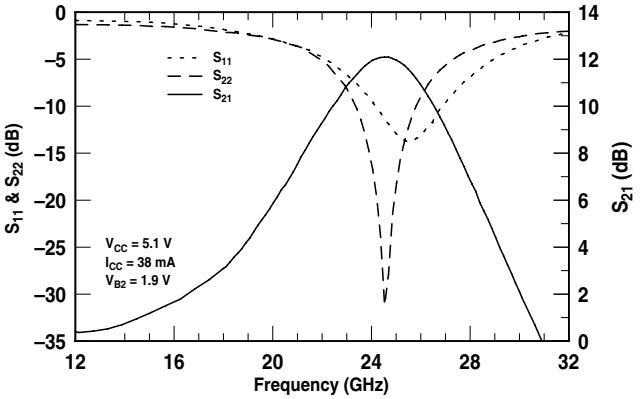

Fig. 8. S_{11}, S_{22}, and S_{21} versus frequency for the 24 GHz power amplifier.

input power, as seen in Fig. 5. The circuit achieved an OP_{1dB} of 20 dBm, with a gain of 10 dB, and a PAE of 14% (Fig. 6). It should be noted that the cable losses of the test setup were accounted for in the power and efficiency measurements, but the probe losses (estimated to be approximately 0.85 dB per probe at 24 GHz) were not, and thus our reported numbers are conservative.

The intermodulation distortion of the amplifier was also quantified, as seen in Fig. 7. The circuit demonstrated 18 dBc of rejection for the third-order intermodulation product for output powers as high as 13 dBm. The small-signal output third order intercept point (OIP_3) was calculated to be 15 dBm from the two-tone measurements. Higher-order intermodulation products were also observed, as shown in Fig. 7, but remained lower in power than the third-order product.

The S-parameters of the circuit were measured at die level from 1 GHz to 40 GHz for accurate gain, return loss, and stability characterization. Both the input and output of the power amplifier were matched to 50 Ω at 24 GHz, as seen in Figure 8, achieving a return loss better than 9 dB for both ports from 23 GHz to 26 GHz. The circuit also achieved a gain of 12 dB (Fig. 8) for the nominal *dc* bias point, with a 3-dB bandwidth from 23.3 GHz to 25.8 GHz. The discrepancy between the measured gain from S-parameters and the measured gain originating from the power measurements, is attributed to probe loss, which was not accounted for during the power measurements. The amplifier's stability factor (K) was also measured for several bias points (I_{CC} = 38, 101, 151 mA), and observed to remain greater than unity for all measured frequencies (1 GHz - 40 GHz).

The breakdown voltage of the amplifier was also characterized for different biasing conditions. As shown in Fig. 9, the circuit can operate with a V_{CC} up to 8V when biased with a *dc* voltage source at the base of Q2. However, when a higher impedance source is incorporated at the base of Q2 (i.e., a voltage source with 300 Ω of series resistance), the circuit can only withstand voltages of 6V before breakdown occurs. These results highlight the voltage swing benefits that the cascode topology allows for SiGe HBT power amplifiers.

IV. Performance Comparison

The performance of this 24 GHz SiGe HBT power amplifier has been compared to other silicon-based power amplifiers (Table II) and is competitive with previously published SiGe power amplifiers in terms

TABLE II

Performance comparison of silicon-based microwave power amplifiers.

Ref.	Freq.	P_{OUT}	Gain	PAE	Size	Technology
	GHz	dBm	dB	%	mm^2	
This work	24	20	12	14	1.02	150 GHz SiGe
[8]	24	14.5*	7	4.5*	1.26	0.18 μm CMOS
[9]	24	12*	18	3*	NR	80 GHz SiGe
[13]	24	12	17.7	2.6	0.25	80 GHz SiGe
[14]	24	21*	19	13*	6.00	120 GHz SiGe

* Correlates to saturated output power.

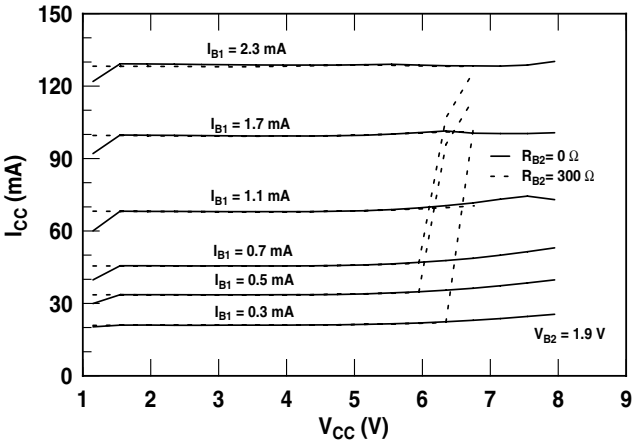

Fig. 9. Output characteristics for various biasing configurations for the 24 GHz power amplifier.

of P_{OUT}, PAE, and total die size. As expected, the present SiGe PA does not out-perform PA's based on GaAs pHEMT technology [15] or InP DHBT [16] technology, but the present solution is 100% Si foundry compatible, and thus should offer a path to low-cost, highly integrated solutions. In addition, we believe the performance of microwave SiGe HBT PAs can be further enhanced, using more advanced layout techniques for power combining and overall performance of passives ([14]), as well as targeting more aggressive PA topologies (such as class E or F designs), ultimately closing the gap between SiGe and III-V power amplifiers for emerging microwave applications.

V. Summary

A 20 dBm, 24 GHz SiGe HBT power amplifier with a PAE of 14% has been presented. The circuit is based on a commercially-available 150 GHz SiGe HBT technology, and incorporates on-chip matching for both the input and output. The amplifier exploits the bias dependence associated with the SiGe HBT's breakdown voltage, as well as the ability to selectively incorporate high-speed and high-breakdown devices in critical circuit locations. This work demonstrates the potential for efficient SiGe HBT microwave power amplifiers, and highlights the versatility of the technology.

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