A Fully Integrated 2 × 2 Power Amplifier for Dual Band MIMO 802.11n WLAN Application Using SiGe HBT Technology

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***Abstract*—A fully monolithic 2 × 2(2 × 5 GHz-band, 2 × 2.4 GHz-band) power amplifier (PA) implemented in a 0.18 μm Silicon Germanium (SiGe) HBT process has been developed for a dual band MIMO 802.11n WLAN system. In order to achieve the required performance for the 5 GHz band while maintaining a high level of integration, different approaches have been investigated. A special Through-Wafer-Via (TWV) process on Si wafer was developed and utilized for this 2 × 2 PA. From fabricated 2 × 2 chip measurement results, both 5 GHz-band and 2.4 GHz-band PAs show above 17 dBm linear power output for −28 dB EVM and more than 18 dBm with >14% efficiency for 5 GHz-band and 19% efficiency for 2.4 GHz-band at −25 dB EVM linear output.**

This fully integrated PA has a total die area of 1.36 mm × 3.68 mm and is packaged in a custom designed QFN4 × 6 32 pin package.

***Index Terms*—Power amplifiers, SiGe, MIMO, 802.11n, WLAN, OFDM.**

I. Introduction

THE original 802.11b standard utilizes complementary code keying (CCK) modulation techniques for communications at rates up to 11 MBps in the 2.4 GHz ISM band. On the other hand, the newer 802.11a and g WLAN protocols utilize a 20 MHz channel bandwidth and carrier frequencies in the 2.4 or 5 GHz bands along with OFDM coding techniques to allow for communications at speeds up to 54 Mbps. Various 801.11a/b/g CMOS transceivers have been reported in the recent years [1]–[3], in which most of the radio subsystems have been integrated in a single die. However, with a few exceptions [4], often in these transceivers the high-power PA section is not integrated. Even in cases where the Tx PA is integrated in the transceiver die such as that of [4], the maximum achievable power has traditionally not been competitive with those in external SiGe or GaAs PA technologies. Additionally no production-quality high-power 5 GHz band 802.11a integrated CMOS PAs have been reported to date. The reasons that the PAs are often not integrated in the same die as the CMOS transceiver range from heat dissipation issues associated with large packages often required for transceiver ICs (which cannot accommodate a heat slug ground paddle), large inductive and capacitive parasitics associated with such large packages, and large dynamic range requirements for high peak-to-average ratio (PAR) OFDM signals. Additionally, well-known short comings of CMOS process technologies as applied to high power PAs such as low supply voltage and headroom, large device parasitics, lack of accurate device models and large passive and substrate losses complicate the issue further. Finally, issues related to coupling from the high power PA output to the sensitive transceiver blocks such as the VCO pose difficult challenges and often adversely affect time to market of a product. The 802.11a/g OFDM standard requires the transmitter output to have a transmit EVM of better than −25 dB for 54 Mbps data rate. The most recent version of the 802.11 PHY standard, 802.11n, utilizes numerous additional techniques that allows for even higher data rates and more robust links in the presence of multipath environments. The 802.11n standard adopts some mandatory or optional techniques such as multiple-input, multiple-output (MIMO) technology, the use of wider band channels, utilization of higher order constellations, and/or the use of lower coding rates for the modulation to achieve these goals. While the latter techniques requires a higher performance single path PA, the use of MIMO on the transmit path dictates the use of multiple PAs since MIMO techniques require dedicated receive or transmit radio paths from the antenna to the DSP core. MIMO production-quality transceiver chips have been reported in CMOS technology [3]. However, once again, the PAs are not integrated due to the high level requirements of the 802.11n standard as well as integration and CMOS challenges outlined above. The highest order modulations utilizing the highest coding rates in 802.11n are required to pass −28 dB transmitter EVM. An 802.11n system operating in a legacy 802.11a/g mode at 54 Mbps is allowed to relax the transmit EVM to −25 dB.

As shown in Fig. 1, the illustration of a 2 × 2 MIMO system, four power amplifiers would be required to interface to a dual-band 2 × 2 transceiver such as that of [3]. Two of these would cover the 2.4–2.5 GHz band, and the other 2 would cover 4.9–5.9 GHz. Although 4 discrete PAs can be used for this purpose, an integrated monolithic 4-PA solution would reduce cost, PCB area and complexity significantly. Maintaining reasonable isolation between the PAs operating simultaneously over the same band is important.

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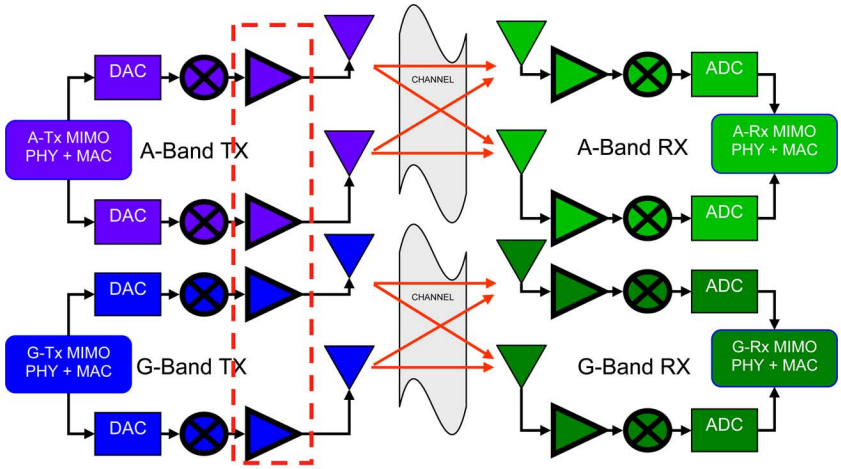


Fig. 1. 2×2 MIMO system block diagram.

Further, production-quality 2.4 GHz PAs have been demonstrated in the past using GaAs HBTs as well as SiGe technologies. However all such 5 GHz PAs have been limited to GaAs HBT technologies with no Si-based 802.11a PAs in the market so far. One of the primary difficulties in the implementation of a 5 GHz WLAN PA in Silicon technology is the reduction in gain at higher frequencies due to source/emitter degeneration by the ground bond-wire inductance. Various approaches have been taken to address this issue [7], [8], and will be discussed in later sections. On the other hand, most GaAs technologies have access to a technology known as a through-wafer-via which reduces the ground inductance quite considerably.

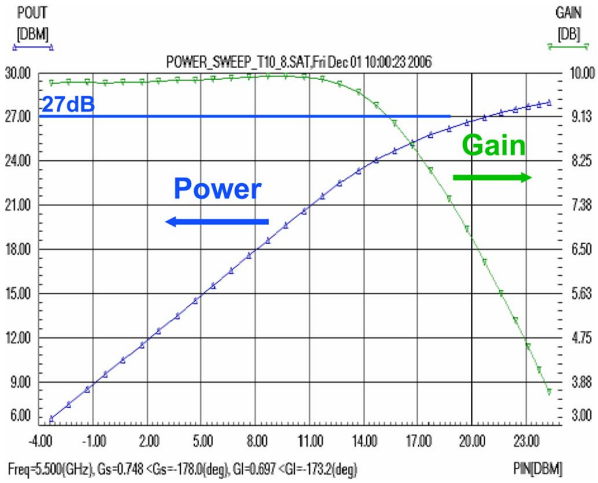
In this paper, a monolithic dual band 2×2 PA which achieves the requirements of 802.11n standard is demonstrated and is implemented in a SiGe BiCMOS process. Innovations in the processing side as well as circuit design techniques enable performance results comparable to those of discrete GaAs HBT solutions at a significantly higher integration level.

II. Challenges and Design Considerations

The choice of process technology has a profound impact not only on the PA design, but also on the commercial viability of a product. Considering integration viability and cost, CMOS would be the most desirable technology if the dual-band 2×2 PA was able to be integrated with the transceiver, such as that of [2], [3]. However CMOS is not the optimal process technology for this project, as discussed in the previous section. Commercially available 5 GHz-band PA products are still dominated by GaAs HBT technology yet their inability to integrate with CMOS circuits is an obvious drawback. For minimizing system size, cost, complexity, and the potential to implement a full 802.11n system on chip (SOC), SiGe HBT technology becomes an attractive alternative because it is developed as an add-on of a standard CMOS technology. Often, the technology is packaged into a design platform with extensive RF capability, such as RF passive components and accurate models. Also it is commercially offered by many established silicon foundries, such as IBM, Jazz, and TSMC.

While the design of a PA using SiGe HBT technology has been explored by many technologists, such as [5], there still remain major design challenges in the implementation of a SiGe 5 GHz-band PA for dual band MIMO 802.11n WLAN applications. The first challenge is how to minimize the emitter degeneration due to ground inductance which significantly reduces the gain of each amplification stage. The output stage which boasts the largest emitter size is particularly sensitive to emitter inductive degeneration. Any non-negligible bond wire or routing inductance will significantly degrade the output stage gain, especially for the single-ended 5 GHz-band PA design. The gain degeneration not only prevents the PA from meeting performance specifications, but also significantly reduces PA output power and efficiency. Another design challenge is optimizing the output power, gain and efficiency using the SiGe HBT at the 5 GHz-band frequency. The SiGe power HBT device which is designed for high breakdown voltage and reliable operation under supply voltage 3.3 V is still short of speed as compared to GaAs technologies [6]. It is a major design challenge to obtain gain, linear power and efficiency across the 4.9–5.9 GHz wide operation frequency. Also, at the 5 GHz-band frequency, higher substrate loss of the Si technology becomes an issue. In GaAs WLAN PA design, substrate loss is generally not a major concern due to the semi-insulating nature of the GaAs wafer. Such a high frequency wide band requirement coupled with the Si substrate loss poses serious challenges on the design of matching networks. The third major challenge is the integration of 4 power amplifiers on one monolithic substrate. Each PA requires its own input and output signal path with a reasonably small coupling between two PAs operating at the same frequency band. Also each PA requires its own power supply, emitter ground paths with minimum inductance, power detector and control signal. The complexity in the floor planning of a dual band 2×2 PA is much higher than that of a single PA. For example, in a single PA, short ground accesses are generally achievable without too much difficulty. However it becomes a different scenario when there are four PAs on a chip together.

In this work, different implementation techniques and design methodologies to achieve minimum emitter ground inductance



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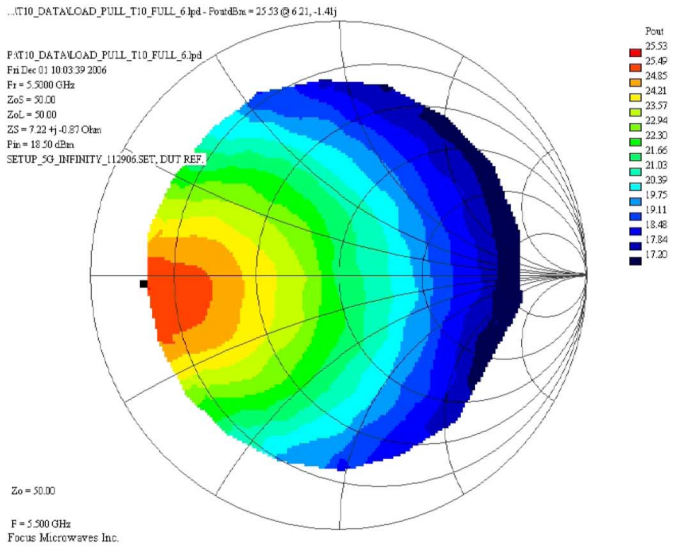

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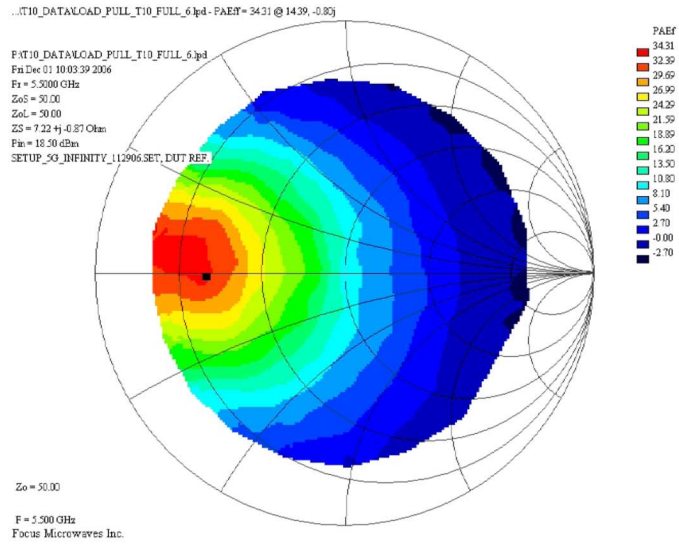


(c)

Fig. 2. (a) Output stage power transistor output power and gain versus input power from load-pull measurement at 5.5 GHz. (b) Output stage power transistor power contour at 5.5 GHz. (c) Output stage power transistor PAE contour at 5.5 GHz.

such as multiple short bond wires [8] and differential designs [7] are investigated and will be discussed in the following sections. Finally, a through wafer via (TWV) technology, similar to what is available with current GaAs technologies, is adopted along with the standard SiGe BiCMOS technology for this 2 × 2 PA implementation. Thus, low impedance ground is achieved and high gain, high efficiency 2.4 GHz and 5 GHz PA designs that can be integrated are therefore feasible with this TWV technology. A monolithic 2 × 2 dual band PA with fully integrated on-chip input, output and inter-stage matching is implemented in SiGe BiCMOS with TWV. Both 5 GHz-band and 2.4 GHz-band PAs achieve desirable gain, linear power and efficiency performances. Measured isolation between PAs also meets MIMO requirements.

III. Device and Process Technologies

The technology used in this work is the Jazz 0.18 μm SiGe BiCMOS based on a volume production technology described in [10]. The peak f_T and $f_{\max}$ of this self-aligned SiGe HBTs with both shallow and deep trench isolation are 38 GHz and 150 GHz, respectively, when V_{BC} is 1 V. The HBT can be operated with a 3.3 V voltage supply with sufficient ruggedness since the worst case collector-base and collector-emitter breakdown voltage is 12 and 4.5 V, respectively. This technology features four Al metal layers including a 5 μm thick top metal layer for inductors. The technology also includes both 3.3 V thick-gate and 1.8 V standard MOSFETs, high density MIM capacitors (1 fF/um^2), poly resistors and lateral pnp transistors. Accurate RF models for both active devices such as npn transistors and passive components such as MIM capacitors and spiral inductors are provided along with this process. These RF models proved to be reasonably accurate for initial schematic level designs, however EM simulation or layout parasitic extraction is still essential to complement the device models to obtain an accurate performance match with the real silicon. For power devices, load-pull measurements are performed to verify large signal models as well as load-line impedances in power simulations.

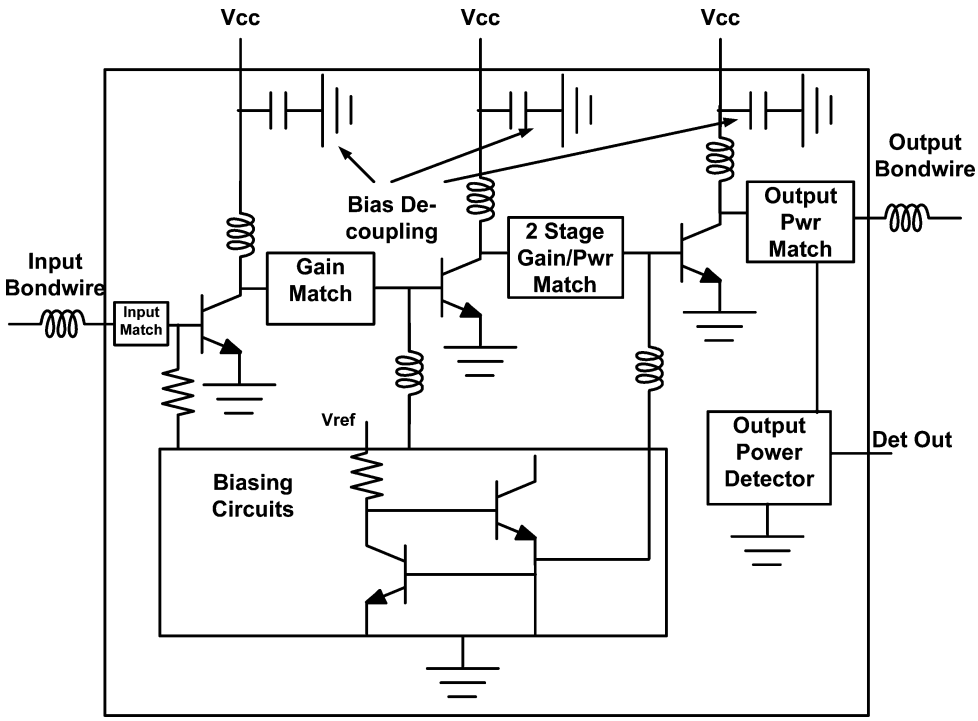


Fig. 3. Simplified schematic of each single PA.

IV. Power Device Load-Pull

The first step in designing a power amplifier is to determine the output power transistor size. An under sized output transistor cannot deliver enough RF power to meet required power output specifications. An oversized power transistor size will result in low PAE at the specified output power as well as excess quiescent current for a given small signal gain. Extensive research is carried out on the design of the power cell based upon load-pull measurement [11].

For an 802.11n OFDM signal with a desired -28 dB EVM, a minimum backoff of about 7 dB from the saturated power would be necessary. Therefore in order to achieve a $+18$ dBm linear power, a power transistor with $+25$ dBm saturation power would be required. For a fully integrated power amplifier with output impedance matching networks on chip, routing and matching network losses need to be carefully considered. As mentioned in the previous sections, Si substrate loss is not negligible and poses a challenge on the 5 GHz PA design. As such, output matching network losses were taken into consideration when determining the output size from the early stages of the design. In this project, output transistor sizes are determined with a saturation power of 27 dBm so that after on-chip matching, package and PCB trace losses the PA is still able to deliver 25 dBm saturation power for a 18 dBm linear power to the antenna.

Fig. 2(a), (b), (c) shows load-pull results of the final determined power device size for the 5 GHz-band. At 5.5 GHz, the saturation output power is about 27 dBm as shown in the plot. Power contours show the loadline impedance for max output power of 6–7 Ω and about 14 Ω for max PAE. When designing an output matching network to provide the loadline for the power transistor, trade-offs need to be taken between the max power and max PAE impedance points. With on-chip low-Q impedance matching elements, 50 Ω to 6 Ω impedance transformation ratio is not easily achievable and will result in a high loss. Actual loadline impedance in the design is therefore determined somewhere in between the max power and the max PAE impedances for a balance of output power, PAE, and design feasibility.

V. Circuit Design

To ensure enough power gain from the transmitter radio input to the antenna output, a three-stage class AB architecture is used for both 5 GHz-band and 2.4 GHz-band PA designs. A simplified schematic for each single PA is shown in Fig. 3, with all the matching elements and biasing circuits integrated.

Since the 5 GHz-band PA operates at a relatively high frequency with $\sim$1 GHz bandwidth, it is a major challenge to design this 5 GHz PA for enough gain and power performances over the entire bandwidth. The key to obtaining optimized output power, gain and efficiency is to find the appropriate size of the final stage PA transistor as mentioned. The final stage PA usually consists of one or several identical power cells whose emitter size, layout style and ballasting resistance are optimized in term of the maximum linear output power, gain, efficiency and thermal stability. As determined from load-pull measurement results, the total emitter area of the 5 GHz-band PA output stage is chosen to be $\sim 900\ \mu m^2$. It not only gives the output stage an adequate saturation power to meet the linear power requirement based on our power budget estimation but also provides enough gain at low biasing current density (0.05 mA/μm^2 in this class AB design). The key to both high PAE and minimum quiescent current is the careful selection of device sizes. The transistor size of sequential stages

are inversely proportional to the gain of the following stage. Therefore, the efficiency of the three-stage PA can be further optimized with carefully designed stage-to-stage drive ratios.

To maximize linear output power, gain and efficiency from 4.9 to 5.9 GHz, impedance matching networks are critical. In the matching circuit design, the output stage is designed to match to the load-line impedance determined by load-pull for an optimized combination of output power and PAE. The matching network is a band pass topology with a combination of shunt-series and series-shunt *LC* networks. Ground connection for the shunt component is critical in realizing this matching circuit. We will discuss implementation of ground connections in following sections. Besides the device load-line impedance, metal trace and substrate losses also need to be carefully taken into consideration when deciding the impedance transform ratio. The 2–3 inter-stage matching is a two-stage matching network, as shown in Fig. 3. When designing inter-stage matching for the driver-to-output stage matching, it is important to keep in mind that the driver stage needs to provide a linear drive to the output stage. Therefore the saturation power of the driver stage must be considerably higher than the required input power to saturate the output stage. The required source power for the output stage is determined from loadpull measurements and the driver stage device size is designed so that it can provide the input power to drive the output device into saturation with a few dB of margin. Gain matching for the inter-stage is equally important. The actual matching impedance for the driver is a compromise of power and gain. With power margin in the driver device size planning, the driver is ensured to provide enough linear drive power to the output stage even with its loadline pulled from the max power impedance toward the conjugate matching impedance to some extent for a better gain matching. The 2–3 inter-stage matching network is also realized with a band-pass *LC* network covering the whole 802.11a bandwidth. The 1–2 inter-stage is a broadband gain matching. This is because the first stage is a gain stage and the drive ratio is designed so that the first stage is able to drive the second stage well within its small signal linear output range.

Each PA also consists of a power detector at the output. The power detector is a B-C junction diode detector coupled to the output power transistor collector through a MIM capacitor and is designed to have a negative slope with output swing range matched to the baseband ADC read range. In each stage, a constant voltage biasing which is controlled by the reference voltage is fed through an inductor to the base of the PA transistor. This biasing circuit is designed to compensate the class AB power transistor base bias voltage drop caused by IR drop from the increased base current when the transistor is driven and self-biases itself. With this compensation, power transistors won't be clamped by the base voltage IR drop when power level increases. The size and geometry of the spiral inductor used in the biasing circuitry is optimized so that its series resistance helps control class AB gain expansion. In this case, the degree of gain expansion is manipulated with the base bias compensation together with the biasing inductor and its series resistance to adjust the AM-AM, AM-PM characteristics of the PA. A non-monotonic EVM versus output power curve which helps maximize low EVM power range for 802.11n applications can thus be obtained, as shown in the EVM versus output power curves in Figs. 14 and 15.

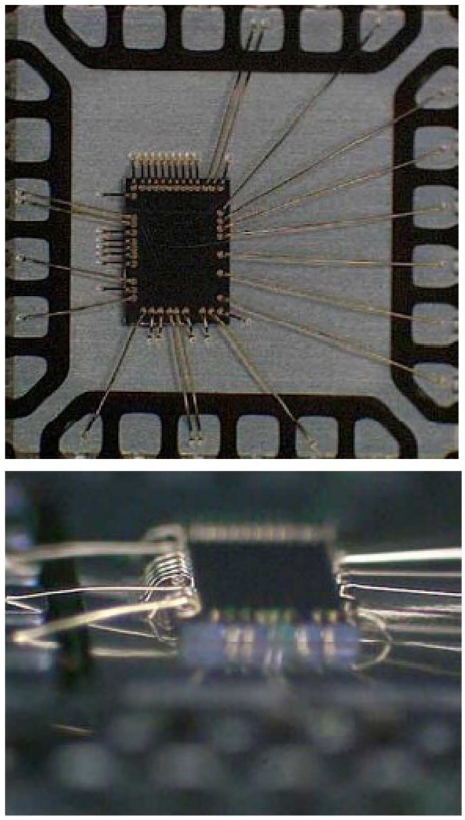


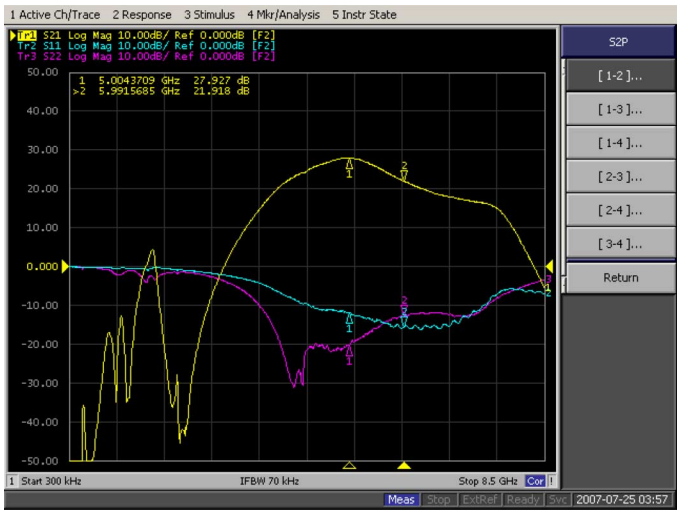
Fig. 4. Single-ended 5 GHz bond-wire PA inside package.

VI. Implementation

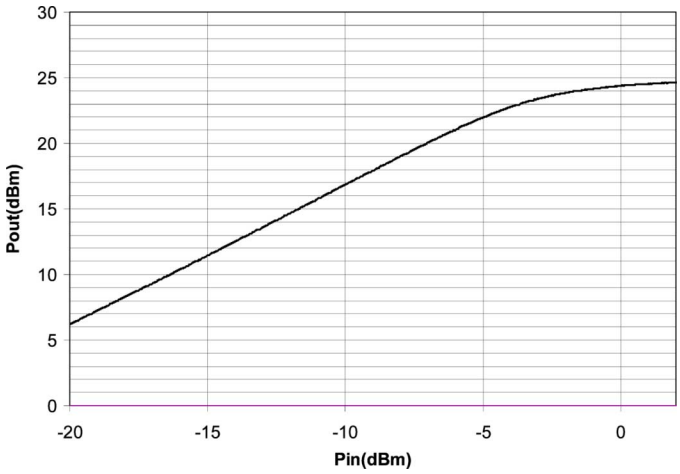
In order to develop a high performance 5 GHz PA for this 2 × 2 integration, different approaches have been taken, and will be discussed in the following sections.

A. Multiple Short Bond Wire Single-Ended Design

As discussed, the first design challenge is to provide a low impedance ground connection to the power transistor emitter such that the most critical power gain of the output stage is not degenerated. A straightforward way is to apply multiple short down bonds to the emitter of the power device to minimize ground impedance for the power stage [8]. In this project, a single-ended 5 GHz PA with multiple short down bonds was first investigated. Fig. 4 shows the photo of a PA die and its bonding in a QFN package. Measurement results from this bond wire 5 GHz PA show 28–22 dB small signal gain across band, saturation power of 24.5 dBm and −26 dB (5%) EVM power of 17.8 dBm with 14% efficiency at 5.75 GHz. Fig. 5(a), (b) show small signal S-parameter and CW output power plots for this PA at room temperature with 3.3 V supply. Although reasonable 802.11a performances can be achieved from this bond wire approach, it is still difficult to integrate four of its kind into a single chip 2 × 2 floor plan due to difficulties in bond wire arrangement and delicate package and bonding process. Another issue associated with this bond-wire 5 GHz PA is its sensitivity to bonding. Variation in wire length will cause significant variation in performances. This raises a concern in mass production yield.



(a)



(b)

Fig. 5. (a) 5 GHz bond-wire PA small signal responses. (b) 5 GHz bond-wire PA output power versus input power at 5 GHz.

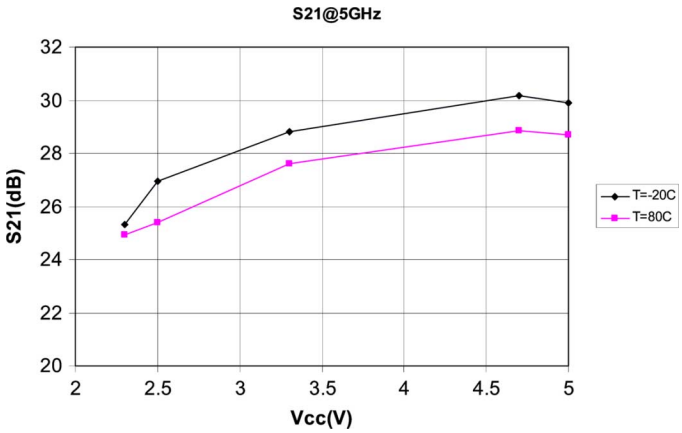


Fig. 6. Small signal gain versus supply voltage at $-20\,^{\circ}$C and $80\,^{\circ}$C ambient temperatures.

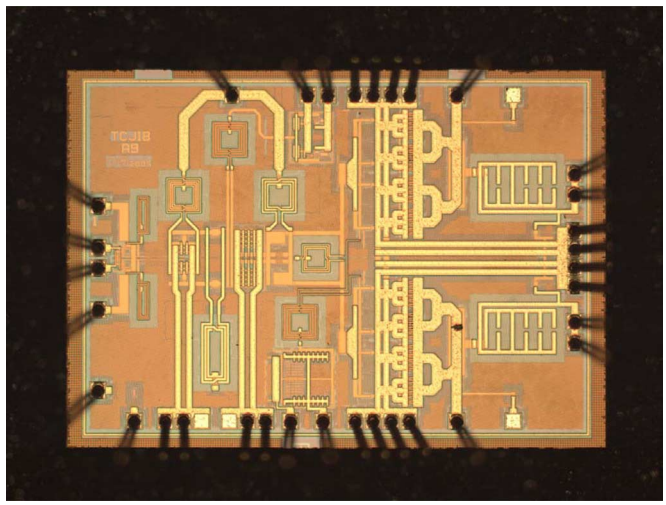


Fig. 7. 5 GHz differential PA die photo.

Measurements across temperature, supply voltage and VSWR have been carried out on this bond-wire 5 GHz PA for initial reliability studies. Comparing to differential or TWV PAs which will be discussed later, this single-ended bond-wire PA better reflects SiGe HBT device reliability due to the elimination of any non device-, or circuit-itself related complexity such as losses and effects from external baluns or from the TWV process. Fig. 6 shows measured S21 from this PA, at $-20\,^{\circ}$C and $80\,^{\circ}$C ambient temperature with V_{cc} from 2.3 V to 5 V. Reliability across temperature, supply voltage and VSWR has also been tested. Initial measurements with CW power stress at saturation output power level indicate the PA can survive VSWR up to 4:1 with $V_{cc} = 4.5$ V at $85\,^{\circ}$C ambient temperature.

B. Differential Design

A second approach to overcome the emitter degeneration is to use a differential topology. The differential design can effectively reduce the emitter degeneration inductance by employing virtual ground from the differential pair. Theoretically, the differential design benefits from the reduced impedance transformation ratio due to a higher single-ended loadline impedance caused by the 1/2 reduction in device size per single ended side. With a virtual ground, the emitter does not require a physical low impedance ground connection for differential signals therefore ground routing for multiple PAs on a single die becomes much easier. Other differential 5 GHz-band PAs have also been demonstrated [7]. In this project, a differential 5 GHz PA was designed and investigated, as showed in Fig. 7. Die size of the differential design is not too much larger than that of the single ended bond wire design due to the use of differential inductors through out the entire signal path for collector loading and impedance matching. These differential inductors save area and minimize DC connections. However as compared to their single ended counterparts, these differential inductors have lower Qs and self resonance frequencies. Therefore they degrade circuit performance such as overall gain, power and PAE. Also the differential design requires differential input signals and an off-chip differential to single end balun in the output to combine the output power to a single ended antenna. Measured S21 for the differential PA is shown in Fig. 8, with 24.5–22.7 dB small signal gain across band. EVM measurement of the differential

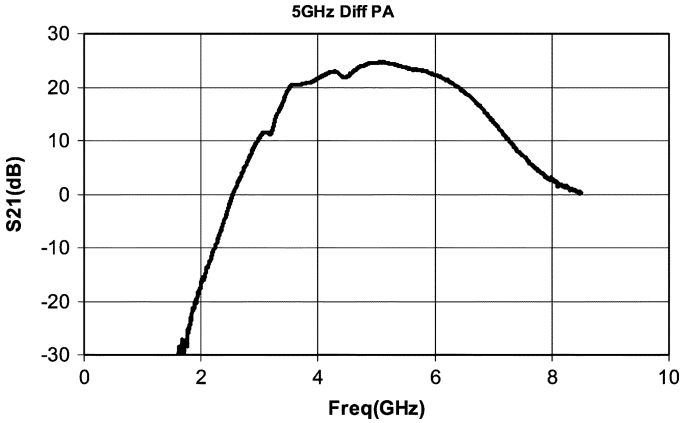


Fig. 8. 5 GHz differential PA small signal gain.

PA shows −26 dB (5%) EVM at a power of 16.9 dBm at the single-end output terminal of the off-chip balun. With excess losses from input and output baluns as well as low Q differential inductors, this differential PA shows less gain and output power as compared to the single ended PA does. Also overall PAE in the system is greatly degraded by the output balun loss. Although virtual ground for differential signals can be obtained from the differential design, excess even harmonics in the output spectrum still prove the common mode ground to be an issue. In order to minimize even harmonics, good common mode ground connections or harmonic traps are still necessary for this differential design to become a production PA design.

C. Single-Ended Design With TWV Technology

As a third approach, a Through Wafer Via (TWV) process (similar to which has been widely used in commercial GaAs PAs) is adopted in a silicon based SiGe BiCMOS platform to address the emitter ground inductance issue. In the single-ended PA design, the emitter degeneration due to bondwire inductance can be minimized by several short bondwires in parallel, as shown above. However, it is also often limited by the frequency, mutual inductances between bondwires and the number of pads that are available for down bonds. A highly doped substrate is proposed as the solution of the low impedance ground [9], especially for the single-ended 5 GHz-band PA. However, the substrate loss associated with the highly conductive substrate deteriorates the efficiency, especially between the PA transistors and the antenna. With the TWV capability on Si wafer, low impedance ground connections can be made anywhere inside the circuit. Power device emitter grounding or shunt matching component grounding is no longer an issue. A highly integrated 2 × 2 PA thus becomes achievable because ground connection difficulties are greatly reduced with this technology.

The TWV process is developed on the 0.18 μm SiGe BiCMOS technology [10] described in the earlier section. As illustrated in Fig. 9 for this Jazz TWV process, a metal layer is plated on the backside of a thinned Si wafer as the electrical ground. A metal post is deposited through the wafer to connect the PA transistor's emitter that is on the upside of the wafer to the backside ground metal layer. With TWVs, the parasitic emitter inductance in a single-end PA is effectively minimized without a delicate short bond wire package and large number of

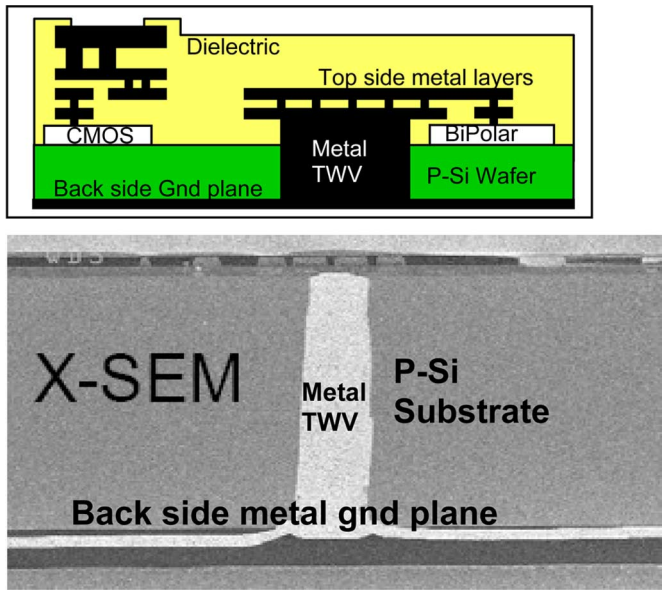


Fig. 9. Illustration of TWV process and its SEM cross section photo.

bond pads. Significant cost saving by the die size reduction can be realized in the 2 × 2 dual-band PA design and/or other SoC designs because low impedance grounds can be easily accessed in the middle of a die.

VII. Floor Planning, Layout and Package

For the dual band 2 × 2 PA integration, floor planning is critically important. In this project, 4 PAs are physically arranged in a A-G-G-A pattern from top to bottom. In order to minimize high frequency coupling between 2 5 GHz-band PAs, both 5 GHz PAs are arranged to the upper end and lower end of the chip, separated by the 2 2.4 GHz-band PAs in the middle.

In order to accurately achieve desired bandwidth and performance with fully integrated on-chip matching, extensive layout optimization and parasitic extraction are carried out using Cadence Assura and ADS Momentum EM simulator. Package effect such as bond wire inductance also needs to be carefully estimated using 3D EM simulation and taken into consideration when designing matching circuits. Each PA is designed to fully match to 50 Ω at package input and output pins without any external matching element. In the 5 GHz PA cell, two- or three-stage matching network designs are required for inter-stage and output matching to meet the gain and power requirement for 1 GHz operation bandwidth. Although more matching stages help widen impedance matching bandwidth, additional matching stages will also increase loss, especially on Si substrate, and die size as well. Therefore in this 5 GHz PA design, each impedance matching network design is limited to three stages at most.

Fig. 10 shows the photo of this 2 × 2 PA die in the package. Total die area measures 1.36 mm × 3.68 mm. In order to accommodate this special die size and pinouts, a QFN 4 mm × 6 mm 32 pin package was custom designed, the package lead frame and bonding are as shown. Input and output pins are arranged in both long sides of the package for easy access to the dual band MIMO transmitter RF outputs in one side and antennas in the opposite side.

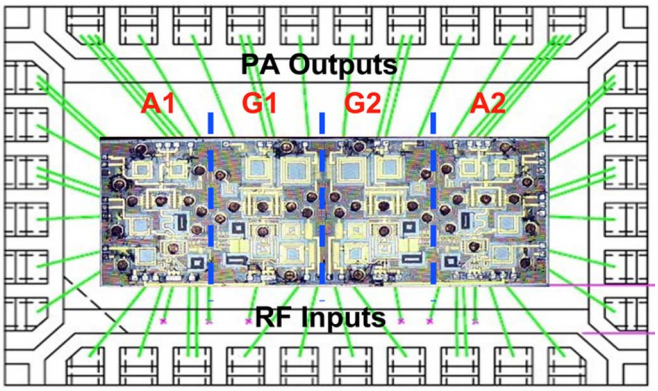


Fig. 10. 2 × 2 PA die photo and package bond diagram.

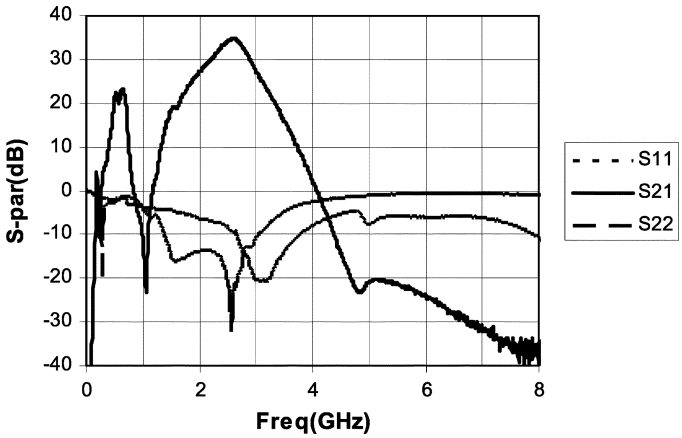


Fig. 11. 2 × 2 PA −2.4 GHz band PA S-parameter plots.

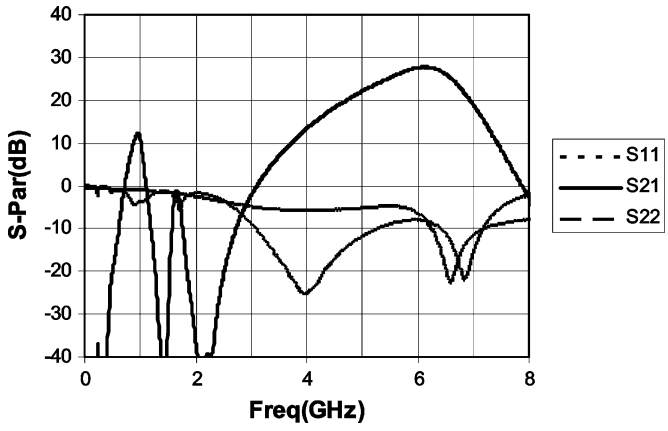
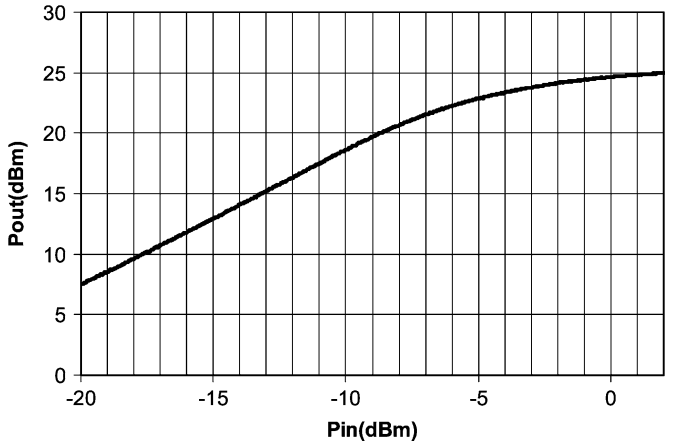
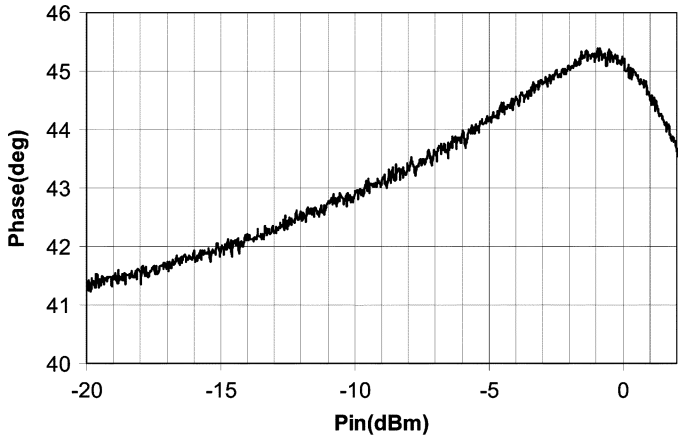


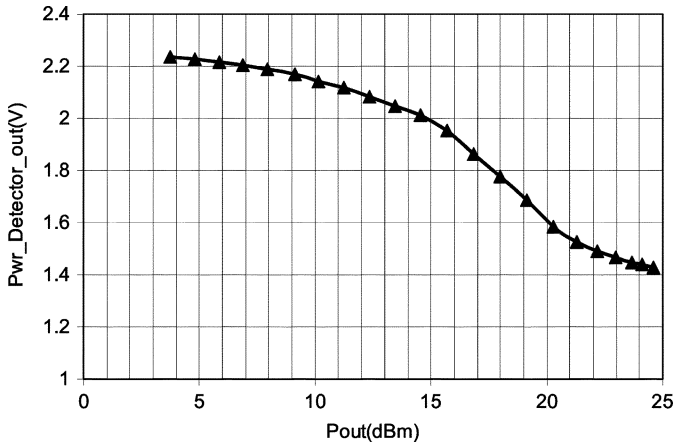
Fig. 12. 2 × 2 PA −5 GHz band PA S-parameter plots.



(a)



(b)



(c)

Fig. 13. (a) 2 × 2 PA −5 GHz band output Pout versus Pin. (b) 2 × 2 PA −5 GHz band output phase versus Pin. (c) Power detector output versus Pout.

VIII. Measurement Results

The packaged QFN 4 × 6 chip was mounted on a 4-layer PCB for testing. Connector and PCB trace losses were calibrated and de-embedded. Agilent E5071B 4-port VNA was used for S-parameters, 4-port isolation and AM-AM, AM-PM measurements.

For the 2.4 GHz PA small signal gain, Fig. 11 shows measured S-parameters, The S21 peaks at 2.6 GHz at 35 dB and at 2.4 GHz the S21 is about 33 dB.

Fig. 12 shows measured S-parameters for the 5 GHz PA, S21 shows peak gain of 27 dB at about 6 GHz. Fig. 13(a), (b) shows Pin-Pout and phase distortion(AM-PM) curve at 5.9 GHz. A saturation power of 25 dBm and phase distortion within 4 degree across the entire output power range are obtained from this PA. The output power detector response is shown in Fig. 13(c). CW power measurement results are consistent with load-pull measurement results for the output transistor, which shows 27 dBm of saturation power. With metal and substrate losses from the

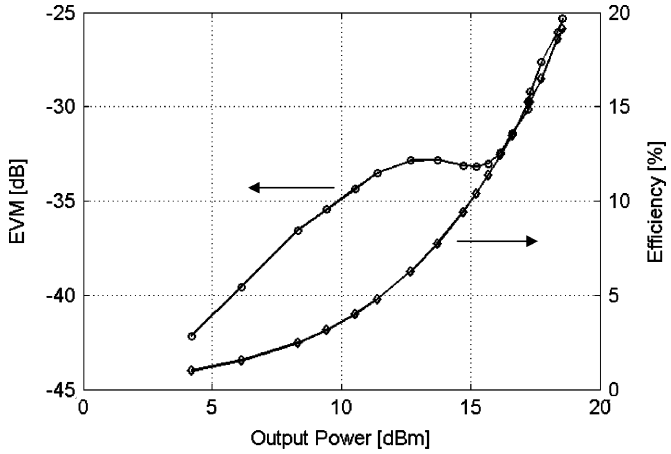


Fig. 14. 2 × 2 PA −2.4 GHz band 54 Mbps OFDM EVM and Efficiency versus Pout.

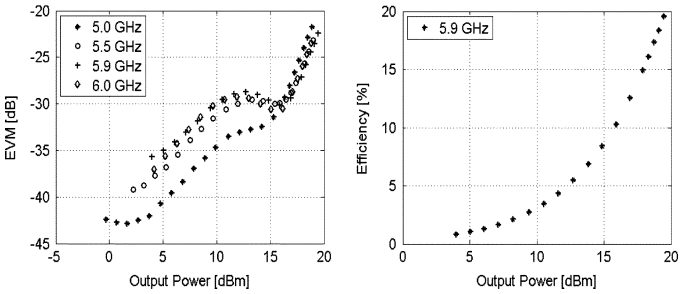


Fig. 15. 2 × 2 PA −5 GHz band 54 Mbps OFDM EVM and Efficiency versus Pout.

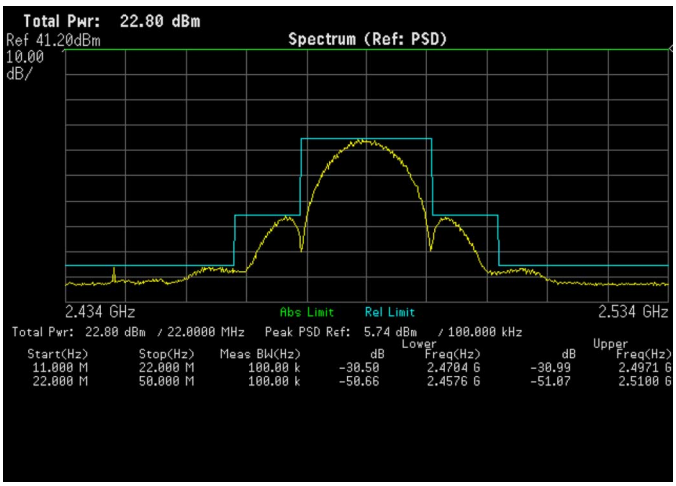


Fig. 16. CCK spectrum for the 2.4 GHz-band PA.

output matching network and package losses, 25 dBm is a reasonable number to be seen at the output pin of this PA.

Error vector magnitude (EVM), instead of traditional *IP3* or $P_{1\mathrm{dB}}$, is measured to determine the linear output power of the PA. Agilent E4438C signal generator and Agilent E4440A PSA + 89641 vector signal analyzer are used for 54 Mbps OFDM EVM measurements. With 3.3 V supply, at −25 dB EVM, the 2.4 GHz-band PA achieves 18.5 dBm output power with 19% efficiency, and the 5 GHz-band PA reaches 18.3 dBm output power with 15% efficiency at 5.9 GHz. At −28 dB EVM, the

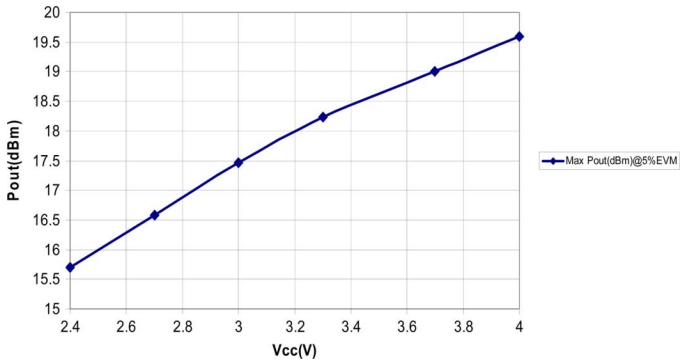


Fig. 17. 5% EVM P_{out} versus supply voltage at 5.9 GHz.

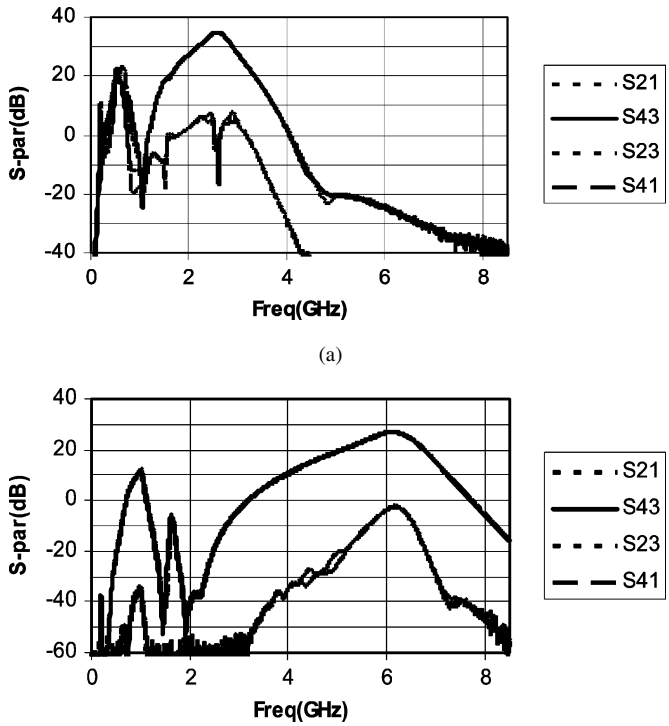


Fig. 18. (a) 2 × 2 PA 2.4 GHz band isolation. (b) 2 × 2 PA 5 GHz band isolation.

2.4 GHz-band PA delivers 17.5 dBm power with 16% efficiency, the 5 GHz-band PA achieves 17 dBm with 12.5% efficiency. The 54 Mbps OFDM modulated EVM and efficiency versus output power are plotted in Fig. 14 for the 2.4 GHz-band and Fig. 15 for the 5 GHz-band. CCK measurements are performed on the 2.4 GHz-band PA. Maximum CCK output power spectrum meeting the 802.11b spectrum mask is shown in Fig. 16. Since the transistor collector voltage swing is proportional to the collector supply voltage, PA saturation power and linear power outputs are thus highly related to Vcc as well, Fig. 17 shows 5%(−26 dB) EVM output power versus supply voltage at 5.9 GHz. It is clear that the PA output power follows supply voltage monotonically.

The isolation between PAs is also an important figure-of-merit for a monolithic dual-band 2 × 2 PA. The isolation performance is measured using Agilent E5071B 4-port VNA. S23 & S41 in Fig. 18(a), (b) shows wideband isolation measurements

for both 2.4 GHz and 5 GHz pairs. In-band isolation is >25 dB for 2.4 GHz-band and >30 dB for 5 GHz-band in this dual-band 2×2 PA configuration.

IX. Conclusion

A fully integrated dual band 2×2 802.11n MIMO PA has been designed and implemented using 0.18 μm SiGe HBT with TWV process. Before the availability of TWV process on Si wafer, both bond wire and differential approaches to the 5 GHz 802.11a PA have been investigated as part of the development process to this 2×2 PA. This paper has presented a complete development of 802.11 power amplifiers using the SiGe technology. Measured results from the fully integrated 2×2 PA show very promising gain, linear power and efficiency performances as well as good PA to PA isolation results. To the knowledge of the authors, this is the first production quality 2×2 dual band 802.11n MIMO PA integrated in a monolithic Si substrate.

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References

[1] S. Mehta *et al.*, "An 802.11g WLAN SoC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 94–95.

[2] A. Behzad *et al.*, "A 5 GHz direct-conversion CMOS transceiver utilizing automatic frequency control for the IEEE 802.11a wireless LAN standard," *J. Solid-State Circuits*, pp. 2209–2220, Dec. 2003.

[3] A. Behzad *et al.*, "A fully integrated MIMO multiband direct conversion CMOS transceiver for WLAN applications (802.11n)," *J. Solid-State Circuits*, pp. 2795–2808, Dec. 2007.

[4] D. G. Rahn *et al.*, "A fully integrated multiband MIMO WLAN transceiver RFIC," *J. Solid-State Circuits*, pp. 1629–1641, Aug. 2005.

[5] J. B. Johnson, A. J. Joseph, D. C. Sheridan, R. M. Maladi, P.-O. Brandt, J. Persson, J. Andersson, A. Bjorneklett, U. Persson, F. Abasi, and L. Tilly, "Silicon-germanium BiCMOS HBT technology for wireless power amplifier applications," *J. Solid-State Circuits*, vol. 39, no. 10, pp. 1605–1614, Oct. 2004.

[6] K. Nellis and P. J. Zampardi, "A comparison of linear handset power amplifiersin different bipolar technologies," *J. Solid-State Circuits*, vol. 39, no. 10, pp. 1746–1754, Oct. 2004.

[7] W. Bakalski, W. Simbürger, R. Thüringer, A. Vasylyev, and A. L. Scholtz, "A fully integrated 5.3- GHz 2.4-V 0.3-W SiGe bipolar power amplifier with 50 Ω output," *J. Solid-State Circuits*, vol. 37, no. 7, pp. 1006–1014, Jul. 2004.

[8] A. Italia, L. L. Paglia, A. Scuderi, F. Carrara, E. Ragonese, and G. Palmisano, "A silicon bipolar transmitter front-end for 802.11a and HIPERLAN2 wireless LANs," *J. Solid-State Circuits*, vol. 40, no. 7, pp. 1451–1459, Jul. 2005.

[9] W. Bakalski, K. Kitlinski, G. Donig, B. Kapfelsperger, C. Kuehn, C. Ahrens, W. Österreicher, W. Auchter, R. W. Arpad, and L. Scholtz, "Design of a dual-band wireless LAN SiGe-bipolar power amplifier," in *Proc. 2004 High Frequency Electronics*, 2004, pp. 18–28.

[10] K. Schuegraf *et al.*, "0.18 μm SiGe BiCMOS technology for wireless and 40 Gb/s communication product," in *Proc. 2001 BCTM*, Sep. 2001, pp. 147–150.

[11] N. Jiang, Z. Ma, P. Ma, V. Reddy, and M. Racanelli, "SiGe power HBT design considerations for IEEE 802. 11 applications," in *Proc. 2005 European Microwave Conf.*, 2005, p. 4.

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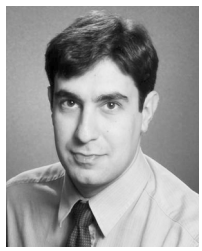

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