Multiband Multi-Standard Transmitter using a Compact Power Amplifier Driver

Håkan Magnusson and Håkan Olsson

Radio Electronics LECS, Department of Microelectronics and Information Technology, Royal Institute of Technology , KTH-Electrum 229, SE-164 40 Kista, SWEDEN, hmag@imit.kth.se

Abstract — **This paper presents a multistandard transmitter solution using a new power amplifier (PA) driver [1] operating in the broadcast, mobile, and the 2&5 GHz ISM bands. The use of dual-loop feedback in the driver provides a matched output without area consuming matching networks. The circuit size is as small as 0.3 mm^2 for the used 0.18 µm CMOS process, saving about 0.7 mm^2 silicon area. Measurement results show a gain higher than 7.8 dB with a maximum output power of +4 dBm for all bands and using a supply voltage of 1.8V.**

Index Terms — **Multiband transmitter, Power amplifiers, Wideband amplifiers, dual-loop feedback, pre-amplifier, PA driver.**

I. INTRODUCTION

The rapid development of wireless communication systems drives the radio-frequency (RF) ICs to complex functionalities and low cost implementations. To avoid the use of expensive (discrete) components, the transceivers are typical highly integrated in a silicon process, such as RF-CMOS. The chip area is desired to be as small as possible for a low cost solution. One of the most area consuming parts in multi-standard transmitters is the power amplifier driver. Typically, each frequency band has one separate narrowband power amplifier (PA) driver [2]-[4]. Using one circuit that can handle different frequency bands and standards would hence save chip area.

A common technique for wideband amplifiers is using several distributed gain stages [5]-[8]. This technique features a large bandwidth and a matched output. However, each gain stage requires a matching section that consists of area consuming inductors and capacitors. Large bandwidth and matched output can however be achieved without distributed gain stages and area consuming matching sections by using dual-loop negative feedback [9]. This technique has previously been implemented in integrated multi-band multi-standard receivers [10] and LNAs [11] where a matched input is required.

This paper presents an area-efficient multiband multistandard transmitter using a compact power amplifier driver. The use of a dual-loop negative feedback in the PA driver provides matched output impedance in all frequency bands without the use of any area consuming on-chip matching section with inductors. The result is a cost effective multiband multi-standard transmitter solution.

In the next section, we will describe basic design principles of this work. In section III, the PA driver circuit topology is presented and discussed. Section IV. Presents measurement results of the circuit discussed in Section III. Finally, we summarize our major findings in Section V.

II. TRANSMITTER DESIGN

Figure 1 shows a conceptual example of an area-efficient multiband multi-standard transmitter. The transmitter architecture is dependent on the used standards. The architecture in Fig. 1 is based on FDD duplexing. If both FDD and TDD duplexing are required, a separate architecture should be designed for the TDD system.

The high efficiency PAs are optimized for certain RF-bands while the preceding on-chip PA driver operates in all frequency bands, handling the requirement of all standards. The minimum requirement on the PA driver is hence set by the most demanding wireless standard.

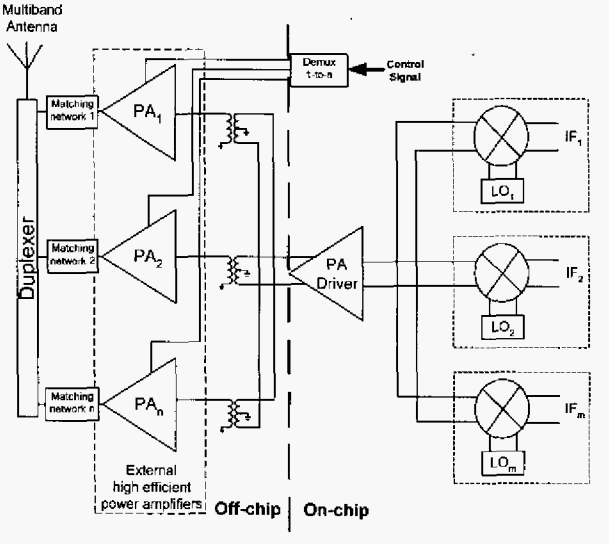

Fig. 1 Conceptual example of a multiband transmitter. (n = index of RF band, m = index of standard

0-7803-8983-2/05/$20.00 © 2005 IEEE

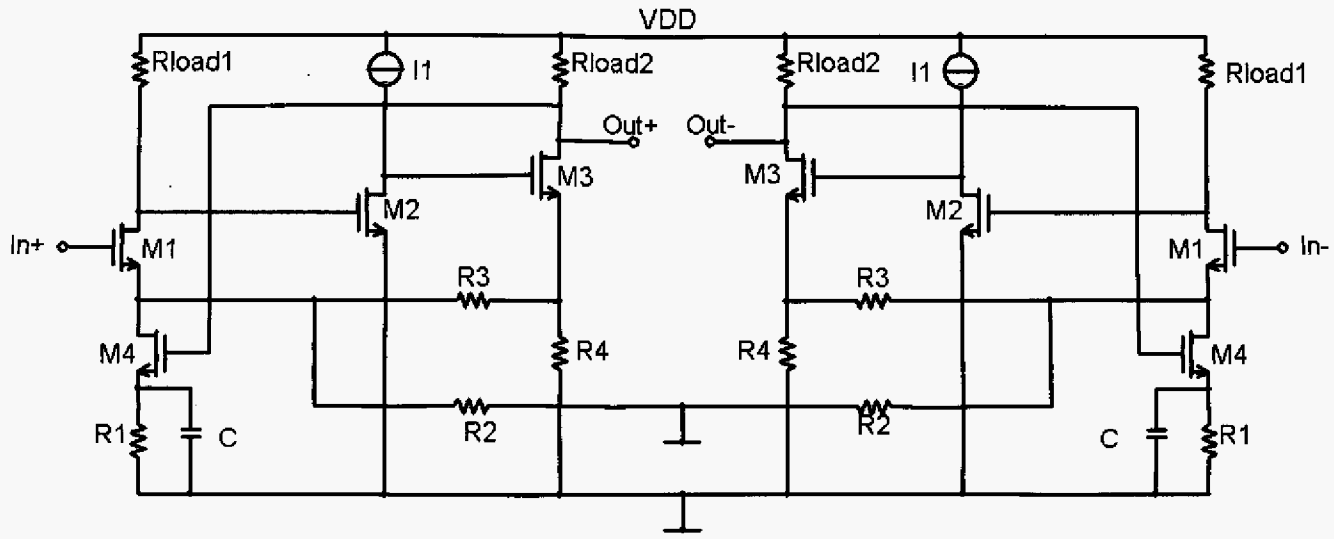

Fig. 2 Schematic of dual-loop power amplifier driver

Important properties of the PA driver, beside output power, are a matched output impedance and linearity. Nonlinearities in the PA introduce both spectral re-growth and signal compression, as well as phase distortion, thus distorting the original signal constellation for digital modulations.

The power consumption on the other hand is not critical as for power amplifiers since the dissipation is comparably small.

The local oscillators (LO) needed are commonly [2]-[4] reused with the receiver part and are hence not addressed here.

III. PA DRIVER CIRCUIT DESIGN

Figure 2 shows the schematic of the class A PA driver. The circuit uses two feedback loops were one feedback-loop fixes the voltage-to-current gain (series-series feedback) and the other fixes the voltage-to-voltage gain (Series-shunt feedback). The output impedance is then the ratio between the two gains [9].

The core circuit consists of the transistors M1-M3 and the resistors R2-R4. This core circuit topology is the voltage-to-current amplifier where the output current is compared with the input voltage indirectly through the drain current of M1. The output current is sensed through the resistance R4 and the resulting voltage across R4 is compared with the voltage over R2 through the resistor R3, thereby controlling the voltage-to-current gain. The second loop fixes the voltage-to-voltage gain using active feedback. The output voltage is sensed by M4 that controls a part of the drain current of M1, thereby controlling the voltage-to-voltage gain. The voltage gain and output impedance are given by (1) and (2):

$$A = \frac{v_{out}}{v_{in}} \approx \frac{R_{load} \cdot \left(R_1 + \frac{1}{g_{m4}}\right) \cdot (R_2 + R_3 + R_4)}{R_{load} \cdot R_2 \cdot (R_3 + R_4) + R_2 \cdot R_4 \cdot \left(R_1 + \frac{1}{g_{m4}}\right)} \quad (1)$$

$$Z_{out} \approx \frac{R_4 \cdot \left(R_1 + \frac{1}{g_{m4}}\right)}{R_3 + R_4} \quad (2)$$

These relations are valid as long as an adequate loop gain can be realized. Further, the transistor M3 are assumed to have adequate size and bias current to have a large drain-source resistance, r_{ds}.

Since the output impedance (2) is dependent of the transconductance of M4, a capacitance C is placed in parallel to R1 to increases the bias current of M4 at higher frequencies. Thereby achieving matched output impedance at high frequencies.

Resistive loads, R_{load1} and R_{load2}, ar e used on M1 and M3 to increase the bandwidth at the cost of reduced gain. To achieve sufficient gain, an active load is used at M2.

A. Output power

The resistor R4 is chosen as small as possible to save voltage headroom at the output without compromising the required loop gain. The maximum output power is determined by the maximum voltage level at the output since the output impedance is fixed through the feedback network. The single-ended output impedance is set to 50Ω. The 1.8 V supply voltage limits the output current and losses from wire resistance are hence reduced. The circuit

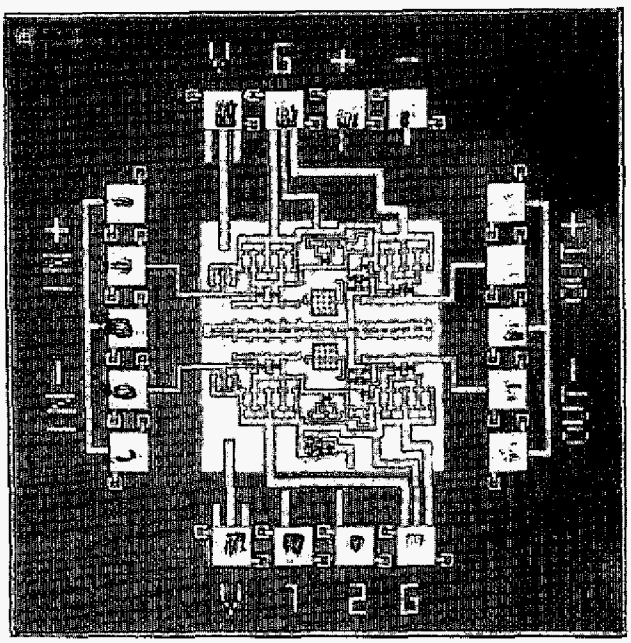

Fig. 3 Die photo. Circuit size is 540x570μm excluding probe pads.

was implemented in a differential configuration to increase the output power and to suppress second order distortion.

B. Linearity

The linearity of the circuit in Fig. 2 depends on the linearity of the voltage-current amplifier and the voltage-voltage amplifier. The former depends on the circuit topology and loop-gain of the core circuit and the later on the active feedback.

The core circuit is a three stage amplifier where the last transistor, M3, is the dominant source of non-linearity. A high gain in the second stage, M2, mitigates this non-linearity in conjunction with increased loop gain.

Using active feedback introduce an additional source of non-linearity due to the property of the feedback transistor M4. However, since the transistor is placed close to the input, the effect on the non-linearity is minimized [9].

IV. MEASUREMENT RESULTS

The dual-loop feedback PA driver shown in Fig 2 was implemented in a 0.18μm RF-CMOS process. The chip area of the fabricated circuit, shown in Figure 3, excluding probe pads was 0.3mm^2 (540μm x 570μm). This is about 0.7 mm^2 less than using separate PA drivers [3].

On-chip measurements were performed in the 0.9GHz, 1.8GHz, 2.4GHz and the 5.2GHz bands. Wide-band baluns were used at both the input and the output up to

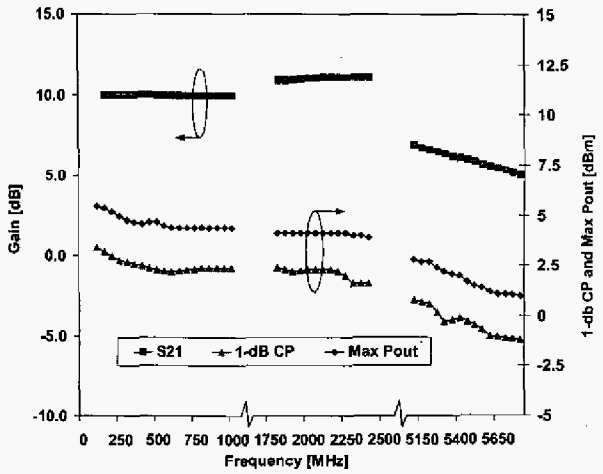

Fig. 4 Measured Gain, 1-dB CP and maximum output power.

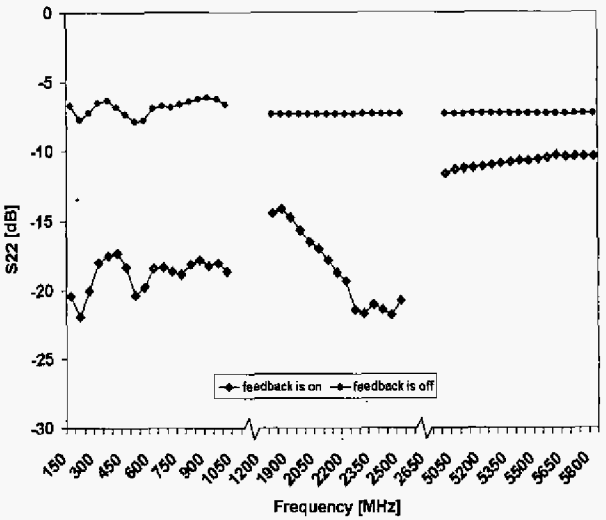

Fig. 5 Measured S22 at the output of the PA driver.

2.4GHz. Measurements at 5.2GHz were performed single-ended, but were corrected by 6dB instead. The input was matched to 50Ω single ended via a shunt resistance.

The input was also biased with 0.9V using a bias-T. All measurements were made using a 50Ω system at room temperature.

The measured gain, 1-dB compression point and the maximum output power are shown in Figure 4. The power gain is 10.0 dB at 900 MHz while the maximum power gain is 11.1dB at 2.4GHz. The small increase in gain at 1.8 GHz is due to the compensation capacitance C.

The 1-dB compression point is +2.4dBm at 0.9GHz and 1.8GHz while +1.6dBm at 2.4GHz and +0.6dBm at 5.2GHz. The maximum output power at 0.9GHz is +4.4dBm, +4.0dBm at 1.8GHz, +3.9dBm at 2.4GHz and +2.7dBm at 5.2GHz

To show the effectiveness of the dual-loop feedback, the reflection parameter S22 at the RF output, both when the supply voltage is turned on and off, is shown in Fig. 5.

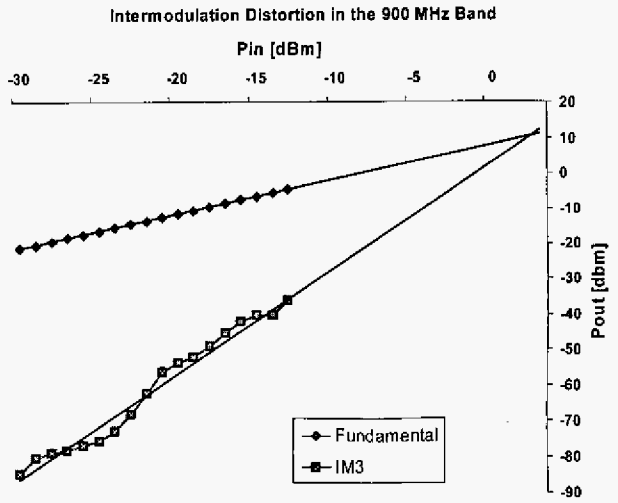

Fig. 6 IP3 measurement of the PA driver in the 900 MHz band.

TABLE I

SUMMARY OF MEASURED PREFORMANCE

	900MHz	1.8GHz	2.4GHz	5.2GHz
Gain [dB]	10.0	11.0	11.1	7.8
S22 [dB]	-18.2	-14.4	-21.4	-11.1
IIP3 [dBm]	+3.5	+1.2	+1.0	+0.5
OIP3 [dBm]	+13.5	+12.2	+12.1	+8.3
Output P_{1dB} [dBm]	+2.4	+2.4	+1.6	+0.6
Power consumption	50mA from 1.8V supply			

S22 is lower than -14.4dB from 0.1GHz up to 4.2GHz while lower than -11.1dB in the 5GHz band. The peaking of S22 at 1.8GHz is due to the compensation capacitance C while the increase in S22 at higher frequencies is an effect of reduced loop-gain.

The linearity of the circuit was measured using a two-tone test. The third-order intermodulation distortion was measured to determine the output IP3. The output IP3 was +13.5dBm at 0.9GHz, +12.2dBm at 1.8GHz, +12.1dBm at 2.4GHz and +8.3dBm at 5.2GHz. The circuit dissipated 50mA with a supply voltage of 1.8V.

V. SUMMARY

The design of a multi-standard transmitter using a new wide-band power amplifier driver and existing components has been presented. Measurements of the PA driver have been performed in the broadcast, mobile, and the 2&5 GHz frequency bands. The PA driver achieves higher than +7.8 dB gain, more than +0.6dBm 1dB CP and higher than +8.3 OIP3, with S22 less than -11.1 dB at the frequency bands of interest. The use of dual-loop feedback thus achieves a wideband matching without area consuming matching networks. A substantial cost reduction of the driver and thus the whole transmitter is now possible.

REFERENCES

[1] H. Magnusson and H. Olsson., "Compact Wideband Power Amplifier Driver with Matched Output", unpublished

[2] S. Aggarwal, *et .al.*, "A Highly Integrated Dual-Band Triple-Mode Transmit IC for Cellular CDMA2000 Applications", *J. Solid State Circuits*, pp. 1561-1569, September 2003.

[3] R. Ahola, *et al.*, "A Single-Chip CMOS Transceiver for 802.11a/b/g Wireless LANs ", ", *J. Solid State Circuits*, vol. 39, pp. 2250-2258, December 2004.

[4] K. Vavelidis, *et al.*, "A Dual-Band 5.15–5.35-GHz, 2.4–2.5-GHz 0.18μm CMOS Transceiver for 802.11a/b/g Wireless LAN ", *J. Solid State Circuits*, vol. 39, pp. 1180-1184, July 2004.

[5] R.-C. Liu, *et .al.*, "Design and Analysis of DC-to-14-GHz and 22-GHz CMOS Cascode Distributed Amplifiers", *J. Solid State Circuits*, vol. 39, pp. 1370-1374, August 2004.

[6] C. Grewing, *et al.*, "Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitters", *Radio Frequency Integrated Circuits Symposium*, pp. 87-90, June 2004.

[7] B. Ballweber, *et al.*, "A Fully Integrated 0.5–5.5-GHz CMOS Distributed Amplifier", *J. Solid State Circuits*, vol. 35, pp. 231-239, February 2000.

[8] C. Duperrier, *et al.*, "New Design Method of Uniform and Nonuniform Distributed Power Amplifiers", *J. Solid State Circuits*, vol. 35, pp. 231-239, February 2000.

[9] E. H. Nordholt, *Design of high-performance negative-feedback amplifiers*, New York, NY: Elsevier Science Publishing Company Inc., 1983

[10] Adiseno, M. Ismail, H. Olsson "A Wide-Band RF Front-End for Multiband Multistandard High-Linearity Low-IF Wireless Receivers", *J. Solid State Circuits*, pp. 1162-1168, September 2002.

[11] Adiseno, H. Magnusson, and H. Olsson, "A 1.8-V Wide-Band CMOS LNA for Multiband Multistandard Front-End Receiver," *In Proc. ESSCIRC2003*, pp. 141-144, September 2003.