A 27GHz, 31dBm Power Amplifier in a 0.25µm SiGe:C BiCMOS technology

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Abstract — **This paper describes an 8-way in-phase current combining power amplifier (PA) for Ka-band applications implemented in a 0.25um SiGe:C BiCMOS technology. The PA achieves a saturated output power of 29.7dBm at 27GHz with a maximum PAE of 10.5%. After applying load-pull, this output power increases further to a level of 31dBm with a maximum PAE of 13%. The small-signal gain is 24.5dB and the saturated gain is more than 14.7dB in the band of interest. The consumed area is only 2.83mm^2.**

Index Terms **— power amplifier, millimeter-wave, power combining, SiGe BiCMOS**

I. INTRODUCTION

The Ka-band offers a wide range of applications, like VSAT, DVB, LMDS and radar. Although compound III-V transistors can be used for implementing the power amplifier in these systems, silicon transistors are becoming more favorable due to their low cost and high integration capability. However, operating in the (near) mm-wave frequency regime complicates the realization of Watt-level output powers due to the low breakdown voltage of these silicon transistors. Recently, silicon-based power amplifiers employing transmission-line based power combiners achieve Watt-range (P>0.5W) output powers in the 45GHz band [1], [2].

The presented work achieves 29.7dBm of output power at 27GHz in a 0.25µm SiGe:C BiCMOS technology which is 1.3dB more power than the highest reported output power in in the (near) mm-wave frequency regime [1]. After applying load-pull, the PA delivers another 1.3dB more power to result in 31dBm. It employs 8-way output power combining, a 4-way power splitter at inter-stage matching and an input splitter.

II. CIRCUIT DESIGN

The circuit diagram of the PA is shown in Fig. 1. It consists of a 2-way transmission-line based input power splitter (PS), with each path followed by a driver (AS1). The inter-stage network consists of a 4-way transmission-line based power splitter, with at each splitter output an output stage (AS2). The output powers of the in total eight output stages are combined towards the 50Ω load by employing an 8-way transmission-line based power combiner (PC).

The output stage (AS2) consists of a cascoded transistor pair, with a low-voltage common-emitter (LV-CE) device and a high-voltage common-base (HV-CB) device, as shown in Fig. 2. This configuration enhances the output stages' gain and available breakdown voltage [3]. The latter increases the required load impedance, which is beneficial for output network losses, and also reduces the required DC-current. This reduces the minimum required metal track width for preventing electromigration. The devices are scaled such that both operate near peak G_{max} current density and in their "safe operating area" (SOA) regarding electro-thermal breakdown [4]. This resulted in a HV-CB device with a 0.4x20.4x20µm emitter area, which is a factor 2.5 larger than the LV-CE emitter area (0.4x20.4x8µm). Resistive base biasing is implemented for both devices with an additional high-pass shunt RC network (41Ω, 2p) at the LV-CE device's base. This improves electrical stability at lower frequencies and also the devices' thermal stability as it functions as base-ballasting. The output stages' load impedance Zas2 its optimum is 3.9+j8.8Ω, where the inductive imaginary part resonates out the output capacitance of the output stage at the fundamental frequency.

The 8-way output power combiner (PC) uses in-phase current combining [5], [1] by employing CPW transmission-lines (TLo0-TLo4), which are kept short to minimize insertion loss. The lines' characteristic impedances and lengths are selected together with lumped series inductors (Lo2) and shunt inductors (Lo4) to perform impedance matching at the same time. Capacitance Co4 is inserted for DC-blocking purposes. Combining transmission lines and lumped components for matching reduces losses and area. Deep trench isolation (DTI) is implemented below the passives to improve their Q-factor by reducing the substrate parasistics. To obtain the combiner's optimum design parameters for minimum loss targeting the output stages' optimum load impedance, an exhaustive search optimization routine was implemented in Matlab. This routine is based on an even-mode analysis of the combiner and uses data-based models for the various matching components to improve accuracy, which are extracted from the technology library. The resulting combiner's loss is 2.4dB with the even-mode impedance transformation path from 50Ω load towards the output stages' output shown in Fig. 3. The combiner's performance is verified by employing an EM-simulator. The layout implementation of the combination of TLo4, Lo4 and Co4 is shown in Fig. 4 with the inductive loop formed by shunt inductor Lo4 visible. As inter-stage network (ISN) two times a 4-way CPW-line in-phase current splitter (TLm1-TLm2) is implemented together with lumped shunt capacitances (Cm2) for matching and series capacitances (Cm1) for DC-blocking purposes. This 4-way splitting topology reduces the number of required parallel drivers

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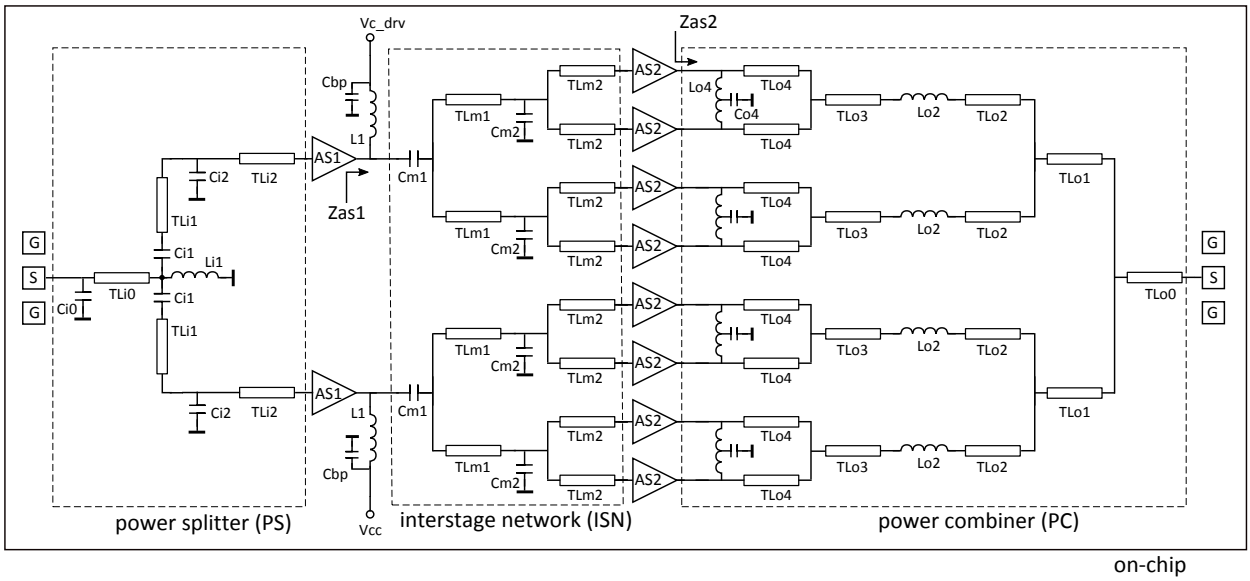

Fig. 1 Circuit diagram of the 8-way power combined PA.

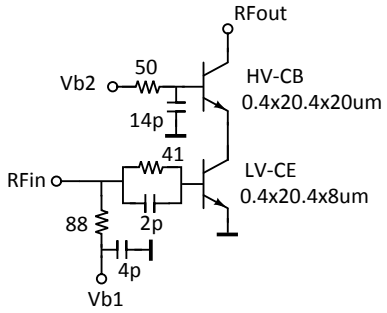

Fig. 2. Circuit diagram of both output stage AS2 and driver AS1.

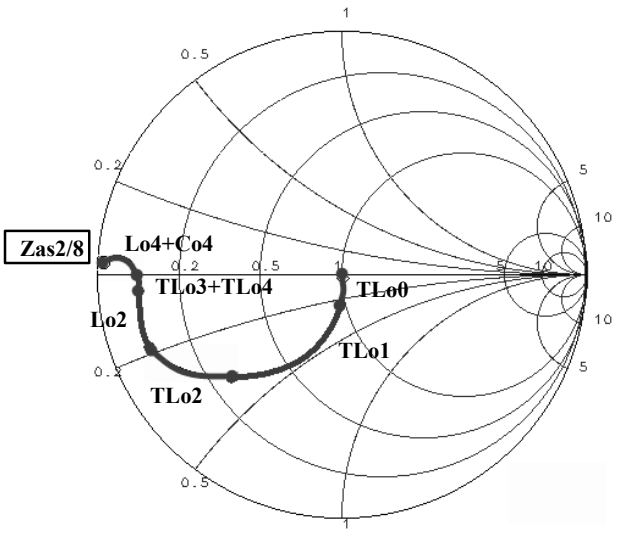

Fig. 3. Impedance transformation 8-way power combiner from 50Ω load to impedance Zas2 after even-mode analysis.

to only two, which reduces the number of required RF chokes (L_1) significantly and hence reduces area. Chokes L_1 are a combined lumped/microstrip-line inductor design and C_{bp} is a distributed bypass capacitor with a total value of 64pF to offer a broadband low impedance path, favorable for low frequency stability. Next to this, both drivers AS1 are operating now fully symmetrical. For the drivers AS1 the same cell used as output stages AS2 is implemented (see Fig. 2).

The 2-way CPW-line in-phase current splitter (PS), using additional lumped components, transforms the input impedance finally to ~50Ω. A high-pass filter is implemented with a shunt inductor (Li1) and series capacitances (Ci1) to reduce gain at lower frequencies.

A combined RC-extraction/EM-simulation is performed on the design to include all the device parasitics, layout interconnect, inductors and bond pads carefully. Stability of the design is checked at distinctive internal nodes using the method described in [6] as internal (odd-mode) oscillation loops can exist within this multi-cell topology. In that case the

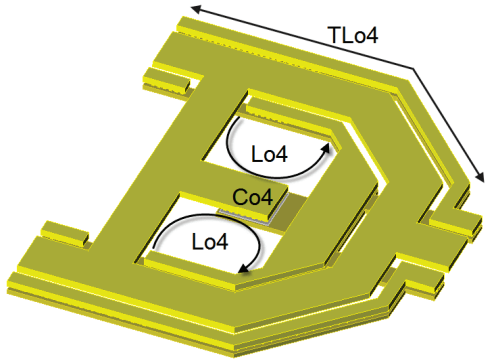

Fig. 4. Layout implementation of the combination of TLo4, Lo4 and Co4, with the inductive loop formed by shunt inductor Lo4 shown.

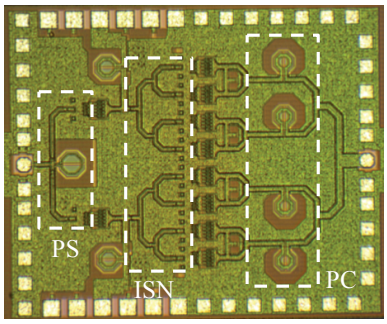

Fig. 5. Chip photograph of 8-way power combining PA. The chip size is 1.86mmx1.52mm (2.83mm^2).

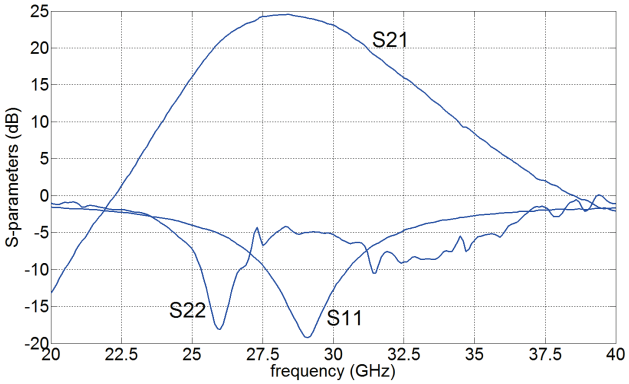

Fig. 6. Measured S_{11}, S_{22} and S_{21}. The peak S_{21} is 24.5dB at 28.3GHz.

conventional k-factor method would not be sufficient to ensure stability.

III. Measurement Results

The PA is implemented in a 0.25um SiGe:C BiCMOS technology with a peak f_t/f_{max} of 216/177 GHz. The chip photograph of the realized PA with a die size of 1860x1520µm is shown in Fig. 5.

A. Small-signal Measurements

On-wafer small signal measurements are carried out using a 67GHz Agilent PNA-X and Cascade Microtech probes. Fig. 6 shows the results in which a maximum gain of 24.5dB can be observed at 28.3GHz. The results reveal a 3dB-bandwidth of 3.8GHz (from 26.5 to 30.3 GHz) and the S_{11} is below -10dB from 27.7GHz to 30.5GHz. Considering S_{22}, a mismatch was observed compared with simulation results, possibly caused by modeling inaccuracies.

B. Large-signal Measurements

Large-signal measurements are performed using an Agilent NVNA which results in accurate fully calibrated measurement results. The measured saturated output power, gain, collector efficiency and PAE versus frequency are shown in Fig. 7 at an output stage's supply voltage (V_{CC}) of 5.5V and driver's supply voltage (V_{Cdrv}) of 4V. The output stage (AS2) its CE base bias voltage ($Vb1_{AS2}$, see Fig. 2) is set to 0.7V, which

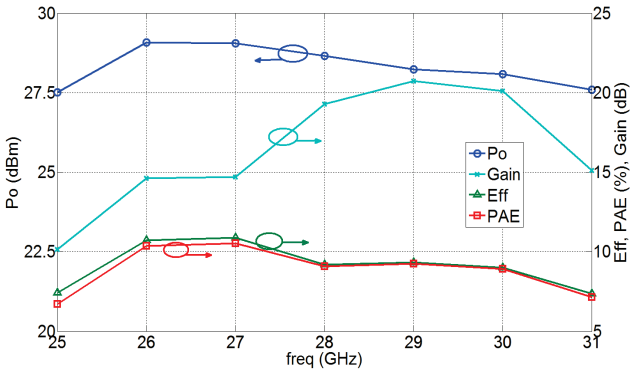

Fig. 7. Measured saturated output power, gain, collector efficiency and PAE versus frequency at V_{CC}=5.5V, $Vb1_{AS2}$=0.7V and Z_L=50Ω.

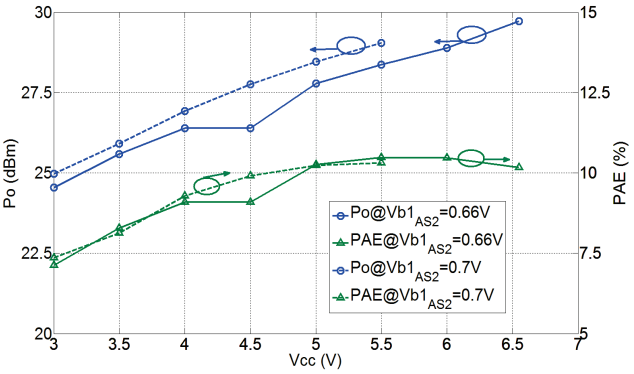

Fig. 8. Measured saturated output power and PAE versus supply voltage V_{CC} at 27GHz for $Vb1_{AS2}$ is 0.7V and 0.66V and at Z_L=50Ω.

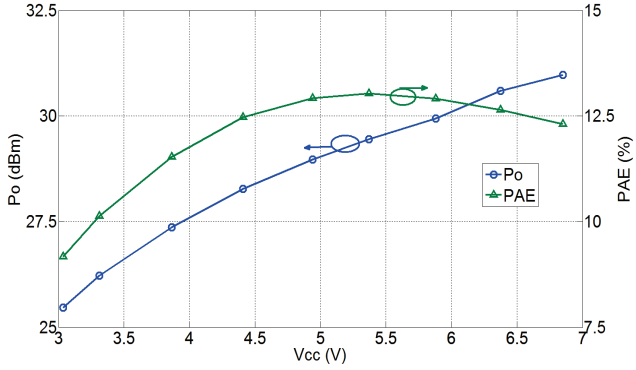

Fig. 9 Measured saturated output power and PAE versus supply voltage V_{CC} at 27GHz for $Vb1_{AS2}$ is 0.7V and at Z_L=21.2-j18Ω.

corresponds with class AB operation. The CB base bias voltage ($Vb2_{AS2}$) is set to 1.4V to optimize PAE. At 27GHz, the PA achieves a maximum saturated output power of 29.1dBm with a PAE of 10.3% and a collector efficiency of 10.7%. The saturated gain is 14.7dB and the output power 1dB bandwidth is about 4GHz, from above 25GHz to 30GHz, and corresponds with a 14.2% fractional bandwidth.

Table I
Comparison with (near) mm-wave silicon PAs with $P_{sat} \geq 23$dBm

	[1]	[2]	[7]	[2]	[8]	[9]	**This work**	**This work***
Technology	0.13um BiCMOS	45nm SOI CMOS	45nm SOI CMOS	45nm SOI CMOS	0.13um BiCMOS	0.20um BiCMOS	**0.25um BiCMOS**	**0.25um BiCMOS**
Topology	16-way in-phase current combiner	8-way lumped λ/4 combiner	4-stacked 2-bit DAC	λ/4 load modulated switched PA	4-way transformer combiner	4-way transformer combiner	**8-way in-phase current combiner**	**8-way in-phase current combiner**
freq. (GHz)	42	37	45	45	60	22	**27**	**27**
Supply (V)	4 / 2.4	4.8	5.1	2.4 / 2.6	4	1.8	**4 / 6.6**	**4 / 6.9**
$P_{sat,max}$ (dBm)	28.4	27.3	24.3	23.4	23	23	**29.7**	**31.0**
PAE_{max} (%)	10	10.7	14.6	6.7	6.3	19.7	**10.5**	**13**
$Gain_{max}$ (dB)	18.5	19.4	18	11.9	20	20	**20.2**	**20.7**
Area (mm^2)	5.55	4.16	0.77	4.16	3.42	6	**2.83**	**2.83**

*at load impedance Z_L=21.2-j18Ω

The measured saturated output power and PAE versus supply voltage V_{CC} are shown in Fig. 8 at a frequency of 27GHz for a base bias voltage $Vb1_{AS2}$ of both 0.7V and 0.66V. The reduction in bias voltage from 0.7V to 0.66V extends the maximum allowable supply voltage before breakdown as it reduces the current conduction angle and hence DC-current consumption. This extends the large-signal SOA regarding electro-thermal breakdown. The driver's supply voltage V_{Cdrv} is set fixed to 4V. At $Vb1_{AS1}$ is 0.66V and a supply voltage of 6.55V, the PA achieves a maximum saturated output power of 29.7dBm with a PAE of 10.2%. This extends the maximum saturated output power with 0.6dB compared with $Vb1_{AS2}$ set to 0.7V.

Due to the mentioned output mismatch (S_{22}), the output stages were not terminated in their optimum load impedance. Therefore load-pull was applied, which resulted in an optimum load impedance of 21.2-j18Ω instead of 50Ω. At this optimum impedance, the measured saturated output power and PAE versus supply voltage V_{CC} are shown in Fig. 9 at a frequency of 27GHz at $Vb1_{AS2}$ is 0.7V. The PA achieves a maximum saturated output power of 31dBm with a PAE of 13% at a V_{CC} of 6.9V. An additional off-chip matching network is still required to match to 50Ω.

Table I summarizes and compares the performance of (near) mm-wave silicon PAs with a saturated power of 23dBm and larger. The proposed PA delivers 1.3dB more saturated output power compared to [1] and has therefore the highest reported output power in the (near) mm-wave regime. After applying Z_L=21.2-j18Ω, the PA delivers another 1.3dB more power. The achieved PAE and gain are comparable with the referenced works. The consumed area is only 2.83mm^2.

IV. Conclusions

This paper presented an 8-way in-phase current combining power amplifier for Ka-band applications, implemented in a 0.25um SiGe:C BiCMOS technology. It achieves a saturated output power of 29.7dBm at 27GHz, which is the highest reported output power for a PA operating in the (near) mm-wave regime. After applying load-pull, the PA output power increases further to a level of 31dBm.

Acknowledgment

The author would like to thank M. v.d. Heijden, J. Bergervoet, Q. Ma, C. Lu, Y. Pei and Y. Chen for helpful discussion, R. van Dommele for measurement support and Focus Microwaves for load-pull tuner support.

References

[1] Wei Tai; Carley, L.R.; Ricketts, D.S., "A 0.7W fully integrated 42GHz power amplifier with 10% PAE in 0.13µm SiGe BiCMOS," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International , vol., no., pp.142,143, 17-21 Feb. 2013.

[2] Bhat, R.; Chakrabarti, A.; Krishnaswamy, H., "Large-scale power-combining and linearization in watt-class mmWave CMOS power amplifiers," Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE , vol., no., pp.283,286, 2-4 June 2013.

[3] J. Andrews, J. Cressler, and M. Mitchell, "A High-Gain, Two-Stage, X-Band SiGe Power Amplifier," IEEE/MTT-S International Microwave Symposium, pp. 817–820, Jun. 2007.

[4] Vanhoucke, T.; Hurkx, G. A M, "Unified electro-thermal stability criterion for bipolar transistors," Bipolar/BiCMOS Circuits and Technology Meeting, 2005. Proceedings of the , vol., no., pp.37,40, 9-11 Oct. 2005.

[5] Bohsali, M.; Niknejad, A.M., "Current combining 60GHz CMOS power amplifiers," Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE , vol., no., pp.31,34, 7-9 June 2009.

[6] M.Ohtomo, "Stability Analysis and Numerical Simulation of Multidevice Amplifiers, " IEEE Transactions on MTT, June/July 1993, vol. 41, pp. 983-991.

[7] A. Balteanu, et al., "A 45GHz, 2b Power DAC with 24.3dBm Output Power, >14Vpp Differential Swing, and 22% Peak PAE in 45nm SOI CMOS," IEEE Radio Frequency Integrated Circuits Symp., pp. 319 – 322, June 2012.

[8] U. R. Pfeiffer and D. Goren, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology," IEEE T-MTT, vol. 55, no. 5, pp. 857 –865, May 2007.

[9] Cheung, T.S.D.; Long, J.R., "A 21-26-GHz SiGe bipolar power amplifier MMIC," Solid-State Circuits, IEEE Journal of , vol.40, no.12, pp.2583,2597, Dec. 2005