# Single-Ended CMOS Doherty Power Amplifier Using Current Boosting Technique

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***Abstract*—In this letter, an efficiency enhancement technique incorporating a gate-voltage boosting of a peaking power amplifier (PA) in a CMOS Doherty PA is presented. To compensate the current driving capability from the low dc bias point of the peaking cell, an auxiliary bias network consisting of an operational amplifier (OPA) is utilized to provide the corresponding gate voltage in accordance with an instantaneous output power level. To verify the superior performance of the proposed technique, a CMOS Doherty PA with a prototype OPA has been fabricated using a commercial 0.18 $\mu$m process. The experimental results show that the implemented PA has an overall efficiency of 43.6% and a gain of 27.2 dB at an average output power of 25.2 dBm for a 10 MHz 3G LTE signal with a 7.6 dB peak-to-average power ratio (PAPR). Under this situation, the spectral performance is −34.1 dBc.**

***Index Terms*—CMOS, Doherty amplifier, power added efficiency (PAE), power amplifier (PA).**

## I. Introduction

A CMOS PA has recently become an attractive area of interest even in a wider-band communication system with a higher peak-to-average ratio (PAPR), such as in third-generation long-term evolution (3G-LTE). Considering the mobility and high data rate in such a system, not only is the linear amplification of the transmitted signal important, an efficiency enhancement is also a critical factor for the PA design. To improve the efficiency, several solutions and architectures have been investigated and reported, such as envelope tracking (ET), envelope elimination reconstruction (EER), and Doherty architecture [1]. Among the various methods available, a Doherty amplifier is attractive owing to its simplicity. A Doherty PA consists of a carrier PA and a peaking PA. While the carrier PA is only responsible for amplifying the signal lower than given back-off power level, the peaking PA remains to be turned off for a high efficiency at the back-off region. As the input power increases, the peaking PA starts to be turned on, but the carrier PA is still operated in saturation mode owing to the load modulation, ensuring a high efficiency. According to [2], [3], when designing a Doherty PA, since the bias point of the peaking PA is inherently lower than that of the carrier PA, the current driving capability of the peaking PA is so low that the overall performance may be degraded. The previous solution to compensate this effect is the use of an asymmetric cell size [4] and uneven input power drive [5]. However, the former has a load mismatch issue due to different cell size whereas the later degrades the power gain. Instead of previous solutions, a simple method in which the bias point of the peaking cell is boosted, which provides the auxiliary gate voltage in accordance with an instantaneous input power level, was introduced in our previous work [2].

In this research, to adopt the proposed compensation for a CMOS PA for mobile applications, a CMOS Doherty PA incorporating a bias boosting circuit has been fabricated and characterized. The measured results reveal that the proposed PA delivers excellent efficiency with high linearity compatible to that of an ET system.

## II. Compensation of Doherty Operation

Fig. 1 shows the simplified schematic of CMOS Doherty PA. The carrier and peaking PAs, which are featured as a cascode stage to mitigate the voltage stress, are connected using a 90° hybrid combiner. In a conventional PA, the bias networks for both PAs feed the fixed dc gate voltage of the common source stage, $V_{b1}$ and $V_{b2}$, respectively. Inferring that the efficiency at the back-off level is a critical value, $V_{b2}$ is chosen as lower level than $V_{b1}$. However, a previous analysis [2] revealed that the current through the peaking PA cannot reach the maximum value at the maximum output power owing to the lower driving capability, resulting in a severe degradation of the overall performance. Fig. 2 shows the simulated gain and power added efficiency (PAE) of a CMOS Doherty PA as a function of $V_{b2}$. For the simulation, a $4608\ \mu\mathrm{m}^2/6144\ \mu\mathrm{m}^2$ gate width of the power cell for both PAs is used, targeting a maximum output power of 31.5 dBm at 847 MHz at $\mathrm{Vcc} = 3.4$ V, as a result of the loadpull simulation. When applying $V_{b2} = 0$, the carrier PA delivers a maximum efficiency of 52.3% at a 6 dB back-off level. However, owing to the low current drive as a function of input power for $V_{b2} = 0$ V, as shown in Fig. 3, the large gain response encounters a nonlinear aspect such as an earlier compression. Thus, to prevent this effect, most of the design adopts a higher $V_{b2}$ by as much as 0.2 to 0.4 V, and it is expected that in this situation the efficiency at the required back-off level is thereby reduced by as much as ∼7% compared with the maximum achievable efficiency for $V_{b2} = 0$ V. Another solution is

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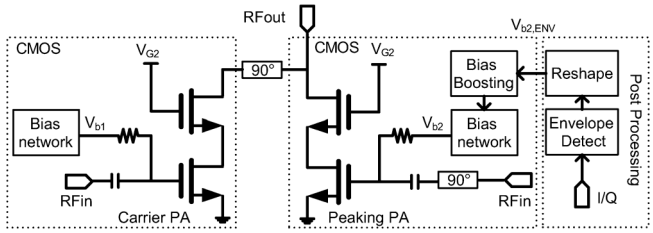


Fig. 1. Simplified schematic of proposed Doherty PA.

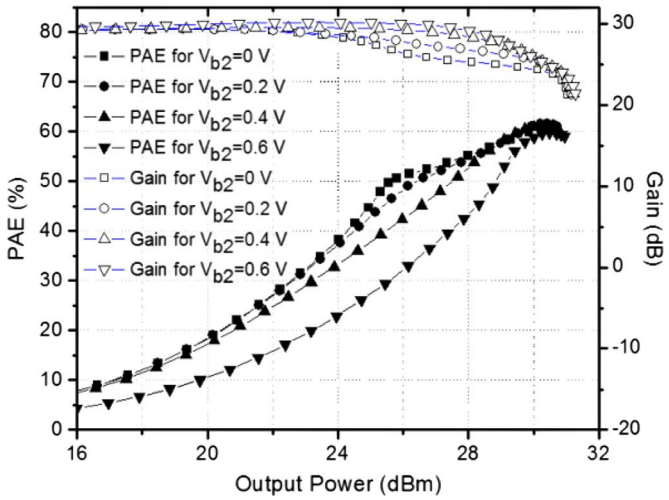


Fig. 2. Simulated gain and PAE versus the output power by sweeping the bias point of the peaking PA, $V_{b2}$.

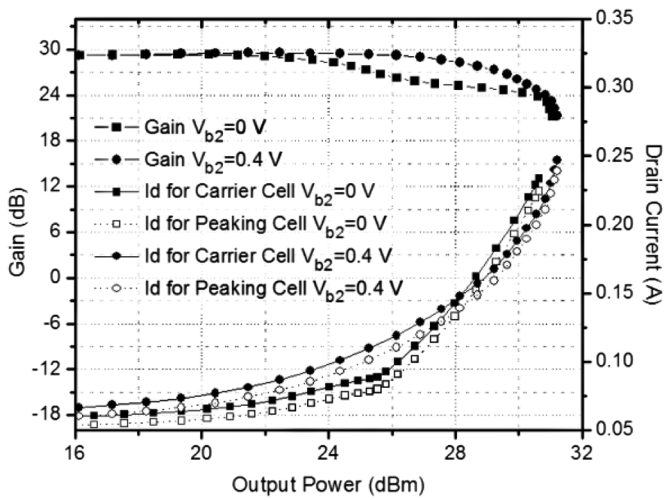


Fig. 3. Gain and current versus the output power for $V_{b2}$ of 0 and 0.4 V.

either to use around 2-times large cell size for peaking cell than carrier cell or to use uneven driving. However, both solutions have inherent drawback when implementing.

To prevent a degradation of the efficiency in this respect, the additional bias boosting circuit using an operational amplifier (OPA) in terms of the instantaneous power level is herein introduced, as shown Fig. 1. When smaller than the back-off region, the peaking PA is absolutely turned off by $V_{b2} = 0$ V. As the input power increases beyond the back-off level, the OPA provides a reshaped envelope voltage normalized by the transfer function of $V_{b2}$. At the saturated output power region, 0.65 V is applied for $V_{b2}$ to extend the gain compression region. It was noted that, since the efficiency in such a maximum region tracks

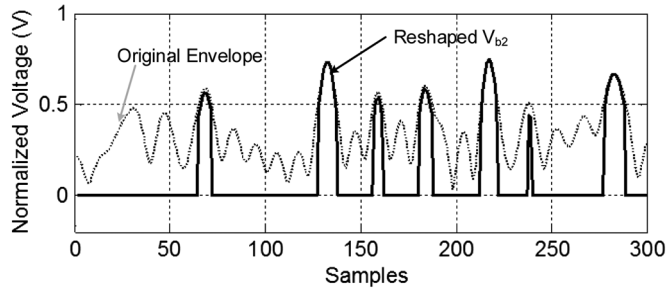


Fig. 4. Reshaped gate voltage of peaking PA $V_{b2}$.

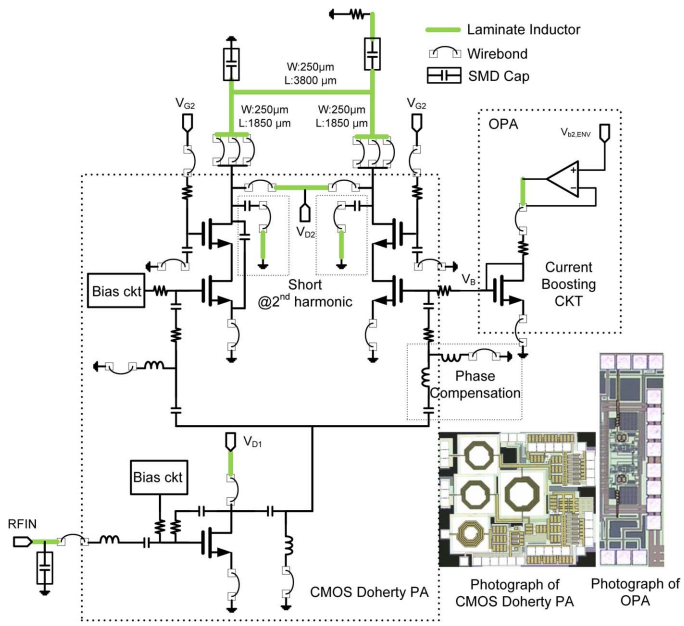


Fig. 5. Proposed Doherty CMOS PA.

the curve for $V_{b2} = 0.65$ V, it is slightly decreased by as much as 1.4%. However, considering the probability function of the given signal, the decrease in the efficiency in this region does not have an impact on the overall efficiency. To model $V_{b2}$ as a function of a normalized input envelope, the transfer function is extracted, as given by

$$V_{b2} = \begin{cases} 0; & 0 \le x \le x_{BO} \\ a \cdot \log(b \cdot x) + c; & x_{BO} < x \le 1 \end{cases} \quad (1)$$

where $x$ and $x_{BO}$ are a normalized input envelope and back-off envelope. In our work, to achieve a high efficiency while maintaining a high linearity, modeling parameters $a$, $b$, and $c$ of 1.15, 0.95, and 0.57 are used, respectively. The transferring $V_{b2}$ is shown in Fig. 4. Using this method, the simulation revealed that the efficiency is improved by as much as 4 and 10%, and the gain response is extended by as much as 0.35 and 0.8 dB, for a fixed $V_{b2}$ of 0.2 and 0.4 V, respectively, which is regarded as a conventional case.

Fig. 5 shows a detailed schematic of the proposed Doherty PA. For a Doherty PA with high efficiency, a class-F load configuration is used by shorting the second harmonic component. To minimize the source degeneration, 5-wirebondings are used as ground connection for each cell. The input phase compensation circuit is integrated, and a shunt inductance along with a wire bond is used for a fine phase adjustment. The output network of

TABLE I
PERFORMANCE COMPARISON

| Ref. | Tech. | Freq. (GHz) | Applic. | Psat (dbm) | Pavg (dBm) | PAE@Psat (%) | PAE@Pavg (%) | ACLR (dBc) | EVM | Output matching | PA type |
|---|---|---|---|---|---|---|---|---|---|---|---|
| [6] | 90nm | 0.93 | 10 MHz LTE | 29.4 | 26 | 25.8 | 17 | -33.4 | - | On-chip | Single |
| [7] | 0.18um | 1.95 | WCDMA | LPM:20.2 HPM:30.5 | LPM:16.4 HPM:28 | LPM:33.9 HPM:42.1 | LPM:27.4 HPM:36.4 | -35 | - | On-chip | Single |
| [8] | 0.18um | 1.85 | 10MHz 3G LTE | 30.2 | 26 | 48 | 34.1 | -34.2 | 2.8 % | Off-chip | ET(4.5V) |
| This Work | 0.18μm | 0.847 | 10MHz 3G LTE | 31.2 | 25.2 | 57.8 | 43.6 | -34.1 | 3.9% | On/Off-chip | Doherty |

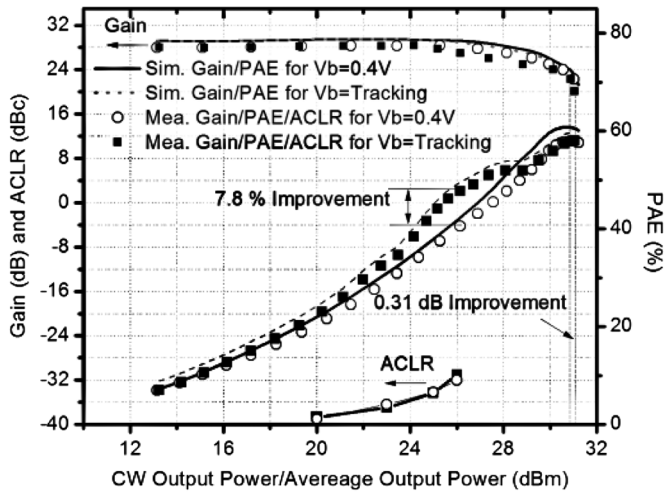


Fig. 6. Measured PAE and gain versus the output power.

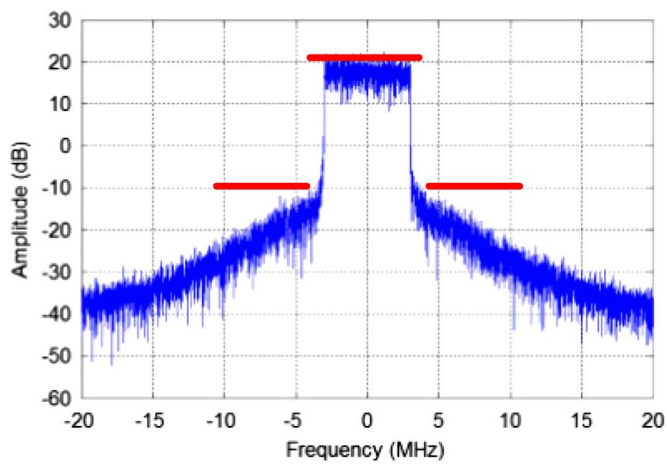


Fig. 7. Measured spectra density at an output power of 25.2 dBm.

90° is achieved using two shunt caps (first cap, fabricated MIM; and second cap, SMT cap for tuning) and trace amount of an FR4 laminate inductor. The fabricated Doherty PA and a prototype OPA are shown in Fig. 6. Fig. 7 shows the measured gain and PAE along with the simulation results. Owing to a slight discrepancy between the simulation and measurement results, the gate node voltage $V_{b2}$ is from 0 to 0.57 V for the proposed method. For a comparison with the results of a fixed bias point, a $V_{b2}$ of 0.38 V is selected. While a Doherty PA with a fixed bias delivers a PAE of 36.7%, an amplifier with a boosting gate voltage provides a PAE of 44.5%, which is 7.8% higher than that of a conventional case. Although the PAE of the proposed PA at the saturated output power region is observed to be up to 1.2% lower owing to the higher gate voltage injection, the measured saturated power is extended by as much as 0.31 dB compared with that of a conventional case. The proposed PA delivers an overall measured efficiency of 43.6% at the average output power of 25.2 dBm using a 10 MHz 3G LTE with a 7.6 dB PAPR signal, which is 7.6% higher than that of a conventional case. To verify the suitable linearity for base station applications, the spectral characteristic was measured, as shown in Fig. 8. The adjacent channel leakage power ratio (ACLR) is below −34 dBc as shown Fig. 6. The performance of the proposed CMOS Doherty amplifier is summarized in Table I, and compared with previous works [6]–[8].

## III. CONCLUSION

An effective compensation technique to enhance the efficiency at the back-off level along with a high linearity was introduced for the design of a CMOS Doherty PA. The proposed gate voltage circuit with a reshaped envelope voltage for a peaking PA not only provides sufficient current driving capability, but also makes the peaking PA able to be optimized at the back-off level of interest to achieve the maximum efficiency in such region. The proposed method was verified using a fabricated CMOS Doherty PA through a 0.18 $\mu$m process. The PA delivers an overall measured efficiency of 43.6% at an average output power of 25.2 dBm using a 10 MHz 3G LTE with a 7.6 dB PAPR signal.

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