Tournament-Shaped Magnetically Coupled Power-Combiner Architecture for RF CMOS Power Amplifier

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***Abstract*—A tournament-shaped magnetically coupled power-combiner architecture for a fully integrated RF CMOS power amplifier is proposed. Various 1 : 1 transmission line transformers are used to design the power combiner. To demonstrate the new architecture, a 1.81-GHz CMOS power amplifier using the tournament-shaped power combiner was implemented with a 0.18-μm RF CMOS process. All of the matching components, including the input and output transformer, were fully integrated. The amplifier achieved a drain efficiency of 38% at the maximum output power of 31.7 dBm.**

***Index Terms*—CMOS, differential, impedance transformation, load impedance, power amplifier, power combiner, transformer, transmission line.**

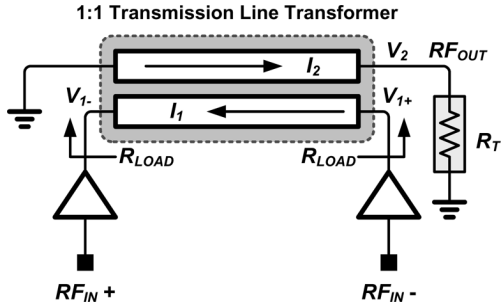

Fig. 1. Operation of a 1 : 1 transmission line transformer.

I. Introduction

A CMOS is the most popular device for a monolithic microwave integrated circuit (MMIC). Most analog circuits, including digital circuits and RF circuits, are designed using the CMOS process. The system-on-a-chip (SoC) techniques have developed very rapidly. However, power amplifiers and millimeter-wave circuits are fabricated using compound semiconductors on account of the losses related to the silicon substrate. Thus, few studies have focused on CMOS power amplifiers. Although CMOS power amplifiers are expected to be cheaper than GaAs HBT power amplifiers and easier to integrate with other circuits, they are not considered to be useful RF power amplifiers with watt-level output powers. Recently, the potential of a CMOS power amplifier was successfully demonstrated using a distributed active transformer [1]–[3]. The distributed active transformer is considered to have the potential to improve the performance of a CMOS power amplifier. In previous studies [1]–[3], a transformer that combines power serially is used. The distributed active transformer has several advantages for use in CMOS power amplifiers, including a boost of the impedance level and a reduction of circuit loss on the conductive silicon substrate [4].

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However, a power amplifier that utilizes a distributed active transformer may experience problems. The first of these is with the distributed active transformer to feed-line coupling. The coupling can eradicate both amplifier stability and asymmetry in the differential input [4]. Additionally, the gate directions of the power transistors must be different in a power amplifier using a distributed active transformer. However, to reduce the asymmetry in this situation, all of the gate directions of the power transistor must be alike. In this study, both the feed-line isolation from the magnetic coupling and the difference in the gate direction of the power transistor are removed using the proposed tournament-shaped transformer, and the benefits of its use are maintained.

In Section II, a conventional output-matching network, the distributed active transformer, and the problems with these methods are explained briefly. In Section III, the tournament-shaped transformer is introduced and its advantages are presented. Section IV outlines the design of a power amplifier using the proposed transformer. Finally, the measurements of the amplifier are given.

II. Transmission Line Transformer

A. 1 : 1 Transmission Line Transformer

A conventional balun can be implemented with a 1 : 1 transmission line transformer. Various transmission line transformers have been the subject of intense study [5]–[7]. Fig. 1 shows the basic operation of the 1 : 1 transmission line transformer. If the amplifier uses a differential structure, the voltages V_{1+} and V_{1-} are assumed as

$$V_{1-} = -V \text{ and } V_{1+} = V. \tag{1}$$

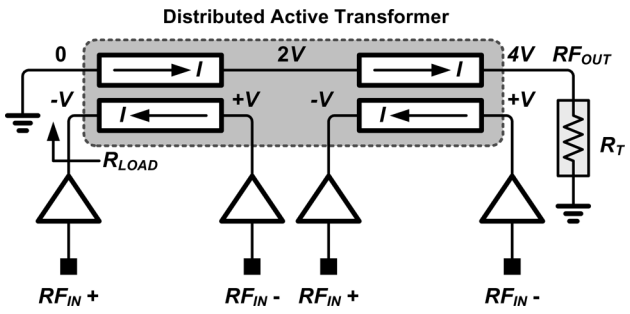

Fig. 2. Simplified distributed active transformer.

With the assumptions of an ideal transformer with perfect magnetic coupling, V_2 and I_2 can be estimated. I_1 is the current through the primary part of the transformer. From basic transmission-line transformer theory [8]–[10], the odd-mode current I_2 flows in the opposite direction in the secondary part of the transformer. As the magnitude of I_2 is identical to that of I_1, the relationship between I_1 and I_2 can be described as

$$I_1 = I_2 = I. \tag{2}$$

The voltage at the output node is assumed to be V_2. At the end of the left side, the voltage difference between the primary and secondary parts is

$$V_{1-} - 0 = -V. \tag{3}$$

This is the same voltage difference as at the end of the right side. Consequently,

$$\begin{aligned} -V = V_{1+} - V_2 &= V - V_2 \\ V_2 &= 2V. \end{aligned} \tag{4}$$

If $R_T = |V_2/I_2|$, then

$$\begin{aligned} R_T &= \left|\frac{V_2}{I_2}\right| = \frac{2V}{I} \\ R_{\mathrm{LOAD}} &= \left|\frac{V_{1+}}{I_1}\right| = \left|\frac{V_{1-}}{I_1}\right| = \frac{V}{I} = 0.5R_T. \end{aligned} \tag{5}$$

Thus, the transformer of the circuit configuration steps down the impedance level by a factor of 2. If the parameter T is defined as the ideal impedance transformation ratio R_T/R_{LOAD}, the T of the transformer shown in Fig. 1 is 2. If the parameter N is defined as the number of power stages, N is 2 for the amplifier architecture shown in Fig. 1. The output power at the output terminal can then be calculated as

$$P_{\mathrm{OUT}} \propto (N \times T) \cdot \frac{V_{DD}^2}{R_T} \tag{6}$$

where the value $N \times T$ of the circuit configuration is 4.

A distributed active transformer uses several $1:1$ transformers by connecting the secondary parts in a series, as shown in Fig. 2.

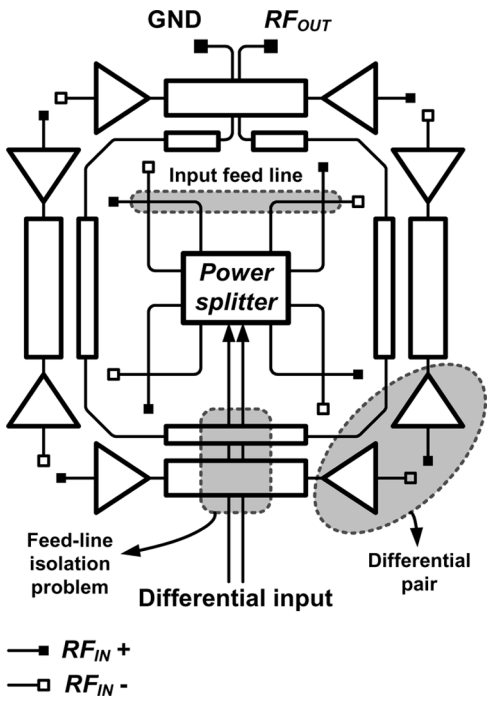

Fig. 3. Representative drawing of a complete distributed active transformer.

B. Distributed Active Transformer

A distributed active transformer uses a $1:1$ transmission line transformer to combine powers. The simplified architecture of the distributed active transformer is shown in Fig. 2. In this arrangement, the ac voltages on the secondary parts are added, while the primary part is driven by the low voltage of separate active devices. However, the current of the secondary part is identical to that of the primary part if the transformer is assumed as ideal. R_{LOAD} can then be calculated as

$$\begin{aligned} R_T &= \frac{4V}{I} \\ R_{\mathrm{LOAD}} &= \frac{V}{I} = 0.25R_T. \end{aligned} \tag{7}$$

As shown in (7), the value of T in the circuit configuration shown in Fig. 2 is 4. The number of power stages is four in this figure; thus, the value $N \times T$ in the circuit configuration is 16. Ideally, the output power is four times higher than that of the circuit configuration shown in Fig. 1. Thus, the distributed active transformer is one of the most efficient power-combining examples of architecture for an RF CMOS power amplifier with a watt-level output power.

Fig. 3 shows a representative drawing of a complete distributed active transformer with eight power stages. To make the virtual ground, circular architecture is used in this drawing. Due to the circular architecture, an input feed-line must be crossed with the transformer. This is one of the components of the transformer, as shown in Fig. 3. The isolation problem between the input feed-line and the distributed active transformer cannot be avoided. As explained in a previous study [4], a specific shielding technique is needed to prevent the feedback loop induced by the coupling between the input feed-line and transformer. The poor isolation characteristic

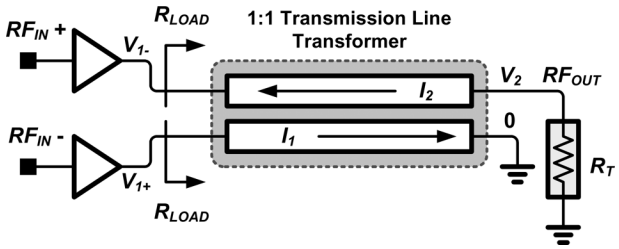

Fig. 4. Unit transmission line transformer of the tournament-shaped power combiner.

between the input feed-line and transformer may cause stability problems in the power amplifier. Additionally, the coupling may cause asymmetries in the push/pull input [4]. This can significantly degrade performance. An additional problem is in the gate direction of the differential pairs. As shown in Fig. 3, the gate directions of each power stage of the differential pairs are not the same. However, the gate directions of all of the transistors must be identical for immunity to the process variations. Additionally, with HBT or pseudomorphic HEMT (pHEMT) technology, the base or gate directions of all of the transistors must be identical, as some processes depend on the crystal orientation in compound semiconductors. Thus, it is difficult to design a circuit-type distributed active transformer. The tournament-shaped power-combiner architecture addresses these problems. It is proposed and analyzed in Section III.

III. Tournament-Shaped Power-Combiner Architecture

Fig. 4 shows the unit transmission line transformer for the tournament-shaped power combiner. The configurations are different from those shown in Fig. 1. A simplified analysis of the circuit shown in Fig. 4 is similar to that of the circuit shown in Fig. 1.

If the amplifier has a differential structure, the voltages V_{1+} and V_{1-} can be assumed as

$$V_{1+} = V \text{ and } V_{1-} = -V. \tag{8}$$

With the assumptions of an ideal transformer with perfect magnetic coupling, V_2 can be calculated. I_2 is the current through the upper part of the transformer, and I_1 is the current through the lower part of the transformer. Due to the differential operations of the power stage, the relationship of I_1 and I_2 is

$$I_1 = I_2 = I. \tag{9}$$

The voltage at the output node is assumed to be V_2. At the end of the left side, the voltage difference between the upper and lower parts is

$$V_{1-} - V_{1+} = (-V) - V = -2V. \tag{10}$$

This is the same voltage difference as at the end of the right side. Consequently,

$$\begin{aligned} -2V &= V_2 - 0 \\ V_2 &= -2V. \end{aligned} \tag{11}$$

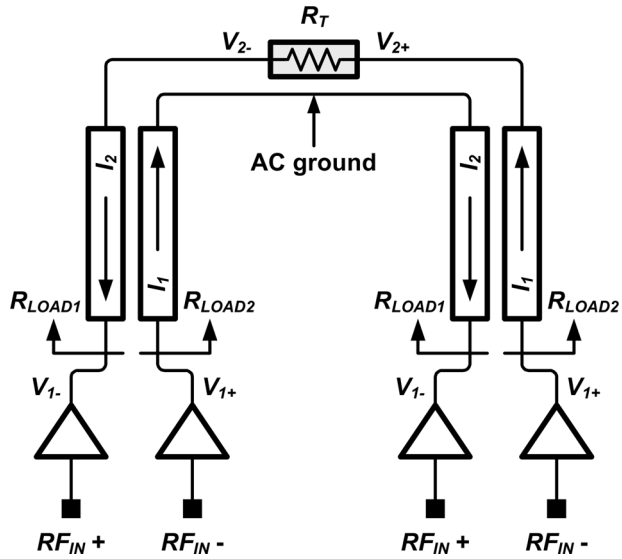

Fig. 5. Basic concept of the tournament-shaped power combiner.

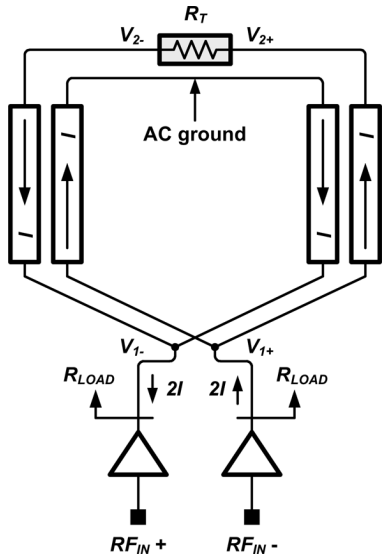

Fig. 6. Basic concept of the tournament-shaped power combiner with equalized load impedances of a differential pair. After [10].

If $R_T = |V_2/I_2|$, then

$$\begin{aligned} R_T &= \left|\frac{V_2}{I_2}\right| = \frac{2V}{I} \\ R_{\text{LOAD}} &= \left|\frac{V_1}{I_1}\right| = \frac{V}{I} = 0.5R_T. \end{aligned} \tag{12}$$

Thus, the transformer of the circuit steps down the impedance level by a factor of 2. The T of the circuit shown in Fig. 4 is 2. N is 2 for the amplifier architecture shown in Fig. 4. The value $N \times T$ of the circuit then becomes 4. Thus, the circuit using the $1:1$ transmission line transformer shown in Fig. 4 can be used as a unit cell for the power combiner. Using two unit transformers, the power-combiner architectures shown in Figs. 5 and 6 were designed [10]. Using the same analysis, the relationship among V_{1+}, V_{1-}, V_{2+}, and V_{2-} for the circuit shown in Fig. 5 can be calculated as

$$\begin{aligned} -V_{1-} &= V_{1+} = V \\ -V_{2-} &= V_{2+} = 2V. \end{aligned} \tag{13}$$

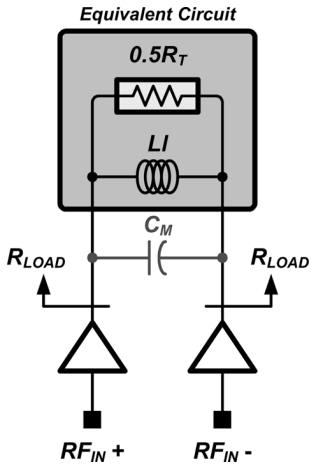

Fig. 7. Equivalent circuit of the circuit shown in Fig. 6.

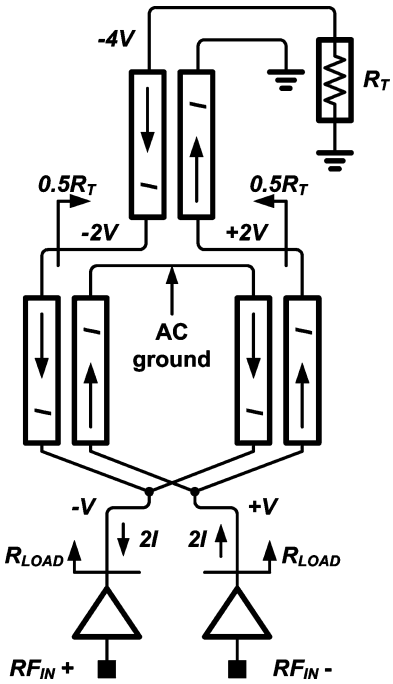

Fig. 8. Amplifier architecture using the tournament-shaped power combiner with a single-ended output port.

$R_{\mathrm{LOAD1}}, R_{\mathrm{LOAD2}}$ and R_T can then be calculated as

$$\frac{4V}{I} = R_T$$
$$\frac{V}{I} = R_{\mathrm{LOAD1}} = R_{\mathrm{LOAD2}} = 0.25R_T. \tag{14}$$

As both T and N at this point are 4, $N \times T$ is 16. Using the same calculations, T is 8 and N is 2 for the circuit shown in Fig. 6. Thus, $N \times T$ for the circuit in Fig. 6 is also 16. The ac ground of the circuit can be used as a point for the supply voltage. From the Appendix, the transformer and R_T can be represented by the equivalent circuit with an inductor and a resistor, as shown in Fig. 7. The inductance in the equivalent circuit can be resonated out with additional matching capacitor C_M.

Fig. 8 shows the circuit with a single-ended output. The 1 : 1 transmission line transformer is added to the circuit shown in Fig. 6, giving it the circuit shown in Fig. 8. If R_T is assumed to be 50 Ω, this 50 Ω is stepped down to 25 Ω by the upper 1 : 1 transformer of Fig. 8. Finally, R_{LOAD} is 6.25 Ω. Thus, T is 8 and N is 2. The $N \times T$ is, therefore, 16.

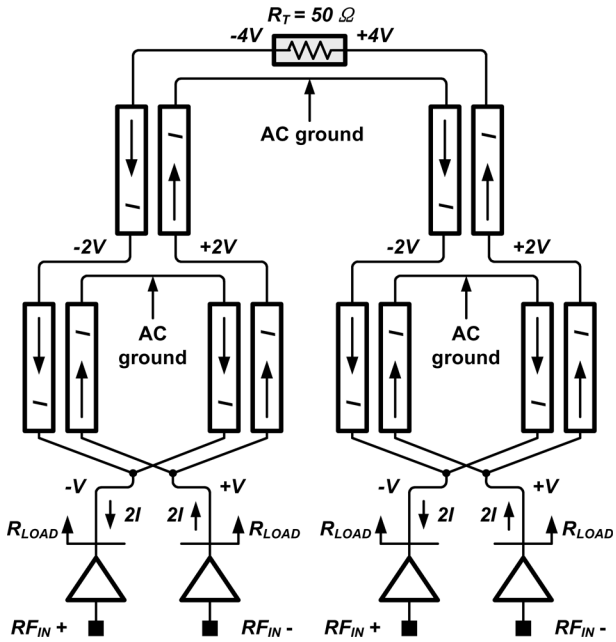

Fig. 9. Amplifier architecture using tournament-shaped power combiner.

Fig. 9 shows combined architecture of the two circuits shown in Fig. 8. If R_T is assumed to be 50 Ω, R_T is transformed to 12.5 Ω by the upper transformer. Next, 12.5 Ω is transformed to 3.125 Ω by the lower 1 : 1 transformers. In the circuit shown in Fig. 9, N is 4 and T is 16. $N \times T$ can be calculated as 64. Thus, the output power with the circuit shown in Fig. 9 is four times higher than the circuit shown in Fig. 8. The proposed tournament-shaped power-combiner functions as both the power combiner and impedance transformer.

In order to obtain a single-ended output power, the circuit shown in Fig. 9 must be modified. The single-ended power amplifiers are shown in Figs. 10 and 11. In the circuit shown in Fig. 10, an additional 1 : 1 transformer is used for the single-ended output. To combine the two circuits shown in Fig. 8, a voltage combining method is used. The ideal impedance transformation ratio T is 16 and N is 4. Thus, $N \times T$ is 64.

Fig. 11 shows an additional example of the power amplifier with the tournament-shaped power combiner. Unlike the circuit shown in Fig. 10, the circuit shown in Fig. 11 does not use an additional transformer for a single-ended output. To combine the two circuits shown in Fig. 8, a current-combining method is used. Thus, the ideal impedance transformation ratio T is different from that of the circuit shown in Fig. 10. For this circuit, N is 4 and T is 4. Thus, $N \times T$ is 16.

In summary, for this section, with additional metal–insulator–metal (MIM) capacitors, as shown in Fig. 7, the tournament-shaped power combiner can be used as power combiner and output-matching network. Various modifications could be possible in the tournament-shaped power combiner to get various values of $N \times T$, as summarized in Table I. Although the product $N \times T$ is used as a figure-of-merit to

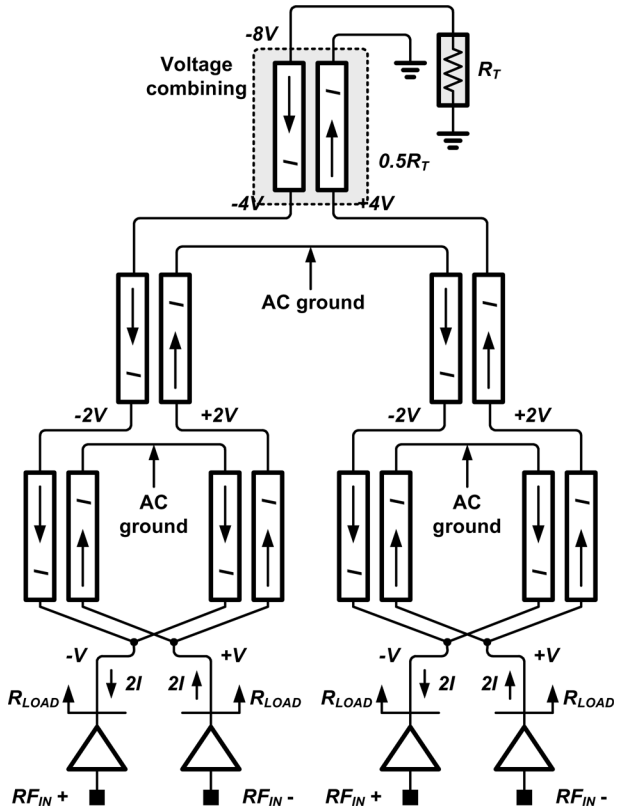

Fig. 10. Amplifier architecture using the tournament-shaped power combiner with a voltage-combining method.

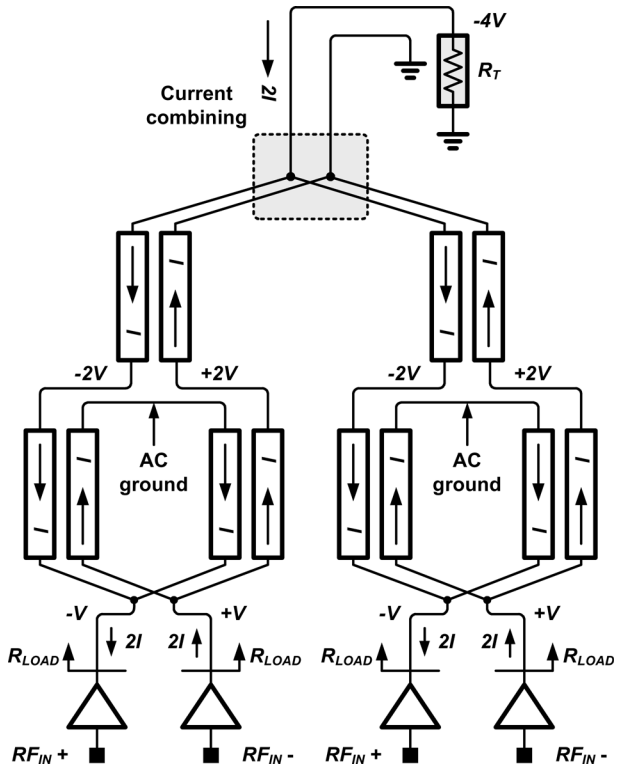

Fig. 11. Amplifier architecture using the tournament-shaped power combiner with the current-combining method.

compare different power-combining topologies, the factor of combining loss is omitted. If the number of used transmission line transformer is increased, the power-combining loss will be increased. There is no feed-line coupling problems because the feed-line does not need to be located near the output power combiner. Additionally, all of the gate direction of the power transistor can be the same.

TABLE I
IDEAL LOAD IMPEDANCES AND $N \times T$ OF VARIOUS CONFIGURATIONS OF THE TOURNAMENT-SHAPED POWER COMBINER

Configuration	R_{LOAD} [Ω]	$N \times T$
Figure 4	25	2 × 2 = 4
Figure 5	12.5	4 × 4 = 16
Figure 6	6.25	2 × 8 = 16
Figure 8	6.25	2 × 8 = 16
Figure 9	3.125	4 ×16 = 64
Figure 10	3.125	4 ×16 = 64
Figure 11	12.5	4 × 4 = 16

The R_T is assumed to be 50 Ω .

IV. DESIGN EXAMPLE OF A POWER AMPLIFIER WITH THE TOURNAMENT-SHAPED POWER COMBINER

A 1.81-GHz power amplifier using the tournament-shaped power combiner with a 0.18-μm RF CMOS process was designed. The tournament-shaped power combiner was used as both the output-matching network and the impedance transformer.

A. Design and Implementation

1) Driver Stage: A spiral transformer is used in the input of the driver stage to convert the single-ended input into a differential input signal. The input-matching network of the driver stage is completed with the input transformer and an additional MIM capacitor $C_{\rm IN}$. The driver stage was designed as class E for high efficiency. A cascode structure is adopted to remove the breakdown problems. The gate length of MD1 and MD2 is 0.18 and 0.35 μm, respectively.

2) Inter-Stage Matching Network: In a conventional inter-stage matching network, an inductor for the load of a driver stage, a dc-blocking capacitor, and an inductor to cancel out the gate–source parasitic capacitance $C_{\rm gs}$ of MP1 is needed. In this study, to reduce the size of the inter-stage matching network, a transformer is used instead of two inductors and a MIM capacitor, as shown in Fig. 12. To complete the inter-stage matching network, two additional MIM capacitors, i.e., $C_{\rm INTER}$ and $C_{P\_{\rm IN}}$, are used.

3) Power Stage: The tournament-shaped magnetically coupled power combiner shown in Fig. 11 was used as the output power combiner. The power stage was designed as class E for high efficiency. With additional MIM capacitors, i.e., $C_{P\_{\rm OUT}}, C_{\rm GND}$, and $C_{\rm OUT}$, the output-matching network is completed. The capacitors $C_{\rm GND}$ and $C_{\rm OUT}$ are utilized to remove the unbalanced signal in the power combiner. The parasitic inductance of the power combiner is used as the inductor for the class-E matching network. A cascode structure was adopted to remove the breakdown problems. The gate lengths of MP1 and MP2 are 0.18 and 0.35 μm, respectively. Fig. 13 shows the simulated drain voltage waveform of the differential power stage. The phase difference of the differential signal

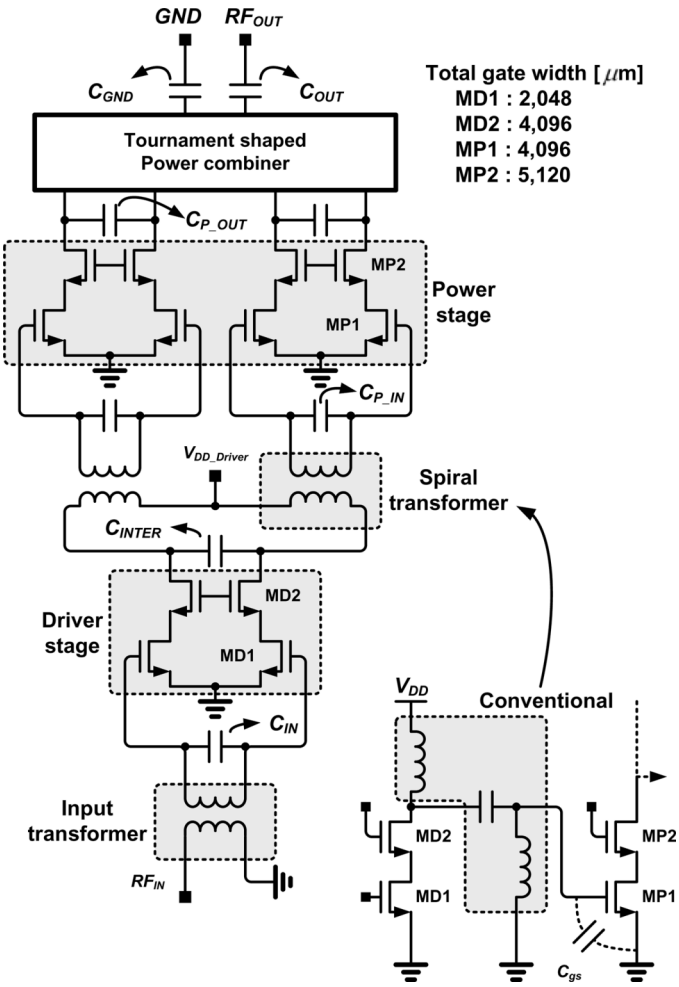

Fig. 12. Simplified schematic of the designed power amplifier.

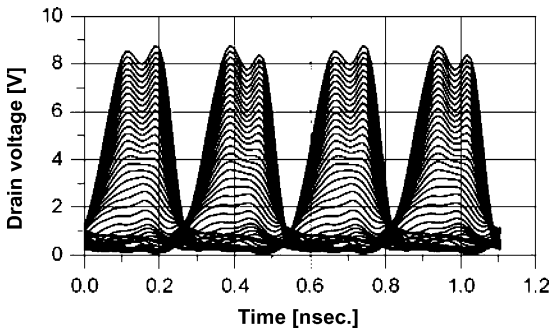

Fig. 13. Simulated drain voltage waveform of the differential power stage.

was almost 180°. The differential signal of the power stage is converted into a single-ended signal by the tournament-shaped magnetically coupled power combiner.

4) Tournament-Shaped Power Combiner: A 0.18-μm RF CMOS process was used to implement the power amplifier using the tournament-shaped magnetically coupled power combiner. The CMOS process has six metal layers. To design a low-loss power combiner, sixth and fifth metal layers were used, as shown in Fig. 14. The two metal layers are connected through a via. If a fourth metal layer is added, the silicon substrate loss of the power combiner is increased. The metal width

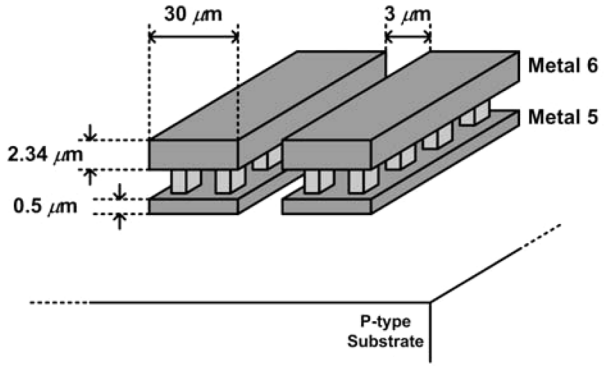

Fig. 14. Cross section of the transmission line transformer.

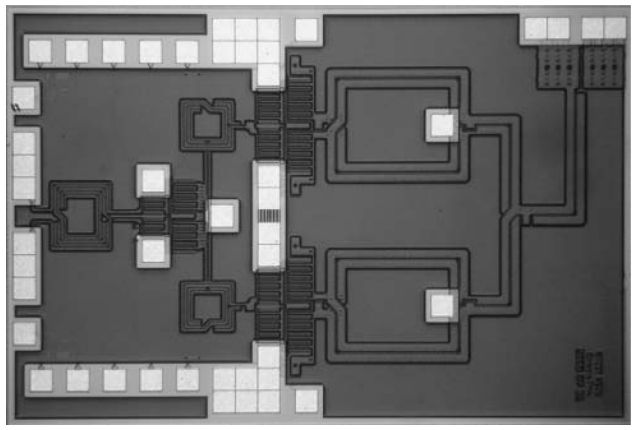

Fig. 15. Chip photograph of the implemented power amplifier.

of the transformer is 30 μm. The metal width is optimized between the parasitic resistance and silicon substrate loss. The space between the two parts of the transformer is 3 μm. The maximum available gain of the designed power combiner is simulated as approximately -1.17 dB. A 2.5-D electromagnetic (EM) simulator was used to design the power combiner.

A chip photograph is shown in Fig. 15. The chip size is 1.4×2.15 mm^2 including the test pads.

B. Measurement

The losses of the bond wire, input transformer, and printed circuit board interconnections are included in the amplifier's measured performance. Fig. 16 shows the measured drain efficiency of the power stage versus the output power $P_{\rm OUT}$, while the supply voltage of power stage varies from 0.5 to 3.3 V. In Fig. 16, the input power is fixed at 10 dBm and the operation frequency is 1.81 GHz. The amplifier achieved a drain efficiency of 38 % at a maximum output power of 31.7 dBm. The measured dynamic range was 15.1 dB for a supply voltage of the power stage from 0.5 to 3.3 V.

Fig. 17 shows the measured output power versus input power. In Fig. 17, the supply voltage and operating frequency are fixed at 3.3 V and 1.81 GHz, respectively.

Fig. 18 shows the measured output power versus the frequency with various supply voltages of the power stage. The flatness of the output power is 0.34 dB at worst for an operating frequency from 1.68 to 1.98 GHz.

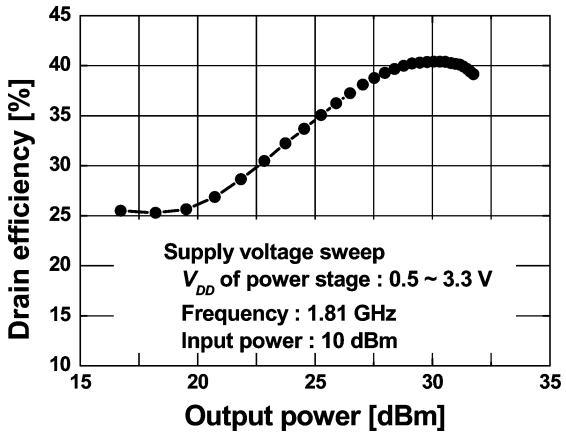

Fig. 16. Measured drain efficiency of power stage versus output power with fixed input power.

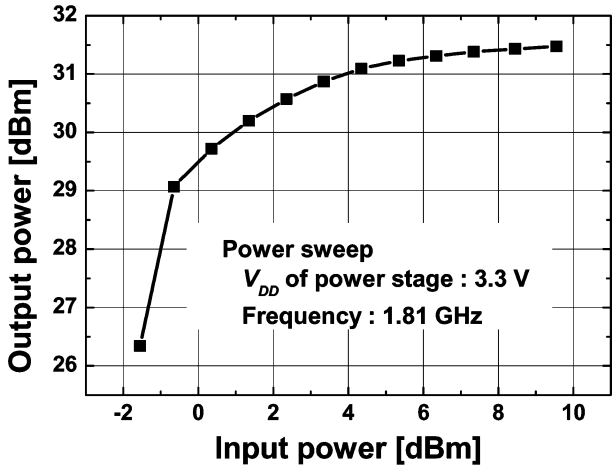

Fig. 17. Measured output power versus input power.

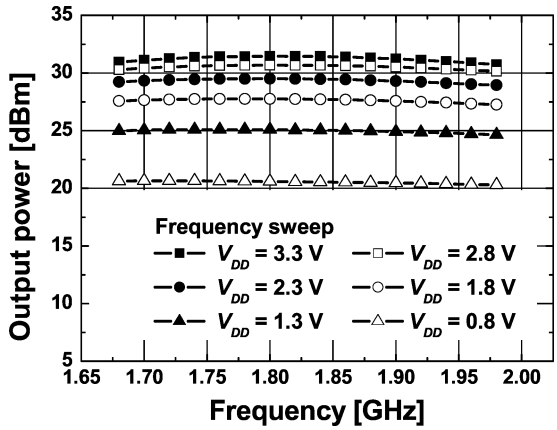

Fig. 18. Measured frequency response.

V. Discussion

As described above, the loss of the designed tournament-shaped power combiner is smaller than that of a previous study [3]. For the tournament-shaped power-combiner architecture, the power generated at the power stages is transferred to the output load directly through the transmission line with the dc-blocking capacitor C_{OUT}. The magnetic coupling between

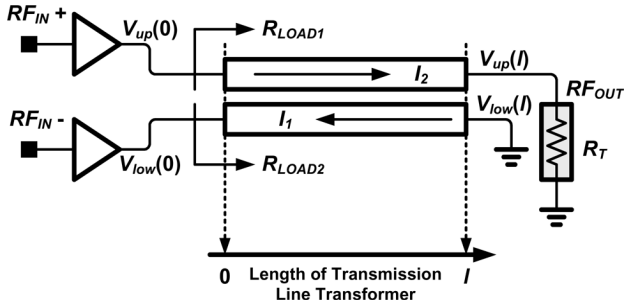

Fig. 19. Analysis of the unit-transmission line transformer of the tournament-shaped power combiner.

transmission lines of the transformer aids transformation of the load impedance in the tournament-shaped power combiner. The coupling factor of the transformer can be low since it doses not significantly influence the output power. However, for a distributed active transformer, the coupling factor directly affects the performance of the amplifier. For this reason, the loss of the tournament-shaped power combiner is smaller than that of the distributed active transformer.

However, the current tournament-shaped power combiner requires a large chip area. The isolation problems and the chip area problems have a tradeoff relationship. Thus, reducing the chip area of the tournament-shaped power combiner remains as further work.

The maximum output power and efficiency of this study are quite similar to those of the previous studies [3]. The gain of the previous study [3] is better than that of the proposed amplifier because the mode-locking technique is used in the former [3].

VI. Conclusion

A tournament-shaped power combiner for a fully integrated RF CMOS power amplifier has been proposed. The input feed-line coupling problems with the transmission line transformer have been solved. Various 1 : 1 transmission line transformers have been used to design the tournament-shaped power combiner. To demonstrate the new concept, a 1.81-GHz CMOS power amplifier using the tournament-shaped power combiner was implemented with a 0.18-μm RF CMOS process. All of the matching components, including the input and output transformer, were fully integrated. The amplifier achieved a drain efficiency of 38 % at a maximum output power of 31.7 dBm.

Appendix
Analysis of the Tournament-Shaped Power Combiner Using Transmission Line Theory

From transmission line theory [11], the transformer shown in Fig. 19 can be analyzed. The input impedances R_{LOAD1} and R_{LOAD2} of the transformer can be determined using the following boundary conditions:

$$V_{\mathrm{up}}(l) = R_T \cdot I_2(l) \tag{A.1}$$

$$V_{\mathrm{low}}(l) = 0 \tag{A.2}$$

$$V_{\mathrm{up}}(0) = -V_{\mathrm{low}}(0). \tag{A.3}$$

By using (A.1), the unbalanced current (I_0) can be calculated by

$$\begin{aligned} I_2(l) &= I_1(l) + I_0(l) \\ Z_0 &= \sqrt{\frac{2L}{C}}, \\ \Gamma &= \sqrt{2LC} \cdot s = j\omega \cdot \sqrt{2LC} \\ I_0/2 &= Ae^{-\Gamma l}[1 - Z_0/R_T] + Be^{\Gamma l}[1 + Z_0/R_T] \end{aligned} \tag{A.4}$$

where L is the inductance and C is the capacitance per unit length. When (A.2) and (A.3) are used, the second equation necessary for determining the ratio B/A is

$$sLlI_0/2 = (Z_0/2) \cdot [Ae^{-\Gamma l} - Be^{\Gamma l}]. \tag{A.5}$$

The ratio B/A can be obtained using (A.4) and (A.5) as follows:

$$\frac{B}{A} = -\frac{e^{-\Gamma l}[1 - Z_0/R_T - Z_0/(2sLl)]}{e^{\Gamma l}[1 + Z_0/R_T - Z_0/(2sLl)]}. \tag{A.6}$$

When B/A is known, the input impedances R_{LOAD1} and R_{LOAD2} can be determined [11]. These impedances are given by the equations

$$R_{\mathrm{LOAD1}} = \frac{Z_0[1 - B/A]}{-[Z_0/(sLl)][e^{-\Gamma l} - (B/A)e^{\Gamma l}] + 2[1 + B/A]} \tag{A.7}$$

$$R_{\mathrm{LOAD2}} = \frac{Z_0[1 - B/A]}{+[Z_0/(sLl)][e^{-\Gamma l} - (B/A)e^{\Gamma l}] + 2[1 + B/A]}. \tag{A.8}$$

It is clear from the different signs in the denominators of (A.7) and (A.8) that the two load impedances are not equal at low frequencies [11]. Thus, the circuits of Figs. 4, 8, 10, and 11 are more suitable for millimeter-wave circuits. If the approximation

$$e^{\pm\Gamma l} \cong 1 \tag{A.9}$$

is used, (A.5) and (A.6) simplify to

$$\frac{B}{A} = -\frac{-2sLlR_T + 2sLZ_0 + Z_0R_T}{2sLlR_T + 2sLZ_0 + Z_0R_T} \tag{A.10}$$

$$R_{\mathrm{LOAD1}} = \frac{R_T}{2} \tag{A.11}$$

$$R_{\mathrm{LOAD2}} = \frac{1}{2} \cdot \left(\frac{sLlR_T}{sLl + R_T} \right). \tag{A.12}$$

The circuit of Fig. 19 is used as unit transmission line transformer for the tournament-shaped power combiner. Using two unit transformers, the power-combiner architectures shown in Figs. 5 and 6 were designed.

R_{LOAD} of Fig. 6 can be calculated using R_{LOAD1} and R_{LOAD2} of Fig. 19 as

$$R_{\mathrm{LOAD}} = R_{\mathrm{LOAD1}} // R_{\mathrm{LOAD2}} = \frac{sLlR_T}{2 \cdot (2sLl + R_T)}. \tag{A.13}$$

From (A.13), the equivalent circuit of the transformer and terminal impedance can be simplified with an inductor and a resistor, as shown in Fig. 7. The inductance of the equivalent circuit can be resonated out with an additional matching capacitor C_M. The ac ground of the circuit shown in Fig. 7 can be used as pad for the supply voltage.

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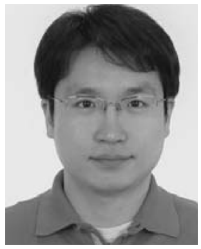

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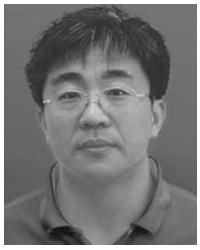

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