Dual-Mode CMOS Power Amplifier Based on Load-Impedance Modulation

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***Abstract*— This letter presents a dual-mode CMOS power amplifier (PA) that has an improved efficiency using load-impedance modulation in the low-power mode (LPM) and a fully differential operation in the high-power mode (HPM). For the LPM, the transistor in the negative path of the differential pair is turned ON, as a switch, to appropriately modulate the load impedance for the transistor in the positive path using the output balun. An external switch is deployed to turn V_{DD} OFF for the negative path. In order to verify the proposed concept, a dual-mode CMOS PA IC was designed using a bulk CMOS process and an off-chip output balun, and it was evaluated using the 920-MHz narrow-band Internet of Things signal with a bandwidth of 200 kHz and a peak-to-average power ratio of 5.7 dB. For the HPM, the implemented PA exhibited a gain of 24.1 dB, a power-added efficiency (PAE) of 44.3%, and an adjacent channel leakage power ratio (ACLR) of −33.9 dBc at an average output power of 27.7 dBm. For the LPM, a gain of 19.3 dB, a PAE of 37.7%, and an ACLR of −34.9 dBc were obtained at an average output power of 21.7 dBm.**

***Index Terms*— Balun, CMOS power amplifier (PA), dual-mode PA, load-impedance modulation, narrow-band Internet of Things (NB-IoT).**

I. Introduction

MODERN wireless communication standards utilize complex modulation schemes that have high peak-to-average power ratios (PAPRs) in order to achieve high data rates. The power amplifier (PA) must operate in the large output power back-off region for high linearity, and this results in a degradation in efficiency.

Recently, transformer-based Doherty PAs have been reported with improved efficiency in the back-off region [1]–[6]. The partial load-impedance modulation for the low-power level was realized using a transformer for a double-balanced structure [1], [2]. The secondary turn for the auxiliary amplifier blocks the full load-impedance modulation for the main amplifier.

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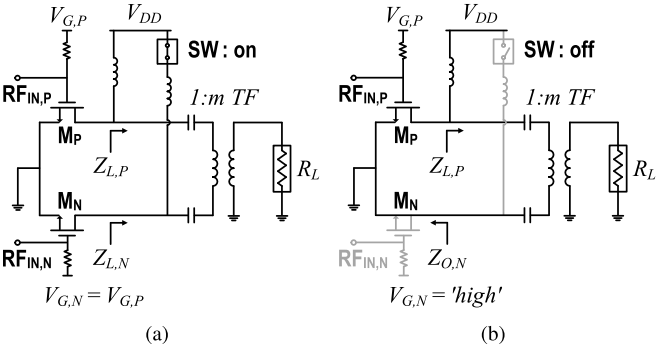


Fig. 1. Operational diagram of the proposed dual-mode PA. (a) HPM. (b) LPM.

A transformer-based voltage-combined Doherty PA was proposed, which used an additional $\lambda/4$ transmission line at the output of the peaking amplifier [3]. However, due to the $\lambda/4$ transmission line, the PA does not have a differential operation. A transformer-based dual-mode PA was proposed using an additional switch to connect a ground to the output of the peaking amplifier in the low-power mode (LPM) for load-impedance modulation [5]. However, the switch has a parasitic capacitance in the OFF-state, and this can cause a mismatch for the differential operation in the high-power mode (HPM).

In this letter, we propose a CMOS dual-mode PA that has a load impedance modulation using an output transformer for the LPM and a full differential operation for the HPM. For the LPM, the transistor in the negative path of the differential pair was completely turned ON to connect a ground to the transformer. An external switch is required to turn the V_{DD} OFF for the transistor in the negative path when it is turned ON. The proposed dual-mode PA was implemented using a 55-nm CMOS process, and this was experimentally verified using a 920-MHz narrow-band Internet of Things (NB-IoT) signal.

II. Design and Simulation Results

Fig. 1 shows the operational diagram of the output network for the proposed dual-mode PA. For the HPM, the proposed PA is just a differential amplifier, in which both transistors in the positive and negative paths work without any imbalance.

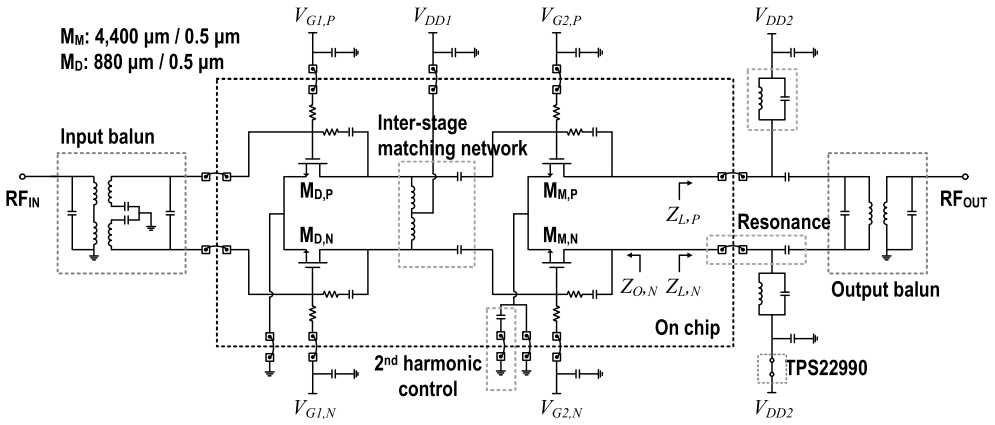


Fig. 2. Schematic of the proposed CMOS two-stage dual-mode PA.

When the power level goes lower than the power threshold for mode switching (i.e., for the LPM), the transistor in the negative path is turned ON, as a switch, and the external power switch is turned OFF to stop supplying V_{DD} to the negative paths. The PA has a single-ended operation only using the transistor in the positive path.

The lower end of the transformer's primary turn is connected to ground; therefore, the load impedance, $Z_{L,P}$, for the LPM of the transistor in the positive path is modulated [3]

$$Z_{L,P} = \begin{cases} \dfrac{R_{\mathrm{L}}}{m^2} \text{ (at LPM)} \\ \dfrac{R_{\mathrm{L}}}{2 \cdot m^2} \text{ (at HPM)} \end{cases} \tag{1}$$

where R_{L} is a load resistance, generally 50 Ω, and m is a ratio of the secondary turn to the primary turn. As shown from (1), $Z_{L,P}$ for the LPM becomes two times larger than that for the HPM, in order to improve the efficiency at the LPM.

For this dual-mode operation, an external switch is required just on a dc path, which results in no imbalance for the HPM between the positive and negative signal paths. An additional switch in the dc path can be cheaper and causes no signal loss. On the other hand, since an additional switch was required on a signal path in the previous related work [5], the parasitic capacitance of the switch and asymmetry in layout can cause an imbalance between the signal paths.

Fig. 2 shows a schematic of the proposed two-stage dual-mode CMOS PA and off-chip input–output baluns implemented on a printed circuit board (PCB). For the first and second stages, the total gate width of 880 and 4400 μm are used, respectively. Thick-oxide transistors with a gate length of 0.5 μm to have a breakdown voltage of about 10 V are used for both stages. *RC* feedback networks are employed to secure the stability of the circuit for both the first and second stages.

The load network includes drain bias feeders using a parallel *LC* resonance circuit for both transistors in the positive and negative paths. Also, included is a power switch to turn the V_{DD} of the transistor in the negative path OFF for the LPM. In addition, the dc-blocking capacitor was optimized to have a series resonance with a bond-wire inductance. The result was that the lower end of the output balun can be grounded for the LPM when the transistor in the negative path is turned ON.

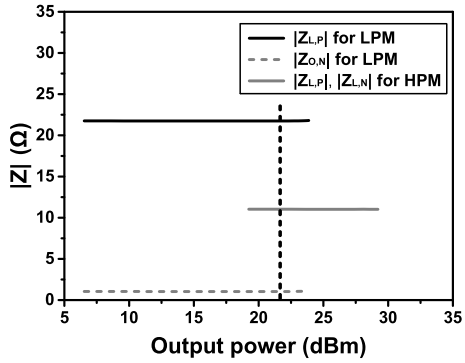
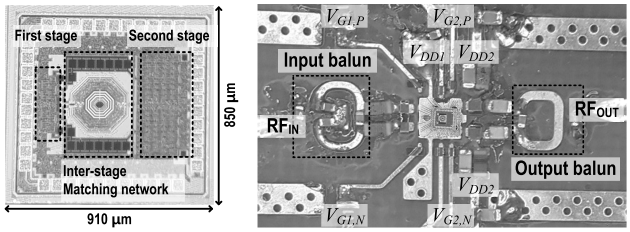


Fig. 3. Simulated impedances for the HPM and LPM.



(a) (b)

Fig. 4. Photographs of the implemented dual-mode PA. (a) Chip microphotograph. (b) Evaluation board.

When the transistor in the negative path is turned ON at the LPM, its ON-resistance is as small as 0.33 Ω and can add very little loss to the transformer.

Fig. 3 shows the simulated impedances for the LPM and HPM. For the LPM, the transistor in the negative path, as an ON-state, provides the balun with very low output impedance, $Z_{O,N}$. For the HPM, the load impedance of the transistors in the positive and negative paths, $Z_{L,P}$ and $Z_{L,N}$, are about 11 Ω with very small reactance, while $Z_{L,P}$ is modulated to have a two times larger value of 22 Ω for the LPM. As in the case of the Doherty PA, the proposed dual-mode PA has a peak efficiency at a power level with 6-dB output backoff.

III. Implementation and Experimental Results

Fig. 4 shows a chip microphotograph of the fabricated dual-mode PA and an evaluation board. The PA IC was fabricated using a SMIC's 55-nm CMOS process. Including bond

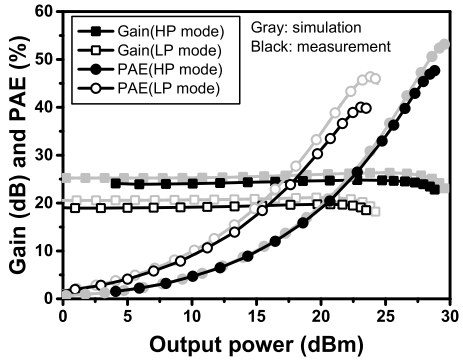


Fig. 5. Measured and simulated results of the proposed PA using 920-MHz CW signal.

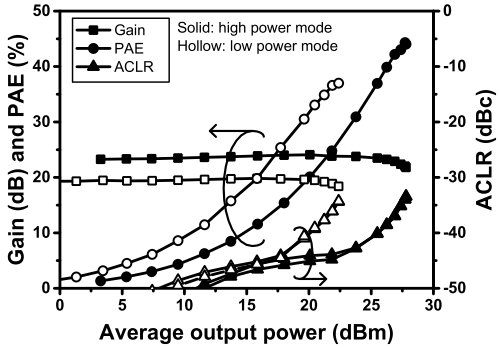


Fig. 6. Measured results of the dual-mode PA using the NB-IoT signal: gain, PAE, and ACLR.

pads, the size of the implemented PA IC is 770×820 μm^2. Input and output baluns were designed using a four-layer PCB. An external switch, Texas Instrument's TPS22990, was deployed on the module. TPS22990 has an ON-resistance of 3.9 mΩ which can drop the V_{DD2} of the negative path for the HPM by just 0.7 mV at the peak output power.

Fig. 5 shows the measured and simulated performances using a continuous wave (CW) signal with a frequency of 920 MHz. The PA has quiescent currents of 16 and 25 mA in the HPM. In the LPM, it has quiescent currents of 7 and 10 mA for the first and second stages, respectively. For both operation modes, V_{DD1} and V_{DD2} are 3.3 V. A power-added efficiency (PAE) of 46.8% was achieved at an output power of 28.2 dBm in the HPM. A PAE of 39.7% was obtained at an output power of 23.1 dBm in the LPM. The measured and simulated performances are in very good agreement.

Fig. 6 shows the measured gain, PAE, and adjacent channel leakage power ratio (ACLR) of the implemented dual-mode PA using the uplink NB-IoT signal, which has a channel bandwidth of 200 kHz (12 subcarriers with a spacing of 15 kHz) and a PAPR of 5.7 dB at a center frequency of 920 MHz. In the HPM, a gain of 24.1 dB, a PAE of 44.3%, and an ACLR of -33.9 dBc at an average output power level of 27.7 dBm were obtained. The PA delivers a gain of 19.3 dB, a high PAE of 37.7% which is 13% points higher than that in the HPM, and an ACLR of -34.9 dBc at an average output power of 21.7 dBm for the LPM. Table I summarizes the measured performances and compares them to the previously reported CMOS PAs with efficiency enhancement techniques.

TABLE I
PERFORMANCE COMPARISON TO THE PREVIOUSLY REPORTED CMOS PAS

Ref.		[2]	[3]	[5]	This work
Freq. (MHz)		1900	880	1850	920
Process		40 nm CMOS	180 nm CMOS	180 nm CMOS	55 nm CMOS
Signal (PAPR)		LTE (8.4 dB)	LTE (7.5 dB)	LTE (7.5 dB)	IoT (5.7 dB)
P_{OUT} (dBm)		23.4	25.5	26.0	27.7
PAE (%)	0 dB BO‡	23.3	43.6	32.9	44.3
	6 dB BO‡	18.4†	23.0	26.4†	37.7†
Gain (dB)		21.3 18.2†	12.7	15.3 10.5†	24.1 19.3†
ACLR (dBc)		–30.1 –30.0†	–34.2	–31.0 –31.4†	–33.9 –34.9†
Output maching		On chip	Off chip	On chip	Off chip
Remark		SCTF DPA	VDPA	Dual-mode	Dual-mode

†: low-power mode (6 dB BO)
‡: back-off for an average power level
SCTF: series combining transformer based Doherty PA
VDPA: voltage combined Doherty PA

IV. CONCLUSION

In this letter, a CMOS two-stage dual-mode PA IC was proposed for the purpose of improving the efficiency at the low-output power level. Load-impedance modulation for the LPM is achieved using the transistor in the negative path as a switch to connect a ground to the lower end of the output balun. For the HPM, full differential operation was achieved without any possible imbalance between the positive and negative signal paths. The proposed two-stage dual-mode PA IC was designed using a 55-nm CMOS process, and this was evaluated using input and output baluns designed on a four-layer PCB. Using an uplink NB-IoT signal with a PAPR of 5.7 dB and a channel bandwidth of 200 kHz for the 920-MHz band, the proposed PA exhibited gains of 24.1/19.3 dB, PAEs of 44.3/37.7%, and ACLRs of $-33.9/-34.9$ dBc at average output power levels of 27.7/21.7 dBm for the HPM/LPM, respectively. Efficiency improvement is as high as 13% points by a mode change to the LPM at a given power level of 21.7 dBm.

REFERENCES

[1] G. Liu, P. Haldi, T.-J. K. Liu, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600–609, Mar. 2008.
[2] E. Kaymaksut and P. Reynaert, "Dual-mode CMOS Doherty LTE power amplifier with symmetric hybrid transformer," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 1974–1987, Sep. 2015.
[3] Y. Cho, K. Moon, B. Park, J. Kim, and B. Kim, "Voltage-combined CMOS Doherty power amplifier based on transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3612–3622, Sep. 2016.
[4] J. Ham *et al.*, "CMOS power amplifier integrated circuit with dual-mode supply modulator for mobile terminals," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 1, pp. 157–167, Jan. 2016.
[5] Y. Cho *et al.*, "Transformer based dual-power-mode CMOS power amplifier for handset applications," in *Proc. Eur. Microw. Conf.*, Oct. 2014, pp. 1380–1383.
[6] H. Lee *et al.*, "Compact load network for GaN-HEMT Doherty power amplifier IC using left-handed and right-handed transmission lines," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 3, pp. 293–295, Mar. 2017.