A single chip SiGe BiCMOS Transceiver and SiGe Power Amplifier for 5.8 GHz WDCT applications

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***Abstract* — A fully integrated RF-transceiver and power amplifier for 5.8 GHz frequency band operation are presented. The transceiver is composed of a low noise amplifier, low-IF receiver, digital demodulator, fully integrated VCO, PLL, transmitter and 2 dBm output amplifier. For typical applications in transmit mode, a subsequent 25 dBm power amplifier (PA) is integrated. The PA and the transceiver are fabricated using Atmel´s SiGe and SiGe BiCMOS technology, respectively. The transceiver and PA operate from a single lithium battery, avoiding mechanical tuning. The number of external components is drastically reduced compared to previous solutions.**

***Index Terms* — Cordless telephone systems; power amplifiers, transceivers.**

I. Introduction

The demand for high performance, low cost RF transceivers is ever increasing in commercial wireless applications. Applications such as digital cordless phones are experiencing constant pressure to reduce price while maintaining or improving performance. Current solutions exploit the worldwide license-free 2.4 GHz frequency band. Unfortunately, the many applications nearly overcrowd this band, such as high-power microwave ovens, cordless phones, Bluetooth® and HomeRF applications, WLAN, game pads, etc. As a consequence, significant RF interference is present within the 2.4 GHz band /1/.

To partly overcome this shortfall, mixed applications using both 2.4 GHz and 5.8 GHz for TX- and RX-link are used /2/.

The license-free 5.8 GHz frequency band has a much wider spectrum available. Furthermore, investigations showed that 5 GHz applications in narrow surroundings can provide better performance than 2.4 GHz applications as the shorter wave length propagates farther. In addition, 5.8 GHz systems can nearly always be operated at higher data rates than 2.4 GHz systems /3/.

In order to exploit these advantages, a single chip 5.8 GHz transceiver and power amplifier (PA) was designed supporting all 142 available channels.

II. Block Diagram

Figure 1 shows the block diagram of the transceiver. The transceiver is composed of a low noise amplifier, image rejection mixer, limiter amplifier, digital demodulator, fully integrated VCO, PLL and 2 dBm output amplifier. It supports two data rates of 576 and 1152 kBit/s and frequency deviations of 200 and 400 kHz. The transceiver is programmed by a 3-wire bus using a 16-bit data word. An integrated bandgap-stabilized voltage regulator supplies the VCO. To support a PIN diode switch at the antenna, two open drain switches sinking 10 mA each are also implemented.

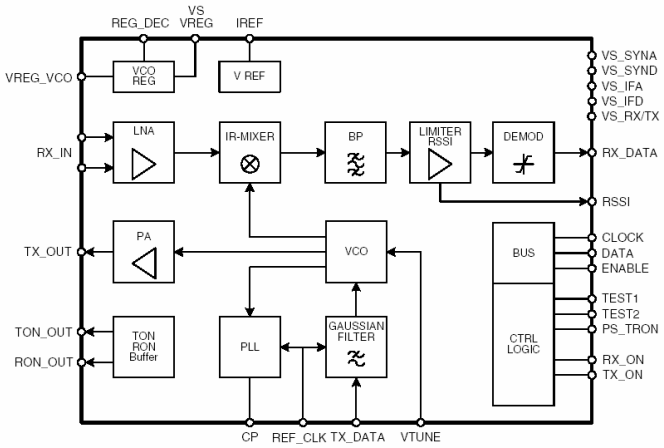


Fig. 1. Block Diagram of Transceiver

A. Receive Mode

The receiver uses a single-conversion low-IF superheterodyne concept. The input signal is fed to the 5.8-GHz low-noise amplifier (LNA), followed by an image rejection mixer. The required 0° / 90° phase shift of the LO is realized by a polyphase filter. The mixer features an image rejection of 30 dB and converts the signal down to the low IF of 864 kHz. Next the signal is filtered by an active polyphase filter, passed to an intermediate-frequency (IF) amplifier and digital demodulator, buffered and then fed to a baseband processing IC. In the IF chain, a received signal-strength indicator (RSSI) signal is also derived.

B. Transmit Mode

In transmit mode the digital data stream is gaussian-type filtered and directly modulates the VCO. This gaussian filter shapes the digital data stream very precisely to keep adjacent channel emissions low (see figure 7). After modulation, the signal is fed to the internal PA which supplies 2 dBm of output power to the subsequent power amplifier. The spectrum of the modulated output signal of the transceiver IC at 5.8 GHz without external filtering can be seen in figure 8.

The fully integrated VCO with on-chip inductor operates at 5.8 GHz with 1GHz tuning range @ Vtune = 0.5 to 2.5V. In order to reduce tuning gain, an automatic pretuning circuitry controlling 4-Bit switched capacitor is implemented. Tuning gain and thus noise sensitivity is reduced to 100 MHz/V at the tuning input. Phase noise of approx. -106 dBc at an offset of 1 MHz is achieved (see figure 9).

C. Power Amplifier

The output level of the transceiver signal is 2 dBm and can be further amplified by a subsequent power amplifier, implemented in SiGe technology. Figure 2 shows the corresponding block diagram. The PA consists of a three stage amplifier with interstage matching and open collector output.

The power amplifier achieves a small signal gain of 30 dB, a maximum PAE of 38% and a saturated output power of 25dBm (at a supply voltage of 3.6V). The operating frequency range is 5.1 to 5.9 GHz.

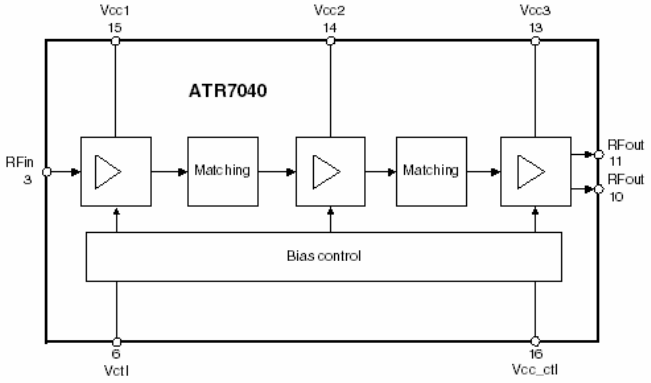


Fig. 2. Block Diagram of Power Amplifier

III. Application

To maintain cost targets, low cost QFN32 (transceiver) and QFN16 (PA) packaging is used. The low paddle inductance used for ground connection and leadless construction provide excellent thermal and electrical performance.

High integration level allows the design of a very compact 2 layer PC board using cost effective FR4 material and only one component side. Furthermore, the transceiver and PA do not require any mechanical tuning. The transceiver operates from 2.9 to 3.6V and supports simple power management by means of an integrated regulator and power down mode. The PA is designed to operate from 3.2 to 3.8V

Table 1 lists the current consumptions of the transceiver in the different modes.

Figure 3 shows the test board used for RF transceiver measurements.

TABLE I
SUMMARY CURRENT CONSUMPTION

Mode	Current	
Power Down	1	µA
Synthesizer	28	mA
Receiver	59	mA
Transmitter	16	mA

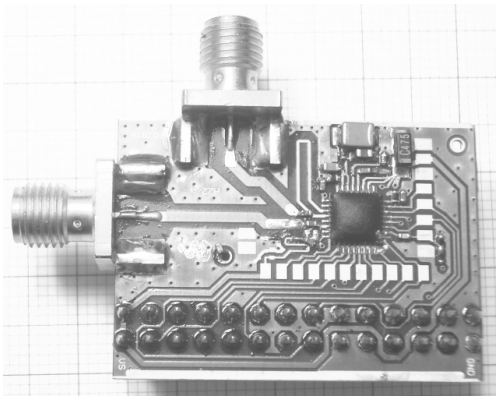


Fig. 3 View of the test board used for measurements (core size 15 mm x 15 mm)

Figures 4 and 5 show typical applications of the transceiver and PA.

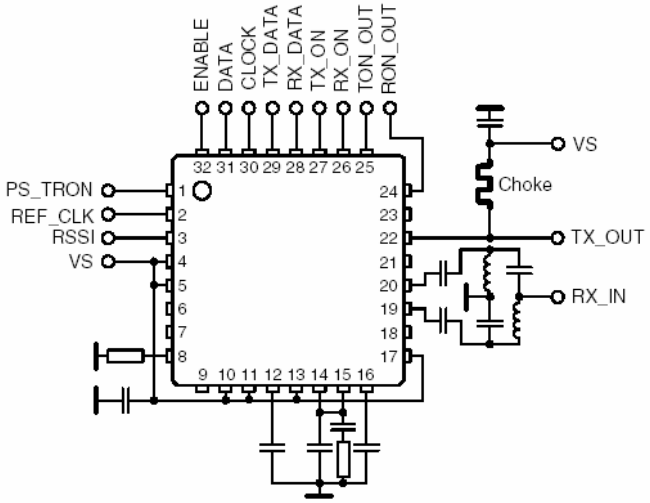


Fig. 4 Typical application circuit (transceiver)

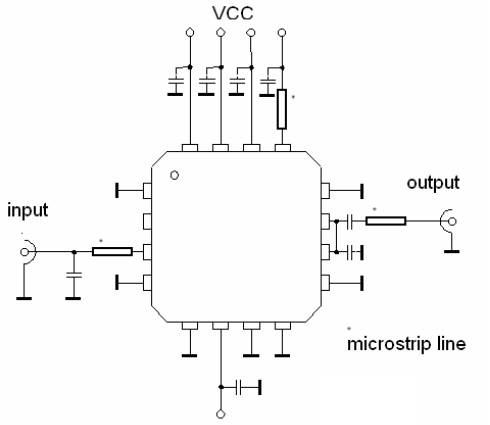


Fig. 5 Typical application circuit (power amplifier)

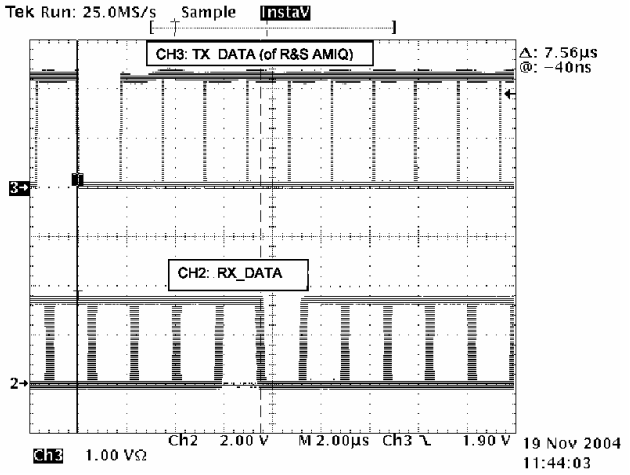


Fig. 6 Eye Diagram of Regenerated RX-Data at -85 dBm

IV. Technologies Used

Due to the requirements of the circuits, two different Atmel technologies were used. The transceiver was fabricated using SiGe BiCMOS AT46k technology, a triple poly hetero bipolar technology including SiGe npn HBT, 0.35 µm CMOS, MIM-(metal insulator metal) and double poly capacitors, different types of poly resistors, as well as three metal layers and an additional inductor layer for spiral inductors.

The HBT´s of AT46k technology are characterized by a minimum emitter size of 0.8µm x 1.6 µm, transit frequencies (f_T) of 35GHz and 50GHz and collector emitter breakdown voltages (BV_{CE}) of 5.0V and 3.0V (non SIC and SIC), respectively.

For the power amplifier, SiGe2Power technology was used. This technology is a double poly hetero bipolar technology with minimum emitter size of 0.5µm x 1.1µm, transit frequencies (f_T) of 33GHz and 42GHz and collector emitter breakdown voltages (BV_{CE}) of 6.3V and 4.5V (non SIC and SIC), respectively.

V. Measured Results

It should be mentioned that all measurements presented were made using first silicon, i.e., complete functionality was achieved using first silicon.

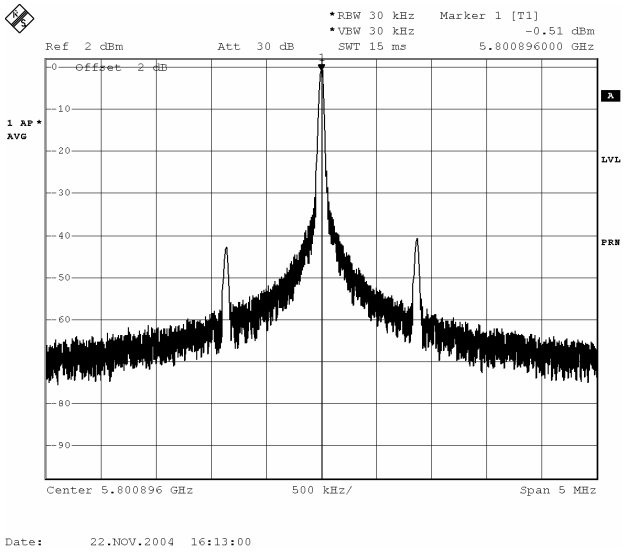
A. Receive Mode

Maximum input sensitivity of –96 dBm @ 576 kbit/s data rate and 200 kHz frequency deviation and of –94 dBm @ 1152 kbit/s data rate and 400 kHz frequency deviation were measured. Figure 6 shows the eye diagrams in receive mode.

A. Transmit Mode

Figures 7 and 8 show the transceiver output signal without modulation, and modulated with a PRBS signal, respectively.

Figure 9 shows the result of phase noise measurement in transmit mode. Phase noise of approx. -106 dBc at an offset of 1 MHz is achieved.



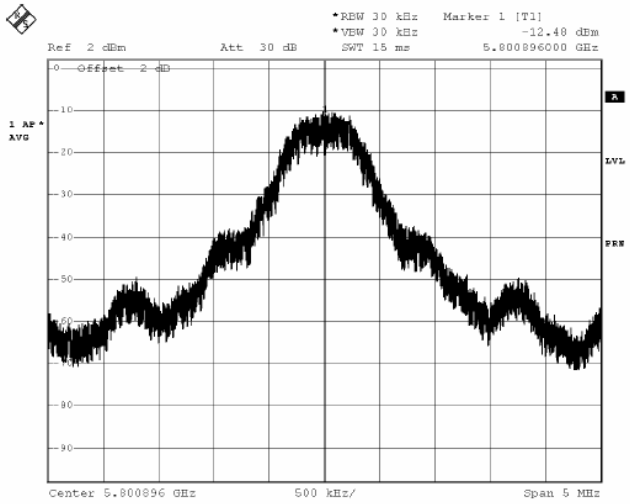


Fig. 7 TX output signal @ 5.8 GHz (carrier only)
Fig. 8 TX output signal @ 5.8 GHz (PRBS modulated)

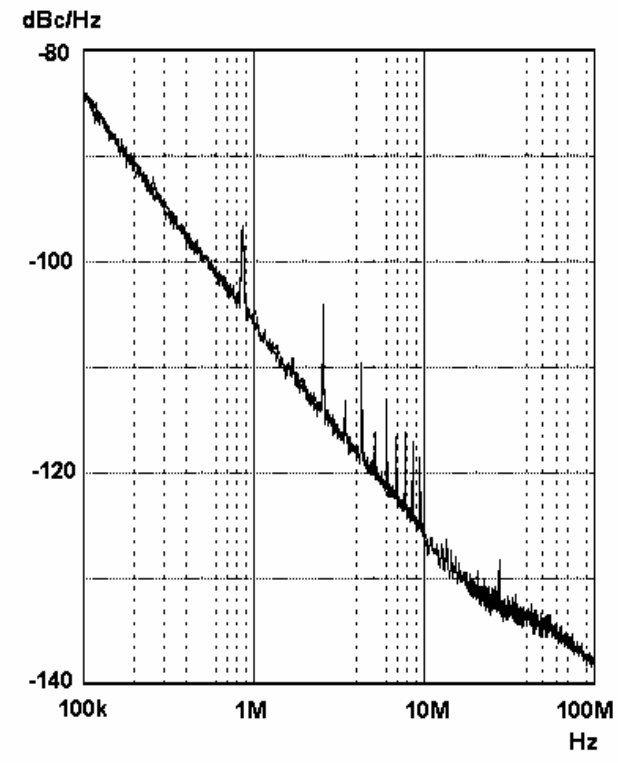


Fig. 9 Phasenoise Performance of VCO in Transmit Mode

Figures 10 and 11 show chip photos of the transmitter and power amplifier chips, respectively.

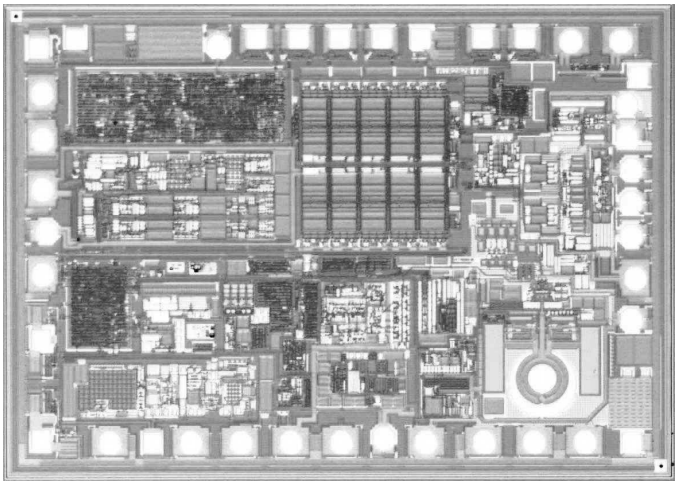


Fig. 10 Chip photo transceiver (AT46k technology)

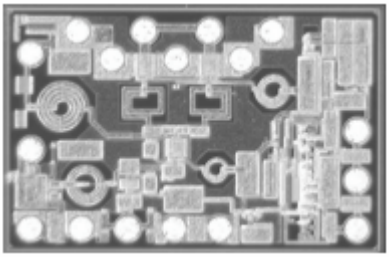


Fig. 11 Chip photo power amplifier (SiGe2Power technology)

VI. Conclusion

The trend to exploit the 2.4 GHz frequency band will further continue. To avoid interference, a change to the 5.8 GHz frequency band is conceivable. In this paper, a one-chip transceiver and power amplifier for application in the 5.8 GHz frequency range were presented. The high integration level and need for fewer external components will help to reduce manufacturing costs of wireless applications.

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