# Differential SiGe Power Amplifier for 3GPP WCDMA

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*Abstract* — **An integrated differential two-stage power amplifier (PA) operating at the 2 GHz frequency range is introduced. The implemented power amplifier uses 2.7 V supply voltage and was fabricated with 0.35μm SiGe BiCMOS technology. The measured output power at the -1 dB compression point is 21 dBm, but the amplifier is capable of providing 26.7 dBm output power at the –5 dB gain compression. The measured linear gain is 22 dB. The chip area is 2.36 mm$^2$ including bonding pads. The linearity performance of the power amplifier was measured with 3GPP WCDMA basestation signal. The power amplifier fulfilled the 3GPP WCDMA Adjacent Channel Leakage Ratio (ACLR) specifications (ACLR1=45 dB and ACLR2=50 dB) with 11.65 dBm average channel output power.**

## I. Introduction

In the last few years the dominant technology in the area of power amplifier design has been gallium arsenide (GaAs). Power amplifiers based on GaAs achieve high efficiency and linearity with high output power [1]. Recently, silicon germanium (SiGe) heterojunction bipolar transistors (HBT) have demonstrated a competitive power added efficiency (PAE) and linearity performance in the power amplifier applications [2]. Using SiGe technology it is possible to improve the performance of Si transistors for RF and microwave applications and still preserve the high yield, cost and manufacturing advantages associated with conventional Si fabrication [3]. SiGe technology provides high current gain (β) and low noise. Furthermore, with BiCMOS technology the integration of logic functions, e.g. power management, is possible. The advantage of the SiGe HBT compared to GaAs HBT is a small $V_{CE,SAT}$, thus the power amplifier can be designed for lower supply voltages ($V_{CC}$ = 2.7 V and below) [4]. In addition, Si has higher thermal conductivity compared to GaAs and thus, the thermal design of the power amplifier is relaxed. The major disadvantage in all silicon-based processes is the low breakdown voltage between the collector and the emitter ($BV_{CEO}$), which leads to very small optimum load resistance values.

The designed chip was processed using 0.35 μm SiGe BiCMOS technology with 5.8 V $BV_{CEO}$. Design aspects and procedure of the implemented power amplifier are discussed in section II and III. Simulations and measurement results are given in section IV.

## II. Design Aspects of Power Amplifier

### *A. Characterization of Unit Transistors*

To achieve desired output power, sufficient current and voltage must be driven from the last amplifier stage to the output load. Therefore, the lowering of the supply voltage increases the required current. This means that an adequate number of parallel unit transistors has to be used in order to meet increased current requirements. The gain and the RF output power of a unit transistor varies as a function of the DC bias current and furthermore, a unit transistor has a certain maximum DC current limit according to electron migration rules of the used technology.

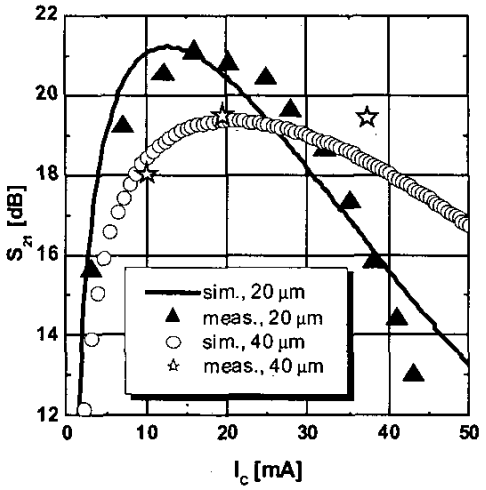


Fig 1. The simulated and measured small signal gain, $S_{21}$, of the SiGe unit transistor with four 20 μm wide and with four 40 μm wide emitter fingers as a function of the collector bias current.

In order to maximize the gain of the single unit transistor and to choose the adequate number of unit transistors for both amplifier stages, the variation of the gain as a function of a DC collector bias current was



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simulated and measured for a two types of fabricated SiGe unit transistors: one with four 20 μm wide emitter fingers and one with four 40 μm wide emitter fingers. These simulation and measurement results are shown in Figure 1. According to these results, the small signal models of the unit transistors are found to be accurate. The unit transistor with 20 μm wide emitter fingers has more small signal gain than the one with wider emitter fingers. Therefore, unit transistors with narrower emitter fingers were used in this design and 16 mA DC collector current was chosen for each unit transistor in the driver and the power stage.

*B. Emitter and Base Ballasting Resistor*

At high current densities, bipolar transistors suffer from thermal instability. However, the thermal instability affects differently in Si BJTs, AlGaAs/GaAs HBTs and SiGe HBTs. Si BJTs have a positive feedback between the current and the base-emitter junction temperature, i.e. current gain (β) increases with temperature. Because of this positive thermal feedback mechanism, at high current densities current crowding occurs, local hot spots are formed and this leads to thermal runaway and junction destruction [5]. In AlGaAs/GaAs HBTs, the current gain decreases with temperature. In this case, device self-heating at high current densities, which results from the increasing of the collector-emitter bias voltage ($V_{CE}$), leads to a thermal phenomenon called the collapse of current gain [6][7]. Although the current gain of the SiGe HBT decreases with temperature, no current crush occurs in this device even at high collector-emitter bias voltages. Instead, at high current densities the emitter current in a SiGe HBT may be constricted to localized hot spots, which eventually can lead to the second breakdown, as is the case with Si BJTs [8].

To quarantee uniform current distribution between all unit transistors and to avoid thermal instability problems, ballasting resistors are used in this SiGe power amplifier. Emitter ballasting resistors can be used in all type of bipolar transistors, but the use of base ballasting resistors requires a negative thermal feedback mechanism. Therefore, the base ballasting resistors are suitable for AlGaAs/GaAs and SiGe HBTs, but not for Si BJTs [7].

The minimum required value of a base ballasting resistance ($R_{bb}$) depends on the intrinsic emitter and base resistances ($r_e$ and $r_b$) of the transistor, common base and common emitter current gains (α and β) as well as the energy gap ($E_g$) of the SiGe transistor's base material [5].

One choice is to integrate the base ballasting resistor in series with the RF input signal path. A series resistor in the RF path introduces loss, which is undesired. However, because of this ballasting resistor is for thermal stability, it can be integrated to the biasing current path. Hence, this is preferable, since the resistor lies now in parallel compared to the RF input signal path, as shown in Figure 2 ($R_1$ and $R_2$), and does not produce any loss. Base ballast resistance of 200 Ω per unit transistor was chosen in this design.

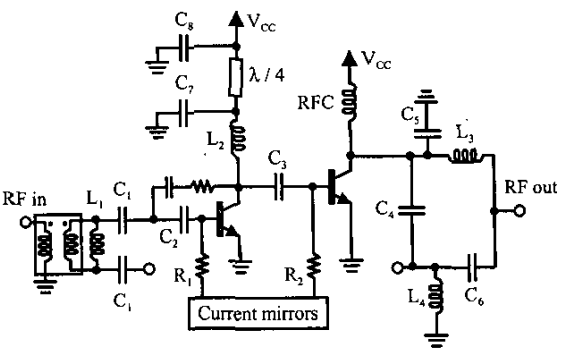


Fig 2. Schematic of the one branch of the differential implemented power amplifier.

## V. Design of the Power Amplifier

The schematic of the designed and realized two stage power amplifier is shown in Figure 2. The output matching network is completely external because of the high output power, but the input and the interstage matching networks are partly integrated on-chip. Biasing of the amplifier was implemented using 1:10 PMOS current mirror. Current mirror includes on-chip RC-filter network to prevent a bias oscillations. A negative on-chip RC-feedback is used in the driver stage to improve the linearity and stability as well as to increase the input resistance. RC-feedback was designed to be tunable with postprocessing. Power amplifier has 16 unit transistors (8 unit transistors for each differential branch) in the driver stage and 60 unit transistors in the power stage. The chip grounding has been realized through bonding wires, which are excluded from the Figure 2. To prevent the gain reduction introduced by the emitter bonding wires, the differential topology was selected.

*A. Interstage Matching*

The interstage matching network in this design contains capacitors $C_3$, $C_7$, $C_8$, an $L_2$ and a λ/4-microstrip, as shown in Figure 2. The purpose of the interstage matching is to provide optimum load resistance, which is approximately 20 Ω, for the driver stage. In addition, the interstage matching has a significant effect on the bandwidth and the stability of the amplifier.

A high-pass series-C and shunt-L topology was chosen to perform the interstage matching, because this topology

reduces the gain below the operating frequency. band. Furthermore, the series-C ($C_3$) is easier to integrate and the shunt-L can be implemented with a bonding wire ($L_2$). The off-chip capacitor $C_7$ is used to tune out the value of the shunt-L inductor. By choosing $C_7$ properly the bandwitdh of the whole power amplifier can be tuned.

The purpose of the λ/4-microstrip and the capacitor $C_8$ is to isolate the interstage matching circuit from the driver supply voltage circuit at the signal frequency: The capacitor $C_8$ is a short circuit at the signal frequency and the λ/4-line will transforms this zero impedance to infinite impedance. Hereby, the interstage matching circuit is isolated from the DC-feed line.

*B. Input and Output Matching*

The input matching circuit consists of a discrete 1:1 balun and a simple external high-pass LC-matching network ($L_1$, $C_1$). The input high-pass LC-network increases the overall stability of the amplifier because of the gain reduction below the operating frequency band. In addition, part of the input matching is realized with the integrated on-chip DC-block capacitor ($C_2$). This DC-block capacitor consists of smaller capacitors that are placed at the base of each unit transistor.

The output matching circuit is a combination of a traditional low-pass network and a lumped-element balun. The low-pass network consists of bonding wires in series at the output of the chip and a parallel off-chip capacitor ($C_4$). The balun has been constructed of discrete inductor ($L_4$) and capacitor ($C_6$) elements forming a high-pass response to the other branch and a low-pass for the other. The balun is used to transform the differential output signal into single-ended output signal.

The microphotograph of the power amplifier chip is presented in Figure 3. The chip area is 1.25 mm x 1.89 mm = 2.36 $mm^2$ including the bonding pads.

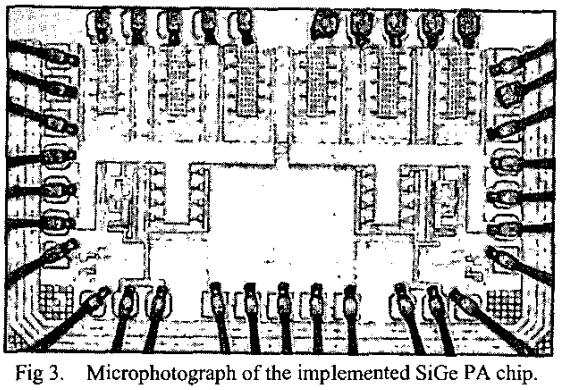

Fig 3. Microphotograph of the implemented SiGe PA chip.

## VI. Simulations and Measurements

The realized power amplifier chip was directly mounted on the measurement PCB by wirebonding. The simulations and measurements include the PCB, which was modeled on the simulator using coplanar lines and microstrips. In addition, parasitic capacitances between the substrate and different nodes, originated from the metal conductors on the chip, were taken into account in the simulations. However, at the input an ideal lossless 1:1 balun model was used in the simulation. The operating frequency range of the balun used in the measurements was limited to 3000 MHz. All bonding wire inductances were estimated for the simulations, because they are an important part of the entire RF design. In addition, the mutual inductance between the output bonding wires was included in the simulations.

The measured small signal scattering parameters $S_{11}$ and $S_{21}$ are presented in Figure 4. RC-feedback in the implemented power amplifier was designed to tunable with post-processing. Measurements for the separate driver amplifier test chip indicated 7.5 dB lower gain than in simulations. Therefore RC-feedback was reduced to half in order to increase the gain of the implemented two-stage power amplifier. From the Figure 4 it can be seen that the gain was increased by 7 dBs after the reduction of RC-feedback.

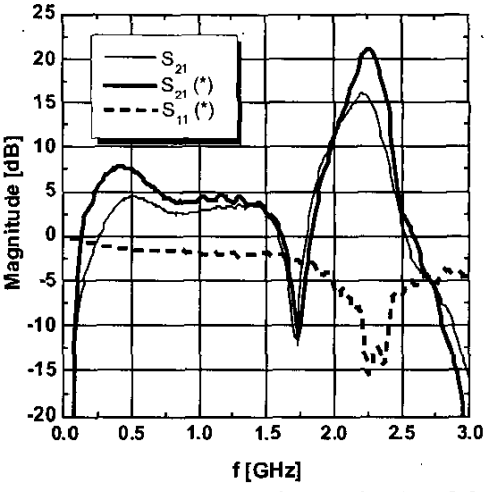


Fig. 4. Measured $S_{11}$ and $S_{21}$. Reduced RC-feedback measurements are indicated with "*".

The measured AM-AM conversion and the gain as a function of input power are presented in Figure 5. The –1 dB compression point of the implemented amplifier is 21 dBm. The measured maximum output power and

power added efficiency (PAE) achieved in –5 dB gain compression are 26.7 dBm and 18.5 % respectively.

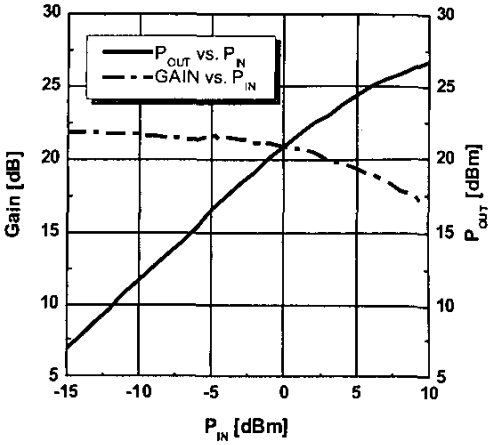


Fig. 5. Measured AM-AM conversion and the gain as a function of input power.

The linearity performance of the implemented power amplifier was measured with the 3GPP WCDMA basestation signal. The power amplifier fulfills the 3GPP WCDMA Adjacent Channel Leakage Ratio specification with the 11.65 dBm channel output power (Figure 6).

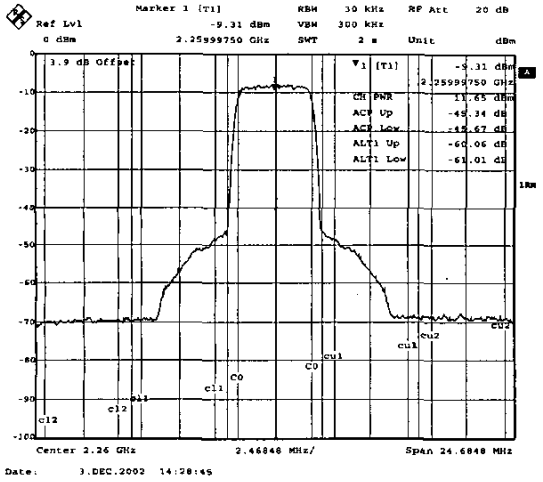


Fig. 6. Measured spectrum of the power amplifier when 3GPP WCDMA Adjacent Channel Leakage Ratio specifications are fulfilled.

## VII. Conclusions

An integrated two-stage power amplifier chip for 3GPP WCDMA was designed and measured. The implemented differential power amplifier uses 2.7 V supply voltage and the measured OCP is 21 dBm. The measured maximum output power and PAE in –5 dB gain compression are 26.7 dBm and 18.5 % respectively. The measured gain was increased to 22 dB from 15 dB with decreasing the negative RC-feedback with post-processing. The linearity of the implemented power amplifier was tested with the 3GPP WCDMA basestation signal. The power amplifier fulfills the ACLR specification for downlink with the 11.65 dBm channel output power. The used SiGe process is potential candidate for PA applications.

## Acknowledgement

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## References

[1] Matilainen M.J., Nummila K.L.I., Järvinen E.A., Kalajo S.J.K. "An Integrated 900-MHz Push-Pull Power Amplifier for Mobile Applications". *IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, pp. 861-864, 2000.

[2] Raghavan A., Heo D., Maeng M., Sutono A., Lim K., Laskar J. "A 2.4 GHz High Efficiency SiGe HBT Power Amplifier with High-Q LTCC Harmonic Suppression Filter". *IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, pp. 1019-1022, 2002.

[3] Cressler J.D. "SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 46, No. 5, pp. 572-589, May, 1998.

[4] Harame D. L. et al. "Current Status and Future Trends of SiGe BiCMOS Technology". *IEEE Transactions on Electron Devices*, Vol. 48, No. 11, pp. 2575-2594, November, 2001.

[5] Arnold R.P., Zoroglu D.S. "A Quantitative Study of Emitter Ballasting". *IEEE Transactions on Electron Devices*, Vol. ED-21, No. 7, pp. 385–391, July, 1974.

[6] Liu W., Nelson S., Hill D., Khatibzadeh A. "Current Gain Collapse in Microwave Multifinger Heterojunction Bipolar Transistors Operated at Very High Power Densities". *IEEE Transactions on Electron Devices*, Vol. 40, No. 11, pp. 1917–1927, November, 1993.

[7] Liu W., Khatibzadeh A., Sweder J., Chau H.F. "The Use of Base Ballasting to Prevent the Collapse of Current Gain in AlGaAs/GaAs Heterojunction Bipolar Transistors". *IEEE Transactions on Electron Devices*, Vol. 43, No. 2, pp. 245–251, February, 1996.

[8] Zhang J., Jia H., Tsien P.H., Lo T.C. "Emitter-Ballasting-Resistor-Free SiGe Microwave Power Heterojunction Bipolar Transistor". *IEEE Electron Device Letters*, Vol. 20, No. 7, pp. 326–328, July, 1999.