A Fully Integrated Triple-Band CMOS Hybrid-EER Transmitter for WCDMA/LTE Applications

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Abstract — This paper presents a fully integrated triple-band CMOS hybrid-EER transmitter for WCDMA/LTE applications. The operation frequency bands are 0.8/2.3 GHz for LTE and 1.9 GHz for WCDMA applications with multi-band class-E power amplifier (PA) using a power cell resizing technique and a multi-tap transformer. The multi-mode envelope amplifier support 3.84-MHz WCDMA and 5-MHz LTE signal with a dual-switching stage for high efficiency. The PA and envelope amplifier are integrated in a single chip using CMOS process with input/output matching networks. To compensate the nonlinearity of the supply modulated transmitter, the on-chip linearizer is design on a chip. The transmitter achieves output powers of 23/26/22 dBm and power-added efficiency of 27/33/23 % at each frequency band. The transmitter is implemented in a 0.18 µm CMOS process. The total chip size is 1.6 x 2.5 mm².

Index Terms — CMOS, Hybrid-EER, LTE, Power Amplifier, WCDMA.

I. Introduction

The new generation of mobile communications demands a reconfigurable radio covering backward compatibility. In particular, a power amplifier (PA) which consumes a significant amount of the area on a chip and which requires stringent specifications for each communication standard, must be reconfigurable with a single-chip structure. However, the PAs developed thus far satisfy multi-band operation requirements using a separate, independent multiple amplifier [1] for each standard or by switching to a corresponding matching network from among a bank of multiple matching networks [2] with a significant penalty in the chip area, cost and complexity. In this paper, we present a fully integrated single chip CMOS transmitter which reconfigures the operating frequency and modulation mode for WCDMA/LTE applications. The multi-band operation mechanism, linearization with common gate (CG) biasing, and power efficient switching of the envelope amplifier (EA) will be discussed. The transmitter was implemented with hybrid-EER (H-EER) structure because this structure has the intrinsic capability of higher average power-added efficiency (PAE) due to the employed switching PA as well as higher linearity due to the immunity to the time mismatch between the envelope and the RF paths [3,4]. The developed transmitter supports triple-bands covering the 800/1900/2300MHz simultaneously in a single chip. For frequency reconfigurable class-E operations, the capacitance was controlled with the number of activated power cells [5] and the inductance with the distance of supply bias node from the symmetric point on an on-chip transformer.

II. Proposed Triple-Band CMOS H-EER Transmitter

The block diagram of the proposed H-EER transmitter is shown in fig. 1. The multi-band class E PA and multi-mode EA were integrated in a single chip. The envelope will be supplied to the EA while the RF signal to the power stage. The common-gate voltage modulation (CGVM) is applied at the gate bias of the CG amplifier to compensate the nonlinearity due to the supply voltage modulation scheme with the shaped envelope signal. The two off-chip inductors with values of 1.7µH and 2µH connected to the output of the switching stage shape the output for envelope amplification along with linear stage output. The amplified envelope will be supplied to the dedicated bias node of the power stage for the selected frequency.

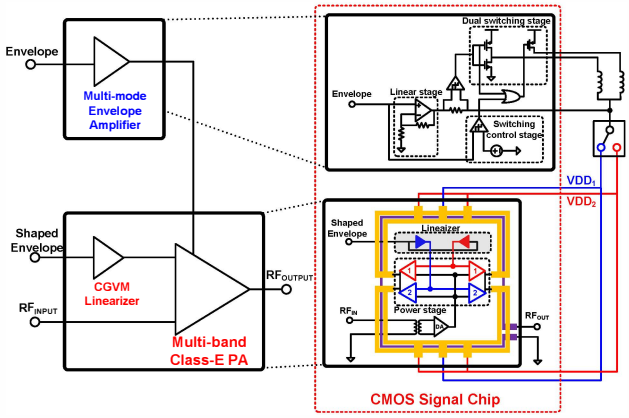

Fig. 1. Proposed H-EER Transmitter.

Fig. 2 shows a multi-band PA schematics. To generate Watt-level output power, the multi-tap transformer has been implemented in order to mitigate the low breakdown voltages of the CMOS technology. The differential cascode structure is adopted to maximize output swing using 0.35µm thick oxide transistor at the CG amplifier. The total gate widths of the common source (CS)/CG amplifiers of powercell-1 (PC-1) and powercell-2 (PC-2) are 5120/4096µm and 3072/2048µm, respectively. For multi-band operation, the PC-1 and PC-2 are activated with selective bias supply to CG and the multi-tap

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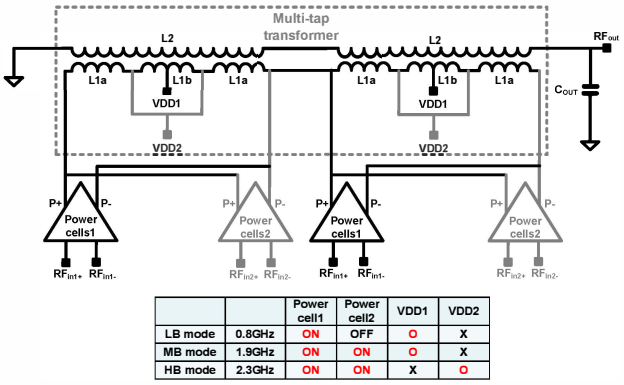
transformer simultaneously. The table in the figure summarizes bias condition of CG and multi-tap transformer for the different bands.



		Power cell1	Power cell2	VDD1	VDD2
LB mode	0.8GHz	ON	OFF	O	X
MB mode	1.9GHz	ON	ON	O	X
HB mode	2.3GHz	ON	ON	X	O

Fig. 2. Schematic of the multi-band class-E PA.

Fig. 3(a) shows a CG amplifier with shaped envelope bias. In the H-EER transmitter, the envelope restoration generates nonlinearity in the output of the PA. At the low supply voltage, the output capacitance increases due to the reverse-biased junction capacitance and the CG amplifier enters in the linear region. The nonlinear capacitance generates AM-AM distortion and the nonlinear resistance of the CG amplifier generated AM-PM distortion. In case of linear PA, the shaped envelope injection to the gate of the CS amplifier was reported for linearity [6]. However, in the switching mode class E PA, the gate bias variation to the CS amplifier distorts clear on-off switching which results in poor efficiency. In this work, we invented the CGVM linearization technique with shaped envelope simply by a linear regulator. Fig. 3(b) shows an evident AM-AM improvement in the normalized input amplitude above 0.2 and AM-PM reduction from 20 to 10 degree simultaneously. The linearization technique dissipates as small as 3.3mW additionally.

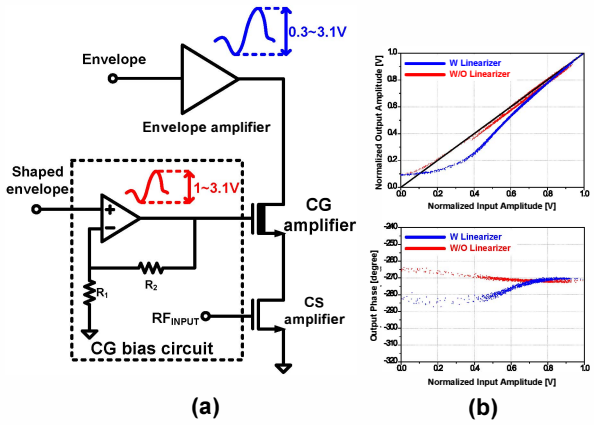


Fig. 3. CG amplifier with shaped envelope bias for linearization.

Fig. 4 shows a schematic of the multi-mode EA. The EA are using dual switching stage for high efficiency [7] The EA includes control stage which senses output envelope level and switches switching stage1 (SW1) and switching control stage which compares the input signal with a reference value (Vref) to switch the switching stage2 (SW2). By switching SW1 and SW2, the efficiency of the EA will be maximized. The EA output current to the PA is provided from SW1 in addition to linear current (Ilinear) when the input signal is lower than the Vref, while from SW1 and SW2 simultaneously when the signal is higher than Vref. The size of the PMOS in SW1 is 20,000μm/0.3μm and SW2 is 10,000μm/0.3μm, respectively. The simulation reveals an improvement of EA efficiency by 3.3 and 2.7% compared to a single switching operation for WCDMA and LTE modes when the V_{ref} value is optimized to 0.7V and 0.62V, respectively.

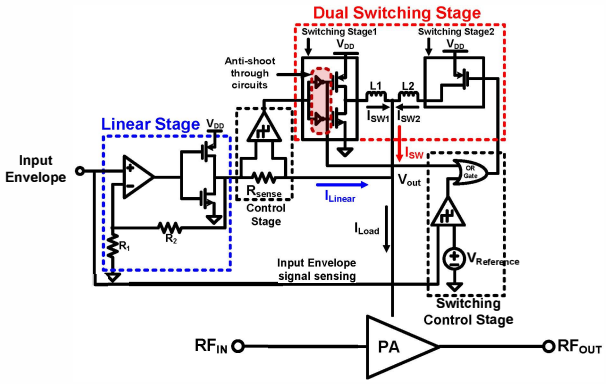


Fig. 4. Switching-controlled Envelope Amplifier.

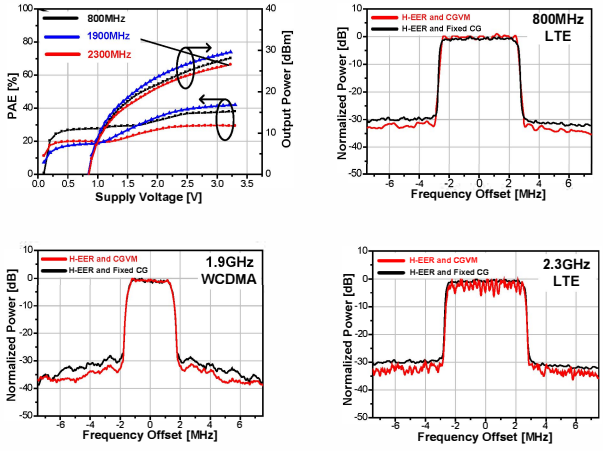


Fig. 5. Measurement Results.

III. Measurement Results

A fully integrated triple-band CMOS H-EER transmitter for WCDMA/LTE applications was fabricated in 0.18μm CMOS technology (Fig. 6), and measurement results are described in Fig. 5. The peak output power and PAE of the PA for each

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band(800/1900/2300MHz) is 28/29.6/26.5dBm and 40/45/37% in CW test. And the maximum output power and overall efficiency of the transmitter satisfying linearity requirement is 26dBm with a PAE of 33% for WCDMA signal at 1900MHz and 23/22dBm with a PAE of 27/23% for LTE signals at 800/2300MHz, respectively. The ACLR improvement at the 5MHz offset with/without linearization technique is above 3dB. The EA efficiency is 72/80/71% for each frequency. The table in Fig. 6 shows a comparison with a recently introduced state-of-the-art multi-band transmitters([1] is a single-chip but with paralleled amplifiers and [2] is with off-chip EA and matching networks). This work reveals a smaller chip size and comparable output power satisfying WCDMA/LTE applications even with the full integration on silicon.

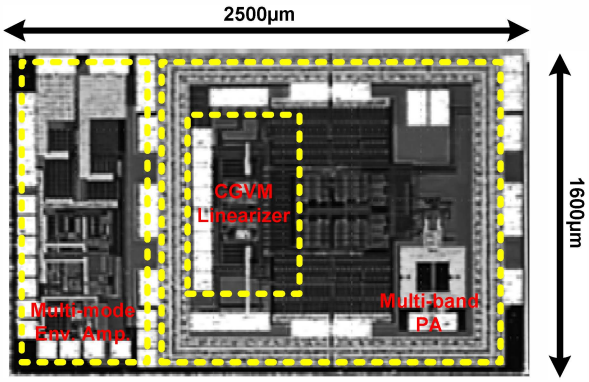

Fig. 6. Die photo of the H-EER transmitter.

IV. Conclusion

We demonstrated a fully integrated triple-band CMOS H-EER transmitter WCDMA/LTE applications. The proposed transmitter is the first single chip integrated PA and EA using CMOS process. And the on-chip linearizer is designed to improve linearity with CGVM technique.

Acknowledgement

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TABLE I
Comparison Table

Section		[4]	[8]	This Work
Band (GHz)		1.7~2.0	0.8/2.3	0.8/1.9/2.3
Mode		LTE	EDGE/WiMAX	WCDMA/LTE
Tehcnology		EA: 0.18μm CMOS PA: pHMET	0.18μm SiGe	0.18μm CMOS
Size (mm^2)		PA: 1.2x1.2 EA: 1.35x1.35	PA: 1.3x1.5 External EA	1.6x2.5 (PA+EA)
Matching Network		Off-chip	Off-chip	On-chip
CW test	Pout (dBm)	-	23/18	28/29.6/26.5
	PAE (%)	-	51/60	40/45/37
Modulation Signal Test	Pout (dBm)	27	20/18.5	27/33/23
	PAE (%)	34.2~39.5	46/30	27/33/23
Envelope Amplifier	Efficiency (%)	-	69/54	72/80/71
	Type	-	Conventional	Dual-swtiching

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