A fully integrated 5.3 GHz, 2.4 V, 0.3 W SiGe-Bipolar Power Amplifier with 50 Ω output

W. Bakalski [1,2], W. Simbürger [2], R. Thüringer [1,2], A. Vasylyev [3], A. L. Scholtz [1]

[1] *Institute of Communications and Radio-Frequency Engineering, Vienna University of Technology*
Gusshausstrasse 25/389, A-1040 Vienna, Austria

[2] *Infineon Technologies AG, Corporate Research, Otto-Hahn-Ring 6, D-81739 Munich, Germany*

[3] *BTU Cottbus, Chair of Circuit Design, Cottbus, Germany*

Winfried.Bakalski@infineon.com

Abstract

A radio frequency power amplifier for 4.8-5.7 GHz has been realized in a 0.25 μm SiGe-bipolar technology. The balanced 2-stage push-pull power amplifier uses two on-chip transformers as input-balun and for interstage matching. Further it uses three coils for the integrated LC-output balun and the rf-choke. Thus the power amplifier is free of any external components. At 1.0 V, 1.5 V, 2.4 V supply voltages output powers of 17.7 dBm, 21.6 dBm, 25 dBm are achieved at 5.3 GHz. The respective power added efficiency is 15.6 %, 22.4 %, 24 %. The small-signal gain is 26 dB.

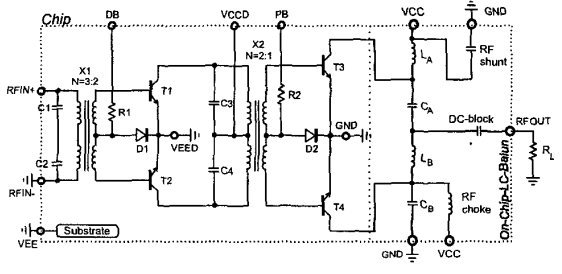

Figure 1. Circuit diagram of the power amplifier.

1. Introduction

Power amplifiers (PA) have always been a key component in mobile radio frequency (rf) systems. As the customers always prefer fully integrated solutions to save cost, a lot of amplifiers have been developed using different techniques to make such devices available [1, 2, 3]. While most fully integrated amplifiers use external output matching using LTCC [4] or laminate housing, the only on-chip matched PA so far reported was [2] for 2.45 GHz in CMOS.

With this work, we present a PA suited for the 5 GHz band with an integrated LC-Output Balun [5, 6] realized in a mass-production SiGe-BiCMOS technology [7, 8]. The push-pull type circuit is based on two on-chip transformers for the input balun and for interstage matching. It features a virtual ground, the easy realization of Class-B or AB amplifiers and a good cancellation of the 2nd harmonics. There also appears a 4:1 load-line impedance benefit for a push-pull combining scheme in an equal power comparison to a single-ended design. This is an advantageous issue at low supply voltages and eases the design of the output matching network.

2. Circuit Design

Fig. 1 shows the circuit diagram of the power amplifier. The circuit consists of a transformer X1 as input balun, a driver stage T1 and T2, a transformer X2 as interstage matching network and the output stage T3 and T4. The bias of the driver stage and the output stage are set by current mirrors D1 and D2, respectively. The effecitve emitter area of T1, T2 is 21 μm^2 and 155 μm^2 for T3, T4 each.

X1 is connected as a parallel resonant device with the input capacitors C1 and C2. The transformer acts as balun as well as input matching network (Fig. 6). In addition there are several advantages:

- No restrictions to the external DC potential at the input terminals.
- No external DC-block capacitor required.
- The input signal can be applied balanced or unbalanced if one input terminal is grounded.
- Relaxed electrostatic device requirements.
- 50 Ω input matching without any external components.

The turn ratio of X1 is N=2:1. The size is 140 × 140 μm^2. The primary winding consists of 2 turns with a width of 10μm on the top metal layer (Metal 3). Metal 1 and 2 are not used to reduce parasitic substrate coupling of the primary winding. The secondary winding consists of two turns connected in parallel. The total coupling coefficient is k = 0.55 at 5.3 GHz.

Fig. 2 shows the interstage power transformer X2. It is connected as a parallel resonant device with two capacitors

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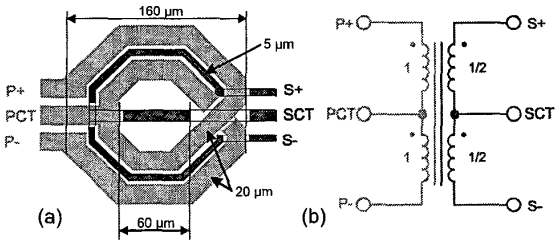

Figure 2. Interstage power transformer X2: (a) Winding scheme (b) Schematic symbol.

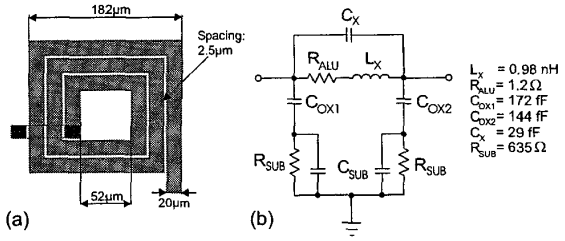

Figure 3. (a) 1nH Coil (b) Equivalent circuit.

C3 and C4. C3 and C4 are connected in antiseries to short the parasitic substrate capacities to the VCCD node. X2 has a turn ratio of N=2:1. The total coupling coefficient is k = 0.45 at 5.3 GHz. The size is $160 \times 160\,\mu m^2$. The primary winding consists of 2 turns with metal 3 and the secondary of 1 turn also using metal 3. Modeling issues of monolithic transformers are presented in [9, 10, 11, 12].

3. On-chip LC-Balun design

During last years several balun concepts have been proposed [13, 14], but most of them result in large structures. The Lattice-type LC-balun [5, 6] is the most compact solution, as it is a solution based on lumped components. Additionally it allows also an impedance transformation and can be realized using transmission lines [15].

The ideal lattice-type balun consists of two inductances $L_A = L_B$ and two capacitors $C_A = C_B$ (Fig. 1). An RF-choke and a DC-block capacitor are used to feed the supply voltage to the collectors. R_1 is the balanced input impedance of the bridge. Each collector is loaded by $R_1/2$. R_L is the load resistance, usually 50 Ω. L and C can be calculated by

$$L_A = L_B = \frac{Z_1}{\omega_1} \quad (1)$$

$$C_A = C_B = \frac{1}{\omega_1 Z_1} \quad (2)$$

where $Z_1 = \sqrt{R_1 \cdot R_L}$ is the characteristic impedance of the bridge. $\omega_1 = 2\pi f_1$ is the frequency of operation.

Unfortunately, the inductance of bond wires [16] at the RF output leads to a complex-valued load impedance. So we use the series circuit of bond-wire and the DC-block capacitor to get approximately a real-valued load (Fig. 6). With the knowledge of this real-valued load, the LC-balun can be designed using equations 1 and 2. Interconnections, inductances and parasitic capacitances will shift the calculated values for L and C. Additionally, bond wires for the power supply feeding have to be considered as well as the interconnect lines at the balun input.

Fig. 3 shows the used coils L_A and L_B.The size is 182 $\times$ 160 μm^2. The winding consists of 2.75 turns. metal 1 and metal 2 are not used to reduce parasitic substrate coupling of the winding. The interconnection uses Metal 1 and 2 to have about the same maximum current density applicable. The inductors are modeled with an in-house tool called Coilgen based on Grovers formula [16] and substrate effects presented in [11, 17]. The equivalent circuit for the used coils L_A and L_B can be found in Fig. 4. Capacitances and DC-block were realized as *m*etal/*i*solator/*m*etal capacitors (MIM-CAPs).

4. Technology

Fig. 4 shows the die photograph of the integrated power amplifier. The die size is 1 x 0.9 mm^2.

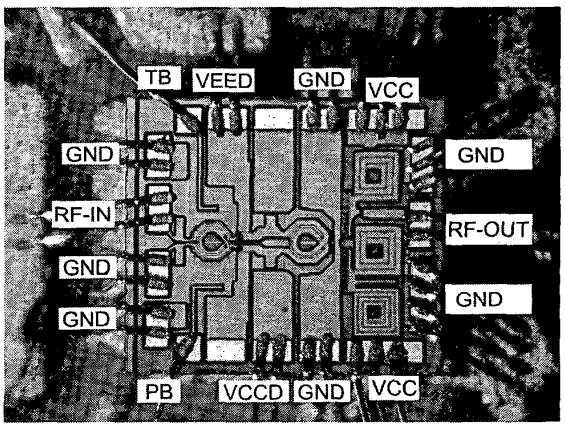

Figure 4. Die photograph of the power amplifier (chip size: $1 \times 0.9\,mm^2$).

The SiGe bipolar technology used in this work is a 0.25 μm, 72 GHz/75 GHz (f_t/f_{max}) volume production process which is described in [7, 8]. The key features of the technology are npn transistors with double-polysilicon self aligned emitter-base-configuration and selective SiGe-epitaxy, a selectivly implanted collector (SIC), trench isolation and 3 metal layers. Further usable devices are a vertical pnp transistor, poly-Si resistors, MIM capacitors and inductors. The worst-case collector-base breakdown voltage is BVCB0 = 8 V (typical: 10 V) and the worst-case

collector-emitter breakdown voltage is BVCE0 = 2.3 V (typical: 2.8 V).

5. Experimental Results

Fig. 5 shows the power amplifier test-board. The substrate parameters are $\varepsilon_r = 3.38$, $\tan\delta = 0.0027$ and the dielectric thickness is 0.51 mm. The metalization layers consist of 18 μm copper with a nickel diffusion barrier and 5 μm gold on top for bonding. The die is attached with a conductive epoxy to the substrate and is bonded directly on the board.

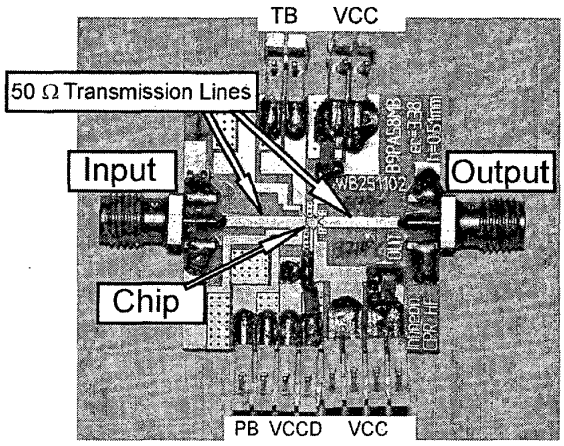

Figure 5. Photograph of the power amplifier test-board (size: $30 \times 30\,\mathrm{mm}^2$).

The input and the output of the amplifier is connected via a 50 Ω microstrip line. The input and output matching of the power amplifier is shown in fig. 6. The power amplifier was characterized operating in a pulsed mode with a duty cycle of 12.5% with a pulse width of 600 μs as well as for CW operation (Tab. I).

Fig. 7 shows the measured power transfer characteristic. The maximum output power is 25 dBm at 2.4 V supply voltage and 5.3 GHz. The maximum PAE is 24%.

Fig. 8 shows the measured power transfer characteristics for supply voltages of 1.0 V, 1.5 V, 2.4 V, 3 V and 2.4 V in continous wave (CW) mode.

Fig. 9 shows the frequency response. The frequency response shows a high PAE and output power level in a frequency range from f = 4.5 GHz to 6 GHz. Tab. 1 shows the performance summary.

6. Conclusion

We have demonstrated a fully integrated power amplifier for 4.8-5.7 GHz in a 0.25 μm-SiGe-bipolar technology. It is based on a push-pull type circuit with on-chip transformer coupling and on-chip output balun. Thus the amplifier does not require any external elements. At a supply

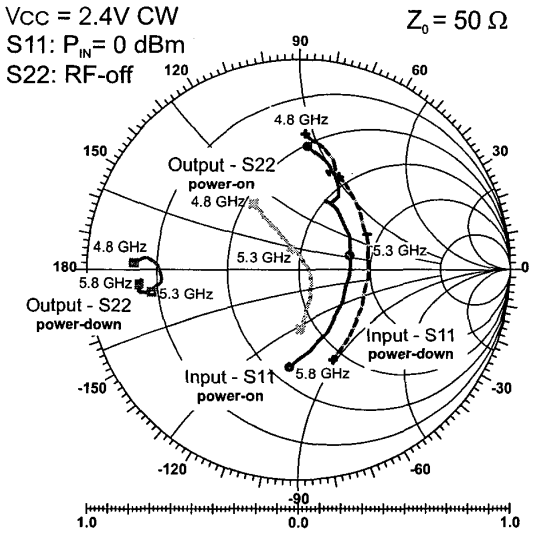

Figure 6. Measured S-Parameters for Input (S11) and Output (S22).

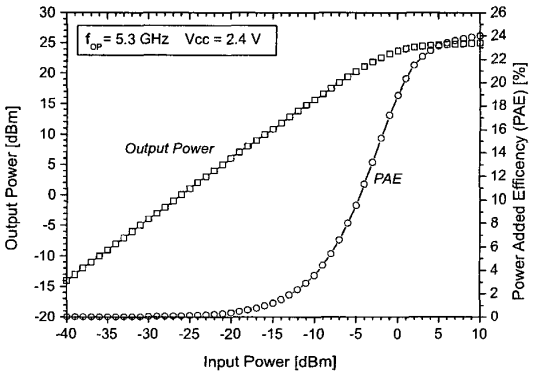

Figure 7. Measured power amplifier transfer characteristic.

voltage of 2.4 V the output power is 25 dBm with a PAE of 24 % at 5.3 GHz. The small signal gain is 26 dB.

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Table 1. Performance Summary (T=300 K, 12.5 % duty cycle, 0.600 ms pulse width - CW: continious wave.)

Operating frequency	4.8 GHz – 5.7 GHz					
Small-signal gain	26 dB					
Supply voltage	1	1.5	2.4	3.0	2.4 CW	V
Maximum output power	17.7	21.6	25	26.6	24.4	dBm
(5.3 GHz, Pin=10 dBm)	(60)	(145)	(316)	(457)	(275)	mW
Power-added efficiency (5.3 GHz, Pin=10 dBm)	15.6	22.5	24	15	22	%
Output stage collector current (RF on) + bias	288 + 6.4	327 + 6.4	443 + 6.4	800 + 6.4	422 + 6.4	mA
Output stage collector current (RF off) + bias	288 + 6.4	321 + 6.4	360 + 6.4	450 + 6.4	370 + 6.4	mA
Driver stage current (RF on) + bias	71 + 4.6	78 + 4.6	96 + 4.6	90 + 4.6	89 + 4.6	mA
Driver stage current (RF off) + bias	26 + 4.6	29 + 4.6	35 + 4.6	36 + 4.6	40 + 4.6	mA

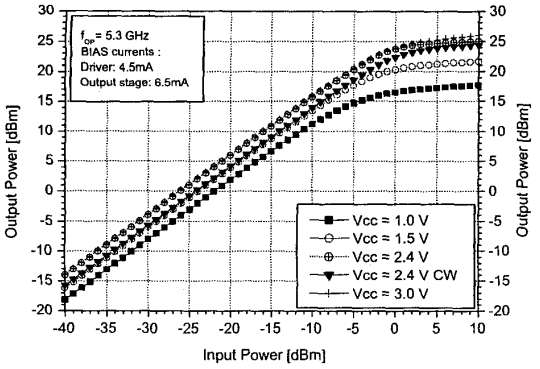

Figure 8. Measured power amplifier transfer characteristic versus supply voltage.

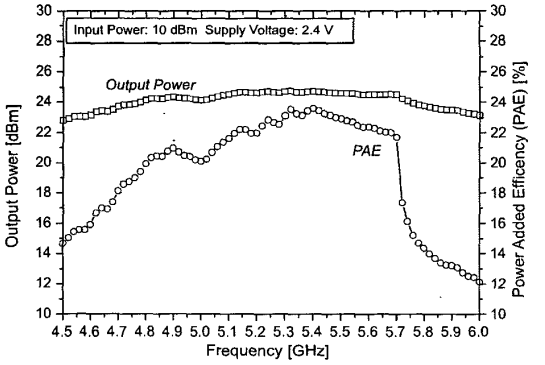

Figure 9. Measured power amplifier frequency characteristic.

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