29.1 A 21 to 26GHz SiGe Bipolar PA MMIC

Tak Shun Dickson Cheung[1], John R. Long[2], David L. Harame[3]

[1]Univesity of Toronto, Toronto, Canada
[2]Delft University of Technology, Delft, The Netherlands
[3]IBM, Burlington, VT

Future wireless broadband networks will utilize integrated circuits that process radio frequency (RF) signals in the 24GHz ISM band to support data services up to 100s of Mb/s. At present, most monolithic microwave ICs (MMICs) are fabricated in technologies that are 3 to 5 times more expensive than silicon (e.g., GaAs or InP). Silicon integration enables new applications incorporating wireless and computing technologies in products affordable to the average consumer.

Implementation of a 24GHz power amplifier in silicon technology is hindered by transmission-line attenuation ranging between 0.5 and 2dB/mm on medium-resistivity silicon substrates. In addition, frequency and voltage-swing limitations of active devices constrain both output power and operating bandwidth. This paper describes a linear IC power amplifier that operates from 21 to 26GHz with approximately 125mW (+21dBm) output power using 1.8V-breakdown (V_{CEO}) 100GHz-f_T SiGe bipolar transistors fabricated on a medium-resistivity (10 to 15Ω-cm) substrate [1]. This 3-stage, single-ended design uses interstage step-down transformers and input/output baluns to optimize the gain in each stage and preserve signal swing, with minimal energy loss to the substrate.

A schematic of the complete power amplifier is shown in Fig. 29.1.1. The desired output power is 21dBm, but 1dB loss in the output balun (T6) and 0.5dB loss between bondpad and circuit board raises the output requirement to 22.5dBm. Limited by the 1.8V breakdown of the SiGe HBTs, a common-emitter transistor operating from a 1.3V supply requires a 2.5Ω load to deliver 23dBm output power. Instead, a common-base configuration with ~4V breakdown is used. A 4-way monolithic balun (T6) transforms the 50Ω load to four 7Ω loads at the output stage.

Three stages of amplification (approximately 6dB small-signal gain/stage) provide 15dB gain at 1dB gain compression per stage, and the amplifier produces full power with a 6dBm RF input. Transistors in the 3 stages could be sized 1:4:16 in area, however, the oversized input stage allows higher DC bias current to control the input impedance for matching purposes. Consequently 1:3:12 sizing is used. To counter localized heating, the transistors are divided into 10×0.2μm² emitter-area units: Q5 to Q12 with 2 units each, Q13 to Q20 4 units, and Q21 to Q24 8 units. The base of each unit is connected to its differential counterpart to form a virtual ground for common-base operation, but the base terminals are not joined together within the same transistor. A ballast resistor of 39Ω (not shown in Fig. 29.1.1) is added in series with the base to provide negative common-mode feedback without degrading the performance of the differential amplifier. To operate at reduced output power, stages can be partly biased class-B via bias control lines V3a-c and V2a-b while the remainder operate at optimal f_T. For testing, the first stage is biased in class-A for optimal gain, while the final stage is class-AB for optimal efficiency.

The optimum collector load for each stage is higher than the input impedance of the following stage, therefore an interstage step-down transformer (2:1 as drawn turns ratio) is used to maximize power transfer. The low-voltage secondary coil (emitter side) of the transformer forms a self-shielding structure around the higher-voltage primary coil (collector side) to minimize substrate loss and skin effect [3]. This realizes a high magnetic-coupling factor (i.e., k>0.85) using just a single-turn secondary to handle up to 400mA DC current. The transformers are scaled in width to account for changes in current density and parasitic capacitance of the transistors used in each stage.

The input and output baluns are identical. At the input, a shielded differential transmission line [4] connects the input balun to the first gain stage. Grounding the center-taps for both baluns is important to achieve good balance between the differential outputs. The balun turns ratio is selected to match the amplifier to a 50Ω source and load. Separate grounds are used for input and output stages to improve isolation.

The amplifier gain, output power and power-added efficiency (PAE) versus input power at various frequencies are shown in Fig. 29.1.2. Small-signal gain is approximately 20dB. For the 3 frequencies shown in Fig. 29.1.2, PAE exceeds 10% at –3dB gain compression. The maximum PAE of 19.7% is obtained at 22GHz, while PAE at 24GHz is 13% (max). The saturated output power, maximum PAE and corresponding gain versus frequency are plotted in Fig. 29.1.2. Peak output power of 23dBm is achieved at 22GHz, and over 20.8dBm output power is available between 20 and 25GHz. PAE exceeds 12.5% between 20.3 and 24GHz. When biased at 230mA (i.e., with no RF signal applied), there is less than 3dB reduction in gain, output power and slightly lower PAE, despite the transistor g_m being reduced by half for all 3 stages.

The small-signal gain and isolation are plotted in Fig. 29.1.4. The gain is approximately 19dB from 21 to 26GHz. Isolation is excellent, exceeding -30dB from 20 to 30GHz. Insertion loss (~1dB) of a 1.5" coplanar waveguide (CPW) thru-line in the same fixture used to characterize the amplifier is also plotted in Fig. 29.1.4. It is used to de-embed the measured performance in Fig. 29.1.2 and Fig. 29.1.3. The intermodulation distortion from a two-tone test at 24GHz (see Fig. 29.1.5) gives an OIP_3 of +23dBm, after 2dB losses in the interconnect cables and test fixture are accounted for.

A photomicrograph of the testchip and test fixture are shown in Fig. 29.1.6 and Fig. 29.1.7. Double stud bumps are used to increase separation to 60μm between the testchip and underlying circuit board when flipchip mounted into the test fixture. The input and output interfaces between K-connectors and the testchip are via CPW on a RO4350 0.5oz copper-clad circuit board. The transformers transfer heat effectively from both the collectors and emitters of the transistors via the 4 V_{cc} and 16 ground stud bumps to the underlying PCB. No heatsink was used during testing.

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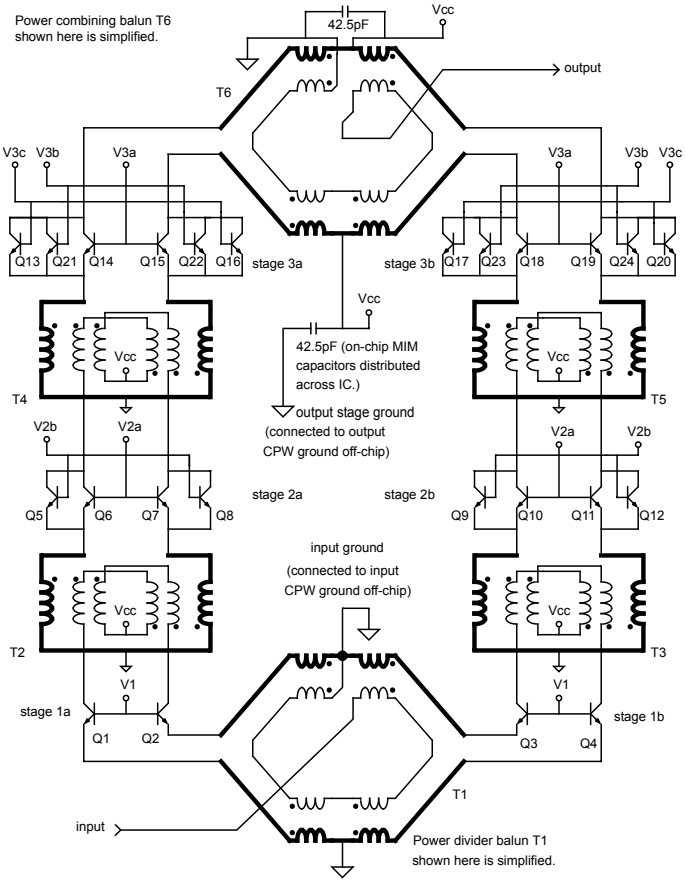


Figure 29.1.1: Power amplifier schematic diagram.

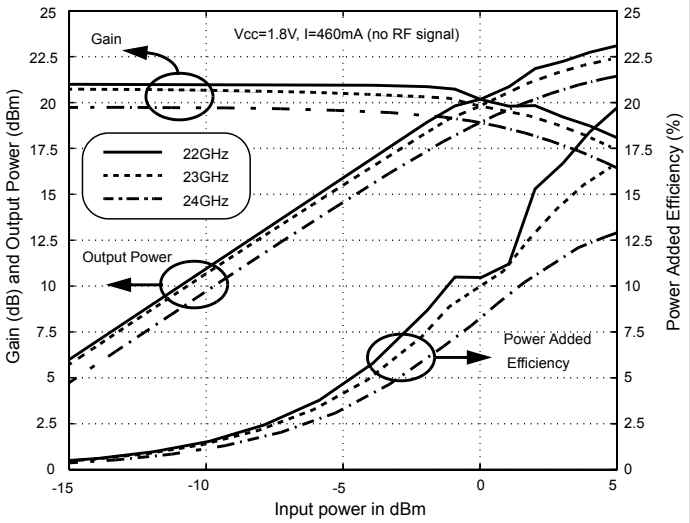


Figure 29.1.2: Gain, output power and power-added efficiency versus input power.

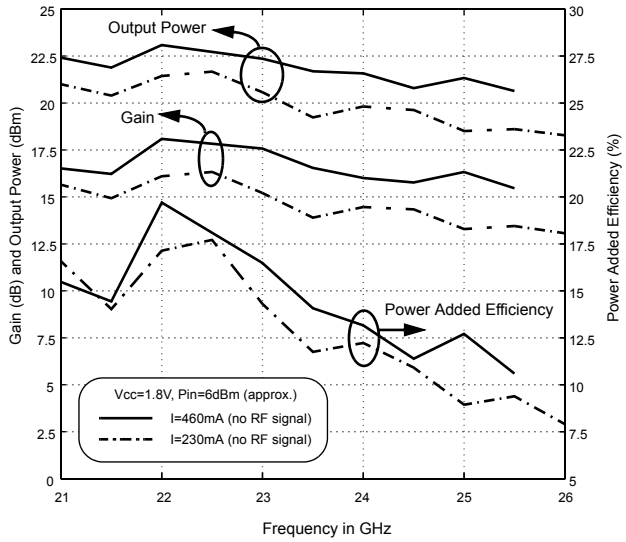


Figure 29.1.3: Gain and efficiency under maximum output power versus frequency.

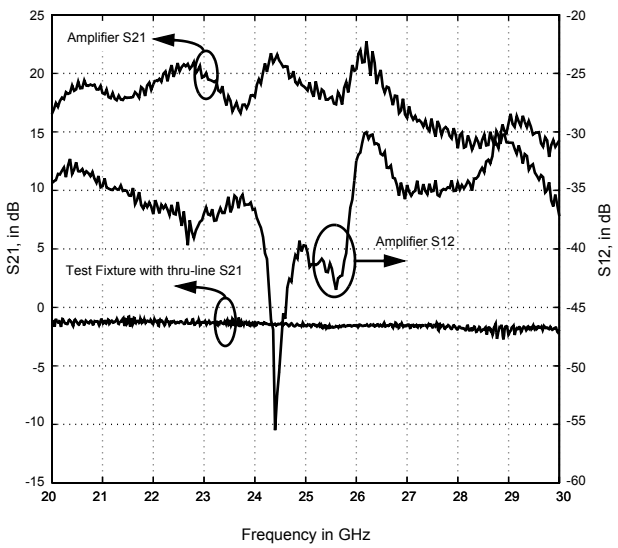
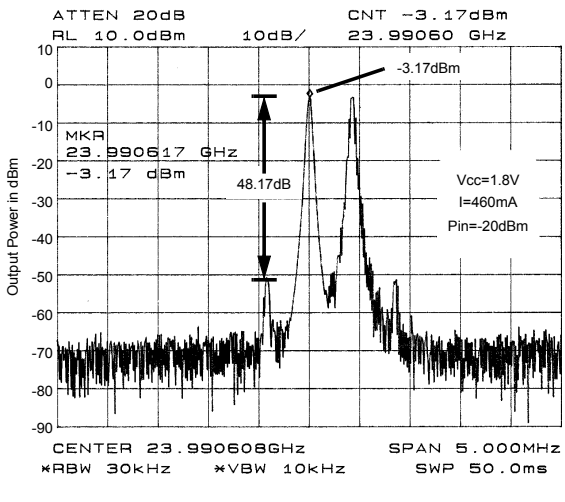


Figure 29.1.4: Measured S21 and S12 for the fixtured power amplifier.



Note: Test fixture and cable loss not deembedded

Figure 29.1.5: Two-tone test result at 24GHz.

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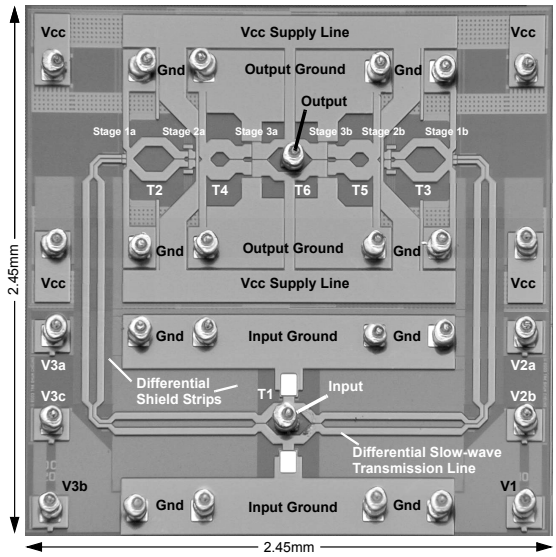

Figure 29.1.6: SiGe power amplifier chip micrograph.

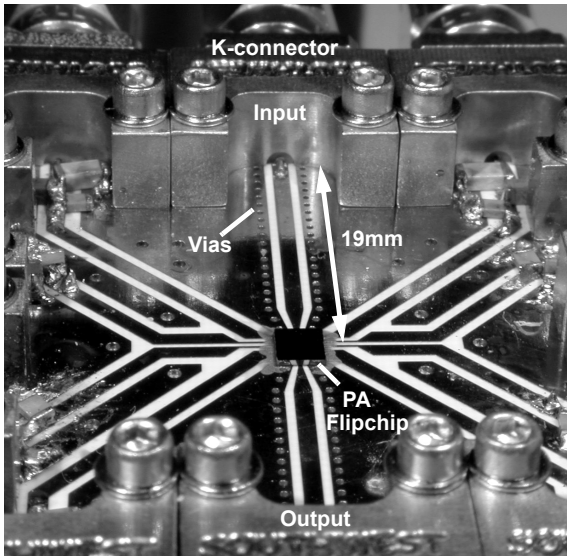

Figure 29.1.7: Power amplifier flipchip mounted in the test fixture.

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