A CMOS Power Amplifier With Integrated-Passive-Device Spiral-Shaped Directional Coupler for Mobile UHF RFID Reader

Sunbo Shim, *Student Member, IEEE*, and Songcheol Hong, *Member, IEEE*

***Abstract*—A CMOS power amplifier (PA) with a compact spiral-shaped directional coupler for a mobile UHF RF identification (RFID) reader is proposed here, and its output power combiner and the directional coupler are implemented using an integrated passive device process. The two-chip solution not only enables a CMOS PA to be highly efficient, but also allows the directional coupler and the power combiner to be mounted in a compact standard package. A polar transmitter is implemented using the CMOS PA with the directional coupler to verify the operation of the proposed configuration for a UHF RFID reader. Measurements indicate that the CMOS PA with the directional coupler transmits 27.3 dBm of output with 44.6% of power-added efficiency and that the implemented polar transmitter satisfies the required UHF RFID reader specifications.**

***Index Terms*—CMOS power amplifier (PA), directional coupler, integrated passive device (IPD), polar transmitter, power combiner, RF identification (RFID).**

I. Introduction

MOBILE UHF RF identification (RFID) systems, which cover the frequency range from 860 to 960 MHz, utilize electromagnetic (EM) waves to transfer and receive data between a tag and a reader for identification. The integrated reader in a mobile terminal first activates passive tags, detects backscattered signals from the tags, and then recognizes the properties of the objects that contain the tags.

One of the essential issues of mobile UHF RFID is to integrate the reader system in a single-chip using a CMOS process. CMOS technology enables reader system integration with high yield, low power consumption, and low manufacturing cost. Fig. 1 shows a conventional UHF RFID reader front-end system that has the direct-conversion transceiver structure. According to previous papers [1]–[3], it is possible to integrate a large portion of a UHF RFID reader system in a single CMOS chip, excluding an antenna, a power amplifier (PA), and a circulator.

Manuscript received March 10, 2011; revised July 27, 2011; accepted August 05, 2011. Date of publication September 26, 2011; date of current version November 16, 2011. This work was supported in part by the National Research Foundation of Korea (NRF) under the Basic Science Research Program funded by the Ministry of Education, Science and Technology R11-2005-029-04001-0 (2009) through the Intelligent Radio Engineering Center, and by Samsung Electro-Mechanics.

The authors are with the School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: xim5un80@kaist.ac.kr).

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Digital Object Identifier 10.1109/TMTT.2011.2165962

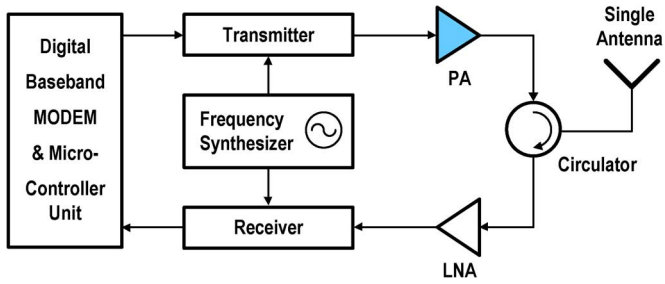


Fig. 1. Conventional UHF RFID reader RF front-end.

Although improved performances of CMOS PAs have recently been reported in the literature [12], [16], it is still unavoidable that a fully integrated PA using standard CMOS technology undergoes a degradation of power-added efficiency (PAE) due to the low quality factor of on-chip inductors or transformers, which are fabricated on a moderately conductive silicon substrate, especially when those passive components are used for output impedance matching circuits. Typically, in the case of a UHF RFID reader, an external PA based on a compound semiconductor process, such as InGaP/GaAs, has been used in the form of a discrete module.

A circulator, which is a three-port microwave component and contains ferrite material with high magnetic permeability, is usually expensive and bulky. It is known that a circulator can be substituted with a directional coupler, which is fabricated on a relatively inexpensive printed circuit board (PCB), for use in UHF RFID reader applications. Nonetheless, its size is still too large to be integrated in a compact package.

In this paper, we propose a spiral-shaped directional coupler in a compact size using an integrated passive device (IPD) process on a highlyvresistive substrate. An IPD directional coupler for a UHF RFID reader was first introduced in [6] with notable isolation at 912 MHz using lumped components, but that configuration suffers from insertion loss higher than 1.1 dB. The compact directional coupler proposed in this work demonstrates relatively low insertion loss and sufficient isolation through the frequency range of interest for UHF RFID reader applications. Additionally, a power combiner for a CMOS PA is also implemented on the same IPD substrate, and it combines the output power from two pairs of a differential PA and performs an impedance transformation from low impedance to 50 Ω. The proposed RF front-end architecture for a UHF RFID reader is shown in Fig. 2. It is revealed that the overall PAE of a CMOS PA can be improved by designing the

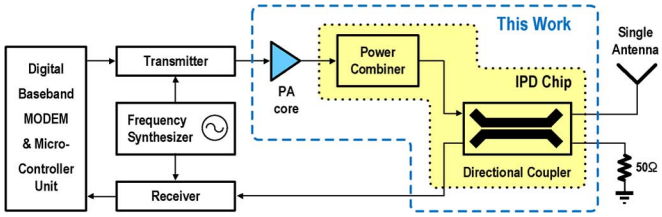


Fig. 2. Proposed UHF RFID reader RF front-end.

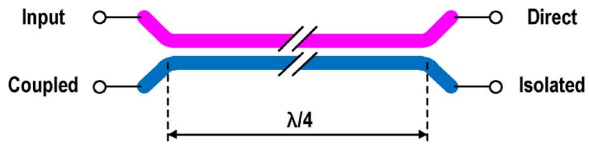


Fig. 3. Conventional parallel-coupled directional coupler.

output matching components using the IPD process [8]–[11]. The designed module, including the CMOS PA and the compact directional coupler, is applied to a polar transmitter for a UHF RFID reader, as described in [11] and [12], for the further improvement of power efficiency of the overall transmitter.

This paper is organized as follows. The specifications of a directional coupler for UHF RFID readers are examined in Section II. Section III describes the proposed spiral-shaped directional coupler. Section IV covers the circuit implementation of the transmitter and the CMOS PA for mobile UHF RFID readers. Section V presents a single chip that includes the proposed directional coupler and the power combiner for a CMOS PA on an IPD substrate. Measurement results are discussed in Section VI. Section VII concludes this paper.

II. Specifications of Directional Coupler for UHF RFID Reader

Fig. 3 shows the diagram of a conventional directional coupler. It is a four-port component with input, direct, coupled, and isolated ports. Usually, it is applied to a UHF RFID reader with the input port connected to the output of a PA, the direct port connected to an antenna, the isolated port connected to the input of a receiver, and the coupled port connected to a 50-Ω resistor.

To be adopted in UHF RFID reader applications, the following parameters should be considered for a directional coupler: coupling factor, insertion loss, and isolation. The coupling factor of a directional coupler in an RFID reader is related to the required noise figure of the receiver and the insertion loss of the transmitter between the PA and antenna. According to the link budget analysis in [1], the minimally detectable power level at a reader antenna is about -53 dBm for the recognition distance of 1 m between a tag and a reader when the one-tone output power is 27 dBm. Since the link loss in the air for 1 m range is about -31 dB, the received power at a tag is about -4 dBm, which is much higher than the sensitivity of a state-of-the-art tag (-18.5 dBm) [5]. The output power of the modulated backscattering signal from a tag is -22 dBm, provided that the tag antenna gain is 2 dBi and the reflected power from a tag antenna is only 1%.

The minimally detectable power at the receiver input $(P_{\mathrm{min,det,RX}})$ of a UHF mobile RFID reader is calculated by the addition of the coupling factor of the directional coupler (C) and the minimally detectable power at the antenna $(P_{\mathrm{min,det,ant}})$ because the coupling factor, which has $(-)$ notation, acts like insertion loss in the receiver link chain. Unless the receiver sensitivity limits the communication range between a tag and reader, the following inequality should be fulfilled:

$$P_{\mathrm{min,det,RX}}(\mathrm{dBm}) = P_{\mathrm{min,det,ant}}(\mathrm{dBm}) + C(\mathrm{dB}) > \mathrm{Sensitivity}. \quad (1)$$

The receiver sensitivity can be obtained using the following equation:

$$\mathrm{Sensitivity(dBm)} = -174 + \mathrm{NF} + 10\log \mathrm{BW} + \mathrm{SNR_{min}}. \quad (2)$$

It is assumed that the noise bandwidth of the receiver is 120 kHz at the data rate of 40 kb/s and that the minimum required signal-to-noise ratio $(\mathrm{SNR_{min}})$ is 11.6 dB for the bit error rate of 0.001% [1], [15]. The reported performance in previous literature for UHF RFID readers [1]–[4] shows that the noise figure of the receiver chain at the normal mode is about 32–39 dB. Consequently, the coupling factor, C, should be more than -19.6 dB, according to the worst case estimation of the noise figure at a receiver.

However, as the coupled power of a directional coupler is increased, the insertion loss from the input port to the direct port through the forward path is also increased. For example, in the case of -15-dB coupling, the minimum insertion loss is 0.14 dB because at least 3.16% of the total power is delivered to the coupled port if no power is detected at the isolated port. When the coupling factor is -10 dB, the minimum insertion loss becomes 0.46 dB. In practice, ohmic loss through metal lines, capacitive coupling to the substrate, and the nonzero isolation of a directional coupler increases the insertion loss. Thus, taking account of the tradeoff between the required noise figure at the receiver and the insertion loss at the transmitter, we determine the targeted coupling factor of the directional coupler to be from -16 to -18 dB. To decrease the insertion loss, it is desirable to lower the coupling factor of a directional coupler so long as the required noise figure of the receiver is not so tight to meet the sensitivity specification of a UHF RFID reader.

The high isolation of a directional coupler for a UHF RFID reader is necessary for the suppression of transmitter power leakage into the receiver. In the case of a passive RFID system, a reader should send a continuous-wave (CW) signal to power-up passive tags. If the isolation performance of the directional coupler is limited, some portion of the transmitted CW signal is directly leaked to the receiver of the reader and causes the saturation of the receiver as a self-jammer, which is usually called blocking. For this reason, the RFID receiver circuit is generally designed to have a high $P_{1\ \mathrm{dB}}$ point for normal mode operation (the listen-before-talking mode operation will not be dealt with in this study). This can be achieved by bypassing a low-noise amplifier (LNA) and utilizing a highly linear down-conversion mixer, such as a passive mixer. According to the implementation of the receiver for the UHF RFID reader in [1], it is possible to design a receiver circuit with 8 dBm of $P_{1\ \mathrm{dB}}$.

Based on the linearity analysis in [4], it is recommended to make the $P_{1\ \mathrm{dB}}$ of the receiver at least 6 dB larger than the power

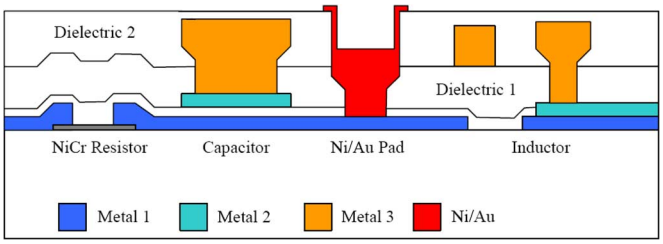


Fig. 4. Layers of IPD process [8].

of the self-jammer so as to prevent the receiver from desensitization or blocking conditions. Therefore, if the output power of the PA is 27 dBm, the maximum allowable power level at the input port of the receiver against the blocking condition caused by self-jamming is 2 dBm and the required isolation of the directional coupler for the UHF RFID reader should be higher than 25 dB for the entire UHF RFID band.

III. Spiral-Shaped Directional Coupler

When a directional coupler is implemented on PCB in the form of two parallel-coupled microstrip lines, as shown in Fig. 3, it becomes too bulky, as large as a quarter-wavelength $(\lambda/4)$ line, which has the magnitude of several centimeters.

To make a small-sized directional coupler, one can choose microfabrication technology, instead of fabrication on PCB. The IPD process, which is a specialized microfabrication technology for building passive circuit elements, can be a good candidate approach to implement a compact directional coupler. Fig. 4 shows the layer stack-up of the IPD process, as provided by the Samsung Electro-Mechanics Corporation [8]. It features a thicker top metal layer than that of the commercial CMOS process, and has a 10-μm thickness of copper and a highly resistive silicon substrate. A spirally wound metal line on a highly resistive substrate can obtain a targeted inductance with shorter length than that on a conductive substrate due to the reduction of the eddy current. Besides, the occupied area of a directional coupler can be dramatically reduced by changing its form from a parallel shape to a spiral shape.

Fig. 5 illustrates the layout diagram and circuit symbol of the proposed directional coupler. Its structure is derived from a transmission-line transformer with two spirally coupled lines. The design procedure is as follows. First, two metal lines interwound with a small space between the primary side and the secondary side are placed and the S-parameters are extracted by EM simulation. Second, a capacitor, C_1, is inserted between the two ports of the secondary side. Next, an additional capacitor, C_2, is inserted between the two ports of the primary side to form an LC tank. Finally, additional shunt capacitors (C_3 and C_4) for impedance matching are placed, as shown in Fig. 5(b).

A large capacitor (C_1) attached between the isolated port and coupled port at the secondary side increases its effective electrical length with much shorter physical length than $\lambda/4$ [17], and enhances the isolation from the input port to the isolation port at the secondary side, whereas only a relatively small amount of the power at the coupled port is reduced. Note that the direction of the directivity is reversed, i.e., to forward-wave coupling, by the addition of the large capacitor at the secondary

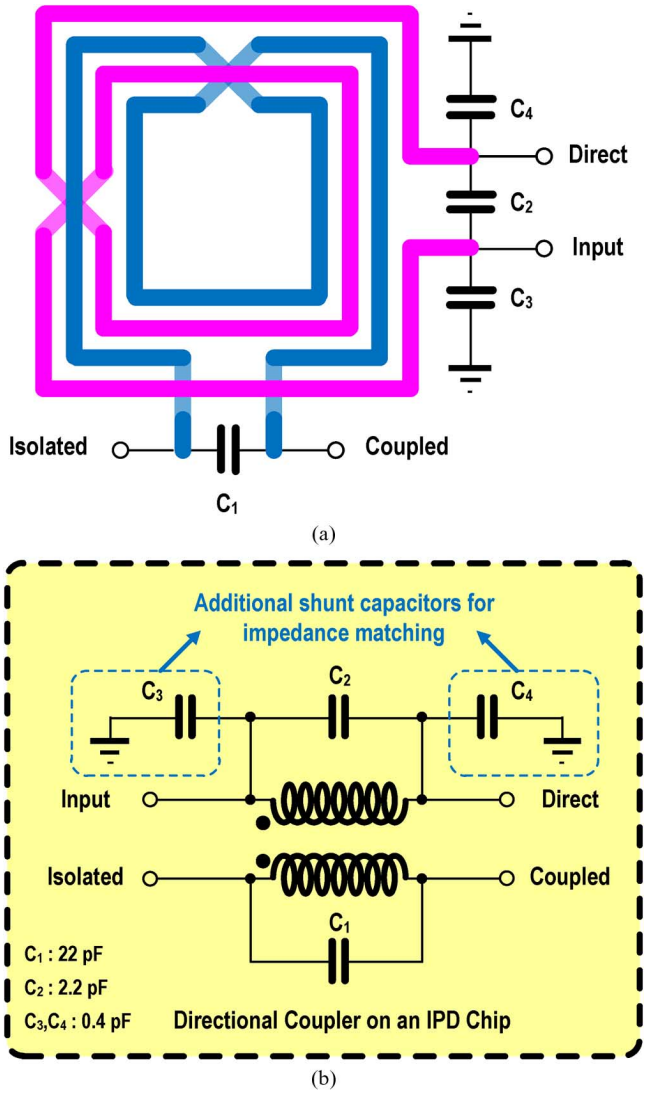


Fig. 5. Proposed spiral-shaped directional coupler. (a) Simplified layout. (b) Schematic symbol.

side, compared with the direction of the isolated port and the coupled port of the conventional directional coupler, which is based on backward-wave coupling, as shown in Fig. 3.

Fig. 6 shows the shift of the coupling and the isolation with respect to the variation of the capacitor C_1. Although the frequency at the null point is not, strictly speaking, inversely proportional to the capacitor value, its tendency implies that the lowest point of the isolation moves down to low frequencies as the capacitor value is increased, contrary to only a small change of the coupling.

Fig. 7 shows the lumped circuit model of the proposed directional coupler. The spirally oupled lines are considered to be equivalent to the low-order model of the 1:1 transformer. The total coupling coefficient of the transformer k is 0.6. Other parameters extracted from the lumped-circuit modeling are shown in Table I.

The placement of the capacitor (C_2) at the primary side between the input port and direct port inserts a zero in the frequency response, aiming for notch filtering of the second harmonic component of the fundamental frequency, which

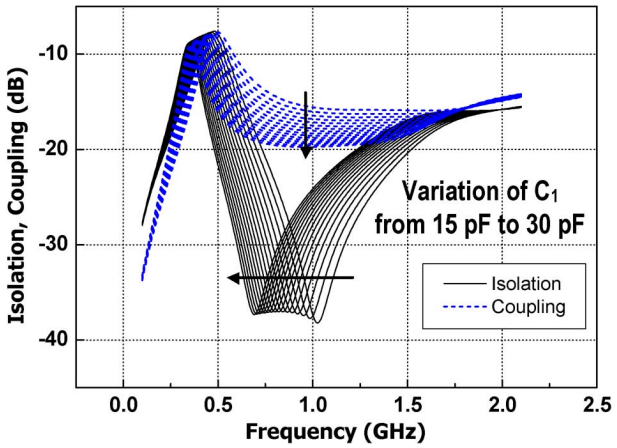


Fig. 6. Simulated coupling and isolation with respect to the variation of capacitor value (C_1) of the proposed spiral-shaped directional coupler.

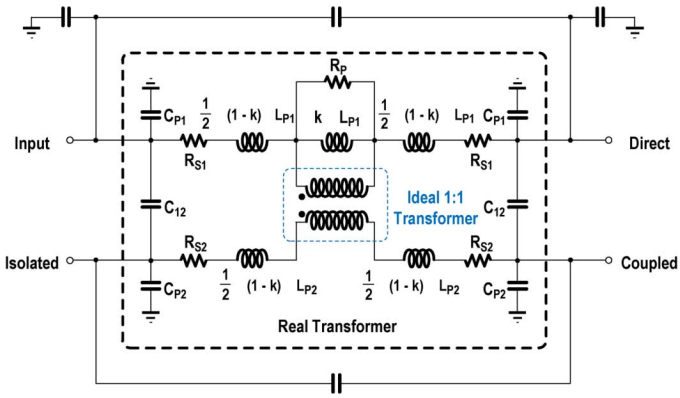


Fig. 7. Lumped model of the spiral-shaped directional coupler.

TABLE I
PARAMETERS FROM EXTRACTION OF LUMPED-CIRCUIT MODEL

Symbol	Quantity	Extracted value
k	Coupling coefficient	0.60
L_{P1}	Inductance of primary side (nH)	5.48
L_{P2}	Inductance of secondary side (nH)	6.24
R_{S1}	Parasitic series resistance of primary side (Ω)	1.02
R_{S2}	Parasitic series resistance of secondary side (Ω)	0.48
R_{P1}	Parasitic shunt resistance of primary side (Ω)	820
C_{P1}	Parasitic cap. to substrate at primary side (pF)	0.12
C_{P2}	Parasitic cap. to substrate at secondary side (pF)	0.086
C_{12}	Parasitic cap. between primary and secondary side (pF)	0.23

will be discussed in detail in Section V. The induced inductance through the main line (input-direct) and the capacitor C_2 performs a parallel *LC* tank to reject a certain frequency component, as described in Fig. 8.

Additional capacitors (C_3, C_4) are used for precise impedance matching to 50 Ω at the input port and the direct port, as depicted in Fig. 5(b). The impedance of the input port (or direct port) approaches 50 Ω after placing C_3 and C_4, as shown in Fig. 9. The insertion loss was improved by 0.1 dB after the placement of C_3 and C_4 according to the simulation. Note that S-parameter at the input port and the direct port of the designed directional coupler are almost the same due to the

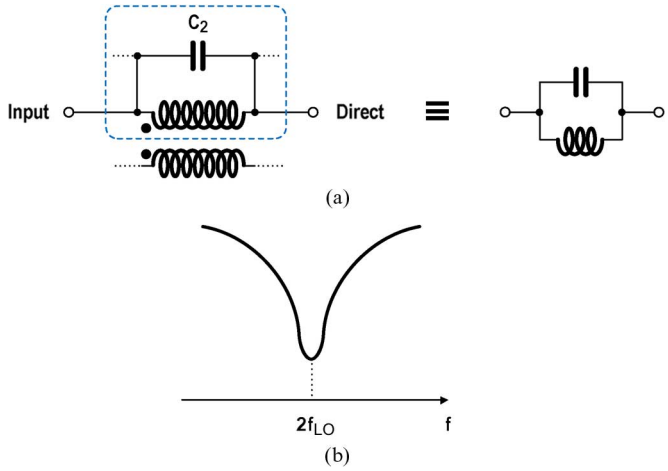


Fig. 8. Second harmonic rejection by a zero insertion. (a) Part of the forward path in schematic symbol of the proposed directional coupler and its equivalent circuit. (b) Notch filtering effect.

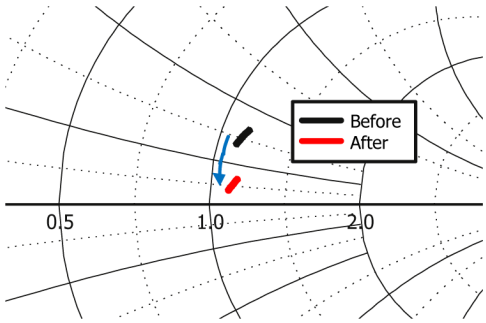


Fig. 9. S-parameter at the input (or direct) port of the directional coupler.

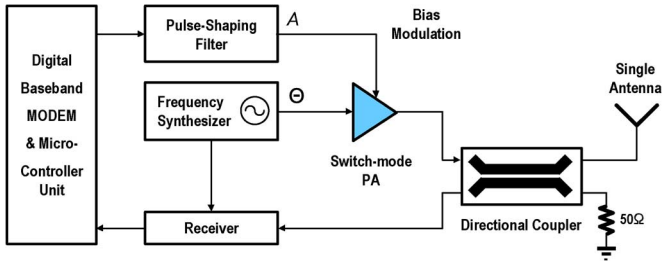


Fig. 10. Polar transmitter architecture for UHF RFID reader.

symmetric structure of the directional coupler. The capacitance values of C_2, C_3, and C_4 are much smaller than that of C_1, and do not make substantial effects on the isolation. The direction of each port in the layout is determined through the consideration of the actual placement of a CMOS transceiver chip and the directional coupler.

IV. TRANSMITTER AND CMOS PA

A. Polar Transmitter Architecture for UHF RFID Reader

In a typical mobile UHF RFID reader system, direct up-conversion transmitter architecture with in-phase/quadrature (I/Q) modulation is prevalently used to support amplitude shift keying (ASK) as a modulation scheme. However, power efficiency degradation is inevitable due to the usage of a highly linear PA. Such degradation causes a serious problem by reducing the

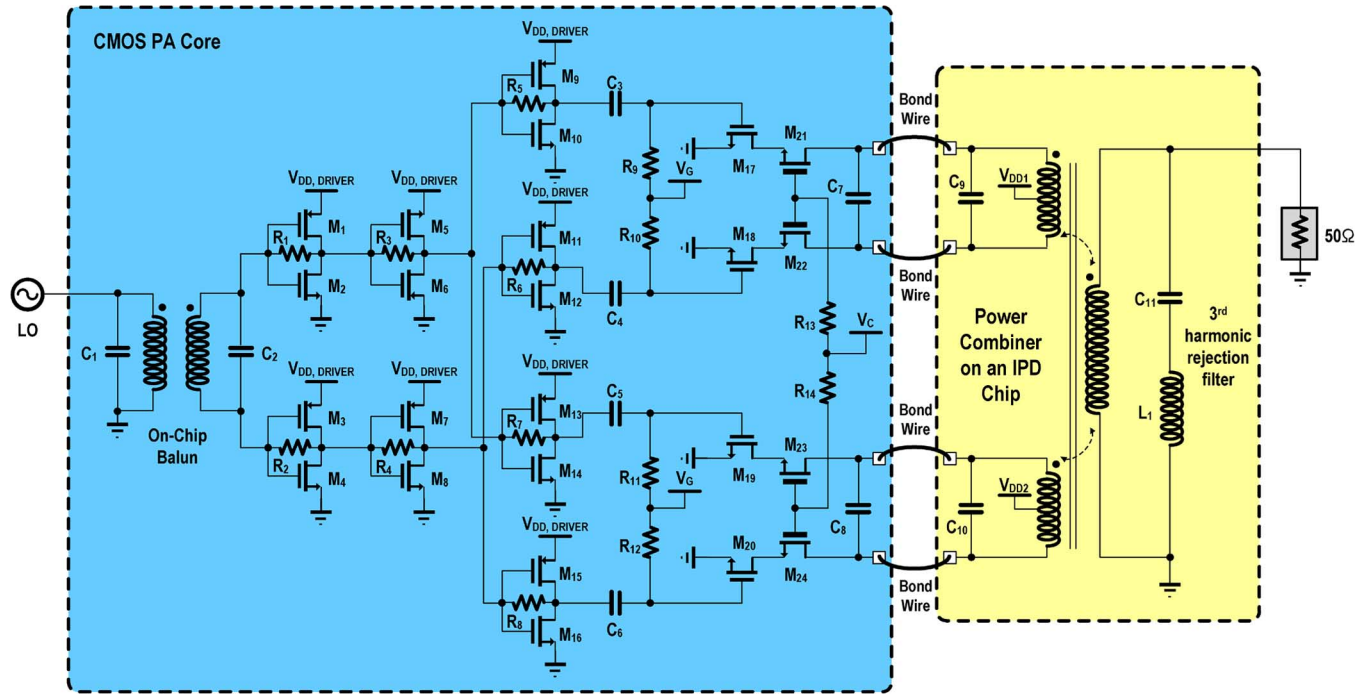


Fig. 11. Schematic of CMOS PA.

battery life of a mobile handset terminal containing an RFID reader chip.

Polar transmitter architecture adopting a nonlinear switch-mode PA for a UHF RFID reader, which is proposed in [12], has some advantages over direct up-conversion transmitter architecture. First, it is able to transmit the output power more efficiently. Generally, a switch-mode PA is more power efficient than a linear PA because it is optimally designed to transmit an output power at a saturated level. Fig. 10 shows the polar transmitter architecture that is applicable to a mobile UHF RFID reader. The utilization of a switch-mode PA in the polar transmitter contributes to the improvement of power efficiency of the overall RFID reader transmitter. In particular, the enhancement of efficiency is maximized when a transmitter provides a one-tone CW signal for a long period of up to a few hundreds of microseconds to activate passive tags between baseband signals, such as "select" and "query" commands since a switch-mode PA can deliver a saturated output power with a better efficiency than a linear PA. An additional advantage of polar transmitter architecture is that it simplifies the circuit constitution of a transmitter. As shown in Fig. 10, the raw data to be transmitted is pulse shaped at an analog low-pass filter before the bias modulation of PA so that the output spectrum of the PA can be controlled not to violate the spectral mask regulation. If the direct up-conversion transmitter structure with I/Q modulation is employed for a UHF RFID reader, the occupied area on a die should be increased to contain two digital-to-analog converters, two mixers, and an additional analog low-pass filter.

B. Switch-Mode CMOS PA

Fig. 11 illustrates the overall schematic diagram of the designed CMOS PA. The PA core chip including the input balun, driver stage, and power stage is designed using a 0.18-μm RF CMOS process. The power stage consists of two pairs of differential cascode amplifiers. The amplified differential signals of each pair are summed up in an in-phase manner at a power combiner, which is fabricated in an IPD process.

The on-chip input balun converts the single-ended signal from an external instrument, for example, an Agilent E4438C signal generator, into differential signals for a measurement. It can be excluded in actual implementation of the overall CMOS transceiver chip because the carrier signal is provided from other circuit blocks on a die, such as a local oscillator or a phase-locked loop, as a form of differential signals.

The driver stage is comprised of three stages of driver amplifiers. The inverter-like driver amplifier has a feedback resistor between the input and output for the stable operation of the rail-to-rail voltage swing. Each driver amplifier is self-biased to almost the center point between the $V_{DD,\mathrm{DRIVER}}$ and GND both at the input and the output by means of determining the proper size ratio of nMOS and pMOS transistors. More stages can be augmented to further increase power driving into the power stage. DC blocking capacitors are not attached between the stages of the driver amplifiers to save the area that would otherwise be occupied by metal–insulator–metal (MIM) capacitors on a die.

The power stage consists of two pairs of differential amplifiers with cascode configuration by stacking the common-source (CS) 0.18-μm-gatelength transistors with thin gate oxide and the common-gate (CG) 0.35-μm-gatelength transistors with thick gate oxide. The nominal supply voltages of these transistors are 1.8 and 3.3 V, respectively. Fig. 12 indicates the simulated waveforms of the drain–source voltage of a CS and CG transistor at the power stage. This reveals that each device in the power stage operates in a marginally safe region from excessive voltage stress since it is known that nMOS devices used

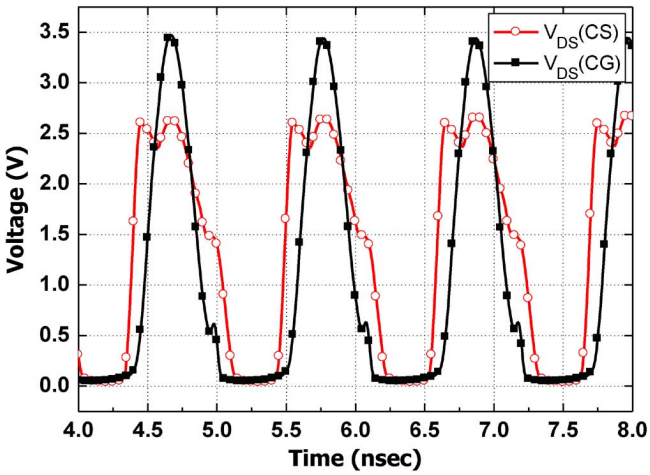


Fig. 12. Simulated voltage waveform of power stage (Freq. = 910 MHz, $P_{\rm IN} = 5$ dBm, $V_{DD1,2} = 2.5$ V).

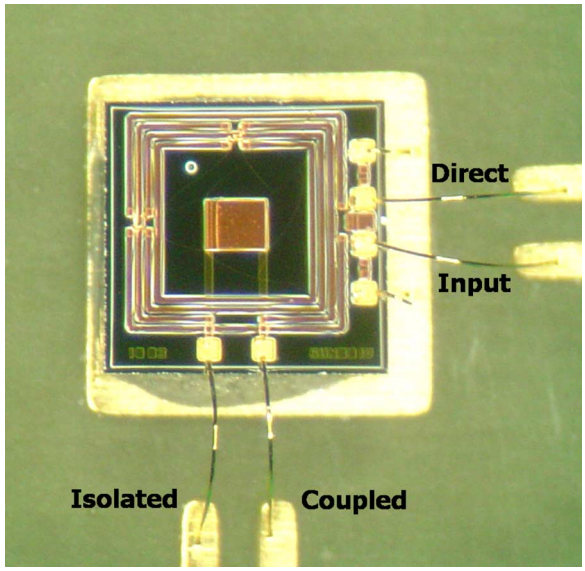


Fig. 13. Photographs of the proposed spiral-shaped directional coupler on an IPD chip.

as power transistors can endure about twice the nominal supply voltage [16]. Although it is possible to increase the drain–source voltage swing of each transistor as high as the limitation allows by changing the load impedance seen at each drain of CG transistors or increasing the size of the transistors, a reliable operation is preferable to avoid the voltage breakdown due to an instantaneous voltage peak from voltage standing wave ratio (VSWR) problems. The gate voltage of the CS transistors, V_G in Fig. 11, is determined as offering the appropriate condition for class-E operation through careful inspection of the transistor size and capacitance value of C_7 and C_8. The gate voltage of the CG transistor, V_C, is fixed to near $V_{DD1,2}$ for the operation of the switch-mode PA to transmit a one-tone CW signal. When the PA transmits an envelope-varying amplitude shift-keying (ASK) signal, the pulse-shaped analog input signal is introduced at V_C through a baseband modem and a low-pass filter and then directly modulated by the carrier signal at the power stage.

The power combiner implemented using the IPD process plays a role of transforming from low impedance to 50 Ω, combining power generated from two pairs of differential amplifiers at the power stage, and converting differential signals to be single ended, based on the parallel-combining transformer (PCT) technique [8], [16]. The structure of a 2 × 1:2 transformer is adopted to combine the power of two pairs of differential amplifiers effectively in a compact area. Since the magnetically coupled metal traces on a highly resistive IPD substrate acquire targeted inductance with less loss than passive elements of a standard CMOS substrate, the PAE of a PA using it is increased significantly. Series connection of the capacitor (C_{11}) and the inductor (L_1) not only contributes to the impedance matching, but also reduces the third harmonic component at the output of the PA by forming a path to the GND like a notch filter.

V. IPD Chip Including Directional Coupler and Power Combiner

There are some advantages of integrating a directional coupler and a power combiner of a PA on a single IPD chip. First, the total occupied area of the implemented UHF RFID reader system can be significantly reduced by integrating all required blocks, except for an antenna in one standard package. No additional external components are needed other than bypass capacitors to the GND at the supply or bias paths. Second, the manufacturing cost can be decreased. Instead of expensive laminate PCB for packaging, a compact standard package can be used for this two-chip solution. Especially, a PA, which accounts for a large portion for the total bill of materials in an RFID reader system, is able to be unified into a single CMOS transceiver chip with only a small area on a die through such integration. Third, the overall power efficiency of the transmitter can be increased by using the IPD process. In particular, the RF signal amplified by a PA is critical to losses because only a small percent of loss can lead to significant power consumption by heat. Components on an IPD achieve a notably low loss with high power capability even after a PA block. Finally, the embedded parallel *LC* tank in the main line of the proposed directional coupler can reduce the second harmonic component from the CMOS PA to some extent. According to [8], the second harmonic of a CMOS PA is caused by the gate capacitance of CS transistors at the power stage when the differential signals swings in turn. To resonate out the effect, center-tapped inductors are required in the CMOS region where chip real-estate is costly. The usage of the directional coupler after a CMOS PA naturally filters the second harmonic from the PA by selecting the series capacitance at the forward path of the directional coupler without increasing the CMOS region.

VI. Measurement Results

Fig. 13 shows a chip photograph of the spiral-shaped directional coupler implemented in the IPD process. The chip area is 1.4 mm × 1.4 mm. The S-parameters of the directional coupler are extracted from a four-port vector network analyzer with the effect of the metal lines on the test fixture de-embedded. The bond-wire effect is included in the measurement of the performance for the consideration of the actual implementation of the

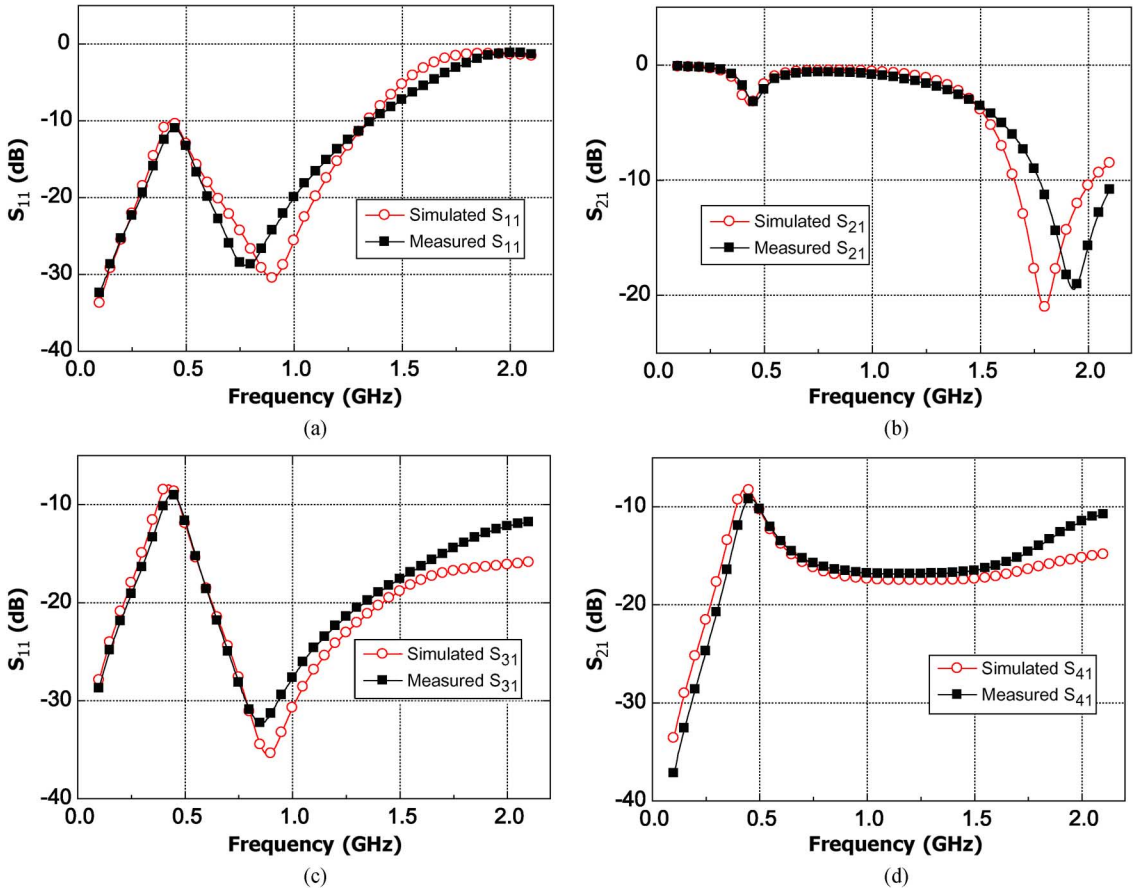


Fig. 14. Measured S-parameters of the spiral-shaped directional coupler. (a) S_{11}. (b) S_{21}. (c) S_{31}. (d) S_{41}.

entire CMOS transceiver with a PA. The measured S-parameters are shown in Fig. 14. The S-parameter designations are as follows: S_{11} stands for the return loss of the input port, S_{21} is the main-line insertion loss, S_{31} is the isolation, and S_{41} is the coupling factor. The insertion loss in the range of interest is from 0.69 to 0.76 dB, the isolation from -32.3 to -29.1 dB, and the coupling factor from -16.4 to -16.7 dB. It is estimated that the discrepancies, including the up-shift of the null position near the second harmonic around 1.7–1.9 GHz in S_{21}, may be attributed to the underestimation of the coupling coefficient of the transformer in the designed directional coupler during the EM simulation.

Table II summarizes the performances of directional couplers presented in [6], [7], and this study. The directional coupler in [6] is also fabricated in the IPD process. The proposed spiral-shaped directional coupler in this work achieves lower insertion loss than that in [6] and near 30 dB of isolation over the UHF RFID band. The isolation of directional couplers in [6] dramatically decreases as the frequency moves at the upper or lower end of the UHF RFID band. The directional coupler in [7], which is fabricated on a PCB, has higher isolation, but it occupies much larger area than that in this study.

Fig. 15(a) shows a photograph of the switch-mode CMOS PA chip and the IPD chip including the spiral-shaped directional coupler and the power combiner of the PA. The dimensions of the CMOS PA chip and the IPD chip are 1.3 mm $\times$ 1.05 mm and 2.8 mm $\times$ 1.4 mm, respectively. The test module on the PCB is shown in Fig. 15(b). Both chips are attached on the ground

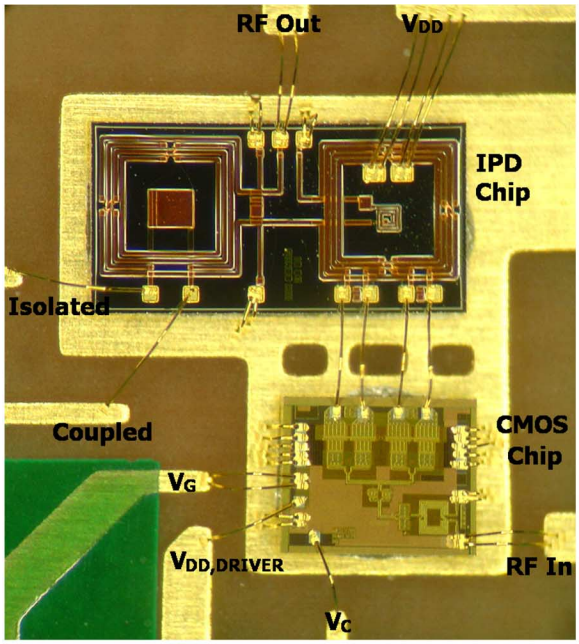
TABLE II
COMPARISON OF PERFORMANCES OF IPD DIRECTIONAL COUPLERS

Property	Freq. (MHz)	Ref. [6]		Ref. [7]	This work
		T-type	π-type		
Insertion loss (dB)	910	1.1*	1.7*	-	0.71
Coupling (dB)	910	-12*	-12*	-14.9	-16.6
Isolation (dB)	860	27**	23**	More than 40	32.3
	910	45*	42*	60.4	30.9
	960	28**	22**	More than 40	29.1
Size (mm^2)	-	1.74×1.6	1.32×1.4	62.2×32.7	1.4×1.4

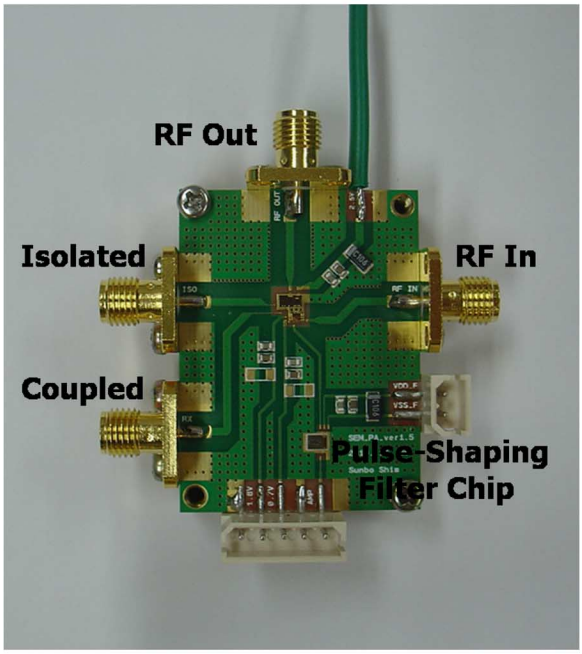
*Measured at 912 MHz.
**Estimated values from the graphs of measurement results in [6].

paddle of an FR4 PCB using conductive epoxy. Each RF signal pad on the CMOS chip and IPD chip is wire bonded to the 50-Ω microstrip lines and then connected to an SMA connector as RF input, RF output, isolated port, or coupled port. An additional chip for low-pass filtering is also attached on the PCB to provide an analog pulse-shaped signal to the gate of the CG transistors of the PA, V_C in Fig. 11, when we investigate the output spectrum with respect to the ASK input signal.

Fig. 16 shows the measured output power and PAE of the standalone CMOS PA and the CMOS PA with the directional coupler with respect to frequency. The supply voltage of the



(a)



(b)

Fig. 15. Photographs of: (a) CMOS PA chip and a single IPD chip consisting of the spiral-shaped directional coupler and the power combiner and (b) test module on a PCB.

driver/power stage of the PA is 1.8 V/2.5 V and the input power introduced from an RF signal generator is 8 dBm. The peak output power and PAE are 27.9 dBm and 53.7% for the standalone CMOS PA, and 27.3 dBm and 44.6% for the CMOS PA with the directional coupler. Although the performance is degraded after passing through the main line of the directional coupler due to its insertion loss, the gap of the output power between them is less than 1 dB over the entire UHF RFID band. The worst case PAE of the CMOS PA including the directional coupler loss is 37.9% at 960 MHz.

Fig. 17 shows the measured power level at the coupled port and the isolated port of the CMOS PA and the directional coupler with respect to frequency. The maximum power at the isolated port is less than 0 dBm, which means that the blocking condition is avoidable if the receiver is designed to have 8 dBm of $P_{1\,\mathrm{dB}}$, as we expected in Section II.

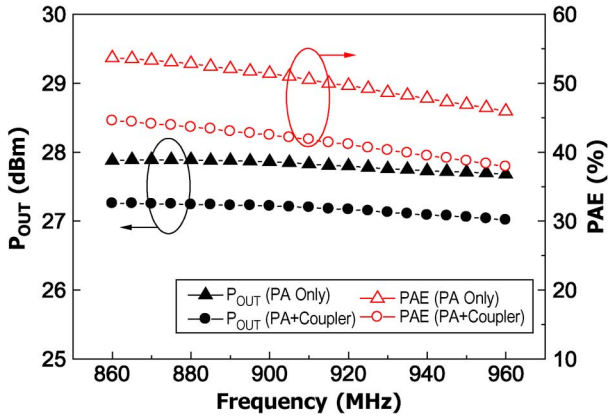


Fig. 16. Measured output power and PAE of the standalone CMOS PA and the CMOS PA with the directional coupler versus frequency.

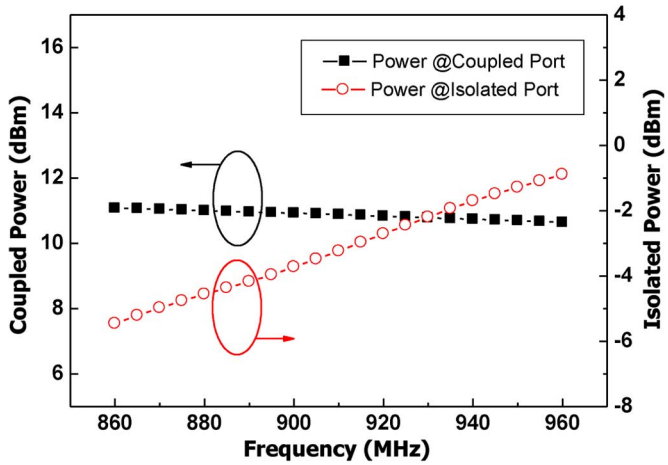


Fig. 17. Measured power at coupled port and isolated port of the CMOS PA and the directional coupler versus frequency.

The harmonics of the CMOS PA and the directional coupler are shown in Fig. 18. Without the shift of the location of the null at the second harmonic to higher frequency, depicted in Fig. 14, we can expect that the second harmonic of the CMOS PA is properly suppressed under −48 dBc after passing through the main path of the directional coupler. Less than −54 dBc of the third harmonic is observed in the UHF RFID band. The measurement results of Figs. 15–17 were based on a one-tone CW signal input.

Table III compares the performances of PAs that were utilized in UHF RFID readers of [1], [4], [13], and this study.

Fig. 19 shows the measured output spectrum of the ASK signal of continuous "select" and "query" commands with 25 μs of Tari for a UHF RFID centered at 910.05 MHz. The specification in [14] for an adjacent channel power ratio (ACPR) is −20/−50/−60 dBc for the first/second/third adjacent channels with 200 kHz of channel bandwidth. The observed output spectrum with a 20-dB attenuator indicates that the ACPR of UHF RFID is satisfied. Fig. 20 exhibits the measured RF envelope

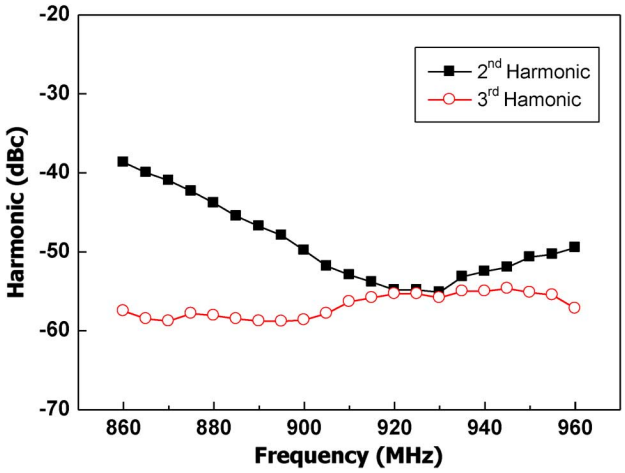


Fig. 18. Measured harmonics of the CMOS PA and the directional coupler versus frequency.

TABLE III
COMPARISON OF PERFORMANCES OF PAs FOR UHF RFID READER

Property	Ref. [1]	*Ref. [4]	Ref. [13]	*This work (Stand-alone PA)
Output power (dBm)	27	22	24	27.9
PAE (%)	40	35	41.3	53.7

*CMOS PAs.

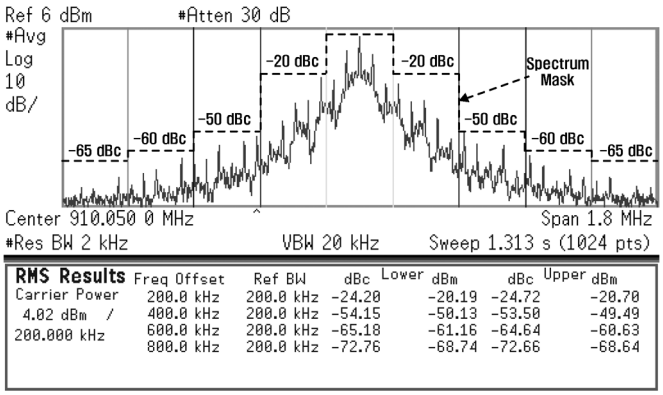


Fig. 19. Measured output spectrum of ASK signal for UHF RFID at 910.05 MHz (Tari $= 25\ \mu$s).

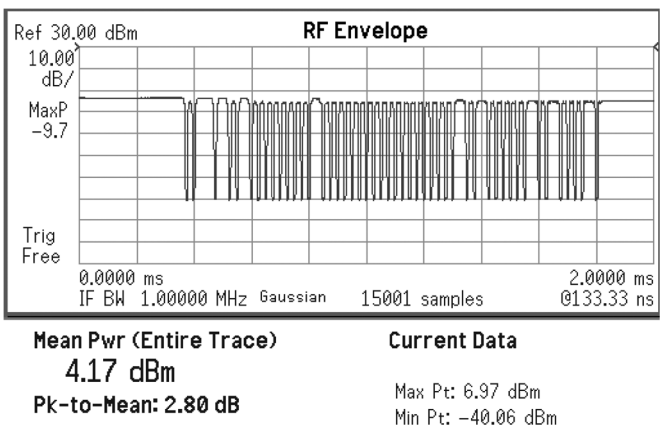


Fig. 20. Measured RF envelope of select command for UHF RFID at 910.05 MHz (Tari $= 25\ \mu$s).

signal with 25 μs of Tari at 910.05 MHz in accordance with the "select" command of the baseband.

VII. CONCLUSION

A CMOS PA with a spiral-shaped directional coupler has been proposed and implemented on a single IPD chip with a power combiner of a CMOS PA. This CMOS PA works as a polar transmitter for UHF RFID reader applications. Including directional coupler loss, the implemented CMOS PA demonstrates a peak output power of 27.3 dBm and a peak PAE of 44.6% in the UHF RFID band. This work suggests an eligible solution for integrating an entire UHF RFID reader transceiver CMOS IC including a PA and an additional IPD chip for a power combiner and a directional coupler in a compact standard package with high power efficiency.

ACKNOWLEDGMENT

The authors would like to thank K. Koo, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, for his helpful advice and discussion.

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Sunbo Shim (S'07) received the B.S. degree in electronics and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2006, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2008, and is currently working toward the Ph.D. degree in electrical engineering at KAIST.

His research interests include transmitter architecture with a switch-mode CMOS PA and digitally intensive RF transmitters.

Songcheol Hong (S'87–M'88) received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 1989.

In May 1989, he joined the faculty of the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. In 1997, he held short visiting professorships with Stanford University, Palo Alto, CA, and Samsung Microwave Semiconductor, Suwon, Korea. His research interests are microwave integrated circuits and systems including PAs for mobile communications, miniaturized radar, millimeter-wave frequency synthesizers, and novel semiconductor devices.