# A Fully-integrated High Power Wideband Power Amplifier in 0.25 μm CMOS SOS Technology

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**Abstract — A fully-integrated wideband power amplifier (PA) is implemented in 0.25 μm CMOS silicon-on-sapphire (SOS) technology. The PA is designed with 4 stacked dynamically biased Cascode cells to increase the overall output voltage swing as well as the output impedance. The fully-insulating substrate in the SOS process significantly suppresses the effect of parasitic capacitance and hence minimizes the amplitude and phase differences among drain-source voltage waveforms across each transistor. The PA measures a saturated output power ($P_{SAT}$) of 34.4 dBm (2.75 W) at 1.4 GHz with a peak PAE and corresponding DE of 38% and 48%, respectively, when biased under a 16 V supply. The measured output power is above 33 dBm (2 W) from 1 to 1.8 GHz. The linearity of the PA is measured with both uplink WCDMA and 10 MHz QPSK LTE signals at 1.4 GHz. The measured output power at ACLR of -33 dBc is 29.2 dBm for the WCDMA signal and 26.3 dBm for the LTE signal. The stacked PA occupies a compact chip area of 2.2 $mm^2$.**

**Index Terms — CMOS, RF power amplifiers, silicon-on-sapphire, wideband.**

## I. Introduction

CMOS technology has been considered as the most attractive technology platform for implementing system-on-chip (SoC) designs because of its low manufacturing cost and integration capability with digital circuits. Implementing a wideband fully-integrated CMOS PA with several watts of output power, however, remains challenging mainly because the low breakdown voltages of high performance CMOS transistors that limit the maximum allowable voltage swings across transistor terminals. Watt-level CMOS PAs have been demonstrated using power combining techniques [1-4]. The on-chip power combiners, nevertheless, occupy large chip area and degrade the PA's efficiency due to limited combining efficiency that can be practically achieved using standard metallization. Stacked PA, on the other hand, have been demonstrated to deliver high output power while providing high output impedance [5]. Traditionally, the internodal parasitic capacitance limited the maximum number of transistors that can be efficiently stacked to 4. A stacked PA with 16 stacked transistors using an additional post-fabrication substrate transfer technique has been demonstrated to suppress the adverse effect of parasitic capacitance [5]. In this work, a fully-integrated wideband stacked PA, designed with 4 stacked Cascode cells (8 stacked transistors), is implemented in 0.25 μm CMOS SOS technology. The fully-insulating substrate ($R_S > 10^{14}$ Ω·cm) in the CMOS SOS technology significantly suppresses the parasitic capacitance and allows 8 transistors to be stacked efficiently. The PA measures a high output power above 2 W over a wide frequency range from 1 to 1.8 GHz.

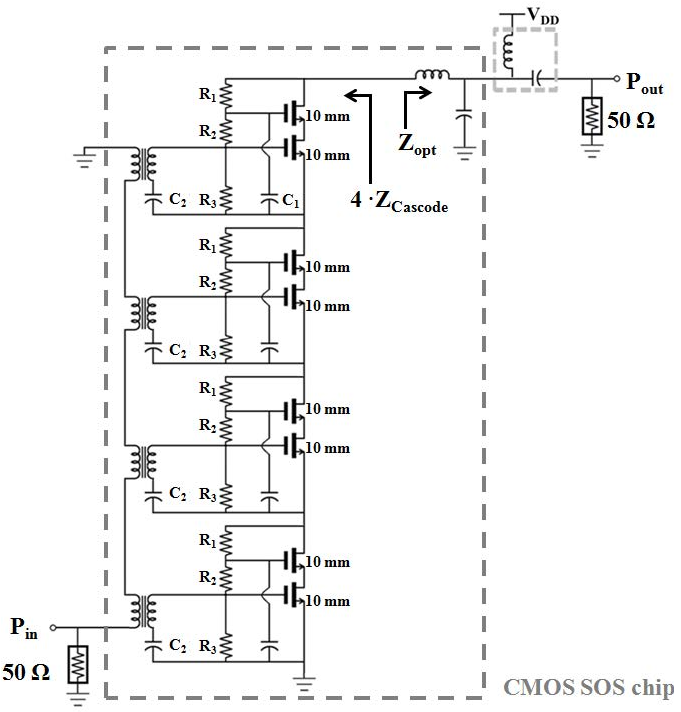


Fig. 1 The circuit schematic of the wideband stacked power amplifier.

## II. Stacked PA Design

The circuit schematic of the fully-integrated CMOS PA designed with 4 stacked transformer-coupled Cascode cells is depicted in Fig. 1. The stack configuration adds the drain-source voltage swings across each stacked transistor constructively to increase the total output voltage swing. The transistors are biased in Class AB operating region where the voltage at the top of the stack swings to $2\times V_{DD}$. To prevent gate oxide breakdown, the gate terminal of each transistor is dynamically-biased through resistor dividers ($R_1$ to $R_3$), which sets the gate voltage between the corresponding drain and source voltages. The Cascode cells provide high gain and high output impedance, and ensure stability. The transistors are implemented with width of 10 mm to provide sufficient gain as well as the necessary output impedance for the operation in 1 to 2 GHz frequency range. The high output impedance of the stacked Cascode cells minimizes the loss from the output matching network and facilitates wideband impedance

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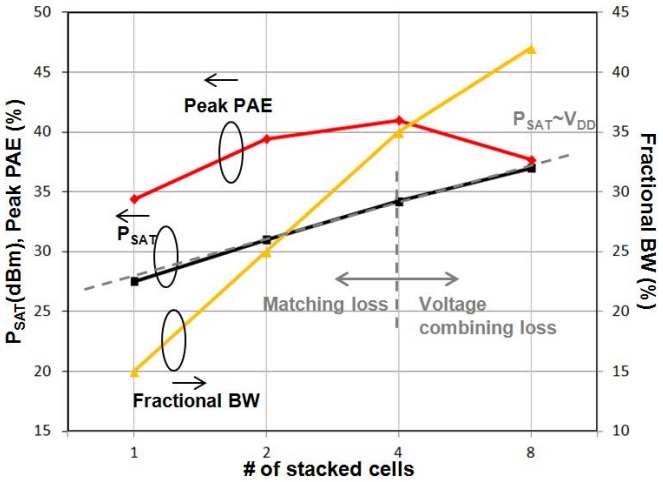


Fig. 2 Simulated $P_{SAT}$, peak PAE, and fractional bandwidth of stacked PAs designed with different number of stacked cells.

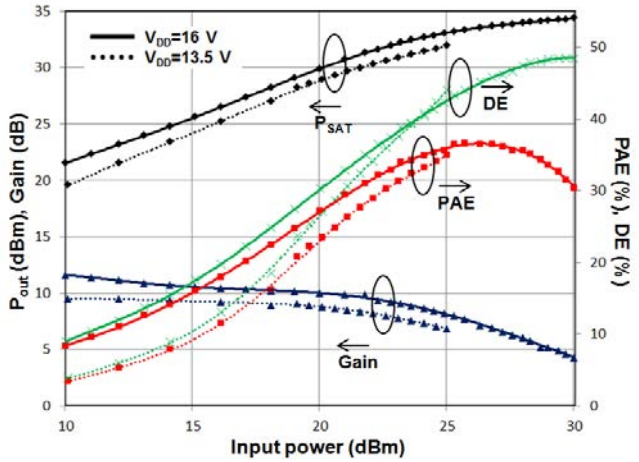


Fig. 3 Measured output power, gain, PAE, and DE at 1.4 GHz when biased under two supply voltages.

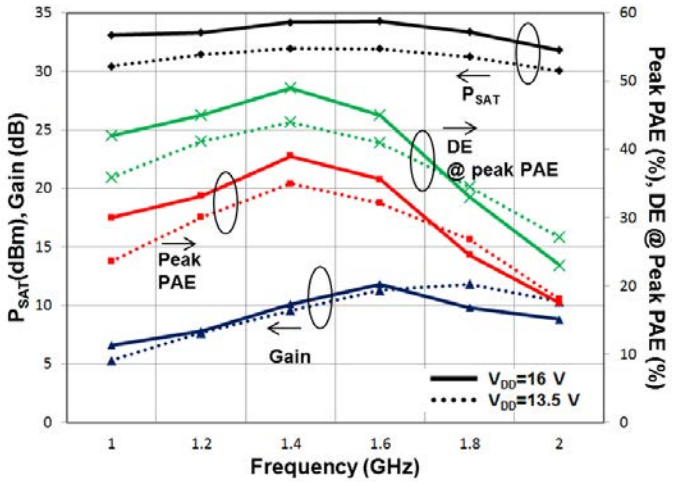


Fig. 4 Measured $P_{SAT}$, gain, PAE, and corresponding DE from 1 to 2 GHz when biased under two supply voltages.

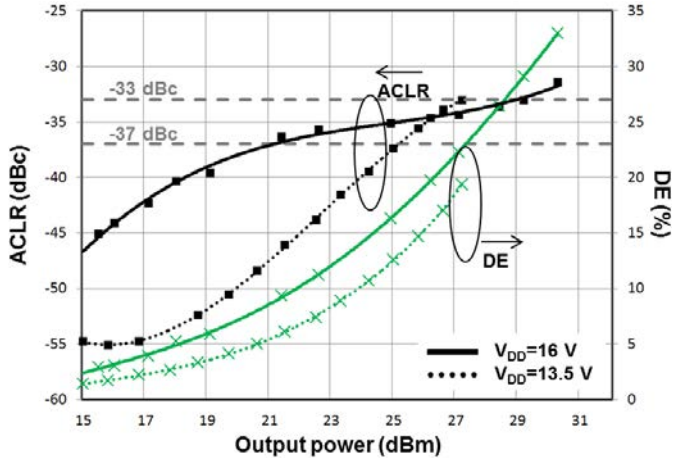


Fig. 5 Measured ACLR and DE versus output power using WCDMA signal at 1.4 GHz when biased under two supply voltages.

matching to a 50 Ω load using a single-stage on-chip LC matching network. The input power is coupled to the Cascode cells using on-chip transformers. The primary coils of the input transformers connected in series provide high input impedance to match to 50 Ω.

Fig. 2 shows the simulated $P_{SAT}$, peak PAE, and -3 dB output power fractional bandwidth (FBW) of PAs designed with different number of stacked Cascode cells. In the simulation, transistor widths are kept constant at 10 mm and the output matching network is designed to achieve maximum output power using a single-stage LC section. As shown in the figure, the peak PAE and FBW for one Cascode cell are dominated by the loss from the output matching network with high output impedance transformation ratio. By increasing number of stacked cells, the FBW and PAE improve due to reduced loss from the output matching network. The output power increases proportional to $V_{DD}$ since the supply voltage doubles as the number of stacked cells doubles while the bias current is kept constant. For 8 stacked cells, however, the voltage combining efficiency of stacked cells drops leading to reduced overall efficiency. The drop in combining efficiency is attributed to a finite phase delay through the transformer ladder leading to small phase shifts to the drain-source voltages across each transistor. In this work, 4 stacked cells with 10 mm width are selected to achieve highest PAE ~40% and a high output power above 34 dBm.

## III. Measurement Results

Fig. 3 plots the measured output power, gain, PAE, and DE of the stacked PA under two supply voltages at 1.4 GHz. The current densities of $I_D$ = 17 mA/mm and $I_D$ = 8 mA/mm at 13.5 V and 16 V, respectively, are selected to achieve highest peak PAE. The PA under a supply voltage of 16 V measures a saturated output power of 34.4 dBm (2.75 Watts) with peak PAE and corresponding DE of 38% and 48%, respectively. Fig. 4 plots the measured $P_{SAT}$, gain, peak PAE, and corresponding DE from 1 to 2 GHz with the two supply voltages. When the PA is biased under $V_{DD}$ = 16 V, the measured $P_{SAT}$ is above 33 dBm from 1 to 1.8 GHz with peak PAE and corresponding DE above 24.5% and 33%, respectively.

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TABLE I
COMPARISON OF WATT-LEVEL CMOS PAS

| Reference | Technology | Frequency (GHz) | $P_{SAT}$ (dBm) | Peak PAE (%) | Chip Area ($mm^2$) | Power Density ($W/mm^2$) | WCDMA $P_{OUT}$ (dBm) | LTE/WLAN $P_{OUT}$ (dBm) | Topology |
|---|---|---|---|---|---|---|---|---|---|
| [1] | CMOS 130 nm | 1.2-2.1 @1.85 | 32 | 15.3 | 4 X 1.5 | 0.264 | 28 @-38.7dBc ACLR | LTE 24.9 @-34.9 dBc ACLR | Power Combined |
| [2] | CMOS 180nm | 1.95 | 30.5 | 42.1 | 2.72 | 0.4125 | 28 @-35 dBc ACLR | N/A | Differential |
| [3] | CMOS 180 nm | 2.4 | 34 | 34.9 | 3.44 | 0.73 | N/A | WLAN 23.5 @-25 dB EVM | Power Combined |
| [4] | CMOS 90 nm | 0.93 | 29.4 | 25.8 | 3.3 | 0.27 | N/A | LTE w/DPD 26 @-25 dB EVM | Power Combined |
| [5] | CMOS 45 nm | 1.5-2.4 @1.8 | 30.2 | 23.8 | 1.2 | 0.833 | 25.1 @ -40.6 dBc ACLR | N/A | Stacked PA w/ AlN substrate |
| **This work** | **CMOS 0.25 µm SOS** | **1 - 1.8 @1.4** | **34.4** | **38** | **0.9 X 2.4** | **1.27** | **29.2 @-33 dBc ACLR** | **LTE 26.3 @-33 dBc ACLR** | **Stacked Cascode** |

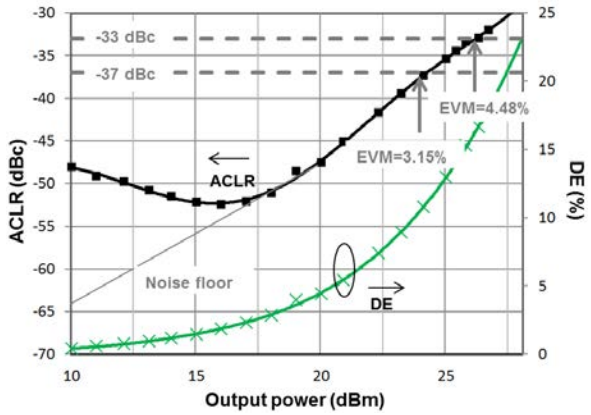


Fig. 6 Measured ACLR and DE versus output power using LTE signal at 1.4 GHz when biased under $V_{DD}$=13.5 V.

The stacked PA is measured using uplink WCDMA signal with chip rate of 3.84 Mcps. The ACLR is measured at 5 MHz offsets from the center frequency. Fig. 5 plots the measured ACLR and DE versus output power at 1.4 GHz under two supply voltages. The PA delivers an output power of 29.2 dBm and DE of 29.1% at ACLR of -33 dBc when biased under $V_{DD}$ = 16 V. Fig. 6 plots the measured ACLR and DE at 1.4 GHz using uplink 10 MHz QPSK LTE signal with peak-to-average ratio of 7.2 dB. The measured output power and DE are 26.3 dBm and 16.7%, respectively, while satisfying the ACLR of -33 dBc and EVM of 4.48% under supply voltage of 13.5 V.

## IV. CONCLUSION

Table I summarizes the performance of the presented stacked PA on UltraCMOS technology in comparison with other watt-level CMOS PAs reported to date. The presented stacked PA achieves the highest output power in GHz operating range while delivering more than 2 W of output power from 1 to 1.8 GHz. Fig. 7 shows the chip micrograph of the stacked PA. The PA occupies a compact chip area of 2.2 $mm^2$ including pads. The stacked scheme eliminates the large area required for on-chip power combiners and hence achieves a relatively high power density (1.27 $W/mm^2$).

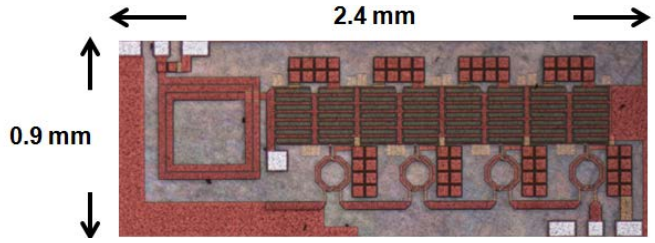


Fig. 7 Chip micrograph of the stacked PA.


## ACKNOWLEDGEMENT

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