A Dual Power-Mode Multi-Band Power Amplifier With Envelope Tracking for Handset Applications

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***Abstract*—This paper presents a dual power-mode and multi-band power amplifier (PA) for handset applications that improves the efficiency in low-power regions. This PA operates in two modes through path control by a shunt switched capacitor. The proposed control method provides efficient mode control without any efficiency degrading and bandwidth (BW) limiting. The proposed PA, in conjunction with a boosted supply modulator for envelope tracking (ET) operation not only in the high-power mode, but also in the low-power mode, delivers good performance at all average output power levels. The linearity is improved by ET through a proper envelope-shaping method. For demonstrative purposes, the PA and supply modulator are implemented using an InGaP/GaAs heterojunction bipolar transistor and AlGaAs/InGaAs enhancement/depletion-mode pseudomorphic high electron-mobility transistor process and a 0.18-μm CMOS process, respectively. The ET PA is tested across the range of 1.7–2.0 GHz using a long-term evolution signal with 16 quadrature amplitude modulation, a 7.5-dB peak-to-average power ratio, and 10-MHz BW. The proposed dual power-mode multi-band ET PA delivers good performance for high- and low-power modes, indicating that the architecture is promising for handset PA applications.**

***Index Terms*—Dual mode, envelope tracking (ET), high-power mode (HPM), long-term evolution (LTE), low-power mode (LPM), power amplifier (PA), supply modulator (SM), switched capacitor.**

I. Introduction

MULTI-FUNCTIONAL smart mobile phones should be able to handle text, voice, data, and broadcast information with global roaming capability. In addition, independently developed wireless communication standards, such as long-term evolution (LTE), mobile worldwide interoperability for microwave access (m-WiMAX), and wideband code division multiple access (WCDMA), increase the number of frequency bands and amount of spectrum fragmentation. Therefore, power amplifiers (PAs) for these phones should have a multi-mode and multi-band capability with high efficiency. Moreover, the signals are coded by a complex modulation method such as orthogonal frequency division multiplexing (OFDM) modulation scheme to enhance the spectrum efficiency. Since the signals with complex modulation have a large peak-to-average ratio (PAPR) and wide bandwidth (BW), PAs should deliver high efficiency and linearity over a large dynamic range. Many techniques have been investigated to improve efficiency for all output power levels [1]–[23].

For enhanced efficiency in a back-off region, a PA with a tunable load is the most popular approach in a handset application [2]. Dual-path structures or stage-bypass structures are also employed for high-power mode (HPM) and low-power mode (LPM) operations [3]–[8]. In this architecture, two different sized linear PAs are used; the LPM employs a small size power cell with high load impedance, and the HPM operates a conventional linear PA. The inputs and the outputs of the HPM and LPM amplifiers are usually connected by a series switch or an impedance transformer with a matching network to set the impedance level for each power mode; however, the efficiency is degraded by the loss of the control component. The power-mode control circuits are sensitive to the operation frequency and limit the BW. Thus, a new control circuit that can operate across a broadband with low loss is required.

The envelope-tracking (ET) PA is another popular efficiency enhancement technique. To reduce the dc power consumption at low power, this technique modulates the supply voltage of the PA according to the input power level. Since the overall efficiency of the ET PA is proportional to the efficiency of the supply modulator, and the linearity of the PA is strongly affected by the linearity of the supply modulator, an optimized design for the supply modulator is very important. There are two types of modulators: a linear amplifier and a switching amplifier. In [9] and [10], a low dropout (LDO) is used as the supply modulator. Although the LDO provides a large BW, its efficiency is poor. In [11]–[13], a switching amplifier is used, and the efficiency is significantly higher than the LDO. However, this structure requires a high-order passive filter, and its BW is too narrow to be used for wide BW signals. To achieve operation with wide BW and high efficiency, a hybrid switching amplifier that possesses a combined structure for the switching amplifier and the linear amplifier is used in [14]–[19]. To improve efficiency, output

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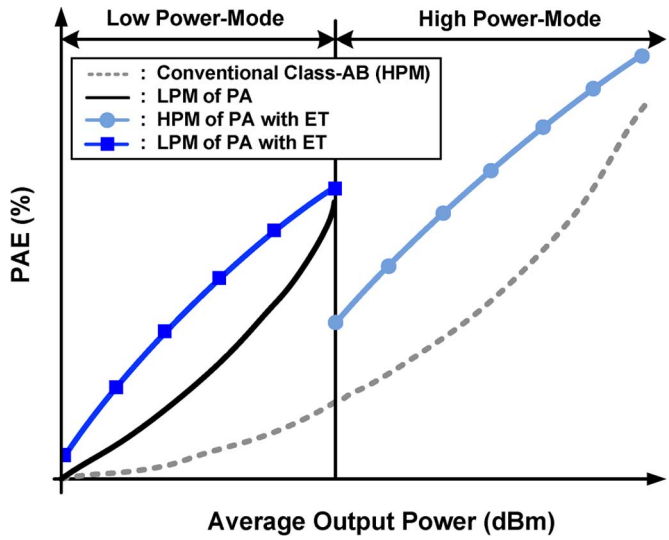


Fig. 1. PAE curve of the dual power-mode PA with ET operation.

power, and linearity, several envelope-shaping methods are suggested [18]–[22]. In the ET operation, only the PA determines the RF operating frequency band and can be rather easily designed for broadband operation.

In this paper, we propose a dual power-mode and multi-band ET PA with a boosted supply modulator for handset applications. A new power mode-control method is proposed for the standalone PA, which can achieve higher efficiency with broadband characteristics. Though the method is demonstrated in [7], this paper presents more detailed analyses with enhanced techniques for efficiency and BW characteristics. In view of the ET PA, the supply modulator is connected to the LPM as well as the HPM. Fig. 1 shows the conceptual curve of the power-added efficiency (PAE) of the PA. In Section II, a broadband matching technique for the dual power-mode PA is explained. To achieve high efficiency and broadband characteristic, a shunt switched capacitor is attached at the output of the LPM for power-mode control. Through the analysis of the input capacitance of the transistor, it is shown that the input signal path can be automatically selected by turning on/off the base bias of the heterojunction bipolar transistors (HBTs) without series switch. This behavior is explained in Section III. In Section IV, the issue of the dual power-mode PA for ET operation is discussed and the design of the boosted supply modulator for the dual power-mode PA is explained. The measurement results for the LTE signals are provided in Section V.

II. Techniques for Broadband PA

In our previous work, a linear broadband PA that has a 300-MHz BW was proposed [21]. The amplifier is a AB biased class-F operation [24], and the third harmonic impedance that is several times larger than the fundamental load impedance delivers high efficiency. This matching can be easily achieved across a broadband frequency range. The matching of the second harmonic impedance is more sensitive than that of the third harmonic impedance, but it is manageable over a few hundred megahertz BW using a second harmonic short circuit.

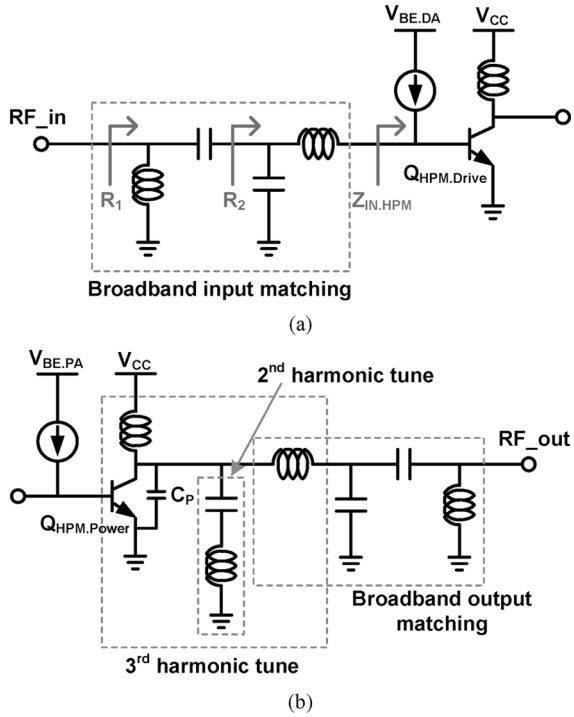


Fig. 2. (a) Input impedance-matching circuit using *LC–CL* BPF type. (b) Output impedance-matching circuit using *LC–CL* BPF type with merged harmonic matching circuit.

The circuit node Q, denoted by Q_n, determines the matching circuit BW and is defined at each node as

$$Q_n = \frac{|X|}{R} \tag{1}$$

where R and X are the real and imaginary parts of the node impedance. For impedance transformation using an LC network from R_T to R_S, where R_T is greater than R_S, Q_n is given by

$$Q_n = \sqrt{\frac{R_T}{R_S} - 1}. \tag{2}$$

In Fig. 2(a), R_1 and R_2 can be considered R_T and R_S, respectively. A smaller Q_n leads to a broader BW, and (2) indicates that a required BW can be achieved using a two-section matching circuit with the same impedance transformation ratio. In Fig. 2(a), to obtain the lowest Q_n with impedance transformation, the relationship of impedances is given by

$$R_2 = \sqrt{R_1 \cdot R_3} \tag{3}$$

where R_3 is the real part of $Z_{\mathrm{IN.HPM}}$ and it is assumed that the imaginary part is tuned out by the inductor. The *LC–CL* BPFs shown in Fig. 2 are employed in this broadband class-F PA design because of their broadband characteristics and their small inductor values, which can be easily replaced by bondwires [24]. As illustrated in Fig. 2(a), the input capacitance composed of C_{be} and C_{bc} increased by the Miller effect is merged into the series inductor of the *LC–CL* broadband matching circuit to maximize the BW. The output matching also comprises the broadband fundamental impedance matching, the second harmonic tune circuits, and the third harmonic tune circuit, as

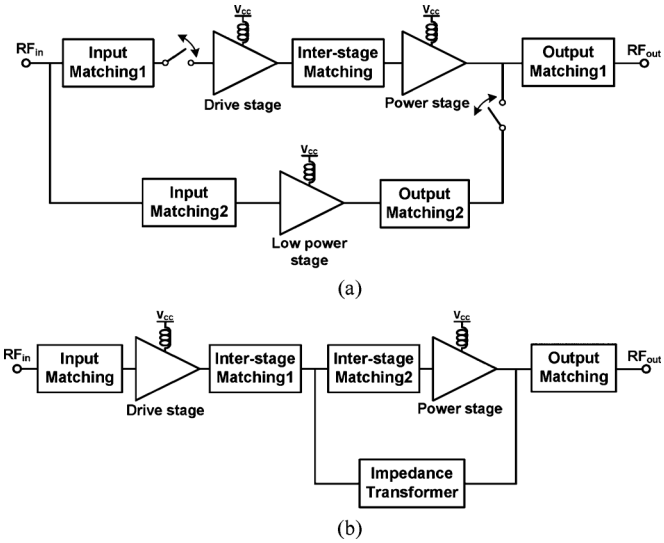


Fig. 3. Block diagram of conventional dual power-mode PA. (a) Dual-path structure with series switch for mode control. (b) Stage-bypass structure with impedance tramsformer for mode control.

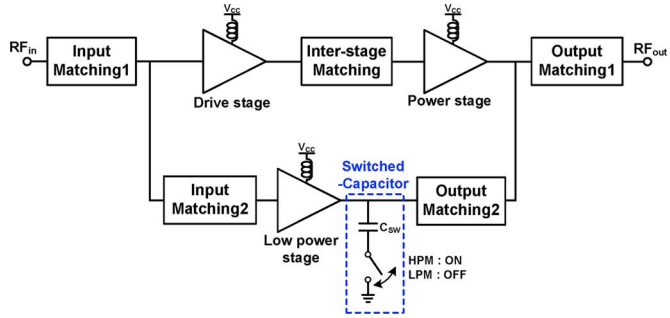


Fig. 4. Block diagram of proposed dual power-mode PA with shunt switched capacitor for mode control.

shown in Fig. 2(b). The output capacitance C_p is resonated out at the fundamental frequency by the inductance at the bias line. The load impedances across the 1.7–2.0-GHz frequency are constant with the power matching. The second harmonic impedances across the 3.4–4.0-GHz frequency are near zero, which is located at the high-efficiency region. The third harmonic impedances across the 5.1–6.0-GHz frequency are high, which is also located at the high-efficiency region for the class-F operation [21].

III. Operating Principle of Broadband Dual Power-Mode PA

In Section II, the broadband technique of the single power-mode PA is explained. These broadband techniques cannot be applied directly to the dual power-mode PA. Conventionally, dual-path structures [3]–[7] or stage-bypass structures [8] are commonly employed for dual power-mode operation. These structures need a series switch or an impedance transformer to set the impedance level for each power mode, as shown in Fig. 3. For broadband operation with a dual power mode, the series switch can be adopted for the mode change due to its broadband characteristics, as shown in Fig. 3(a). However, in this case, efficiency is degraded by the loss of the series switch because the loss is directly included in the output matching. Generally, the impedance transformer, called a chain matching network in [3], consists of two or more components, which can degrade the efficiency. Moreover, the impedance transformer should have a high-Q factor, limiting the BW characteristics. Therefore, conventional methods cannot achieve broadband characteristics with high efficiency in the dual power mode. To solve this problem, we employ a shunt switched capacitor for the control. The proposed dual power-mode PA with a shunt switched capacitor, shown in Fig. 4, is optimized for the LPM/HPM with appropriate load impedance transforms without any efficiency degrading and BW limiting. The high-power path is designed to deliver maximum output power, while the low-power path targets the back-off power level. Depending on the output power requirement, the PA chooses between the high- and low-power paths, thereby achieving higher efficiency under the back-off operation. Fig. 5 shows the schematic of the proposed dual power-mode ET PA. The proposed dual-path PA is discussed in detail in this section together with the efficiency and BW enhancements.

A. Selection of Input Path

The parameters of an HBT nonlinear equivalent circuit shown in Fig. 6 are extracted from the HBT model described in [26]. The extracted $C_{\rm in}$ is given by

$$C_{\rm in} = C_{\rm be} + C_{\rm bc}(1 + g_m(R_o \parallel R_{\rm opt})) \tag{4}$$

where $R_{\rm opt}$ is the output load impedance. Due to the varactor characteristics of the input capacitance, $C_{\rm in}$ can be increased dramatically as the base voltage increases. In this work, the drive stage and the low power stage employ the same size of the transistor of $720\mu{\rm m}^2$. The variation of the input capacitance for the transistor is calculated, and the results are shown in Fig. 7, indicating about 600% variation. These large differences in the input impedance can be used to select the input path for the mode change.

The signal path is automatically selected by turning on/off the base bias of the HBTs. In the HPM case, $V_{\rm BE.DA}$ and $V_{\rm BE.PA}$ are high to turn on $Q_{\rm HPM}$, and $V_{\rm BE.LPA}$ is low to turn off $Q_{\rm LPM}$. The input capacitor characteristics and the input matching circuit make the impedance ratio of $Z_{\rm IN.LPM}/Z_{\rm IN.HPM}$ a high value. To calculate the input power dividing ratio, the load–pull simulation is carried out. At the on-state of the drive stage, Port.2 of the HPM path has a fixed input impedance, as shown in Fig. 8(a). With the fixed input impedance of $Z_{\rm IN.HPM}$, the load–pull results of the $S_{2,1}$ contours show that in the off-state of the low power-mode transistor, most of the input power is delivered to the HPM path with loss lower than 0.17 dB, which is delivered to the LPM [see Fig. 8(b)].

When the circuit operates in the LPM, $V_{\rm BE.DA}$ and $V_{\rm BE.PA}$ are set to low to turn off $Q_{\rm HPM}$, and $V_{\rm BE.LPA}$ is set to high to turn on $Q_{\rm LPM}$. In this case, the impedance ratio of $Z_{\rm IN.HPM}/Z_{\rm IN.LPM}$ is high, and we check the input power dividing ratio by the same load–pull simulation. As shown in Fig. 9, the $S_{3,1}$ contours show that the input power passes through the LPM path with loss lower than 0.5 dB. Due to the

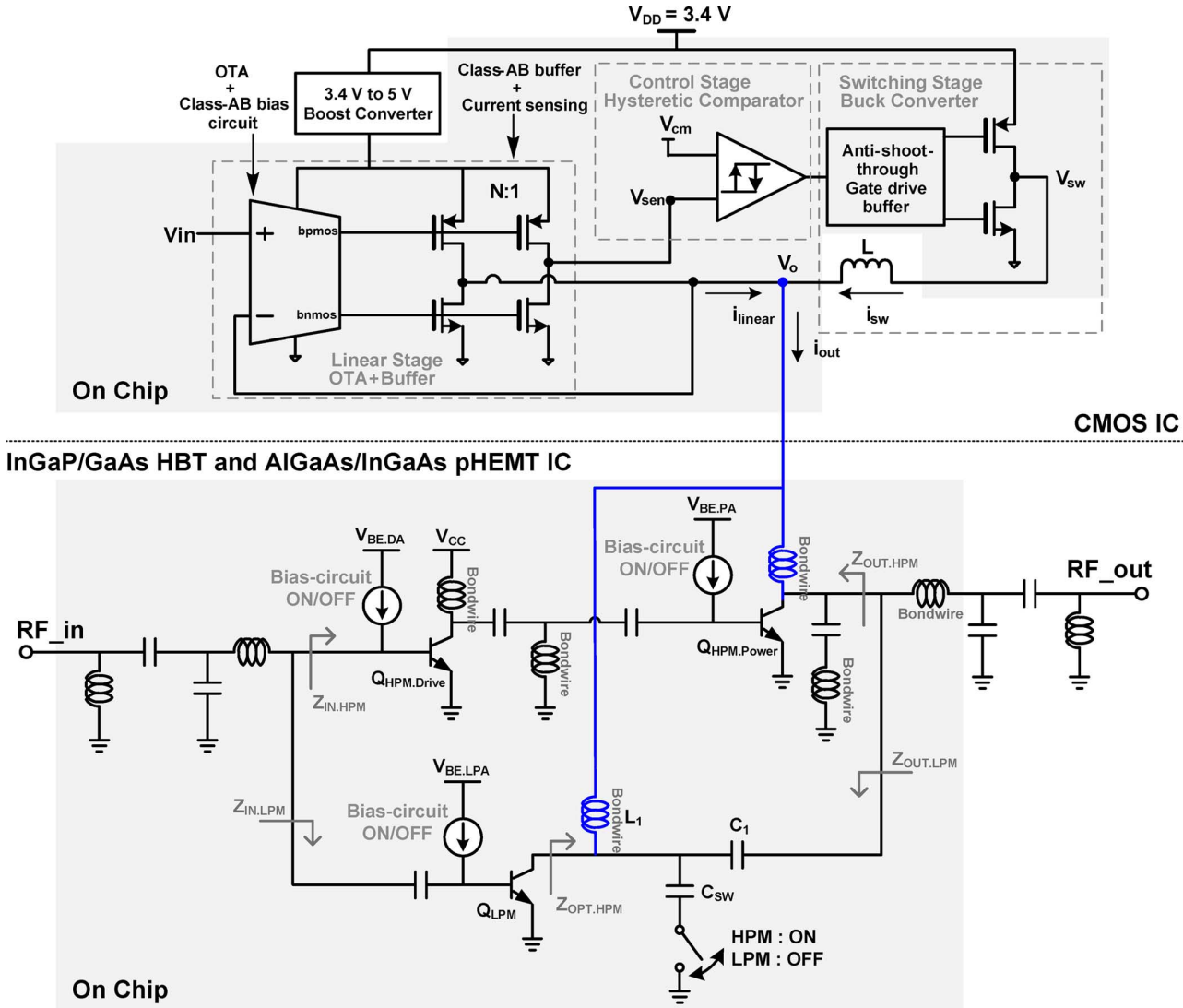


Fig. 5. Schematic of the ET transmitter with dual power-mode PA and boosted supply modulator.

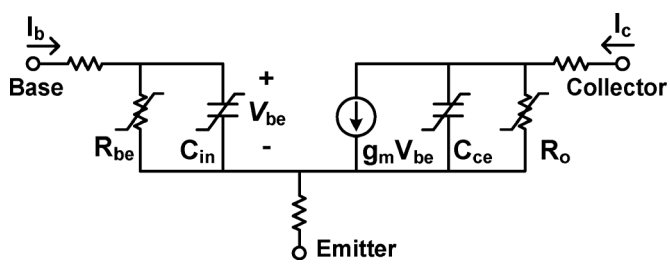


Fig. 6. HBT nonlinear equivalent-circuit model.

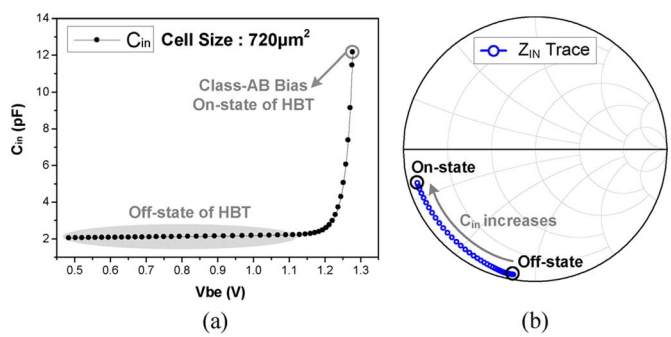


Fig. 7. Input capacitance variation with base bias voltage. (a) Value of input capacitance versus base bias voltage. (b) Trace of input capacitance on the Smith chart.

input capacitor characteristics, no switch is required for the signal path selection.

B. High-Power Operation

For proper HPM operation, the output of $Q_{\mathrm{HPM.Power}}$ should not leak to the $Z_{\mathrm{OUT.LPM}}$ path. We propose the shunt switched capacitor at the LPM path instead of a series switch or an impedance transformer. Fig. 10 shows the equivalent circuit of the $Z_{\mathrm{OUT.LPM}}$ path under HPM operation with the capacitor in an on-state. The total reactance value of the $Z_{\mathrm{OUT.LPM}}$ path is equivalent to a small capacitor of 0.3 pF, which makes a high-impedance level of about 280 Ω over a 300-MHz BW. Therefore, the $Z_{\mathrm{OUT.LPM}}$ path barely affects the output matching circuit of HPM. Since the optimum load impedance for power matching of the HPM that is identical to the $Z'_{\mathrm{OUT.LPM}}$ is about 6 Ω, the optimum load impedance for

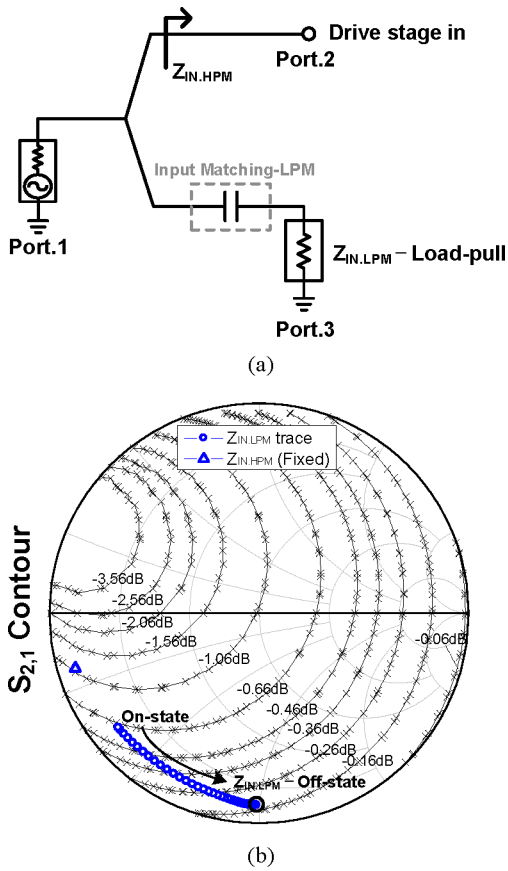


Fig. 8. Load–pull simulation of Port.2 for the HPM case with the fixed input impedance of $Z_{\mathrm{IN.HPM}}$. (a) Simulation setup of load–pull. (b) $S_{2,1}$ contour of simulated load–pull results.

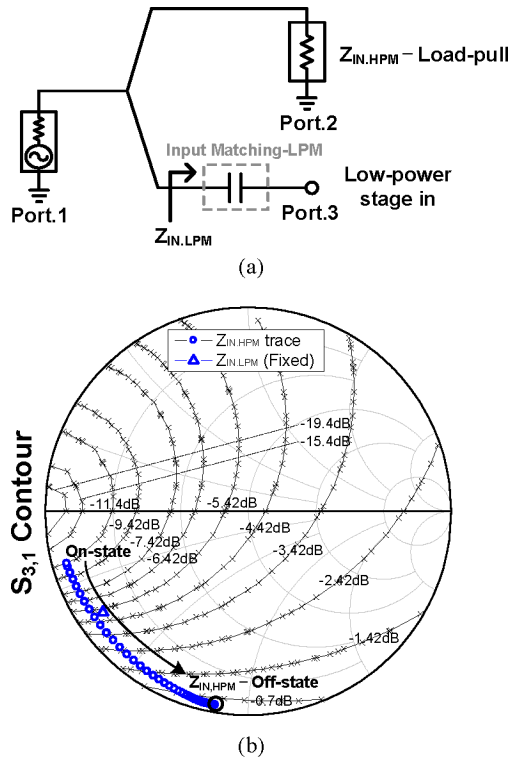


Fig. 9. Load–pull simulation of Port.3 for the LPM case with the fixed input impedance of $Z_{\mathrm{IN.LPM}}$. (a) Simulation setup of load–pull. (b) $S_{3,1}$ contour of simulated load–pull results.

power matching of the LPM is about 60 Ω. Thus, the output matching for the LPM output path should have an impedance transformation ratio, m, of 10

$$m = \frac{Z_{\mathrm{OPT.LPM}}}{Z'_{\mathrm{OUT.LPM}}} = 10. \tag{5}$$

Equations (6) and (7) provide the high-pass matching component values of C_1 and L_1 for the LPM

$$L_1 = \frac{Z_{\mathrm{OPT.LPM}}}{w_0 \cdot \sqrt{m-1}} \tag{6}$$

$$C_1 = \frac{1}{w_0 \cdot \sqrt{m-1} \cdot Z'_{\mathrm{OUT.LPM}}} \tag{7}$$

where w_0 is the center frequency. High-pass matching is the suitable approach to merge the dc block and collector bias line into the matching components. Without the switched capacitor, the resonance frequency, w_{res}, of the LPM path can be given by

$$w_{\mathrm{res}} = w_0 \sqrt{\frac{m-1}{m}} \tag{8}$$

where $C_{\mathrm{LPM}} \parallel L_1 \approx L_1$ is assumed. When the center frequency is 1.85 GHz, the LPM output path resonates about 1.76 GHz, which is in the band. $S_{2,1}$ is calculated using the simplified circuit shown in Fig. 11(a). The results shown in Fig. 11(b) show almost the same value calculated by (8). This resonance

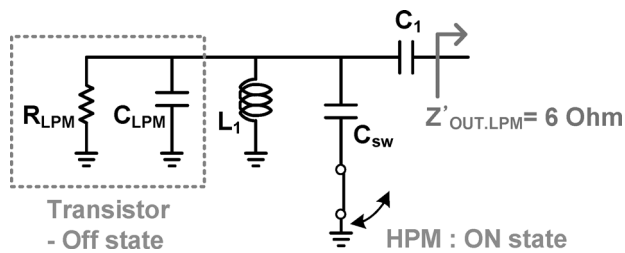


Fig. 10. Equivalent circuit of LPM path in HPM operation.

state disturbs the matching circuit of the HPM and generates instability. The switched capacitor ensures stability by shifting the resonance frequency away from the operating frequency band. Therefore, most of the signals are passed to the output of the PA. Since there is no added component in the HPM path for the mode control, there are not any additional loss and limitation of BW. It means that the broadband techniques explained in Section II can be applied in high-power operation.

C. Low-Power Operation

In the LPM operation, the output of Q_{LPM} should not leak to the $Z_{\mathrm{OUT.HPM}}$ path. The output capacitance of $Q_{\mathrm{HPM.Power}}$ and the series LC circuit for the second harmonic control are resonated out by the inductance of the bias line. Therefore, the imaginary part of $Z_{\mathrm{OUT.HPM}}$ is eliminated, and $Z_{\mathrm{OUT.HPM}}$ has a high impedance, about 347 Ω at 1.85 GHz, as shown in Fig. 12(a). The $Z_{\mathrm{OUT.HPM}}$ has about ten times larger than Z_{OUT} over a 300-MHz BW, preventing any power leakage, as shown in Fig. 12(b). The signal does not see the switch loss because the shunt switched capacitor is in the off-state in the LPM.

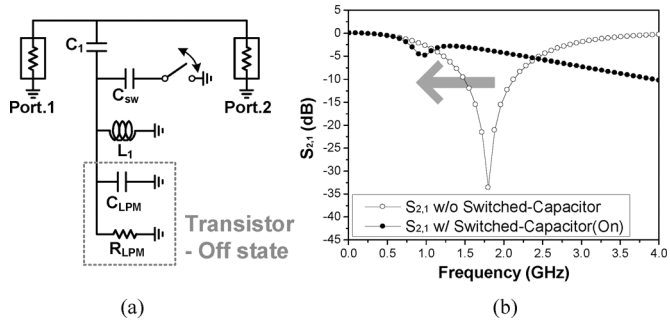


Fig. 11. Resonance frequency of LPM path in HPM operation. (a) Simulation setup of S-parameter. (b) Resonance frequency is shifted from the operating frequency by the switched capacitor.

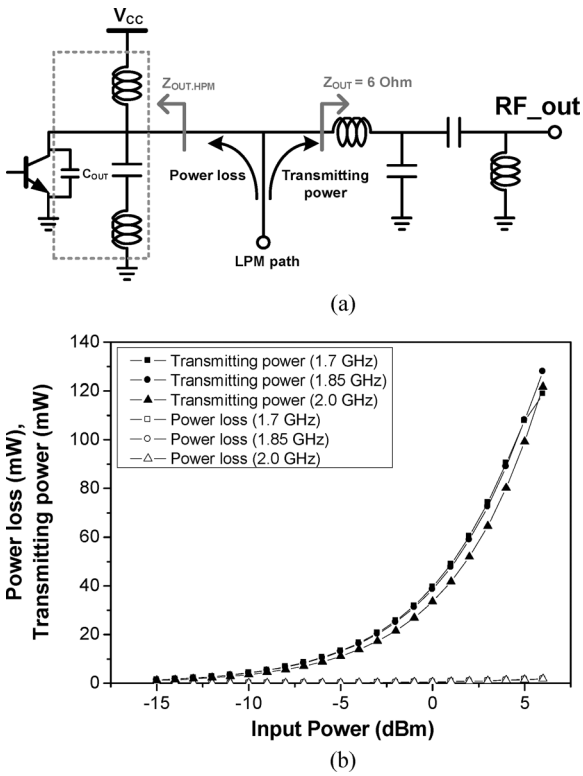


Fig. 12. (a) Schematic with output impedance of $Z_{\mathrm{OUT.HPM}}$ in LPM operation. (b) CW simulated results of power loss and transmitting power in LPM operation.

Except for one series capacitor for matching, which is insensitive to the BW, no other components are added in the LPM path. The LPM path shares the *LC–CL* broadband matching circuit so the LPM can be operated across the same 300-MHz BW.

D. Highly Efficient Broadband Dual Power-Mode PA

In the conventional control method using a series switch, the loss of the switch is directly included in the output matching at one of the two power modes, resulting in efficiency degradation. Although the proposed method uses the switch, it is used in a shunt configuration, and the loss is not included in the output matching circuit in both power modes. Therefore, the system achieves high efficiency. Additionally, the proposed control method does not degrade the BW as much compared to the conventional method using an impedance transformer,

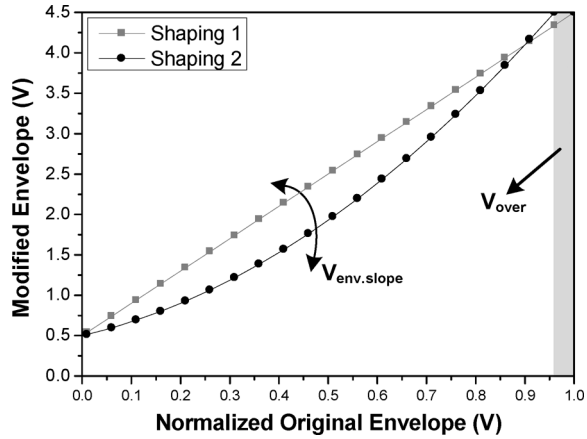


Fig. 13. Envelope-shaping curves.

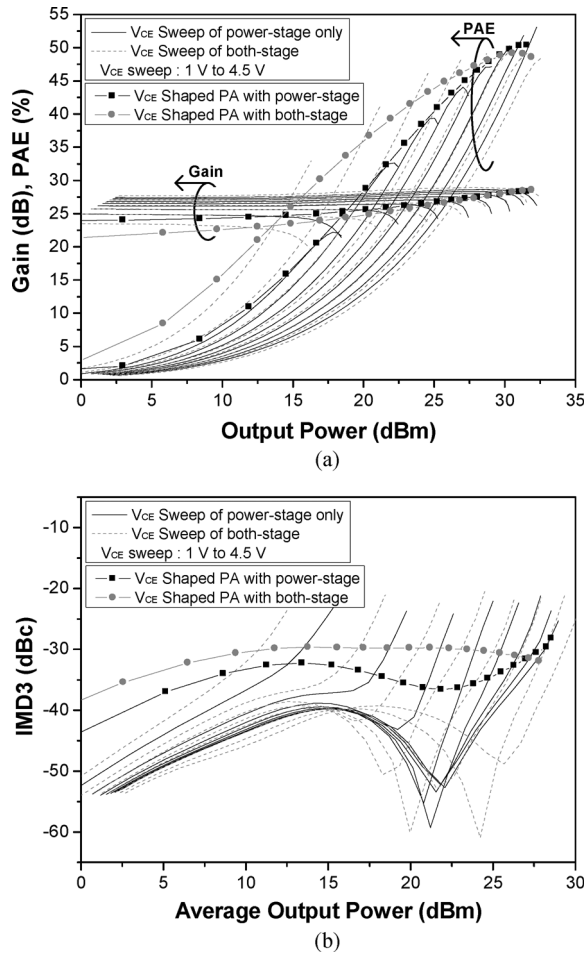
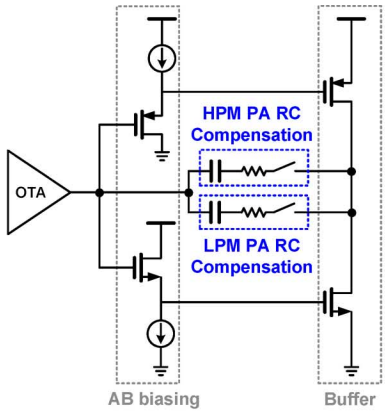
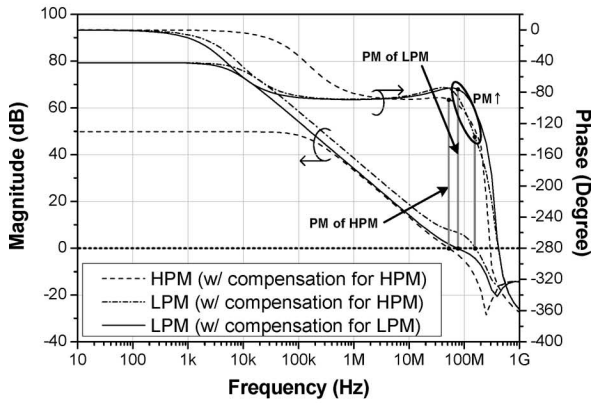


Fig. 14. (V_{CE}) sweep of the dual power-mode PA in the HPM and the shaped collector voltage (V_{CE}) applied to the power-stage only and both-stage at 1.85 GHz. (a) CW simulation results. (b) Two-tone simulation results.

and it achieves the high efficiency over a broad BW, 300 MHz from 1.7 to 2.0 GHz in this study. The mobile signals are intensively distributed at the high-band (1.7–2.0 GHz) such as the LTE band1 (1.92–1.98 GHz), band2 (1.85–1.91 GHz), band3 (1.71–1.785 GHz), and band4 (1.71–1.755 GHz). The proposed single PA can cover these important bands. The conventional control method can be superseded by this proposed method



(a)



(b)

Fig. 15. In the linear stage of the supply modulator. (a) Added *RC* compensation circuits for dual power mode of PA. (b) Comparison of the phase margin with and without the *RC* compensation circuits.

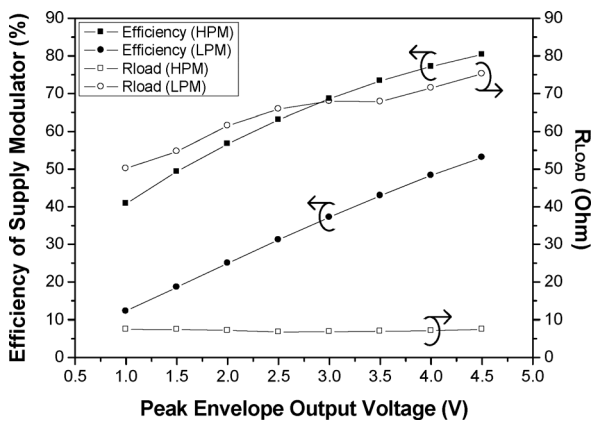


Fig. 16. Overall efficiencies of the supply modulator with the proper load conditions.

using a shunt switched capacitor with a dual-path structure, as well as with a stage-bypass structure. For the ET operation with the dual power modes, the dual-path structure is implemented in this work and will be discussed in Section IV.

IV. Dual Power-Mode PA With Boosted Supply Modulators

The boosted supply modulator consists of a boost converter, linear stage, hysteretic comparator, and switching stage, as shown in Fig. 5. The boosted supply modulator delivers a high voltage (4.5 V) to the PA due to the high voltage supplied to the linear stage by the boost converter. By boosting the battery voltage to 5 V and employing a hybrid switching architecture (HSA), we can achieve high efficiency and high power operation of the PA over the entire battery voltage range, performing a power-management integrated circuit (PMIC) [21], [22].

A PA with the boosted supply modulator has the following advantages. As the output voltage of the lithium-ion battery changes from 4.2 to 3.4 V, it is discharged by about 80% from the full charge. Therefore, conventional PAs are designed at 3.4 V to ensure the rated output power, degrading the PA performance at the higher voltage. The boosted supply modulator provides a constant supply voltage so that it maintains the maximum performance all the times at the desired output power. The

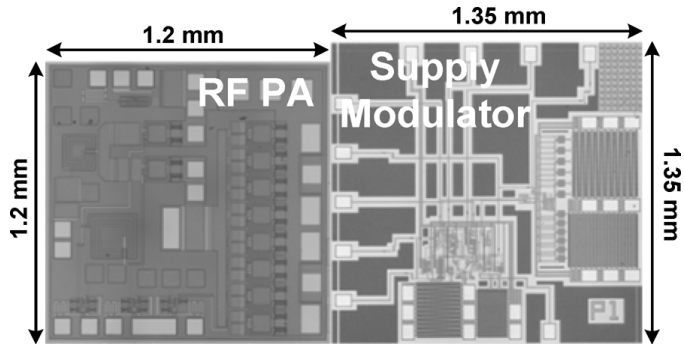
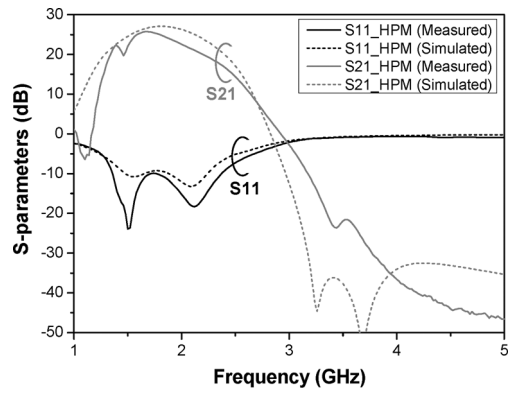
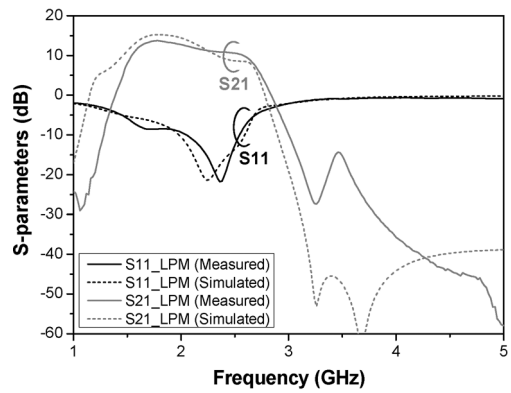


Fig. 17. Fabricated chip photographs of the proposed PA and supply modulator.



(a)



(b)

Fig. 18. Measured and simulated S-parameters with a supply voltage of 3.4 V at: (a) HPM operation and (B) LPM operation.

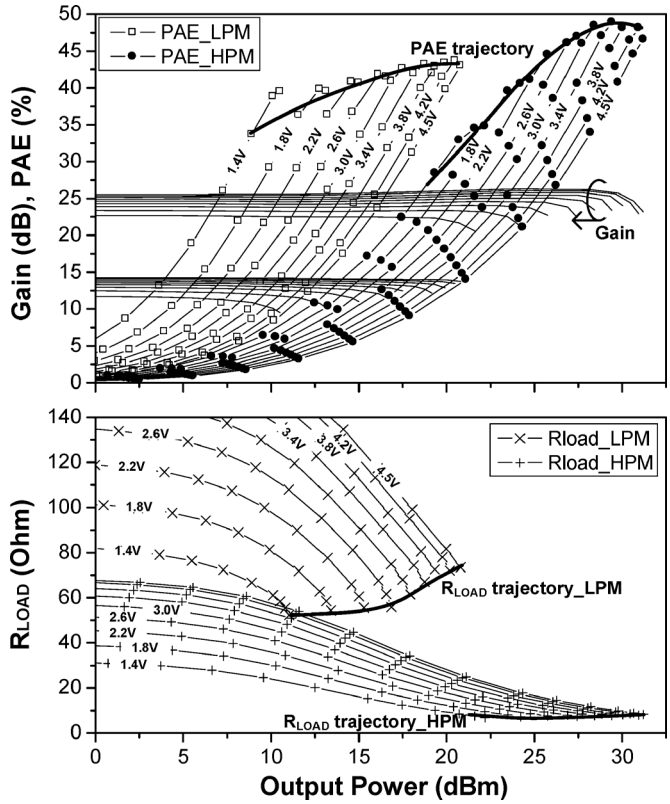


Fig. 19. Measured CW performance at 1.85 GHz by sweeping the collector voltage from 1.4 to 4.5 V.

load impedance for 4.5 V is larger than that of the low voltage one and gives higher efficiency and broader BW, as well as more linear ET operation at the low power level due to the lower portion of knee voltage. Also, as the supply voltage increases, the output capacitance decreases [21]. At an output power of 32 dBm, the PA using $R_{\rm opt}$ of 2.5 Ω with a supply voltage of 3 V has about a 10% larger output capacitance than that using $R_{\rm opt}$ of 6 Ω with a supply voltage of 4.5 V. Besides the smaller output capacitance, the PA with the 4.5-V supply voltage has a smaller impedance transformation ratio, which is favorable for increasing the operational RF BW.

A. Dual Power-Mode PA for ET Operation

The envelope shaping is important for the ET operation and can describe the characteristics of the ET PAs. Fig. 13 shows the envelope shaping. The Shaping 1 expressed as

$$V_{\rm CE} = \frac{V_{\rm CE.MAX} - V_{\rm knee}}{V_{\rm CE.MAX}} \cdot V_{\rm in.env} + V_{\rm knee} \tag{9}$$

is popularly employed [22]. However, we have found a further optimized shaping function, Shaping 2, given by

$$V_{\rm CE} = k \cdot \frac{V_{\rm CE.MAX} - V_{\rm knee}}{V_{\rm CE.MAX}} \cdot V_{\rm in.env} + V_{\rm knee} \tag{10}$$

$$k = \frac{10^{x/20} + V_{\rm env.slope} + V_{\rm over}}{V_{\rm CE.MAX} + V_{\rm env.slope}} \tag{11}$$

where x is the back-off power level from the peak average power, $V_{\rm env.slope}$ is the factor that changes the slope of the

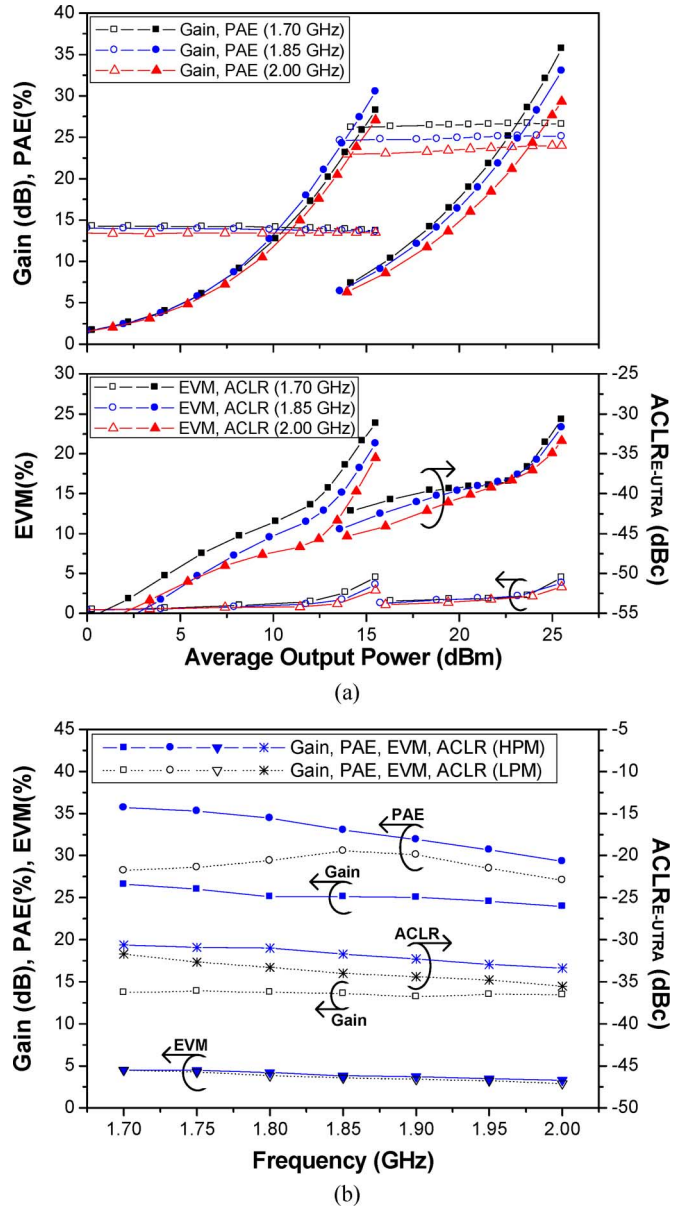


Fig. 20. Measured performance of the proposed standalone PA with 3.4-V Vcc and 16-QAM 7.5-dB PAPR LTE signal. (a) Gain, PAE, EVM, and $\rm ACLR_{E-UTRA}$ performances versus the power sweep. (b) Measured performances across 1.7–2.0 GHz at the output powers of 25.5 dBm for HPM and 15.5 dBm for LPM, respectively.

shaping function, and $V_{\rm over}$ is the factor that changes the overdriven range, as shown in Fig. 13. The optimized Shaping 2 is applied to the circuit and the simulation that results are shown in Fig. 14. The efficiency of two-stage ET PA is higher at the back-off power level than power stage only case. However, its linearity is worse than the power-stage ET PA because the drive stage operates in the saturation region, generating the high-order distortion. The decoupling capacitors at the collector bias line cannot be employed for the ET PA because the modulated signals flow through the capacitor. Instead, the output impedance of the linear stage takes the role of the decoupling capacitors since it has low output impedance at a low frequency. The two-stage ET PA shares the collector bias line without decoupling capacitors. Therefore, the low-frequency

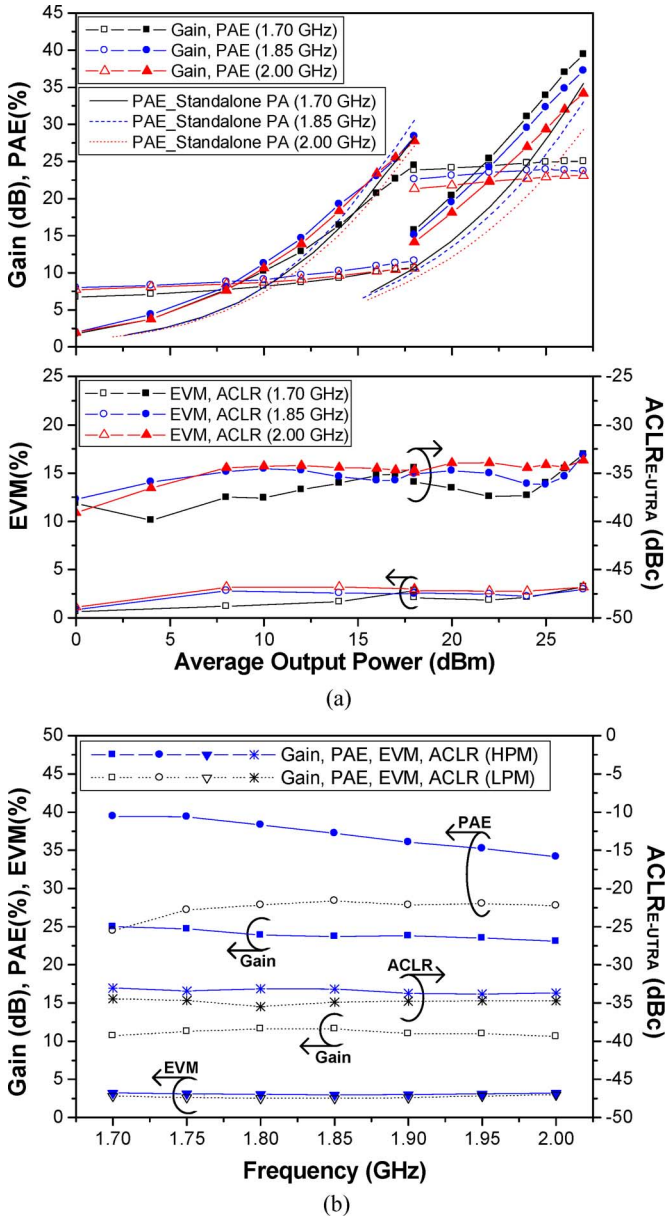


Fig. 21. Measured performance of the proposed ET PA with 16-QAM 7.5-dB PAPR LTE signal. (a) Gain, PAE, EVM, and $\mathrm{ACLR}_{\mathrm{E-UTRA}}$ performances versus the power sweep. (b) Measured performances across 1.7–2.0 GHz at the output powers of 27 dBm for HPM and 18 dBm for LPM, respectively.

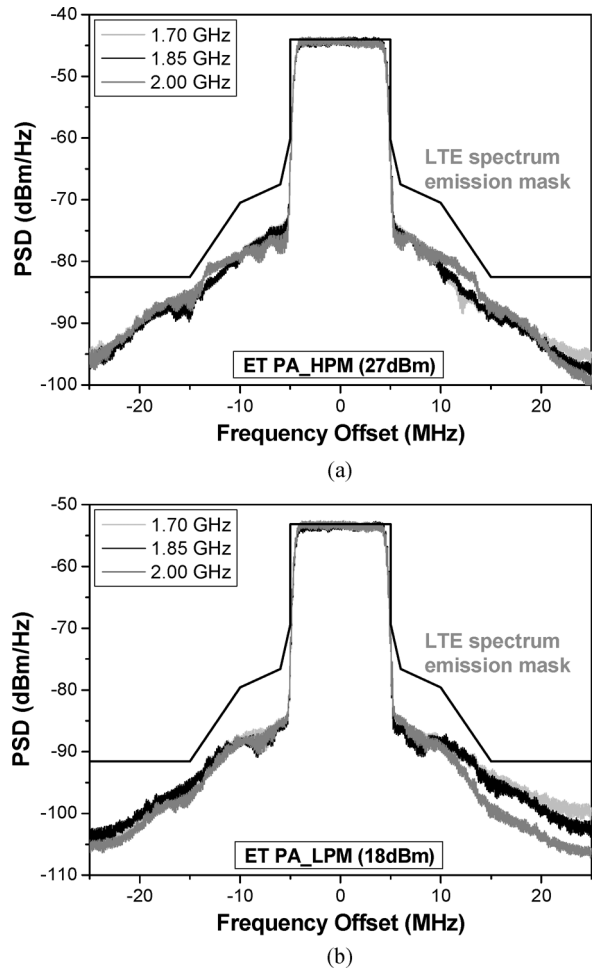


Fig. 22. (a) Measured spectrum of ET PA at an average output power of 27 dBm in HPM. (b) Average output power of 18 dBm in LPM.

distortion cannot be suppressed sufficiently and it generates the memory effect. Therefore, the third-order intermodution distortion (IMD3) is worse than the other case, as shown in Fig. 14(b). In addition, the gain drop is more severe due to the low collector bias of the drive stage at the back-off region. To get higher linearity above 20 dBm of average output power, the supply modulator is connected to the power stage.

B. Supply Modulator for Dual Power-Mode PA

The PA, which is a load for the supply modulator, can be modeled as a resistor [22]. In the dual power-mode PA, the load conditions of the HPM and LPM are quite different. In our design, the loads of the supply modulator are 7.5 and 75 Ω at the peak voltage level for the HPM and LPM, respectively. The significantly different load conditions of the two power modes deteriorate the stability of the supply modulator. To increase the phase margin, two different *RC* compensation circuits for the HPM and LPM are added in the linear stage between the AB biasing circuit and buffer, as shown in Fig. 15(a). The phase margins of the two power modes, which have 92° and 104° of the HPM and LPM, respectively, secure the stability, as depicted in Fig. 15(b). In the supply modulator, the sizes of the switch stage and the linear stage are optimized for 7.5 Ω of load condition for HPM. When it operates in the LPM, the load condition changes from 7.5 to 75 Ω and its output current is reduced drastically. The difference of load condition degrades the efficiency of the supply modulator in the LPM.

In the design of the supply modulator, the load of HPM is fixed at the average value of the envelope. However, the current consumed by PA is proportional to the input signal voltage the load does not change much during the ET operation. The LPM PA has about 20-mA quiescent current, which is two times lower than HPM PA. However, the PA operates up to peak current level of 60 mA, which is ten times lower than HPM. The LPM load at the peak voltage is about ten times larger than HPM case. However, at the low power region, the LPM PA draws more current and the load resistance somewhat decreased. Fig. 16 shows

TABLE I
PERFORMANCE COMPARISON OF RECENTLY REPORTED LTE HANDSET PAs

Ref.	Technology	PAPR/BW	Frequency	Pout (dBm)	PAE (%)	$\mathrm{ACLR1_{UTRA}}^*$ (dBc)	$\mathrm{ACLR_{E-UTRA}}^*$ (dBc)	EVM (%)
TMTT 2012 [25]	0.15-μm CMOS, HBT	6.6 dB/20 MHz	2.535 GHz	18	15†	–	–	–
				29	43‡	-49‡	–	1.9‡
BCTM 2011 [5]	HBT/pHEMT	– /10 MHz	1.95 GHz	16	24	-39	–	–
				27.5	38	-39	–	–
JCASII 2011 [6]	HBT/pHEMT	– /10 MHz	835 MHz	17	18.9	–	-31.6	2.84
				27	34.5	–	-31.2	2.97
TMTT 2010 [21]	65-nm CMOS, HBT	7.5 dB/10 MHz	1.7 – 2.0 GHz	18	12 – 13†	–	35 – 36†	2.5 – 3.5†
				27.8	33.3 – 39	–	34 – 36†	2.5 – 3.5
This Work	0.18-μm CMOS, HBT/pHEMT	7.5 dB/10 MHz	1.7 – 2.0 GHz	10	10.2 – 11.3	–	-34.5 – -37.5	1.2 – 3.1
				18	24.5 – 28.4	–	-34.5 – -34.9	2.5 – 2.9
				27	34.2 – 39.5	–	-33.1 – -33.7	2.9 – 3.2

*LTE specifications : $\mathrm{ACLR1_{UTRA}} < $ -33 dBc, $\mathrm{ACLR_{E-UTRA}} <$ -30 dBc.
†graphically estimated ‡with DPD

the load conditions (R_{LOAD}) of the HPM and LPM, and efficiencies of the supply modulator versus the envelope voltage with the load conditions. In the simulation, efficiencies of the supply modulator at the peak output voltage is 80.4% with 7.5-Ω load (HPM condition) and is 52.9% with 75 Ω load (LPM condition).

V. IMPLEMENTATION AND MEASUREMENT

The proposed dual power-mode and multi-band PA is fabricated using co-integration of the InGaP/GaAs HBT and the AlGaAs/InGaAs enhancement/depletion-mode (E/D-mode) pseudomorphic high electron-mobility transistor (pHEMT) process. The emitter areas of the low power stage, drive stage, and power stage are 720, 720, and 5760 $\mu\mathrm{m}^2$, respectively. The switched capacitor for the LPM/HPM control is built using the pHEMT device, which has 500 μm of gate width. The two capacitors at the output are external components. The inductors are replaced by bondwires and spiral inductors on the chip. The boosted supply modulator is fabricated using a CMOS 0.18-μm process with thick oxide I/O devices for high-voltage operation and all the circuit blocks are integrated on the chip, except the large inductor. The two chips are mounted on an FR-4 printed circuit board. A chip photograph is shown in Fig. 17 and its sizes are 1.2 mm × 1.2 mm and 1.35 mm × 1.35 mm for the PA and supply modulator, respectively.

Fig. 18 shows that the simulated and measured results of the PA with a constant supply voltage of 3.4 V are in good agreement with each other, except for $S_{2,1}$ of the HPM. Although some mismatch in the inter-stage matching causes the variation of $S_{2,1}$, the performance of the PA is still acceptable across 1.7–2.0 GHz, in which the uplink LTE bands I–IV are located. With the supply voltage of 3.4 V, the quiescent currents of the drive-stage and power-stage PAs are 23 and 48 mA, respectively, in the HPM. The quiescent current of the low-power stage is 19 mA in the LPM. PAE, gain, and R_{LOAD} are measured with the supply voltage swept from 1.4 to 4.5 V at a 1.85-GHz continuous wave (CW) signal, and the expected PAE and R_{LOAD} for the ET operation are depicted in Fig. 19. The R_{LOAD} trajectories show 7.5-Ω load for the HPM and 75-Ω load for the LPM, as expected.

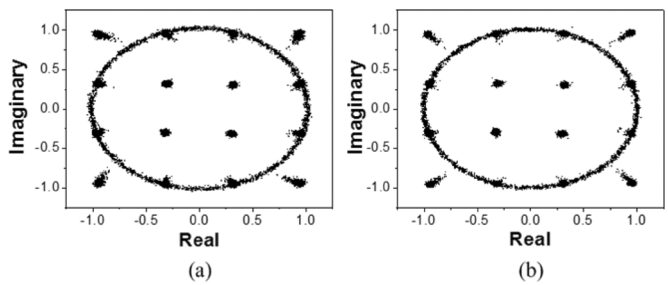


Fig. 23. Measured EVM plot of ET PA at 1.85 GHz. (a) Measured HPM EVM of 2.9% at an average output power of 27 dBm. (b) Measured LPM EVM of 2.5% at an average output power of 18 dBm.

Fig. 20 shows the measured performance across the 1.7–2.0-GHz frequency band with a 10-MHz BW 16 quadrature amplitude modulation (QAM) 7.5-dB PAPR LTE signal. With the supply voltage of 3.4 V, the standalone PA in the HPM delivers a gain of 24–26.6 dB, a PAE of 29.3%–35.7%, an error vector magnitude (EVM) of 3.3%–4.3%, and an evolved universal terrestrial radio access adjacent channel leakage ratio ($\mathbf{ACLR_{E-UTRA}}$) from −30.6 to −33.4 dBc at an average output power of 25.5 dBm. $\mathrm{ACLR_{E-UTRA}}$ is measured with a 9-MHz resolution BW at both a center frequency and a 10-MHz offset and its specification is −30 dBc. In the LPM, the PA delivers a gain of 13.5–13.6 dB, a PAE of 27.1%–30.6%, an EVM of 2.9%–4.3%, and an $\mathrm{ACLR_{E-UTRA}}$ from −31.7 to −35.5 dBc at an average output power of 15.5 dBm. The HPM and LPM of the standalone PA are designed for ET operation with the boosted supply modulator to deliver peak average output powers of 27 and 18 dBm, respectively. The drive stage is operated with the supply voltage of 3.4 V, and the power stage and the low power stage are connected to the boosted supply modulator for the ET operation. As shown in Fig. 21, the dual power-mode ET PA has a gain of 23.1–25 dB, a PAE of 34.2–39.5%, an EVM of 2.9–3.2%, and an $\mathrm{ACLR_{E-UTRA}}$ from −33.1 to −33.7 dBc at an average output power of

27 dBm in the HPM and a gain of 13.5–13.7 dB, a PAE of 24.5%–28.4%, an EVM of 2.5%–2.9%, and an $\mathrm{ACLR_{E-UTRA}}$ from -34.5 to -34.9 dBc at an average output power of 18 dBm in the LPM. To compare the performance, the PAE curves of the standalone PA are shifted 1.5 and 2.5 dB respectively, to offset the power of the HPM and LPM. The efficiencies at the low power levels in the LPM and HPM are improved significantly by the ET operation. Since the supply modulator is optimized for the HPM, the efficiency at the peak power level of LPM is a little degraded compared to the standalone PA case. However, the EVM and $\mathrm{ACLR_{E-UTRA}}$ at the peak power of the LPM are improved by about 3 dBc, thanks to the linearizing envelope-shaping method [22]. Fig. 22 shows the measured spectra, satisfying the standard spectrum mask at an average output power of 27 dBm for the HPM and 18 dBm for the LPM, respectively. Fig. 23 shows the measured EVM plots of 2.9% and 2.5% at the HPM and LPM, respectively. Table I summarizes the measured results and compares them with the previously reported results among LTE handset PAs. Although the proposed PA covers the multi-band across the 1.7–2.0 GHz, it deliveries higher efficiency at the overall output power level in comparison to recent works. To the best of the authors' knowledge, this work proposes the first dual power-mode structure supporting multi-band and ET for both HPM and LPM.

VI. Conclusion

A dual power-mode and multi-band ET PA, with a shunt switched capacitor for the mode control, has been developed. Without the series switch or impedance transformer for the signal path selection, the PA delivers good power performance with low control loss. The PA can also cover the broad BW across the 1.7–2-GHz frequency. The dual power-mode ET PA has a gain of 23.1–25 dB, a PAE of 34.2%–39.5%, an EVM of 2.9%–3.2% and an $\mathrm{ACLR_{E-UTRA}}$ of -33.1–-33.7 dBc at an average output power of 27 dBm for the LTE signals having BW of 10 MHz and PAPR of 7.5 dB. In the LPM, the ET PA has a gain of 13.5–13.7 dB, a PAE of 24.5–28.4%, an EVM of 2.5–2.9%, and an $\mathrm{ACLR_{E-UTRA}}$ of -34.5–-34.9 dBc at an average output power of 18 dBm. The highly efficient PA, in conjunction with the boosted supply modulator, achieves good results at all average output power regions. The proposed dual power-mode ET PA can be operated for multi-mode signals such as WCDMA and EDGE by employing the supply modulator with a programmable hysteretic comparator [18], [21]. These data indicate that the dual power-mode ET PA structure is a promising architecture for handset PA applications.

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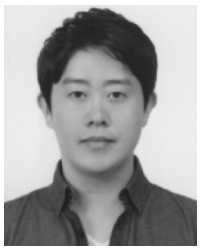

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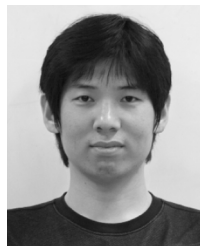

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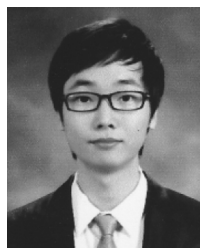

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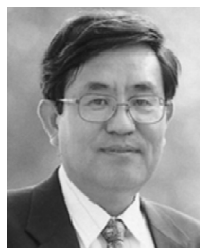

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