A Reconfigurable *K*-/*Ka*-Band Power Amplifier With High PAE in 0.18-μm SiGe BiCMOS for Multi-Band Applications

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***Abstract*—This paper presents a high power efficient broad-band programmable gain amplifier with multi-band switching. The proposed two stage common-emitter amplifier, by using the current reuse topology with a magnetically coupled transformer and a MOS varactor bank as a frequency tunable load, achieves a 55.9% peak power added efficiency (PAE), a peak saturated power of +11.1 dBm, a variable gain from 1.8 to 16 dB, and a tunable large signal 3-dB bandwidth from 24.3 to 35 GHz. The design is fabricated in a commercial 0.18-μm SiGe BiCMOS technology and measured with an output 1-dB gain compression point which is better than +9.6 dBm and a maximum dc power consumption of 22.5 mW from a single 1.8 V supply. The core amplifier, excluding the measurement pads, occupies a die area of 500 μm $\times$ 450 μm.**

***Index Terms*—Current reuse, dual band, *K*-band, *Ka*-band, power added efficiency (PAE), SiGe BiCMOS, transformer coupled load, tunable amplifier, variable gain amplifier (VGA).**

I. Introduction

In THE RECENT decade, the rising demand in short-range high-speed wireless communication systems have nurtured the development of radio frequency (RF) integrated circuit design for the diversified K-band (18–27 GHz) and Ka-band (26.5–40 GHz) applications such as 24 GHz industrial scientific and medical (ISM) band gigabit-per-second wireless systems [1], wireless sensor network [2], point-to-point communication (18–23 GHz) [3], local multipoint distribution service (27.5–29.5 GHz) [4], and short-range (22–29 GHz) automotive radar applications for anti-collision detection [5], [6].

The power amplifier (PA) design often involves the tradeoff between the efficiency and linearity. This limitation can be mitigated by using several design techniques such as the stacked amplifier design proposed in [7] that supports a large signal swing to increase the output power by alleviating the high frequency device's low V_{beo} at the cost of large supply voltage. An alternative design technique is the switched mode PA in which the circuit operation adapts dynamically based on instantaneous characteristics (amplitude, phase, frequency) of the input signal such as the class E in [8] and class $\mathrm{F}^{-1}/\mathrm{F}$ in [9] that minimizes power in the amplifying transistors by avoiding overlap between the current and voltage waveforms by using the digital ON/OFF switches. However, such designs require special linearization techniques to reduce the nonlinearities introduced by the output harmonics of the switching distorted waveforms. In contrast, PA design is also based on continuous power control such as adaptive biasing technique implemented in [10] and by using load impedance modulation technique of the Doherty PA in [11]. However, these PA design techniques involve large dynamic range complex circuitry that consumes additional dc power. An implementation technique to enhance PA efficiency as well as linearity is by reducing the losses involved in the interconnects and passive components by using distributed structure equivalents in physical layout such as Wilkinson couplers [12] and the thin-film micro-strip lines (MSL) [13] as the power splitter/combiner between multiple PA stages, the substrate-shielded coplanar waveguide (CPW) structures [14], the transmission line transformers (TLT) [3], and the substrate-shielded MSL [6], [15]. However, these distributed structures occupy a large die area. The amplifier power efficiency can be improved by using various current-reused topologies [16] such as the capacitive-coupling [17], the inter-stage LC series resonance, and the transformer-coupling. The transformer-based LC tank has been already proposed in the design of various transceiver building blocks such as the voltage controlled oscillator (VCO) [18], low noise amplifier (LNA) [19], and Class-F PA [20]. The work in [17] presents an inductor load based current-reused LNA at Ku-band with an efficiency of up to 37%.

In this paper, a SiGe BiCMOS based K-/Ka-band digitally controlled variable gain amplifier (DVGA) with multiple frequency tunable bands is proposed, designed and verified by on-wafer measurement. This work is extended from [21] to include the physical implementation details of the loaded tank circuit, together with a detailed analysis of its quality factor (Q) enhancement, and henceforth the resulting improvement in the overall amplifier PAE of 55.9% and the linearity performance. The proposed design improves power efficiency by simultane-

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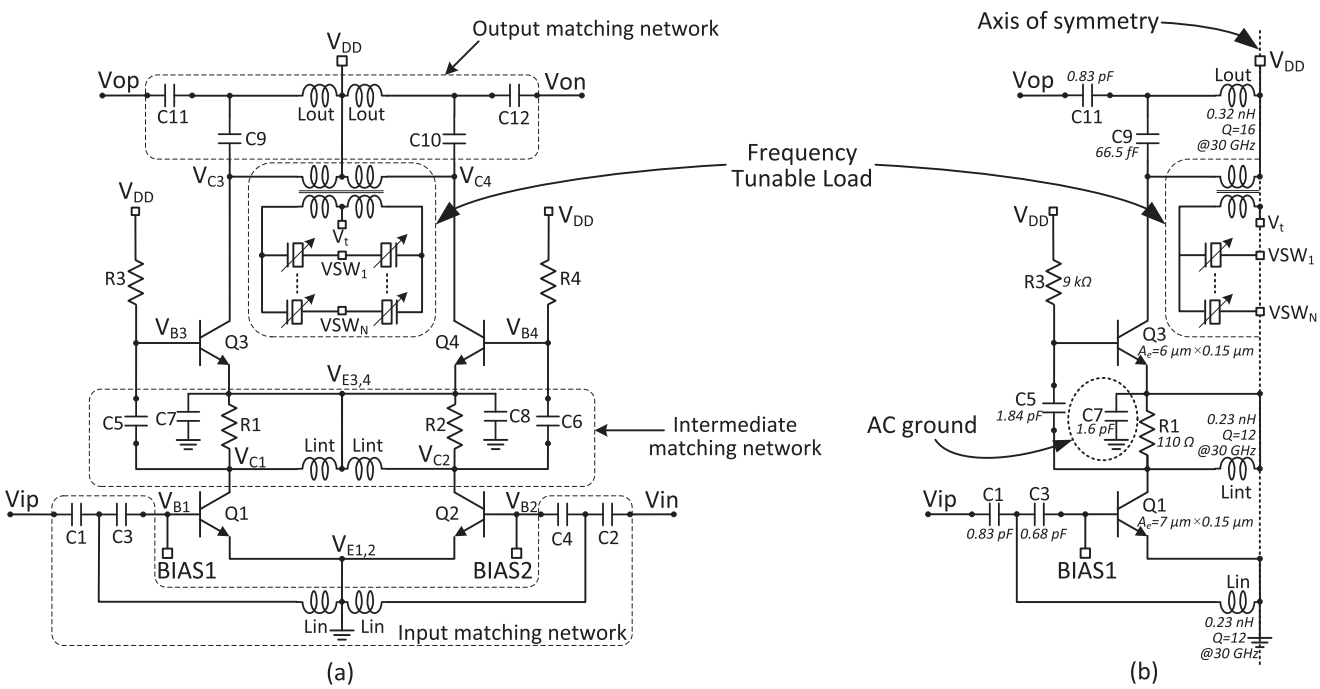


Fig. 1. Circuit schematic of (a) the proposed reconfigurable multi-band amplifier and (b) half circuit equivalent.

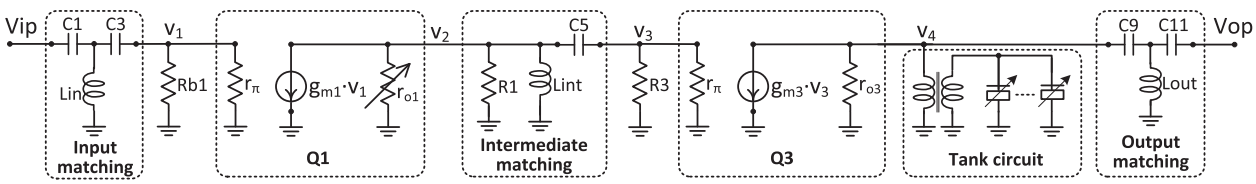


Fig. 2. Hybrid-π small signal half circuit equivalent of the proposed reconfigurable multi-band amplifier.

ously reducing the overall dc power consumption using the current reuse technique and improving the amplifier linearity by using a loaded tank circuit's enhanced Q. The proposed design provides a variable gain control, frequency-band switching, wideband small signal gain flatness, low power consumption, improved linearity, and high PAE.

This paper is organized as follows. Section II describes the detailed analysis of the proposed amplifier circuit. The detail implementation of the frequency tunable load is explained in Section III. Section IV discusses about the load tank circuit's Q-factor enhancement resulting in improvement of proposed amplifier's linearity and PAE performance. The design analysis is verified in Section V by on-wafer measurement with the performance comparison of this work against the state-of-the-art K-/Ka-band amplifiers. Finally, the paper conclusion is provided in Section VI.

II. Circuit Analysis

The circuit schematic of the proposed multi-band tunable amplifier is a fully differential two-stage ac cascaded and dc stacked common emitter amplifier as shown in Fig. 1(a). The first stage is a DVGA with a four bit ($B_3 \sim B_0$) digital gain control and the second stage is a frequency tunable amplifier. The block depicted as the frequency tunable load is the tank circuit that consists of an integrated 2-coil spiral transformer and the varactor bank. The inductors and the transformer used in the proposed differential circuit are chosen with center tap configuration to significantly improve the die area utilization. The capacitors $C7/C8$ provide the ac ground for second stage differential amplifier.

The circuit in Fig. 1(a) is symmetric and can be folded along the vertical axis of symmetry as shown in Fig. 1(b). By replacing the transistors with the hybrid-π model of the $Q1/Q2$ and $Q3/Q4$ transistors and re-arranging the circuit components in Fig. 1(b), the small signal equivalent half-circuit of the proposed tunable amplifier is obtained as shown in Fig. 2.

A. Variable Gain Amplifier Stage Analysis (A_{v1})

The output power of the proposed tunable amplifier can be adjusted by varying the gain of the first stage amplifier using the four digital bits ($B_3 \sim B_0$). Based on Figs. 2 and 3, the amplifier gain of first stage is given as

$$A_{v1}(s) = g_{m1} \cdot \frac{V_{A1}}{\left[\left(\frac{\beta_f}{\lambda_0}\right) \cdot \left(\sum_{n=0}^{3} B_n \cdot I_n \cdot 2^n + I_{\min}\right)\right]} \quad (1)$$

where transconductance g_{m1}, early voltage V_{A1}, the common-emitter forward current gain $\beta_f (= I_{C1}/I_{B1})$, and the output resistance's ($r_{o1} \approx V_{A1}/I_{C1}$) degradation factor due to transistor saturation λ_0 with ($0 < \lambda_0 \leq 1$) are indicated for the transistor pair $Q1/Q2$, the constant coefficients of the estimated

linear gain function $I_n (n = 0 \text{ to } 3)$, the digital gain control configuration as received from the digital controller or the digital baseband B_n $(n = 0 \text{ to } 3)$, and $I_{\min}$ which is the dc current corresponding to the amplifier minimum gain when all the digital control bits B_n are reset $(= 0\ \text{V})$.

The gain control based on the base bias current variation of the first stage amplifier in the stacked structure mainly affects the output resistance r_{o1} and does not significantly alter the transconductance (g_{m1}) of the HBT pair $Q1/Q2$ [17].

From the variable gain control bias circuit shown in Fig. 3, the mirrored variable base biasing currents through the nodes BIAS_T $(T = 1 \text{ and } 2)$ has to be properly matched to avoid offset errors in the first stage differential amplifier. Unlike voltage biasing of amplifiers, the current biasing circuit provides a gain control along with the power down (PD) capability. The maximum limited input signal level at BIAS_1 and BIAS_2 nodes provides a small voltage fluctuation at the drain of the PMOS current mirror transistors which continues to operate in the strong saturation region by generating almost same bias currents. Hence the induced nonlinearity effect due to input signal on the input transistor's bias currents is very minimal.

B. Frequency Tunable Amplifier Stage Analysis (A_{V2})

The second stage amplifier gain from Fig. 2 is based on the fixed biasing transconductance (g_{m3}) of the $Q3/Q4$ transistor pair [21] and frequency tunable load impedance $Z_L(s)$ as

$$A_{v2}(s) = g_{m3} \cdot [r_{03} \| Z_L(s)]\,. \tag{2}$$

From Fig. 4(a), the load impedance of the second stage amplifier is determined by a high Q-factor transformer with the primary coil (L_p) which is magnetically coupled (M) to an LC tank circuit built by using the transformer secondary coil (L_s) and the varactor bank (C_{vT}). This load impedance is connected in parallel to the output matching network and the influence of the tank circuit on output matching is described in the following section. The transformer used in the load circuit can be represented as a T-network based on [22] and also the varactor bank can be modeled as a series combination [23] of the capacitor C_{vT} and varactor loss r_{vT} as shown in Fig. 4(b). By using loop analysis of the network in Fig. 4(b), we obtain the load impedance as (3) shown at the bottom of the page.

1) Varactor Bank Q-Factor: The varactor bank, as viewed from the transformer secondary coil [shown in Fig. 4(a)], consists of the parallel connected variable capacitors with equivalent impedance Z_v. The equivalent lumped circuit model of the varactor bank impedance Z_v as determined by [23] is shown in Fig. 5. The varactor bank impedance consisting of N identical varactors is given by

$$Z_v = \frac{1}{N \cdot Y_1} = \frac{r_v}{N} - \frac{j}{N \cdot \omega \cdot C_v}. \tag{4}$$

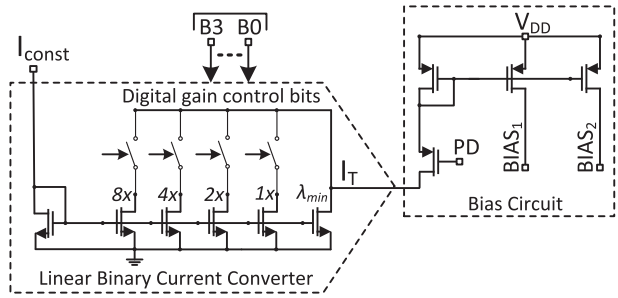


Fig. 3. Variable gain control base biasing circuit.

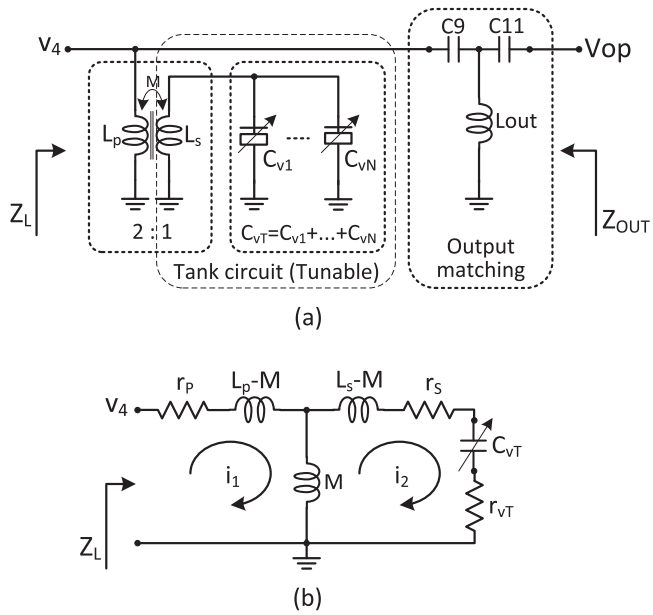


Fig. 4. (a) Tunable load (transformer and MOS-varactor bank) with output matching network. (b) T-section model of transformer with MOS-varactor.

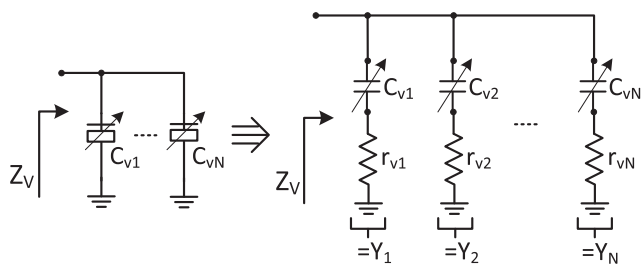


Fig. 5. Varactor bank with equivalent lumped circuit model.

From (4), the varactor bank Q-factor is

$$Q_{CvT} = -\frac{\text{Im}(Z_v)}{\text{Re}(Z_v)} = \frac{1}{\omega \cdot C_v \cdot r_v} = Q_{Cv}. \tag{5}$$

$$Z_L(s) = \frac{s^3 \cdot \left[\left(L_P L_S - M^2\right) \cdot C_{vT}\right] + s^2 \cdot \left[\left(r_P L_S + r_S L_P + r_{vT} L_P\right) \cdot C_{vT}\right] + s \cdot \left(L_P + r_P \cdot \left(r_S + r_{vT}\right) \cdot C_{vT}\right) + r_P}{\left(s^2 \cdot L_S \cdot C_{vT} + s \cdot \left(r_S + r_{vT}\right) \cdot C_{vT} + 1\right)} \tag{3}$$

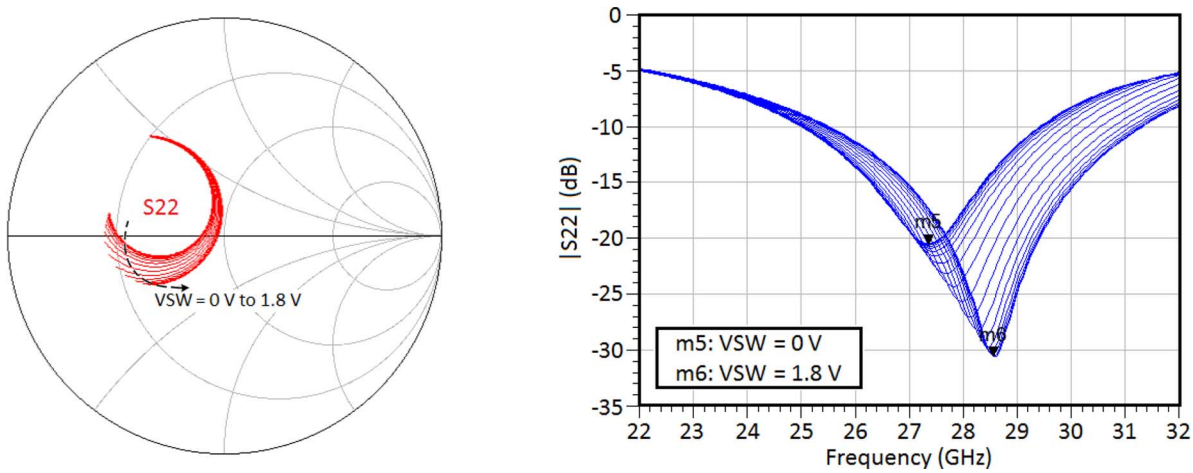


Fig. 6. Simulation plots of output matching by tuning the tank circuit load with $\mathrm{VSW}(\mathrm{VSW}_1 = \mathrm{VSW}_2)$ varied together from 0 V to 1.8 V (step = 0.1 V).

Based on (5) it is deduced that by connecting any number of varactors (N) in parallel for the tunable tank circuit, the Q-factor contribution from the varactor bank is almost fixed.

2) Transformer Secondary Coil Q-Factor: The transformer secondary coil's Q-factor is given as

$$Q_{Ls} = \frac{\omega_n \cdot L_s}{r_S}. \tag{6}$$

3) Overall Tank Circuit Q-Factor: For the tunable load impedance transfer function as given in (3), we can deduce that

$$\omega_n^2 = \frac{1}{L_S \cdot C_{vT}} \tag{7}$$

$$\omega_n \cdot Q_{\mathrm{tank}} = \frac{1}{(r_S + r_{vT}) \cdot C_{vT}} \tag{8}$$

where ω_n is the angular resonant frequency and Q_{tank} is the overall tank circuit Q-factor.

By re-arranging (8), the overall tank Q-factor is given as

$$Q_{\mathrm{tank}} = \frac{1}{(r_S + r_{vT})} \cdot \sqrt{\frac{L_S}{C_{vT}}}. \tag{9}$$

The overall tank Q-factor [24] based on the individual Q-factors of the inductance and the varactor bank is given by

$$Q_{\mathrm{tank}} = \frac{Q_{Ls} \cdot Q_{CvT}}{Q_{Ls} + Q_{CvT}}. \tag{10}$$

By using (5) and (6) in (10) we get

$$Q_{\mathrm{tank}} = \frac{\omega_n \cdot L_s}{r_S + r_{vT}} = \frac{1}{(r_S + r_{vT})} \cdot \sqrt{\frac{L_s}{C_{vT}}}. \tag{11}$$

The overall tank Q-factor as determined by (9) is the same as (11). Furthermore, the Q-factor of second-stage amplifier response in (2) is mainly determined by transformer secondary coil and a single identical varactor of the varactor-bank.

Hence, the overall Q-factor of the second stage amplifier load is obtained by considering the mutual magnetic coupling due to the in-phase currents of the transformer primary coil and the induced current from the secondary coil shunted with the varactor bank. This enables the design to be scalable in frequency with a voltage controlled tuning range.

By assuming a negligible effect of the large shunt bias resistors $Rb1$ and $R3$ on the small signal analysis, the overall multi-band tunable amplifier gain (A_v) is determined by the gain product of the cascaded stages as

$$A_v(s) = \frac{g_{m1} \cdot V_{A1} \cdot g_{m3} \cdot [r_{03} \| Z_L(s)]}{\left[\left(\frac{\beta_f}{\lambda_0}\right) \cdot \left(\sum_{n=0}^{3} B_n \cdot I_n \cdot 2^n + I_{\min}\right)\right]}. \tag{12}$$

From (12), we can infer that the frequency response of the overall proposed amplifier gain is a function of the four bit digital gain control configuration $(B_3 \sim B_0)$ as well as the tunable varactor control voltage $(\mathrm{VSW}_1 = \mathrm{VSW}_2 = \mathrm{VSW})$.

C. Impedance Matching Analysis

The amplifier input and output terminals are matched to 100-Ω differential impedance by using T-networks as shown in Fig. 1(a). The intermediate matching network which is also the first stage amplifier's load is L-network and its passive component values, including the inductor L_{int} and de-Q resistors $(R1/R2)$, are optimized for better amplifier gain flatness. Based on the amplifier circuit topology, the output return loss is mainly determined by the output matching network as well as the load tunable tank circuit. By using the frequency band selection $(\mathrm{VSW}_1 \sim \mathrm{VSW}_2)$ bits of the load tank circuit, an adaptive output return loss is achieved as shown in Fig. 6. This allows the output return loss to be frequency band reconfigurable unlike the input return loss which is almost unaffected by the tank circuit tuning. The bandwidth for both the frequency bands are governed by the output matching network's loaded Q-factor as well as the tank Q-factor.

III. Frequency Tunable Load Design

The frequency tunable load in the second stage amplifier consists of a 2-coil center tap transformer and a MOS varactor bank connected to the secondary coil as shown in Fig. 7. The primary and secondary coils of the transformer are built on the same plane with edge coupling to avoid formation of a broadside coupled parasitic capacitance between the coils. Hence it shifts the tank circuit self-resonance to a higher frequency. The transformer coils are oriented in non-inverting mode [22] and are implemented by using the top metal layer (with thickness

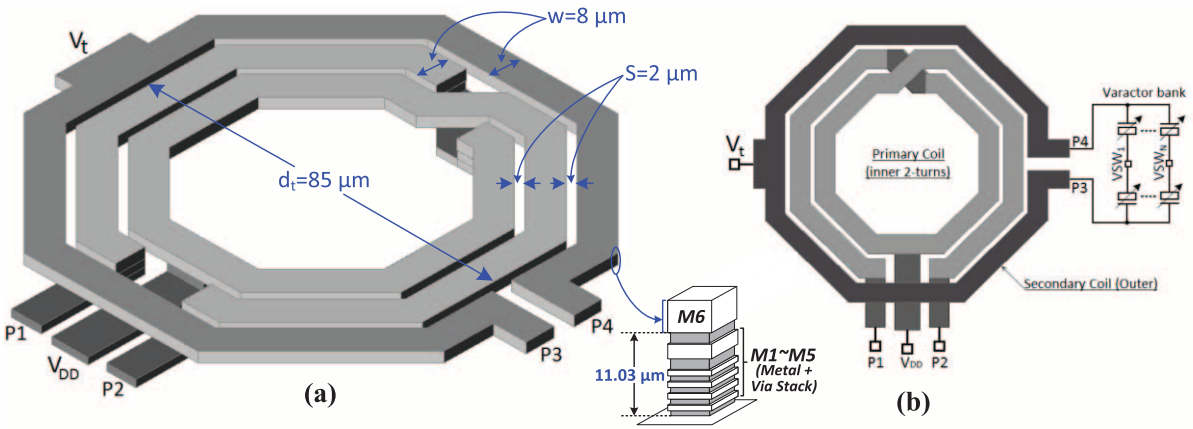


Fig. 7. Transformer layout (a) 3D view and (b) top view with interface to the varactor bank.

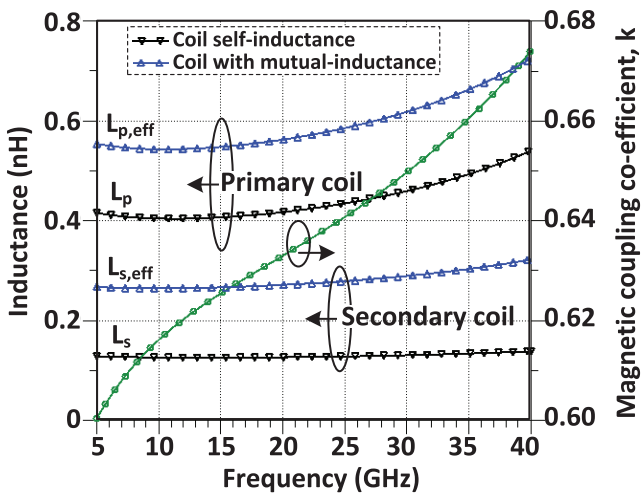


Fig. 8. EM simulation plot of the designed transformer's primary and secondary coil inductance along with the coupling coefficient against the standalone inductance.

of 2.81 μm and sheet resistance of 10.5 m$\Omega/\square$) as supported in the fabrication process to achieve a high Q-factor. The transformer's primary outer coil size is 85 μm, the secondary coil size is 105 μm, the uniform coil width is 8 μm, and the coil spacing is 2 μm (shown in Fig. 7). The transformer is designed and optimized using the Agilent ADS Momentum 2.5D EM simulator in RF mode to estimate the desired primary and secondary coil inductance over the entire operating frequency range as shown in Fig. 8. The transformer design does not include any kind of shielding structures.

When compared to the scheme with a standalone inductive load, the transformer by using a magnetic coupling coefficient k provides an enhanced Q-factor that increases the effective secondary coil inductance as given by

$$L_{s,\text{eff}} = L_s \cdot (1 + 2k)\,. \tag{13}$$

The transformer in the proposed design has turns ratio of 2:1 which is also evident in Fig. 7. Hence the ratio of primary coil inductance to secondary coil inductance by assuming almost equal sized coils is 4:1. This assumption is also validated by the inductance plot obtained from the EM simulation as shown in Fig. 8.

The work in [18] claims that for a same area constraint, there is no Q-improvement for transformer tank resonator as compared to a standalone inductor tank resonator which is not completely agreeable for the planar transformer with in-phase current orientation. Since in this work [18], the limitations such as reduction of the coil inductance by increasing its width and spacing as well as the loss contributions of the tank circuit capacitors are neglected. Moreover, due to the increased effective coil inductance by the magnetic coupling, the length of the coil can be reduced to provide the same inductance value as a standalone inductor in the required frequency range. This reduces the resistive loss associated with the transformer coil and eventually enhances the Q-factor due to the transformer coupled tank circuit as compared to the standalone load inductor.

The varactor bank is parallel-connected MOS varactors that are operating in the accumulation mode with the gate-source tuning voltage (V_{gs}) ranging from -0.9 to $+0.9$ V to traverse across the C_{MIN} to C_{MAX} value, respectively. To avoid negative external tuning voltages at the varactor source/drain terminals $(\text{VSW}_1 \sim \text{VSW}_2)$, the varactor gate voltage is level-shifted to $+0.9$ V through the secondary transformer's center tap (V_t) as shown in Fig. 7(b). This ensures a positive external voltage ranging from 0 to 1.8 V to be used as the varactor tuning voltage (VSW) with the capacitance tuning characteristics as shown in Fig. 9(a). The simulation plots in Fig. 9(a) and (b) are obtained for N identical varactors connected in parallel against the same varactor tuning voltage $(\text{VSW}_N \approx \text{VSW})$. From Fig. 9(a), the equivalent capacitance adds up as the number of identical varactors (N) in parallel increases. An interesting observation noticed in the varactor bank Q-factor plot, shown in Fig. 9(a), is the equivalent Q-factor of the varactor bank which is unaffected by any number of parallel connected varactors (N). This behavior agrees with (5) as described in Section III. This is one of the merits of this proposed design and the amplifier operating frequency range can be easily reconfigured based on the number of varactors in parallel (N) as shown by the intrinsic tank frequency plot in Fig. 9(b). As the number of varactors (N) in the varactor-bank increases, the main design trade-off taken into consideration is the shrinking of the tunable frequency range due to the increased tank minimum capacitance value which is limited by $(N \cdot C_{\text{MIN}})$.

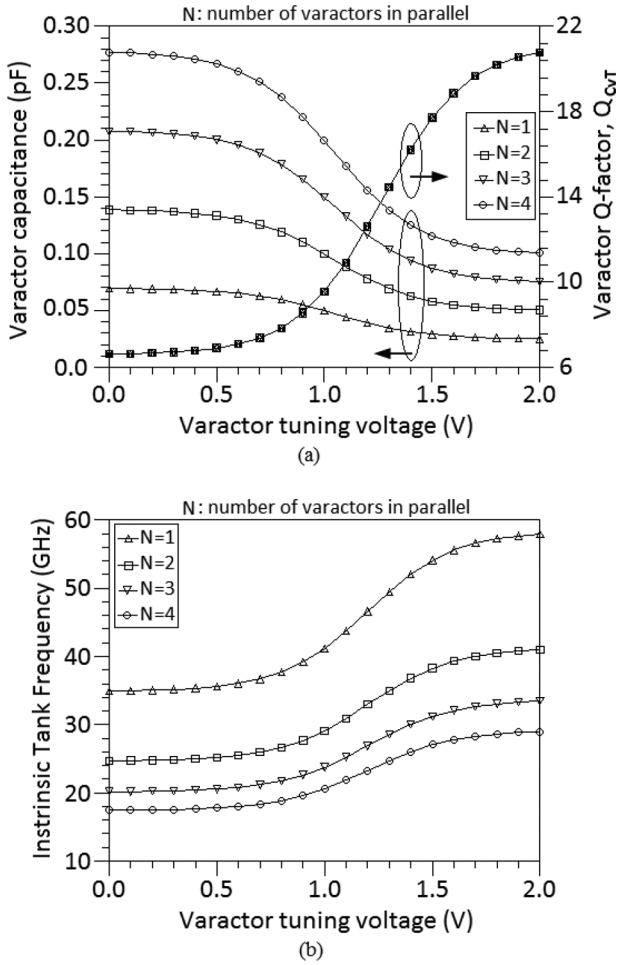


Fig. 9. Simulation plots at 30-GHz frequency of the designed varactor's (a) capacitance and quality factor and (b) intrinsic tuned tank frequency.

The variation [23]of the varactor capacitance C_{vT} by the tuning voltage VSW_N ($N = 1, 2$, etc.) is defined as

$$C_{vT} = C_{\mathrm{MIN}} + dC_{vT0}\left(1 + \tanh\left(\frac{V_t - \mathrm{VSW}_N - dV_{gs0}}{V_{gsnorm}}\right)\right) \quad (14)$$

where, C_{MIN} is the minimum capacitance value of varactor, dC_{vT0} is the varactor tuning range, dV_{gs0} is the range of gate bias at which C_{vT} has a maximum variation for VSW_N, V_{gsnorm} determines the normalized bias voltage range.

From (3), (7), (12) and (14) we can infer that by changing C_{vT} using a corresponding varactor tuning voltage VSW_N ($N = 1$, 2, etc.), the center frequency of the overall amplifier frequency response can be tuned.

IV. Q-Factor Enhancement

As evident from the simulation plot in Fig. 10, the loaded tank Q-factor (Q_{tank}) is enhanced under two conditions namely,

A. Loaded Tank Q-Enhancement From Q_{t2} to Q_{t1}

The loaded tank Q-factor curves from Q_{t2} to Q_{t1} in Fig. 10 are obtained by reducing the transformer size of the primary outer coil (d_t) from 94 to 85 μm and the secondary coil

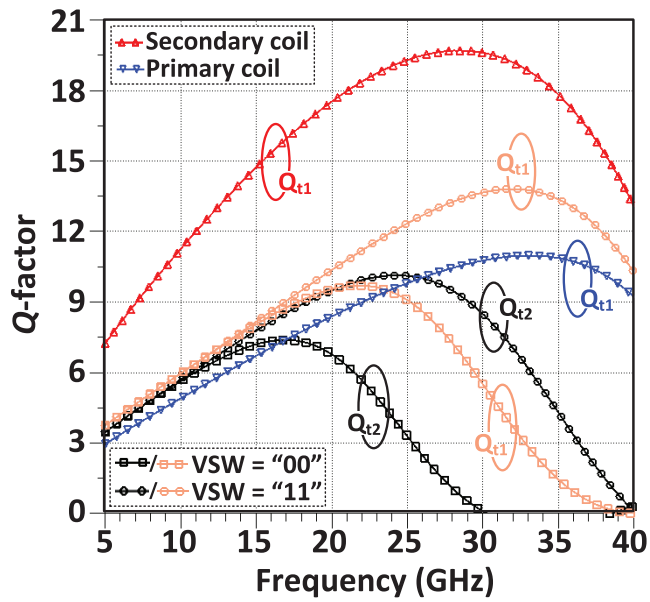


Fig. 10. Simulated single-ended open circuit (self-inductance) and varactor bank loaded tank Q-factor for two versions of the transformer primary coil size (d_t) and the MOS varactor length (l_v) as $Q_{t1}(d_t = 85\ \mu\mathrm{m}, l_v = 500\ \mu\mathrm{m})$ and $Q_{t2}(d_t = 94\ \mu\mathrm{m}, l_v = 650\ \mu\mathrm{m})$.

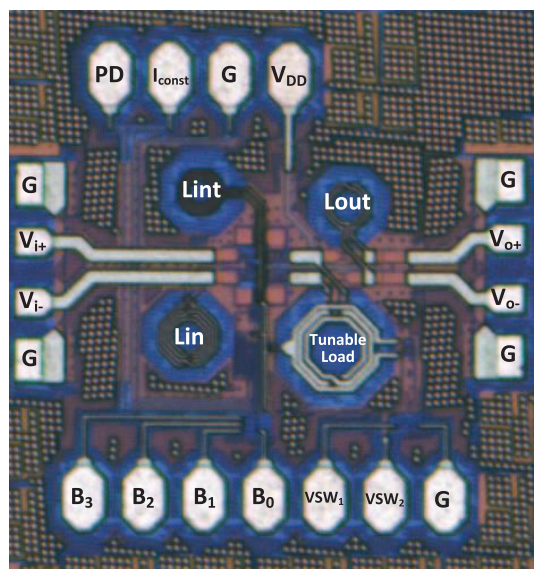
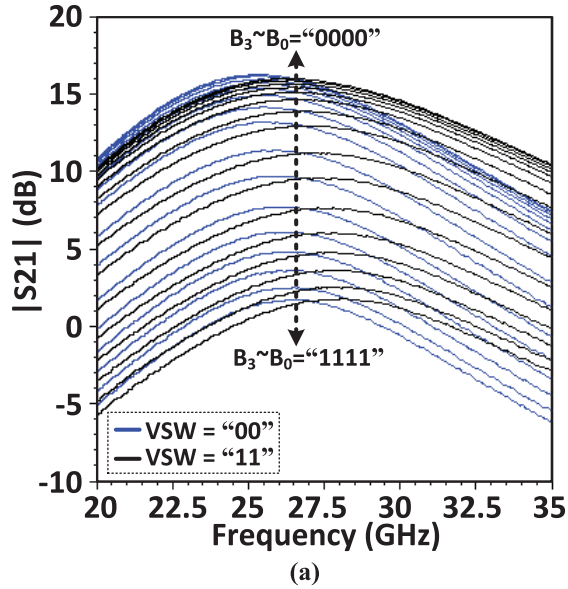


Fig. 11. Microphotograph of proposed multi-band amplifier with tunable load (Core area: 500 × 450 μm^2, Total area with I/O pads: 890 × 810 μm^2).

size from 114 to 105 μm as well as by concurrently decreasing the MOS varactor-bank's channel length (l_v) from 650 to 500 μm. From Fig. 10, the Q_{tank} curves from Q_{t2} to Q_{t1} are upshifted both along the frequency as well as the peak value. Both these observations can be illustrated by considering the simultaneous reduction of the tank circuit component dimensions (d_t and l_v) from Q_{t2} to Q_{t1} that results in a frequency upshift due to the decreased $(L_s \cdot C_{vT})$ product according to (7) as well as an increased Q_{tank} peak value by the resulting decreased resistive losses r_S and r_{vT} as discussed in (9) and (13).



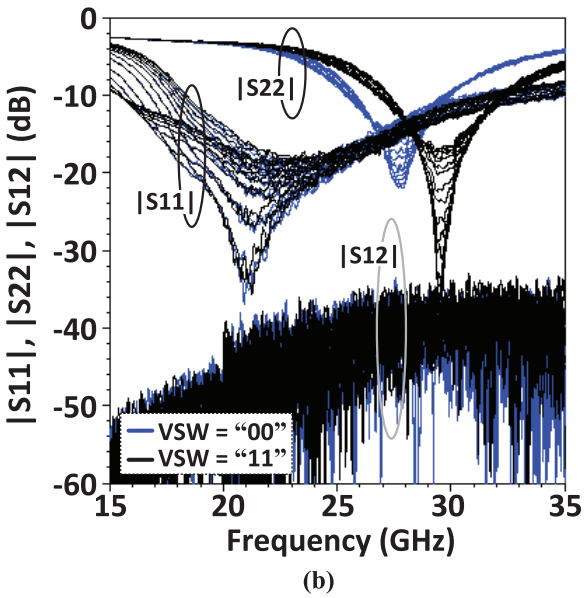


Fig. 12. Measured S-parameter variation based on $B_3 \sim B_0$ (16 steps), band switch based on VSW (2 steps) (a) gain and (b) return loss and isolation.

B. Loaded Tank Q-Enhancement By Band-Select Input VSW From "00" to "11" Configuration

From Fig. 10, we also observe that, for either of the curves Q_{t1} or Q_{t2}, the frequency upshifts for band-select input VSW configuration switching from "00" to "11" as well as the peak $Q_{\rm tank}$ value is enhanced. This can be analytically justified by considering the intrinsic tank frequency (ω_n) characteristics and the MOS varactor bank's Q-factor (Q_{CvT}) as shown in Fig. 9(b) and (a), respectively for an increase in the VSW voltage from 0 to 1.8 V.

Both these Q-factor enhancements simultaneously improves the proposed amplifier's PAE, linearity and the peak gain performance by reducing the tank circuit losses which are also evident from the on-wafer measurement results.

The choice of the proposed transformer coil dimensions and the varactor bank aspect ratios are mainly determined by considering the fact that the peak of the loaded resonant tank Q-factor is positioned within the pass-band of the amplifier's interested frequency range. Hence we can mitigate the complicated tank circuit analysis by neglecting the high-order effects of transformer secondary coil loaded by the capacitive varactor bank [19].

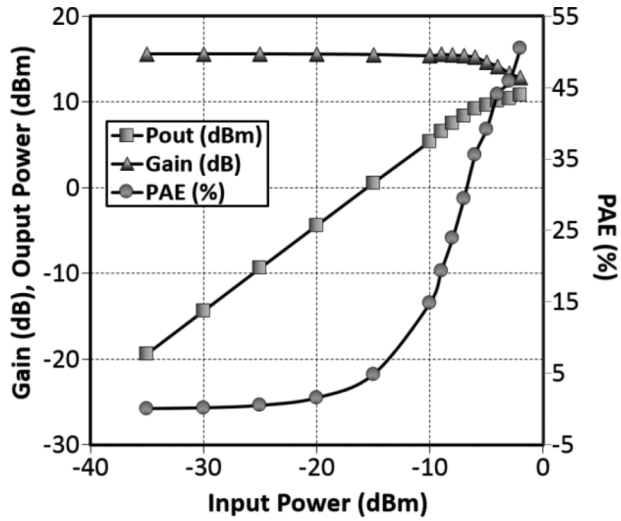


Fig. 13. Large signal measurement plot of the proposed tunable amplifier at 29.5 GHz frequency, maximum gain setting, and band #2 (VSW = "11").

V. Experimental Results

The proposed K-/Ka-band frequency tunable DVGA is implemented in a 0.18-μm SiGe BiCMOS process from Tower Jazz Semiconductors. The microphotograph of the proposed amplifier in the fabricated wafer is shown in Fig. 11 which occupies an overall die area of 0.89 mm $\times$ 0.81 mm including the on-wafer probing pads. The proposed design performance is experimentally verified by using on-wafer probing with the Agilent E8364B PNA network analyzer that supports a 4-port calibration and mixed mode scattering parameter measurement by avoiding the use of any balun. The proposed amplifier consumes a total dc current ranging from 9.9 to 12.5 mA for the maximum to minimum gain variation, respectively during its normal operation mode $(PD = 0$ V) and during the power down mode $(PD = 1.8$ V) dissipates a dc current of 106 μA from a single 1.8 V supply voltage. The gain reduction with an increase in the bias current is due to the transition of first stage amplifying transistors $(Q1/Q2)$ from active region (maximum gain) towards saturation region (minimum gain).

The measurement setup consists of wafer probe station with two RF GSSG probes for probing the amplifiers' differential input and output, along with a 7-pin dc probe that provides a 4-bit digital gain control $(B_3 \sim B_0)$ signal along with a 2-bit frequency band selection $(\mathrm{VSW}_1 \sim \mathrm{VSW}_2)$ input, and individual dc probes for supply voltage $(V_{DD} = 1.8$ V), the base bias circuit constant current $(I_{\rm const} = 50\ \mu$A), and the power down mode control (PD) as marked in Fig. 11. The digital pins namely $B_3 \sim B_0$, $\mathrm{VSW}_1 \sim \mathrm{VSW}_2$ and PD are applied with dc voltages of either 0 V (for bit "0") or 1.8 V (for bit "1").

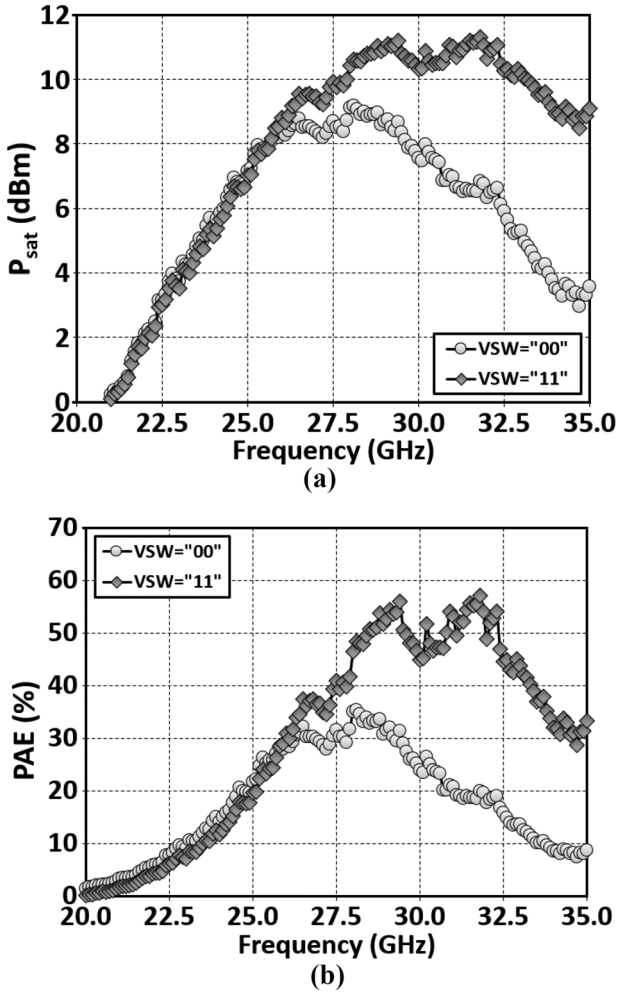


Fig. 14. Measured linearity performance over the two bands (VSW) of the proposed design with maximum gain ($B_3 \sim B_0$ = "0000") (a) $P_{\rm sat}$ and (b) PAE.

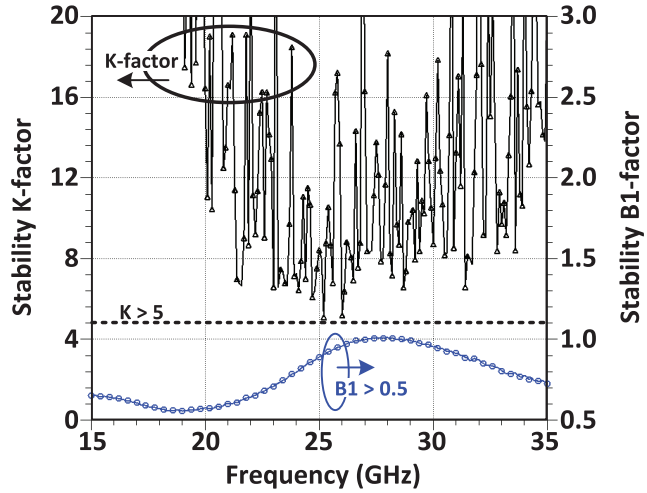


Fig. 15. Measured stability factors of the proposed amplifier design for the maximum gain and band #1 condition.

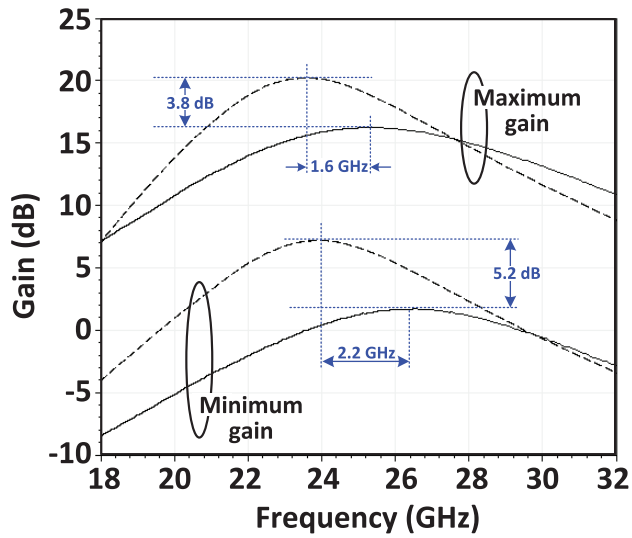


Fig. 16. Simulated (dashed line) and measured (solid line) gain of proposed design for maximum/minimum gain conditions band#1 (VSW = "00").

The variable gain control using the four gain control bits $B_3 \sim B_0$ of the proposed amplifier is verified by the measured S-parameters shown in Fig. 12(a) and (b). Additionally, Fig. 12 indicates the frequency band switching functionality of the proposed amplifier that is achieved by providing a same voltage to $\rm VSW_1 \sim VSW_2$ pins (together depicted as VSW). By providing option for dual-band switching, the center frequency of the gain response can be changed. The small-signal gain's 3-dB bandwidth can support K-band by selecting band#1 (VSW = "00") and Ka-band using band#2 selection (VSW = "11"). Additionally, a $\pm$0.75 dB small signal gain flatness is achieved for a frequency ranging from 22.67 to 30.2 GHz across both the frequency bands.

The high Q transformer coupled load along with the current reuse topology of the proposed design provides a high gain and an improved linearity performance together with low dc power consumption. This results in an output 1-dB gain compression point ($\rm OP_{1\ dB}$) of +9.6 dBm for the band#2 (VSW = "11"), and the maximum gain condition ($B_3 \sim B_0$ = "0000") at a measured frequency of 29.5 GHz as shown in Fig. 13.

The measured $P_{\rm sat}$ and PAE (with a +11.1 dBm peak saturated power and 55.9% peak PAE) of the proposed tunable amplifier over the two switchable frequency bands based on VSW and maximum gain setting ($B_3 \sim B_0$ = "0000") are shown in Fig. 14(a) and (b), respectively. Both these plots indicate that the linearity and PAE performance are improved for band#2 (VSW = "11") by considering the tank circuit load Q enhancement as illustrated in Fig. 10.

Although, the peak output power in both the configurations is comparative by only about 1.9 dB difference as well as the amplifier performance with VSW = "00" configuration is also comparable with the state-of-the-art performance to support dual band reconfigurability. Hence the configuration of VSW = "00" is necessary which also highlights the merit of this dual-band amplifier design.

Based on this proposed power down method, there is a possibility to turn on the input transistors, $Q1/Q2$ under power down (PD) mode by a large input signal power level of at least +8 dBm. This signal level is much larger than the input $P_{\rm 1\ dB}$ point of the proposed amplifier design under normal dc bias condition. Hence by providing the same limitation on the input power

TABLE I
PERFORMANCE SUMMARY OF WIDEBAND K-/KA-BAND DRIVE POWER AMPLIFIERS

	Frequency (GHz)	Gain (dB)	OP_{1dB} (dBm)	Peak P_{sat} (dBm)	Peak PAE (%)	Power (mW)	Voltage [dc] (V)	Die area (mm^2)	Technique / Topology	Technology
[25]	24	19	15.7	19	24.7	-	± 3.6	0.56 × 0.67	reverse body bias	0.18-µm CMOS
[12]	16.5 to 28	37.6	15**	19.4	22.3	228	2.4	2 × 1	driver + 2 parallel PA	0.18-µm SiGe HBT
[10]	20 to 25	11.9	15.4	17.4	12	108	3.6	0.83 × 0.48	adaptive bias	0.18-µm CMOS
[13]	24	8	20	22	20	504	3.6	0.6 × 0.7	4-way combining PA	0.18-µm CMOS
[9]	24 to 31	10.3	15	17.1	40.7	-	2.2	0.6 × 0.45	1-stage class F^{-1}/F	0.13-µm SiGe HBT
[15]	31.9 ± 2.4	46.8	15.4	19.4	6.18	1410	2.5/1.4	3.5 × 4	4-way combining + MSL[¥]	0.12-µm SiGe HBT
[26]	17 to 35	12	21~22	22.5~23.5	30~40	498	4	1.5 × 1	binary combining PA	0.15-µm pHEMT
[14]	22.9 to 26	7	11	14.5	6.5	280	2.8	0.7 × 1.8	substrate-shielded CPW[€]	0.18-µm CMOS
[8]	20 ± 3**	26	-	10.2	20.5	52.5	1.5	0.9 × 0.4	class E + mode locking	0.13-µm CMOS
[7]	35 to 40**	5.2	14.5/17.5	20.2/21.4	11.2/7	-	3.6/4.4	0.28	stacked cascode	45-nm SOI CMOS
[3]	18 to 33	15.2	16	19.5	10.2	711	3.6	1.41 × 0.61	darlington + TLT[£]	0.18-µm CMOS
[6]	27 ± 1.5**	14.5	-	14	13.2	169.2	1.8	0.7 × 1.2	substrate-shielded MSL[¥]	0.18-µm CMOS
This work	**24.3 to 32.4***	**1.7 to 16.3**	**8.3**	**9.2**	**35.3**	**22.5**	**1.8**	**0.89 × 0.81**	**current reuse + tunable load**	**0.18 µm SiGe HBT**
	25.8 to 35*	**1.8 to 16**	**9.6**	**11.1**	**55.9**					

*large signal -3dB bandwidth, **estimated value from the measurement plot, [£]transmission line transformer, [¥]micro-strip line, [€]coplanar waveguide

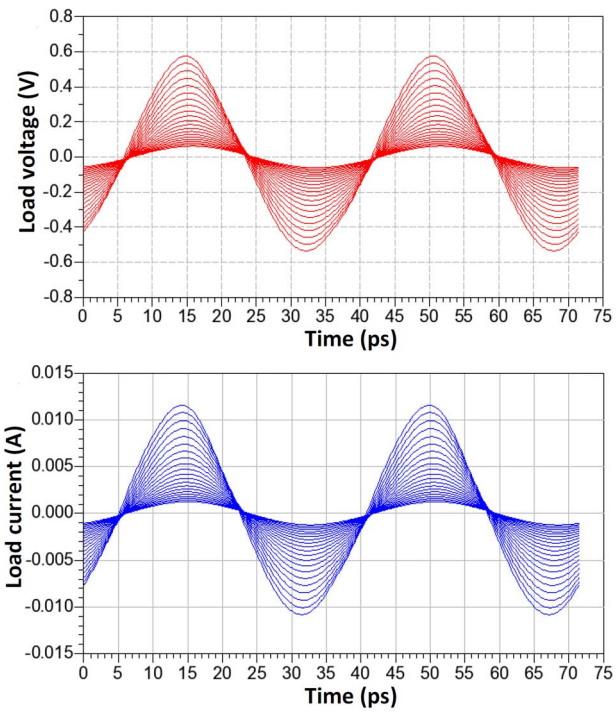


Fig. 17. Simulated load voltage and load current waveforms at 28 GHz with VSW = "00" configuration for band #1 against input power sweep from −35 to −10 dBm (step = 1 dB).

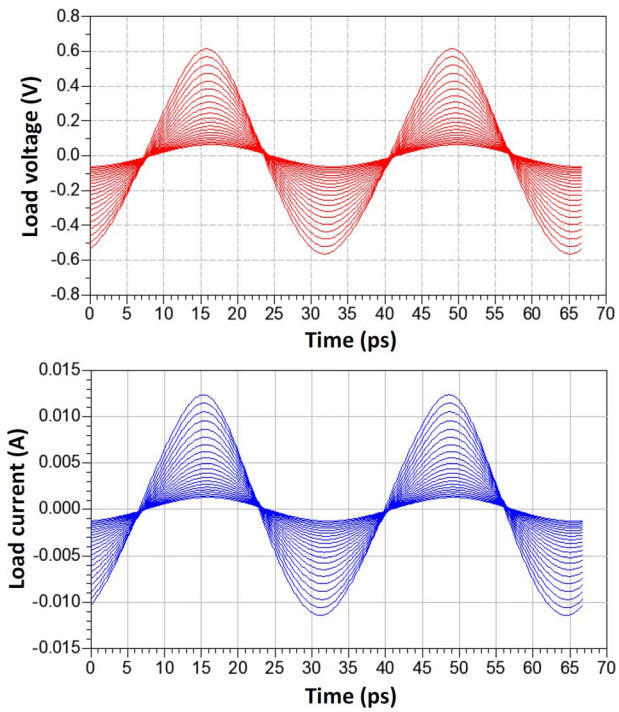


Fig. 18. Simulated load voltage and load current waveforms at 30 GHz with VSW = "11" configuration for band #2 against input power sweep from −35 to −10 dBm (step = 1 dB).

level as boundary condition we can still achieve the power down using the proposed method.

The stability factors ($K$and $B1$) extracted from measured S-parameters shown in Fig. 15 indicates that the proposed amplifier has unconditional stability over the operating frequency range. The difference between the simulation and measurement results as shown in Fig. 16 for the maximum and minimum gain condition can be attributed to the transistor and varactor model inaccuracy at such high frequencies.

The simulation load voltage and load current waveforms at each of the band based on VSW configuration for input power sweep indicates that the proposed dual band amplifier design operates in linear region as shown in Figs. 17 and 18 for a large input power level of −10 dBm which is close to the input $P_{1\ \mathrm{dB}}$ point.

The performance of the proposed multi-band amplifier is consolidated in Table I and compared with the state-of-the-art K-/Ka-band monolithic amplifier designs. By using dc current reuse topology along with a high Q frequency tunable transformer coupled load and a variable gain control option, the PAE and the overall amplifier performance is improved as compared to other works in Table I. It is also evident that the amplifier's linearity performance (P_{sat} and $\mathrm{OP}_{1\ \mathrm{dB}}$) in other works are mainly achieved by using a larger supply voltage (increased headroom) and also high dc power consumption that supports the large signal drive capability.

Although the proposed amplifier design has enhanced PAE performance as compared to the state-of-the-art works, the high linearity performance becomes a hard limit and a major concern in power amplifier specifications and reconfigurable devices.

VI. Conclusion

This paper presents a high power efficient broadband DVGA with reconfigurable dual-band switching capability to support K-band (18–27 GHz) satellite communication, short range 24 GHz ISM (22–29 GHz) automotive radar system and Ka-band (26.5–40 GHz) applications. In this work, the tunable loaded tank circuit Q-factor enhancement along with the variable gain control, and the frequency-band switching of the proposed amplifier, together with their resulting improvement on PAE and linearity performance are theoretically analyzed and experimentally verified.

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References

[1] T. Tokumitsu, "K-band and millimeter-wave MMICs for emerging commercial wireless applications," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 11, pp. 2066–2072, Nov. 2001.

[2] I. Gresham *et al.*, "Ultra-wideband radar sensors for short-range vehicular applications," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 9, pp. 2105–2122, Sep. 2004.

[3] C.-W. Kuo, H.-K. Chiou, and H.-Y. Chung, "An 18 to 33 GHz fully-integrated darlington power amplifier with guanella-type transmission-line transformers in 0.18 μm CMOS technology," *IEEE Microw. Wirel. Compon. Lett.*, vol. 23, no. 12, pp. 668–670, Dec. 2013.

[4] M. K. Siddiqui, A. K. Sharma, L. G. Callejo, and R. Lai, "A high power and high efficiency monolithic power amplifier for LMDS applications," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 12, pp. 2226–2232, Dec. 1998.

[5] FCC, Washington, DC, USA, "First report and order, revision of part 15 of the commission's rules regarding ultra wideband transmission systems ET Docket 98–153," 2002.

[6] J.-W. Lee and S.-M. Heo, "A 27 GHz, +14 dBm CMOS power amplifier using 0.18 μm common-source MOSFETs," *IEEE Microw. Wirel. Compon. Lett.*, vol. 18, no. 11, pp. 755–757, Nov. 2008.

[7] J.-H. Chen, S. R. Helmi, and S. Mohammadi, "A fully-integrated Ka-band stacked power amplifier in 45 nm CMOS SOI technology," in *Proc. IEEE Topical Meet. Silicon Monolithic Integr. Circuits RF Syst.*, Jan. 2013, pp. 75–77.

[8] C. Cao, H. Xu, Y. Su, and O. K. Kenneth, "An 18-GHz, 10.9-dBm fully-integrated power amplifier with 23.5% PAE in 130-nm CMOS," in *Proc. 31st Eur. Solid-State Circuits Conf.*, Sep. 2005, pp. 137–140.

[9] S. Y. Mortazavi and K.-J. Koh, "A class F-1/F 24-to-31 GHz power amplifier with 40.7% peak PAE, 15 dBm OP 1 dB, and 50 mW Psat in 0.13 μm SiGe BiCMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, San Francisco, CA, USA, Feb. 2014, pp. 254–255.

[10] N. -. Kuo, J.-C. Kao, C.-C. Kuo, and H. Wang, "K-band CMOS power amplifier with adaptive bias for enhancement in back-off efficiency," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4.

[11] E. Kaymaksut and P. Reynaert, "Transformer-based uneven Doherty power amplifier in 90 nm CMOS for WLAN applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1659–1671, Jul. 2012.

[12] K. Kim and C. Nguyen, "A 16.5–28 GHz 0.18-μm BiCMOS power amplifier with flat 19.4 $\pm$1.2 dBm output power," *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, no. 2, pp. 108–110, Feb. 2014.

[13] P.-C. Huang, J.-L. Kuo, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "A 22-dBm 24-GHz power amplifier using 0.18-μm CMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Anaheim, CA, USA, May 2010, pp. 248–251.

[14] A. Komijani, A. Natarajan, and A. Hajimiri, "A 24-GHz, +14.5-dBm fully integrated power amplifier in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1901–1908, Sep. 2005.

[15] P. J. Riemer, J. S. Humble, J. F. Prairie, J. D. Coker, B. A. Randall, B. K. Gilbert, and E. S. Daniel, "Ka-band SiGe HBT power amplifier for single chip T/R module applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1071–1074.

[16] V. Giammello, E. Ragonese, and G. Palmisano, "A transformer-coupling current-reuse SiGe HBT power amplifier for 77-GHz automotive radar," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1676–1683, Jun. 2012.

[17] T. B. Kumar, K. Ma, and K. S. Yeo, "A Ku-band variable gain LNA with high PAE in 0.18 μm SiGe BiCMOS technology," *IEEE Microw. Wirel. Compon. Lett.*, submitted for publication.

[18] H. Krishnaswamy and H. Hashemi, "Inductor- and transformer-based integrated RF oscillators: A comparative study," presented at the IEEE Custom Integr. Circuits Design Conf., San Jose, CA, USA, Sep. 2006.

[19] Y. Xiaohua and N. M. Neihart, "Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multitap transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1236–1246, Mar. 2013.

[20] K. K. Sessou and N. M. Neihart, "An integrated 700–1200-MHz class-F PA with tunable harmonic terminations in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1315–1323, Apr. 2015.

[21] T. B. Kumar, K. Ma, and K. S. Yeo, "A low power programmable gain high PAE K-/Ka-band stacked amplifier in 0.18 μm SiGe BiCMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Phoenix, AZ, USA, May 2015, pp. 1–4.

[22] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[23] K.-H. Tsai and S.-I. Liu, "A 104-GHz phase-locked loop using a VCO at second pole frequency," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 1, pp. 80–88, Jan. 2012.

[24] L. Li, P. Reynaert, and M. Steyaert, "Design and analysis of a 90 nm mm-wave oscillator using inductive-division LC tank," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1950–1958, Jul. 2009.

[25] J.-L. Kuo and H. Wang, "A 24 GHz CMOS power amplifier using reversed body bias technique to improve linearity and power added efficiency," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Montreal, QC, Canada, Jun. 2012, pp. 1–3.

[26] P. C. Huang, Z. M. Tsai, K. Y. Lin, and H. Wang, "A 17–35 GHz broadband, high efficiency pHEMT power amplifier using synthesized transformer matching technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 112–119, Jan. 2012.

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