A +31.5 dBm CMOS RF Doherty Power Amplifier for Wireless Communications

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***Abstract*—A fully differential Doherty power amplifier (PA) is implemented in a 0.13-μm CMOS technology. The prototype achieves a maximum output power of +31.5 dBm with a peak power-added efficiency (PAE) of 36% (39% drain efficiency) with a GMSK modulated signal. The PAE is kept above 18% over a 10 dB range of output power. With a GSM/EDGE input signal, the measured peak output power while still meeting the GSM/EDGE mask and error vector magnitude (EVM) requirements is +25 dBm with a peak PAE of 13% (PAE is 6% at 12 dB back-off). Instead of using a bulky $\lambda/4$ transmission line, a passive impedance inverter is implemented as a compact lumped-element network. All circuit components are fully integrated on a single CMOS die except for an off-chip capacitor for output matching and baluns. The die size is 2.8 $\times$ 3.2 mm^2 including all pads and bypass capacitors.**

***Index Terms*—CMOS RF, Doherty amplifier, power amplifier, wireless communication.**

I. Introduction

GROWTH in the wireless communication market in recent years has been driving the demand for higher integration of wireless transceivers in order to achieve lower cost, smaller form factor, and more functionality. One possible solution to meet this demand is to increase the level of transceiver integration by using a low-cost CMOS technology [1], [2]. After years of research effort, System-on-Chip (SoC) integration has recently been demonstrated in some wireless applications, such as Wireless LAN and Bluetooth [3], [4]. Even in highly demanding applications such as cellular communications, a high level of integration has been achieved, dramatically reducing the number of ICs and discrete components [5]. However, SoC integration has not yet been achieved for these high-performance transceivers; a major roadblock has been the integration of the power amplifier (PA).

Due to the vastly inferior performance of CMOS PA implementations, most existing wireless transceivers that require high output power resort to using discrete PAs which are usually implemented in more costly technology such as GaAs or LDMOS. PAs in these technologies offer much better performance than their CMOS counterparts, but they are not amendable to high integration. This work focuses on demonstrating design techniques to implement a highly-integrated linear and efficient PA in deep-submicron CMOS technology, which can potentially be integrated with the rest of the transceiver. A concept first developed in the vacuum tube era by Doherty [6] to improve amplifier efficiency over a wide range of output power is applied. A prototype is described, embodying a fully differential Doherty PA in 0.13-μm CMOS technology. The prototype was designed to operate in the DCS-1800 band for both GSM and GSM/EDGE. The achieved output power is +31.5 dBm with GMSK modulation and +25 dBm of output power with EDGE modulated signal. All components are integrated on a single CMOS die except for a capacitor in the output matching network and baluns.

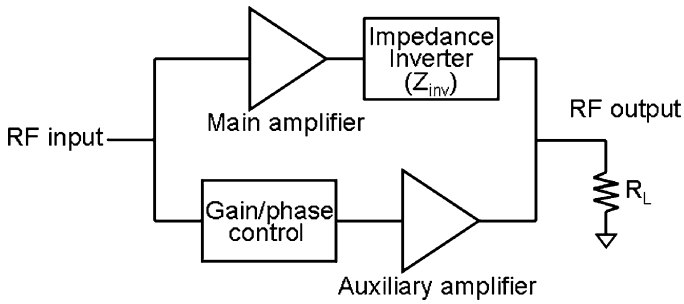

Fig. 1. Block diagram of Doherty amplifier.

Section II discusses requirements and issues in PA design along with enhancement techniques to improve CMOS PA performance. Section III describes the Doherty PA architecture that is used to improve PA power efficiency and addresses many circuit level implementation issues. The Doherty CMOS PA prototype and several circuit techniques are described in Sections IV and V. Section VI presents the measurement results from the prototype, followed by a brief conclusion in Section VII.

II. Power Amplifier Design

In most existing wireless applications, high data-rate transmission is desirable. As frequency bands are a scarce resource, spectrally efficient modulation schemes are utilized to permit more data to be transmitted within a given bandwidth. These modulation schemes carry information in the forms of amplitude and phase and therefore have non-constant envelope. Radio transceivers used in these applications must have sufficient linearity in order to faithfully transmit and receive the signal. Nonlinearities in the transceiver can increase the bit error rate of the received signal, thus corrupting the integrity of the wireless communication link.

Unlike digital circuit design, which continually benefits from CMOS technology scaling, analog circuit design suffers from supply voltage diminution and several short-channel effects. This is particularly significant for PA design where

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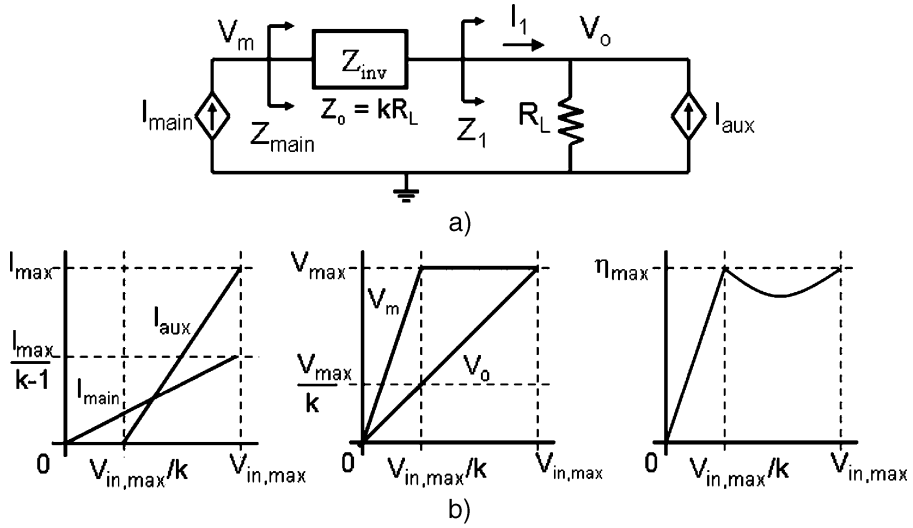

Fig. 2. (a) Simplified schematic diagram of Doherty amplifier. (b) Output current, voltage, and overall efficiency plots.

large voltage and current swings are usually desired for high output power and good power efficiency. High PA efficiency is essential for longer battery life in portable wireless devices. With linearity requirements added to its design specifications, the task of integrating a PA becomes even more challenging. In conventional PA design, there is a direct trade-off between linearity and efficiency which makes the design of a linear and efficient PA difficult. This trade-off is particularly severe in CMOS technology. To overcome this trade-off, PA enhancement techniques must be explored. These techniques can be categorized into efficiency enhancement techniques and linearization techniques [7]. Efficiency enhancement techniques attempt to improve efficiency of an inefficient linear PA, whereas linearization techniques attempt to improve linearity of an efficient nonlinear PA. The main focus of this work is to apply an efficiency enhancement technique invented by Doherty [6]. Other notable enhancement techniques include Cartesian feedback [8], adaptive predistortion, and polar modulation [9], [10]. These techniques can be used in conjunction with efficiency enhancement for further improvement of PA performance.

III. Doherty Amplifier Technique

A. Doherty Operation

A common characteristic of conventional PAs is that peak efficiency can be obtained only at peak output power. Efficiency degrades significantly as the output power decreases below peak power. Under typical operating conditions, the PA transmits much lower than its peak output power; therefore, the average power efficiency is much lower than the maximum value. The Doherty configuration consists of two sub-amplifiers, a main and an auxiliary amplifier, as shown in Fig. 1. During low output power operation, only the main amplifier is turned on. The main amplifier operates alone until its output power is limited by its maximum voltage swing, achieving the first efficiency peak. To further increase the output power, the auxiliary amplifier is also turned on. The key to this technique is the use of a passive impedance inverter network, $Z_{\rm inv}$, to combine the output power from both amplifiers in a way that achieves low losses and does not require increased voltage swings. The passive $Z_{\rm inv}$ network used in this architecture is a symmetric network which has the impedance looking into one side of the network being proportional to the reciprocal of the impedance on the other side. This can be mathematically given by

$$Z_{\rm in} = \frac{Z_o^2}{Z_L} \tag{1}$$

where $Z_{\rm o}$ is the network characteristic impedance and Z_L is the impedance seen on the opposite side of the network. The $Z_{\rm inv}$ network is conventionally implemented by a $\lambda/4$ transmission line [6], [11]. Alternatively, a lumped-element network that mimics the $\lambda/4$ line characteristic at the center frequency can also be used [6]. This lumped-element network can potentially be more suitable for integration due to its small form-factor and will be further discussed in Section IV. One inherent property of a $Z_{\rm inv}$ network is the 90° phase shift across the network. For proper power combining, a 90° phase shift is added at the input of the auxiliary amplifier to match signal delay of the two signal paths.

Fig. 2(a) depicts a simplified schematic of a Doherty amplifier. It is assumed that both amplifiers have high output impedance and can be represented by a current source. During low output power operation, the auxiliary amplifier is turned off. The load impedance seen by the main amplifier is

$$Z_{\rm main} = \frac{Z_o^2}{Z_1} = k^2 R_L. \tag{2}$$

Due to the lossless nature of the $Z_{\rm inv}$ network, the relationship between the main and auxiliary amplifier output voltages can be found from conservation of energy and is given by

$$\frac{V_o}{V_m} = \frac{Z_1}{Z_o} = \frac{Z_1}{kR_L}. \tag{3}$$

Once the main amplifier reaches its maximum output swing, the auxiliary amplifier is turned on to further increase the output

power. Once the auxiliary amplifier is turned on, the effective impedance Z_1 is no longer R_L but is

$$Z_{1,\text{eff}} = R_L\left(1+\frac{I_{\text{aux}}}{I_1}\right). \tag{4}$$

If the phase of I_{aux} is designed to be the same as that of I_1, the effective impedance Z_1 increases as I_{aux} increases. Through impedance inversion, Z_{main} decreases as I_{aux} increases, allowing the main amplifier to supply more current and, hence, power. If the magnitude of the main amplifier current is increased in the correct proportion, the output swing of the main amplifier can be kept at its peak value without saturating, allowing the main amplifier to maintain its peak efficiency operating condition. As I_{aux} increases, V_{o} also increases, as suggested by (4) and (3). Once V_{o} reaches the peak output swing, both amplifiers operate with peak efficiency and attain the second peak in the overall efficiency. Fig. 2(b) shows the main and auxiliary amplifier voltage and current plots, and the overall efficiency of the composite amplifier.

There are two approaches to achieve the auxiliary amplifier current characteristic as shown in Fig. 2(b). The first approach is a self-biasing scheme which can be achieved by biasing the auxiliary amplifier in class C mode such that it starts conducting right when the main amplifier is about to saturate. With this approach, the auxiliary amplifier device size must be made significantly larger than the main amplifier, due to its reduced conduction angle operation and its higher transconductance requirement (by a factor of k) as suggested in Fig. 2(b). Due to these reasons and the fact that a class C amplifier does not have linear transconductance, the self-biasing approach is often not effective for real implementation. An alternative is to use an adaptive biasing scheme which uses the power control information to set the amplifier bias current such that it follows the curve shown in Fig. 2(b). Even though this approach requires more control circuitry, it can potentially achieve a more effective Doherty action without using excessively large auxiliary amplifier device size.

B. Overall Linearity

The overall linearity of the Doherty amplifier can be best understood by transforming the I_{main} current source and the Z_{inv} network into a Thevenin equivalent as shown in Fig. 3. Under the assumption that the main amplifier has infinite output impedance and assuming the Z_{inv} network is lossless, this transformation results in a single voltage source across the load resistance. In this ideal situation, the amplifier's overall linearity is solely determined by the main amplifier. The function of the auxiliary amplifier is only to keep the main amplifier from saturating, so that it remains a good current source. Since the overall efficiency is a weighted average of the two amplifier efficiency, it is more beneficial to bias the auxiliary amplifier in class C mode so that the overall efficiency can be improved beyond that of the main amplifier alone. However, in reality the auxiliary amplifier cannot be made arbitrarily nonlinear. Due to the finite output impedance of the main amplifier and finite Q of the Z_{inv} network, the Thevenin voltage source may have a small impedance in series, allowing nonlinearities in the auxiliary amplifier current to leak to the load. Thus, a shallow class C amplifier is a strong candidate for the auxiliary amplifier, since it preserves a certain degree of linearity with significantly improved efficiency. This is also why the self-biasing scheme is hard to realize since the auxiliary amplifier can be very nonlinear when biased in a deep class C region, thus affecting the overall linearity, unless a good active device and Z_{inv} network are available.

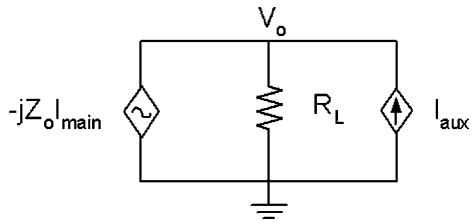

Fig. 3. Simplified schematic diagram with Thevenin equivalent.

IV. Design and Implementation

To apply the discussed concept, a prototype was designed and fabricated in a 0.13-μm CMOS process. The goal of this prototype is to achieve over +30 dBm of saturated power while maintaining high efficiency over a wide range of output power. The prototype is also designed to meet the linearity requirements of DCS-1800 GSM/EDGE standard, which has the transmit band between 1715 MHz and 1785 MHz. A block diagram of the prototype is depicted in Fig. 4. The passive impedance inverter is fully integrated by using on-chip passive components. Both amplifiers are designed to be three-staged to provide sufficient power gain so that the overall amplifier can be easily driven by the preceding circuit. Bondwire inductors are used at the output of the final stage to minimize power loss. A polyphase filter is used at the input to provide 90° phase difference between the two signal path to compensate for the phase shift from the Z_{inv} network. The output matching network consists of a pair of bondwires and an off-chip capacitor to transform the 50-Ω load impedance to approximately 8-Ω differential. All circuits are implemented differentially to minimize substrate injection and ground bounce, and to double the output swing which translates into lower current density in the output devices. As will be seen later in this section, differential topology also allows the use of a capacitive neutralization technique to help improve the amplifier linearity. Each circuit block will now be discussed in detail.

A. Passive Impedance Inverter

At low gigahertz frequencies, a $\lambda/4$ transmission line is several centimeters long and unsuitable for on-chip implementation. In order to facilitate high integration, the lumped element pi network shown in Fig. 5 is used instead. The T-equivalent of this network can also provide the impedance inversion function, but the pi network was deemed more suitable for this prototype implementation. One advantage of this topology is that the output capacitance from both amplifiers can be lumped into the network, hence reducing the required resonating inductance. The lumped network consists of three reactive components with the same magnitude of impedance. Both capacitors partially use the amplifier junction capacitance from the amplifier outputs along with additional MIM capacitors. These MIM capacitors are designed as switchable capacitor arrays in order to allow the

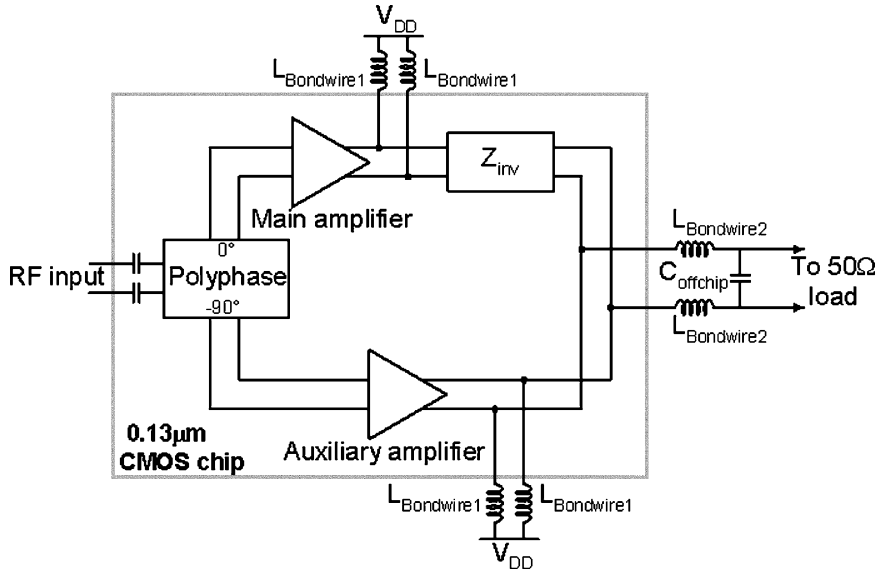

Fig. 4. Block diagram of the CMOS RF Doherty PA prototype.

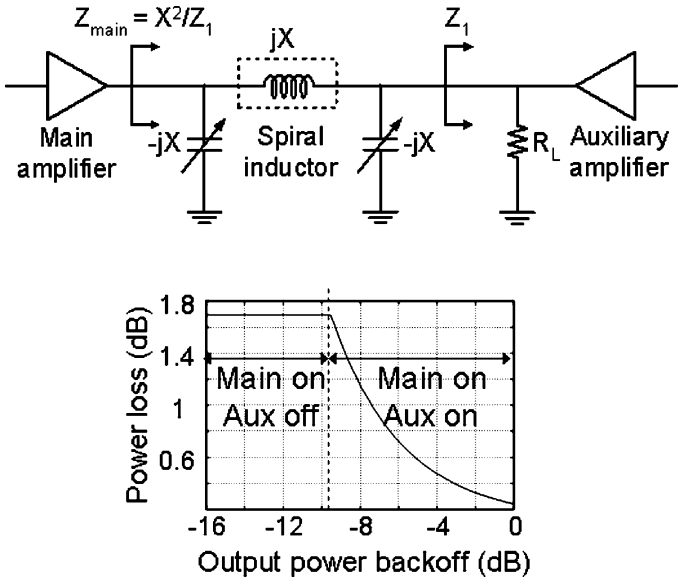

Fig. 5. Passive impedance inverter.

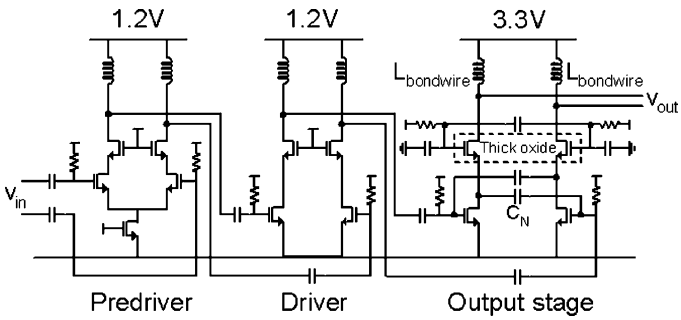

Fig. 6. Main/auxiliary amplifier circuit diagram.

impedance of the shunt elements to be tuned to match that of the series inductor. The series inductor is implemented as an on-chip spiral inductor. However, due to its low Q nature, loss of this network becomes an issue. With $k = 3$ and inductor Q of 7, the network loss was found from simulation to be 1.7 dB when only the main amplifier is on. Once the auxiliary amplifier is turned on, its current through the spiral inductor partially cancels that coming from the main amplifier causing the ratio of the inductor loss to the output power to decrease. At full output power, the network loss is merely 0.25 dB.

B. Main/Auxiliary Amplifier

In order to achieve sufficiently large power gain, both amplifiers were designed to have three stages with approximately 40 dB of power gain. The schematic diagram is shown in Fig. 6. They were designed to share the same schematic and layout in order to allow the phase of the two signal paths to be better matched. Having matched layout also simplifies the tuning of the Z_{inv} network. The predriver and driver use a 1.2-V supply voltage. Both stages are biased in class A mode to obtain good linearity. Due to the lower output swing requirement at the output of the predriver, a tail current source can be used in this stage to improve the amplifier's common mode rejection. For the output stage, thick-oxide cascode transistors and a 3.3-V supply voltage are used. The main amplifier output stage was designed to be a class AB amplifier to achieve good linearity whereas the auxiliary amplifier output stage is biased slightly below the threshold voltage for shallow class C operation. In order to obtain good linearity from the class AB amplifier, the input swing has to be kept small in an effort to keep the active device in saturation region as long as possible. For the auxiliary amplifier, a much larger input drive can be used without significantly degrading the overall linearity, thus allowing the maximum output current of the auxiliary amplifier to be almost twice that of the main amplifier, necessitating $k = 3$ in the Z_{inv} network. The W/L of the g_m and cascade transistors in the output stage are 11.75 mm/0.13 μm and 11.75 mm/0.35 μm, respectively.

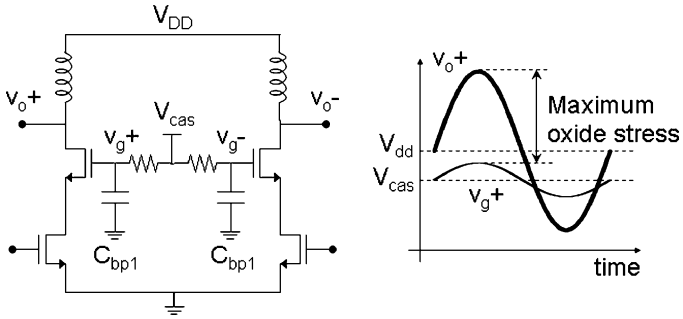

Fig. 7. Cascode transistor bypassing.

C. Capacitive Neutralization

The load network of the driver is formed by the input capacitance ($C_{\rm in}$) of the output stage, an inductor (usually an on-chip spiral inductor), and a load resistance which is dominated by the inductor parasitic resistance. One common problem in a linear driver design is the nonlinear input capacitance of the output stage. This problem arises when the cascode transistor of the output stage enters triode region while the g_m transistor is still in saturation. As a result, the Miller gain across $C_{\rm gd}$ of the g_m transistor expands, resulting in a higher input capacitance. For a differential design, cross-coupled capacitors can be used to neutralize this effect as shown in Fig. 6. Then the input capacitance of the output stage becomes

$$\begin{aligned} C_{\rm in} &= C_{\rm gs} + (1 - A_{\rm vM})C_{\rm gd} + (1 + A_{\rm vM})C_N \\ &= C_{\rm gs} + C_{\rm gd} + C_N + A_{\rm vM}(C_N - C_{\rm gd}) \end{aligned} \tag{5}$$

where $\rm A_{vM}$ is the Miller gain, which shows expansion behavior at high output swing. By choosing $C_N = C_{\rm gd}$, $C_{\rm in}$ can be independent of $\rm A_{vM}$. Although C_N and $C_{\rm gd}$ may not be well-matched, partial cancellation can still significantly improve the overall linearity. Having cross-coupled neutralization capacitors essentially forms a feedback loop that is potentially unstable. Stability analysis shows that if C_N is chosen to be approximately $C_{\rm gd}$, the loop is unlikely to become unstable.

D. Cascode Bypass

Conventionally, the gate of the cascode transistor is heavily bypassed by a large capacitor to make an AC ground. This prototype uses a different strategy in which the cascode gate is not completely bypassed as shown in Fig. 7 for two reasons. First, due to large $C_{\rm gs}$ and $C_{\rm gd}$ of the cascode transistor, an excessively large capacitor would be needed in order to completely bypass the AC signal at that node. Second, by not completely bypassing the cascode gate, $C_{\rm gd}$ of the cascode transistor and the bypass capacitor ($C_{\rm bypass}$) form a capacitive divider, allowing the voltage swing at the cascode gate to be in phase with the output node. Thus, the maximum voltage swing across the oxide region of the cascode transistor can be reduced. This helps improve the reliability of the amplifier. However, this technique effectively increases the impedance seen by the g_m transistor. Its effect on the overall amplifier linearity can be minimized by carefully choosing the gate bias voltage of the cascode transistor such that the g_m transistor does not enter triode region prematurely.

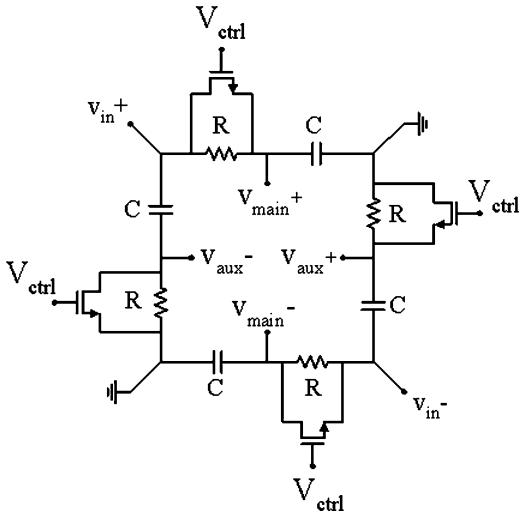

Fig. 8. Polyphase circuit diagram.

E. 90° Phase Shifter

The Doherty amplifier consists of the main signal path and the auxiliary signal path. The main path has an impedance inverter network, which gives 90° phase shift, at the output. To equalize the delay of the two signal paths, a polyphase circuit is used as the phase shifter network at the inputs of the two amplifiers. Inserting a phase shift network at the input does not incur extra insertion loss after the amplifier which would directly lower the overall efficiency. A polyphase circuit is an *RC-CR* ladder which gives 90° phase difference at its two outputs regardless of frequency of operation, as long as all *R*s are matched and all *C*s are matched. The output phase difference is also insensitive to capacitive load. A schematic diagram of the polyphase circuit is shown in Fig. 8.

Although a polyphase circuit gives a robust 90° phase shift, the output amplitudes depend on the magnitude of the impedance of *R*s and *C*s, which are not intrinsically matched when subject to process variations. NMOS triode resistors are used in parallel with the fixed resistors to allow trimming for this effect. Furthermore, they can also be used to adjust the relative amplitude of the two outputs at different output power levels to achieve optimal overall efficiency. For this prototype, the values of *R* and *C* are 250 Ω and 1 pF, respectively. The W/L of the nMOS transistors is 4 μm/0.2 μm, giving over 6 dB of relative gain adjustment. In order to avoid distortion in nMOS resistors, the input amplitude of the polyphase circuit is designed to be below 150 mV.

F. Impedance Inverter Tuning

For the Doherty amplifier to function properly, the $Z_{\rm inv}$ network must be tuned such that the magnitudes of impedance of all three reactive components are matched. Shunt switched capacitor arrays are used as tuning elements as shown in Fig. 5. Tuning can be done by turning on only the auxiliary amplifier and adjusting the capacitor array at the output of the main amplifier until it resonates with the series inductor between the two amplifiers. At resonance, the auxiliary amplifier sees small impedance looking into the series *LC* tank, hence giving the

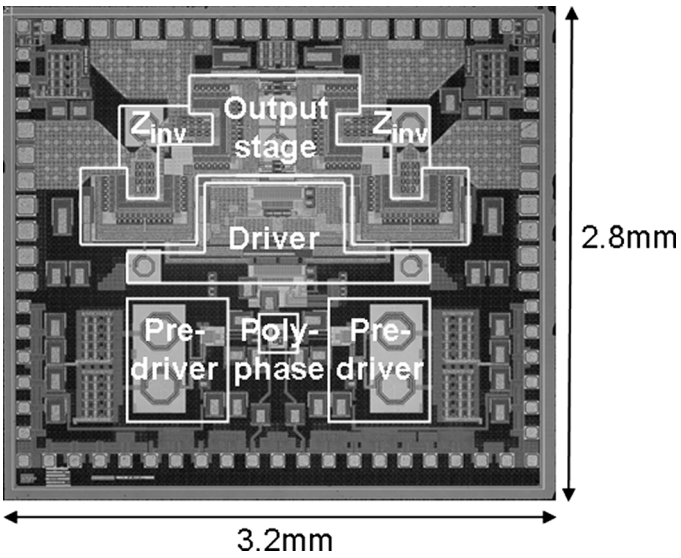

Fig. 9. Chip micrograph.

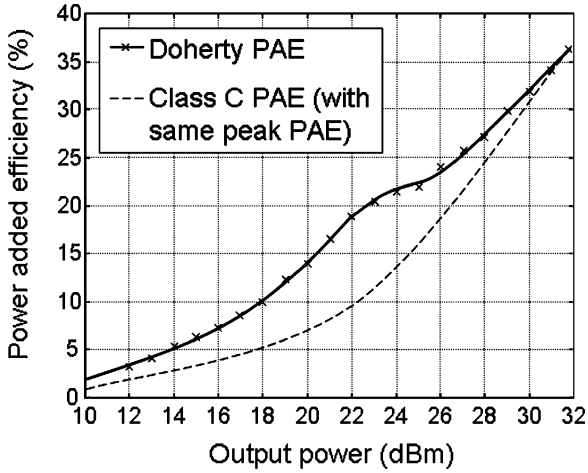

Fig. 10. Measured PAE for different output power levels.

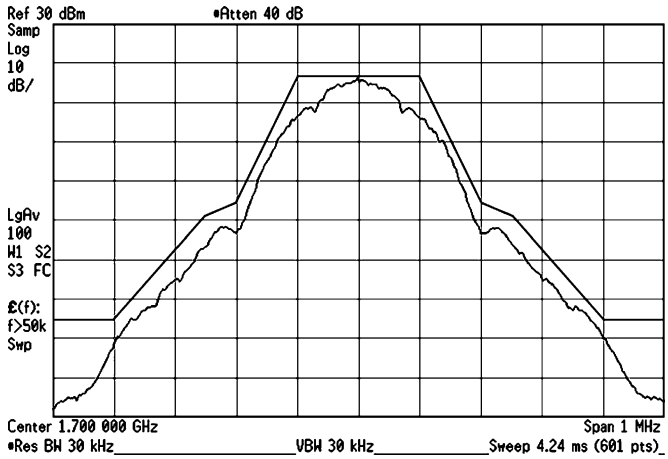

Fig. 11. Measured GMSK output spectrum.

minimum signal at the output (with high Q assumption). The same capacitor code can then be applied to the capacitor array at the output of the auxiliary amplifier since both amplifiers are identical by design. Variations of bondwire inductance can also be tuned out with this scheme. Since the output nodes of both amplifiers have relatively low Q, precise tuning is not required. During measurement, this tuning process was carried out manually. However, it can be implemented as an automatic algorithm without any loss of accuracy.

V. Experimental Prototype

The prototype was fabricated in a 0.13-μm CMOS process with MIM capacitor and triple-well options. The die size is 2.8×3.2 mm^2 including all on-chip bypass capacitors and pads. A chip micrograph is presented in Fig. 9. The prototype was assembled on a four-layer FR-4 test board using chip-on-board packaging. Gold bondwires are used to achieve high-Q inductance. PA output pads and 3.3-V power supply pads are double-bonded to minimize the bondwire inductance. Since the prototype is fully differential, baluns are used at the input and output to interface with the signal generator and spectrum analyzer.

VI. Measurement Results

A. Measured With GSM Signal

The prototype was measured with a GSM input signal at 1.7 GHz. For this measurement, the amplifier was hard-over-driven in order to achieve the desired peak output power. With only the main amplifier operating, the peak output power was measured to be +24 dBm with 22% power-added efficiency (PAE). With both amplifiers on, the peak power is +31.5 dBm with 36% PAE (39% drain efficiency). When including the output balun loss, the peak PAE is 33%. The PAE plot is shown in Fig. 10. Note that the first efficiency peak is much lower than the second peak, due to loss of the Z_{inv} network. From this plot, it can be seen that the PAE is kept above 18% over a 10 dB range of output power. When compared with the efficiency of a typical class C amplifier with the same peak efficiency, the prototype shows significant improvement at large back-off power over the stand-alone design. Fig. 11 shows the output spectrum at the peak output power setting. The output spectrum of the prototype fits under the GSM mask requirement across all output power levels. The peak phase error was measured at 1.2°.

B. Measured With EDGE Signal

The modulation scheme used in GSM/EDGE is $3\pi/8$ 8PSK. With the pulse shaping filter specified by the standard, the peak-to-average ratio of the signal is 3.5 dB. With the main amplifier operating alone, the maximum linear output power while still meeting the mask and error vector magnitude (EVM) requirements is +13 dBm. With both amplifiers operating together, the maximum linear power is +25 dBm and the rms EVM is 3.8%, while achieving 13% peak PAE. Noise in the receive band at 20 MHz away is −109.8 dBm/Hz and the third harmonic is −51 dBc. Fig. 12 shows the output spectrum plot at +25 dBm power level. The operating frequency for this measurement is 1.75 GHz.

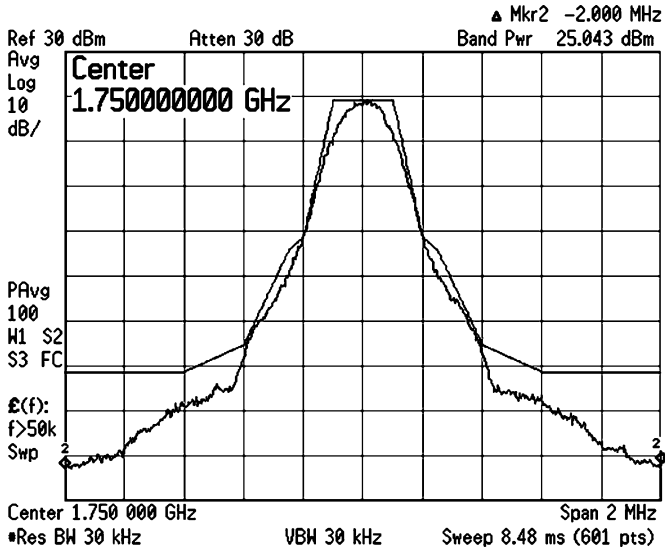

Fig. 12. Measured EDGE output spectrum.

VII. Conclusion

A highly integrated CMOS Doherty RF PA is demonstrated in a deep-submicron CMOS technology. The passive impedance inverter which is a critical block in Doherty configuration is implemented as a lumped-element network and is fully integrated on-chip. The prototype achieves over +31.5 dBm of output power and meets GSM/EDGE linearity requirements at +25 dBm output power. With the use of the Doherty technique, the amplifier PAE is kept above 18% over a 10 dB range of output power, making it suitable for wireless applications where the typical transmitter output power is usually much less than the peak power.

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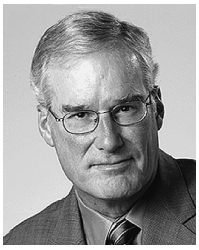

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