A Broadband Switched-Transformer Digital Power Amplifier for Deep Back-Off Efficiency Enhancement

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***Abstract*— This article presents a switched-transformer-based polar Doherty digital power amplifier (DPA) for deep back-off efficiency enhancement. A single-transformer-footprint parallel-combining transformer (PCT) power combiner is introduced for 1.3–3.5-GHz wide frequency coverage, dynamic load modulation at 0-/6-/12-/18-dB power back-off (PBO) levels, and an ultra-compact die size. Implemented in 40-nm CMOS, the DPA is powered by a 1.1-V supply and only occupies 0.7 × 1.15 mm^2 chip area. It achieves 21.4-dBm peak power with the power added efficiencies (PAEs) of 31.3%, 27.7%, 16.6%, and 7.7% for 0-/6-/12-/18-dB PBOs at 1.5 GHz. With 20-MHz 64QAM long term evolution (LTE) signal, the DPA achieves P_{avg} of 15.2 dBm and the average PAE of 25.3% with −32.5-dB error vector magnitude (EVM) at 1.5 GHz. Moreover, for 20-MHz 64 QAM WLAN signal, P_{avg} of 14.7 dBm with the average PAE of 20.1% is obtained with − 25-dB EVM at 2.4 GHz.**

***Index Terms*— CMOS, deep back-off, digital power amplifier (DPA), Doherty, efficiency enhancement, switched transformer.**

I. Introduction

In face of scarce spectrum resources and increasing demand for higher data throughput, sophisticated orthogonal frequency-division multiplexing (OFDM) modulation schemes are widely adopted in modern wireless communication systems, which often result in a large peak-to-average power ratio (PAPR) [1], [2]. Besides, wireless standards, such as long term evolution (LTE), WLAN, and NB-IoT, require a wide transmission power range to accommodate various communication environments and devices often function at low average output power. Therefore, it is critical for the PA to be efficient not only at peak power but also at deep power back-off (PBO) levels (e.g., 12/18 dB or higher) so as to achieve good overall efficiency and extend battery lifetime [3].

Many techniques have been studied to improve the PBO efficiency of the PA, such as envelop tracking [4], [5], outphasing [6]–[8], Doherty [9]–[13], and Class-G [14], [15]. For envelope tracking, the design of a supply modulator often meets stringent tradeoffs among speed, efficiency, and dynamic range. In an outphasing architecture, it requires the judicious design of the outphasing power combiner. Doherty or Class-G techniques usually provide an efficiency peaking at 6-dB PBO. However, most Doherty PAs suffer from large area overhead since they need transmission lines or at least two transformers for dynamic load modulation, whereas Class-G PAs require two power supplies with wide dynamic output current range and low noise that increase the design complexity of PMU.

To enhance the efficiency beyond 6-dB PBO, extensions and combinations of aforementioned techniques are researched in the literature, such as dynamic power control [16], multi-level outphasing [17], Class-G Doherty [18]–[20], and sub-harmonic switching [21]. The dynamic power control or multi-level outphasing PA requires multiple phase modulators and amplitude-level transitions, which cause inherent discontinuities and degrade the linearity. Multi-way Doherty PAs provide extra efficiency peakings at 6–12-dB PBO at the cost of large-area overhead due to the complex passive network [22], [23]. Class-G Doherty PAs take advantage of both supply modulation and load modulation to boost the efficiency at 6- and 12-dB PBOs, but it has the linearity degradation issue due to the power mode transition in the Class-G operation. Furthermore, multi-subharmonic switching technique can also be combined with Class-G to increase PBO efficiency enhancement range to 13 dB [21]. However, it demands three transformers to perform subharmonic cancellation and would introduce the nonlinearity problems during power mode and frequency switchings.

The digital power amplifier (DPA) plays a dominant role in digital transmitters [24]–[28]. Recently, intensive research works have been directed toward Class-D-based switched-capacitor PAs (SCPAs) [29]–[32]. In this article, a switched-transformer-based SCPA is proposed for wide-range PBO efficiency enhancement. This topology takes full advantage of load modulation technique and does not need multiple power supplies. In the matching network, an eight-way parallel-combining transformer (PCT) power combining scheme is introduced for broadband coverage, dynamic load modulation, and an ultra-compact die size. The DPA realizes multiple efficiency peakings at 0-/6-/12-/18-dB PBOs and wide frequency coverage with a single-transformer footprint and only one supply voltage.

Manuscript received September 12, 2019; revised February 11, 2020; accepted June 6, 2020. Date of publication July 16, 2020; date of current version October 23, 2020. This article was approved by Associate Editor Alyosha Molnar. This work was supported in part by the National Natural Science Foundation of China under Grant 61874153 and Grant 61974171 and in part by the Research Project Fund of State Key Laboratory of ASIC and System, Fudan University, under Grant 2018MS007. *(Corresponding author: Hongtao Xu.)*

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Digital Object Identifier 10.1109/JSSC.2020.3005798

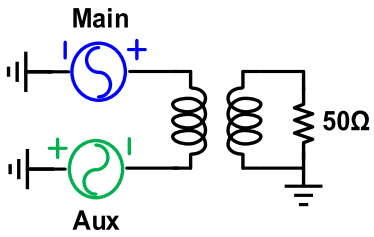

Fig. 1. Block diagram of the voltage-mode SCPA with Doherty load modulation [18], [33].

This article is organized as follows. In Section II, theoretical operations of the typical voltage-mode Doherty DPA and the proposed switched-transformer DPA for deep PBO efficiency enhancement are discussed. Section III describes the detailed circuit implementations. Section IV shows the measured results, with conclusions drawn in Section V.

II. Theory of Operation

A. Typical 6-dB PBO Efficiency Enhancement With Voltage-Mode Doherty Topology

The voltage-mode SCPA with 6-dB Doherty load modulation is shown in Fig. 1 [18], [33], where the main and aux PAs are two identical sub-PAs. At peak power, both sub-PAs are fully switched ON, and the load impedance seen by each sub-PA is the optimal impedance R_{opt}. As output power decreased during 0–6-dB PBO, the aux PA is gradually turned off. Then, the impedance seen by the main PA is

$$R_m = 2R_{\text{opt}}/(1+V_a/V_m) \tag{1}$$

where V_m and V_a represent the voltage amplitudes of main and aux PAs, respectively. At 6-dB PBO, the aux PA is fully OFF, and thus, the load impedance seen by the main PA increases to $2R_{\text{opt}}$, leading to another efficiency peaking via load modulation.

The differential topology of the Doherty SCPA is given in Fig. 2(a). Fig. 2(b)–(d) shows different configurations at 6-dB PBO between the active and passive circuits, where these three different configurations offer the same peak power and peak efficiency. However, there exists a significant difference among their effects of PBO efficiency enhancement. Fig. 2(b) and (c) performs the Doherty load modulation by controlling main/aux PAs asynchronously but combined in different ways, where Fig. 2(c) utilizes the whole transformer structure at 6-dB PBO while Fig. 2(b) merely utilizes half of the structure. Compared with Fig. 2(c), Fig. 2(b) would introduce more insertion loss at back-off powers due to the resistive loss of shorted primary coils and degrade PBO efficiency [33]. If main and aux PAs are using the same control codes and both operate with half amplitude at 6-dB PBO [see Fig. 2(d)], the load impedance seen by both PAs will stay the same at back-off powers without any load modulation, leading to no PBO efficiency enhancement. As shown in Fig. 2(e), with the non-ideal transformer combiner, Fig. 2(c) offers the best efficiency and an extra 6-dB efficiency peaking when compared with Fig. 2(b) and (d).

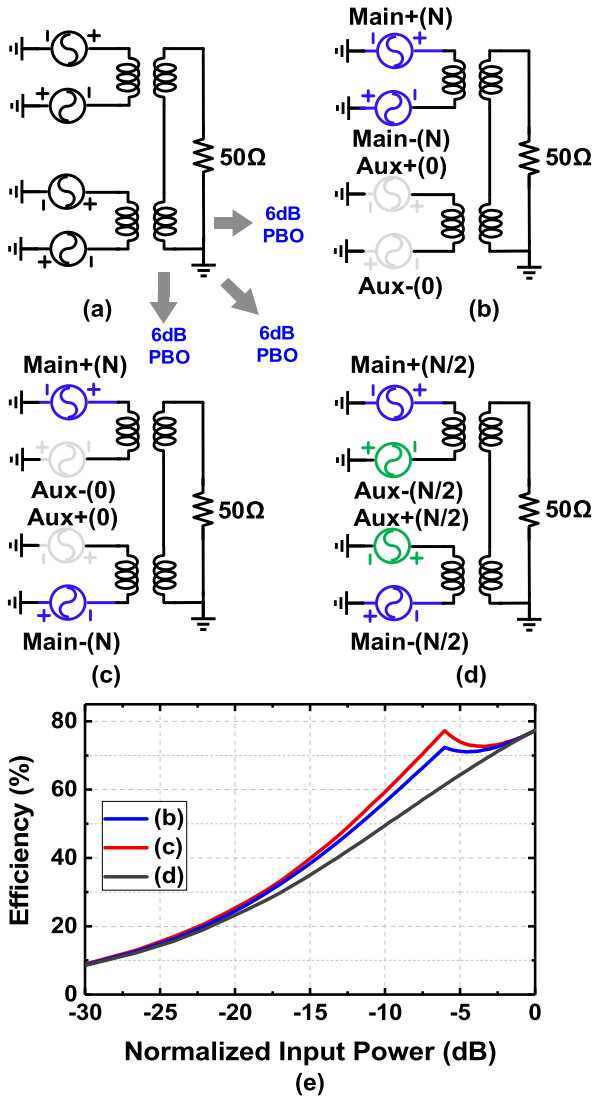

Fig. 2. (a) Differential topology of the voltage-mode Doherty SCPA at 0-dB PBO. Different configurations at 6-dB PBO: (b) main and aux PAs are controlled asynchronously and combined at the secondary coil, (c) main and aux PAs are controlled asynchronously but combined at the primary coil, (d) main and aux PAs are controlled synchronously, and (e) efficiency comparisons among (b)–(d) with the non-ideal power combiner ($Q_1 = Q_2 = 10$, $k = 0.8$, $Q_{\text{Load}} = 3$).

Therefore, the following insights can be drawn for the operation guidance of transformer-based Doherty SCPAs to enable deep PBO efficiency enhancement.

1) The sub-PAs should be controlled independently to perform dynamic load modulation, i.e., the main PA should be kept at full amplitude until the aux PA is totally turned off.
2) The differential sub-PA should bridge between the two adjacent primary coils to utilize the whole transformer-based network and avoid large insertion loss in the primary coils.

B. Ideal Model of the Proposed 0–18-dB PBO Efficiency Enhancement With Switched-Transformer Load Modulation

Fig. 3 shows the block diagram of the proposed switched-transformer DPA configurations at 0-/6/12-/18-dB PBOs.

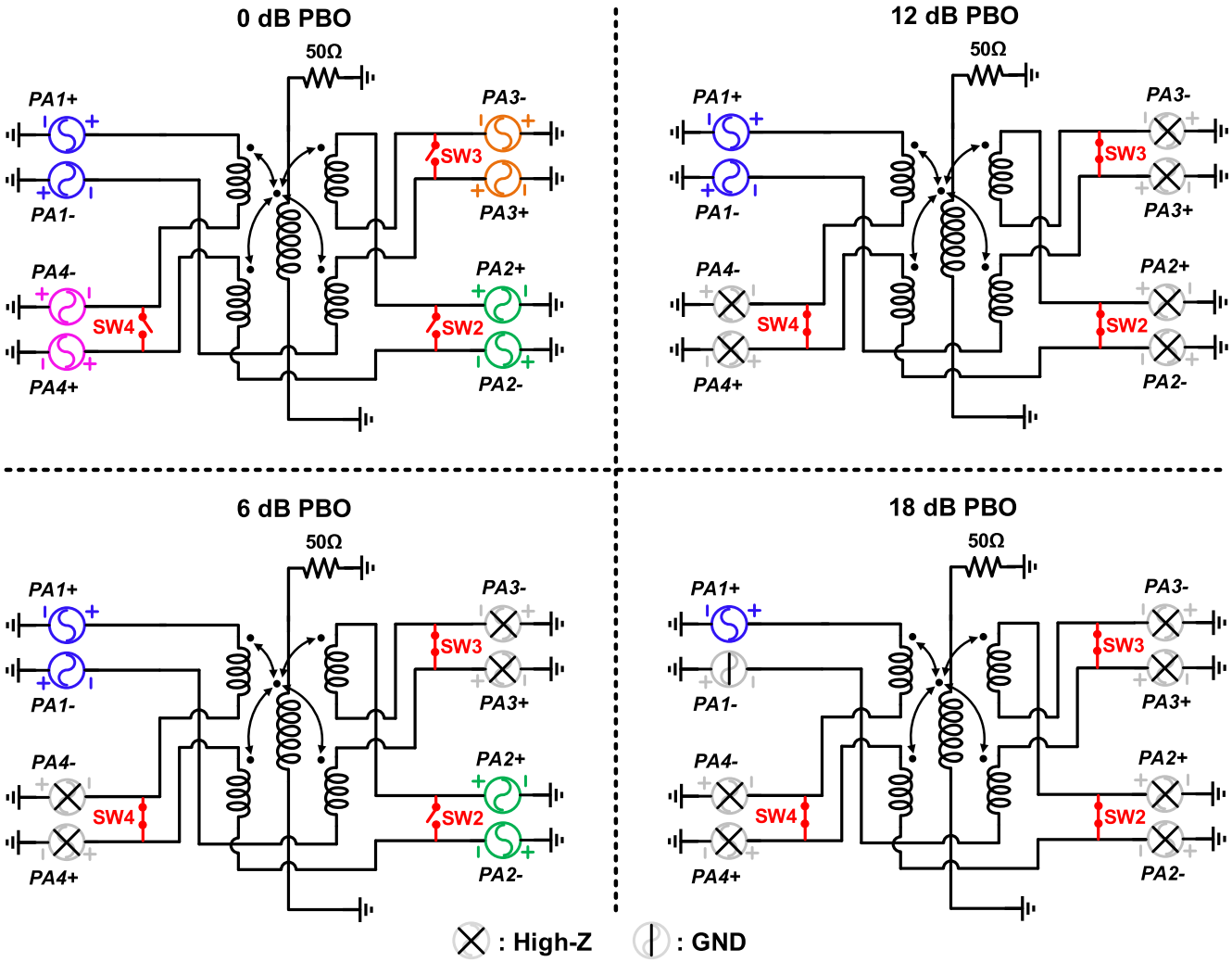

Fig. 3. Block diagram of proposed switched-transformer DPA configurations at 0-/6-/12-/18-dB PBOs with PCT power combiner.

In order to achieve the highest efficiency at all PBO levels, both active and passive circuits need to be designed deliberately according to the conclusions mentioned earlier. The proposed DPA consists of four sub-PAs (PA1–PA4) that are controlled independently and turned on in proper order. Each differential sub-PA pair is connected to the terminals of two adjacent primary coils to utilize the whole transformer power combiner at all PBO levels and perform the load modulation.

First, at 0-dB PBO, PA1–PA4 are totally turned on and the switches SW2–SW4 bridged between the transformers are all switched OFF. The outputs of the four sub-PAs are finally combined through the transformer power combiner. Then, at 6-dB PBO, PA3/4 are both switched to the high-impedance state, and the switches SW3 and SW4 are switched ON to connect the differential output terminals, which realizes the Doherty load modulation for PA1/2 and achieves good structure symmetry. At 12-dB PBO, PA2 is also switched to the high-impedance state; meanwhile, all the switches SW2–SW4 are switched ON to maintain the integrity of the entire transformer power combiner. Finally, when the output power drops by 18 dB, the single-ended PA1− will be turned off and connected to ground, so the load modulation is implemented and another efficiency peaking is achieved. To accomplish this, the structure of PA1 should be designed to be different from that of PA2/3/4, which will be discussed in detail in Section III-B.

Assuming that the total number of DPA cells is N, thus, there are $N/4$ cells in each differential sub-PA pair. Let n_{1+} and n_{1-} denote the number of switched-ON cells in PA1+ and PA1−, respectively, whereas n_2, n_3, and n_4 denote the number of switched-ON differential pairs in PA2/3/4. As the cells in PA3 and PA4 will be switched OFF by turn during 0–6-dB PBO, $n_{3,4}$ is used to represent the sum of n_3 and n_4. When the input code is n ($0 \leq n \leq N$), the turn-on sequence of the whole DPA can be given by the following expressions (2)–(5), which are shown in Fig. 4. As the input code increases from 0 to $N/8$, the cells in PA1+ start to turn on in sequence until they are all at ON state; then, during the phases of $N/8 \leq n \leq N/4$ and $N/4 \leq n \leq N/2$, the cells in PA1− and PA2 start to turn on in sequence, respectively. When it comes to the last phase ($N/2 \leq n \leq N$), PA3 and PA4 take turn to switch ON their cells. This turn-on sequence guarantees the load modulation during 0–18-dB PBO and circuitry

symmetry

$$n_{1+} = \begin{cases} 2n, & 0 \le n < \frac{N}{8} \\ \frac{N}{4}, & \frac{N}{8} \le n \le N \end{cases} \tag{2}$$

$$n_{1-} = \begin{cases} 0, & 0 \le n < \frac{N}{8} \\ 2\left(n - \frac{N}{8}\right), & \frac{N}{8} \le n < \frac{N}{4} \\ \frac{N}{4}, & \frac{N}{4} \le n \le N \end{cases} \tag{3}$$

$$n_{2} = \begin{cases} 0, & 0 \le n < \frac{N}{4} \\ n - \frac{N}{4}, & \frac{N}{4} \le n < \frac{N}{2} \\ \frac{N}{4}, & \frac{N}{2} \le n \le N \end{cases} \tag{4}$$

$$n_{3,4} = \begin{cases} 0, & 0 \le n < \frac{N}{2} \\ n - \frac{N}{2}, & \frac{N}{2} \le n < \frac{3N}{4}. \end{cases} \tag{5}$$

Then, the load impedance seen by each sub-PA is given by

$$\begin{cases} V_{1-} = 0,\ V_{1+} = \dfrac{n_{1+}}{N/4} \cdot V_{\mathrm{DD}} \\ Z_{1+} = 8R_{\mathrm{opt}} \\ Z_{1-} = Z_2 = Z_{3,4} = 0 \end{cases} \quad 0 \le n < \frac{N}{8} \tag{6}$$

$$\begin{cases} V_{1-} = \dfrac{n_{1-}}{N/4} \cdot V_{\mathrm{DD}},\ V_m = V_{\mathrm{DD}} \\ Z_m = Z_{1+} = \dfrac{V_m}{V_m + V_{1-}} \cdot 8R_{\mathrm{opt}} \\ Z_{1-} = 8R_{\mathrm{opt}} - Z_m,\ Z_2 = Z_{3,4} = 0 \end{cases} \quad \frac{N}{8} \le n < \frac{N}{4} \tag{7}$$

$$\begin{cases} V_2 = \dfrac{n_2}{N/4} \cdot 2V_{\mathrm{DD}},\ V_m = 2V_{\mathrm{DD}} \\ Z_m = Z_{1+} = Z_{1-} = \dfrac{V_m}{V_m + V_2} \cdot 4R_{\mathrm{opt}} \\ Z_2 = 4R_{\mathrm{opt}} - Z_m,\ Z_{3,4} = 0 \end{cases} \quad \frac{N}{4} \le n < \frac{N}{2} \tag{8}$$

$$\begin{cases} V_{3,4} = \dfrac{n_{3,4}}{N/2} \cdot 4V_{\mathrm{DD}},\ V_m = 4V_{\mathrm{DD}} \\ Z_m = Z_{1+} = Z_{1-} = Z_2 = \dfrac{V_m}{V_m + V_{3,4}} \cdot 2R_{\mathrm{opt}} \\ Z_{3,4} = 2R_{\mathrm{opt}} - Z_m \end{cases} \quad \frac{N}{2} \le n \le N \tag{9}$$

where V_{1+} and V_{1-} represent the output voltages of the differential PA1+/PA1−, respectively, and V_2 and $V_{3,4}$ represent the output voltages of PA2 and PA3/4, respectively. V_{DD} denotes the supply voltage, and V_m represents the output voltage of the equivalent main PA part. R_{opt} denotes the single-ended optimal load impedance seen by each sub-PA at peak power, and Z_m represents the load impedance seen by the equivalent main PA part. Z_{1+} and Z_{1-} are the load impedances seen by the differential PA1+/PA1−, and Z_2 and $Z_{3,4}$ are the load impedances seen by each differential terminal in PA2 and PA3/4, respectively. Fig. 5(a) shows the load impedance variations seen by each sub-PA versus output power, which demonstrates the Doherty load modulation at 6-/12-/18-dB PBO levels.

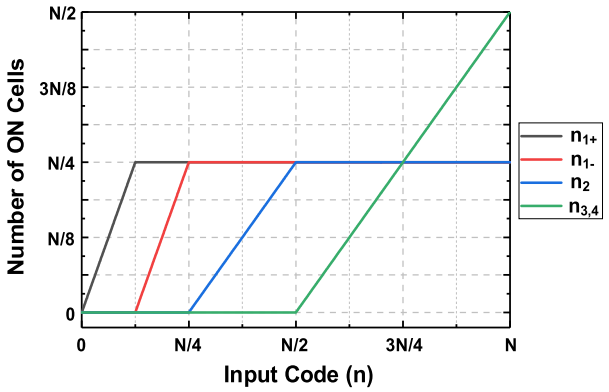

Fig. 4. Turn-on sequence of PA1+/PA1−/PA2/PA3/PA4.

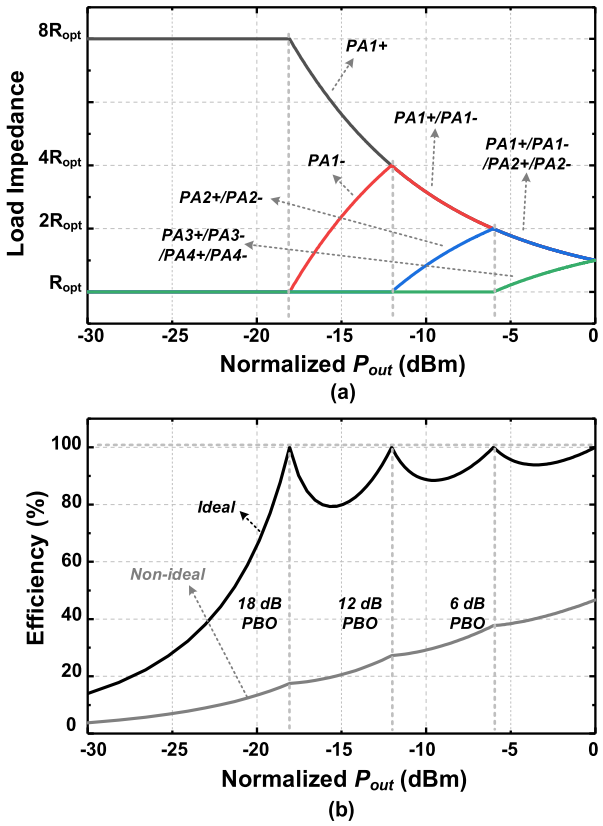

Fig. 5. (a) Load impedance seen by each sub-PA. (b) Ideal efficiency curve ($Q_{\mathrm{Load}} = 3$) and non-ideal efficiency curve ($\alpha = 0.7$, $R_{\mathrm{on}}/R_{\mathrm{opt}} = 1/7$, $f = 1.5$ GHz, and $f_{\mathrm{sw}} = 23$ GHz, $Q_{\mathrm{Load}} = 3$) versus normalized output power.

As for efficiency calculation, with the ideal passive network and ignoring the transistors' crowbar currents and parasitics, the total power consumption will be transformed into the output power P_{out} and the dynamic power consumption of switched capacitors P_{sc}. The DPA output power is given by

$$P_{\mathrm{out}} = 8 \cdot \frac{\left(\frac{2}{\pi} \cdot V_{\mathrm{DD}}\right)^2}{2 \cdot \left(R_{\mathrm{opt}}\right)} \cdot \left(\frac{n}{N}\right)^2 = \frac{16}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{\mathrm{DD}}^2}{R_{\mathrm{opt}}}. \tag{10}$$

Assuming that C represents the DPA total switched capacitance, the dynamic power P_{sc} and the ideal efficiency η of the proposed switched-transformer DPA can be expressed

as [30], [33]

$$P_{\rm sc}=\begin{cases}\dfrac{n\cdot(N-8n)}{N^2}\cdot \mathrm{CV}_{\rm DD}^2 f_{\rm LO}, & 0\le n<\dfrac{N}{8}\\ \dfrac{(8n-N)\cdot(N-4n)}{4N^2}\cdot \mathrm{CV}_{\rm DD}^2 f_{\rm LO}, & \dfrac{N}{8}\le n<\dfrac{N}{4}\\ \dfrac{(4n-N)\cdot(N-2n)}{2N^2}\cdot \mathrm{CV}_{\rm DD}^2 f_{\rm LO}, & \dfrac{N}{4}\le n<\dfrac{N}{2}\\ \dfrac{(2n-N)\cdot(N-n)}{N^2}\cdot \mathrm{CV}_{\rm DD}^2 f_{\rm LO}, & \dfrac{N}{2}\le n<N\end{cases} \tag{11}$$

$$\eta=\frac{P_{\rm out}}{P_{\rm out}+P_{\rm sc}}=\begin{cases}\dfrac{4n}{4n+\frac{\pi\cdot(N-8n)}{Q_{\rm Load}}}, & 0\le n<\dfrac{N}{8}\\ \dfrac{16n^2}{16n^2+\frac{\pi\cdot(8n-N)\cdot(N-4n)}{Q_{\rm Load}}}, & \dfrac{N}{8}\le n<\dfrac{N}{4}\\ \dfrac{8n^2}{8n^2+\frac{\pi\cdot(4n-N)\cdot(N-2n)}{Q_{\rm Load}}}, & \dfrac{N}{4}\le n<\dfrac{N}{2}\\ \dfrac{4n^2}{4n^2+\frac{\pi\cdot(2n-N)\cdot(N-n)}{Q_{\rm Load}}}, & \dfrac{N}{2}\le n<N\end{cases} \tag{12}$$

where $Q_{\rm Load}$ is the loaded quality factor that is given by

$$Q_{\rm Load}=\frac{1}{2\pi f_{\rm LO}\cdot(\frac{C}{8})\cdot R_{\rm opt}}. \tag{13}$$

C. Model With Nonideal Components

Various non-ideal factors need to be considered when implementing the DPA circuit, including conduction loss $P_{\rm cond}$, switch loss $P_{\rm sw}$ and passive loss. The power added efficiency (PAE) calculation considering these losses has been demonstrated in [20]. Similarly, assuming that $R_{\rm on}$represents the conduction resistance of a single branch in a sub-PA, the DPA output power without passive loss and the conduction power loss can be expressed as

$$P_{\rm out}=\frac{16}{\pi^2}\left(\frac{n}{N}\right)^2\frac{V_{\rm DD}^2}{R_{\rm opt}}\left(\frac{R_{\rm opt}}{R_{\rm opt}+R_{\rm on}}\right)^2 \tag{14}$$

$$P_{\rm cond}=P_{\rm out}\cdot\frac{R_{\rm on}}{R_{\rm opt}}. \tag{15}$$

As for the switch loss, it consists of the dynamic power of parasitic capacitance and power consumption of the crowbar current of driver circuits. The equivalent parasitic capacitance of a single branch in a sub-PA at drain and gate are denoted as C_{pd} and C_{pg}, respectively. Since their voltage amplitudes are different, their power consumption is provided separately

$$P_{cpd}=f\cdot\left(\mathrm{VDD}\frac{R_{\rm opt}}{R_{\rm opt}+R_{\rm on}}\right)^2\cdot C_{pd}\cdot\frac{8n}{N} \tag{16}$$

$$P_{cpg}=f\cdot\mathrm{VDD}^2\cdot C_{pg}\cdot\frac{8n}{N}. \tag{17}$$

The values of C_{pd} and C_{pg} are both set based on simulation results, whereas the values of C_{pg} also includes the effect of crowbar current loss of driver circuits. Therefore, the switch loss can be represented as

$$P_{\rm sw}=P_{cpd}+P_{cpg}. \tag{18}$$

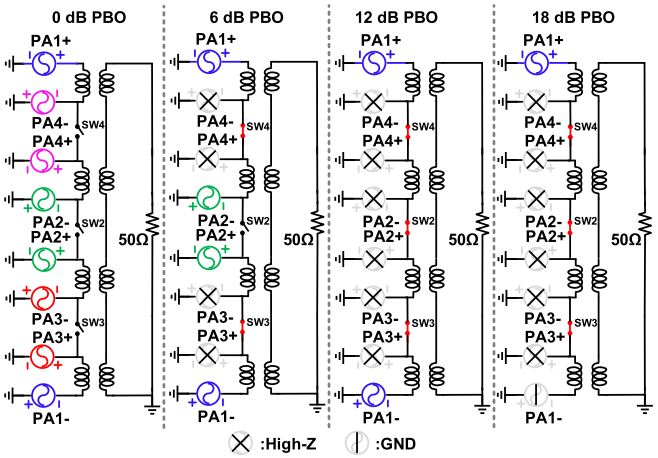

Fig. 6. Block diagram of the proposed switched-transformer DPA configurations at 0-/6-/12-/18-dB PBOs with SCT power combiner.

Assuming that the passive loss attenuates the output power by the factor of α, the non-ideal efficiency considering the abovementioned non-ideal factors can be expressed as

$$\eta=\frac{\alpha P_{\rm out}}{P_{\rm out}+P_{\rm sc}+P_{\rm cond}+P_{\rm sw}}=\frac{\alpha}{1+\frac{P_{\rm sc}}{P_{\rm out}}+\frac{P_{\rm cond}}{P_{\rm out}}+\frac{P_{\rm sw}}{P_{\rm out}}} \tag{19}$$

in which $(P_{\rm sc}/P_{\rm out})$ could be given by (11) and (14) and $(P_{\rm cond}/P_{\rm out})$ could be given by (15). According to (11), (16), and (17), $(P_{\rm sw}/P_{\rm out})$ could be expressed as

$$\frac{P_{\rm sw}}{P_{\rm out}}=\frac{\pi}{4}\frac{N}{n}\frac{R_{\rm opt}}{R_{\rm on}}f\left\{2\pi R_{\rm on}\left[C_{pd}+C_{pg}\left(1+\frac{R_{\rm on}}{R_{\rm opt}}\right)^2\right]\right\} \tag{20}$$

$$=\frac{\pi}{4}\frac{N}{n}\frac{R_{\rm opt}}{R_{\rm on}}\frac{f}{f_{\rm sw}} \tag{21}$$

where $f_{\rm sw}$ represents the totem pole driver figure of merit [20], which could be improved by CMOS process scaling, delicate driver design, and good layout practice.

Fig. 5(b) shows the DPA efficiency curves under ideal and non-ideal conditions, where four efficiency peakings are achieved at 0-/6-/12-/18-dB PBOs, and thus significantly improves the average efficiency. Here, these two efficiency curves from theoretical calculation have also been verified by simulation.

Although the proposed DPA architecture shown in Fig. 3 is based on the PCT power combiner, it can also be implemented using serial-combining transformer (SCT) power combiner, as shown in Fig. 6. This SCT-based switched-transformer DPA shares the same active circuits with the PCT-based architecture and achieves the same load modulation within 0–18-dB PBOs. The main difference lies in the implementation of power combiner, and the PCT-based architecture would cost less die area with the proposed single-transformer-footprint topology, which will be discussed in Section III-C.

III. Circuit Implementation

A. Switched-Transformer Digital Doherty PA and Floorplan

Fig. 7 shows the block diagram of the proposed switched-transformer Doherty DPA [34]. The polar SCPA architecture is employed due to its high efficiency and good linearity.

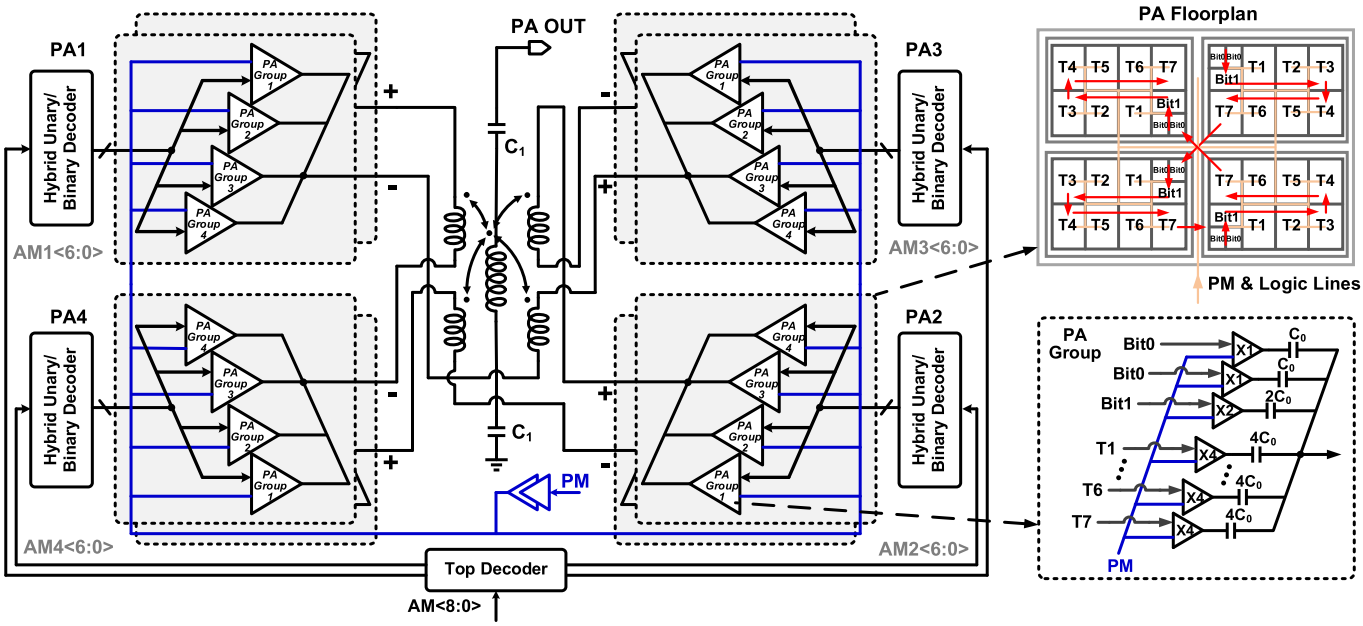

Fig. 7. Block diagram and floorplan of the proposed switched-transformer digital Doherty PA.

In the design, the total resolution of 9-bit AM⟨8:0⟩ is employed and the two MSBs' control four 7-bit sub-PAs. In each sub-PA, the hybrid unary/binary array is used to obtain a better resolution and reduce layout mismatch. Each sub-PA is divided into four groups controlled by AM⟨6:5⟩, and each group consists of seven thermometer-coded cells and 2-bit LSB binary-coded cells.

During 0–12-dB PBO, the unit cells of PA3/PA4 and PA2 will be gradually transformed from ON-state to high-impedance state in sequence and the transformer power combiner is reconstructed through switches. Within 12–18-dB PBO, the differential branches of PA1 are controlled independently and PA1− is gradually switched OFF. At 18-dB PBO, PA1+ is fully at ON-state, whereas PA1− is completely at OFF-state with outputs grounded, thus performing Doherty load modulation and enhancing the deep PBO efficiency.

In the floorplan, each sub-PA is arranged in order of four groups (Group4-1), and each group comprises seven thermometer-coded cells (T7-1) and three binary-coded cells (Bit1-0). As shown in Fig. 7, the "snake" traverse movements are performed end-to-end among unit cells in each sub-PA, which shows good center symmetry to mitigate layout PVT variations and improve differential non-linearities (DNLs) [35]. Moreover, the distribution of PM and logic lines to each unit cell is routed as H-trees to minimize delay mismatches. The LO gating technique is also employed to scale down LO distribution power at low output power.

B. Operation Modes of All the Sub-PAs

As shown in Fig. 8, the inverter-based Class-D topology is adopted in the differential unit PA cells. PA2/PA3/PA4 are three identical sub-Pas, whereas PA1 is slightly different from the others since it has the single-ended operation mode. The tri-state control logic is employed in PA2/PA3/PA4 to switch the operations between the ON-state and high-impedance states. At ON-state, the A/B terminals are square waves at LO frequency and D/E terminals are in anti-phase. Besides, the C terminal is decoded to be logic low, so the transformer switches are turned off at this state. When PA2/PA3/PA4 are turned off, the A/D signals are at logic high and B/E signals are at logic low to keep the inverters at high-impedance state. The C terminal is changed to logic high to turn on the switches between the differential outputs. Here, the switches are formed by three NMOS transistors, where the two additional NMOS transistors are small size and adopted to pull the differential outputs to the dc ground so that the NMOS switch can be kept at the deep linear region. Otherwise, the switch size should be quite large to achieve the same ON-resistance and introduce large parasitics. In the design, the W/L sizes of the PMOS and NMOS transistors in the unit PA cell are 9.2 μm/40 nm and 3 μm/40 nm, respectively. The ON-resistance of the whole sub-PA is 1 Ω. Besides, the sizes of the shunt NMOS switch and the small pull-down NMOS switch are 1.5 μm/40 nm and 0.12 μm/40 nm, respectively. In order to optimize the power consumption of the driver circuit, the rising/falling time is designed to be 5% of a clock period and the fan-out is set as 4.

As shown in Fig. 8, the differential pairs of PA1 are controlled independently through the DBO signal and both have two operation modes of ON-state and OFF-state. The DBO signal as well as the G_i, G_{i+1}, and T_j signals is generated by the decoder and then fed into the control logic circuit inside the unit PA cell. It is worth mentioning that the LSB of the entire DPA is the step resolution of a differential unit PA cell controlled by bit0. With output power decreased beyond 12-dB PBO, the number of unit cells that need to be switched OFF in PA1− and PA1+ should be twice the original resolution, which is implemented by a shift operation in the decoder.

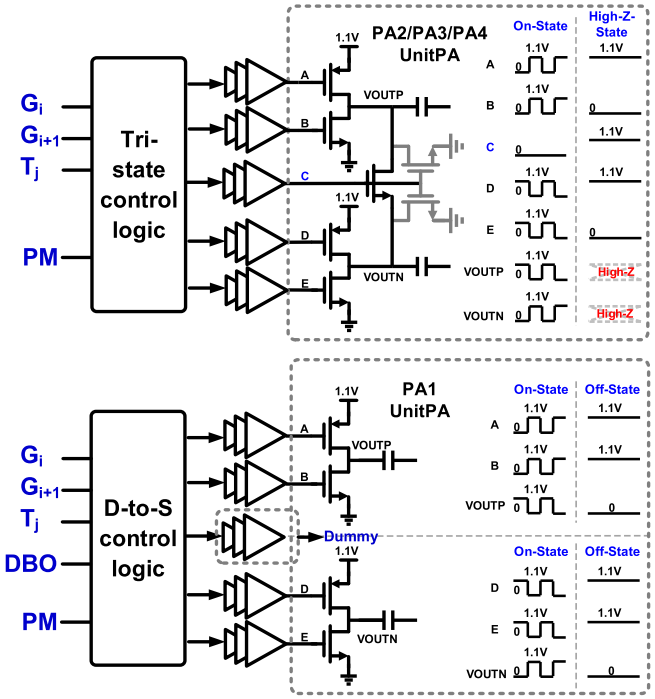

Fig. 8. Schematics and operation modes of PA2/3/4 and PA1.

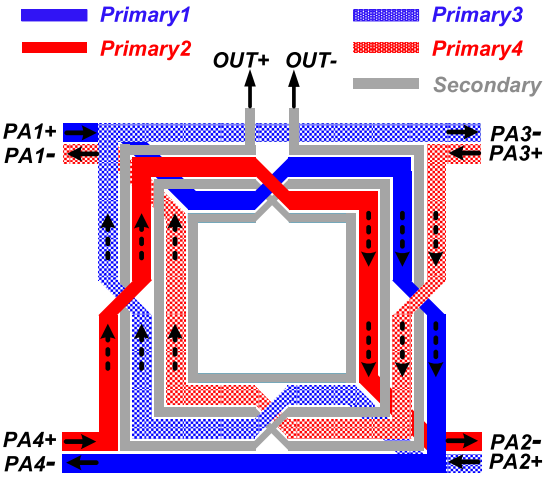

Fig. 9. Implementation of the proposed eight-way single-transformer-footprint PCT power combiner.

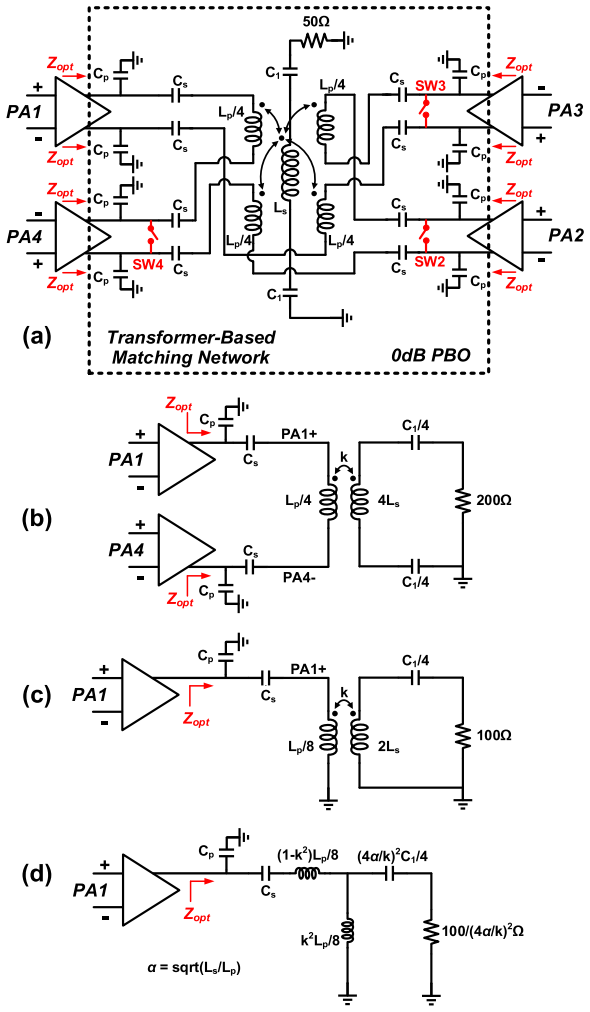

Fig. 10. Differential-to-single-end conversion of the PCT power combiner at peak power. (a) Lumped model equivalent circuit. (b) Single-primary equivalent circuit. (c) Single-sub-PA half circuit. (d) Simplified single-sub-PA half circuit.

C. Passive Matching Network Using Proposed Single-Transformer-Footprint PCT Power Combiner

As shown in Fig. 9, an eight-way single-transformer-footprint PCT power combiner is introduced in this work, which only occupies $500 \times 500\ \mu\text{m}^2$ die area. It has six turns, three of which are the primary coils and the other three turns are the secondary coils. The primary and secondary coils are both routed with the top metal MTT layer whose thickness is 3.4 μm. The metal widths of the primary and secondary coils are 24 and 14 μm, respectively. This power combiner is elaborately designed to maintain a high quality factor and coupling coefficient to improve power transfer efficiency. The four sub-PAs are located at the four corners to maintain good differential matching and diagonal symmetry. The output currents from the four sub-PAs flow in parallel directions in the primary coils, which obtains magnetic enhancement and increases the effective primary inductance, thus contributing to further size reduction and lower loss

As shown in Fig. 10, the proposed passive matching network can be equivalent to the single-sub-PA half circuit. First, the lumped model equivalent circuit at peak power is shown in Fig. 10(a). Assuming that the total primary inductance is L_P, the secondary inductance is L_S, the device parasitic capacitance is C_p, and the switched capacitance is C_s; when it comes to the single-primary equivalent circuit, as shown in Fig. 10(b), all the impedances of components at the secondary coil will be increased by four times due to the effect of parallel power combining. Then, it is further simplified to a single-sub-PA half circuit, as shown in Fig. 10(c). Here, the equivalent turn ratio is $N_P = (16L_S/L_P)^{1/2}/k = 4\alpha/k$, where $\alpha = (L_S/L_P)^{1/2}$ and k represents the coupling coefficient. Finally, the non-ideal transformer is simplified using the ideal $1{:}N_p$ transformer, and the impedances at the secondary coil are transformed to the primary side with the impedance scaling factor, as shown in Fig. 10(d). Thus, the single-ended load

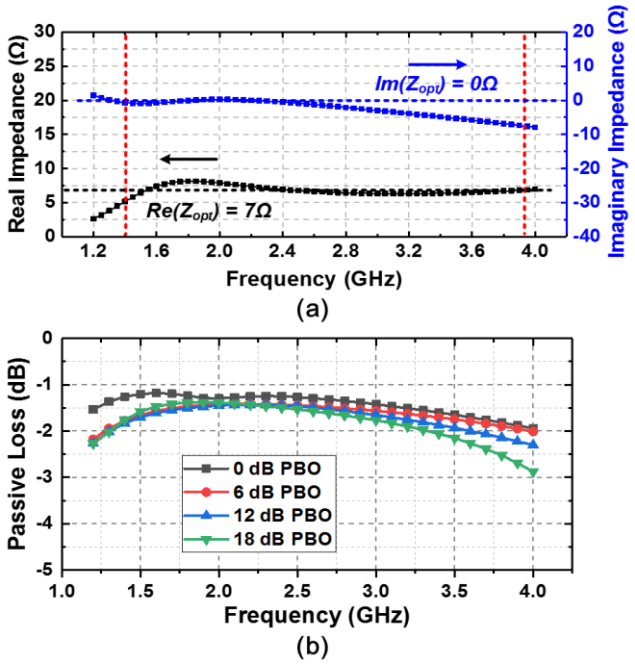

Fig. 11. (a) Simulated sub-PA single-ended optimal complex load impedance over the frequency. (b) Simulated passive loss of the matching network at flow in parallel directions in the primary coils, which obtains magnetic enhancement and increases the effective primary inductance, thus contributing to further size reduction and lower loss.

impedance Z_{opt} seen by the sub-PA can be expressed as [36]

$$Z_{\text{opt}} = \frac{1}{sC_p}\left\|\left[\frac{1}{sC_s} + \frac{s(1-k^2)L_p}{8} + \frac{sk^2L_p}{8}\left\|\frac{1+25sC_1}{4\left(\frac{\alpha}{k}\right)^2 sC_1}\right.\right]\right. . \tag{22}$$

Fig. 11(a) shows the simulated single-ended complex load impedance Z_{opt}, where the real part $\text{Re}(Z_{\text{opt}})$ maintains the desired value of about 7 Ω over a wide frequency span and the imaginary part $\text{Im}(Z_{\text{opt}})$ is around zero to achieve high efficiency. The simulated passive loss of the matching network at 0-/6-/12-/18-dB PBOs is shown in Fig. 11(b), which shows less than 1.5-dB passive loss at peak output power, and the loss variations are maintained within 0.5 dB over 1.3–3.5 GHz. Fig. 12 shows the simulated impedance transformation trajectories on the Smith chart from 0-to 18-dB PBO, which demonstrates the load modulation effects seen by PA1+, PA1−, PA2+/−, PA3+/−, and PA4+/−, respectively.

IV. Measurement Results

The proposed switched-transformer digital Doherty PA is implemented in a 40-nm CMOS process. As shown in Fig. 13, the chip occupies a total area of 0.7 × 1.15 mm^2, including all decoupling capacitors and electro-static discharge (ESD) I/O pads. The DPA is surface mounted on an evaluation PCB board with a single-ended LO input and an RF output. The external losses, including a 20-dB attenuator and the PCB path loss at different frequencies, are calibrated in the measurements. The DPA operates with only one 1.1-V power supply. In the PAE calculation, the power consumption of IO buffers, LO distribution drivers, logic blocks, and sub-PAs

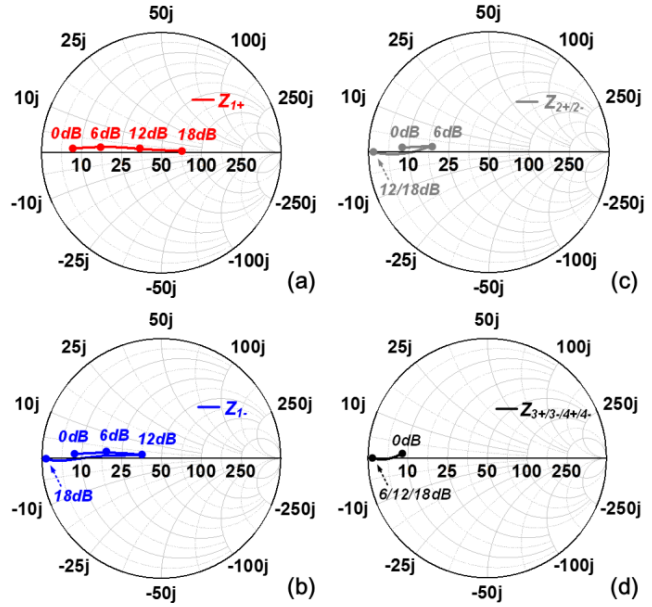

Fig. 12. Simulated impedance transformation trajectories on the Smith chart from 0- to 18-dB PBO. (a) Z_{1+}. (b) Z_{1-}. (c) $Z_{2+/2-}$. (d) $Z_{3+/3-/4+/4-}$.

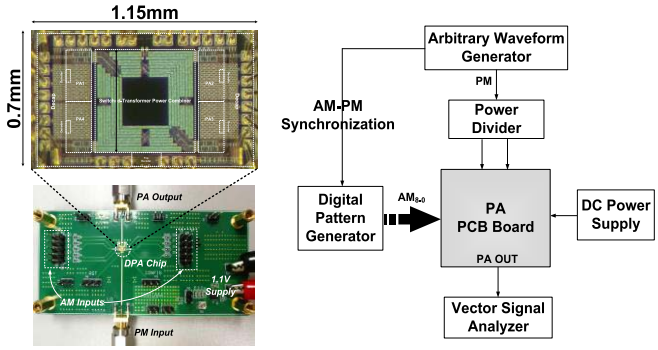

Fig. 13. Chip microphotograph, evaluation PCB board, and measurement setup.

is all included, which is equivalent to the system efficiency. In the measurement, the AM and PM signals are exported from a digital pattern generator and an arbitrary waveform generator (AWG), respectively. The AM–PM synchronization is performed by using a 10-MHz reference combined with a trigger signal from the AWG, which enables the trigger signal to be delayed with specific time adjustment.

Fig. 14 shows the measured continuous-wave (CW) results, in which the DPA achieves 21.4-dBm peak output power with 31.3% PAE at 1.5 GHz and 20.4-dBm peak output power with 24.5% PAE at 3.5 GHz. The 1-dB RF bandwidth is over 90% spanning from 1.3 to 3.5 GHz while maintaining good PAE performance. Compared with the simulated output power, the measured output power is decreased by 1.4 and 1.8 dB at 1.5 and 3.5 GHz, respectively. Due to the switched-transformer power combining and Doherty load modulation techniques, the expected deep back-off efficiency enhancement is realized. With the carrier frequency of 1.5 GHz, the DPA achieves the PAE of 27.7%, 16.6%, and 7.7% for 6-, 12-, and 18-dB PBOs, which shows the

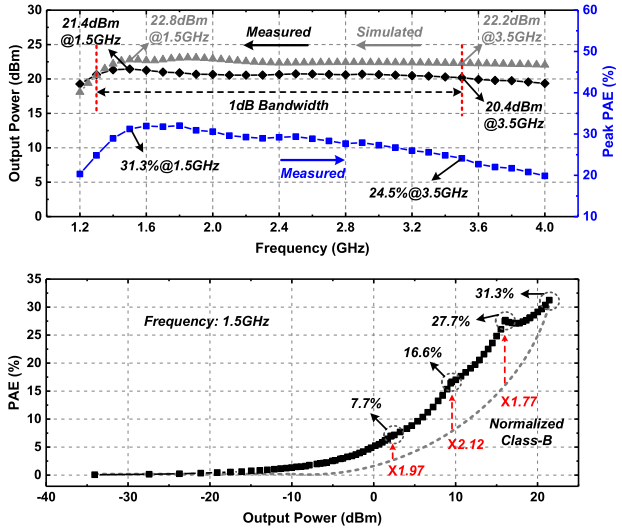

Fig. 14. Measured DPA CW results of output power and PAE performance.

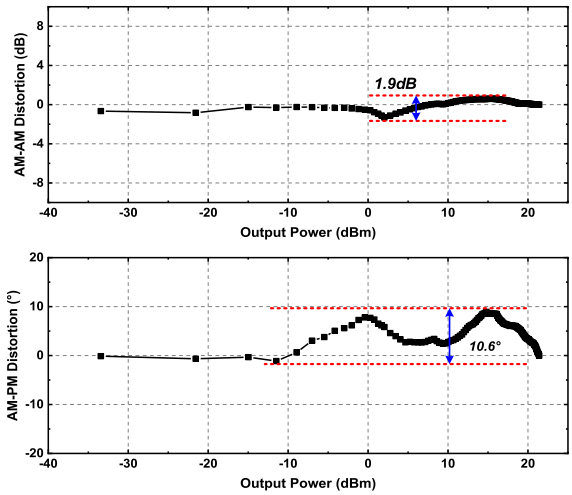

Fig. 15. Measured DPA AM–AM and AM–PM nonlinearities at 1.5 GHz.

PAE improvement of 1.77×, 2.12×, and 1.97×, respectively, when compared with the traditional Class-B PA.

Fig. 15 shows the AM–AM and AM–PM nonlinearities. The DPA achieves 1.9-dB AM–AM distortion and 10.6° AM–PM distortion, which are mainly due to the performance variations among the sub-PAs since they are located at the four corners over a wide area. It can be observed that the AM–AM distortion is less than 0.8 dB within 0–12 dB PBO range, where a high probability of signal power distribution is located. This indicates that the DPA guarantees good linearity when transmitting signals with large PAPR and is applicable for most modulation schemes. Moreover, these nonlinearities can be corrected by digital pre-distortion (DPD).

As for modulation tests, two memoryless 1-D lookup tables are used to linearize the DPA. With the 20-MHz 64 QAM LTE signal, the output spectrum and constellation at 1.5 GHz are shown in Fig. 16. With −32.5-dB error vector magnitude (EVM), the DPA achieves P_{avg} of 15.2 dBm with the average PAE of 25.3%. The measured upper/lower ACLRs are −30.4 and −33.0 dBc, respectively. Fig. 17 shows the EVM and average PAE at different PBO levels, where it achieves

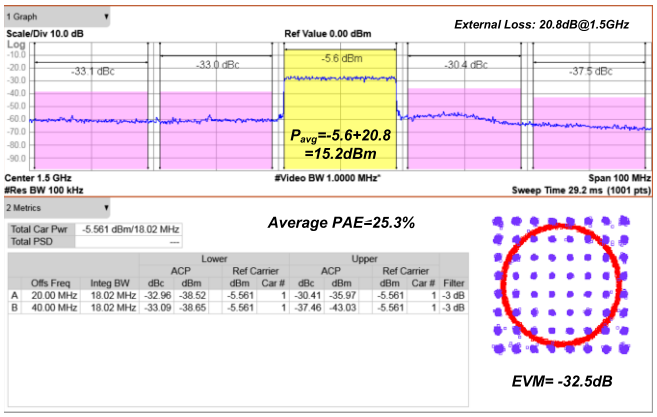

Fig. 16. Measured DPA output spectrum, average output power, and average PAE of the 20-MHz 64 QAM LTE signal at 1.5 GHz.

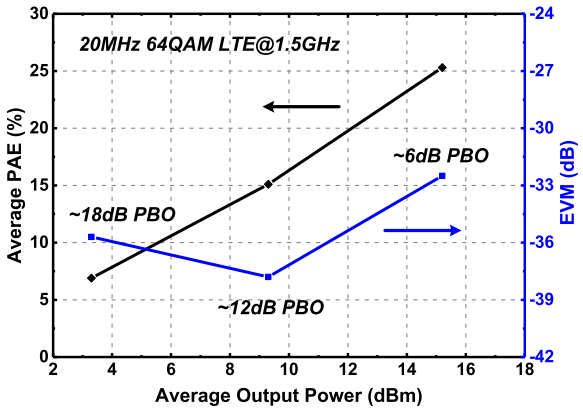

Fig. 17. Measured DPA EVM and average PAE of the 20-MHz 64QAM LTE signal at different PBO levels.

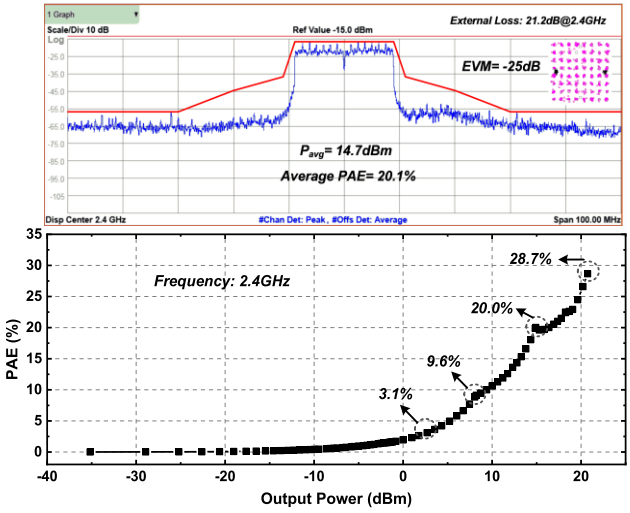

Fig. 18. Measured DPA demodulated 20-MHz 64 QAM WLAN signal and its CW PAE performance versus output power at 2.4 GHz.

P_{avg} of 15.2, 9.1, and 3.1 dBm with the average PAEs of ∼25%, ∼15%, and ∼7% at around 6-, 12-, and 18-dB PBOs, respectively.

As shown in Fig. 18, for the 20-MHz 64 QAM WLAN signal, the DPA achieves P_{avg} of 14.7 dBm and the average PAE of 20.1% with −25-dB EVM at 2.4 GHz. The CW performance at 2.4 GHz demonstrates the PAE of 28.7%,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	This work	RFIC 2018 [8]	ISSCC 2015 [19]*	JSSC 2017 [20]*	ISSCC 2019 [21]	JSSC 2019 [29]
Architecture	**Switched-transformer-based polar**	Multi-level outphasing	Class-G+Doherty polar	Class-G+Doherty polar	Subharmonic switching	Class-G IQ-cell-shared
Matching Newtork	**On-chip (1 transformer)**	Off-chip	On-chip (2 transformers)	On-chip (2 transformers)	On-chip (3 transformers)	On-chip (2 transformers)
PAE Improvement @Deep PBOs	**6/12/18 dB**	2.5/6/12 dB	6/12 dB	6/12 dB	3.5/7/9.5/12 dB	6 dB
Frequency (GHz)	**1.5**	1.7	3.71	3.5	1.9	2.2
1dB RF BW (GHz) (Frequency Coverage)	**1.3-3.5 (91.7%)**	NA	3.1-4.7 (41.0%)	2.9-4.3 (38.9%)	0.4 (36.4%)	NA
Peak Pout (dBm)	**21.4**	29.7	26.7	25.3	30	30.1
Peak PAE (%)	**31.3**	34.7	40.2 (DE)	30.4	45.9 (DE)	37.0
PAE @Different PBOs (%)	**27.7/16.6/7.7**	20.5/11.5/3.5†	37.0/26.2/NA (DE)	25.3/17.4/8††	41.3/35.3/ 32.2/24.2 (DE)	26.1
Modulation Signal	**20MHz 64QAM LTE**	20MHz LTE	1MS/s 16QAM	10MHz 256QAM	5MHz 16QAM	802.11g 20MHz 64QAM
Average Pout (dBm)	**15.2**	23.1	20.8	19.0	22.8	19.5
Average PAE (%)	**25.3**	15.3	28.8 (DE)	24.0	31.4 (DE)	14.7
EVM (dB)	**-32.5**	-21.9	-24	-35.0	-24.7	-40.7
Supply (V)	**1.1**	1.8/3.6	1.4/2.8	1.2/2.4	2.4/3.6	1.2/2.5
Chip Size (mm^2)	**0.8**	1.31	3.2	1.2	7.2	3.0
Technology	**40nm CMOS**	28nm CMOS	65nm CMOS	45nm CMOS SOI	65nm CMOS	65nm CMOS

*Results measured with GSG probe. †Estimated from Fig. 6 in [8]. ††Estimated from Fig. 6 in [20].

Fig. 19. Measured demodulated 40-MHz 256 QAM WLAN signal at 2.4 GHz.

20.0%, 9.6%, and 3.1% for 0-, 6-, 12-, and 18-dB PBOs, respectively. In addition, the measured demodulated 40-MHz 256 QAM WLAN signal is shown in Fig. 19, where the DPA achieves P_{avg} of 6.7 dBm and the average PAE of 6.5% with −33.7-dB EVM.

Table I summarizes the performance and compares with prior works. With the switched-transformer power combiner, the Doherty load modulation is realized and the DPA achieves effective efficiency enhancement during 0–18-dB PBO range. Moreover, it achieves broadband coverage over 1.3–3.5 GHz with an ultra-compact single-transformer footprint and only one 1.1-V power supply. If combined with the Class-G technique, the output power and PBO range will be further enhanced by 6 dB.

V. CONCLUSION

In this work, a fully integrated switched-transformer polar Doherty DPA is demonstrated, which introduces an eight-way PCT power combiner for broadband frequency coverage, deep PBO efficiency enhancement, and ultra-compact implementation. The wideband impedance transformation, power combining, and Doherty load modulation at multiple PBO levels are realized using a single-transformer footprint. The DPA achieves the state-of-the-art performance in terms of 0–18-dB deep PBO efficiency enhancement with only one 1.1-V power supply and the smallest die size. This switched-transformer Doherty DPA is suitable for low-cost SoC integration and most wireless applications with a wide dynamic power range.

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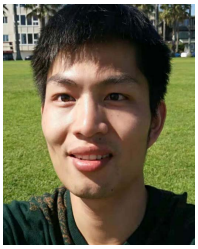

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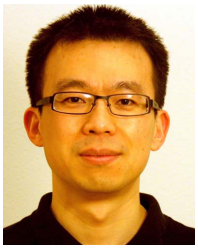

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