A 20dBm Outphasing Class E PA with High Efficiency at Power Back-off in 65nm CMOS Technology

Ali Ghahremani[#1], Anne-Johan Annema[#2], Bram Nauta[#3]
[#]IC design group, University of Twente, Enschede, Netherlands
[1]a.ghahremani@utwente.nl, [2]A.J.Annema@utwente.nl, [3]B.Nauta@utwente.nl

***Abstract*— This paper presents an outphasing class E PA (OEPA) in a 65nm CMOS technology, using a pcb transmission-line based power combiner. The OEPA can provide +20dBm output power from V_{DD}=1.25V at 1.4GHz with 61% drain efficiency (DE) and 58% power added efficiency (PAE). We introduced a technique to rotate and shift power and efficiency contours of the two branch PAs that enables more than 44dB output power dynamic range, reduces switch voltage stresses compared to conventional OEPAs and enables 41% DE and 24% PAE at 12.5dB back-off.**

***Index Terms*— Class E, Outphasing power amplifier, Load insensitive, Power contours, Efficiency contours, Reliability.**

I. Introduction

Reliable, efficient and highly linear Power Amplifiers (PAs) with high output power dynamic range (OPDR) are crucial building blocks for transmitters. For this, switch-mode class E power amplifiers with robust linearization techniques, e.g. outphasing class E PAs (OEPAs), are quite promising [1]. However, the design of such PAs in modern CMOS technologies is challenging because of the low break-down voltages of transistors. Moreover, mismatch between the two branches and component spread limit the OPDR [1] while imaginary parts of the PA loads reduce the efficiency in deep power back-off in outphasing systems [2].

Recently some papers reported on improving the efficiency of OEPAs in power back-off. The quasi load-insensitive OEPA with a package-integrated transformer based power combiner and Chireix compensation elements was proposed in [3] which could achieve high efficiency at power back-off. In this paper, we will use a similar structure but we use a transmission-line based power combiner, see Fig. 1 and add configurability to increase power efficiency in back-off. In [3], class E PAs were designed for a relative tank resonance frequency $q = \frac{1}{\omega_0\sqrt{LC}} = 1.3$ and d=1 (50% duty cycle) where L is the feed inductance, C is the total capacitance at the switch node and ω_0 is the operating (angular) frequency. Looking into the combiner, the load of the two class E branch amplifiers, Z_1 and Z_2, are given in [3] and are shown on the Smith chart in Fig. 1b for outphasing angles $0 < \Delta\theta_{out} < \pi$; the reference impedance is 20Ω. Compensation elements $\pm jB_c$ null

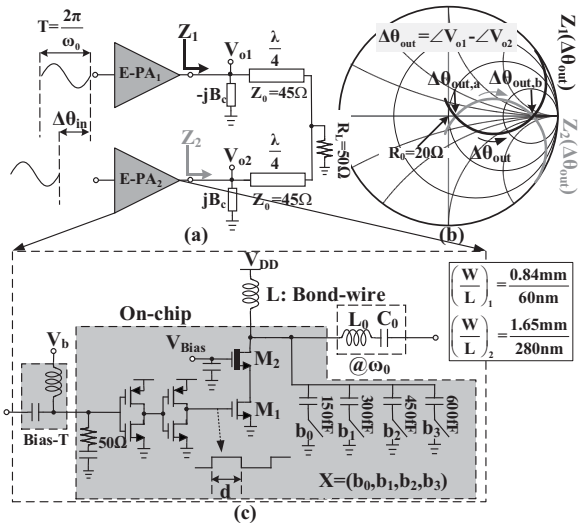

Fig. 1. a) OEPA structure with transmission-line based power combiner. b) Z_1 and Z_2 for $0 < \Delta\theta_{out} < \pi$ for a quasi-load insensitive OEPA [3]. c) schematic of the designed class E PA.

the imaginary part of Z_1 and Z_2 at $\Delta\theta_{out,a} = \pi/5$ and $\Delta\theta_{out,b} = \pi - \Delta\theta_{out,a}$. Fig. 2a shows simulated output power (P_{out}) and efficiency contours of a single class E PA in the configuration of Fig. 1a with an ideal switch, q=1.3 and d=1, and shows the outphasing angle dependent PA loads Z_1 and Z_2. Fig. 2b shows that at compensation points $\Delta\theta_{out,a}$ and $\Delta\theta_{out,b}$, corresponding to 1dB and 10dB back-off respectively, the loads of both branch PAs are purely ohmic and ideal OEPAs provide 100% efficiency. For $\Delta\theta_{out} > \Delta\theta_{out,b}$, however, OEPA efficiency reduces rapidly with increasing $\Delta\theta_{out}$ (and hence with increasing back-off) due to the non-zero imaginary part of the loads. Conventional compensation at lower power levels can improve deep power back-off efficiency at the cost of reduced efficiency at higher power levels, shown in Fig. 3. A 4-way outphasing system [2] can theoretically break this trade-off but adds complexity and lossy elements at the output that compromise efficiency. In this work, we present a new technique to achieve high efficiency at deep power back-off while keeping high efficiency at higher power levels.

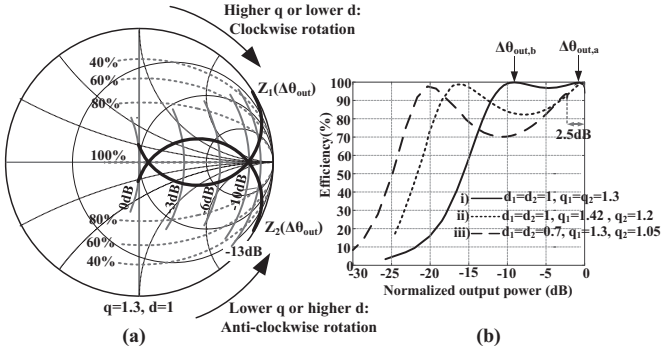

Fig. 2. a) Simulated normalized P_{out} (dB) and efficiency (%) contours of ideal single class E PA with q=1.3 and d=1. b) Efficiency versus normalized P_{out} for 3 different cases.

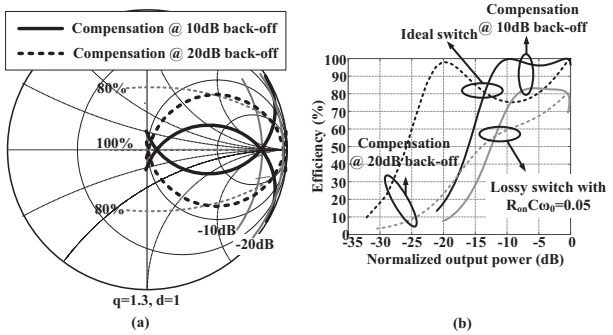

Fig. 3. Efficiency versus normalized P_{out} for compensation at 10dB and 20dB back-offs for ideal and lossy switches (with switch-on resistance R_{on}). Conventional compensation at lower power levels reduces the efficiency at higher power levels.

II. Rotation

As illustrated in the Smith chart of Fig. 2a, by changing the duty cycle d and the relative tank resonance frequency q, the shape of the power and efficiency contours hardly changes except for a rotation: clockwise (anti-clockwise) rotation for higher (lower) q or lower (higher) d. Proper combinations of q for the branch PAs (e.g. higher q for E-PA_1 and lower q for E-PA_2) now can shift the compensation points, thereby allowing (theoretically) 100% efficiency at many more back-off points. Curves i) and ii) in Fig. 2b illustrate this principle: by changing the branch PAs' q about 10% in opposite directions the compensation point is shifted almost 7dB into back-off. Noting that q is proportional to the resonance frequency of the tank at the switch node, the rotation can be implemented by switched capacitor banks X_1 and X_2 at the class E switches' outputs as shown in Fig. 1c.

III. Shift

It can be shown that reducing d and q rotates the contours in opposite directions. Therefore for a lower value of d for both branch PAs, a lower value of q can be found to keep the contours (almost) unchanged while the output power of both branch PAs are reduced; this corresponds to shifting the power contours to the left. This can be combined with rotation to improve the efficiency in deep power back-off. Curves i) and iii) in Fig. 2b illustrate this: reducing d_1=d_2 to 0.7 for q_1=q_2=1.1 shifts power contours 2.5dB to the left. Subsequently changing q_1 to 1.3 and q_2 to 1.05 rotates power and efficiency contours to obtain the compensation point shifted to almost 20dB back-off.

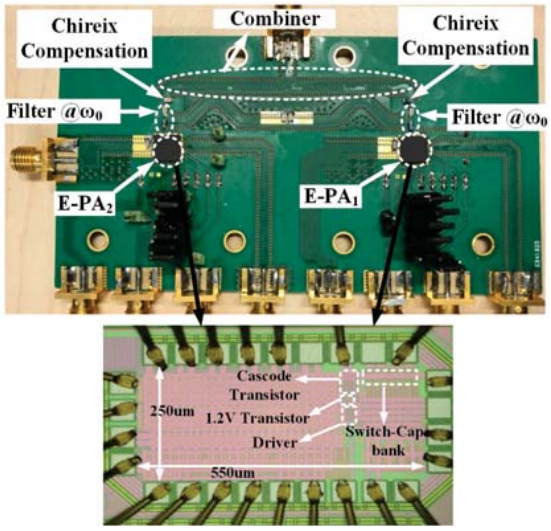

Fig. 4. Measurement setup and chip microphotograph

IV. Implementation

To experimentally demonstrate this rotation-shift principle to keep high efficiency at deep power back-off, an OEPA was implemented in a standard 65nm CMOS technology, using a pcb transmissionline based power combiner. The schematic of a single class E PA and driver stage are shown in Fig. 1c. The switch transistor is a 1.2V device while the cascode transistor is a thick oxide 2.5V device, allowing switch voltage up to 4V. At zero outphasing angle (maximum P_{out}) V_{DD} up to 1.25V can be used, resulting in maximum +20dBm P_{out} at 1.4 GHz. The feed inductance was implemented by a bond-wire inductance. The loaded Q of the output filter for maximum P_{out} was 5 for R_L=50 Ohm. The duty cycle d of the input driving waveform can be controlled by bias voltage V_b. Switch-capacitor networks with 4 control bits X_1 and X_2 were used at the switches' outputs to tune the q of the 2 branch PAs independently. Chireix compensation elements were used to compensate the imaginary part of the loads at almost 10dB back-off. The measurement set-up and the chip microphotograph are shown in Fig. 4.

V. Measurement Results (CW Operation)

Fig. 5 shows measured P_{out} versus input phase difference for 3 situations. For the conventional load insensitive design, +20dBm maximum P_{out} is achieved while the minimum P_{out} is limited to -15dBm which result in OPDR=35dB. For setting 1, the power contours are shifted by almost -2.1dB and rotated which result in a maximum output power of +17.9dBm. OPDR is improved to more than 37.5dB. Further reducing duty cycles (setting 2), result in almost -5.4dB shift in power contours and the OPDR is improved to more than 44dB.

	V_b	X_1	X_2
Conventional	0.6	0000	0000
Setting 1	0.5	0111	0101
Setting 2	0.45	0000	1111

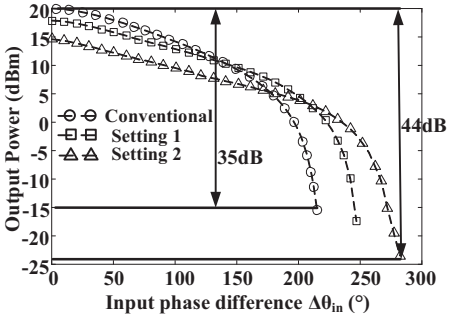

Fig. 5. Measured P_{out} versus input phase difference $\Delta\theta_{in}$.

Fig. 6 shows measured drain efficiency (DE) and power added efficiency (PAE) versus normalized output power. Measured DE at peak output power is 61% and maximum efficiency is 69% at 2.5dB back-off. PAE versus normalized output power is also shown in Fig. 6; at maximum P_{out}, PAE is 58%. By shifting and rotation, more than $\times$2.5 better DE and almost $\times$2 better PAE at 12.5dB back-off were achieved. PAE at 0dBm output power (20dB back-off) is improved from 2% to 3.5% and hence to transmit 1mW power the conventional OEPA draws 50mW from the supply while the proposed technique reduces the supply power to less than 29mW.

VI. Maximum Switch Voltage

Measured maximum switches' voltages for both PAs are shown in Fig. 7. For the conventional quasi load-insensitive configuration, maximum switches voltages at peak output power are almost 4V. For E-PA_1, the maximum switch voltage is increased to 4.6V at 15dB back-off which can cause reliability issues. Measurements show that our rotate-and-shift technique can significantly reduce the maximum switch voltage in power back-off which reduces transistor degradation and hence improves the PA life-time.

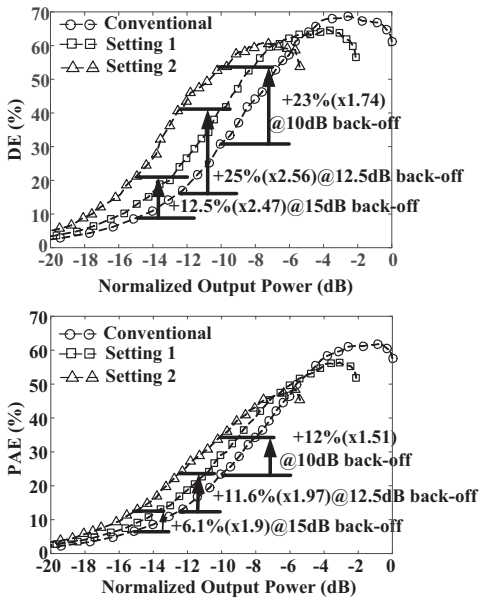

Fig. 6. Measured drain efficiency and power added efficiency versus normalized P_{out}; 0dB corresponds to 20dBm.

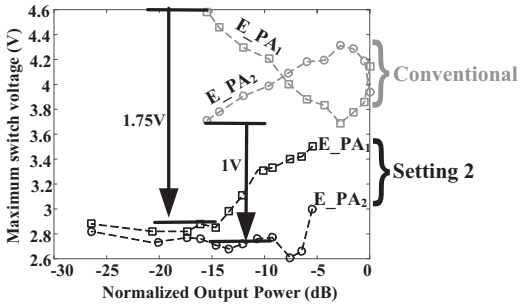

Fig. 7. Measured maximum switches' voltages versus normalized P_{out} for conventional quasi load-insensitive OEPA and for the proposed technique with setting 2

VII. Measured QAM Performance

The designed OEPA was also characterized using single carrier 7.1dB PAPR 256QAM amplitude modulated signal with 40Mbit/s (6.75MHz BW) data rate. After measuring AM-AM and AM-PM conversions using a CW single tone signal at 1.4GHz, a memory-less digital pre-distortion (DPD) was implemented. The effect of the pre-distortion on the power spectral density (PSD) of the transmitted signal is shown in Fig. 8a. Symbol constellation is shown in Fig. 8b; -37.4dB EVM is obtained for 40Mbit/s data rate. The measured average output power of the OEPA in conventional setting is 12.9dBm with measured 42% DE and 34% PAE.

Finally, QAM modulated signals with different average output power levels are applied to the OEPA to

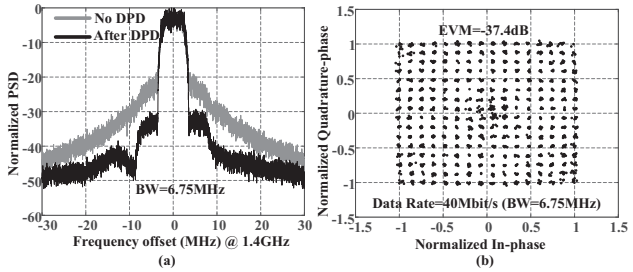

Fig. 8. (a) Measured output power spectral density and (b) symbol constellation with a 7.1dB PAPR 256-QAM modulated signal

demonstrate the effect of the proposed technique in efficiency improvement of OEPA at back-off. A summary of measured DEs and PAEs are given in Table I for 6.5dB PAPR 64-QAM modulated signals with 30Mbit/s data rate. At 5dB back-off (8.5dBm average output power) the DE and PAE are improved from 21% and 16% for the conventional load insensitive OEPA to more than 37% ($\times$ 1.75) and 24% ($\times$ 1.5). At 10dB back-off DE and PAE are improved by $\times$2.4 and $\times$1.8.

TABLE I
DE AND PAE FOR 64-QAM MODULATED SIGNAL FOR DIFFERENT AVERAGE OUTPUT POWER LEVELS AT 30MBIT/S

$P_{out,avg.}$	DE (%)		PAE (%)		State
	Conv.	Sett.2	Conv.	Sett.2	
13.5dBm	45	-	37	-	Max (modulated) power
8.5dBm	21	37	16	24	5dB back-off
3.5dBm	6.3	15	4.9	8.9	10dB back-off

In Table II the measured results are benchmarked against other CMOS PAs. Operating in the conventional load-insensitive mode, our OEPA has the best DE and PAE for maximum output power as well as for modulated signals with high PAPR. DE at 12.5dB back-off is more than $\times$2 better than other published CMOS PAs. Reported PAE at 12.5dB back-off in [6] is comparable to the presented work; however the multi level outphasing technique proposed in [6] comes with high system complexity and lower DE and PAE for maximum output power. Note that scaling our PA to achieve higher than 20dBm maximum output power levels has (ideally) no impact on DE and PAE numbers [8]. Also, this technique can be shown to be effective at higher frequencies for OEPAs with integrated combiners [4] if switch loss is the dominant loss mechanism. Although our rotation-shift technique also reduces switch voltage stresses, we cannot benchmark this due to lack of relevant data in literature.

VIII. CONCLUSION

A new technique to improve power back-off efficiency of outphasing class E PAs was presented. This technique also improves the output power dynamic range and PA life-time. It was shown that by rotating and shifting power contours and rotating efficiency contours of the two branch PAs, more than $\times$2 efficiency improvement at 12.5dB back-off can be obtained. The technique was validated with CW measurement and on 6.5dB PAPR 5MHz 64-QAM modulated signals with different average output power levels.

TABLE II
PERFORMANCE COMPARISON

	[4]	[5]	[6]	[7]	**This Work**
CMOS Technology	40(nm)	45(nm)	65(nm)	65(nm)	**65(nm)**
Topology	OEPA	ODPA(a)	OEPA	Doherty	**OEPA**
Combiner	On-chip	Off-chip	Off-chip	On-chip	**Off-chip**
Frequency (GHz)	5.9	0.9-2.4	2.4	3.71	**1.4**
Supply (V)	1.2	1.2	2.5-0.8(b)	3-1.5(c)	**1.25**
$P_{out,Max}$ (dBm)	22.2	25-25	27.7	26.7	**20**
DE at $P_{out,Max}$	49.2	60-52	NR(d)	40.2	**61**
PAE at $P_{out,Max}$	34.9	55-45	45	NR	**58**
DE/PAE at 12.5dB back-off (%)	<18 /<13(e)	17/12 -10/7(f)	NR /20(f)	11/NR -24/NR(f)	**41 /24**
Signal (PAPR(dB))	64-QAM (7.5)	LTE (6)	OFDM (7.5)	16-QAM (5.4)	**256-QAM (7.1)**
Fractional BW (%)	0.34	1.11-0.42	0.83	– –(g)	**0.48**
$P_{out,avg.}$(dBm)	16.4	18.9	20.2	20.8	**12.9**
DE at $P_{out,avg.}$	23.3	– –	31.9	28.8	**42**
PAE at $P_{out,avg.}$	16.1	32-22	27.6	– –	**34**
$\frac{V_{cmax}}{V_{DD}}$ at $P_{out,Max}$ / 15dB back-off (h)	NR	NR	NR	NR	**3.3 /2.3**

(a)Outphasing class D PA (b)Multi-level supply (c)Full and half V_{DD} (d)Not reported (e)DE=18% and PAE=13% at 9dB back-off, obtained from publication figures (f)Obtained from publication figures (g)4Mbit/s data rate (h)$\frac{V_{cmax}}{V_{DD}}$: maximum switch voltage normalized to V_{DD}

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