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A Common-Gate Switched, 0.9W Class-E Power Amplifier with 41% PAE in 0.25μm CMOS

Changsik Yoo* and Qiuting Huang

Integrated Systems Laboratory (IIS), Swiss Federal Institute of Technology (ETH), Zurich, Switzerland

Abstract

A power amplifier (PA) has been implemented in a standard 0.25μm CMOS technology and shown to deliver 0.9W output power to 50Ω load with 41% power added efficiency (PAE) from a 1.8V supply. The PA employs the class-E configuration with finite DC-feed inductance and common-gate switching scheme to achieve high efficiency and not to stress the active devices.

Introduction

Progresses in the last five years have shown that CMOS can be a competitive technology also for RF transceivers, including those for applications with stringent requirements such as cellular telephony [1]. The prospect of a single-chip radio arouses considerable interest, even though it remains to be researched whether it is either feasible or advantageous to put the RF front-end on the same die as the rest of the mobile terminal. Even the less ambitious objective of implementing the mobile terminal in a set of separate chips in the same CMOS technology may bring considerable economic benefits, however, as it enables a company to rationalize the number of different technologies that have to be maintained for a given product. In this spirit, the feasibility of realizing efficient PAs in regular CMOS technology is also beginning to receive increased attention. Recent papers have reported 1W PAs with more than 40% PAE using 0.8μm and 0.35μm CMOS, respectively [2]-[3]. This paper reports a 0.25μm CMOS PA at 900MHz.

Effect of scaling on the design of a CMOS PA

Power consumption considerations dictated by standby time require that the RF receiver front-end for a wireless application be realized in a deep sub-μ CMOS technology [4] and recent studies have shown that a 0.25μm CMOS GSM receiver is capable of 20mA performance [1]. For a CMOS PA to be compatible with the objective of either a single-chip radio or a chip set in the same technology, it is important that it also be realized in the same deep sub-μ CMOS process. Since the safe operating voltage of a FET reduces as its minimum channel length L_{min} scales down, it becomes increasingly hard to realize a good PA, in contrast to the case for the receiver. The quadratic dependence of the power output on the supply voltage means that the load resistance R_L seen by the PA needs to be reduced rapidly for a given output power as L_{min} decreases, and the transformation ratio m of the impedance matching network between the PA output and the antenna increases. For a given quality factor, the loss due to the matching network increases with m, and the efficiency decreases. Although decreasing L_{min} and increasing transconductance coefficient (K') enable the on-resistance r_{on} of the switch in a switching PAs to improve, this improvement (offset also by the reduction in gate-drive) is slower than the decrease in R_L, as shown in Fig. 1, which further decreases efficiency. The increase of the inductor and capacitor loss relative to R_L also decreases achievable efficiency.

To maintain efficiency in a deep sub-μ CMOS PA, positive feedback has been combined with class-E configuration recently to form an injection-locked oscillator whose oscillation frequency is locked to that of the input signal [3]. The drawback of such a technique is that the PA is prone to locking onto interfering signals picked up by the antenna from adjacent mobile users. On reliability grounds, it would also be more prudent to limit the stress on a transistor to the recommended supply voltage (3.3V for 0.35μm and 2.5V for 0.25μm) rather than the maximum rating, therefore delivering 1W RF power remains a challenge for a deep sub-μ CMOS PA.

Common-gate switched class-E PA with finite DC-feed inductance

Given the above, our focus in the 0.25μm CMOS PA design is on finding ways to relieve the pressure on the supply voltage V_{DD} and the load resistance R_L. One way to provide such relief is to use a finite inductance L_1 instead of an RF-choke (RFC) for the DC feed [5] in a class-E PA, shown in Fig. 2. The load network can still be optimized to ensure the voltage across the switch is settled to zero with zero slope before the switch turns on, so that the power loss due to overlapping nonzero switch voltage and current is minimized by such soft switching. Fig. 3 shows the optimal values of $B_1=\omega C_1$ and R_L for 1W output with V_{DD}=1.8V versus $X_1=\omega L_1$. With L_1=0.5nH at 900MHz, the optimum R_L reaches a peak of 4.4Ω, which is more than twice that for an RFC. Compared to other classes of both linear and switching PAs, R_L=4.4Ω is also 2–3 times higher. The required shunt capacitance C_1 is now 60% larger, which can absorb the output capacitance of wider switching transistors (smaller r_{on}), whereas L_1 is small enough to be implemented by bondwire. Therefore, for the same output power and supply voltage, higher efficiency can be achieved in a class-E PA with finite DC-feed inductance. One further advantage is that the additional degree of freedom provided by finite L_1 enables C_1 and R_L to be set in such a way that, for a constant output power, the peak voltage stress on the switch is no longer $3.57\times V_{DD}$, as is the case with an RFC. At a limited efficiency of 50–60% or less for practical class-E PAs, the peak stress can be as low as $2.5\times V_{DD}$.

A further way to reduce the stress on the switching transistor is to switch it from the source instead of the gate. Since the switching

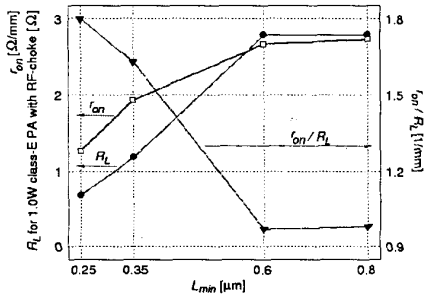

Fig. 1. Load resistance R_L for 1.0W class-E PA with RF-choke, the on-resistance r_{on} of an nMOS switch per unit channel width, and r_{on}/R_L versus minimum channel length L_{min}.

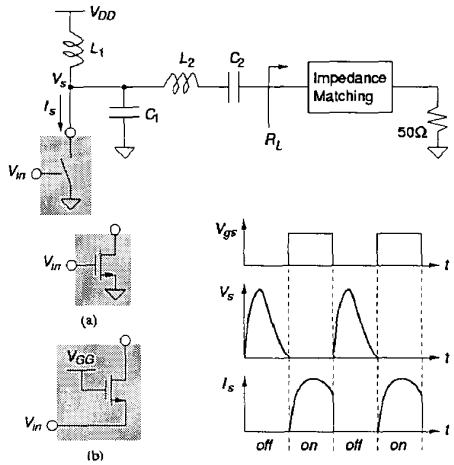

Fig. 2. Class-E PA with (a) CS switch and (b) CG switch.

*He is now with Samsung Electronics, Yongin, Korea.

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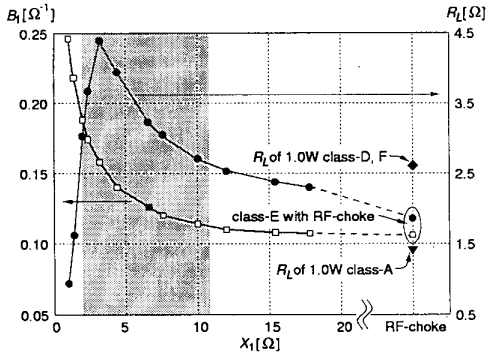

Fig. 3. Element values of class-E load network for 1.0W with V_{DD} = 1.8V ($B_1 = \omega C_1, X_1 = \omega L_1$).

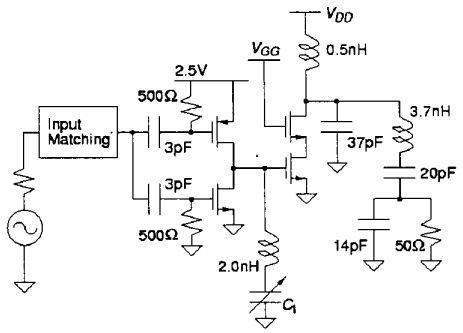

Fig. 4. Common-gate switched class-E PA with finite DC-feed inductance.

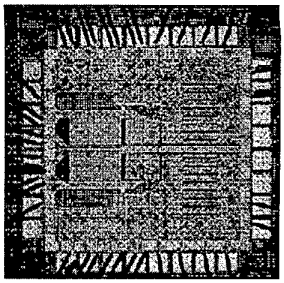

Fig. 5. Chip photograph.

transistor's source swings up with the input voltage, its drain-source voltage swing is reduced. To avoid presenting the input driver stage with a low impedance node, a common-source (CS) stage is combined with the common-gate (CG) switch into a cascode. This is shown in the single-ended version of our common-gate switched class-E PA in Fig. 4, complete with the load network and the input driving stage. During OFF state, the drain voltage of the CS switch rises to V_{GG}–V_T, which in a 0.25μm technology is roughly 2V if V_{GG}=2.5V. Since the CG switch can safely sustain another 2.5V, the allowable maximum stress on the combined switch is 4.5V. This allows the supply voltage to be as high as about 1.8V, which is almost twice the value allowed for a single CS switch. One watt power can now be delivered without forcing the load resistance R_L to an unrealistically low value.

Since a cascode switch has higher r_{on} per unit channel width than a single transistor during ON state, wider transistors (15mm) have been used so that the resulting r_{on} is sufficiently small compared to the loss in the reactive components of the load network. The junction capacitances associated with the output node of the cascode switch can still be absorbed by the large shunt capacitance C_1. The gate capacitance of the cascode switch, on the other hand, is as high as 26pF. To mitigate its loading on the preceding driver stage, a 2nH bondwire inductance is used to resonate out the gate capacitance. An external series capacitor is also included in the LC network to allow some fine tuning of the resonant frequency. The push-pull input stage operates in class-C mode.

Experimental Results

Fig. 5 is the photograph of the fabricated CMOS PA whose size of is 2.0mm×2.0mm. During test, bare die has been attached directly to the PCB ground plane. To minimize the number of passive components, the inductance of the impedance matching network is merged with that of the load network, so that the complete passive network of the PA's output stage consists of two bondwire inductors and one on-chip and two off-chip capacitors. High integration level is thus achieved. The implemented PA is differential and baluns are used at both the input and the output to combine the two single-ended paths.

The measured output power, drain efficiency (DE) and PAE of the PA at 900MHz are shown against the supply voltage in Fig. 6. At the designed V_{DD} of 1.8V, the PA delivers 0.9W power to the 50Ω load. The DE is roughly constant, reaching 46% at 0.9W, where the PAE reaches 41%. Measurements shown in Fig. 7 confirm that output power, DE and PAE are fairly constant over a 60MHz frequency range. Despite the much lower breakdown voltages of the 0.25μm CMOS technology, this PA has achieved comparable performance to the other CMOS PAs as shown in Table 1.

Conclusion

With the trend moving towards lower power-class (20–24dBm) transmitters in next generation wireless standards, the results achieved in this design present another step forward towards showing that CMOS PAs with good efficiencies are realistic despite steadily declining FET breakdown voltages.

Table 1. Performance comparison of CMOS PAs. (V_{STRS} = maximum voltage stress on transistors.)

Ref.	L_{min} [μm]	Freq. [GHz]	V_{DD} [V]	V_{STRS} [V]	P_{out} [W]	PAE [%]	Class
[2]	0.8	0.85	2.5	5.0	1.0	42	D
[3]	0.35	1.9	2.0	~5.0	1.0	48	E
This PA	0.25	0.9	1.8	2.5	0.9	41	E
			1.9	2.75	1.0	41.4	

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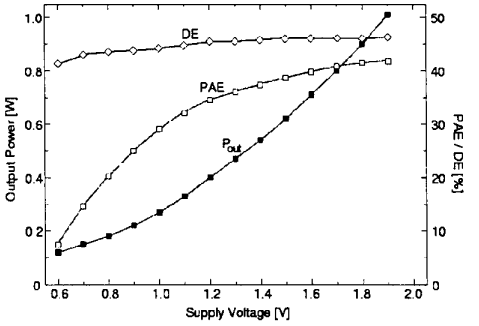

Fig. 6. Measured output power and efficiency vs. supply voltage.

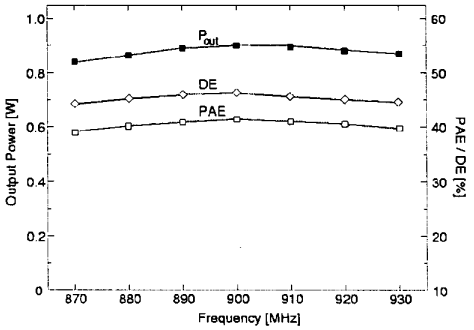

Fig. 7. Measured output power and efficiency vs. frequency.

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