A 29 dBm 70.7% PAE Injection-Locked CMOS Power Amplifier for PWM Digitized Polar Transmitter

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***Abstract*—This letter presents an injection-locked CMOS power amplifier for pulse width modulation (PWM) digitized polar transmitter. A power oscillator combined with injection-locking technique reduces the required driving power and provide high drain efficiency in the power stage. The switched power oscillator is proposed for PWM digitized polar transmitter. To achieve differential to single output and impedance transformation, a lumped element balun, employing a minimum number of discrete components, is used. The power amplifier achieved a power-added efficiency of 70.7% at a maximum output power of 29.05 dBm. The measured drain efficiency in the power stage was 72.7% at 820 MHz. The chip is implemented with a 0.18 μm CMOS process. The total chip size is 0.48 mm^2.**

***Index Terms*—CMOS, drain efficiency (DE), injection-locked, power amplifier (PA), power-added efficiency (PAE), switched power oscillator (SPO).**

I. Introduction

RECENTLY, efforts toward a single-chip radio have stimulated the development of a CMOS power amplifier (PA). The integration of radio-frequency (RF) components, including PA, is needed to realize the true meaning of system-on-a-chip. Recent works in CMOS switching PAs show high power and efficiency performance [1]–[5].

To achieve the high efficiency performance, the on-resistance of the switching transistor should be minimized and sufficient drive power should be provided to the input of the switching transistor. The size of the switching transistor should be large enough to reduce r_{on}. However, the large size of the transistor also increases the parasitic gate capacitance. This burdens the LO driving circuits and requires a substantial driving power. Therefore, in the conventional Class-E PAs of the previous works, the power consumption of the driver stage degraded the power added efficiency (PAE) by over 10% from the drain efficiency (DE) of the PA.

The linear amplification using pulse width modulation (PWM) digitized polar transmitter enables the linear amplitude modulation with high-Q band-pass filter (BPF) [6]. Therefore, the design of high efficient CMOS switching PA, which enables switching operation with a pulse stream of amplitude information, is required.

In this letter, an injection-locked CMOS PA [4], [5] for PWM digitized polar transmitter is proposed and demonstrated. To achieve high PAE, power oscillator (PO) and injection-locking concept are employed.

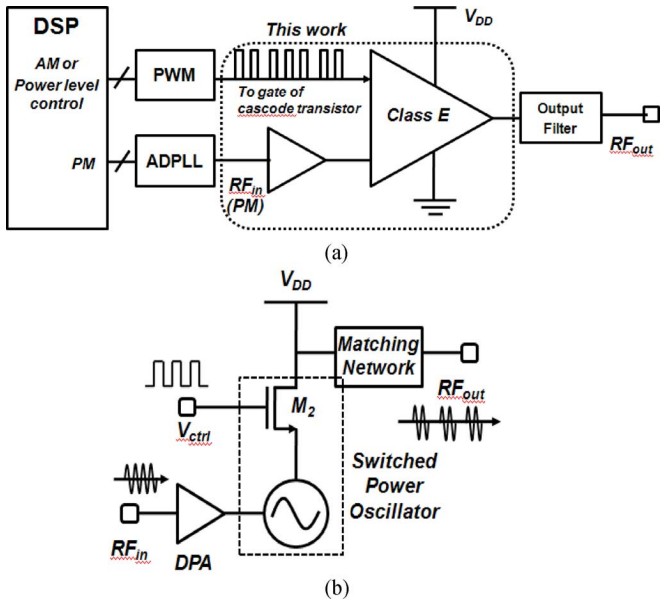

Fig. 1. (a) PWM digitized polar transmitter (b) Injection-locked CMOS PA.

II. Switched Power Oscillatorfor PWM Digitized Polar Transmitter

Fig. 1(a) shows the simplified block diagram of PWM digitized polar transmitter. The PWM digitized amplitude signal is modulating the gate bias of the cascade transistor. The simplified block diagram of injection-locked CMOS PA is shown in Fig. 1(b). The cascode transistor, M_2, prevents the breakdown of the switching transistor in the near watt-level CMOS PA. Furthermore, the cascade transistor is used to switch the RF signal by PWM digitized amplitude signal [6]. Fig. 2 shows the schematic of proposed CMOS PA. The PA consists of an output matching network, cascode transistors (M_2), parasitic gate capacitance, negative resistance of a CS transistor (M_1), and the resonant inductor (L_t). The core circuit of the PA is a switched

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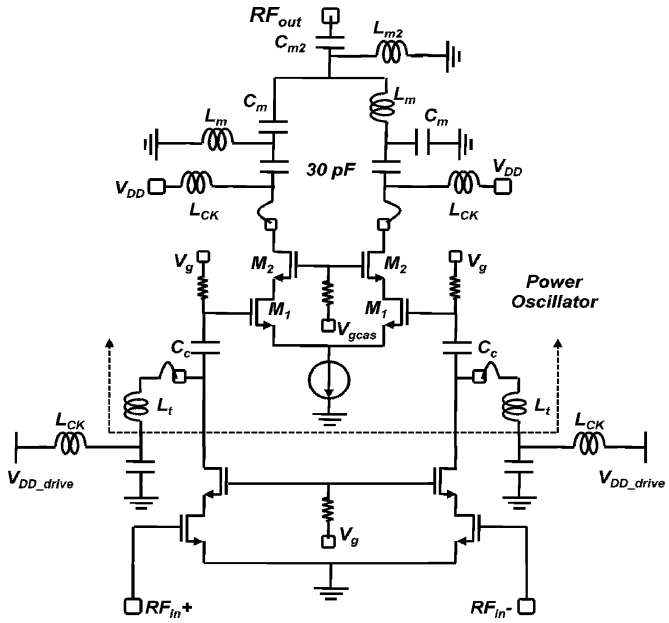

Fig. 2. Schematic of injection-locked CMOS PA.

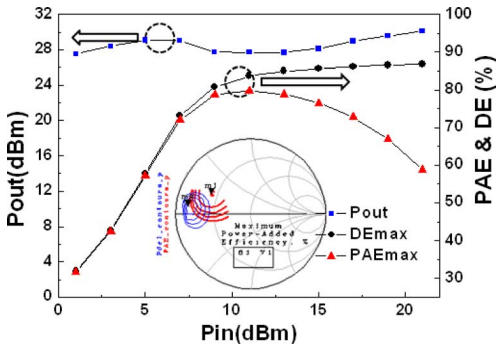

Fig. 3. Load-Pull simulation with respect to input power.

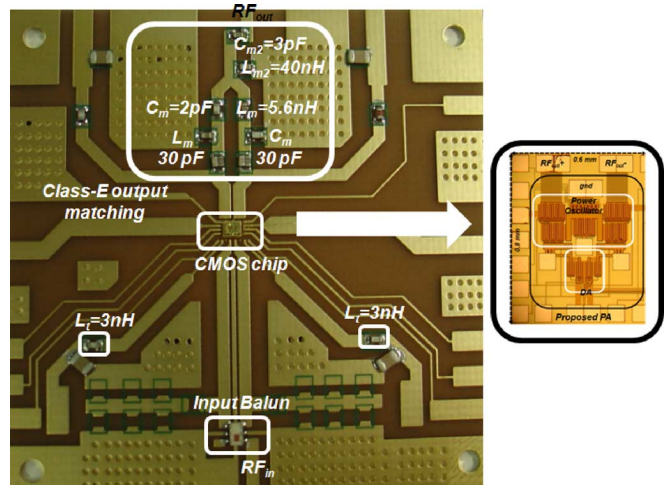

Fig. 4. Chip micrograph.

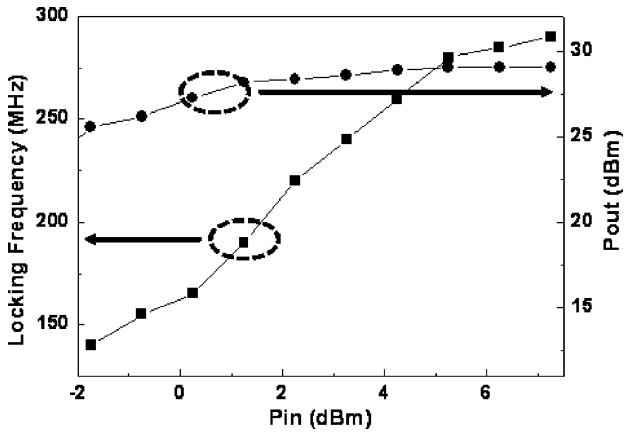

Fig. 5. Measured output power, and locking frequency versus input power with 3.3 V supply voltage.

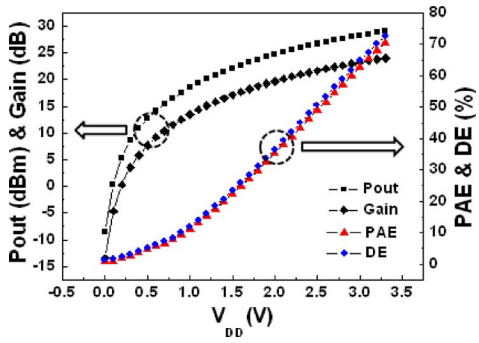

Fig. 6. Measured output power, PAE, and DE versus $\mathrm{V_{DD}}$ with 5 dBm input power.

power oscillator (SPO). The SPO works as a typical power amplifier at the drain node and it also works as an oscillator at the gate of common source (CS) power transistor [4], [7].

III. The Proposed Injection-Locked CMOS PA

A differential cascode CMOS PA and an integrated driver amplifier have been designed by using the TSMC 0.18 μm CMOS process. The injection-locked CMOS PA consists of the power oscillator and a driver amplifier. The output of the SPO is locked to the injected signal through the driver amplifier. The size of CS transistor, M_1, should be large enough to reduce on-resistance to achieve high output power and high efficiency. The selected gate length and width of the CS power transistor, M_1 are 0.18 and 3072 μm, respectively. The corresponding dimensions of the CG transistor are 0.35 and 3072 μm. The gate bias voltage of the CS power transistor is 1.0 V. Fig. 3 shows the load pull simulation results with respect to the input power. The single-ended cascode power stage was used in the simulation with the assumption of an ideal load. From the simulated results, we obtained the maximum output power and efficiency by finding the optimal load impedance. Too small driving power shows a poor efficiency and too large driving power degrades the PAE from the DE. The optimal load impedance, Z_{opt}, which gives the maximum efficiency of $14.4 + \mathrm{j}10.54$ at the input power of 13 dBm. The simulated single-ended output power was 27.7 dBm and the maximum DE and PAE were 85% and 78%, respectively. The output matching network in Fig. 2 was made with off-chip LC components to achieve the optimal load impedance in the PA implementation. Furthermore, to combine the outputs of differential PA into a single-ended output and to perform the impedance transformation simultaneously, a simple LC-CL network is adopted [2] as shown in Fig. 2. However, the large power transistor size requires the large driving power of

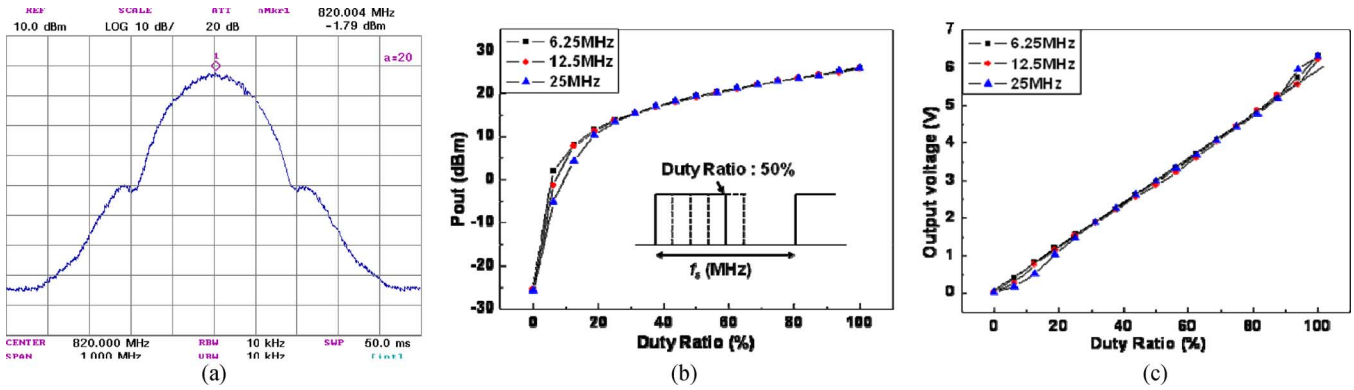

Fig. 7. (a) Spectrum mask with GSM modulation (b) Measured output power of PWM digitized polar Tx. (c) Measured output voltage with PWM.

13 dBm and degrades the PAE by over 7% from the DE of PA. The efficiency of the driver stage is also not 100% and driving ability is not perfect. Therefore, the power consumption of the driver stage has degraded the PAE by over 10% from DE of PA. To overcome this problem, the power oscillator and injection-locking concept are employed. The injection-locking requires only small driving power for the SPO which has the large power transistor size [4]. Therefore, high drain efficiency can be achieved due to low on-resistance and the high PAE is also achieved due to the small driving power.

IV. Measurement Results

A micrograph of the proposed PA and output matching network with the printed circuit board (PCB) is shown in Fig. 4. The chip size is 0.6×0.8 mm^2 including pads. The chip is directly mounted on a FR4PCB. The output balun uses discrete high frequency LC components. The input power is fixed at 5 dBm, and the output power is controlled by the supply voltage of the power stage. The measured injection-locking frequency was from 630 to 910 MHz when the input power was 5 dBm. The injection locking occurs at the input power as low as 1 dBm. Fig. 5 shows the measured output power and locking frequency versus input power. The desirable input driving power range is 4 to 6 dBm from Fig. 5.

The output power and efficiency were measured when the supply voltage varies from 0.3 to 3.3 V. The measured driving current was only 17 mA with 1.8 V supply voltage. Fig. 6 shows the measured PAE and DE versus V_{DD} at 820 MHz of the injection-locked frequency. The maximum output power is 29.05 dBm. The PAE and DE are 70.7% and 72.7% at the maximum output power, respectively. The difference between PAE and DE are only 2%. Therefore, the proposed injection-locked CMOS PA shows a very high overall efficiency. The measured dynamic range was 20.5 dB at supply voltages range from 0.3 to 3.3 V. This result shows a good match with theoretical value of 20.7 dB. The maximum PAE and DE of 71.8% and 73.9% at the output power of 28.97 dBm are achieved by controlling the cascode gate bias voltage of 2.3 V. The single-ended output power is higher than 28 dBm over a frequency range of 730–880 MHz. Fig. 7(a) shows the measured spectrum with GSM signal at 28 dBm of output power. The linearity performance versus the duty ratio of PWM are measured in Fig. 7(b) and (c) with PWM signals, which sampling frequencies are 6.25, 12.5, and 25 MHz. The leakage at off-state was 44.6 dBc. The measured results show the linear amplitude modulation. The performance of the designed PA is compared with that of PAs in other literatures in Table I.

TABLE I
Comparison the Performance of Power Amplifiers

Freq. (GHz)	P_{out} (dBm)	V_{DD} (V)	PAE (%)	DE (%)	Tech. (CMOS)	Ref.
0.875	31.7	3.3	62.4	67.2	0.18-μm	[1]
1.7	31	2.5	58	67	0.13-μm	[2]
0.7	30	2.3	62	-	0.35-μm	[3]
1.9	30	2.0	48	49	0.35-μm	[5]
0.82	**29.05**	**3.3**	**70.7**	**72.7**	**0.18-μm**	**This work**

V. Conclusion

A 29 dBm 70.7% PAE injection-locked CMOS PA for PWM digitized polar transmitter is implemented using the 0.18 μm RF CMOS process. To achieve a high PAE, power oscillator and injection-locking concept are employed. The achieved peak PAE and DE were 71.8% and 73.9%, respectively. By using the injection-locked CMOS PA, the only 2% of difference between PAE and DE can be achieved.

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