A 2–24 GHz SiGe HBT Cascode Non-uniform Distributed Power Amplifier Using A Compact, Wideband Two-Section Lumped Element Output Impedance Transformer

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***Abstract*—This paper presents a 2–24 GHz SiGe HBT cascode, non-uniform distributed power amplifier (NDPA). Optimum impedances at each SiGe HBT cascode are obtained by simultaneous characteristic impedance scaling of the collector transmission lines (TLs) and SiGe HBT emitter area tapering. To further boost output power (P_{out}), a compact, wideband two-section lumped-element output impedance transformer is proposed, which lowers a load impedance from 50 to 25 Ω. Each λ/4 transformer is realized by four cascaded C-L-C π-networks integrated into a single symmetric inductor, for its compact size and high passive efficiency. The proposed SiGe HBT cascode NDPA achieves a saturated P_{out} of 21.3 dBm at 8 GHz and peak power added efficiency (PAE) of 21.7% at 4 GHz, with its 3 dB bandwidth and PAE higher than 12.2% from 2 to 24 GHz.**

***Keywords*—BiCMOS, broadband, cascode, distributed power amplifier (DPA), HBT, lumped element, non-uniform, phased array, SiGe, transformer, transmission line (TL), wideband.**

I. Introduction

The increasing demand for highly integrated wideband phased arrays for high resolution imaging, electronic warfare, and wireless communications has accelerated the development of compact, low cost, and energy-efficient Si-based transmit and receive chains [1]. Among many building blocks, design of Si-based broadband power amplifier (PA) is the most challenging due to the unavoidable trade-off between high speed and large voltage swing operation of the transistors. Distributed amplifiers, a well-known topology to achieve larger than one-decade bandwidth, suffers from poor power added efficiency (PAE) and low output power (P_{out}). While distributed PAs with stacked transistors [2][3] have attained high P_{out}, the phase misalignment among transistors and the non-optimum load at each active device limit their PAE lower than 20%.

Non-uniform distributed PAs (NDPAs) achieve optimum power matching by simultaneously scaling the active device area and characteristic impedance (Z_0) of output transmission lines (TLs) [4]. Bandwidth (BW) extension and increasing P_{out} of the NDPA, however, are restricted by a very high Z_0 of first section of the output TLs (>100 Ω), which are difficult to implement in Si-based technologies, since their maximum achievable Z_0 is typically less than 80 Ω. To resolve this, the authors in [5] proposed a GaN NDPA with a coupled line-based output impedance transformer. This bulky on-chip impedance transformer, however, is not suitable for a fully integrated Si-based phase array.

In the present paper, a 2–24 GHz SiGe HBT cascode NDPA with a compact, low loss, and wideband output impedance transformer is proposed. For broadband impedance transformation of R_L from 50 to 25 Ω, two λ/4 lumped element impedance transformers are placed in series at the output of the NDPA. Each λ/4 impedance transformer, realized by four-section C-L-C π-networks embedded into a single 3-turn symmetric inductor, dramatically reduces die area and insertion loss. The proposed SiGe HBT cascode NDPA, with an on-chip RF choke, achieves a peak saturated P_{out} (P_{sat}) of 21.3 dBm and a PAE of 12.2–21.7%, with a 3-dB P_{sat} BW of 2–24 GHz, demonstrating optimum power matching capability over wide bandwidth, and the best PAE from 2 to 24 GHz among all fully-integrated Si-based DPAs.

II. Circuit Design

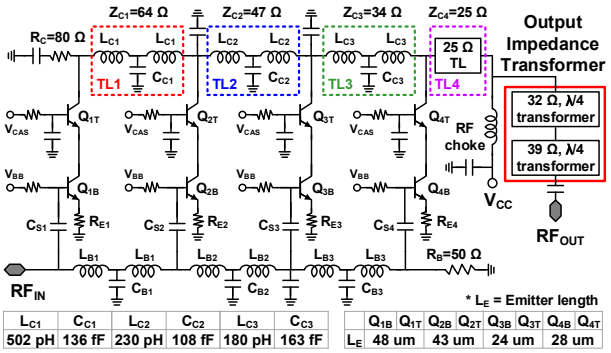
A. Circuit Schematic of the Proposed SiGe HBT NDPA

Fig. 1 describes a circuit schematic of the proposed SiGe HBT cascode NDPA. It consists of 50 Ω base TLs, a 4-stage SiGe HBT cascode core, collector TLs with their scaled Z_0, an on-chip RF choke, and a compact, wideband two-section lumped element λ/4 impedance transformer. The non-uniform design scheme with a lower load of 25 Ω is adopted here, which leads to an increase in the number of active stages and/or total emitter area of SiGe HBT cascode, to achieve higher P_{out}. The base and collector TLs were realized using a symmetric inductor with a metal-insulator-metal (MIM) capacitor at its center-tap [6], for its compact size and high cut-off frequency (f_c). The Z_0 of the collector TLs was determined based on following equations [4]

$$G_{C1} = G_c = G_{opt,1} \quad (1)$$

$$G_{ci} = \frac{{G_{C1}}^2}{G_c + G_{C1}} + \sum_{k=2}^{i} G_{opt,k} \text{ where i = 2,3,4, …} \quad (2)$$

where $G_{opt,i}$ is the optimum conductance of *ith* SiGe HBT cascode stage, G_{Ci} is the characteristic conductance of *ith* collector TLs, and G_c is a dumping conductance terminated at the first collector TL. In order to meet the 23 dBm target P_{sat}, SiGe HBT cascode emitter lengths (L_E) from the first stage to



L_{C1}	C_{C1}	L_{C2}	C_{C2}	L_{C3}	C_{C3}
502 pH	136 fF	230 pH	108 fF	180 pH	163 fF

	Q_{1B}	Q_{1T}	Q_{2B}	Q_{2T}	Q_{3B}	Q_{3T}	Q_{4B}	Q_{4T}
L_E	48 um	43 um	24 um	28 um				

Fig. 1. Circuit schematic of the proposed SiGe HBT cascode NDPA. A table inset summarizes L and C values of lumped-element collector TLs (Z_{C1}–Z_{C4}).

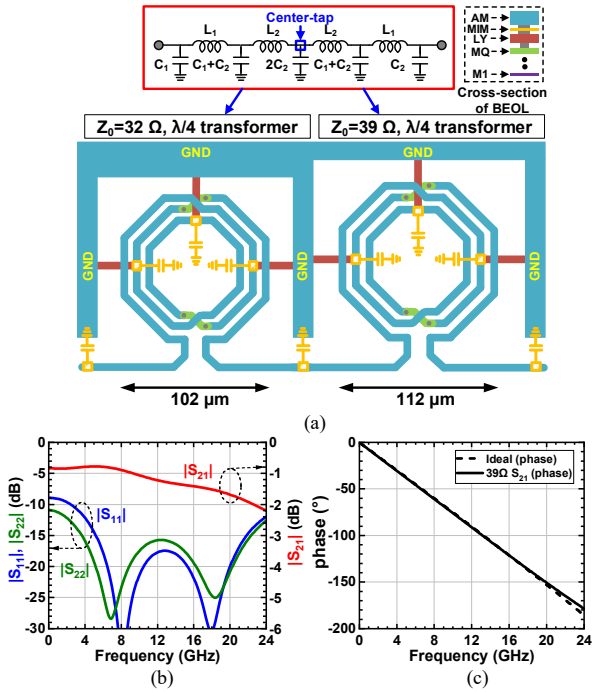


Fig. 2 (a) Top view of a lumped-element two-section output impedance transformer (Bottom) and its equivalent circuit (Top), (b) Simulated S-parameters of a two-section output impedance transformer and (c) Simulated phases of the 39 Ω λ/4 transformer (Solid) and ideal λ/4 transformer (Dashed).

the last stage were scaled from 48 to 28 μm, such that their corresponding optimum impedances ($R_{opt,i}$=1/$G_{opt,i}$) are 1/$G_{opt,1}$= 64 Ω, 1/$G_{opt,2}$ = 74 Ω, 1/$G_{opt,3}$ = 128 Ω, and 1/$G_{opt,4}$ = 96 Ω. Based on equation (2) and the obtained 1/$G_{opt,i}$, the calculated Z_0 values of the collector TLs (Z_{C1}–Z_{C4}) were 64, 47, 34, and 25 Ω, from the first stage to the last stage. A table in Fig. 1 summarizes the extracted values of inductances and capacitances of the collector TLs and L_E of each cascode core. The 50 Ω lumped-element base TLs are phase-aligned with their corresponding collector TLs. Input and output parasitic capacitances of each SiGe HBT cascode have been absorbed into their corresponding base and collector TLs. Dumping resistors R_B and R_C guarantee a flat gain response and good input/output return losses over wide bandwidth. A series base capacitive coupling (C_{Si}) and an emitter ballasting resistor (R_{Ei}) of a lower SiGe HBT (Q_{1B}–Q_{4B}) in a cascode further extend the

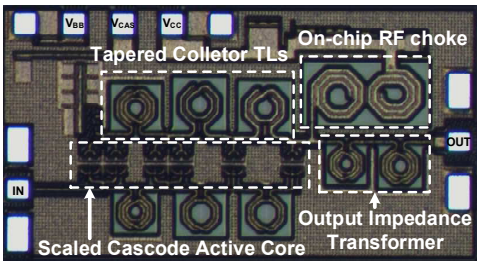


Fig. 3. Chip microphotograph of the 2-24 GHz SiGe HBT cascode NDPA.

BW of the NDPA. A RF choke is implemented by on-chip inductors with bypass capacitors.

B. Two-Section Lumped-Element λ/4 Impedance Transformer

A multi-section λ/4 impedance transformer is useful for wideband impedance conversion, but it is too bulky to be integrated on the present NDPA. A lumped element λ/4 impedance transformer is popular for its compact size, but BW is severely limited by its low f_c. To resolve the BW limitation while leveraging its compactness, a novel two-section lumped-element λ/4 output impedance transformer is proposed. Fig. 2 (a) shows a top view of the two-section lumped element output impedance transformer and its equivalent circuit. It consists of 39 and 32 Ω λ/4 transformers which are obtained based on Chebyshev design coefficients [7] to maximize the BW. The central idea is to divide a single 3 turn symmetric inductor into four-section π-networks, each symmetrical with respect to its center tap, by embedding the MIM capacitors at proper places, as highlighted in Fig. 2 (a). With this simple but novel layout scheme, two π-networks (C_1-L_1-C_1 and C_2-L_2-C_2) with a very high f_c now form a quasi-λ/4 transformer. A key design parameter of the proposed lumped element λ/4 transformer is the ratio between L_1 and L_2 in the symmetric inductor. With EM simulation using EMX® and a multiport inductor extraction method [8], an extracted L_1/L_2 ratio is 1.5 for the 39 Ω lumped element λ/4 transformer. Once this ratio is known, C_1 and C_2 are obtained based on the image parameter method [7]

$$Z_{i\pi} = \frac{Z_0}{\sqrt{1-(\frac{f}{f_c})^2}} \; where \; Z_0 = \sqrt{\frac{L}{2C}} \; and \; f_c = \frac{1}{\pi\sqrt{2LC}} \quad (3)$$

$$\varphi = \frac{180}{\pi} \cdot imag\left[ln\left(1 - 2\left(\frac{f}{f_c}\right)^2 + 2\frac{f}{f_c}\sqrt{\left(\frac{f}{f_c}\right)^2 - 1}\right)\right] \quad (4)$$

where $Z_{i\pi}$ and φ are an image impedance and a phase of a π-network. Using the above equations and a condition on total phase of 45 degrees for the two π-networks, the extracted L_1/L_2 and C_1/C_2 of the 39 Ω lumped element λ/4 transformer are 240/160 pH and 79/53 fF, respectively. An identical design procedure was adopted for the 32 Ω λ/4 transformer.

Simulated *S*-parameters of the proposed two-section lumped-element output impedance transformer are plotted in Fig. 2 (b)-(c). An insertion loss lower than 2.2 dB and return losses higher than 9 dB were obtained from DC to 24 GHz. Simulated phase response of the 39 Ω λ/4 impedance transformer is 89.7 degrees at 12 GHz, and its phase deviation from the ideal TL is less than 7 degrees at 24 GHz, thus

Table 1. Comparison with state-of-the-art Si-based Distributed Power Amplifiers.

Reference	Technology	Power Cell	Topology	Supply (V)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	3dB P_{sat} BW (GHz)	PAE (%)	External Bias-tee	Area (mm^2)
[2] JSSC'2019	45-nm CMOS SOI	4-stack	Uniform	6.6	23.0	21.5	20.8	DC–70	6.8–13.4	No	0.31**
[3] IMS'2018	45-nm CMOS SOI	4-stack	Uniform	4.4	17.1	21	18.2*	1–17	12.2–19.0	Yes	1.14
[9] TMTT'2017	130-nm CMOS Bulk	4-stack	Uniform	3.5	10.0	18.0*	15.0*	2*–13*	9.0–15.0*	Yes	0.83
[10] MWCL'2017	180-nm CMOS Bulk	Cascode	Tapered output	2.8	11.9	16.7	14.5	2–21*	6.2–16.0	Yes	1.70
[11] JSSC'2016	130-nm SiGe BiCMOS	Cascode	Supply scaling	2.7–4.0	12.0	17.0	14.9	15–85	7.0*–12.6	No	1.51
[12] TMTT'2011	130-nm SiGe BiCMOS	Cascode	Stage scaling	3.0	10.0	17.5†	16.7†	DC–77	6.3*–13.2	Yes	2.18
This work	**130-nm SiGe BiCMOS**	**Cascode**	**Non-uniform**	**3.6**	**11.2**	**21.3**	**19.0**	**2–24**	**12.2–21.7**	**No**	**0.77****

* Estimated from plots, ** Core area, †Pseudodifferential architecture.

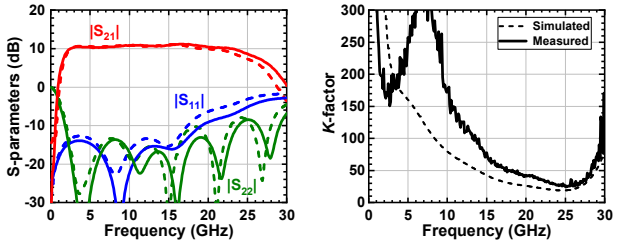


Fig. 4. Measured (solid) and simulated (dashed) (a) *S*-parameters and (b) *K*-factor.

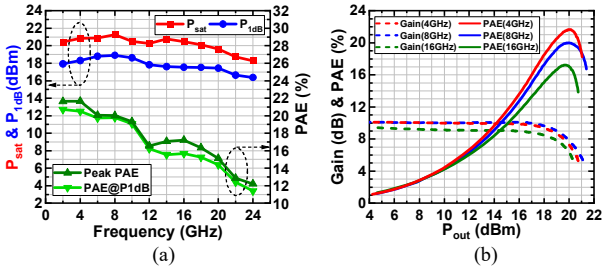


Fig. 5. Measured (a) P_{sat}, P_{1dB}, and PAE with frequency sweep and (b) Power gain and PAE with P_{out} sweep at 4, 8, and 16 GHz.

demonstrating that the proposed design method is feasible for realizing a compact, highly efficient, and broadband multi-section λ/4 impedance transformer.

III. Measurement

The proposed SiGe HBT cascode NDPA was implemented in GlobalFoundries 130-nm 8HP SiGe BiCMOS technology, which features a peak f_T/f_{max} of 220/280 GHz and BV_{CEO}/BV_{CBO} of 1.8/6.0 V. A chip microphotograph of the fabricated NDPA is shown in Fig. 3 and its core area is 1.26 x 0.61 mm^2. On-wafer measurements were performed using the on-chip integrated RF choke. A quiescent current of the NDPA was 23 mA at V_{CC} of 3.6 V, with V_{BB}/V_{CAS} of 0.87/1.90 V.

Fig. 4 (a) shows the simulated and measured *S*-parameters of the SiGe HBT cascode NDPA. A close match between the two is observed. The measured peak gain is 11.2 dB at 16.7 GHz, with a 3 dB BW of 1.8–25.5 GHz. Input and output return losses are higher than 10 dB from DC to 19.2 GHz, and from 1.9 to 23.8 GHz, respectively. Fig. 4 (b) shows the measured stability *K*-factor, higher than 24.6 across the entire BW.

Fig. 5 (a) shows measured results of P_{sat}, 1-dB gain compressed P_{out} (P_{1dB}), peak PAE, and PAE at P_{1dB}. Peak P_{sat}/P_{1dB} and PAE are 21.3/19.0 dBm at 8 GHz, and 21.7% at 4 GHz, respectively. The 3 dB P_{sat} and P_{1dB} BW range from 2 to 24 GHz and the peak PAE is still higher than 12.2% across that

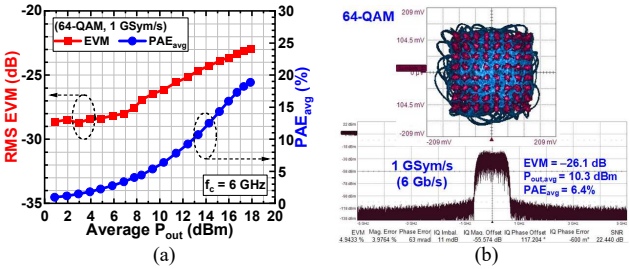


Fig. 6. Measured modulation test for a 1 GSym/s 64-QAM modulated signal at 6 GHz carrier frequency. (a) EVM (Red; Rectangle) and PAE_{avg} (Blue; Circle) over $P_{out,avg}$ sweep, (b) IQ constellation and spectrum at $P_{out,avg}$ of 10.3 dBm.

spectrum. Fig. 5 (b) shows the measured power gain and PAE over P_{out} sweep at 4, 8, and 16 GHz. The peak PAE is 17.2% at 16 GHz, which demonstrates the broadband optimum power matching capability of the proposed SiGe HBT cascode NDPA.

Modulation tests were performed using a Tektronix arbitrary waveform generator and a Teledyne-Lecroy LabMaster 10-100Zi-A oscilloscope. Fig. 6 (a) plotted RMS EVM and average PAE (PAE_{avg}) for a 1 GSym/s 64-QAM modulated signal at a 6 GHz carrier, vs. average P_{out} ($P_{out,avg}$). The $P_{out,avg}$ and PAE_{avg} satisfying EVM of –26 dB is 10.3 dBm and 6.4%, respectively. Fig. 6 (b) depicts the corresponding measured IQ constellation and power spectrum, indicating that the proposed NDPA supports 6 Gb/s in 64-QAM.

Table I summarizes state-of-the-art Si-based distributed PAs. The proposed SiGe HBT cascode NDPA achieves the best peak PAE performance among any Si-based DPAs from 2 to 24 GHz, with comparable and/or higher P_{sat} and P_{1dB}.

IV. Summary

This paper presents a broadband SiGe HBT cascode NDPA with a novel, compact two-section lumped-element λ/4 output impedance transformer. The optimum impedance matching capability at each SiGe HBT cascode, and low loss, wideband output impedance transformation at the NDPA load, enable achievement of the highest PAE of 12.2–21.7% from 2 to 24 GHz and the peak P_{sat} of 21.3 dBm, without any requirement for a bulky external bias-tee. Thus, the proposed SiGe HBT cascode NDPA offers a promising solution for a low cost, fully integrated wideband phased arrays.

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