A High-Power and High-Gain X-Band Si/SiGe/Si Heterojunction Bipolar Transistor

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***Abstract*—A double mesa-type Si/SiGe/Si (n-p-n) heterojunction bipolar transistor (HBT) with record output power and power gain at X-band (8.4 GHz) is demonstrated. The device exhibits collector breakdown voltage $\mathrm{BV_{CBO}}$ of more than 24 V and a maximum oscillation frequency $f_{\max}$ of 37 GHz. Under continuous-wave operation and class-AB biasing conditions, 24.2-dBm (263-mW) RF output power with concurrent gain of 6.9 dB is measured at the peak power-added efficiency (28.1%) from a single ten-emitter fingers (780-μm^2 emitter area) common-base HBT. The maximum RF output power achieved is as high as 26.3 dBm (430 mW in saturation) and the maximum collector efficiency is 36.9%. The low collector doping concentration together with the device layout result in negligible thermal effects across the transistor and greatly simplifies the large-signal modeling. The conventional Gummel–Poon model yields good agreement between the modeled and the measured dc characteristics and small-signal S-parameters. The accuracy of the model is further validated with the measured power performance of the SiGe power HBT at X-band. These results set a benchmark for power performance for SiGe-based HBTs and indicate promise for their implementation in efficient X-band power-amplifier circuits.**

***Index Terms*—Class AB, Gummel–Poon model, HBT, large-signal modeling, PAE, SiGe.**

I. Introduction

THE wireless communication market has experienced a substantial and rapid growth over the past few years and this growth is expected to continue within the foreseeable future. Future wireless communication units will require higher speed for faster data transmit rate, higher operation frequency to accommodate more channels and users, more functionality, light weight, low power consumption, and low cost. One of the solutions to meet these requirements is the concept of a complete wireless system on a chip. Integrating receiver, transmitter, and other processing circuits on a single chip cannot only reduce the volume and weight of a wireless communication unit significantly, but can also reap the cost benefit from volume production. To meet the high-speed and high-frequency requirements with the high level of integration for such a system-on-a-chip, the material system has to be well selected. Devices made from III–V materials exhibit high-speed characteristics and are suitable for high-frequency operation. However, the high-cost, low thermal conductivity, and poor mechanical strength of these materials have made them slightly inaccessible for high-level integration. On the other hand, the conventional low-cost Si-based devices, in which the poor frequency response is limited by intrinsic Si material properties, are not suitable for microwave applications. Fortunately, advances in SiGe-based devices made in recent years have reduced, or removed, the limitations posed by conventional Si technology. With the realization of both $f_{\max}$ and f_T over 100 GHz [1]–[3], SiGe-based devices have demonstrated their suitability for microwave and millimeter-wave applications. In addition, the SiGe-based material system, like Si, has the advantages of low cost, maturity of process technology, superior thermal conductivity, compatibility with CMOS technology, mechanical stability of substrate, and ease of high-level integration. In particular, compatibility with CMOS technology provides the opportunity for integration of RF/microwave modules with low-frequency circuitry and, hence, offers the feasibility of realization of a complete wireless system-on-a-chip.

A prevailing concern with the SiGe material system has been its potential to realize efficient power amplifiers, which are crucial circuit components of RF/microwave transmitters. Compared to field-effect transistors (FETs), bipolar junction transistors (BJTs) have a higher current-handling capability and promise higher voltage operation with better linearity. In addition, HBTs usually exhibit high gain even at low bias conditions, which is essential for class-AB and class-B operations. As a result, higher efficiency power amplifiers can be realized with these devices. However, since the demonstration of the highest $f_{\max}$ in an SiGe HBT [1], the investigation and development of SiGe microwave power HBTs have only received limited attention. Efforts on the microwave power application of SiGe-based HBTs have thus far been limited to L- [4]–[8], S- [9], [10] , and C-band [11] operations. The demand for higher channel capacity in wireless communication will naturally drive the wireless operation frequency to X-band and the reported performance characteristics of SiGe HBTs [12], [13] operating in this band are rather limited. A drawback in the development of X-band power SiGe HBTs, arising from the 6-dB/octave power gain reduction for small-signal operation and additional gain compression for large-signal

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operation, is that high output power can only be obtained at the cost of low power gain [12] and vice versa [13]. Nevertheless, a high output power with a concurrent high power gain (hence, power-added efficiency (PAE) at a certain class of operation) is always required for the implementation of efficient power amplifiers. To achieve this goal, the heterostructure and the device layout have to be well designed with considerations of thermal effects, breakdown voltage, $f_{\max}$, and output power. In this paper, we report the design, processing, and characterization of large-signal Si/SiGe/Si power HBTs, fabricated from heterostructures grown by one-step chemical vapor deposition (CVD). The devices demonstrate benchmark operation in terms of output power and concurrent power gain.

In what follows, the device design and fabrication will be detailed in Section II, followed by the description of dc, small-, and large-signal performance in Section III. The large-signal modeling of the device is presented in Section IV and conclusions are made in Section V.

II. Device Design and Fabrication

A. Vertical Heterostructure Design Consideration

The design of an Si/SiGe/Si power HBT includes vertical heterostructure design, focusing on the determination of thickness, composition, and doping concentration of each layer, and lateral layout design, which relates to the device active area, suppression of heat dissipation, and performance optimization. The design goal for a power HBT is to achieve high-frequency operation while maintaining high breakdown voltages and high current density for high output power. These requirements are interrelated and an optimal choice has to be made. Regardless of the fact that the design of base and emitter regions influences the HBT performance [14], the design of the collector region has a more profound effect on the overall performance of a power HBT [15]. Device performance characteristics such as collector–base avalanche breakdown voltage $(\mathrm{BV_{CBO}})$, maximum collector current density $(J_{C,\max})$, carrier total transit delay time from emitter to collector (τ_{EC}) and base–collector junction capacitance (C_{BC}) are mainly determined by collector thickness and doping concentration. Generally, lighter collector layer doping concentration and larger layer thickness result in higher breakdown voltage and lower maximum collector current density and vice versa. In particular, the maximum current density that the device can handle is very sensitive to the collector doping concentration, which has to be appropriately selected and well-controlled during growth. A high output power can be realized in two ways: either employing a higher breakdown voltage with a lower current density or employing a lower breakdown voltage with a higher current density. The former also offers the advantage of better output linearity. The latter, in its extreme, can result in excessive heat generation across the device with a very high and nonuniformly distributed junction temperature. Usually, the junction temperature in the center of the device is higher than that at the edges. The nonuniform temperature distribution deteriorates the power performance by rendering the center part of the device useless for high-power operation [16]. As a consequence, a high breakdown voltage with low current density, which can be obtained by designing a thick and lightly doped collector layer (limited by the Kirk effect), is preferred for power HBT design. The maximum collector thickness, however, should not exceed the collector-side depletion width of the base–collector junction under normal operating conditions, as the undepleted portion of the collector layer will lead to parasitic collector resistance. With respect to the frequency response, a thicker collector layer will result in a larger delay time when carriers are moving at their saturation velocity in the fully depleted collector layer, which constitutes the largest contribution to τ_{EC} in the case of a power HBT. If the cutoff frequency f_T is used to evaluate the transistor speed, a compromise has to be made between the requirements of breakdown voltage and speed. However, $f_{\max}$ is a better performance indicator than f_T in evaluating microwave power devices and, as shown in the following, a thick and fully depleted collector layer is usually favorable for large $f_{\max}$. The total transit time is expressed as

$$\tau_{\mathrm{EC}} = \tau_E + \tau_B + \tau_C + \tau_{\mathrm{CSCL}} \tag{1}$$

where

$$\begin{aligned}\tau_C =& C_{\mathrm{BC}}\left(\frac{kT}{qI_C} + R_E + R_C\right)\\ \approx& \frac{\varepsilon_{\mathrm{Si}} A_{\mathrm{BC}}}{W_C}\left(\frac{kT}{qI_C} + R_E + R_C\right)\end{aligned} \tag{2}$$

and

$$\tau_{\mathrm{CSCL}} = \frac{W_{\mathrm{CSCL}}}{2\upsilon_s} \approx \frac{W_C}{2\upsilon_s}. \tag{3}$$

The cutoff frequency

$$f_T = \frac{1}{2\pi\tau_{\mathrm{EC}}} \tag{4}$$

and

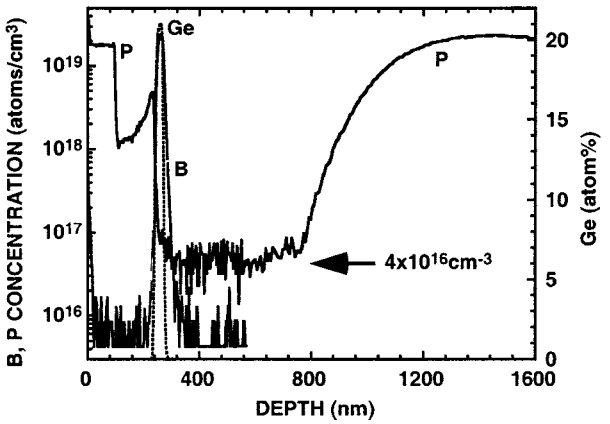
$$\begin{aligned}&f_{\max}\\ &= \left(\frac{f_T}{8\pi R_B C_{\mathrm{BC}}}\right)^{1/2}\\ &= \left(16\pi^2 R_B \varepsilon_{\mathrm{Si}} A_{\mathrm{BC}}\left(\frac{\tau_E+\tau_B}{W_C} + \frac{\varepsilon_{\mathrm{Si}} A_{\mathrm{BC}}}{W_C^2}\right.\right.\\ &\qquad \left.\left.\times\left(\frac{kT}{qI_C} + R_E + R_C\right) + \frac{1}{2\upsilon_s}\right)\right)^{-(1/2)}\end{aligned} \tag{5}$$

where W_C is the fully depleted collector thickness, A_{BC} is the base–collector junction area, and υ_s is the saturation velocity.

A collector doping concentration of 4×10^{16} cm^{-3} is chosen in this study with the objective of having a large breakdown voltage for a collector thickness of 500 nm. The heterostructure, as shown in Fig. 1(a), is grown on high-resistivity 4-in Si wafer in one step by CVD. The measured secondary ion mass spectroscopy (SIMS) profile of the device is shown in Fig. 1(b). The maximum boron concentration of 2.4×10^{19} cm^{-3} ensures a low base access/spreading resistance. The thickness of the sub-collector layer is chosen to be 1 μm, to achieve a smaller collector access/spreading resistance. The doping concentration in both the emitter cap layer and the sub-collector layer is $\sim 2\times$

Emitter cap	Si	n+	P	2×10^{19} cm^{-3}	100 nm
Emitter	Si	n	P	1×10^{18} cm^{-3}	100 nm
Spacer	$Si_{0.75}Ge_{0.25}$	i			5 nm
Base	$Si_{0.75}Ge_{0.25}$	p+	B	5×10^{19} cm^{-3}	20 nm
Spacer	$Si_{0.75}Ge_{0.25}$	i			5 nm
Collector	Si	n-	P	4×10^{16} cm^{-3}	500 nm
Sub-collector	Si	n+	P	2×10^{19} cm^{-3}	1000 nm
Substrate	Si(100)	p-		1×10^{12} cm^{-3}	540 μm

(a)



(b)

Fig. 1. (a) SiGe/Si double-heterostructure HBT design. (b) Measured SIMS profile in a CVD-grown device.

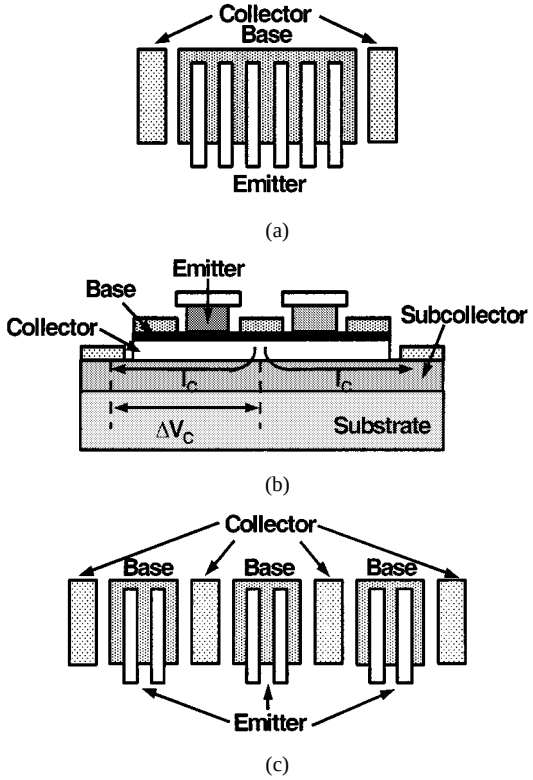


Fig. 2. Layout considerations for SiGe power HBT design. (a) Compact layout in which all emitter fingers are bound together. This layout leads to high temperature rise in the center area. (b) Significant voltage drop for many finger devices due to the high spreading collector resistance. (c) Noncompact layout with two emitter fingers bound together in a subcell. Collector spreading resistance is reduced and thermal effects are suppressed to an acceptable level.

10^{19} cm^{-3}, which is the upper limit that can be achieved with *in situ* doping during CVD growth.

B. Lateral Layout Design Consideration

Layout has a significant influence on the performance of microwave power HBTs, as the output power and, more importantly, the suppression of thermal effects is dependent on the lateral layout design. A multifinger emitter configuration is required for high current density, which also minimizes the lateral current crowding effect at high bias levels. The number of emitter fingers, finger width, finger length, and finger spacing need to be optimized for the multifinger configuration. A detailed discussion of the parameter selection rules can be found in [17]. A self-aligned base–emitter structure is widely used to reduce the base access resistance. The emitter finger spacing, which is the width of the base metal in a self-aligned structure, affects the total base resistance, as well as the base–collector junction capacitance $(C_{\rm BC})$. Increasing the finger spacing will increase $C_{\rm BC}$, which will adversely affect the $f_{\max}$, as expressed in (5). The advantage of a wide finger spacing is reduced thermal effects, which can significantly degrade the HBT power performance [17]. A compromise can be made by dividing all the emitter fingers into several subcells, in each of which several fingers with narrow finger spacing are bound together. This configuration can reduce thermal effects without increasing $C_{\rm BC}$, but with the extra advantage of decreased collector spreading resistance. The scheme is illustrated in Fig. 2. The emitter parameters need to be carefully chosen and, in our case, the finger width is 2 μm, finger length is 30 μm, the finger spacing is 2 μm, and there are two fingers in each subcell. The subcell spacing was designed to be 10 μm, leading to a temperature increase within the acceptable range. Collector metal is formed between subcells with an interdigitated configuration, in order to minimize the parasitic collector resistance. Our measurements have shown that, with the same number of fingers, an SiGe HBT with the layout of Fig. 2(c) exhibits better performance than that of Fig. 2(a).

C. Device Fabrication

Double mesa-type HBTs were fabricated with standard liftoff and etching techniques. The fabrication process is initiated by evaporating Cr/Au (500/2000 Å) on top of the wafers with standard lithography and liftoff techniques. The patterned emitter metals serve as the self-aligned mask for base exposure. To obtain a vertical sidewall, a 45°-rotated alignment was used for emitter metal mask [18]. To reduce the undercut, a combination of reactive ion etching (RIE) and wet etching with KOH is used to expose the SiGe base layer. This is followed by base metal $(\text{Pt/Au} = 200/1300\ \text{Å})$ deposition. The base mesa is next formed by RIE etching with photoresist protection

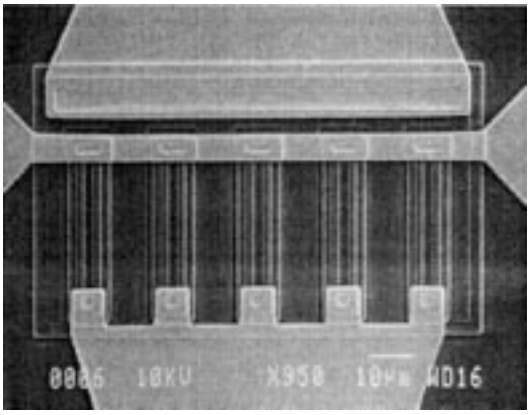


Fig. 3. Photomicrograph of a ten-finger common-base SiGe/Si HBT with an emitter area of $A_E = 780\ \mu\text{m}^2$ and interdigitated collector electrode metal.

of the emitter–base area. The sub-collector layer is exposed in this step and collector metal (Ti/Pt/Au = 300/200/2000 Å) is deposited. Individual devices are isolated by removing the extra sub-collector layer material around the devices while covering the active devices with a thick layer of photoresist. In this step the high-resistivity substrate is also exposed. Device passivation is achieved by the PECVD deposition of 1 μm SiO_2 at 200 °C. This layer also serves as the dielectric layer for interconnection metal deposition. Via-holes are then opened using RIE and the evaporation and liftoff of thick interconnection metals (Ti/Al/Ti/Au = 500/11 000/500/4000 Å) concludes the fabrication process. Fig. 3 shows the micrograph of a finished ten-finger common-base HBT. As shown in this figure, the emitter via-hole contacts increase the actual emitter area from $10 \times 2 \times 30\ \mu\text{m}^2$ to 780 μm^2.

III. Device Performance

A. DC and Small-Signal Performance

Common-base devices show better high-frequency performance than common-emitter devices with the same layout, mainly because the physical separation of input port (emitter) and output port (collector) for a common-base configuration leads to a smaller value of S_{12}. The following discussion will focus on the characteristics of ten-emitter-finger common-base devices with emitter area $A_E = 780\ \mu\text{m}^2$. If the undercut (estimated to be 0.25 μm) from wet etching is taken into account, the actual emitter area is 600 μm^2. The common-base current–voltage characteristics are shown in Fig. 4(a). From measurements on the same device in the common-emitter configuration, a dc current gain of 31 is obtained at $V_{\text{CE}} = 7$ V. The measured BV_{CEO} is over 8 V and BV_{CBO} is about 24 V. The high breakdown voltages are ascribed to the thick and lightly doped collector layer. The forward Gummel plot was also measured in common-emitter configuration and is shown in Fig. 4(b). The nonideal base current, which is frequently observed in Si/SiGe/Si n–p–n type HBTs, mainly arises from the fact that the base–emitter p–n junction does not coincide with the Si/SiGe heterojunction and can also be attributed to a small extent to the "cold" process induced unpassivated surface states. The outdiffused boron dopant atoms lead to a parasitic energy barrier near the emitter–base junction, as a result of which few electrons can be injected into the base layer at very low base–emitter bias values. The base current is increased and can be larger than the collector current at low base–emitter bias. Since it is usual to operate power HBTs at high base–emitter bias levels, the nonideal base current has negligible effect. An advantage arising from the small boron outdiffusion at the emitter side is a better base ohmic contact.

Small-signal S-parameters were measured in the frequency range of 2–40 GHz with an HP8510C network analyzer in order to investigate the RF characteristics of the device. Fig. 4(c) shows the power gain (U) and maximum stable gain (MSG)/maximum available gain (MAG) as a function of frequency at a bias point of $I_E = -77$ mA and $V_{\text{CB}} = 7$ V. The unilateral power gain U at 8.4 GHz is 12.6 dB. Higher power gain values at the operation frequency can be obtained if the base doping level is increased, and the emitter finger width and the undercut from wet etching are decreased. The measured $f_{\max}$ is 37 GHz and the gain drop of 12 dB/octave beyond 27 GHz is due to the second pole generated by the high base–collector junction capacitance.

B. Large-Signal Performance

The power performance of the ten-finger common-base SiGe HBT was tested on wafer at 8.4 GHz using a single-tone Focus Microwave load–pull system under class-AB operation in continuous wave (CW) mode. No special arrangement for heat dissipation was employed in the measurements. The device was biased at $V_{\text{EB}} = -1.176$ V and $V_{\text{CB}} = 8.1$ V in order to provide class-AB operation, and the source ($\Gamma_S = 0.64\angle 178°$) and load ($\Gamma_L = 0.71\angle 85°$) matching were optimized for maximum output power. The measured output power P_{out}, gain, PAE, and collector efficiency η_{col} are plotted as a function of input power P_{in} in Fig. 5. The measured linear gain is 10.9 dB. At 1- and 3-dB gain compression, the RF output power $P_{1\text{ dB}}$ and $P_{3\text{ dB}}$ are 21.5 (140 mW) and 23.5 dBm (224 mW), respectively. The maximum PAE, i.e., 28.1%, is achieved at 4-dB gain compression with associated RF output power of 24.2 dBm (263 mW). The largest RF output power (in saturation, gain drops to near unity) that the device can generate is as high as 26.3 dBm (430 mW, 0.55-mW/μm^2 power density) and the maximum collector efficiency is 36.9% for $P_{\text{in}} = 20.2$ dBm. These characteristics provide a benchmark for large-signal performance of SiGe HBTs operating in the X-band. Higher PAE could be obtained if the measurement is optimized for highest PAE. No thermal or electrical instability was observed under these operating conditions. The thermal stability is mainly ascribed to the high thermal conductivity of the silicon substrate.

IV. Large-Signal Modeling

An accurate large-signal model is essential for the design of nonlinear circuits, such as high-power amplifiers and oscillators. The conventional Gummel–Poon model serves as the basis of all modified versions, which may account for self-heating, collector delay, and breakdown. Incorporating thermal effects into the large-signal model significantly complicates the modeling procedure and the incorporation of thermal circuits often results in a convergence problem during the harmonic-balance

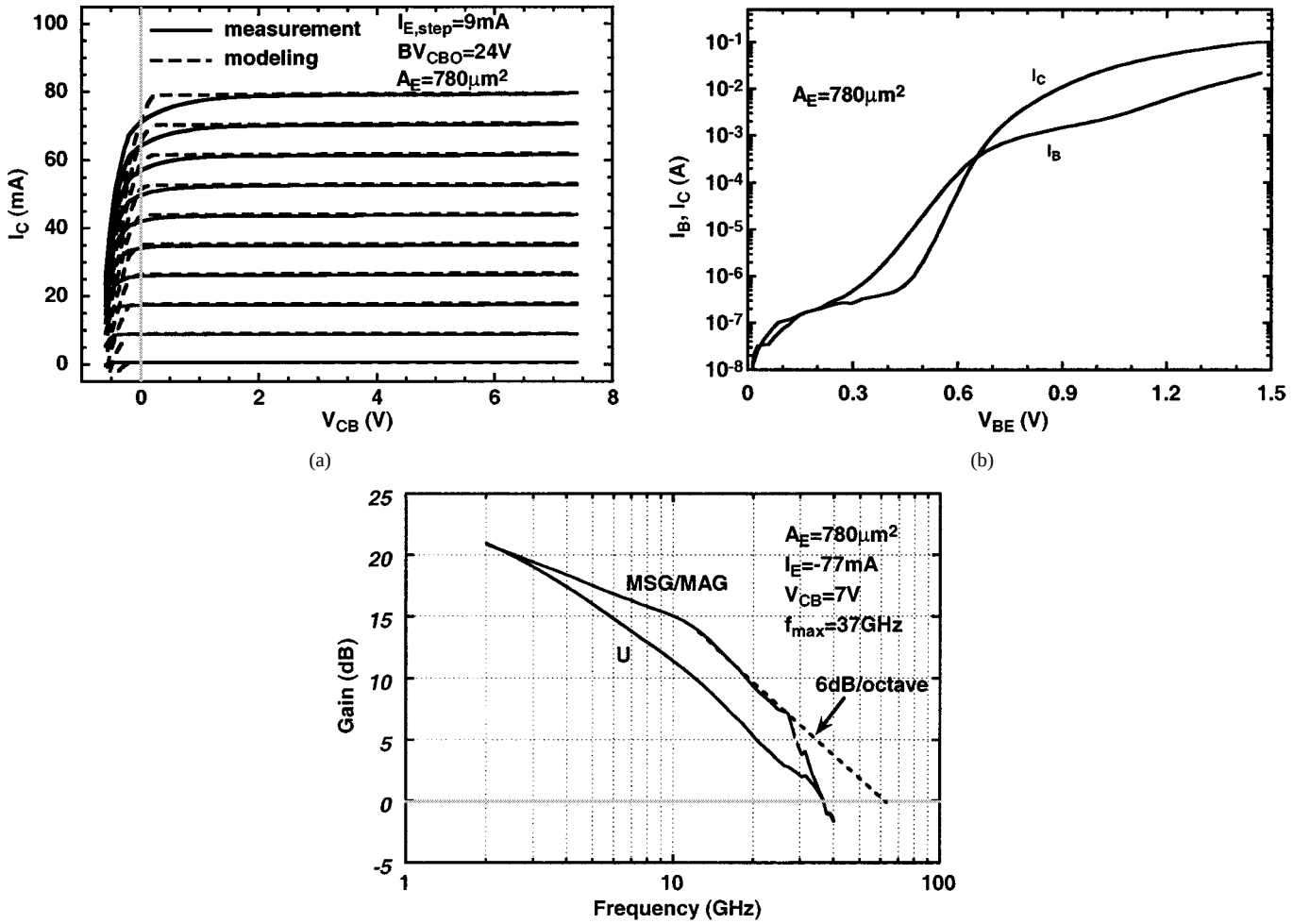


Fig. 4. (a) Measured and modeled dc current–voltage characteristics of ten-finger common-base SiGe/Si HBT with emitter area of $A_E = 780\ \mu\text{m}^2$. (b) Gummel plots measured in common-emitter configuration showing nonideal base current at low base–emitter bias. (c) Unilateral power gain U and MSG/MAG measured at $I_E = -77$ mA and $V_{\text{CB}} = 7$ V. The measured $f_{\max}$ is 37 GHz.

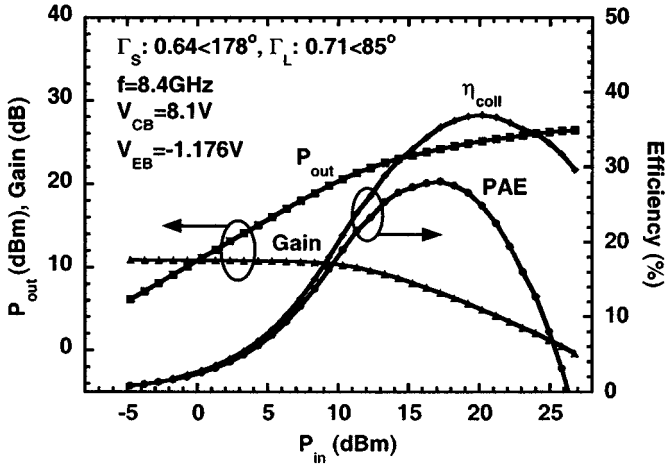
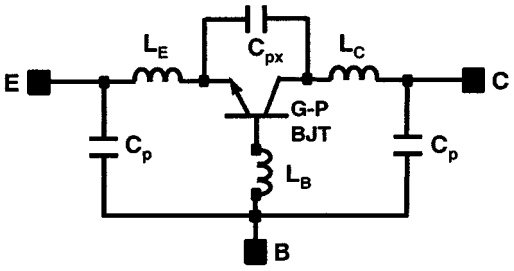


Fig. 5. Measured output power P_{out}, gain, PAE, and collector efficiency η_{coll} as a function of input power P_{in} at 8.4 GHz for a ten-finger ($A_E = 780\ \mu\text{m}^2$) common-base SiGe HBT biased for class-AB operation ($V_{\text{EB}} = -1.176$ V and $V_{\text{CB}} = 8.1$ V) under CW conditions. The source ($\Gamma_S = 0.64\angle 178°$) and load ($\Gamma_L = 0.71\angle 85°$) matching are optimized for high output power. The output power is 24.2 dBm with concurrent gain of 6.9 dB and 28.1% PAE. Maximum P_{out} is 26.3 dBm and maximum η_{coll} is 36.9%.

analysis. On the other hand, the conventional Gummel–Poon model is available in most commercial software, such as EES of LIBRA, ADS, and HSPICE. The suitability of this model for SiGe HBT large-signal modeling can facilitate power-amplifier design with SiGe HBTs. Since Si has very good thermal conductivity, the thermal effects of SiGe HBTs can be minimized with specially designed layout and heterostructure, as discussed in Section II. Our attempt in using the conventional Gummel–Poon model, which accounts for the Early and Kirk effects, but does not include thermal circuits, to model the ten-finger common-base power HBTs described in Section III has yielded good agreement between simulated and measured dc characteristics and small-signal S-parameters. In addition, the accuracy of the large-signal model has been validated with the measurement of HBT power performance, which shows the possibility of using this model for power-amplifier designs.

For modeling purposes, the dc and small-signal S-parameters of the fabricated ten-finger CB HBTs were measured in a wide range of bias values. From the measured forward and reverse Gummel plots, relevant dc model parameters (IS, ISE, ISC, IKF, IKR, BF, BR, NF, NE, NR, NC, NKF, RE, RB, RC) were first extracted using the optimization capabilities of HSPICE. The ac model parameters such as capacitances and transit times were



Gummel-Poon Large-Signal Model Parameters

Parameter	Value	Parameter	Value	Parameter	Value
IS	2.06e-12 A	RB	3 Ω	VJS	0.75 V
BF	52	RE	3.5 Ω	EG	1.11 eV
NF	1.09	RC	4.7 Ω	XTI	3
VAF	17 V	CJE	1e-12 F	FC	0.5
IKF	0.5 A	VJE	0.75 V	NK	0.5
ISE	2.02e-5 A	MJE	0.33	TNOM	300 K
NE	6.53	TF	5.9e-12 s	L_E	8e-12 H
BR	7.3e-6	CJC	1.29e-12 F	L_B	3e-11 H
NR	1.54	VJC	0.4 V	L_C	3e-11 H
ISC	1.25e-9 A	MJC	0.5	C_p	9e-14 F
NC	3.91	XCJC	0.35	C_{px}	3e-14 F

Fig. 6. Complete Gummel–Poon model for ten-emitter fingers common-base SiGe power HBT with values of the device parameters and parasitics used in the model.

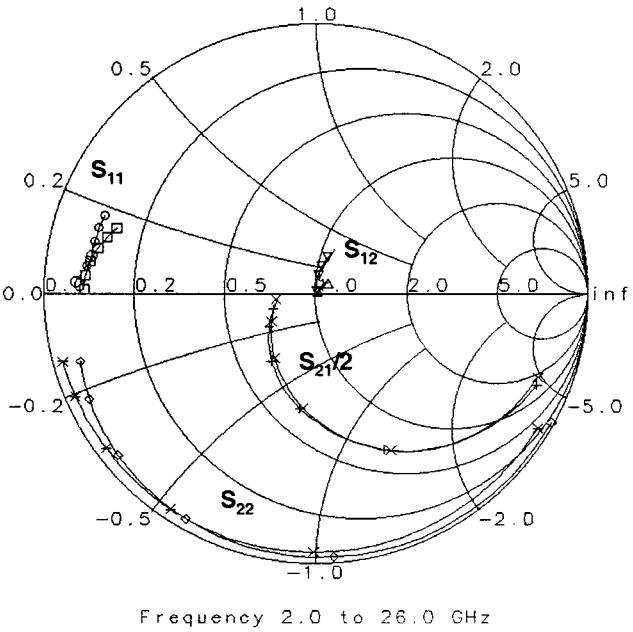


Fig. 7. Modeled and measured small-signal S-parameters of ten-finger common-base Si/SiGe/Si HBT at $I_E = -77$ mA and $V_{\rm CB} = 7$ V from 2 to 26 GHz.

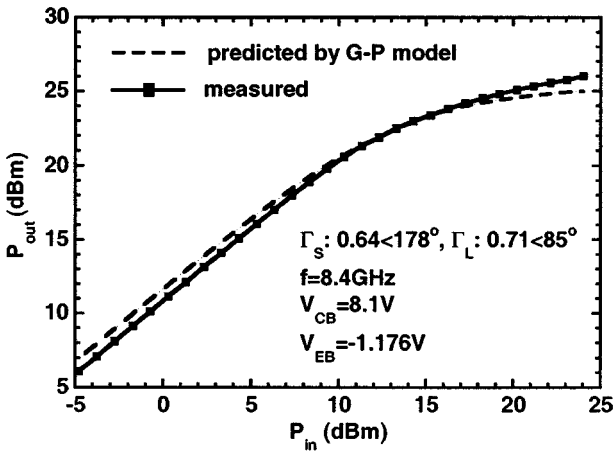


Fig. 8. Predicted from Gummel–Poon model and measured output power of ten-finger common-base Si/SiGe/Si HBT as a function of input power under the same source ($\Gamma_S = 0.64\angle 178°$) and load ($\Gamma_L = 0.71\angle 85°$) matching and same bias conditions ($V_{\rm EB} = -1.176$ V and $V_{\rm CB} = 8.1$ V).

next extracted following the procedures described by Pehlke *et al.* [19]. The parasitic elements, such as L_E, L_B, and L_C were also taken into account. The value of the capacitance of the interconnect pads was first extracted and this value was confirmed by S-parameter measurements of a dummy pad frame. These parameters, along with the dc model parameters, were further optimized in HP EES of LIBRA by fitting the measured S-parameters at various biases and in a frequency range of 2–26 GHz. The Gummel–Poon model with the values of the model parameters are listed in Fig. 6. From the modeling, it was found that the Early and Kirk effects are related to each other, particularly at high bias levels. For the HBT described in Section III, a large Early voltage is expected from its high base doping level (2.4×10^{19} cm^{-3}) and low collector doping level ($\sim 4 \times 10^{16}$ cm^{-3}) since the base-width modulation by the collector–base bias $V_{\rm CB}$ is very small. However, this point is only valid at low bias levels. When the HBT is biased at higher levels, the base push out due to Kirk effect will create an extended base region. The width of this extended base region can be much larger than the original SiGe base region, but the hole concentration in this region is very low and, hence, the modulation of this extended base by the bias is significant. As a result, at very high bias levels, which are typical of high-power operation, the Early voltage is significantly reduced. The reduction of Early voltage occurs as long as the Kirk effect takes place and the manifestation of the reduction is a steep rise of collector current at high $V_{\rm CE}$ bias values in a measured current–voltage curve in common-emitter configuration. This steep rise of collector current is a phenomenon that is different from the sudden increase of collector current due to breakdown. Considering the high bias levels in large-signal operation of the device, the S-parameter fitting is particularly optimized at relatively high bias points in this modeling. The modeled dc characteristics are also plotted in Fig. 4(a) along with the measured data for comparison. The agreement is good for almost the entire measurement range. The discrepancy between the model and measurement at the low $V_{\rm CB}$ and high I_C region is due to the simplicity of the Gummel–Poon model. Fig. 7 shows the measured and simulated small-signal S-parameters for the optimum operating point ($I_E = -77$ mA, $V_{\rm CB} = 7$ V). Again, fairly good agreement is observed and larger discrepancy for S_{11} is still due to the simplicity of the Gummel–Poon model. Since f_T, $f_{\max}$, and stability factors are directly derived from S-parameters, good agreements can also be expected for these parameters. To further validate the accuracy of the large-signal model, the power performance predicted by the model was compared with the measured power data under the same impedance matching and bias conditions. This is shown in Fig. 8 and again excellent agreement is achieved. Other power performance parameters, such as PAE and power gain, can also be accurately predicted

as they are directly related to output power $P_{\rm out}$. The fair accuracy and suitability of the conventional Gummel–Poon model is mainly ascribed to the device design, in which thermal effects are minimized with a noncompact layout and a lightly doped collector, and consideration of the Early and Kirk effects. In the future, modified Gummel–Poon models will be developed to take into account other effects associated with these SiGe-based HBTs.

V. Conclusion

A high-performance double mesa-structure X-band Si/SiGe/Si HBT has been designed, fabricated, characterized, and modeled. The common-base HBT (emitter area, $A_E = 780\ \mu\text{m}^2$) exhibited high breakdown voltages with BV_{CEO} larger than 8 V and BV_{CBO} of 24 V. An $f_{\max}$ of 37 GHz was derived from small-signal S-parameter measurements. The large-signal characteristics of the SiGe HBT operating at 8.4 GHz, biased in class-AB mode under CW operation, exhibit record power performance, with 24.2-dBm (263-mW) output power, associated 6.9-dB gain, and 28.1% PAE. The highest RF output power is 26.3 dBm (430 mW in saturation) and the maximum collector efficiency is 36.9%. A specially designed layout and heterostructure minimized thermal effects in the device and facilitated the large-signal modeling of the HBT. Taking the Kirk and Early effects into account, the conventional Gummel–Poon model demonstrated its accuracy and suitability for large-signal modeling of SiGe HBTs. The excellent device performance achieved in this study indicates the potential of implementing X-band power amplifiers with SiGe HBTs.

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