Analysis and Design of a Polar Digitally Modulated CMOS PA Based on Switched Constant-Current

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***Abstract*— Typical polar digital power amplifiers (DPAs) employ unit-cells operated in class-E or D^{-1}, denoting a switched-resistance operation which degrades linearity. Besides introducing higher demand on digital predistortion (DPD), it also requires extra quantization bits, impacting the overall efficiency and system complexity. To address this, the present work makes use of an optimized constant-current cascode unit-cell which is combined with reduced conduction angle to achieve linear and efficient operation, while minimizing the effort on DPD and/or calibration. A design strategy is developed which focuses on the cascode bias voltage and transistor relative dimensions as design parameters, allowing cascode efficiency optimization without compromising linearity or reliability. A single-ended polar switched constant-current DPA is implemented in 180−nm standard CMOS. Continuous-wave measurements performed at 800 MHz demonstrate an output power of 24 dBm with a PAE of 47%. The DPA dynamic behavior was tested with a 64-QAM signal with 10 MS/s, achieving an average PAE of 20.9% with a peak-to-average power ratio (PAPR) of 8.7 dB and adjacent-channel leakage ratio (ACLR) = 40.34 dB. These results demonstrate comparable performance with the prior art while using only 6-bits clocked at 100 MHz baseband sampling frequency.**

***Index Terms*— CMOS, current-mode (CM), linearity, radio-frequency integrated circuits, switched-mode power amplifier.**

I. Introduction

MOBILE device quest for lower cost, smaller form factors and longer battery lifetime is constantly pushing the performance and integration limits of CMOS RF transmitters (TXs) [1]. CMOS scaling has always accelerated digital processing, which favors the switched-mode transistor operation when compared to its linear capabilities, motivating the design of digitally assisted RF TXs to address such development demands [1]. The use of digital techniques in advanced CMOS nodes enables not only higher process robustness, flexibility, and integration but also lower power consumption by slashing the count of the blocks and enabling higher TX efficiency [2], [3]. The digital power amplifier (DPA) allows the digital baseband to be closer to the antenna, since it performs power modulation by individually turning on/off an array of sub-PAs, according to an amplitude code word (ACW).

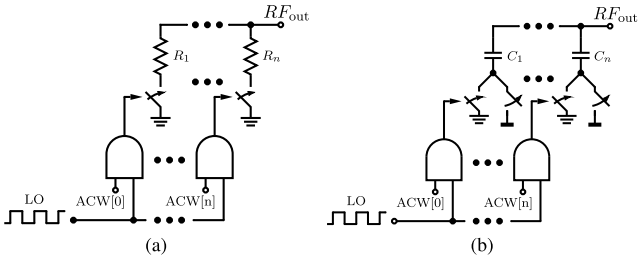

Fig. 1. (a) SR and (b) SCAP DPA unit-cell.

Triode-operated sub-PAs dominate the majority of CMOS implementations due to digital amenity and higher drain efficiency than their analog counterparts [4]–[11]. Hence, each unit-cell usually acts as a switched-resistance (SR) or switched-capacitor (SCAP) [4] (see Fig. 1), which enables efficient switched-mode class-E [5], F^{-1} [6], D [7], or D^{-1} [11]. Unfortunately, this introduces excessive AM-AM and AM-PM nonlinearities that are generally corrected by means of digital predistortion (DPD). Due to RF-DAC operation, the DPA's effective number of bits (ENOB) and sampling frequency need to be reasonably large to achieve adequate spectral replica suppression and reduce quantization noise [8], [9]. Thus, nonlinear DPAs must spare extra design bits to circumvent nonuniform quantization noise, which increases design complexity and power consumption [8], [10]. These impairments are even worse on the polar DPA since it experiences bandwidth expansion due to the nonlinear coordinate conversion. When aiming to reconstruct modulated signals with large instantaneous bandwidths (e.g., 10–40 MHz), polar DPA DPD blocks must run ≈10–20× higher than the modulated bandwidth, dissipating more power than the driver stages [9].

Less-intensive DPD operation is desirable since it can relax the up-sampling frequency, number of bits, and TX complexity, as well as leading to improved system efficiency [9], [11]. Hashemi *et al.* [12] proposed a class-E based unit-cell

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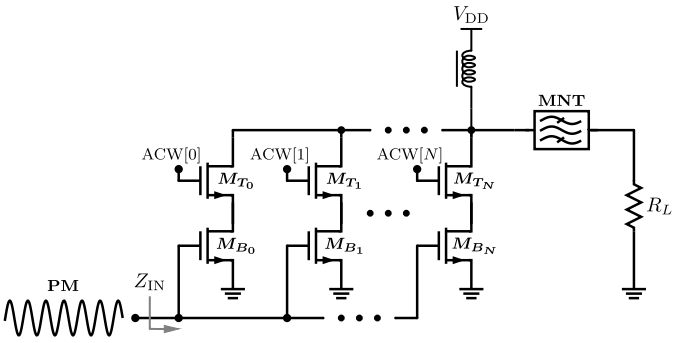


Fig. 2. Typical CM DPA implementations [8], [15], [16].

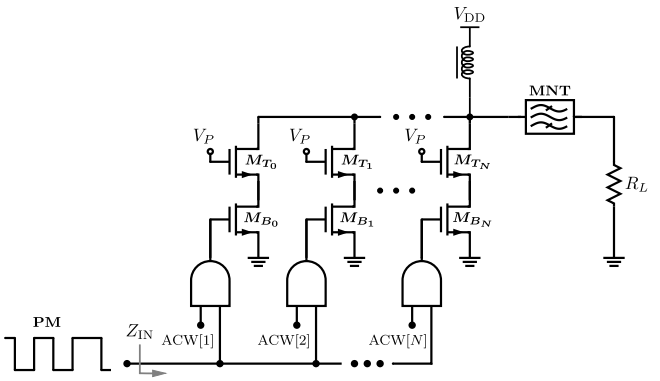


Fig. 3. Proposed fully digital CM DPA with constant input impedance to the PM driver and highly linear switched constant-current operation.

DPA with intrinsically linear behavior by combining nonlinear transistor width sizing, overdrive voltage control, and multiphase (MP) RF clocking. Park *et al.* [11] proposed an adaptive biasing scheme with a feedforward capacitor technique to mitigate the intrinsic AM-PM distortion of class-D^{-1} unit-cells. A DPA based on SCAP is presented in [13], which achieves linear behavior at the expense of lower output power (≈0 dBm). As an alternative, digitally assisted current-mode (CM) DPAs (see Fig. 2) can achieve superior linearity, lowering the requirements for TX calibration [8], [9], [14]–[16]. In comparison with SR and SCAP, the power stage is operated in constant transconductance (g_m), leading to linear response at the expense of efficiency. Besides, to generate adequate RF power, the output stage is generally cascoded/stacked [8], [14]–[16]. This introduces not only additional complexity in the process of efficiency optimization but also increased levels of nonlinearity [17], [18]. Zheng and Luong [16] addressed this problem with a constant-g_m cascode class-AB DPA, where the AM-AM/PM linearization was achieved by tuning the common-gate (CG) bias voltage with a replica feedback PA.

This article presents a fully digital polar CM-DPA with efficient operation aiming at reducing or eliminating DPD. To enable this, a constant-current squared-driven cascode power stage is investigated. A design strategy is developed to improve the typical cascode efficiency–power tradeoff by exploring higher efficiency loadlines without comprising linearity and reliability. This strategy will be studied on standard CMOS, with a circuit implementation on a 180-nm process node. This article is organized as follows. Section II describes the main idea behind the proposed architecture, while Section III discusses in detail the RF power stage efficiency, power-output capability and linearity. Section IV presents a single-ended (SE) circuit realization, and Section V presents the measurement results.

II. Proposed CM-DPA Architecture

To withstand large RF voltage swings, cascode stages are usually employed where the CG is a thick-gate device, while the common-source (CS) is a thin-gate nMOS for reduced power dissipation and higher gain [11]. In typical constant-g_m DPAs, both nMOS must be operated in saturation, which trades off RF power and reliability for efficiency [8], [15], [16]. Furthermore, to achieve a fully digital design, the CM-DPA should be driven by a constant amplitude square-wave, as proposed in this article and illustrated in Fig. 3. This removes the need for dedicated drivers and allows digital "AND" mixing as in SR- and SCAP-based designs [5], [16]. Likewise, this also guarantees that the input impedance, Z_{IN}, remains approximately constant with varying ACW, reducing the AM-PM distortion [16]. For a cascoded unit-cell DPA, the efficiency is given by

$$\eta_D = \eta_{\text{casc}} \times \eta_{\text{wv}} \tag{1}$$

where $\eta_{\text{casc}} = V_O / V_{\text{DD}}$ is the intrinsic cascode efficiency, V_O being the output voltage swing, and η_{wv} is the drain current–voltage waveform (wv) efficiency. For simplicity, class B-like matching conditions are considered. Fig. 4 illustrates in blue the dynamic loadlines of squared driven thick-gate nMOS transistors for 180- and 55-nm nodes, where the overdrive voltage is $V_{\text{OV}} = V_{\text{GS}} - V_T = V_{\text{DD}} - V_T$. From these, we can state that: 1) the ratio V_O / V_{DD} is nowhere close to unity and 2) the typical squared current waveform leads to high power dissipation given that $i_{\text{DS}}(t) \cdot v_{\text{DS}}(t) \gg 0$, reaching only $\eta_{\text{wv}} = 63.66\%$ when the duty-cycle (DT) is 50%. To counteract: 1) a reduction in V_{OV} allows for higher voltage swing (red loadlines), increasing efficiency by $\eta_{\text{incr}} = 18\%$ ($V_{\text{GS}} = 2.0$ V) and $\eta_{\text{incr}} = 16\%$ ($V_{\text{GS}} = 1.5$ V) at the expense of power-output capability reduction of $\simeq 2$. As for the 2), the conduction angle can be reduced to increase η_{wv} without significant impact on the power-output capability when compared to class-B operation [19]. Therefore, to tackle the cascode efficiency–power tradeoff, we propose to explore loadlines with higher efficiency by combining reduced conduction angle and lower saturation voltages. Contrary to a single nMOS scenario, it will be demonstrated that the cascode sub-PA can effectively operate with lower saturation voltages without comprising RF power and reliability. This operation region can be achieved by either: 1) reducing the CS V_{OV} voltage or 2) appropriately selecting V_P and CG–CS width ratio W_T / W_B. The former is not practical since it would require an extra voltage domain and higher design complexity; therefore, the latter is pursued in this article. Unlike in typical CM-DPAs, the approach taken here allows the CS to be operated in either point of the I–V loadline, considering that the CG is used to sustain the constant-current operation. Hence, this degree of freedom is

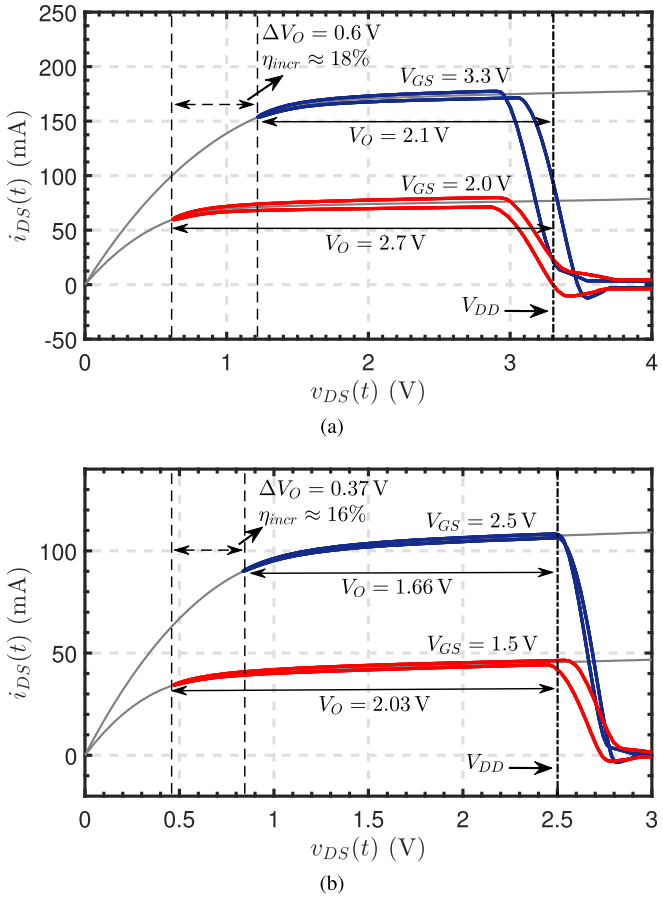


Fig. 4. Dynamic $i_{\mathrm{DS}}(t)$ versus $v_{\mathrm{DS}}(t)$ CM-DPA loadlines trajectories using class B-like matching conditions (all harmonics short-circuited) plotted in output characteristics of thick-gate nMOS with two different (over) drive input voltages. (a) CMOS 180-nm node. (b) CMOS 55-nm technology.

used to optimize the cascode efficiency–power tradeoff. The RF power supply is 3.5 V to achieve a reasonable tradeoff between output power, impedance transformation ratio, and RF voltage stress [20].

III. Design of Cascode CM Unit-Cell: Efficiency, Power-Output Capability and Linearity

To predict the theoretical efficiency and power-output capability of the CM-DPA, a simple, yet reasonably accurate model will be presented. Afterward, switched-mode capacitive dynamic power dissipation is discussed and its impact minimized. Phase and amplitude linearity are analyzed and the impact of channel length modulation (CLM) is assessed, demonstrating highly linear behavior. Furthermore, we also verify that the impact of nonlinear parasitic capacitors in the overall linearity is negligible. Finally, reduced DT is combined to provide higher efficiency.

A. Efficiency and Power-Output Capability

To provide a linear response, the cascode must be able to keep the constant-current operation and avoid crossing operating regions (e.g., triode to saturation or vice-versa) during full ACW sweep [16]. Hence, each PA subunit must

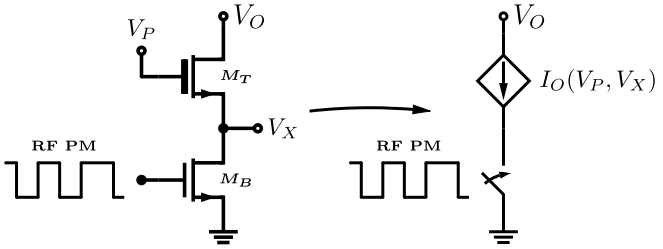


Fig. 5. Cascode cell acting as a highly efficient linear switched current-source.

be able to: 1) achieve low-power dissipation; 2) be able to deliver adequate RF power; and 3) provide rather linear AM-AM and AM-PM responses. Hypothetically, the cascode should behave as an ideal dependent current-source that is switched on–off by the RF PM signal, as depicted in Fig. 5. To guarantee the desired AM-AM profile, M_T and M_B can work either as: 1) current-current (CC), 2) current-resistance (CR), or 3) resistance-current (RC). The latter can be seen as a particular case of CC that occurs for large output power (PBO $\leq$ 6–7 dB), whereas at low output power, the cell goes back to CC. This has been widely discussed as a source of AM-PM nonlinearity [14], [16], thus being avoided here.

Since M_T and M_B can operate either in triode (r_{ON}) or saturation (g_m) modes, a simple model is developed to predict the RF output power and η_{casc} based on dc I–V curves. Hence, each nMOS will be modeled as

$$I_{\mathrm{DS}} = \begin{cases} 2 \cdot k' \cdot \dfrac{W}{L} \cdot V_{\mathrm{OV}}^{\alpha_1} \cdot V_{\mathrm{DS}}, & V_{\mathrm{DS}} \leq \dfrac{1}{2} V_{\mathrm{DS_{SAT}}} \\ k' \cdot \dfrac{W}{L} \cdot V_{\mathrm{OV}}^{\alpha_1}, & V_{\mathrm{DS}} \geq \dfrac{1}{2} V_{\mathrm{DS_{SAT}}} \end{cases} \tag{2}$$

where W and L are the width and the channel length, respectively; $k' = \mu \cdot C_{\mathrm{ox}}$; $V_{\mathrm{OV}} = V_{\mathrm{GS}} - V_T$, where V_T is the threshold voltage; and $V_{\mathrm{DS_{SAT}}} = C \cdot (V_{\mathrm{GS}} - V_T)^{\alpha_2}$ is the drain saturation voltage with C as a scaling constant. This simplified I–V model is derived from the Nth power law model [21]. Body effect is neglected since the CG is implemented with triple-well nMOS. Also, CG and CS channel lengths are $L_T = 340$ nm and $L_B = 180$ nm, $V_{T_T} \approx 0.65$ V and $V_{T_B} \approx 0.5$ V. The parameter k' assumes different values for thin and thick devices. Considering $L_{T,B} = L_{\min}$, we will represent $k'_T = \rho \cdot k'_B$, where $\rho \sim 0.35$. Constant α_1 assumes near unitary values for short-channel MOSFETs, while $C_{T,B}$ and $\alpha_{2_{T,B}}$ are fit as proposed in [21] to model triode-saturation transition.

When the cascode operates in CR, I_O is imposed by the CG and is equal to $I_{\mathrm{DS}_T} = (W_T/L_B) \cdot \rho \cdot k'_B \cdot (V_P - V_X - V_{T_T})$. The $V_{X_{\mathrm{CR}}}$ value is simply given by $I_O \cdot r_{\mathrm{ON}_B}$, hence

$$V_{X_{\mathrm{CR}}} = \frac{(V_P - V_{T_B}) \cdot \rho \cdot (W_T/W_B) \cdot V_{\mathrm{DS_{SAT}}_B}}{2 \cdot V_{\mathrm{OV}_B} + \rho \cdot (W_T/W_B) \cdot V_{\mathrm{DS_{SAT}}_B}} \tag{3}$$

and consequently the maximum RF output voltage is given by $V_O = V_{\mathrm{DD}} - (V_{X_{\mathrm{CR}}} + V_{\mathrm{DS_{SAT}}_T})$. As for the CC condition, the output current is obtained by solving $I_{\mathrm{DS}_T} = I_{\mathrm{DS}_B}$, which results in

$$V_{X_{\mathrm{CC}}} = V_P - V_T - \frac{W_B \cdot V_{\mathrm{OV}_B}}{\rho \cdot W_T} \tag{4}$$

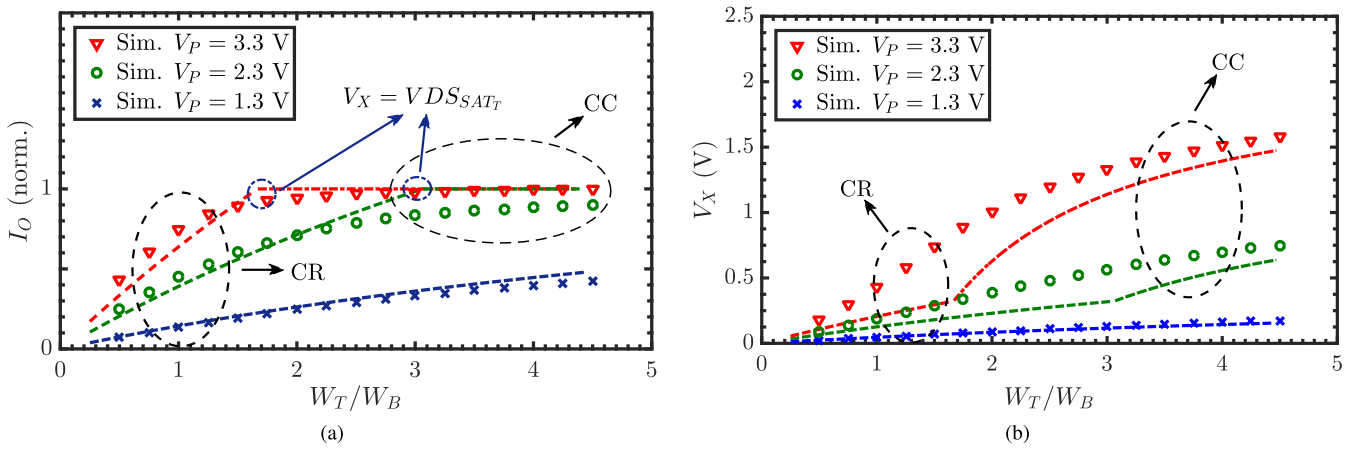


Fig. 6. (a) Cascode I_O current. (b) Cascode V_X node voltage. Markers denote BSIM results, while (---) illustrates the adopted model estimates for CR behavior and (---) CC operation.

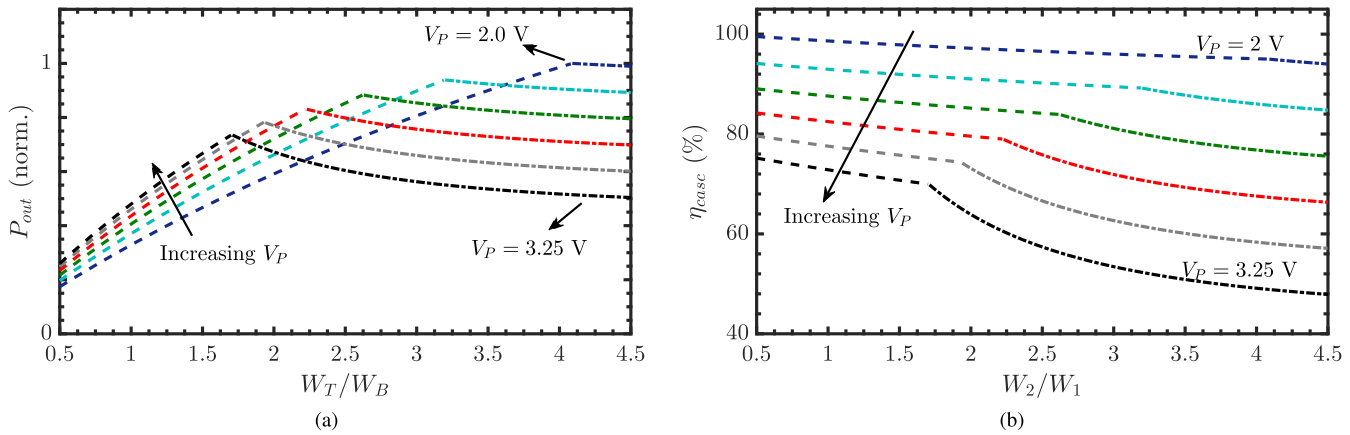


Fig. 7. (a) Normalized peak output power. (b) Peak DPA efficiency as a function of W_T/W_B and several different V_P values. Both CR and CC operation modes are denoted by (---) and (---) lines, respectively.

while the peak output voltage is $V_O = V_{\rm DD} - (V_{\rm DS_{SAT_T}} + V_{\rm DS_{SAT_B}})$. The output current is

$$I_O = I_{{\rm DS}_{T,B}} = \frac{W_T}{L_{\rm min}} \cdot \rho \cdot k'_B \cdot (V_P - V_{X_{\rm CC}} - V_{T_T}). \quad (5)$$

To verify the validity of this simplified I–V model, Fig. 6 illustrates I_O and V_X (both normalized) between the calculated values (dashed curves) and simulated (BSIM) models (markers) for three different V_P values. As expected, the largest deviations occur near the soft triode-saturation transition. Nevertheless, the model provides useful guidance to assess the impact of V_P and W_T/W_B on DPA performance.

Intrinsic cascode efficiency and output power, $P_{\rm out}$, are calculated and plotted in Fig. 7 as a function of W_T/W_B for several V_P values. On one hand, high V_P and large W_T/W_B lead to high I_O values (due to CC regime), while V_O decreases substantially leading to deteriorated $\eta_{\rm casc}$. On the other hand, relatively low values of V_P and large width ratios lead to CR operation where achievable output power is greater than in CC due to increased $V_O \cdot I_O$. Moreover, efficiency enhancement of $\eta_{\rm incr} \approx$ 20–30 % are easily achievable. However, one must ensure that V_P is neither high (e.g., $V_P \sim 3.3$ V) or low ($V_P \sim 1$ V) enough to stress the gate-drain oxide in excess. For this, the maximum $V_{\rm DG}$ should not exceed $2 \cdot V_{\rm DD_{nom}}$ [5], [17], which is 1.8 and 3.3 V for thin and thick nMOS

$$V_{\rm DG} = \begin{cases} V_{\rm DD} + V_O - V_P \le 6.6 \text{ V}, & \text{thick-gate} \\ V_P - V_{T_T} \le 3.6 \text{ V}, & \text{thin-gate.} \end{cases} \quad (6)$$

According to (6), selecting $V_P = 2.0$ V and $W_T/W_B = 2.5$ results in a maximum voltage of $V_{{\rm DG}_T} \approx 4.1$ V and $V_{{\rm GD}_B} \approx 1.5$ V, which indicates perfectly safe operation given that these values are both below 60% of maximum $\Delta V_{\rm DG}$, while delivering $\eta_{\rm casc} \approx 72\%$ and a reasonable cell power-output capability. Thus, operating in CR mode with $V_P \approx 2$ V and $W_K/W_B \approx 2.5$ yields a good tradeoff between power-output capability, efficiency and MOSFET reliability. Interestingly, as W_T/W_B assumes high values (i.e., ≥ 3.5), the cell theoretically delivers both high efficiency and output power in CR mode. Note that at $W_T/W_B \ge 4$, the cell enters in CC mode with considerably good output power and reasonably high efficiency ($\eta_{\rm casc}$ only decreases $\approx$ 3–4% from $W_T/W_B = 2.5$ to $W_T/W_B = 4.5$).

B. Dynamic Capacitive Power Dissipation

As in a typical CM operation, the DPA output capacitance is absorbed into the matching network [20]. However, the

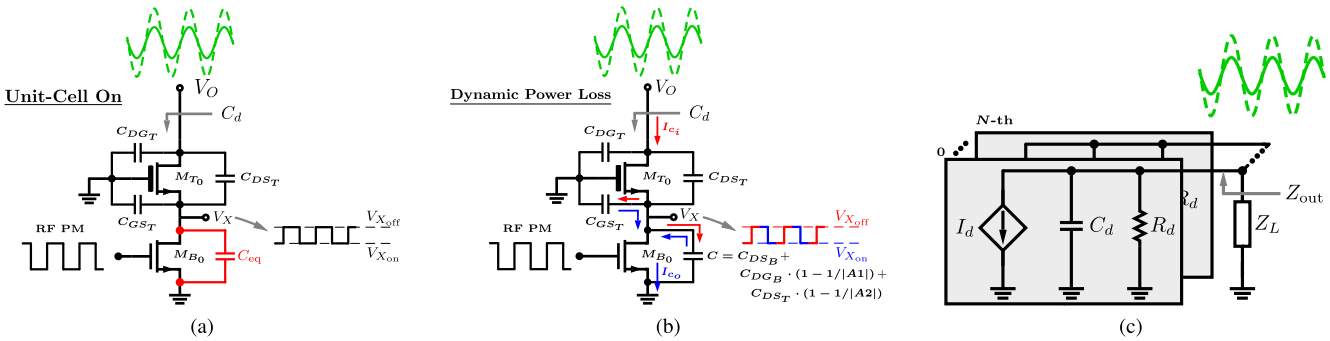


Fig. 8. (a) Parasitic capacitances and main node voltages when the unit-cell is switching. (b) Illustration of the charge/discharge process of parasitic capacitances that are not resonated by the output matching network. (c) Equivalent linear model of the proposed cascode CM-DPA.

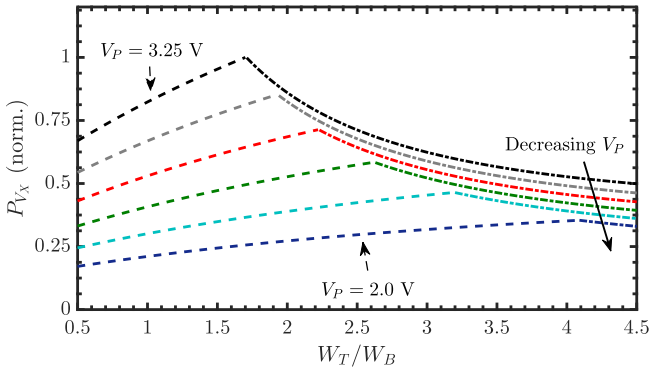


Fig. 9. P_{V_X} as a function of W_T/W_B for several V_P values. Curve (---) illustrates CR behavior and (---) the CC operation.

cascode structure has parasitic capacitors that cannot resonate with the output network since their voltage levels are being forced upon. Fig. 8(a) and (b) illustrates V_X node voltage variation as the cascode toggles on/off, resulting in a square-like waveform. When the cascode is off, the output matching network charges V_X node through M_{T_0} up to $V_P - V_{T_T}$. However, as it turns on, V_X is rapidly adjusted to allow for constant-current operation. Red and blue arrows indicate the charge-discharge current path of V_X node, indicating that the energy accumulated in each RF cycle is being dissipated by M_{B_0}. This effect has already been identified as a non-negligible source of efficiency degradation in switched-mode cascode PAs [17]. Even though its impact on CM operation is diminished, it must not be overlooked [18]. Although an analytical closed-form solution does not exist [17], we will assume the following expression for the power dissipation, P_{V_X}:

$$P_{V_X} \approx \frac{1}{2} \cdot (C_{M_T} + C_{M_B}) \cdot f_{\mathrm{RF}} \cdot (V_P - V_{X_{\mathrm{ON}}} - V_{T_T})^2 \quad (7)$$

where $C_{M_T} = (W_T/W_B) \cdot C_{M_B}$[1] and C_{M_B} are the contributions of M_T and M_B, respectively, and $V_{X_{\mathrm{ON}}}$ is either given in (3) or (4), allowing us to estimate the relative impact of V_P and W_T/W_B. Fig. 9 portrays the evolution of P_{V_X} as a function of W_T/W_B for several V_P voltages. As V_P is set to lower values, the power loss is reduced, while W_T/W_B increments/decrements the power loss in CR/CC mode. Based on this, choosing low V_P voltage will result in lower power dissipation, particularly for CR mode. Hence, $V_P \in [\ 1.8\text{–}2.5\ ]$ V enables W_T/W_B ratios above 2, allowing high η_{casc} and P_{out} while mitigating capacitor-induced dynamic power dissipation. Therefore, no extra silicon area is required based on the proposed CM-DPA operation [18].

[1]For simplicity, it is assumed that both transistors contribute equally to V_X parasitic capacitance.

C. Phase Linearity

DPA phase linearity can be impaired by various effects, namely, supply parasitic inductors [22], [23], layout/routing delay [6], [22] and input–output code-dependent impedances [8], [9], [11], [16], [24]. Parasitic supply inductance creates nonzero settling time at the power supply rails, which leads to variable delay as the current draw is time-varying [22], [23]. Its impact is more pronounced when using old process nodes, aiming for Watt-level P_{out} or amplifying high bandwidth signals, and it can be reduced by employing low inductance packaging or by integrating power management and digital TX on the same die/package [23], [25]. Due to DPA-segmented nature, RF routing lines and layout parasitics can produce cell to cell delays that result in PM distortion, this being mitigated by careful layout techniques and short routing traces [6], [22]. Code-dependent input impedance can be reduced to almost negligible levels by replacing class-B unit-cells with switched-mode sub-PAs, allowing for digital mixing before the output stage [5], [16].

As the DPA is modulating the output power, each unit-cell experiences time-varying voltage swing. This can cause parasitic capacitors to transit between operating regions, leading to ACW-dependent output capacitance, which in turn modulates the matching network and creates PM distortion [11]. The cascode unit-cell parasitic capacitances are shown in Fig. 8(a) and (b). Note that CG gate terminal is ac-grounded ($\Delta V_g \approx 0$). The total DPA output capacitance will depend on the weighted sum of the on–off cells, where the latter can be expressed as

$$C_d = \begin{cases} C_{\mathrm{DG}_T} + C_{\mathrm{DS}_T} /\!/ (C_{\mathrm{DS}_B} + C_{\mathrm{DG}_B} + C_{\mathrm{GS}_T}), & \mathrm{OFF} \\ C_{\mathrm{DG}_T} + C_{\mathrm{DS}_T} \cdot (1 - 1/|A_1|), & \mathrm{ON} \end{cases} \quad (8)$$

where $|A_1|$ is the gain from the cascode node, V_X, to V_O, $C_{\mathrm{DG}} = W \cdot C_{\mathrm{ov}}$ for either cutoff or saturation where C_{ov} is

the overlap capacitance and $C_{\rm DS}$[2] is the nonlinear drain-bulk junction capacitance that remains fairly constant regardless of $V_{\rm BS}$ up to triode region [26]. The total output capacitance, $C_{\rm out}$, is a combination of the on–off cells [see Fig. 8(c)] and is calculated as

$$C_{\rm out}({\rm ACW}) = {\rm ACW}\cdot C_{d_{\rm ON}} + ({\rm ACW}_{\rm max} - {\rm ACW})\cdot C_{d_{\rm OFF}} \quad (9)$$

where $C_{d_{\rm OFF}} \approx C_{{\rm DG}_T} + C_{{\rm DS}_T}$ considering relatively small W_T/W_B, $|A_1| = (I_{f_{1_u}}\cdot R_L\cdot {\rm ACW})/\Delta V_X$, where $\Delta V_X = V_{X_{\rm ON}} - V_{X_{\rm ON}}$ and $I_{f_{1_u}}$ is the unit-cell fundamental current. Thus

$$\begin{aligned} C_{\rm out}({\rm ACW}) &\approx C_{{\rm DG}_T}\cdot {\rm ACW}_{\rm max} \\ &\quad + C_{{\rm DS}_T}\cdot\left[{\rm ACW}_{\rm max} - \frac{{\rm ACW}\cdot\Delta V_X}{I_{f_{1_u}}\cdot R_L\cdot {\rm ACW}}\right] \\ &= C_{{\rm DG}_T}\cdot{\rm ACW}_{\rm max} + C_{{\rm DS}_T}\cdot{\rm ACW}_{\rm max}\cdot\left[1 - \frac{\Delta V_X}{I_{f_{1_u}}\cdot R_L}\right] \quad (10)\end{aligned}$$

which indicates that, on a first-order approach, $C_{\rm out}$ is constant regardless of power modulation. This remains accurate as long as the output resistance of the cascode stays high compared to R_L, leading to constant V_X voltage over ACW and the thin/thick-gate operated over constant region (cascode in either CR or CC). Simulation results indicate that $C_{\rm out}$ variation is $\leq 0.5\%$ for $W_T/W_B \in [1,4]$ and $V_P \in [1.6, 2.8]$ V over full ACW range.[3] Therefore, designing the DPA to operate in CR mode enables improved performance over typical CM designs without sacrificing PM linearity.

D. CLM

The CM DPA can be modeled by the linear time-invariant circuit illustrated in Fig. 8(c), where Z_L is the output load presented by the matching network at the fundamental harmonic. For simplicity, $I_d = I_{f_{1_u}}$ to represent only the fundamental tone, while R_d and C_d are the unit-cell output resistance and capacitance, respectively. Assuming $Z_L = R_L$ the output amplitude can be expressed by

$$V_O({\rm ACW}) = {\rm ACW}\cdot I_d\cdot\left(R_L /\!/ (R_d/{\rm ACW})\right) \quad (11)$$

indicating that as $R_d/{\rm ACW}$ becomes comparable with R_L, AM-AM distortion occurs [8], [27]. As transistors are shrinking in size, this effect is even more pronounced. One way to circumvent this is to adopt the cascode technique to increase output resistance. To assess the impact of CLM, we will the express the output resistance as $1/(\lambda\cdot I_d)$. Thick and thin devices are fit to $\lambda_T = 0.04$ and $\lambda_T = 0.13$ and, for $L \geq 250$ nm, λ is practically independent of $V_{\rm GS}$ [28]. The cascode output resistance R_d is given as follows:

$$R_d = \frac{1}{I_d}\cdot\left(\frac{1}{\lambda_T} + \frac{1}{\lambda_B} + \frac{1}{\lambda_T}\cdot\frac{1}{\lambda_B}\cdot\frac{g_{m_T}}{I_d}\right). \quad (12)$$

Fig. 10 shows us the theoretical AM-AM distortion based on (12), indicating that the soft triode-saturation transition will dominate the AM-AM linearity over CLM.

[2]For simplicity $C_{\rm GS}$ in cutoff will be assumed to be on the same order value of $C_{\rm DS}$ in saturation [26].

[3]Only nMOS intrinsic capacitors are considered, therefore $C_{\rm out}(ACW)$ impact will be even lower after layout parasitic capacitors are accounted for.

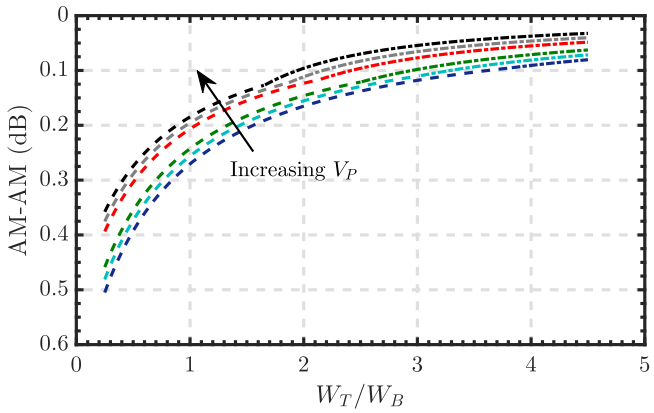
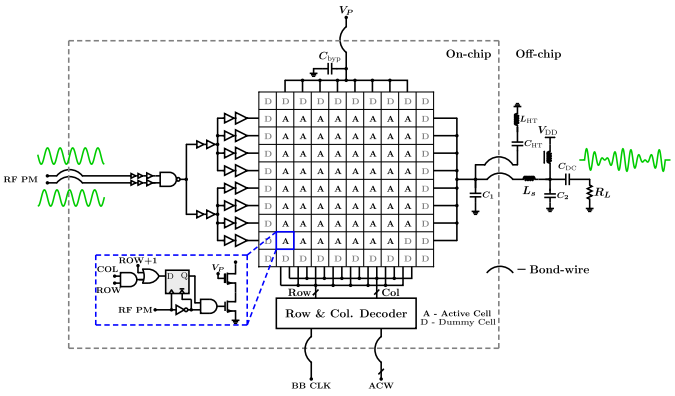


Fig. 10. Theoretical AM-AM distortion as a function of V_P and W_T/W_B (soft triode-saturation transition impact excluded).

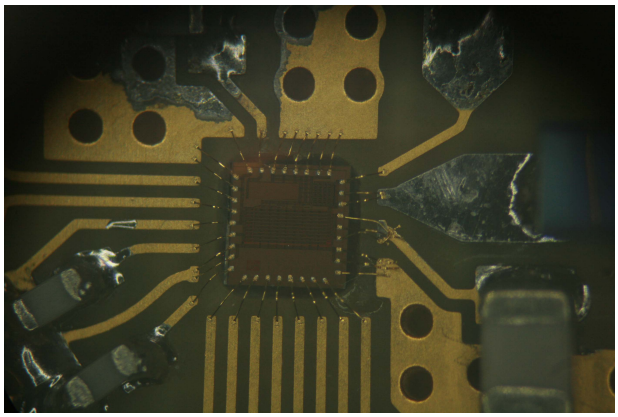
IV. Circuit Implementation

A proof-of-concept SE DPA was implemented and fabricated in 180-nm bulk CMOS to experimentally evaluate the proposed architecture. The IC measures 1550×1550 $\mu{\rm m}^2$ and the area is pad dominated due to a large number of IOs. Due to semi-manual bond-wire-related spacing constraints, only 34 IC pads are possible; thus, 10 are selected to provide a low-impedance analog ground connection for the cascode output stage, while $5+5$ are used for the digital supply rails.

The DPA unit-cell was designed to have $W_T/W_B = 2.5$ and $V_P = 2.0$ V as it provides a good tradeoff between power, linearity, efficiency and reliability. A fully thermometer code approach is used in this implementation and $W_{B_u} = 23$ μm. Fig. 11(a) shows the 6-bit AM resolution DPA floor plan. The DPA core is composed of 63 equally sized cells surrounded by dummy cells for improved process uniformity [5]. Each unit-cell has an AND–OR AM signal decoder, a time synchronizer flip-flop, RF buffer (inverter), and an AND gate acting as a digital mixer [5]. This implementation allows the use of the widespread row-column decoder approach, which guarantees monotonicity and reduces glitches on the AM-AM/PM characteristics, increasing the overall linearity. Also, the flip-flop helps to ensure on-chip AM-PM synchronization to enable wideband power modulation with reduced glitches [13]. Row, column, and binary-to-thermometer decoders are implemented through digital synthesis (RTL). Due to relatively high parasitics, which induce large surge currents on digital supplies rails, the analog and digital return paths are separated and united off-chip. For simplicity, DT = 25% is used since it can be easily generated on chip by driving an AND/NAND cell with quadrature PM signals. Thus, the quadrature RF PM signals are generated by driving a quadrature balun with the RF PM signal, while 50-Ω resistors are placed as near as possible to chip pads to avoid unwanted reflections. Afterward, the signal is squared and appropriately buffered to each row by a chain of inverters to guarantee uniform delay. To reduce the settling time on V_P, a $C_{\rm byp} = 200$ pF is used to ac ground all CG gates [29]. Note that on a differential implementation, such a capacitor would be dismissed [11]. All digital logic runs at $V_{\rm DD_{DIG}} = 1.8$ V while the DPA output is biased at $V_{\rm DD_{RF}} = 3.5$ V through an RF choke $L = 33$ nH.



(a)



(b)

Fig. 11. (a) SE circuit implementation of proposed CM-DPA. (b) Microphotograph of the IC bond-wired to the test PCB.

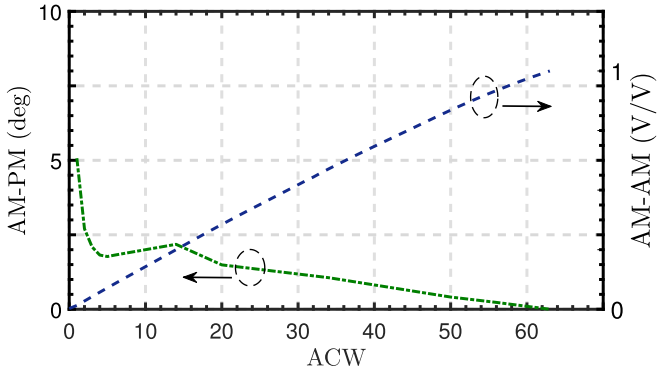
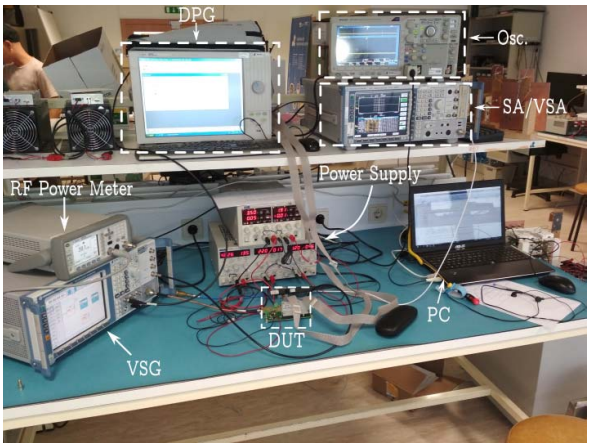
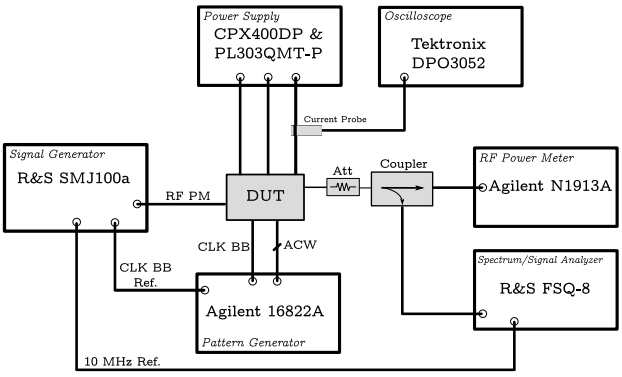


Fig. 12. DPA simulated AM-AM and AM-PM performance.

Due to their digitally intensive nature, DPAs provide enough flexibility to operate across wide frequency spans, being only limited by the output matching network. An RF frequency of 800 MHz is chosen to test the proposed 180-nm DPA to reduce the effects of slower rise/fall times at GHz-frequency when compared to more advanced nodes. In this article, an off-chip π matching network is used to transform the 50-Ω reference impedance to $R_L \approx 10\ \Omega$ at 800 MHz with an insertion loss of 0.5 dB. Please observe that only C_1 is integrated on chip to provide a capacitive low-impedance path to higher order current harmonics. Moreover, an harmonic trap is used to mitigate the effect of the second



(a)



(b)

Fig. 13. DPA measurement setup for CW and modulated tests.

harmonic in V_{DS} [19]. Fig. 12 shows the final DPA-simulated AM-AM/PM performance while delivering peak $P_{out} = 24.5$ dBm with $\eta_D = 54$ % and $\eta_{sys} = 50$ %. This indicates the suitability of the proposed DPA to realize highly linear and efficient operation, being suitable to be integrated on-die with remaining baseband circuitry to form a fully digital TX with reduced DPD requirements.

V. Experimental Results

To experimentally validate the proposed design, an IC was fabricated and bond-wired to an FR4 printed-circuit board (PCB), as illustrated in Fig. 11(b), where all I/Os and power supplies are interfaced via PCB traces + bond-wires. Fig. 13 shows the measurement setup that was used to validate continuous wave (CW) and modulated performance. A computer with MATLAB is used to generate all data and control the measurement equipment. The BB PM modulated data are uploaded to an R&S SMJ100a vector signal generator (VSG) that outputs the RF PM signal which is used to drive the PCB. The ACW data are stored on the data pattern generator (DPG) Agilent 16822A. To guarantee proper alignment between AM and PM paths, the DPG uses the BB clock from the VSG as a reference. PCB and IC delay mismatches cannot be easily corrected since the coarse adjustment is only n_c/f_s samples. For this, the DPG allows delaying the AM BB clock with respect to the PM signal in steps of $D_{frac} = n_f/(15 \cdot f_s)$.

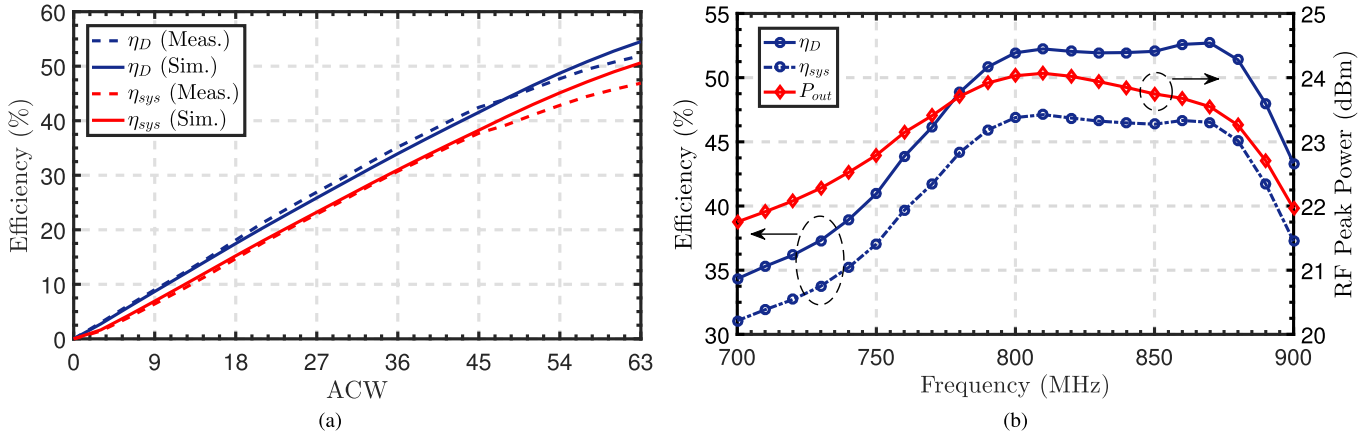


Fig. 14. (a) Peak CW efficiency at $f_c = 800$ MHz. (b) Peak efficiency and RF power over frequency.

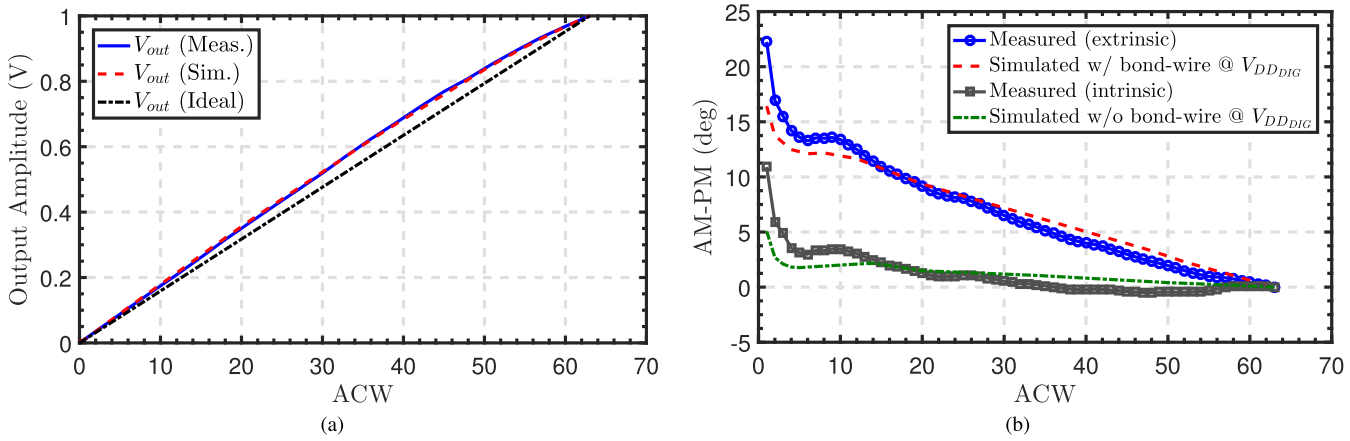


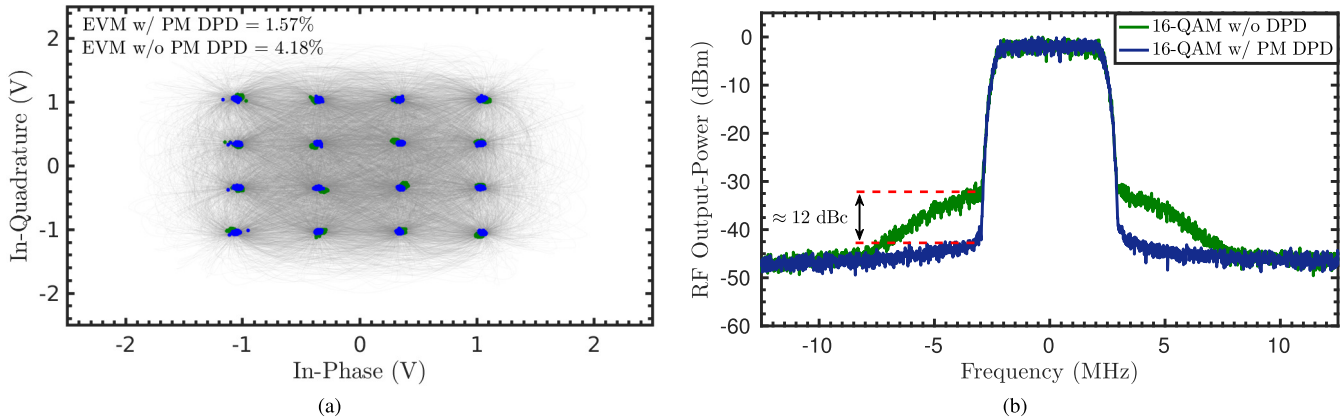
Fig. 15. (a) AM-AM and (b) AM-PM profiles obtained from raw static measurements and simulations.

To measure the dc power consumption, a Tektronix oscilloscope model DPO3052, equipped with a wideband current probe (TCP0030A) is used, while the RF power is measured with an Agilent N1913A power meter. To assess the dynamic behavior, modulated signals are captured and down-converted to BB with a vector signal analyzer (VSA) R&S FSQ8. Afterward, the data are transferred to the PC and demodulation is performed. To suppress time-varying carrier offsets, both the VSA and the VSG share the 10-MHz reference clock.

When performing dynamic measurements with high sampling frequency ($f_s \geq 50$ MHz), fast glitches (RF speed) were observed on the AM-AM characteristic. These result from the voltage ringing induced by digital supply parasitic inductances (PCB + bond-wire) that generate time-varying $V_{\mathrm{DD_{DIG}}}$ that is momentarily captured by the synchronizer flip-flop (updated every RF cycle). Also, the ringing magnitude, and consequently its settling time will also vary with ACW. Note that on a fully digital TX the core DPA would have smaller parasitics due to shorter power interconnects and on-chip decoupling, eliminating these effects [7], [22], [30], [31]. For this reason, the following measurement were carried out considering $V_{\mathrm{DD_{RF}}} = 3.5$ V and $V_{\mathrm{DD_{DIG}}} = 2.2$ V and $V_P = 1.9$ V.

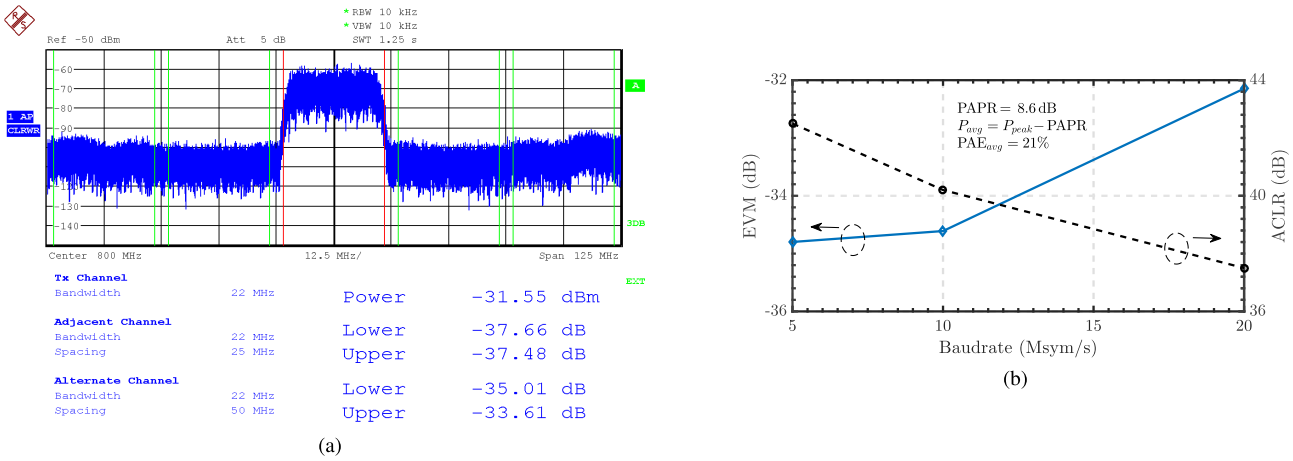
A. Static Measurements

Fig. 14(a) shows the efficiency as a function of ACW. The measured peak drain efficiency was $\eta_D = 52\%$ while the system efficiency was $\eta_{\mathrm{sys}} = 47$ %, showing reasonable agreement with simulated results ($\eta_D = 54$ % and $\eta_{\mathrm{sys}} = 50$ %). Fig. 14(b) shows the efficiency and RF power as a function of frequency, where $P_{\mathrm{out}} = 24$ dBm was measured at 800 MHz. To measure the linearity in static conditions a ramp signal is generated and uploaded to the DPG with $f_{\mathrm{ramp}} = 1$ kHz with a fixed PM phase, providing enough settling time to fade away possible dynamic effects. Fig. 15 depicts the raw static AM-AM and AM-PM profiles measured at 800 MHz. The amplitude linearity is consistent with the simulation results, indicating that it is kept under 1 dB for full-ACW. The measured AM-PM profile shows some discrepancy that results from parasitic inductances on the digital power supply [22]. Thus, an estimate is used to derive a lumped-model on the digital supply rail [22], where the simulated AM-PM result is shown in dashed red, demonstrating good agreement with the measurements. Therefore, by using the simulation results, one can calculate the added phase shift due to parasitics as $\Delta\phi$ = Simulated w/ bond-wire − Simulated w/o bond-wire, and estimate the intrinsic DPA phase linearity by subtracting



(a) (b)

Fig. 16. (a) Demodulated 5—Msym/s 16-QAM constellation. (b) PSD with and without PM path DPD. Note that no AM DPD is applied.



(a) (b)

Fig. 17. (a) PSD of 20—Msym/s 64-QAM. (b) EVM, ACLR, and η_{sys} for 64-QAM as a function of baudrate. Note that no AM DPD is applied.

$\Delta\phi$ to the measured extrinsic results, leading to the gray curve with square markers. This enables us to infer from the extrinsic measurement the intrinsic linearity of the DPA, which reasonably matches the simulated results. Therefore, compared to the typical highly compressed AM-AM and nonlinear AM-PM profiles of triode operated unit-cells [5], [11], [23], [32], the proposed design attains improved raw linearity.

B. Dynamic Signal Measurements

Wideband complex modulated signals are employed to access the dynamic performance of the proposed DPA. Polar TXs are particularly sensitive to AM-PM misalignments [8]. Therefore, coarse tuning and fine-tuning are employed to ensure that the adjacent-channel leakage ratio (ACLR) and error vector magnitude (EVM) are both optimized. The baseband sampling frequency is fixed at $f_s = 100$ MHz and up-sampling is applied to all M-QAM signals after polar decomposition with a raised cosine filter with a span of 20 symbols and roll-off of 0.2. A $5-$ Msym/s 16-QAM signal with peak-to-average power ratio (PAPR) of 8.6 dB is used to perform AM-PM alignment. Fig. 16 shows the demodulated constellation and power spectral density (PSD) after alignment. Also, a memoryless lookup table (LUT)-based DPD is applied on the PM up-sampled signal, demonstrating an increase of ≈12 dB on noise PSD and EVM from 4.18% to EVM= 1.57% without the need for digital power back-off. A two-tone test with 2-MHz spacing is performed with PM DPD achieving 38.7 dBc, representing an improvement of 11 dBc when compared to the situation without PM DPD. The DPA was also tested with 64-QAM and 256-QAM with 10 and 20 Msym/s baudrate, achieving EVM $=$ 1.86% and EVM $=$ 2.36%, respectively. Thus, this demonstrates the high level of linearity that the proposed CM-DPA is able to achieve with reduced design complexity and improved system efficiency. Fig. 17(a) reports an ACLR of 37.5 dB for a BW = 22-MHz wideband signal (20-Msym/s 64-QAM) with PM DPD only. Considering that the output signal-to-noise ratio (SNR) around the carrier is dominated by the AM quantization noise

$$\text{SNR}_i = 6.02 \cdot N + 1.76 + 10 \cdot \log_{10}\left(f_s/(2 \cdot \text{BW})\right) \quad (13)$$

where N is the number of bits, f_s is the sampling frequency, and BW is the signal bandwidth, the achievable SNR would be $\text{SNR}_i = 41.44$ dB, thus a depreciation of only ≈ 4 dB is verified during measurements. Fig. 17(b) shows the evolution of 64-QAM EVM and ACLR as a function of signal baudrate (PAPR $=$ 8.7 dB). The measured system efficiency

TABLE I
COMPARISON WITH STATE-OF-THE-ART DPA TXS

[Ref.] Year	CMOS node	Architecture unit cell	f (GHz), P_{sat} (dBm), PAE	MNT on chip	BW, Mod EVM_{rms}	Linearization	$ACLR_1$ (dBc)	f_{samp} (MHz)	Res.
[32] 2017	40 nm	Digital polar class E/F_2	2.6, 17.2, 45 %	×	40 MHz, QAM NA	Nonlinear sizing + V_{OV} control + MP RF clock	40	625	9 bits
[16] 2015	65 nm	Digital polar class AB	2.1, 22.8, 27.6 %	√	20 MHz, 802.11g −28 dB	Replica PA SCAP DPM	46†	246	9+6 bits
[11] 2018	28 nm	Digital polar class D^{-1}	2.5, 24.5, 42.7 %⋆	√	20 MS/s, 64-QAM −32.4 dB	AM DPD + Feedforward Cap + Bias Scheme	31.2	NA	8 bits
[14] 2017	28 nm	Digital IQ CM stacked	1.0 21, 33 %	×	40 MHz, WLAN 64-QAM −30.3 dB	2D-DPD	NA	500	12 bits
[33] 2017	28 nm	Digital-IQ SCAP + cell sharing	0.8 13.9, 40.4 %	×	10 MHz, LTE 16-QAM −26 dB	No	32.5	100	6 bits
[23] 2017	130 nm	Digital MP SCAP	1.8 26, 24.9 %	√	10 MHz, LTE 16-QAM −29 dB	2D DPD	30.8	200	7 bits
[22] 2018	65 nm	Digital split array MP SCAP	1.8 24, 40 %	√	1.4 MHz, LTE 64-QAM −31.5 dB	AM/PM DPD	30.7	100	13 bits
[30] 2017	65 nm	Digital polar VM Doherty SCAP	0.9 24, 45 %	×	40 MHz, 802.11ac 256-QAM −34.8 dB	AM/PM DPD	NA	360	10 bits
[34] 2017	180 nm	Analog Class-B/AB	1.85 27◇, 32 %◇	√	10 MHz, LTE 16-QAM −30.3 dB	Anti-phase + MGTR	30	–	–
This work	**180 nm**	**Digital polar CM cascode**	**0.8 24, 47 %**	×	**20 MS/s, 256-QAM −32.5 dB** / **10 MS/s, 64-QAM −34.6 dB**	**PM DPD**	**37.6** / **40.34**	**100**	**6 bits**

NA = not available; †measured at 30 MHz; ⋆drain efficiency; ◇graphically estimated from available data at 1 dB gain compression point;

is approximately $\eta_{sys} = 21\%$ while the degradation on both EVM and ACLR are dominated by the decreased ratio f_s/BW.

Table I compares the proposed architecture with the state-of-the-art DPAs. Note that the test signal PAPR for all references is usually between 7 and 9 dB, not shown in the table for the sake of simplicity. Compared to the prior art, this article approach requires less design complexity, lower number of bits, and less sampling frequency to achieve a given EVM and/or ACLR. This eventually leads to a higher η_{sys}/η_D ratio which is already favored in this design by adopting power cells with higher gain than traditional nonlinear DPAs. Therefore, this demonstrates that inherently linear CM power cells are good candidates to be used in the future high-performance digital TXs to optimize both the efficiency and the linearity while also reducing design complexity.

VI. CONCLUSION

This article presented a linear and efficient CM-DPA with relaxed requirements for DPD. Instead of adopting the commonly used linear switched constant-g_m approach (analog-based), we proposed a linear switched constant-current design (digital-centric), allowing higher digital integration and lower design complexity. The core of the DPA is the cascode unit-cell which supports the constant-current operation throughout the entire PBO range. To circumvent the typical efficiency degradation of cascode/CM operation, both the polarization voltage and transistor relative width are optimized to explore higher efficiency loadlines without comprising linearity or reliability. This optimization is combined with a reduction in the conduction angle to further increase the efficiency. When compared to typical SR and SCAPs TXs (class-E and D/D^{-1}), comparable efficiency is achieved while relaxing the requirements for sampling frequency as well as the number of bits to quantize the modulated signal in order to achieve a target ACLR. Thus, compared to the prior art, the proposed design effectively reduces the need for DPD since no AM correction is applied, whereas most of DPAs require both AM and PM DPD when aiming to power amplify high PAPR signals with modulated BW $= 5-20$ MHz. Besides lower design complexity and power consumption, this alleviates the burden that is usually placed on DPD without requiring extra silicon area for calibration/compensation circuitry.

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