

# A 2-GHz Highly Linear Efficient Dual-Mode BiCMOS Power Amplifier Using a Reconfigurable Matching Network

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**Abstract**—A highly linear, efficient, two-stage power amplifier for high-data-rate wireless applications is presented. The linearity is greatly improved by adding an auxiliary amplifier to the main bipolar transistor amplifier in a feed-forward approach to cancel out the nonlinearity terms. The efficiency enhancement is achieved using a switchable biasing and a reconfigurable output-matching network based on the available input power which is monitored by an on-chip envelope detector. The PA is fabricated using 0.25- $\mu\text{m}$  SiGe:C BiCMOS technology and works at 2 GHz with a supply voltage of 2.5 V. The experimental results show a gain of 13 dB and a maximum output power of 23 dBm with a PAE of 38%. The 1-dB output power compression point is 21 dBm with a 32% PAE. The 6-dB power back-off PAE is 23%. The IM<sub>3</sub> and IM<sub>5</sub> terms are 41 and 44 dB below the fundamental tone for the 21-dBm output power, respectively. The EVM has been measured to be  $-30.7$  dB at 15-dBm average output power using IEEE 802.16e standard WiMAX 64QAM modulated signal. By employing the linearization technique, EVM and ACLR are improved by 4.5 and 5 dB, respectively, for a WiMAX 64QAM 10-MHz signal bandwidth at 14-dBm average output power.

**Index Terms**—BiCMOS power amplifier, bipolar transistor, dual-mode, feed-forward linearization,  $g_{m3}$  cancellation, peak-to-average-power ratio (PAPR), power back-off, reconfigurable matching network, second-harmonic rejection.

## I. INTRODUCTION

MODERN communication systems target higher data rates for portable devices such as personal communication systems (PCS) and satellite communications. High-data-rate applications require modulation techniques such as orthogonal frequency-division multiplexing (OFDM). These systems implemented in handsets should employ power amplifiers with both high linearity to achieve the required signal-to-noise ratio (SNR) for low bit error rate ( $\text{BER} = 10^{-6}$ )

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and high efficiency for long battery life in portable devices. In these systems, peaks occur for a small amount of time, and most of the time the signal envelopes are below the peak power. Class A or AB are typically used in highly linear power amplifiers (PAs); however, they have a poor efficiency due to the larger peak-to-average-power ratio (PAPR) of the signal. The higher the data rate, the larger the PAPR is, which requires a large back off to maintain a good linearity. This results in much lower efficiency [1]. For possible application in portable devices, the efficiency should be greatly improved. On the other hand, as the technology scales down, lower breakdown voltages and more nonlinear behavior of the transistors lead to an inferior signal-to-distortion ratio (SDR) which limits the data rate in linear PAs. Therefore, both linearity and efficiency should be improved in modern communication systems.

Recent reported PAs can be roughly categorized into three different sections; 1) highly efficient; 2) highly linear; and 3) highly linear and efficient amplifiers. In [2] and [3], the efficiency of a class-A PA is improved up to 10% by modifying the power supply based on the signal envelope at the price of linearity degradation. In [4], the efficiency of the PA at power back-offs is improved to 30% by manual adaptation of the output-matching network. In [5], a linearizer circuit has been used to increase the bias value of the input bipolar transistor at high input powers which compensates for the gain drop. In [6] and [7], envelope elimination and restoration method has been used to increase PAE with a reasonable linearity performance. Other linearization techniques such as cancelling  $g_{m3}$  (third-order coefficient of nonlinearity) employing Doherty operation [8] or suppressing the input harmonics of a class-AB PA [9] are also reported in the literature. In [10], a combination of class-A and class-B PAs has been used to improve both linearity and efficiency. In [11], a class-AB/F PA has been proposed to work in two modes, one efficient mode (class F) and one linear mode (class AB) suitable for multiple systems on chip. In [12], it has been shown that the deep n-well (DNW) of nMOS transistor lowers the harmonic distortion generated from the gate–source capacitance which improves the linearity of the PA by 7 dB. In [13], by an optimum transistor gate bias and second-harmonic termination, the IM<sub>3</sub> level is improved by 7 dB. In [14]–[16], the outputs of multiple PA stages are combined as voltages in series by employing transformers. In this case, the efficiency of the PA can be improved at power back-offs by turning off one or two stages.

This paper presents a new reconfigurable matching network technique in a fully integrated class-AB PA in  $0.25\text{-}\mu\text{m}$  SiGe:C BiCMOS technology [17]. The PA delivers 23-dBm maximum output power with simultaneous efficiency and linearity improvement. Efficiency improvement is achieved by switching the biasing states of the transistors based on the input power level of the signal which is monitored by an envelope detector. The gain of the PA in transition remains constant by implementing a reconfigurable matching network for both high and low input signal levels. The linearity is greatly enhanced based on a feed-forward nonlinear cancellation technique. Therefore, the proposed PA can improve both PA efficiency and linearity in high-data-rate standards such as WiMAX, and 4G LTE for handsets, and can be tuned to the desired frequency band. Section II discusses the fundamentals of the proposed PA and different modes of operation. In Section III, the linearization technique and the circuit implementation is discussed in details. Section IV presents the efficiency improvement technique and the reconfigurable matching network. The measurement results are summarized in Sections V, and VI concludes the paper.

## II. SYSTEM IMPLEMENTATION

In an OFDM system, a high data rate is achieved with multicarrier modulation in which the transmitted power may vary greatly. Therefore, it suffers from a large PAPR. In a practical RF transmitter, PAPR determines the linear dynamic range requirement for the PA. A potentially large PAPR will result in the following disadvantages [18].

- 1) If the peak power exceeds the dynamic range of the PA, the transmitted signal will be clipped and gives rise to out-of-band radiation.
- 2) In OFDM systems, the biasing point of the designed PA should be optimized for the performance at  $P_{1\text{dB}}$ , even though the efficiency is dominated by the efficiency of the average output power which is 8 to 10 dB lower.

Fig. 1(a) shows a time-domain OFDM signal that has a large PAPR, and Fig. 1(b) shows the probability of a peak power occurrence in an OFDM signal [19]. The graph shows that the probability of having a peak power is really small in these systems. Therefore, as shown in Fig. 1(a), the transmitter operation can be divided into two different regions, a low-power and a high-power region, in which decreasing the power consumption in lower input powers would result in a great efficiency improvement.

Fig. 2 shows the system implementation of the proposed PA in which the efficiency is improved by switching between two different modes of operation based on the input power signal. The input signal is being monitored by an on-chip envelope detector. Based on the comparison between the input signal and a reference voltage, which is usually 6 dB below the peak input power, a decision signal is generated at the output of the comparator. The signaling determines if the amplifier is in high- or low-power mode. For the high output power, the amplifier dc biasing is switched to higher values to deliver higher output powers with good linearity. In the low-power mode, the biasing is decreased in order to enhance the efficiency. While the  $g_m$  of the amplifier is decreased due to lower dc biasing values, the output load ( $R_L$ ) is increased through a switchable matching

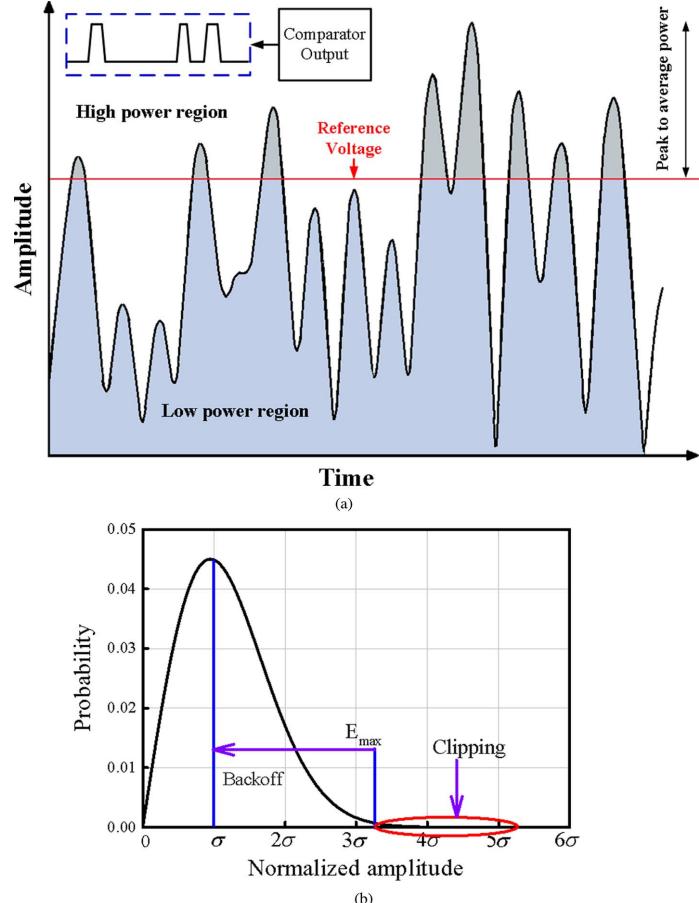


Fig. 1. (a) PA operation mode is divided into two regions for the transient OFDM signal based on the reference voltage. (b) Envelope amplitude distribution for IEEE 802.11a OFDM signal.

network to sustain a constant output voltage  $g_m R_L$  for both modes. Therefore, the PA maintains the linearity performance of a constant dc bias PA. A preamplifier is designed to drive the high input capacitance of the main amplifier. Also, the linearity of the main amplifier is greatly enhanced based on a feed-forward cancellation technique. An auxiliary path is added to the main amplifier to cancel out the nonlinear terms of the main amplifier. Since the linearity of the main amplifier is sufficient for low-input-power signals, the auxiliary path can be switched off to further increase the PAE of the entire PA.

## III. LINEARITY IMPROVEMENT TECHNIQUE

### A. Fundamentals

Nonlinear current–voltage relationship in transistors is the major factor for nonlinear behavior of the RF blocks and as the technology scales down it is further degraded. The voltage–current relationship of a transistor can be written as follows:

$$i = g_{m1}v + g_{m2}v^2 + g_{m3}v^3 \quad (1)$$

where  $g_{mi}$ , ( $i = 1, 2, 3$ ) is the  $i$ th-order term coefficient. In narrowband systems,  $g_{m2}$  causes some out-of-band second-order inter-modulation terms that would be filtered through the output-matching network. The input-referred third-order intercept point ( $IIP_3$ ) is one of the parameters for monitoring the

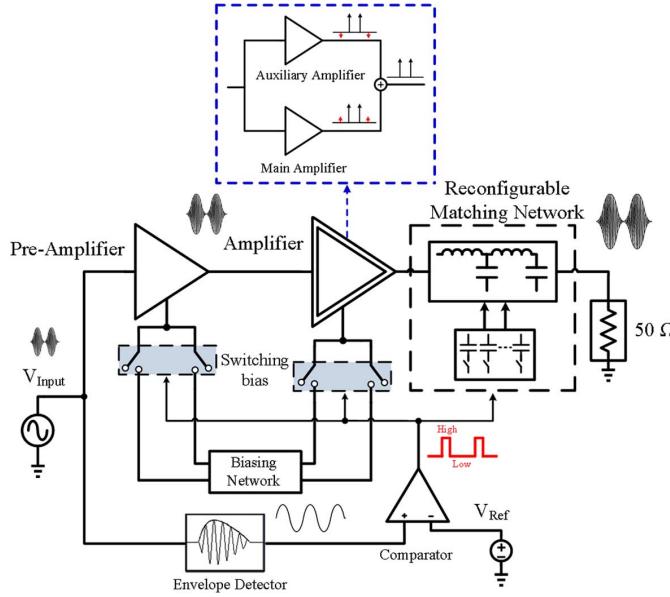


Fig. 2. System implementation of the proposed PA.

linearity performance of the circuit and can be found as follows [20]:

$$A_{\text{IIp3}} = \sqrt{\frac{3}{4} \frac{g_{m1}}{g_{m3}}}. \quad (2)$$

Therefore,  $g_{m3}$  is the main source of nonlinearity in PAs, and the linearity can be greatly improved by cancelling out  $g_{m3}$ . The current of a bipolar transistor can be approximated as follows:

$$i_{ce} = \alpha_1 v_{be} + \alpha_2 v_{be}^2 + \alpha_3 v_{be}^3 \quad (3)$$

$$i_{CE} = I_{S0} e^{\frac{V_{BEQ}+v_{be}}{\phi_t}} = I_Q e^{\frac{v_{be}}{\phi_t}} \quad (4)$$

$$\alpha_3 = \frac{I_Q}{6\phi_t^3} \quad (5)$$

where  $V_{BEQ}$  is the base-emitter bias voltage,  $I_{S0}$  is the saturation current, and  $\phi_t$  is the thermal voltage. As shown in (5), the third-order power coefficient for bipolar transistors is positive due to exponential relationship between the collector current and the base-emitter voltage [21].

CMOS transistors biased in saturation have a negative third-order coefficient. The current of an nMOS transistor in strong inversion can be approximated as follows [21]:

$$i_{ds} = \beta_1 v_{gs} + \beta_2 v_{gs}^2 + \beta_3 v_{gs}^3 \quad (6)$$

$$i_{DS} = \frac{x^2}{1 + \theta x} \quad (7)$$

$$x = 2\eta\phi_t \ln \left( 1 + e^{\frac{v_{gs}-v_{th}}{2\eta\phi_t}} \right) \quad (8)$$

$$\beta_3 = -\frac{\theta K}{(1 + \theta V_{\text{eff}})^4} \quad (9)$$

where  $v_{th}$  is the threshold voltage,  $\phi_t$  is the thermal voltage,  $\theta$  is the normal field mobility degradation factor,  $\eta$  is the ratio of the exponential increase of the drain current with  $V_{gs}$  in sub-threshold region,  $K = 0.5 \mu_n C_{ox} W/L$  [21],  $V_{\text{eff}} = V_{gs0} - V_{th}$ , and  $V_{gs0}$  is the dc gate-source bias voltage [22]. By adding a

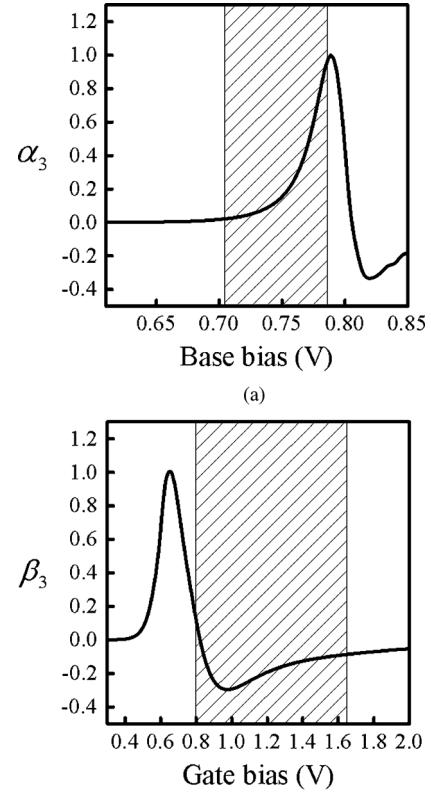


Fig. 3. (a) Normalized  $\alpha_3$  coefficient versus the base bias voltage for the bipolar transistor. (b) Normalized  $\beta_3$  coefficient versus the gate bias voltage for the nMOS transistor.

current with positive  $g_{m3}$  to the nMOS transistor, it can be linearized. The goal is to linearize the PA with a minimum number of transistors since any increase in the number of the transistors would degrade the PAE. Therefore, the current in bipolar and nMOS transistors can be added at the output to cancel out the  $g_{m3}$  of the entire PA as follows:

$$i_O = (\alpha_1 + \beta_1)v_{in} + (\alpha_2 + \beta_2)v_{in}^2 + (\alpha_3 + \beta_3)v_{in}^3 \\ = g_{m1}v_{in} + g_{m2}v_{in}^2 + g_{m3}v_{in}^3. \quad (10)$$

The phase and the magnitude of the  $g_{m3}$  are a function of the dc biasing, and the size of the transistors. Fig. 3 shows the simulation results for  $g_{m3}$  as a function of the dc biasing for both BJT and nMOS transistors for a particular size. As it is highlighted in the figure, for certain biasing voltages,  $\alpha_3$  is positive, while  $\beta_3$  is negative, and the total  $g_{m3}$  can be cancelled out.

### B. Main Core PA

Fig. 4(a) shows the schematic of the core PA. If the output load is connected to  $V_{dd}$  through an RF choke or an  $LC$  tank which doubles the output swing, the output power will be

$$P = \frac{1}{2} \frac{V_{dd}^2}{R_L}. \quad (11)$$

The dc supply voltage used in the amplifier is 2.5 V. If a 0.5-V margin is considered for the saturation voltage in the transistors and the losses, the output peak-to-peak swing is 4 V. To achieve output power of 25 dBm, the required load ( $R_L$ ) will be 10  $\Omega$ .

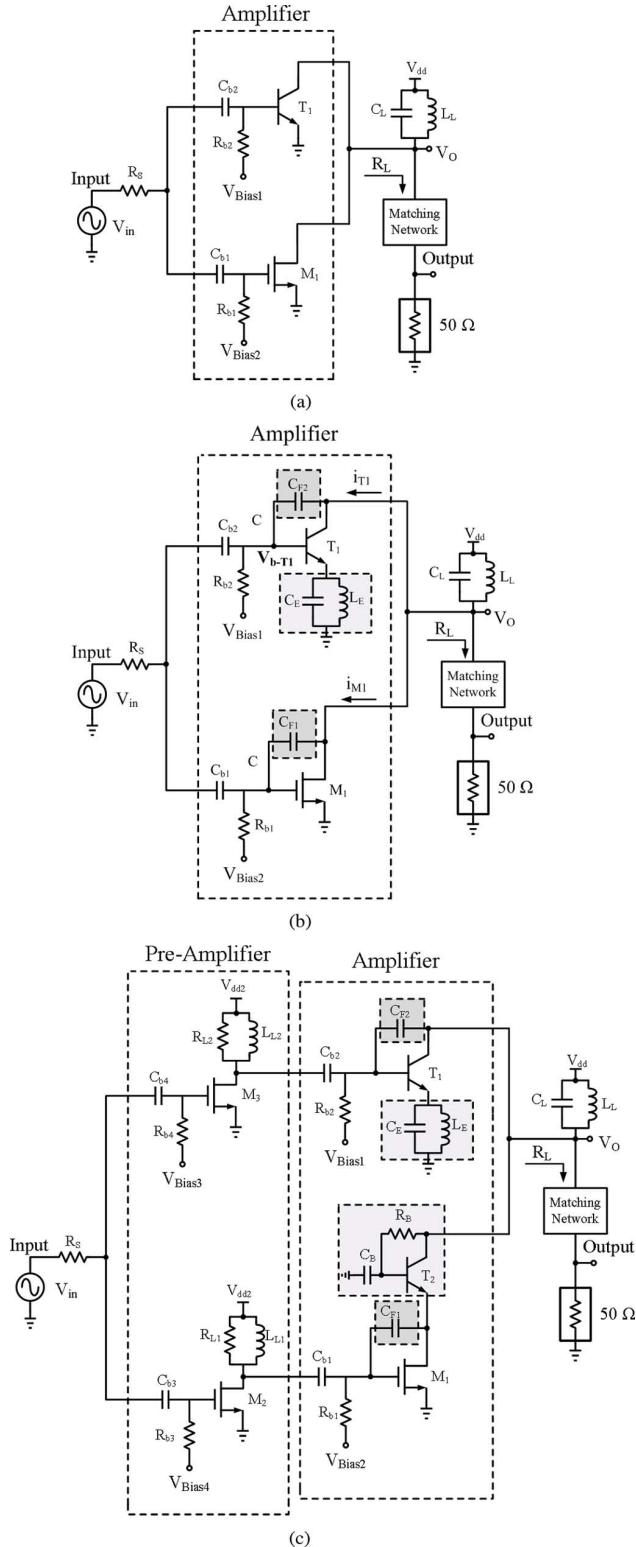


Fig. 4. (a) Schematic of the core PA. (b) Core PA with second-harmonic rejection and IM<sub>3</sub> phase adjustment. (c) Core PA with the preamplifier stage.

As shown in Fig. 4(a), the signal is applied to both  $T_1$  and  $M_1$ , and the output currents are combined. Since BJT is capable of providing a higher amount of current compared to its nMOS counterpart,  $T_1$  is employed as the main amplifier. Although the third-order coefficients ( $\alpha_3$  and  $\beta_3$ ) are out of phase, the signals

TABLE I  
NMOS TRANSISTOR PARAMETERS USED IN THE CORE PA

	Length	Width	No. of Stripes	No. of Parallel cells
NMOS Transistor	0.25μm	133μm	14	6

TABLE II  
BIPOLAR TRANSISTOR PARAMETERS USED IN THE CORE PA

	Emitter Length	Emitter Width	No. of Emitters	No. of Repeated cells
BJT Transistor	35μm	0.4μm	3	3

are in phase for both transistors and the output power would be combined similar to a parallel power combination topology [14]–[16].

In order to achieve a higher PAE, both transistors are biased in the class-AB region.  $T_1$  works as a linear amplifier and has a large  $g_m$  which provides most of the gain, while  $M_1$  is providing a small  $g_m$  compared with  $T_1$ , leading to  $\alpha_3$  much larger than  $\beta_3$ . To be able to cancel out the third-order coefficient terms ( $\alpha_3$  and  $\beta_3$ ), transistor  $M_1$  is intentionally forced to be mostly in nonlinear region. Therefore, transistor  $M_1$  linearizes the bipolar transistor  $T_1$  while increasing the output power by providing in phase fundamental current component. DC biasing adjustment and sizing of the transistors are based on perfect cancellation of the third-order coefficients at the peak input signal power. For high output power (25 dBm), the base of  $T_1$  is biased at 765 mV while the gate of  $M_1$  is biased at 1 V; the size of the transistors are included in Tables I and II. The currents are added at the output and applied to the matching network. Instead of using an off-chip RF choke, a parallel  $LC$  network ( $C_L$  and  $L_L$ ) has been employed at 2-GHz resonance frequency.  $L_L$  is designed to be 1 nH while  $C_L$  is set to be 3 pF. The loss of the tank decreases the voltage swing which degrades the maximum output power to 24 dBm.

### C. Nonlinear Base Capacitance

Although the bipolar transistor has high power-handling capabilities, it has a highly nonlinear capacitance at the base junction [23]. This capacitor results in a large second-order harmonic current and lowers the available output power to 16 dBm. To overcome this issue, a parallel  $LC$  network ( $C_E$  and  $L_E$ ) in Fig. 4(b) is employed in the emitter of  $T_1$ , resonating at the second harmonic of the fundamental tone. This  $LC$  tank acts as a source degeneration circuit and decreases the current at 4 GHz.  $L_E$  should be small since the inductor will degenerate the fundamental tone, which will result in a lower output power.  $L_E$  is chosen to be 140 pH while  $C_E$  is 8 pF, including the parasitic capacitance in the emitter of  $T_1$ . The circuit is simulated with and without the  $LC$  tank, and, as shown in Fig. 5, the  $LC$  tank attenuates the higher harmonics, especially the second harmonic by 19 dB. Since  $L_E$  is small, the  $Q$  of the inductor is larger than 9 at 2 GHz, and therefore 0.8-dB gain drop is mostly because of the impedance of the tank at the fundamental tone rather than

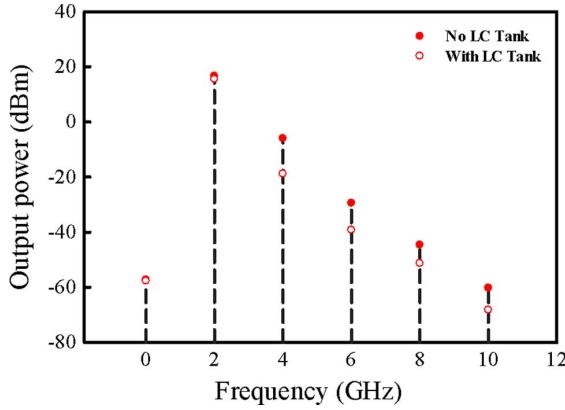


Fig. 5. Second-harmonic and higher harmonic rejection of the output power by employing the *LC* tank in the emitter of the bipolar transistor.

the inductor loss. As shown in [13], second-harmonic degradation can improve the linearity of the PA by decreasing  $\text{IM}_3$  and  $\text{IM}_5$  levels.

#### D. IMD Phase Adjustment

The nonlinear base-emitter capacitance of  $T_1$  at high output powers will change the phase of both  $\alpha_3$  and  $\beta_3$ . This will degrade the feed-forward cancellation technique. The phase of  $\alpha_3$  and  $\beta_3$  can be adjusted by adding feedback capacitors,  $C_{F1}$  (300 fF) and  $C_{F2}$  (150 fF), in parallel with the gate-drain and base-collector capacitors, respectively [Fig. 4(b)]. Due to nonlinear base capacitance in  $T_1$ , the input base voltage, the currents  $i_{T1}$  and  $i_{M1}$  are given by [Fig. 4(b)]

$$V_{b-T_1} = \sigma_1 v_{in} + \sigma_2 v_{in}^2 + \sigma_3 v_{in}^3 \quad (12)$$

$$i_{T1} = (v_O - \sigma_1 v_{in} - \sigma_2 v_{in}^2 - \sigma_3 v_{in}^3) C_{F2}s + \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 \quad (13)$$

$$i_{M1} = (v_O - v_{in}) C_{F1}s + \beta_1 v_{in} + \beta_2 v_{in}^2 + \beta_3 v_{in}^3 \quad (14)$$

$$v_O \cong -\{(\alpha_1 + \beta_1) \times R_L\} v_{in} \quad (15)$$

and (16), shown at the bottom of the page. Therefore, the phase difference between  $\alpha_3$  and  $\beta_3$  can be compensated through the feedback capacitors and the  $\text{IM}_3$  of the main amplifier would be cancelled out. As can be seen in (16), the fundamental currents are no longer in phase, which will cause a small drop at the output power.

#### E. Self-Biased Cascode Unit

To increase the output power, the power supply should be as large as possible (2.5 V in this technology). The collector and the drain of the BJT and nMOS transistors are connected together and share the same dc voltage. Because of the low gate-drain breakdown voltage of the nMOS transistor at this

technology (1.7 V), the power supply cannot be connected directly to the drain. To overcome this issue, a self-biased cascode structure [24] is employed to divide the output swing between the two transistors. As shown in Fig. 4(c), transistor  $T_2$  is added to the circuit as a cascode device. The values of  $R_B$  and  $C_B$  are set not to affect the phase of the current in transistor  $M_1$ . The average current consumption of the main amplifier stage is 105 mA.

#### F. Preamplifier Stage

Large-input transistors ( $M_1$  and  $T_1$ ) result in a large input capacitance of the order of 1–2 pF. To drive the main transistors, a preamplifier stage is employed. The transistors in this stage are biased in class A region to provide sufficient linearity. As shown in Fig. 4(c), the preamplifier stage is realized using nMOS transistors to make the input capacitance smaller. For further improving the efficiency and also preventing the nMOS transistors from breakdown, the supply voltage for this stage is lowered down to 1.7 V.  $L_{L1}$  (1.6 nH) and  $L_{L2}$  (2 nH) are employed to tune out with the input parasitic capacitance of the main amplifier stage at 2 GHz. Resistors  $R_{L1}$  and  $R_{L2}$  are added to eliminate large peaking and potential oscillation. The current consumption in this stage is around 38 mA, which results in a small efficiency degradation.

#### G. Gain of the PA

The total gain of the system is the sum of the two stage gains which can be written as follows:

$$\begin{aligned} \text{Gain} = & (g_{m_{M1}} + g_{m_{T1}}) R_L \times [g_{m_{M2}} (Q_{L1}^2 R_{S_{L1}} \parallel R_{L1}) \\ & + g_{m_{M3}} (Q_{L2}^2 R_{S_{L2}} \parallel R_{L2})] \end{aligned} \quad (17)$$

in which  $g_m$  is the transconductance of the transistors,  $Q_{L1}$  and  $Q_{L2}$  are the quality factor of the inductors  $L_{L1}$  and  $L_{L2}$  at 2 GHz, respectively.  $R_{S_{L1}}$  and  $R_{S_{L2}}$  are the series losses associated with the inductors  $L_{L1}$  and  $L_{L2}$ , and  $R_L$  is the impedance seen form the matching network. Considering  $R_L$  to be 8  $\Omega$ , the total gain is calculated as follows:

$$\begin{aligned} \text{Gain} = & [(290 \text{ mS} + 100 \text{ mS}) \times 8] \\ & \times [(40 \text{ mS} \times 21) + (40 \text{ mS} \times 23)] \\ & \cong 5.11(14 \text{ dB}). \end{aligned} \quad (18)$$

The gain of the preamplifier is only 4 dB to minimize nonlinearity degradation by this stage.

#### H. Two-Tone Linearity Test

In order to simulate the effect of linearity improvement technique, two tones are applied to the PA, and the output  $\text{IM}_3$  and  $\text{IM}_5$  are monitored for different output powers. The dc biasing

$$A_{\text{IIP3}} = \sqrt{\frac{3}{4} \left| \frac{j\omega(-(\alpha_1 + \beta_1) \times R_L \times (C_{F1} + C_{F2}) - C_{F1} - \sigma_1 C_{F2}) + \alpha_1 + \beta_1}{-j\omega C_{F2}\sigma_3 + \alpha_3 + \beta_3} \right|} \quad (16)$$

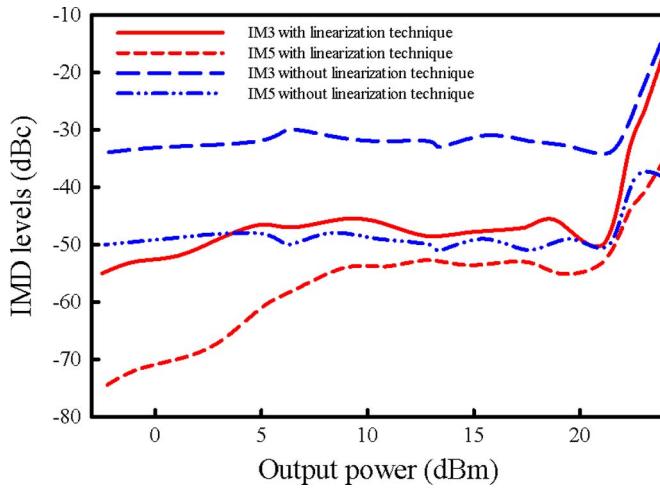


Fig. 6. IMD levels versus output power with and without linearization technique.

values are adjusted to get the best  $\text{IM}_3$  cancellation at the highest output power. The test has been performed for 1-MHz frequency spacing between the two tones, with and without the feed-forward cancellation technique versus the output power. The simulation results are shown in Fig. 6. This technique improves the  $\text{IM}_3$  levels by 10–20 dB, and as the frequency spacing becomes smaller, a better  $\text{IM}_3$  cancellation is achieved. In this approach, the  $\text{IM}_5$  levels are also improved especially for output powers below 5 dBm.

### I. Effect of Temperature, Bias Value, and Supply Voltage Variations

In 0.25- $\mu\text{m}$  BiCMOS NXP process, the substrate thermal resistance is 125 K/W. Based on the dissipated power in the power amplifier, the temperature of the die can be calculated using the following equation [25]:

$$T_{\text{die}} = T_{\text{ambient}} + R_{\text{Th-substrate}} \times P_{\text{dissipated}} \quad (19)$$

$$T_{\text{die}} = 303K + 125 \frac{K}{W} \times 250 \text{ mW} = 333K = 60^\circ\text{C}. \quad (20)$$

Therefore, the nominal temperature of the die is  $60^\circ\text{C}$ , and all of the designs and simulations have been performed at the same temperature. Since the threshold voltage of nMOS transistors and base-emitter on-voltage of bipolar transistor are temperature dependent, a change in the temperature can degrade the  $\text{IM}_3$  cancellation. As a result the  $\text{IM}_3$  level increases. Fig. 7(a) shows the simulated  $\text{IM}_3$  and  $\text{IM}_5$  levels at the output of the PA for high-power mode versus the temperature variations. The two-tone test has been performed for the average output power of 20 dBm and two different frequency spaces (1 and 10 MHz). As the temperature increases, by keeping the same biasing values, the transistors  $M_1$ , and  $T_1$  move toward the saturation region, causing the output signal to show a more nonlinear behavior. On the other hand, as the temperature decreases, the transistors  $M_1$ , and  $T_1$  move toward triode and linear region, respectively, and the performance of the  $\text{IM}_3$  cancellation technique degrades. Therefore, automatic calibration can be done when temperature changes significantly. By readjusting the biasing values of  $M_1$  and  $T_1$  to be far from saturation (decreasing the base and the

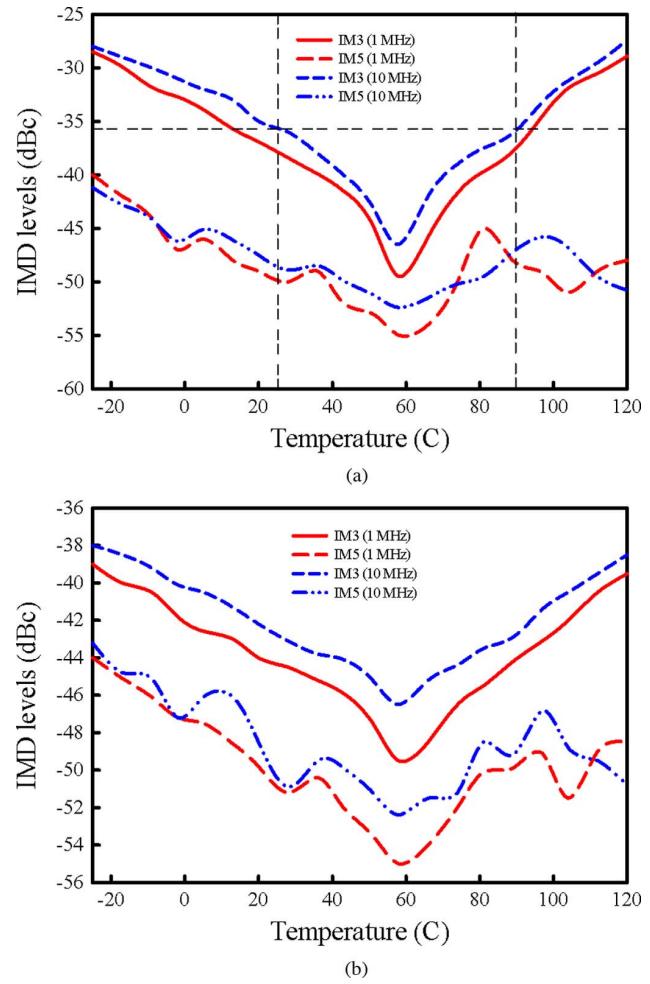


Fig. 7. (a) Effect of temperature variations on  $\text{IM}_3$  cancellation technique (20-dBm average output power). (b) Effect of temperature variations on  $\text{IM}_3$  cancellation technique after readjusting the biasing values of transistors  $T_1$  and  $M_1$ .

gate dc values of  $T_1$  and  $M_1$  for higher temperatures and increasing them for lower temperatures), the effect of temperature variations can be compensated, and the output power can be linearized as shown in Fig. 7(b).  $\text{IM}_3$  level below  $-36$  dBc is considered a reasonable value for 20-dBm output power (it results in an OIP<sub>3</sub> of 38 dBm). Therefore, this technique can tolerate  $23^\circ\text{C}$ – $89^\circ\text{C}$  temperature variations. By readjusting the bias values, the linearization technique covers the temperature range of  $-25^\circ\text{C}$  to  $120^\circ\text{C}$ .

The  $\text{IM}_3$  cancellation technique is not strongly dependent on the power supply as far as the variations in the power supply do not cause any clipping at the output signal. Fig. 8 shows the simulated  $\text{IM}_3$  levels for different power supply values at different frequency spaces (1 and 10 MHz) for the two-tone test (the average output power: 20 dBm). Since there is a large voltage swing at the output, lowering down the power supply below 2.2 V will cause clipping at the output and degrades the linearity of the PA.

The robustness of the linearization approach over transistor dc bias value variations is also tested with the two-tone test. The dc biasing of nMOS transistor  $M_1$  and bipolar transistor  $T_1$  are swept, and the effect of the variations are shown on the  $\text{IM}_3$  and

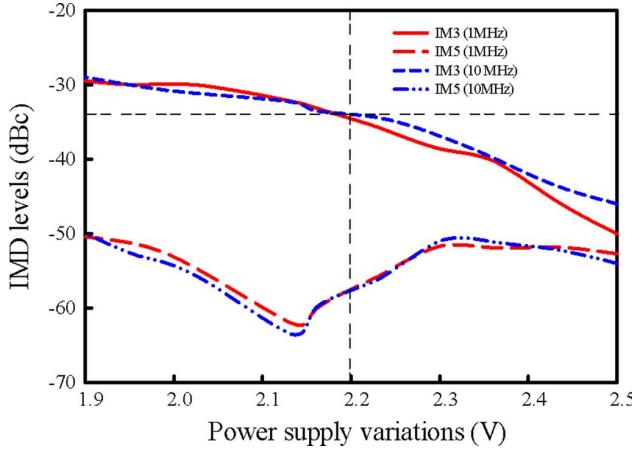
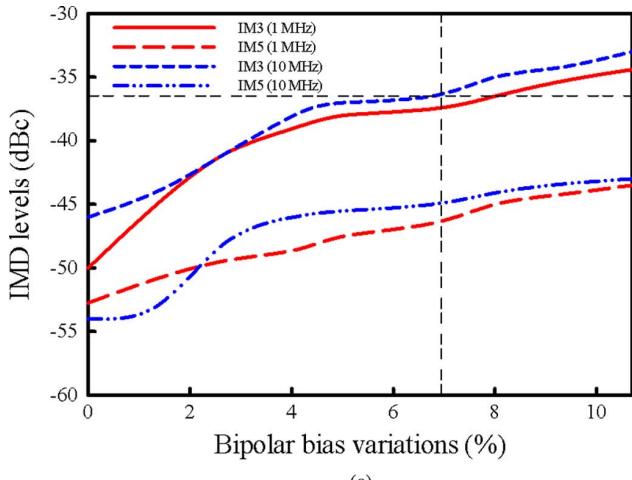
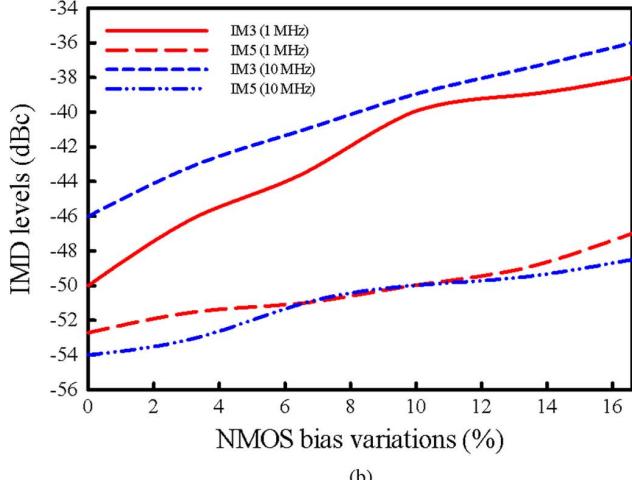


Fig. 8. Effect of power supply variations on  $\text{IM}_3$  cancellation technique (20-dBm average output power).



(a)



(b)

Fig. 9. Effect of bias variations on  $\text{IM}_3$  cancellation technique. (a) Bipolar transistor. (b) nMOS transistor.

$\text{IM}_5$  levels in dBc in Fig. 9. Since the collector current of bipolar transistor is an exponential function of the input base voltage, it is more sensitive to base dc biasing variations compared with its nMOS counterpart. For a reference  $\text{IM}_3$  level of  $-36$  dBc, the linearization technique can tolerate 16% biasing variations for the nMOS transistor and 7% biasing variations for the bipolar

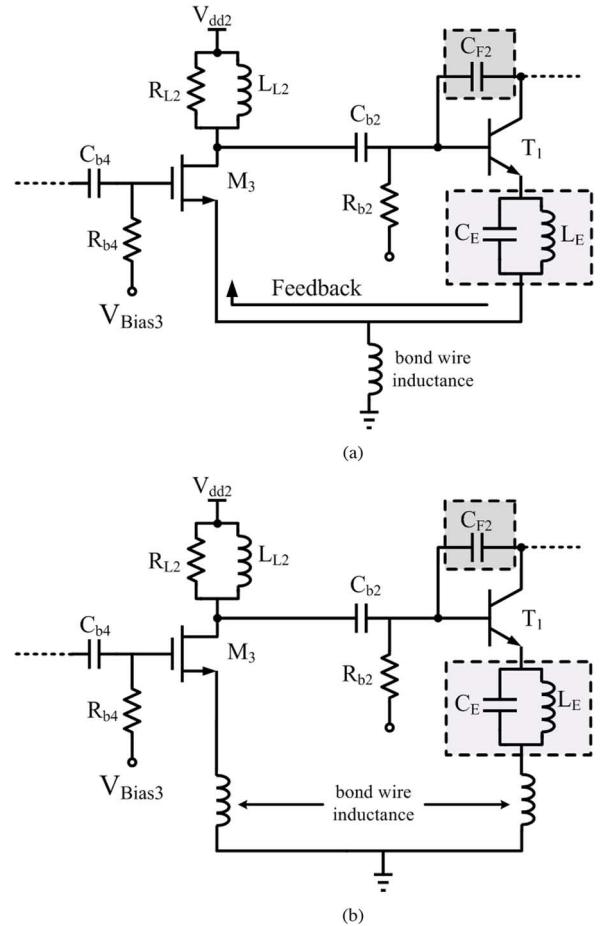


Fig. 10. (a) Feedback loop in the PA caused by both stages sharing the same ground bond-wire. (b) Different ground bond-wires for the two stages of the PA.

counterpart. Based on the linearity requirement in the system, the linearization technique can be readjusted to achieve a better  $\text{IM}_3$  cancellation for temperature and voltage bias variations.

#### J. Ground Bond-Wires

Although the ground bond-wires are connected to the package plate, and the inductance is smaller than the pin bond-wires (close to 500 pH), it decreases the gain of the amplifier and changes the resonance frequency of the  $LC$  tank used in the emitter of  $T_1$ . These effects are considered in the design of the circuit. Also, one of the main reasons for oscillation in PAs is the same ground for the multiple stages (Fig. 10). To overcome this problem, the grounds for the two stages are isolated in the chip layout and have been connected through different bond-wires to the package plate. Also, multiple pads are assigned for grounds to minimize the bond-wire inductance.

## IV. EFFICIENCY IMPROVEMENT TECHNIQUE

### A. On-Chip Envelope Detector and Comparator

As mentioned before, in OFDM systems, due to large PAPR, the signal envelope is mostly below the peak, resulting in a poor efficiency for constant bias class-A PAs. The efficiency of the PA can be improved by adjusting the transistor dc current based on the input signal. Suppose the input envelope is equally

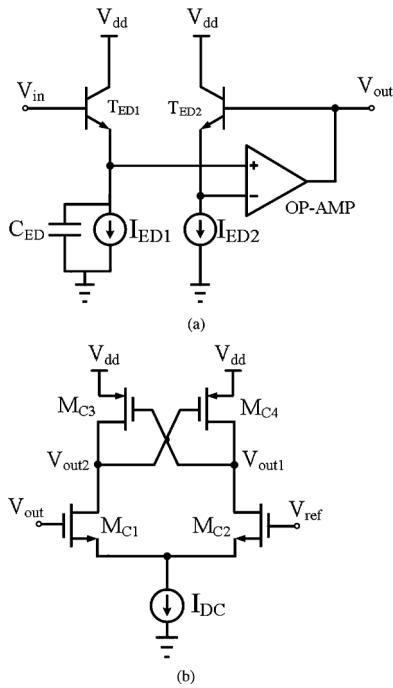


Fig. 11. (a) Schematic of the envelope detector employed in the peak detector. (b) Schematic of the comparator for decision signal generation.

divided into  $N$  different levels which require  $N$ -step biasing schemes and different output loads. If the difference between each two levels is  $\Delta V$ ,  $\Delta V \rightarrow 0$  results in an infinite number of levels with infinite biasing schemes and output loads. This assumption is equivalent to a continuous biasing scheme in which the gate bias is adjusted continuously based on the input envelope. In this case, the PA power consumption is a linear function of the input signal, and, therefore, the PA efficiency will greatly improve. On the other hand, since this approach requires continuous tuning of the matching network, the linearity of the matching network will be very difficult to maintain using analog tuning, since gain matching between all of the levels should be preserved over a wide analog tuning range. Therefore, the overall linearity will be degraded drastically comparing to the two-step biasing scheme based on the envelope detector.

An on-chip envelope detector shown in Fig. 11(a) monitors the input signal level. Transistor T<sub>ED1</sub> acts like a diode, and the OP-AMP forces the base of transistor T<sub>ED2</sub> to follow the emitter of T<sub>ED1</sub>. T<sub>ED2</sub> and I<sub>ED2</sub> are the replicas of T<sub>ED1</sub> and I<sub>ED1</sub> to cancel out the distortion through the OP-AMP [6]. The total power consumption of the envelope detector is 500  $\mu$ A. The output of the envelope detector is compared with a reference voltage, V<sub>ref</sub> (6 dB below the peak input signal) by a comparator shown in Fig. 11(b). This comparator consumes 400  $\mu$ A of current. The comparator output generates a decision signal which determines the appropriate biasing for the transistors by turning on and off the required switches. Fig. 12(a) shows a 4QAM OFDM signal in the time domain generated using MATLAB.<sup>1</sup> The simulated output of the envelope detector and the comparator are shown in Fig. 12(b) and (c), respectively.

<sup>1</sup>[Online]. Available: [http://www.ece.gatech.edu/research/labs/sarl/tutorials/OFDM/Tutorial\\_web.pdf](http://www.ece.gatech.edu/research/labs/sarl/tutorials/OFDM/Tutorial_web.pdf).

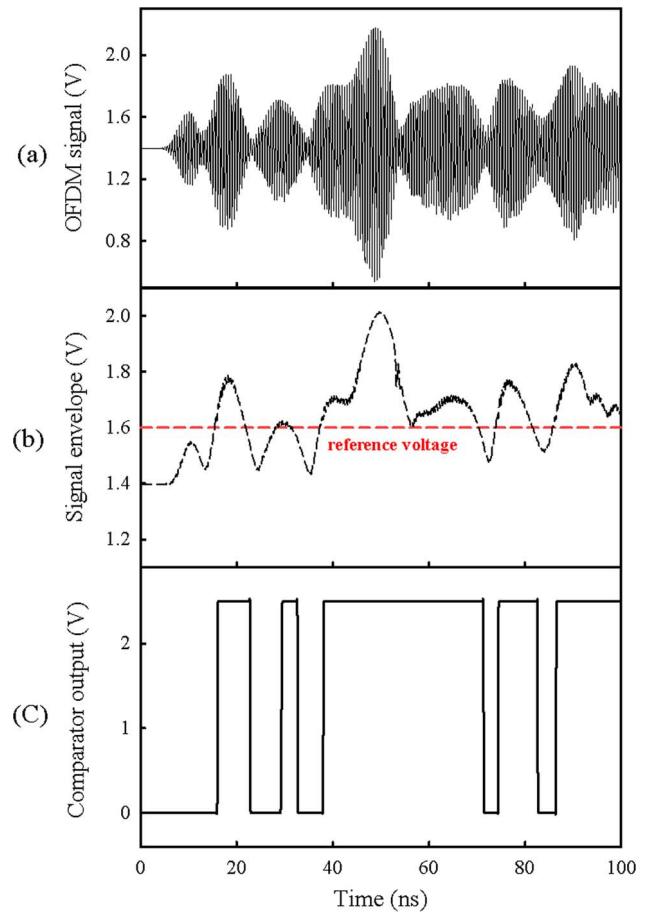


Fig. 12. (a) 4QAM OFDM time-domain signal at the input of the envelope detector. (b) Output signal of the envelope detector. (c) Output of the comparator based on the reference voltage.

### B. Reconfigurable Output Matching Network

Switching to a smaller dc current will reduce the  $g_m$  of the transistors and will cause a drop in the gain. This will cause a discontinuity in the output waveform, and severely degrades the linearity. To keep the gain of the system constant, the output load should be increased to compensate for the  $g_m$  drop. In the high-power mode, the 50- $\Omega$  load is converted to an 8  $\Omega$  load through an on-chip impedance transformer to maintain a gain of 14 dB as shown in (18). To reduce the power consumption in the low-power mode, the dc voltage biasing is decreased for both the preamplifier and the main amplifier. The current consumption of the main amplifier stage is decreased to 52 mA, and the preamplifier to 20 mA. The gain in the low-power mode is as follows:

$$\begin{aligned} \text{Gain} = & [(130 \text{ mS} + 70 \text{ mS}) \times 8] \\ & \times [(25 \text{ mS} \times 21) + (25 \text{ mS} \times 23)] \\ & \cong 1.76 \text{ (5 dB)}. \end{aligned} \quad (21)$$

In order to compensate for this gain drop, the impedance seen from the matching network ( $R_L$ ) should be increased to 25  $\Omega$ . Therefore, the matching network should be able to transform  $R_{50} = 50 \Omega$  to  $R_1 = 8 \Omega$  in the high-power mode and  $R_{50} = 50 \Omega$  to  $R_2 = 25 \Omega$  in the low-power mode based on

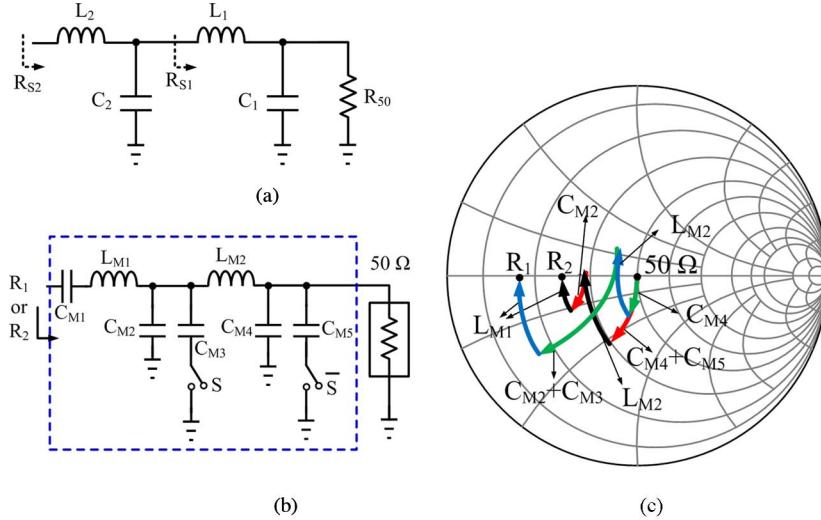


Fig. 13. (a) Low-pass L-match resistive transformer. (b) Schematic of the output matching network. (c) Smith chart of the proposed matching network for the two modes.

the signal generated at the output of the comparator. Considering the low-pass L-match network shown in Fig. 13(a), the input resistance \$R\_{S2}\$, can be calculated as follows (\$Q\_{C1} = \omega\_0 C\_1 R\_{50}\$, \$Q\_{L1} = (L\_1 \omega\_0)/(R\_{L1})\$, \$Q\_{L2} = (L\_2 \omega\_0)/(R\_{L2})\$ and \$\omega\_0 = (1)/(\sqrt{L\_1 C\_1}) = (1)/(\sqrt{L\_2 C\_2})\$):

$$\begin{aligned} R_{S2} &= R_{L1} + \frac{R_{50}}{Q_{C1}^2} \\ &= \frac{L_1 \omega_0}{Q_{L1}} + \frac{R_{50}}{(\omega_0 C_1 R_{50})^2} \end{aligned} \quad (22)$$

$$Q_{C2} = \omega_0 C_2 R_{S1} = \omega_0 C_2 \left( \frac{L_1 \omega_0}{Q_{L1}} + \frac{R_{50}}{(\omega_0 C_1 R_{50})^2} \right) \quad (23)$$

$$\begin{aligned} R_{S2} &= R_{L2} + \frac{R_{S1}}{Q_{C2}^2} \\ &= \frac{L_2 \omega_0}{Q_{L2}} + \frac{R_{S1}}{\left( \omega_0 C_2 \left( \frac{L_1 \omega_0}{Q_{L1}} + \frac{R_{50}}{(\omega_0 C_1 R_{50})^2} \right) \right)^2} \end{aligned} \quad (24)$$

$$R_{S2} = \frac{L_2 \omega_0}{Q_{L2}} + R_{50} \left( \frac{C_1}{C_2} \right)^2 \frac{1}{\frac{R_{50}}{R_{L2} Q_{L1} Q_{L2}} \left( \frac{C_1}{C_2} \right) + 1} \quad (25)$$

$$R_{S2} = R_{L2} + R_{50} n^2 \frac{1}{\frac{R_{50}}{R_{L2} Q_{L1} Q_{L2}} n + 1} \quad (26)$$

where \$n\$ is the ratio between the two capacitors (\$C\_1/C\_2\$) and \$R\_{L\_k}\$ is the resistive loss of the inductor \$k(k = 1, 2)\$, \$Q\_{L1}\$, \$Q\_{L2}\$, \$Q\_{C1}\$ and \$Q\_{C2}\$ are the quality factor of inductors \$L\_1\$, \$L\_2\$, and capacitors \$C\_1\$ and \$C\_2\$, respectively. If the inductors are assumed to be loss less, then the input resistance would be \$R\_{50} n^2\$. Therefore, by changing the ratio of the capacitors, the input resistance can be changed. In practical cases, because of the parasitic of inductors and MIM capacitors, the impedance transformation from 50 to 8 or 25 \$\Omega\$ is really difficult to be achieved just by switching one of the capacitors. The reconfigurable matching network is realized as shown in Fig. 13(b). Both \$C\_{M3}\$ and \$C\_{M5}\$ are switching for accurate resistive transformation in the two

TABLE III  
CALCULATED VALUES FOR THE ELEMENTS EMPLOYED IN THE MATCHING NETWORK

\$C_{M1}\$	\$L_{M1}\$	\$C_{M2}\$	\$C_{M3}\$	\$L_{M2}\$	\$C_{M4}\$	\$C_{M5}\$
7 pF	1.36 nH	0.75 pF	1.35 pF	1.91 nH	0.75 pF	1.55 pF

modes. Due to the large current flow through the matching network, switches are avoided in series configuration. The actual impedance transfer diagram is shown in Fig. 13(c). The inductors in series will cause a 0.5-dBm drop in the output power. The capacitor and inductor values are shown in Table III. The matching network is designed to provide \$R\_1 = 8\$–\$10\ \Omega\$ or \$R\_2 = 23\$–\$25\ \Omega\$ output load for the high and the low input powers, respectively, by digitally calibrating 5-b switch capacitors \$C\_{M2}\$ and \$C\_{M4}\$ to achieve the highest output power. The designed output load range can also be compensated for any gain mismatch between the two modes of the PA and maintain a good linearity in PVT variations. Signal \$S\$ is high for input signal envelopes larger than the reference voltage, while \$\bar{S}\$ is high for envelopes smaller than the reference voltage. Capacitor \$C\_{M1}\$ is used as a dc block.

#### C. Circuit-Level Representation of the Entire PA

In the low-power mode, the larger load resistance \$R\_2\$ can be affected by the transistors small output impedance. Due to large base-collector and gate-drain capacitances added (\$C\_{F1}\$ and \$C\_{F2}\$) for phase equalization at the high-power mode; the output impedance of the main transistors is in the order of \$50\ \Omega\$ at 2 GHz, which will shunt the output current in the low-power mode. Therefore, more dc current needs to be provided by the transistors \$T\_1\$ and \$M\_1\$ to provide the same output power, which degrades the efficiency improvement. By adding a switch in the path of both \$C\_{F1}\$ and \$C\_{F2}\$ and turning both switches “off” in the low-power mode, the output impedance of the main transistors are increased; the associated switches (\$SW\_{CF1}\$ and \$SW\_{CF2}\$)

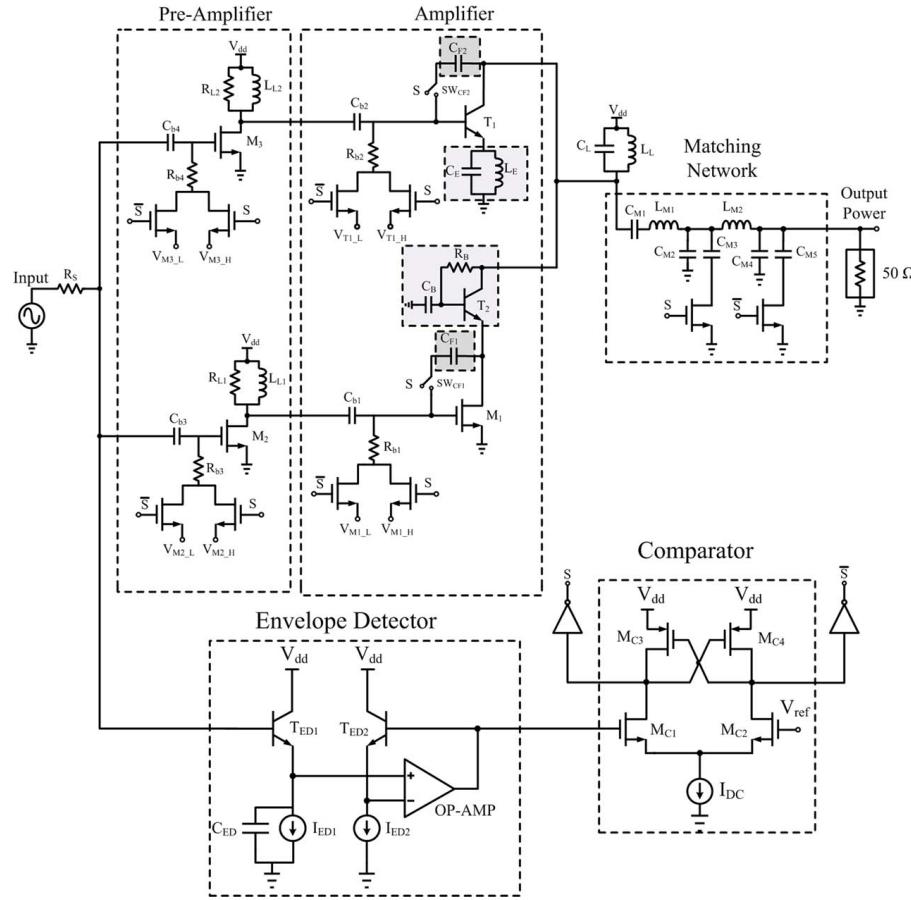


Fig. 14. Circuit-level schematic of the entire PA.

are implemented by transmission gates. The final PA schematic is shown in Fig. 14, where both linearity and efficiency improvement techniques are shown. The envelope of the signal in the OFDM systems varies with a low frequency of the order of 1–10 MHz, the ac coupling capacitors and resistor  $C_{bi}$  and  $R_{bi}$ ,  $i = 1, 2, 3, 4$ , for the biasing of each transistor will form a low-pass filter for the decision signal generated by the comparator. For proper system operation, the cutoff frequency of each low-pass filter should be larger than the frequency variation of the envelope. There is a transient at the input of each stage due to the change of the dc bias values, when the PA operation mode switches. At the input of the preamplifier stage, the bias voltage experiences a smooth first-order transition. For the main amplifier stage, there is some ringing due to the nature of the second order system (due to the inductors in the load of the preamplifier stage). The added parallel resistors ( $R_{L2}$  and  $R_{L1}$  in Fig. 14) lower the quality factor of the second order transition, avoiding any large ringing at the base and the gate of  $T_1$  and  $M_1$ , respectively.  $R_{b3}$  and  $R_{b4}$  are set to be 100 Ohms to provide 50 ohms matching at the input.

#### D. Effect of Switch Nonidealities on the Matching Network

The effect of switch nonidealities in the reconfigurable matching network is considered in high- and low-power modes separately. In high-power mode, switch  $SW_1$  is ON, and  $SW_2$  is OFF, and the output impedance of the matching network ( $R_{S2}$  in Fig. 15) can be written as follows ( $R_{SWk}$  and  $C_{SWk}$

( $k = 1, 2$ ) are the switch on-resistance and the off-state parasitic capacitance):

$$Q_{CM4+C_{SW2}} = \omega_0(C_{M4} + C_{SW2})R_{50}$$

$$Q_{LM1} = (L_{M1}\omega_0)/(R_{LM1})$$

$$Q_{LM2} = (L_{M2}\omega_0)/(R_{LM2})$$

$$C_{M5} \gg C_{SW2}$$

$$R_{S1} = \frac{L_{M2}\omega_0}{Q_{LM2}} + \frac{R_{50}}{(\omega_0(C_{M4} + C_{SW2})R_{50})^2} \quad (27)$$

$$Q_{CM2+C_{M3}} = \omega_0(C_{M2} + C_{M3})R_{S1}$$

$$= \omega_0(C_{M2} + C_{M3})$$

$$\times \left( \frac{L_{M2}\omega_0}{Q_{LM2}} + \frac{R_{50}}{(\omega_0(C_{M4} + C_{SW2})R_{50})^2} \right) \quad (28)$$

and (29), shown at the bottom of the next page.

As shown in (29), the effect of the OFF-state parasitic capacitance can be compensated ( $C_{SW2}$ ) by decreasing  $C_{M4}$ . The switch ON resistance ( $R_{SW1}$ ) appears at the output load ( $R_{S2}$ ) with a factor of  $((C_{M3})/(C_{M2} + C_{M3}))^2$ . Since the output load should be small (10 Ω) in the high-power mode, this resistance should be as small as possible not to affect  $R_{S2}$ . Therefore,  $R_{SW1}$  need to be included in the design of the matching network.

In the low-power mode, switch  $SW_2$  is ON, and  $SW_1$  is OFF. For this case, the switch ON resistance ( $R_{SW2}$ ) in series with

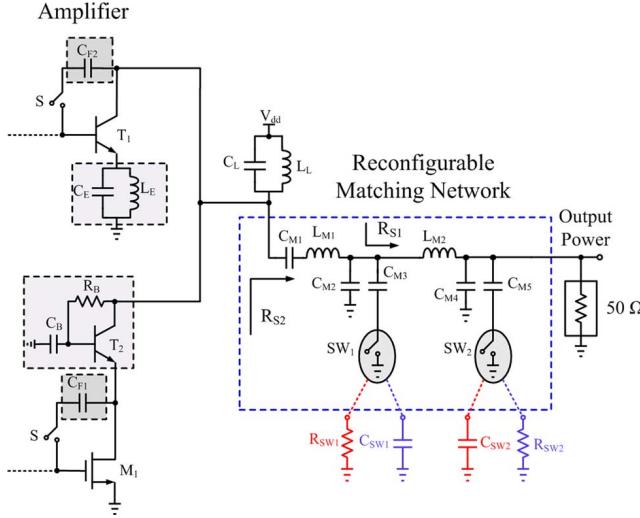


Fig. 15. Reconfigurable matching network to study the effect of the switch nonidealities in both low-power and high-power modes.

the CM<sub>5</sub> capacitor, is translated into a resistance in parallel to the 50-Ω antenna impedance. Therefore, the output load in this mode can be calculated as follows ( $R'_{50}$  is the new antenna impedance):

$$\begin{aligned} Q_{C_{M4}+C_{M5}} &= \omega_0(C_{M4}+C_{M5})R_{50} \\ Q_{LM1} &= (L_{M1}\omega_0)/(R_{LM1}) \\ Q_{LM2} &= (L_{M2}\omega_0)/(R_{LM2}) \\ C_{M3} &\gg C_{SW1} \\ R'_{50} &= R_{50} \parallel \frac{1}{\omega_0^2 C_{M5}^2 R_{SW2}} \end{aligned} \quad (30)$$

$$R_{S2} = \frac{L_{M2}\omega_0}{Q_{LM2}} + \frac{1}{\omega_0^2(C_{M2}+C_{SW1})^2 \left( \frac{L_{M1}\omega_0}{Q_{LM1}} + \frac{R'_{50}}{(\omega_0(C_{M4}+C_{M5})R'_{50})^2} \right)} \quad (31)$$

$$R_{S2} = \frac{L_{M2}\omega_0}{Q_{LM2}} + R'_{50} \left( \frac{C_{M4}+C_{M5}}{C_{M2}+C_{SW1}} \right)^2 \times \frac{1}{\frac{R'_{50}}{R_{LM2}Q_{LM1}Q_{LM2}} \left( \frac{C_{M4}+C_{M5}}{C_{M2}+C_{SW1}} \right) + 1}. \quad (32)$$

As shown in (32), the output load impedance is not too sensitive to the effect of  $R_{SW2}$  in the low power mode. The effect of  $C_{SW1}$ , can be compensated by decreasing capacitor CM<sub>2</sub>. Table IV shows the characteristics of the switches SW<sub>1</sub> and

TABLE IV  
CHARACTERISTIC OF THE SWITCHES SW<sub>1</sub> AND SW<sub>2</sub> IN THE MATCHING NETWORK OF FIG. 14

SW <sub>1</sub>		SW <sub>2</sub>	
R <sub>ON</sub>	C <sub>OFF</sub>	R <sub>ON</sub>	C <sub>OFF</sub>
1.7 Ω	730 fF	3.2 Ω	280 fF

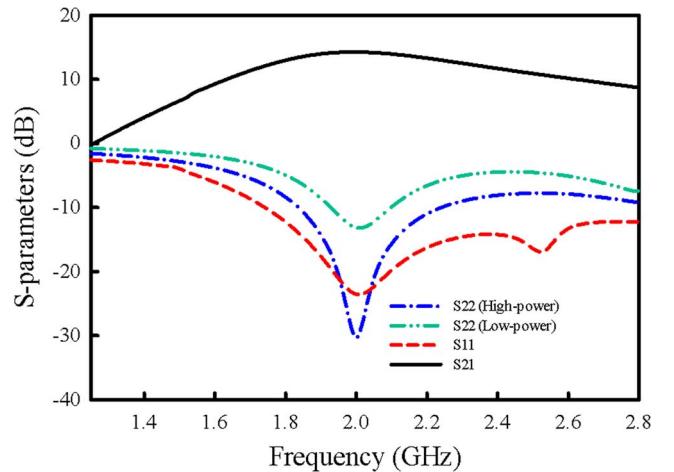


Fig. 16. Simulated S-parameters for the proposed PA.

SW<sub>2</sub> in the matching network in Fig. 15. The effect of parasitic capacitance has been absorbed in C<sub>M2</sub> and C<sub>M4</sub> capacitors. The switch on resistance will also affect the output power level, and this loss will degrade the output power by 0.3 dB. Therefore, the total loss of the reconfigurable matching network increases to 1.5 dB. The two-tone test simulation (1-MHz frequency spacing) has been performed to investigate the effect of the switch nonidealities on the PA performance. The IM<sub>3</sub> level degrades by less than 0.5 dB for 20-dBm average output power, by adding the switches to the reconfigurable matching network.

#### E. S-Parameter Evaluation of the PA

The input port of the PA is matched to 50 Ω through the biassing resistors R<sub>b3</sub> and R<sub>b4</sub> in Fig. 14. S-parameter simulations have been performed (PSS and PSP analysis in Cadence Spectre) to simulate the frequency response of the PA over the desired band. Fig. 16 shows the input return loss versus frequency. The input matching shows a narrowband response due to the feedback from the LC tank load of the preamplifier stage through the gate-drain parasitic capacitance.

The output return loss depends on the PA operation mode. To determine the output return loss, the output impedance of the PA without the matching network should be calculated for both modes of operation. As shown in Fig. 17, this impedance

$$R_{S2} = \frac{L_{M1}\omega_0}{Q_{LM1}} + \frac{1}{\omega_0^2(C_{M2}+C_{M3})^2 \left( \frac{L_{M2}\omega_0}{Q_{LM2}} + \frac{R_{50}}{(\omega_0(C_{M4}+C_{M5})R_{50})^2} \right)} + \left( \frac{C_{M3}}{C_{M2}+C_{M3}} \right)^2 R_{SW1} \quad (29)$$

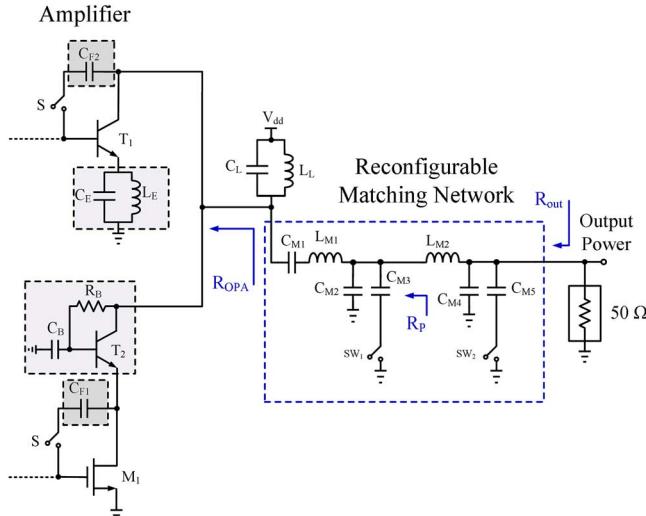


Fig. 17. Reconfigurable matching network.

( $R_{OPA}$ ) is translated into the impedance of  $R_{out}$  through the matching network. If the effect of the capacitor loss compared with inductor loss is neglected, the output return loss is then calculated as follows:

$$R_P = Q_{LM1}^2 R_{OPA} \quad (33)$$

$$Q_{L1} = \frac{L_{M1}\omega_0}{R_{OPA}} \quad (34)$$

$$R_{out} = Q_{LM2}^2 R_P \quad (35)$$

$$Q_{L2} = \frac{L_{M2}\omega_0}{R_P} \quad (36)$$

$$R_{out} = \left( \frac{L_{M2}}{L_{M1}} \right)^2 R_{OPA} \quad (37)$$

For high-power mode,  $R_{OPA} = 25 \Omega$ . Because of the matching network, we have

$$R_{out} = \left( \frac{1.91 \text{ nH}}{1.36 \text{ nH}} \right)^2 25 = 49.3 \Omega \quad (38)$$

$$S_{22} = 20 \times \log \left( \frac{50 - 49.3}{50 + 49.3} \right) = -39 \text{ dB}. \quad (39)$$

For low-power mode,  $R_{OPA} = 45 \Omega$ . Because of the matching network, we have

$$R_{out} = \left( \frac{1.91 \text{ nH}}{1.36 \text{ nH}} \right)^2 45 = 88.7 \Omega \quad (40)$$

$$S_{22} = 20 \times \log \left( \frac{88.7 - 50}{50 + 88.7} \right) = -11.7 \text{ dB}. \quad (41)$$

Therefore, the output return loss is really small for the high-output-power mode, which is more critical than the low-power mode. Fig. 16 shows the simulated  $S_{22}$  of the PA when the PA operates in both high-power and low-power modes. As expected,  $S_{22}$  degrades in low-power mode, the simulation results are in close agreement with the mathematical derivations. The simulated gain ( $S_{21}$ ) of the PA is also shown in Fig. 16. Since the entire matching network and the output loads are implemented on-chip, the 3-dB bandwidth of the PA is around 700 MHz.

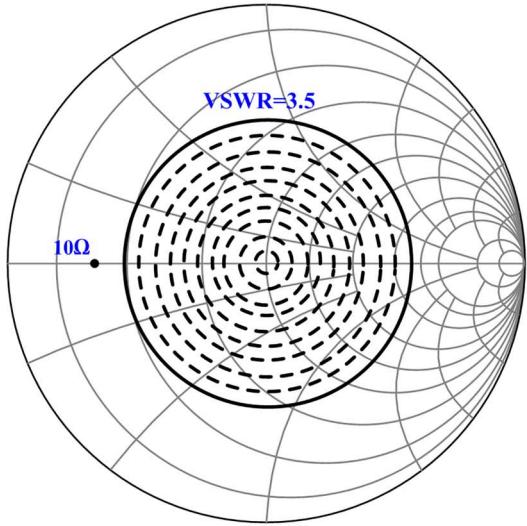
#### F. Load Mismatch Analysis

One of the critical factors in handset PAs that impacts linearity, power efficiency, and maximum output power is the load impedance mismatch. As the handset is used in different positions, the antenna load no longer provides the nominal input impedance of  $50 \Omega$ , and it varies within a certain voltage standing wave ratio (VSWR) circle in the smith chart. In order to evaluate the PA performance under load mismatch conditions, the translated antenna load through the reconfigurable matching network has been derived for different antenna loads. The matching network provides  $10 \Omega$  for high-power mode and  $25 \Omega$  for low-power mode. As long as the matching network adapts itself to provide the same output load in two modes under mismatch condition, the PA performance will be preserved. The matching network consists of two cascaded L networks. Assuming all of the capacitors ( $C_{M2}$ ,  $C_{M3}$ ,  $C_{M4}$ , and  $C_{M5}$ ) are tunable by changing the ratio between the two capacitors  $C_{M2} + C_{M3}$  over  $C_{M4}$  in the high-power mode, and  $C_{M2}$  over  $C_{M4} + C_{M5}$  in the low-power mode, the load mismatch effect can be compensated within a certain VSWR circle. Simulation results in Fig. 18(a) and (b) show that all of the impedances inside the  $VSWR = 3.5 : 1$  circle are matched to  $10 \Omega$  in the high-power mode, while the tuning range is decreased to  $VSWR = 1.9 : 1$  in the low-power mode since it is matched to  $25 \Omega$ .

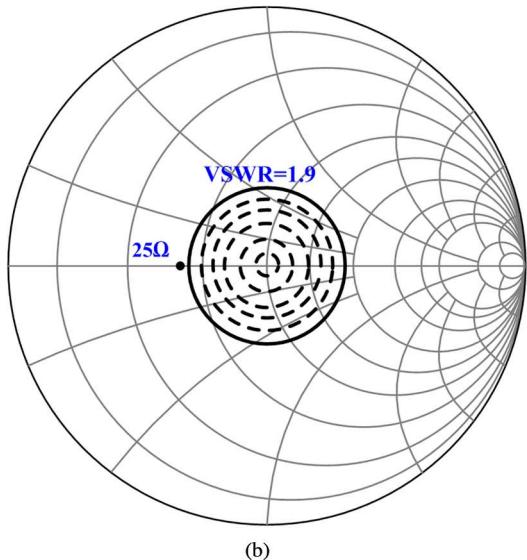
#### G. Effect of Timing Misalignment on Linearity Performance

There are three switching blocks in the PA, two for switching the bias values of the preamplifier and the main amplifier, and one for switching the reconfigurable matching network. These blocks should be switched based on the input signal timing pattern in each stage. Fig. 19 shows the possible delays between the PA stages,  $\tau_{a1}$  is the delay of the input RF signal between preamplifier and the main amplifier stage, and  $\tau_{a2}$  is the delay of the RF signal between the amplifier and the matching network.  $\tau_{s1}$  is the delay of the decision signal, between the output of the comparator and the main amplifier, and  $\tau_{s2}$  is the delay of the decision signal between the main amplifier and the matching network. If  $\tau_{a1} = \tau_{s1}$ , and  $\tau_{a2} = \tau_{s2}$  the PA performance would be preserved. On the other hand, if the delays are not equal, for example, if  $\tau_{a2} < \tau_{s2}$ , then the amplifier switches to the low-power mode, while the matching network is still in the high-power mode. Therefore, the gain drops until the matching network is switched to the low-power state as well. This will cause signal discontinuity at the output, which degrades the linearity.

The output of the comparator will be directly applied to the preamplifier stage. This signal is routed throughout the chip until it switches the amplifier stage, and finally it switches the matching network. The effect of  $\tau_{s1}-\tau_{a1}$ , and  $\tau_{s2}-\tau_{a2}$  delays on IM<sub>3</sub> and IM<sub>5</sub> levels has been simulated. Fig. 20 shows the simulation results of the two-tone test, for the two delays and frequency spacing of 10 MHz. As can be seen, the system is more sensitive to the delay  $\tau_{s2}-\tau_{a2}$ , particularly the IM<sub>5</sub> level degrades as the delay increases. The delays up to 3 ns can be tolerated for a 10-MHz input signal envelope. The effect of the delay for lower frequency signal envelopes is smaller, and the linearity of the PA is not too sensitive as the envelope frequency



(a)



(b)

Fig. 18. (a) VSWR circle matched to  $10\Omega$  for the antenna load mismatch inside the circle (high-power mode). (b) VSWR circle matched to  $25\Omega$  for the antenna load mismatch inside the circle (low-power mode).

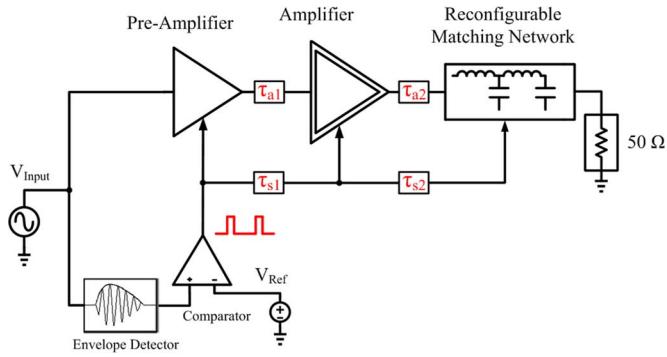


Fig. 19. Timing delays between different stages of the PA.

decreases. In order to apply the comparator output, and the RF signal to each stage simultaneously, the routing of the input RF signal and the switching signal has been performed along with each other throughout the entire chip. By careful layout and

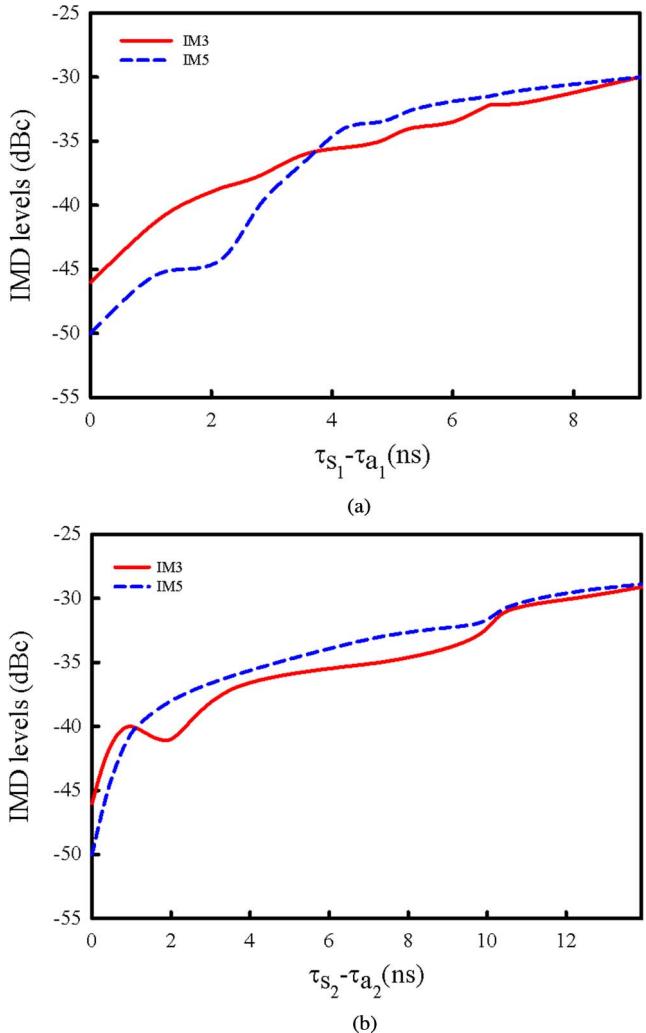


Fig. 20. Effect of timing misalignment on PA linearity performance. (a)  $\tau_{s1} - \tau_{a1}$ . (b)  $\tau_{s2} - \tau_{a2}$ .

post layout simulations, the delays between the two signals are minimized.

#### H. Automatic Gain Calibration

The most important mismatch factor in the linearity performance of the PA is the gain mismatch between the two modes of operation. To adjust the gain using an automatic calibration mechanism, two different signal amplitudes can be applied to the PA at low-power and high-power modes, respectively, and the biasing values are adjusted until equal gains in both modes are achieved. This can be performed with the aid of the available DSP unit required for OFDM modulation. The block diagram of the automatic gain adjustment is shown in Fig. 21. The biasing values are set for low-power or high-power mode through the DSP as follows: in the PA initial setup for gain matching calibration, a single tone signal is up-converted to the frequency of operation. By turning on the switch  $S_1$  at the output of the PA, the signal is down-converted back to the DSP by employing a replica of the up-conversion mixer. Therefore, the gain of the PA can be measured directly using the DSP for each mode of operation, and then the biasing values are adjusted to achieve the best gain matching in the two modes, which translates to better linearity. After the calibration is performed, the switch

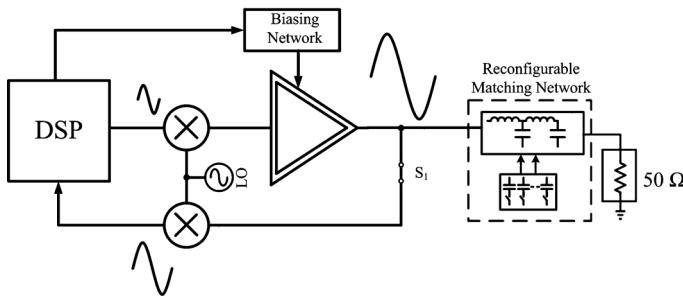


Fig. 21. Block diagram of the gain mismatch automatic calibration.

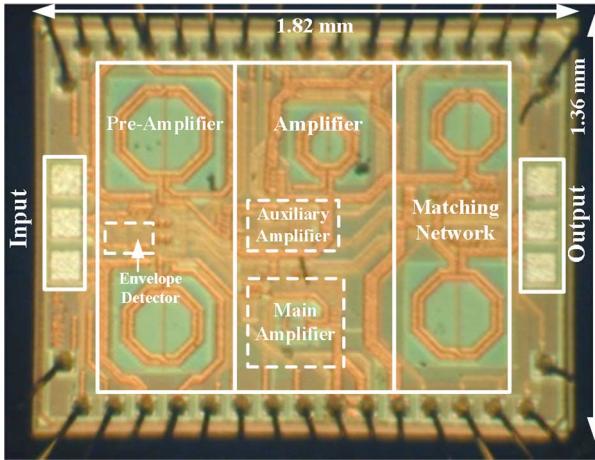


Fig. 22. Die micrograph of the fabricated PA in  $0.25\text{-}\mu\text{m}$  BiCMOS Technology.

$S_1$  is turned off, and the PA works with an OFDM modulated signal generated by the DSP Unit.

## V. MEASUREMENT RESULTS

The PA has been fabricated using  $0.25\text{-}\mu\text{m}$  SiGe:C BiCMOS Technology from NXP semiconductors.<sup>2</sup> All of the components including the matching network and the envelope detector are integrated and no off-chip element has been used. The PA is designed to be single-ended to avoid any baluns in the circuit. The chip has been open-packaged using a 56-pin HVQFN package. To remove the effect of the package parasitic and bond-wire inductance, ground-signal-ground (GSG) RF probes are landed on the input and output pads. The die micrograph is shown in Fig. 22 with the dimensions of  $1820\text{ }\mu\text{m} \times 1360\text{ }\mu\text{m}$ , including the wire-bonding pads. Supply voltages for the main amplifier and the preamplifier are 2.5 and 1.7 V, respectively.  $S$ -parameter measurements have been performed for the designed PA using the Agilent N5230A PNA series network analyzer, and the results are shown in Fig. 23. The measured gain of the PA is 13 dB, which is 1 dB lower than the simulation results. The gain drop is mostly because of inaccurate modeling of the ground bond-wires. The 3-dB gain BW is around 600 MHz, and the maximum output power is at 2.03 GHz. The input match is better than  $-9.5$  dB in the desired frequency band. The input matching has a frequency shift; this shift is mostly because of the effect of the bond-wires through the switches for

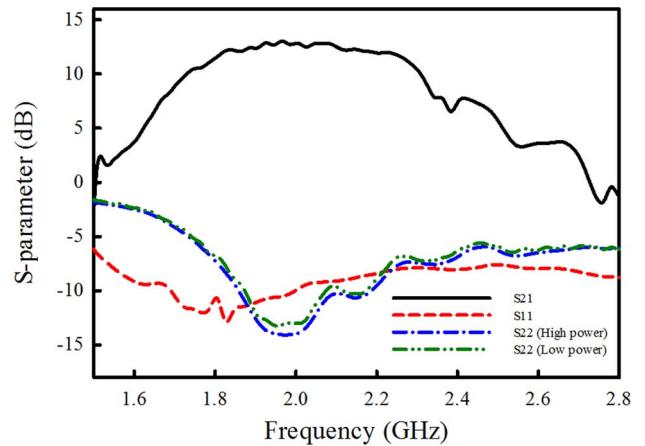


Fig. 23. Measured  $S$ -parameters for the designed PA.

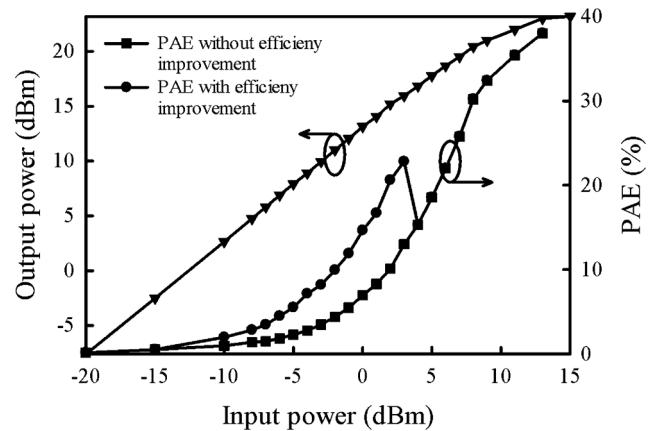


Fig. 24. PA output power and PAE measurement results versus the input power. PAE is shown with and without efficiency improvement technique.

two different biases. The output matching for high-power and low-power modes is better than  $-14$  and  $-13$  dB, respectively, in the desired frequency band (2 GHz).

The input signal is swept from  $-20$  to  $13$  dBm, while the output power is monitored using a spectrum analyzer. Fig. 24 shows the output power and the PAE of the PA versus the input power. Output  $P_{1\text{ dB}}$  of the PA is  $21$  dBm with PAE of  $32\%$ . The saturating output power is  $23$  dBm in which the PAE is increased to  $38\%$ . Since  $P_{1\text{ dB}}$  happens to be at  $9\text{-dBm}$  input power (the peak input power), the system is switched to a low-power mode when the input is  $6$  dB lower than the peak input power, or  $3$  dBm, in which there is a small difference between the output powers at the transition ( $<0.2$  dB). For  $21\text{-dBm}$  output power, the measured current consumption for the amplifier and preamplifier stages are  $110$  and  $40$  mA, respectively. The current consumption lowers down to  $54$  and  $22$  mA for  $15\text{-dBm}$  output power. The PAE at  $6$  dB back-off from  $P_{1\text{ dB}}$  is  $23\%$ , therefore the efficiency improvement employing switching biasing technique is more than  $10\%$ .

The linearity of the PA is measured first by employing the two-tone test. The tones are located at  $2.03$  GHz with a  $1\text{-MHz}$  space. The bias values of each transistor are tuned for the maximum  $\text{IM}_3$  cancellation for the highest output power. Fig. 25 shows the measurement results for the output  $\text{IM}_3$  and  $\text{IM}_5$

<sup>2</sup>[Online]. Available: <http://www.nxp.com/>.

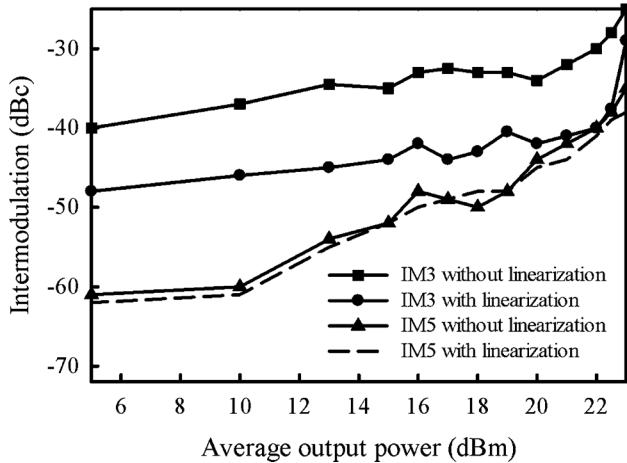


Fig. 25. Measured difference between fundamental tone IM<sub>3</sub> and IM<sub>5</sub> in dBc in a two-tone test with 1-MHz spacing at 2.03 GHz with and without linearization technique.

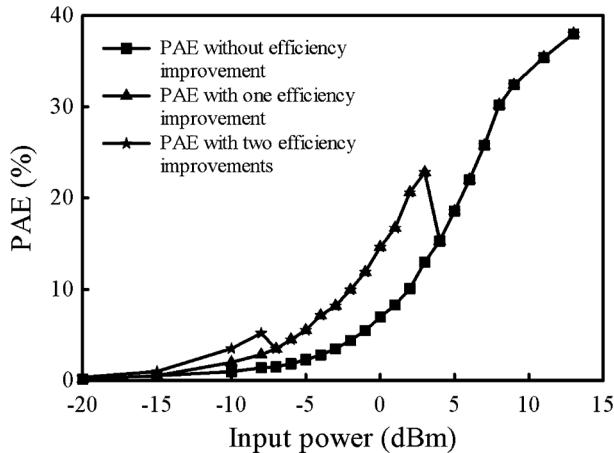


Fig. 26. PAE measurement results versus the input power with different efficiency improvement techniques compared to a fixed bias PA.

versus the average output power. The IM<sub>3</sub> and IM<sub>5</sub> are 41 and 44 dB below the fundamental tone for the entire nonsaturated output power. By turning off the transistor M<sub>1</sub>, IM<sub>3</sub> is increased by more than 10 dB, which shows the effectiveness of the feed-forward cancellation approach. The two-tone test has also been performed for 10-MHz frequency spacing, and the results are very close to the 1-MHz frequency spacing with a small degradation in IM<sub>3</sub> cancellation (less than 1 dB). Since the main amplifier transistors, T<sub>1</sub> and M<sub>1</sub> are in class-AB region, the level of the IM<sub>5</sub> is not small, and as the linearization technique is tuned for IM<sub>3</sub> cancellation, minor improvement can be seen at the output power IM<sub>5</sub>. An extra nMOS transistor can be added to the output in parallel to T<sub>1</sub> and M<sub>1</sub> [26], with a certain biasing for each mode of operation. By characterizing the biasing and the size of the added transistor, the IM<sub>5</sub> level at the output can also be cancelled out to further improve linearity, error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR).

For the low input powers ( $P_{in} < -8$  dBm) the  $g_m$  of T<sub>1</sub> is almost six times larger than its nMOS counterpart (M<sub>1</sub>) and it provides most of the gain. On the other hand, the linearity of T<sub>1</sub> is sufficient for the low input power levels since the IM<sub>3</sub> levels

are small at the output (below -45 dBc). Therefore, for further improvement of the PAE, M<sub>1</sub> and the preamplifier transistor M<sub>2</sub>, can be turned off without sever degradation in the linearity performance of the PA. As shown in Fig. 26, this will result in further efficiency improvement in larger power back-offs.

Fig. 27(a) and (b) show the time-domain signals for the two-tone test. Fig. 27(a) shows a smooth transition which is accomplished by achieving an equal gain between the two modes, while in Fig. 27(b) a mismatch is intentionally applied between the two modes by introducing mismatch in the voltage biases. As a result, the gain in the low-power mode is higher than the gain in the high-power mode. IM<sub>3</sub> level is degraded from -40 to -26 dBc with introducing the mismatch [Fig. 27(c) and (d)]. These results prove the effectiveness of the reconfigurable matching network technique to improve linearity and efficiency by setting the gains of the two modes of the PA to be equal.

The EVM has been measured to determine the linearity of the designed PA using the IEEE 802.16e WiMAX standard with OFDM 64-QAM modulation at a carrier frequency of 2 GHz (Fig. 28). For WiMAX standard, 56 Mbps and 10-MHz channel bandwidth PAPR is around 12 dB. The average rate for a 10-MHz WiMAX packet varies between 1–15 MHz, and the stages are switched with the same rate. The measured EVM is below -30 dB for the output powers below 15.5 dBm. Fig. 29 shows the measured output spectrum of the PA for 14-dBm output power, ACLR of -36 dBc is achieved. Also, the average efficiency of the PA with efficiency improvement technique at -28 dB EVM (15.9-dBm average output power) is 19%, which drops to 11% as the efficiency technique is switched off. In order to realize how much improvement is achieved by using the IM<sub>3</sub> cancellation technique, ACLR and EVM have also been measured without applying the linearization technique as shown in Figs. 28 and 29. To measure ACLR and EVM without linearization technique, the nMOS path is turned off by grounding the biasing values. Since turning off one path, drops the output power by 5–6 dB, for fair comparison, the PA gain is increased by increasing the bias values in the bipolar path. In order to only observe the effect of linearization technique, the reference voltage in the comparator is set to maximum value to avoid the effect of reconfigurable matching switching and gain mismatch on linearity. As can be seen in Fig. 29, the ACLR improves from -31 to -36 dBc using the IM<sub>3</sub> cancellation technique for a 10-MHz bandwidth WiMAX 64QAM signal with 14-dBm average output power. The EVM is also measured for different output powers, and the linearization technique improves the EVM by 4.5 dB at 14-dBm average output power.

As discussed before, the gain of the PA in the low- and high-power modes needs to be matched. Any gain mismatch between the two operating modes degrades the linearity performance of the linearized PA. On the other hand, maintaining equal gains in both modes is really challenging due to PVT variations. In order to evaluate the performance of the PA under gain mismatch, several measurements have been performed. Gain mismatch is achieved by changing the bias values and reconfigurable matching network. Fig. 30(a) shows the effect of gain mismatch on IMD levels at 20-dBm output power, the IM<sub>3</sub> levels are still below -36 dBc for 1.3-dB gain mismatch while the total PA gain is 13 dB. Fig. 30(b), and (c) shows the EVM

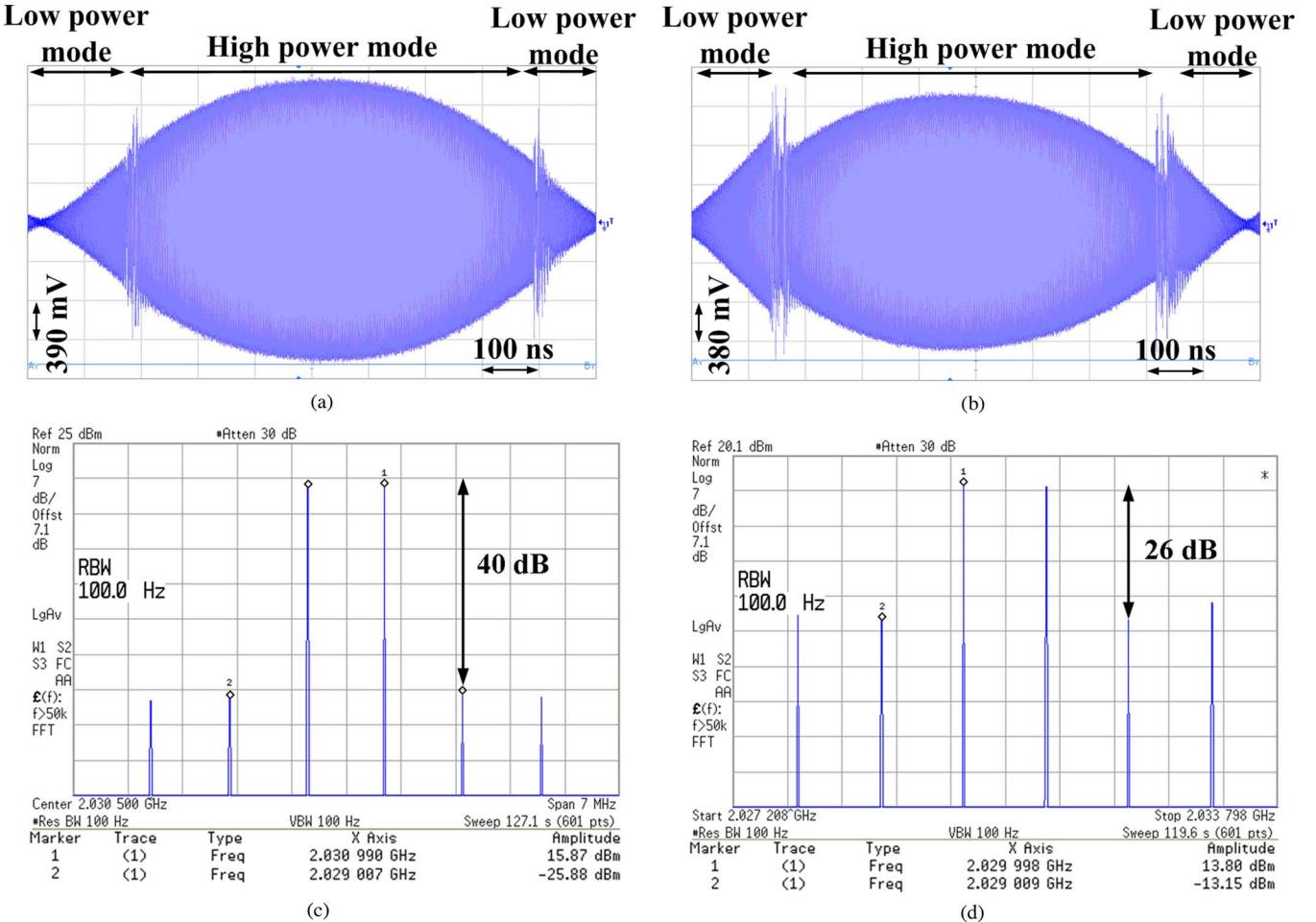


Fig. 27. Time-domain measurement of the two tone test with 1-MHz spacing at 2.03 GHz. (a) Equal gain in the transition between the two modes. (b) Unequal gain in the transition between the two modes. (c) Spectrum of the signal at (a). (d) Spectrum of the signal at (b).

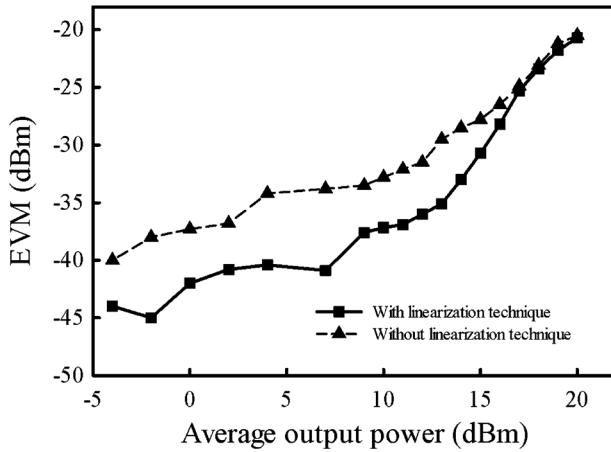


Fig. 28. Measured EVM as a function of average output power for WiMAX standard with 64QAM modulation and 10-MHz signal bandwidth with and without linearization technique.

and ACLR performance under gain mismatch for a WiMAX 64QAM signal ( $BW = 10$  MHz) with 14- and 10-dBm output power, respectively. For 14-dBm output power, the EVM degrades by 3 dB in 1.2-dB gain mismatch. For 10-dBm output power, the EVM under gain mismatch up to 2.8 dB is always below  $-30$  dB. The gain mismatch of 1.2 dB also degrades

ACLR by 4 dB at 14-dBm output power, while for 10-dBm output power the ACLR is always below  $-36$  dBc for gain mismatch up to 2.8 dB.

In Table V, the performance of the PA is compared with recently reported linear efficient PAs. Based on the comparison, it is concluded that the implemented PA has a superior performance compared with the state of the art in case of linearity and efficiency in both 1-dB compression point and power backoffs. In case, the technology could tolerate a larger power supply, the output power, and the average PAE would be increased with the same EVM achieved for WiMAX 64QAM signal with 10-MHz BW.

## VI. CONCLUSION

In this paper, a fully integrated linear and efficient PA in  $0.25\text{-}\mu\text{m}$  SiGe:C BiCMOS technology is presented. A new technique based on reconfigurable matching network has been proposed to improve the efficiency at power backoffs. The efficiency is improved by decreasing the dc bias values during the low input power signal, which has a higher probability over high input power during normal operation. To maintain the same gain during the transition from low to high input power, an on-chip reconfigurable matching network is implemented.

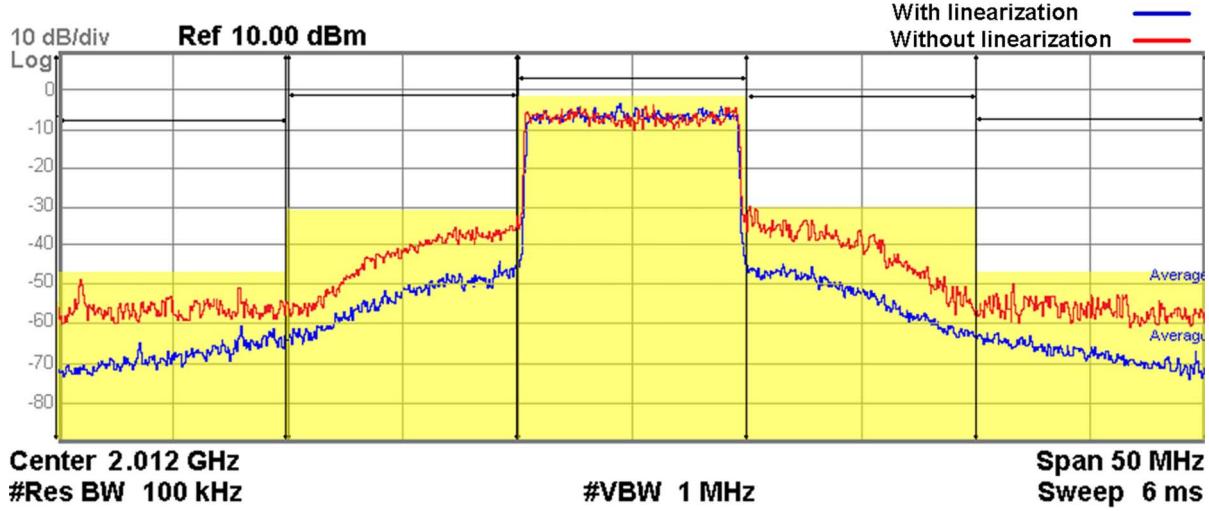


Fig. 29. Output spectrum of the PA excited for WiMAX standard with 64QAM modulation and 10-MHz signal bandwidth (14-dBm average output power) with and without linearization technique.

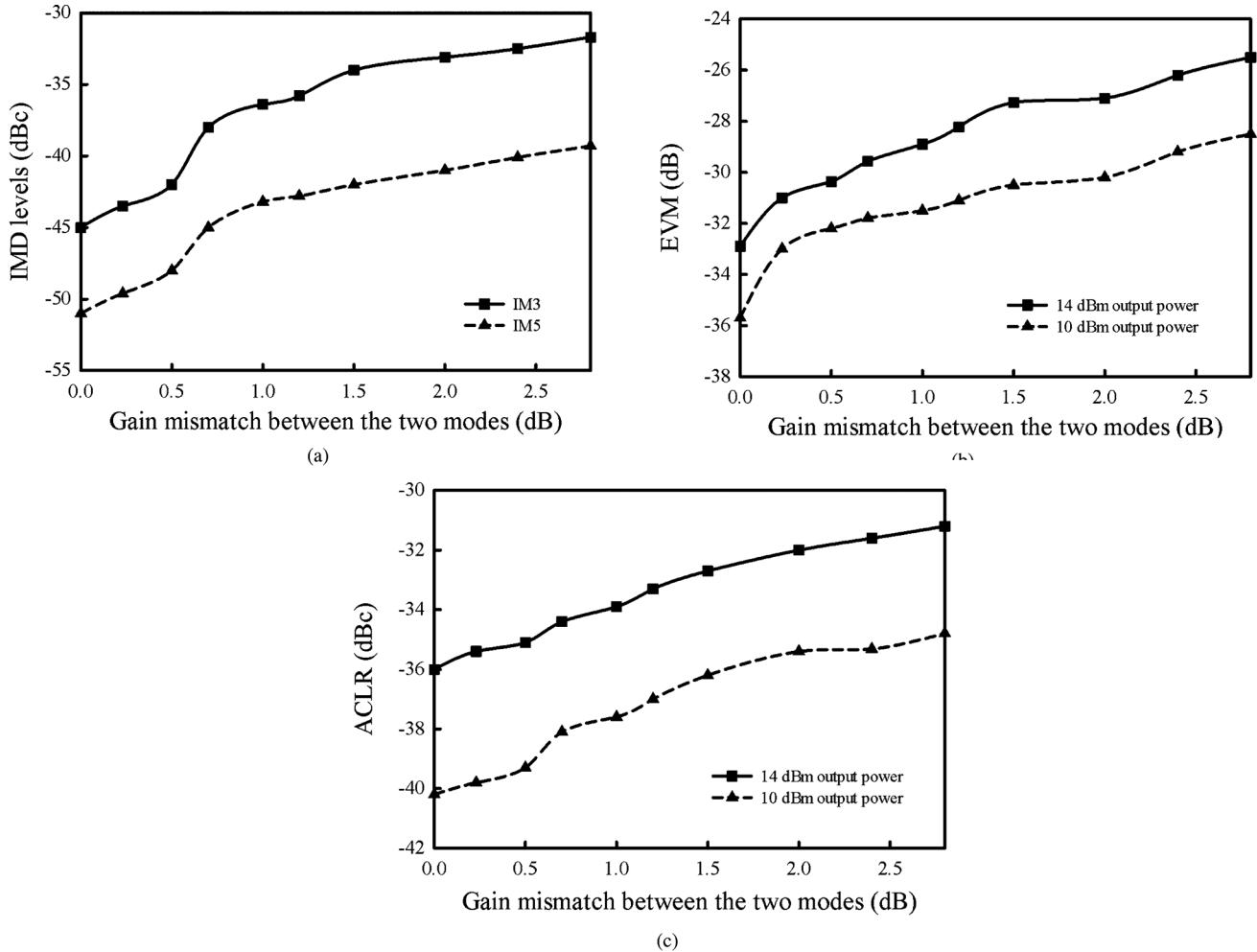


Fig. 30. Effect of gain mismatch between the two PA operating modes on linearity performance, (a) IMD levels under gain mismatch, (b) EVM under gain mismatch for a WiMAX 64QAM 10 MHz signal bandwidth with 14 and 10 dBm average output power, (c) ACLR under gain mismatch for a WiMAX 64QAM 10 MHz signal bandwidth with 14 and 10 dBm average output power.

Using this technique, the efficiency is improved by 10%. The linearity is greatly improved by adding a linearizer nMOS transistor to the main BJT to cancel out  $g_{m3}$ . A second-harmonic

current degradation is used to improve both output power and the linearity. By adding this feed-forward path, the  $IM_3$  of the PA is 41 dB below the fundamental during the entire output

**TABLE V**  
PERFORMANCE SUMMARY AND COMPARISON OF THE LINEARIZED EFFICIENT PA COMPARED WITH THE STATE-OF-THE-ART PA DESIGNS

	Technology	Frequency (GHz)	Power Supply (V)	Gain (dB)	P <sub>1dB</sub> (dBm)	PAE (%)		Inter-modulation levels at P1dB			EVM @ average P <sub>out</sub>	Average PAE (%)	Modulation (Signal BW)
						P <sub>1dB</sub>	6dB BO	IM <sub>3</sub> (dBc)	IM <sub>5</sub> (dBc)				
[9] <b>JSSC 04</b>	0.5 μm CMOS	1.75	3.3	21	20.2	13.5	5	-45	N/A	-	-	-	
[10] <b>JSSC 05</b>	0.18 μm CMOS	N/A	N/A	12	20	36	15	-25	N/A	-25 dB @ 14.5 dBm	-	-	
[12] <b>JSSC 06</b>	0.18 μm CMOS	2.45	2.5	18.9	20.2	35	13	-28	-45	-	-	-	
[13] <b>JSSC 06</b>	0.18 μm CMOS	2.45	N/A	17.5	20.5	37	14	-27	-43	-27 dB @ 15 dBm	14	WLAN 64QAM (20 MHz)	
[27] <b>JSSC 07</b>	0.18 μm SiGe BiCMOS	2.4	3.3	11	25	30	13	-	-	-26 dB @ 20dBm	28	WLAN 64QAM (20 MHz)	
[14] <b>JSSC 08</b>	0.18 μm CMOS	2.4	1.2	17	24	31.5*	16*	-29**	-36**	-27 dB @ 14.5 dBm	9*	WLAN 64QAM (200KHz)	
[15] <b>JSSC 09</b>	90 nm CMOS	2.4	3.3	28	28	25	14	-34***	-42***	-25.3 @ 22.7 dBm	12.4	WiMAX 64QAM (10 MHz)	
[28] <b>JSSC 09</b>	0.13 μm SOI CMOS	1.92	1.2	15	-	-	-	-	-	-36.47 @ 15.3 dBm	22	WiMAX 64QAM (5MHz)	
[29] <b>TCASI 11</b>	0.18 μm SiGe BiCMOS	2.3	4.2	10.5	20	49	10	-	-	-26.19 @ 17.4 dBm	30.5	WiMAX 64QAM (8.75 MHz)	
[16] <b>JSSC 11</b>	0.18 μm CMOS	2.5	3.3	31.3	28	30	19	-	-	-31 @ 17 dBm	8	WLAN 64QAM (10 MHz)	
<b>This Work</b>	0.25 μm SiGe:C BiCMOS	2	2.5	13	21	32	23	-41	-44	-30.7 @ 15 dBm	16	WiMAX 64QAM (10 MHz)	

\* Drain Efficiency

\*\* At 18 dBm output power

\*\*\* At 23 dBm output power

power, which shows 10-dB improvement compared with the case of a single bipolar transistor. P<sub>1dB</sub> of the PA is 21 dBm with a PAE of 32%. By employing the linearization technique, EVM and ACLR are improved by 4.5 and 5 dB, respectively, for a WiMAX 64QAM signal at 14-dBm average output power. By increasing the number of comparator levels, the input signal will be divided into more levels. Therefore, the PA will have more modes of operation each with a specific biasing value, and the output load provided by the reconfigurable matching network. By increasing the number of PA operation modes, the power consumption will be a more linear function of the input signal; therefore, the PAE will increase at the price of having a more challenging reconfigurable matching network. Also, the automatic gain control loop can be added to the PA to tune the gain in different modes to achieve the best gain match, which will result in a better linearity.

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Caen.

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