A Wideband Voltage Mode Doherty Power Amplifier

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***Abstract*—This paper presents a new wideband Doherty Amplifier technique that can achieve high efficiency while maintaining excellent linearity. By modifying a "forgotten" topology originally proposed by Doherty, a new Doherty Amplifier architecture is realized with two voltage mode PAs and transformers, thus eliminating a narrowband impedance inverter. The voltage mode PA is implemented with a switched capacitor PA known for its excellent linearity. The PA is fabricated in 65 nm low-leakage CMOS and achieves 24 dBm saturated power (at standard supply voltage) with 45%/34% PAE at peak and 5.6dB back-off over 750 MHz to 1050 MHz 1dB bandwidth. With memory-less linearization, this PA can transmit 40 MHz 256-QAM 9dB PAPR 802.11ac modulation centered at 900 MHz meeting the spectral mask with measured EVM of -34.8dB and 22% PAE without backing-off or equalization.**

***Index Terms*—CMOS technology, Doherty power amplifier, transformer, polar transmitter, RF DAC, SCPA.**

I. Introduction

In modern communication systems, the need for high spectral efficiency and wide bandwidth in multi-path channels has led to the use of high peak to average power ratio (PAPR) modulation. Since conventional PAs only operate efficiently at peak power, having high peak efficiency is no longer enough to maintain high overall efficiency. Moreover, achieving an acceptable bit-error rate for spectrally efficient modulation puts a stringent linearity requirement on the PA. The 802.11ac standard requires overall Tx EVM of better than -32dB when transmitting 256-QAM symbols. Maintaining high linearity usually requires operating the PA at back-off, degrading the efficiency even further. While the classical Doherty Amplifier greatly improves power back-off (PBO) efficiency, the linearity degrades. This degradation in linearity requires the PA to operate in further back-off preventing it from achieving its full efficiency enhancement potential, especially with recent modulation standards. In this work, a new wideband Doherty technique that enhances PBO efficiency while maintaining excellent linearity is presented.

II. Previous Architectures

A. Classical Doherty Amplifier

The classical Doherty Amplifier [1] consists of two current-mode PAs (Main and Peaking) and an impedance inverter as shown in Fig. 1a. The impedance inverter lowers the impedance at the Main PA when the Peaking PA turns on, providing efficiency peaking at 6dB back-off (Fig. 1b). This structure suffers from narrow bandwidth at 6dB back-off due to the impedance inverter bandwidth [2].

In [1] Doherty proposed that a "hypothetical" voltage source (not efficiently realizable at the time) and a current source driving a balanced load can achieve back-off efficiency enhancement (Fig 1c). One can also show that two voltage sources driving a balun can achieve the same effect (Fig 1d). Recent advances in CMOS technology and PA architecture [5] allows implementation of a high efficiency voltage mode amplifier at GHz frequencies. Therefore, it is now possible to implement a wideband impedance inverter-less Doherty amplifier. Due to the low output impedance of the main and peaking PAs in this architecture, we refer to it as "Voltage Mode Doherty".

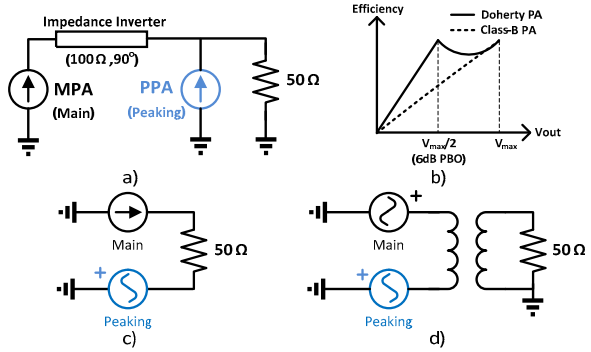

Fig.1. a) Classical Doherty; b) Efficiency vs Output Voltage; c) Voltage-Current Doherty Amplifier; d) Voltage Mode Doherty

III. Proposed Architecture

A. Voltage Mode Doherty (VMD)

Our proposed architecture consists of two voltage-mode PAs and a transformer (Fig. 1d). In this architecture, the output voltage amplitude of each PA can be independently controlled to enable power back-off efficiency enhancement as shown in Fig. 2. At low power, the peaking PA is off, the main PA sees high impedance (50Ω) causing the main PA to saturate at 6dB back-off. As the peaking PA is turned on, the impedance of the saturated main PA decreases providing more power to the load and maintaining high overall efficiency as the power increases from 6dB back-off to saturation. The efficiency vs output power is similar to the classical Doherty PA when Class B back-off is assumed for the voltage-mode PAs.

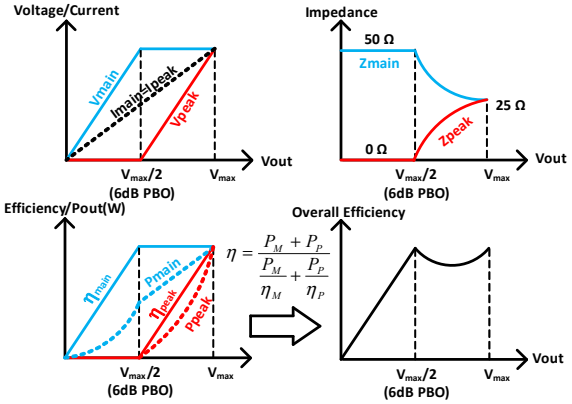

Fig.2. Voltage-Mode Doherty Operation

Fig. 3 shows two pseudo-differential implementations of Voltage Mode Doherty. In each case, load modulation occurs on the primary side of the transformer and the resulting power is combined in series and parallel respectively. These structures keep the transformer fully utilized at all power level resulting in low loss in the load modulation network at all power levels [4].

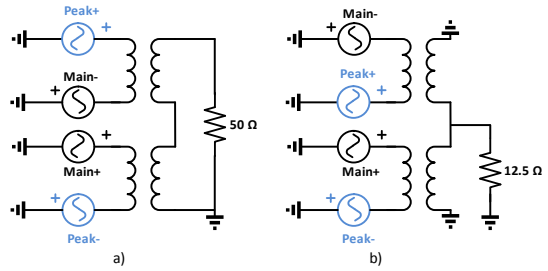

Fig.3. Voltage Mode Doherty (Primary Load Modulated) with a) Series Power Combining and b) Parallel Power Combining

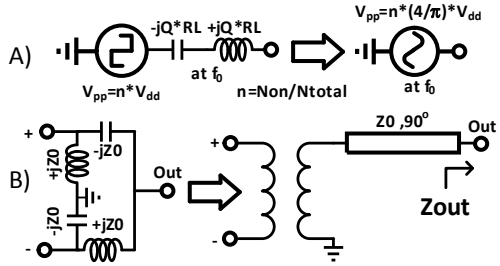

Fig.4. Equivalent Circuit of a) SCPA and b) Lumped Balun

B. SCPA as Voltage Mode Power Amplifier

The voltage-mode amplifier can be efficiently realized at GHz frequency with a switched capacitor PA (SCPA) [5]. A voltage-mode class-D PA (VMCD) is segmented into smaller unit cells, and the output voltage is digitally controlled by turning on a sub-set of the unit cell array forming a capacitive divider. Due to excellent capacitor matching in CMOS technology, SCPAs have been shown to have excellent linearity. The series resonance in the SCPA (Fig. 4a) provides low output impedance regardless of output power level, and the extra inductor can be lumped into the leakage inductance of the transformer enabling compact on-chip implementation. The Q of the series resonance can be designed to be about unity providing wide bandwidth with slightly better than class B PBO efficiency. These characteristics make the SCPA an ideal choice for Voltage Mode Doherty.

IV. Implementation

The two pseudo-differential polar SCPAs [5] are designed in low-leakage 65nm CMOS with standard power supply of 1.2V. Each SCPA is designed with 2-stack driver (2.4V) to drive a 25Ω differential load with 5 bits unary (Fig. 5) and 5 bits binary segmented DAC architecture. A 1:20 deserializer is used to provide the amplitude control word (ACW) to each SCPA. The same phase modulated LO (PMLO) is used for both SCPAs.

A parallel power combined Voltage Mode Doherty (Fig. 3b) is implemented on the PCB (Fig. 7). Two primary load modulated transformers are implemented with lumped element baluns (LB) for ease of experimentation. The LB is an ideal transformer in series with an impedance inverter at its center frequency (Fig 4b). We designed the LBs such that the impedance inverter behaves like a through transmission line (Z0=Zout, similar to a classical Doherty amplifier operating at peak power [2]) resulting in wide bandwidth.

To provide proper impedance for the PAs, an additional 50Ω to 12.5Ω impedance matching network is needed. The T-network is chosen to cancel the reactance of the lumped element balun at a frequency offset, improving the overall bandwidth similar to adding 180 degree transmission line in the peaking PA path in Classical Doherty Amplifier [2].

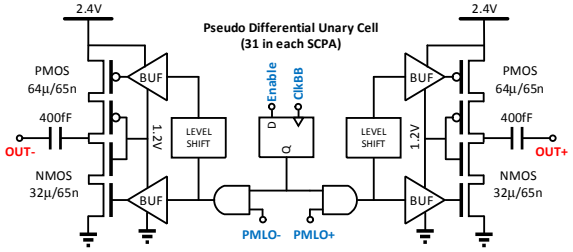

Fig.5. A pseudo differential SCPA unit cell

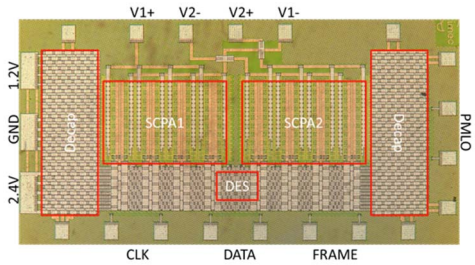

Fig.6. Chip Micrograph (1.8mm x 0.9mm)

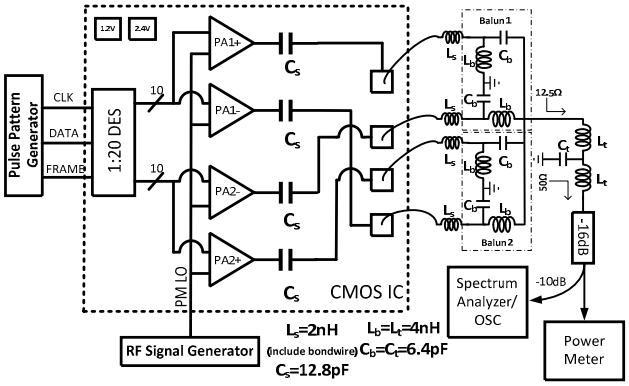

Fig.7. Implementation and measurement setup of Primary-Load Modulated Voltage Mode Doherty with Parallel Power Combining

V. Measurement Setup

The measurement setup was composed of RF vector signal generator to provide the PM-LO, high-speed serial pulse pattern generator to provide ACW, spectrum analyzer for spectrum and narrowband EVM measurement (VSA Mode), high speed oscilloscope for wideband EVM measurement and RF power meter for accurate power measurement. PAE includes all power consumption on-chip, as well as insertion loss of the output load modulation network to the edge of the PCB (50Ω). The external PM-LO and Serial Data/Clk/Frame power is excluded because most of the power is consumed in termination resistors. In an integrated implementation, these will be about the power to drive a few minimum size CMOS inverters, which is negligible.

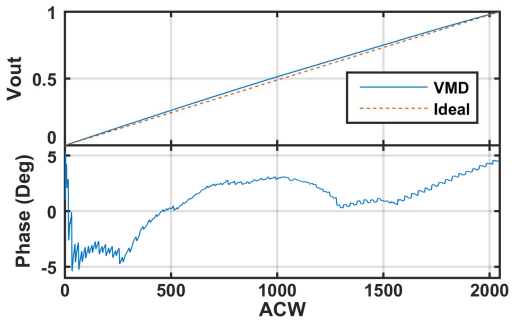

Fig.8. Measured ACW-AM and ACW-PM at 900 MHz

The baseband signal generation and linearization is performed in Matlab with baseband sampling frequency of 360 MHz. Since there is no on-chip interpolation filter [8], digital replicas are expected at multiples of 360 MHz offset. Static look-up table linearization for both ACW-AM and ACW-PM is used. A 10 kHz AM signal with 100% modulation index centered at 900 MHz is used as a training signal. The measured ACW-AM and ACW-PM are shown in Fig 8. The ACW-AM is highly linear and comparable to that of a single SCPA. ACW-PM appears as a weighted average of ACW-PM of each SCPA and is comparable to peak-to-peak ACW-PM for a single SCPA.

VI. Measurement Result

A. CW Measurement

Measurement shows peak power, PAE (0 dB PBO), and PAE (5.6 dB PBO) to be 24 dBm, 45%, and 34% respectively. With 1.5/3V, 26dBm and same efficiency is achieved with no degradation observed. The efficiency peaking point is located at 5.6 dB rather than 6 dB due to loss in the load modulation network. The 1dB power and efficiency bandwidth spans from 750 MHz to 1050 MHz, an over 33% fractional bandwidth. The efficiency around 6dB PBO is lower than at the peak because the output power decreases by 6dB while the VMCD switching loss is only decreased by 3dB, similar to a class-G SCPA [6].

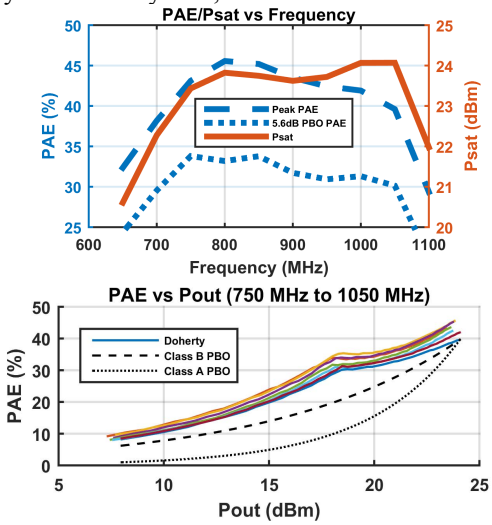

Fig.9. Top: PAE and Psat vs Frequency. Bottom: PAE vs Pout from 750 MHz to 1050 MHz in 50 MHz step.

B. Narrowband Modulation

A 9 MHz 1024-QAM, 32 Carrier OFDM signal hard-clipped to 8.6dB PAPR and centered at 900 MHz is used. The result shows 15.1dBm Pout, 22.9% PAE, -41.2dB EVM and better than 45dBc ACPR. This demonstrates excellent linearity without the need to back-off the output power (Psat-Pout=PAPR). The ACW-AM and ACW-PM show minimal memory effects.

C. Wideband Modulation

A 40 MHz 256-QAM 802.11ac modulation (108 Data, 6 Pilot OFDM) hard-clipped to 9dB PAPR is used. The result shows 14.7dBm Pout with 22.0% PAE and -34.8dB EVM, meeting the EVM spec and Tx mask. No equalization or back-off is required. The ACW-AM and ACW-PM show moderate amounts of memory effect as expected. This is mainly due to passband Psat ripple and non-ideal supply decoupling at baseband frequencies.

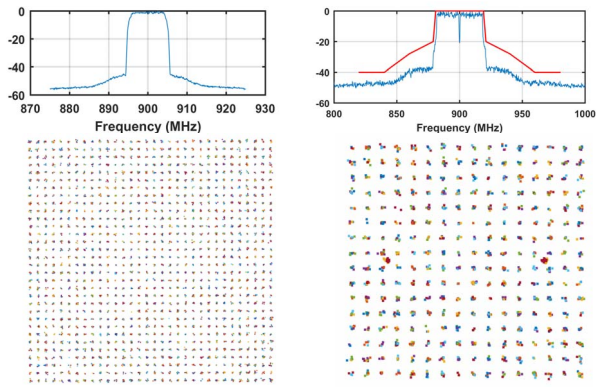

Fig.10. Left: Measured spectrum and constellation of 9 MHz 1024-QAM OFDM modulation. Right: Measured spectrum and constellation of 40 MHz 256-QAM 802.11ac modulation.

VII. Comparison with the State of the Art

This PA achieves superior linearity suitable for modern and future modulation standards while maintaining similar efficiency as the current state of the art.

To account for PAPR differences in the average efficiency comparison in Table I, we use "equivalent efficiency" (the peak efficiency of an ideal class-B amplifier that gives the same average efficiency). It can be approximated by $\eta_{eff} = \eta_{avg}\sqrt{PAPR}$ with reasonable accuracy.

TABLE I
Comparison with CMOS PA
with Back-off Efficiency Enhancement

	This Work	**[6]**	**[7]**	**[8]**	**[3]**	**[4]**
Freq(MHz)	900	2000	2000	2200	3500	1900
1dB Psat BW(%)	**33**	15	10	29	25	17
Psat (dBm)	24	24.3	20	23.3	27.3	28
Technology	65(LP)	65(LP)	65	65	65	40
Vdd	1.2/2.4	1.4/2.8	-	1.2	1.2/3	1.5
Peak/6dB Eff(%)	45/34 (PAE)	44/37[6] (PAE)	22/17 (PAE)	43/33 (DE)	33/34 (DE)	34/26 (PAE)
Topology	VMD	ClassG	ClassG	XFMR	Doherty	Doherty
Modulation	**40MHz 802.11ac 256QAM**	20MHz 802.11g 64QAM	5MHz LTE 64QAM	20MHz 802.11g 64QAM	0.5MHz 16QAM	20MHz LTE 16QAM
PAPR(dB)[4]	**9.0**	7.5	5.8	6.5	5.5	4.6
EVM (dB)	**-34.8**[1]	-30.8[3]	-28[1]	-28[1]	-25[2]	-23[3]
Avg Eff(%)	22	33[6]	12	21.8	22.1	23.3
Equivalent Eff (%)[5]	**62**	78[6]	24	46	42	40
Matching Network	Off-Chip	Off-Chip	On-Chip	Off-Chip	On-Chip	On-Chip

[1]With LUT [2]Partial LUT [3]No LUT [4]Output PAPR=Psat-Pout
[5]Efficiency of ideal Class-B PA that achieve the same Avg Eff
[6]Output balun loss is not included

VIII. Conclusion

This paper demonstrates a new Doherty technique that eliminates the impedance inverter enabling wide bandwidth. To the author's best knowledge, this is the widest fractional bandwidth (at both peak and 6dB PBO) Doherty Amplifier ever demonstrated in CMOS technology. With only simple look-up table linearization, this amplifier can transmit a 256-QAM 40 MHz 802.11ac modulation meeting the spec without backing-off, maintaining excellent efficiency. As CMOS technology scales, switching loss significantly improves, especially in PMOS transistors. This makes it possible to use this technique for a 6 GHz carrier with integrated transformer, amplifying up to 160 MHz modulation (similar fractional bandwidth) with reasonable efficiency.

Acknowledgment

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