A 24 GHz Signal Generator with 30.8 dBm Output Power Based on a Power Amplifier with 24.7 dBm Output Power and 31% PAE in SiGe

Benedikt Welp
Fraunhofer FHR
53343 Wachtberg, Germany
Email: benedikt.welp@fhr.fraunhofer.de

Karam Noujeim
Anritsu
Morgan Hill, USA
Email: karam.noujeim@anritsu.com

Nils Pohl
Fraunhofer FHR
53343 Watchberg, Germany
Email: nils.pohl@fhr.fraunhofer.de

***Abstract*—High-frequency systems such as mm-wave radar transmitters and LO/RF chains in vector network analyzers (VNAs) often require the generation of signals with high output power. While these systems benefit considerably from the reduction in size and weight provided by SiGe integration, their output power must be further increased in order to meet the performance of other technologies (e.g. GaAs). To this end, a SiGe signal generator was developed that achieves 28.7 dBm peak output power with 21.9% of PAE and over 27.4 dBm of output power over its whole frequency range from 19.7 GHz to 28.2 GHz. The output power is scalable with DC current up to a maximum of 30.8 dBm with 17.6% PAE. It is based on a voltage controlled oscillator (VCO), power amplifier cells (PA cells) and lumped-element Wilkinson power combiners/dividers. Its phase noise is less than -94 $\frac{\text{dBc}}{\text{Hz}}$ at 1 MHz offset over the entire frequency range. The developed single PA cell achieves a maximum saturated output power P_{sat} of 24.7 dBm with a peak PAE of 31%.**

I. Introduction

A challenging requirement in modern high-frequency SiGe technologies is the generation of sufficient output power for use in a variety of applications such as communications, radar, and instrumentation. This requirement is a necessity for SiGe to further extend its benefits of large-scale integration and low cost (i.e. when compared with GaAs, InP or GaN) to these applications. For instance, high-frequency measurement instruments such as VNAs would be prime beneficiaries of high-output-power SiGe since a highly stable signal source with high output power could be used to drive non-linear transmission lines (NLTLs) that generate VNA stimulus frequencies in the mm-wave range [1]. In this work, the goal was to realize a single-chip, high-power signal generator in SiGe with high PAE in order to reduce the cost of frequency-multiplication chains or other measurement devices.

The developed signal generator consists of a 24 GHz VCO with a static divide-by-8-section for PLL stabilization, five identical PA cells with one used as preamplifier to saturate the other four, and Wilkinson power combiners/dividers for the splitter and combiner networks. The 24 GHz VCO in this work is a modified version of the VCO presented in [2] and [3]. A block diagram of the signal generator is shown in Fig. 1 with the preamplifier and the PA stage (four parallel PA cells). The system is set up to be completely differential. Fig. 2a and Fig. 2b show chip photographs of the PA cell itself and of the complete signal generator MMIC.

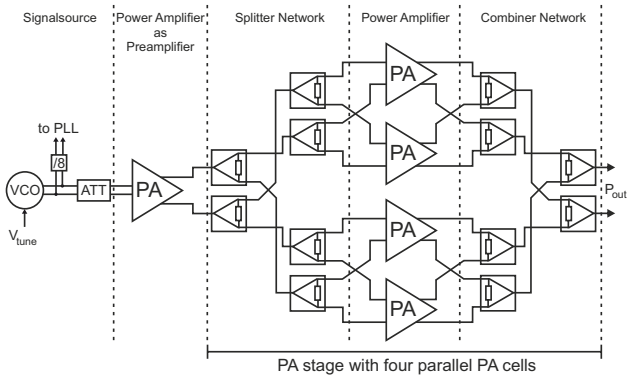
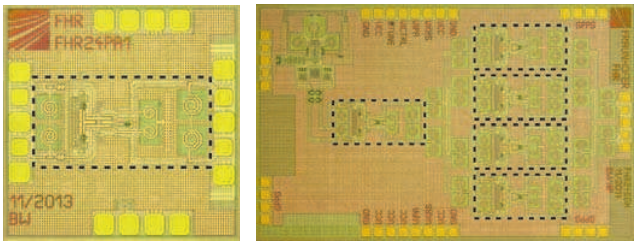


Figure 1: Block diagram of signal generator MMIC.



(a) PA cell. The chip is 1x1 mm^2.

(b) Signal Generator. The chip size is 3x2 mm^2.

Figure 2: Chip Photos. Dashed active PA area 0.252 mm^2.

Both MMICs were developed in Infineon's current SiGe production technology which is a 0.35 μm technology with an effective emitter width of 0.18 μm. It provides an f_{T} of 200 GHz and an f_{max} of 250 GHz.

II. Power Amplifier Cell

The PA cell's architecture (Fig. 3) is fully differential. It consists of a common emitter stage Q_2 with a current source Q_3-Q_5 followed by a cascode stage Q_1 which is connected to an inductive load L. The input matching network is designed for wideband operation between 19.7 GHz and 28.2 GHz. The

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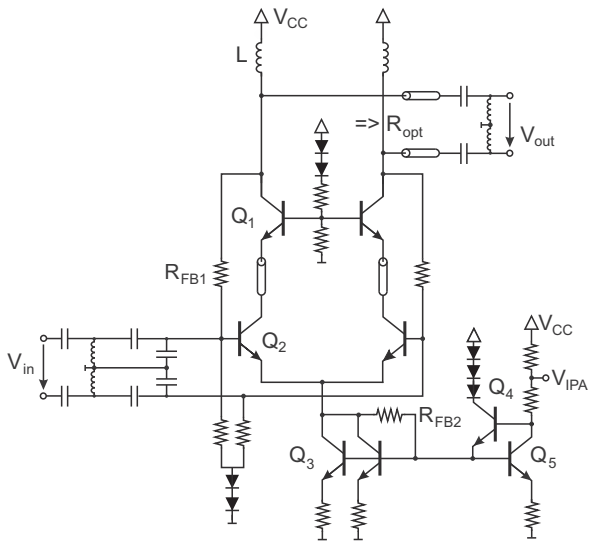

Figure 3: Schematic of the PA cell architecture.

output matching network selected to achieve the load line transformation was made as simple as possible in order to reduce insertion loss at the PA's output. Additionally, large valued feedback resistors at the current source (R_{FB2}), and from the output to the input of the amplifier (R_{FB1}) were used to achieve stability. This stacked architecture and also the output matching network stand out due to low loss compared to transformer coupling.

There are multiple effects that limit output power in SiGe technologies. The avalanche-breakdown limit arises at relatively low voltages in modern SiGe technologies compared to that in III-V technologies. This is due to the extremely thin base region (<30 nm) in the used technology, resulting in a collector emitter breakdown voltage BV_{CES} of typically 6.5 V, with the base shorted to ground. This voltage decreases even more with a higher load impedance at the transistor base. For transistors with an open base, the breakdown voltage BV_{CEO} is typically 1.7 V. The avalanche-breakdown is most critical at the cascode stage where a high output voltage swing is generated. Therefore a differential architecture was chosen because this leads to a virtual ground at the transistor base of the cascode stage for differential ac signals. Hence, BV_{CES} can be expected for those signals. Especially in the PA layout the base interconnection at the cascode stage is the most critical part because it demands a very low parasitic inductance and resistance in order to handle the high output current.

Another important performance factor is the high-current limit. It degrades the transistor's current amplification factor β, and therefore reduces the cut-off frequency [4].

The high-current limit restricts the maximum possible current amplitude $\hat{I}_{\mathrm{out,max}}$, and the avalanche-breakdown limit restricts the maximum possible differential voltage amplitude $\hat{V}_{\mathrm{out,max}}$. In order to achieve the maximum output power, it is necessary to reach the maximum voltage and current amplitude at once. Thus the inner current sources of the cascode stage transistors must work on an ohmic load. Hence, the inductive

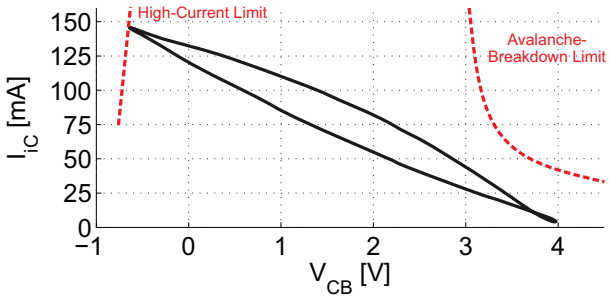

Figure 4: Simulation of the dynamic load line of the inner transistor current source of the cascode stage at 25 GHz for 169 mA DC current.

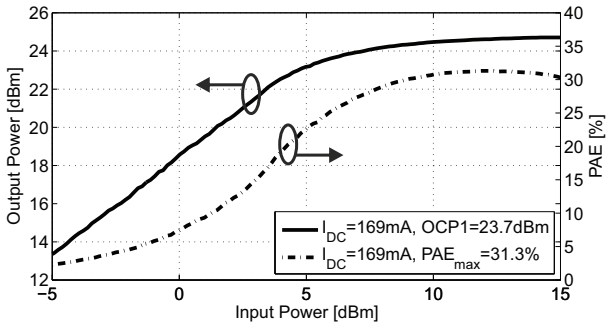

Figure 5: Measured compression behavior of the PA cell at 25 GHz with 24.7 dBm P_{sat} and 31.3% PAE.

load L from Fig. 3 is in resonance with the parasitic collector-base capacitance C_{CB} of the cascode transistors. Finally the differential 100 Ω load has to be transformed by the output matching network to match the optimum load impedance which is $R_{\mathrm{opt}} = \frac{\hat{V}_{\mathrm{out,\,max}}}{\hat{I}_{\mathrm{out,max}}}$. In this case, 4 V (theoretical limit 5.7 V of V_{CB} for 0.8 V of V_{BE} , 4 V chosen as safety margin) and 72 mA, respectively. These values were chosen to achieve an output power of at least 21 dBm and result in an optimum load resistance R_{opt} of 55 Ω which was also found to be the best value in load pull simulations. Therefore the maximum current through the inner current source is $2\hat{I}_{\mathrm{out,max}}$. It is important to choose a transistor size which is able to handle a collector current density j_{C} that corresponds to $2\hat{I}_{\mathrm{out,max}}$ and does not cause high-current limit effects because of excessively high current density.

The simulation of the dynamic load line for a load-line-matched single-ended output at 25 GHz can be seen in Fig. 4. The dynamic load line depends on the phase relationship between output current and output voltage swing. In this graph the inner collector current I_{iC} which is the current generated by the transistor's current source is plotted over the collector-base voltage V_{CB} because those are the critical values of the inner transistors [5]. The nearly linear behavior shows that the transistor's load is mainly ohmic. With a more imaginary load this curve would get more circular which would increase the likelihood that the dynamic load line will run into the critical high-current limit or avalanche-breakdown limit regions.

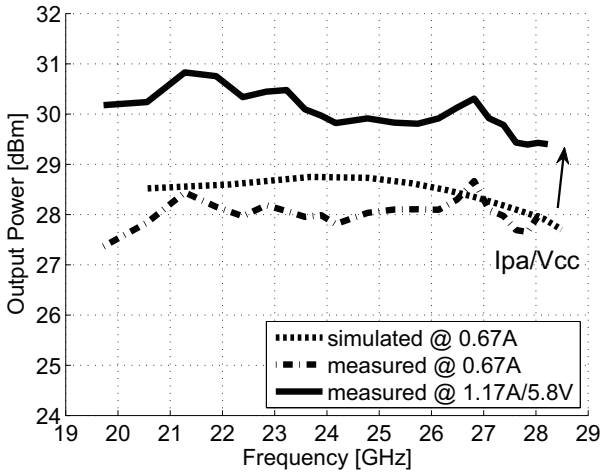

Figure 6: Measured signal generator output power with variation of DC current (higher current results in higher PA cell OCP1).

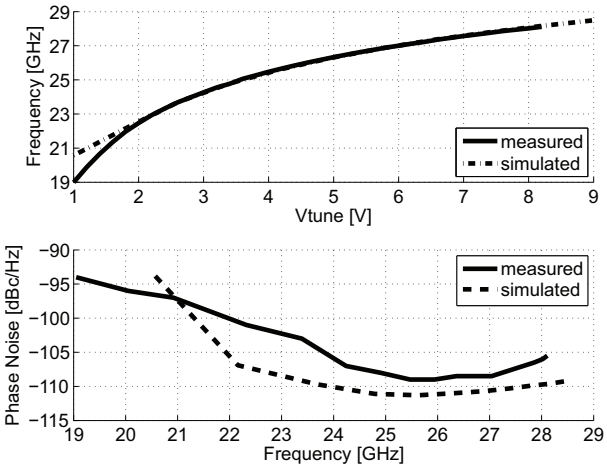

Figure 7: Measured and simulated tuning characteristic (top) and phase noise behavior @ 1 MHz Offset (bottom) of the signal generator (higher current results in higher VCO output power).

The transistor model does not contain self-heating and high current effects but the avalanche-breakdown behavior is modeled by Miller's avalanche multiplication coefficient and is thus part of the simulation.

In Fig. 5 the measurement results of the PA cell's OCP1 with 23.7 dBm and 24.7 dBm P_{sat} at 25GHz and the PAE with 31% for a DC current of 169 mA can be seen. This shows that with this architecture and the used load-line matching the theoretical limit of the maximum voltage amplitude $\hat{V}_{\text{out, max}}$ of 5.7 V is reached as a stable operating point[1]. By increasing the DC current (incl. bias current) up to 220 mA at the V_{IPA} pin (see Fig. 3) the OCP1 rises up to 24.6 dBm with a maximum saturated output power of 25 dBm.

III. Signal Generator

The signal generator contains four PA cells in parallel and one PA cell as preamplifier in order to drive the PA stage (four parallel PA cells) into saturation.

The PA cell signals are split and joined together by lumped-element Wilkinson combiners/dividers which have a simulated insertion loss of 0.6 dB. In Fig. 6, a simulated peak output power of about 28.7 dBm can be seen in addition to the corresponding curve of the measured PA stage with 0.67 A of DC current. The achieved PAE of the PA stage with four parallel PA cells with splitter and combiner network (see Fig. 1) is 21.9%. The PAE of the complete system including the preamplifier and the VCO is 17%. The deviation of the measurement from the simulation is caused by higher than simulated loss of the Wilkinson combiners/dividers and the transmission line interconnection between the PA cells and the combiners/dividers of about 700μm which have not been part of the simulation.

By increasing the PA stage's DC current up to 1.17 A the signal generator achieves over 29.4 dBm of output power in the complete frequency range from 19.7 GHz to 28.2 GHz and 30.8 dBm peak output power but the PAE of the PA stage decreases to 17.6%.

The tuning characteristic and phase noise behavior are shown in Fig. 7. The VCO itself is able to generate signals from 19.7 GHz up to 28.2 GHz which results in a relative bandwidth of 35.5 %. In the lower tuning voltage range there is a deviation of the measurement and simulation results because the model of the used differential varactors dynamically leaves the accurately modeled reverse biased region due to the fact that the DC voltage across the diodes in this area is about 0 V.

The phase noise is better than $-94\,\frac{\text{dBc}}{\text{Hz}}$ at 1 MHz offset over the whole frequency range, and reaches a minimum phase noise of about $-109\,\frac{\text{dBc}}{\text{Hz}}$ at 1 MHz offset at 25.7 GHz. The DC current variation of the VCO and thus the VCO's output power hardly affects the tuning characteristic. By increasing the VCO's output power, the oscillator core power rises, leading to an improvement in phase noise performance as predicted by Leeson's equation.

IV. Conclusion

We have presented the development and measurement of a 19.7-28.2 GHz PA cell and its application together with a 24 GHz VCO as part of a signal generator MMIC. Both systems were realized in Infineon's current 0.35 μm SiGe production technology B7HF200. The standalone PA cell and the signal generator consume 845 mW and 4.35 W respectively from a single 5 V supply voltage with all biasing on chip. All measurements were done on-chip and have been verified at a chuck temperature of 25°C and 120°C within a decrease of output power below 0.7 dB for the higher temperature.

The PA cell itself is able to reach a maximum saturated output power P_{sat} of 25 dBm, while the signal generator is able to reach over 29.4 dBm of output power and a good phase

[1] $24.7\,\text{dBm} = 10 \cdot \log_{10}\left(1000 \cdot \frac{(5.7\,\text{V})^2}{55\Omega \cdot \sqrt{2^2}}\right)\,\text{dBm}$

Table I: Comparison of SiGe Power Amplifiers.

Ref	Freq. [GHz]	P_{sat} [dBm]	PAE [%]	Gain [dB]	Chip Area [mm^2]	Supply	Technology
This work (PA cell)	24	24.7	31	18.5	0.86	5 V @ 169 mA	0.35 μm SiGe
This work (PA stage)	24	28.7	21.9	$\approx$ 16.1	5.37	5 V @ 0.67 A	0.35 μm SiGe
		29.8	19.8			5 V @ 0.96 A	
		30.8	17.6			5.8 V @ 1.17 A	
[6]	22	23	19.7	19	6	1.8 V @ 522 mA	0.18 μm SiGe
[7]	24	20	14	12	1.02	5.1 V @ 140 mA	0.18 μm SiGe
[8]	24	19.4	22.3	37.6	1.1	2.4 V @ 163 mA	0.18 μm BiCMOS
[9]	27	31	13	20.7	2.83	6.9 V @ 1.4 A	0.25 μm BiCMOS

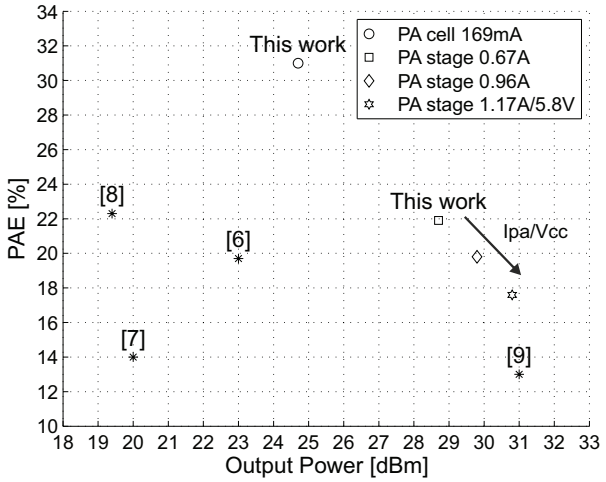

Figure 8: Comparison with similar PAs in output power and PAE.

noise performance over its whole frequency range from 19.7-28.2 GHz. The peak output power is 30.8 dBm.

In Tab. I the developed PA cell and stage are compared with recently published SiGe PAs. The combination of high output power and power-added efficiency are very good and the achieved PAE of the single PA cell with 31% is clearly exceeding the state of the art. And even the PA stage with a maximum PAE of 21.9% and 28.7 dBm output power shows the excellent performance of the design. The high efficiency and output power are the result of a carefully designed stacked differential architecture and a PA output network which compensates parasitic effects of the cascode stage and has low insertion loss. Especially the differential architecture enables the output transistors to work at their inherent physical limits in order to deliver maximum output power to the load.

Fig. 8 visualizes the results of the compared PA realizations of Tab. I. The PA cell and the PA stage from this work show a excellent combination of P_{sat} and PAE in comparison with other state-of-the-art PAs in SiGe.

The PA stage scales linear with variation of the PA current and the supply voltage. This suggests that this curve could be extrapolated even more for a PA stage realization with eight PA cells, so that more output power would also be possible by increasing transistor size and scaling the other components, or by extending the parallelization of the developed PA cells which consume only 0.252 mm^2 of the active chip area.

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