A CMOS Class-E Power Amplifier With Voltage Stress Relief and Enhanced Efficiency

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Abstract—This paper proposes a class-E power amplifier (PA) with double-resonance circuit to reduce voltage stress on CMOS transistors. The voltage waveform applied to the CMOS transistor is shaped by harmonic control and the transistors are relieved from breakdowns. A negative capacitance is also implemented for efficiency enhancement, compensating for surplus capacitance from parasitic components on the drain node. Thus, nominal class-E operation is restored and high efficiency is achieved. We present a cascode differential class-E RF PA that is fabricated using a 0.13-μm CMOS technology that delivers 31.5-dBm output power with 54% drain efficiency and 51% power-added efficiency at 1.8 GHz.

Index Terms—Class-E, CMOS power amplifiers (PAs), switching amplifiers, zero voltage switching (ZVS).

Fig. 1. Basic class-E amplifier schematic with CMOS switch.

I. INTRODUCTION

MOBILE equipment demands highly efficient RF transmitters to conserve battery life. The power amplifier (PA) is the most critical component used to determine overall RF transmitter efficiency because it consumes the largest portion of dc power in the transmitter. Thus, highly efficient PAs are necessary to improve overall efficiency. A class-E PA is adaptable for a high-efficiency transmitter due to its high efficiency and simplicity. A class-E amplifier with a shunt capacitor was introduced by Sokal and Sokal in 1975 and was examined by Raab in an analysis of idealized operation [1], [2]. As a kind of switching amplifier, it can achieve the ideal 100% drain (or collector) efficiency by shaping the voltage waveform and current waveform so that they do not overlap, making it a strong candidate for a highly efficient RF PA [3]–[10]. Many designs have been presented on new devices, such as GaAs HBTs, GaN HEMTs, and InP double HBTs (DHBTs), used to operate on microwave and higher frequencies with better RF performances [11]–[13]. Recently, many researchers have been conducted about watt-level output power PAs using CMOS technology on microwave due its low cost [14]–[22].

In spite of its cost effectiveness, the CMOS PA has a serious weakness: a low breakdown voltage. As the process scale becomes smaller, the breakdown voltage is also reduced. As a re-
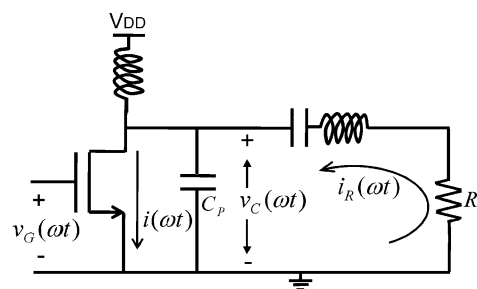
sult, supply voltage is limited to avoid breakdowns. In delivering large output power under a low-supply voltage, low load impedance is inevitable, which causes efficiency degradation and a narrowband load matching network [15], [18].

This study presents a double-resonance circuit for harmonic control, which gives relief to CMOS transistors from breaking downs. This circuit shapes a voltage waveform applied to the transistor gate and reduces voltage stress across the CMOS transistors. When voltage stress is reduced, the voltage margin from the breakdown increases, enabling the application of a higher supply voltage. With higher supply voltage, higher load impedance can be implemented to deliver the same output power with greater efficiency.

Additionally, CMOS PAs require wide gatewidths to reduce on-resistance for high efficiency and to drive sufficient currents for watt-level output power. The maximum operation frequency of class-E (f_{MAX}) is also proportional to peak drain current (I_{MAX}). For these reasons, the applicable gatewidths are some millimeters wide [14]–[17], [21]. However, widening the gatewidth introduces undesired parasitic components, such as parasitic capacitance. Parasitic capacitance increases the value of shunt drain capacitance (C_P), depicted in Fig. 1, which determines the nominal operation condition and maximum operation frequency of a class-E amplifier since f_{MAX} is determined by an I_{MAX}/C_P ratio [23]. When C_P deviates from its optimum value determined by the condition of nominal class-E operation, the efficiency degradation occurs. To maintain high efficiency, the surplus capacitance from parasitic capacitance should be tuned out. We set a negative capacitance using a simple capacitor to tune out surplus capacitance without adding external circuits.

In this paper, differential architecture is used to deliver higher output power than a single-ended PA. Differential architecture can provides 3-dB more output power with the same supply voltage and load impedance than single-ended architecture.

Differential architecture also disturbs other circuits less than a single-ended architecture in the same chip during the operation. Furthermore, it restrains the second harmonic at the output. An off-chip passive LC balun is used to transform the output structure from differential to single-ended.

This paper is organized as follows. Section II introduces the fundamental theory of a class-E PA. In Section III, a double-resonance circuit for voltage stress relief is addressed. In Section IV, we present a cascode class-E PA with negative capacitance to compensate for the surplus C_P. After that, we explain our CMOS PA design in Section V, and our measurement results are shown in Section VI. Conclusions are given in Section VII.

II. FUNDAMENTAL THEORY OF CLASS E

The class-E amplifier is composed of a switch (usually a transistor) and a shunt capacitor. Its basic schematic is shown in Fig. 1 and i_R is determined as

$$i_R(\omega t) = I_R \sin(\omega t + \varphi). \tag{1}$$

In addition, based on previous study, the voltage across the switch $v_C(\omega t)$ and the current through the switch $i(\omega t)$ are stated as follows [24]:

$$v_C(\omega t) = -\frac{I_R}{\omega C_P}[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi] \tag{2}$$

$$i(\omega t) = I_R[\sin(\omega t + \varphi) - \sin\varphi]. \tag{3}$$

The operation of class E is the charging/discharging of C_P following an operating signal. For a nominal class-E operation, $v_C(\omega t)$ should satisfy two conditions, which are: 1) zero voltage switching (ZVS) and 2) zero voltage derivative switching (ZVDS). ZVS prevents the dissipation of the energy stored by the C_P when it turns on, and ZVDS makes the circuit robust in the face of variations in the components, frequency, and switching instants [25], [26]. When a class-E amplifier operates in a nominal condition with a 50% duty cycle (the transistor is on for $0 \leq \omega t < \pi$ and off for $\pi \leq \omega t < 2\pi$), the value of φ is determined as $-32.482°$. Consequently, (2) and (3) can be written in normalized form as

$$\frac{v_C(\omega t)}{V_{DD}} = \pi\left[\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos(\omega t) - \sin(\omega t)\right] \tag{4}$$

$$\frac{i(\omega t)}{I_0} = \frac{\pi}{2}\sin(\omega t) - \cos(\omega t) + 1 \tag{5}$$

where $I_0 = -I_R\sin(\varphi)$.

A class-E amplifier operation with waveforms of (4) and (5) achieves 100% drain (or collector) efficiency because, in theory, they do not create dc losses by overlapping $v_C(\omega t)$ and $i(\omega t)$ in the operation. The relationship between the operation frequency C_P and the load impedance (R_L) is calculated as $\omega C_P R_L = 0.1836$ in a nominal class-E operation [27].

However, in the real world, variation exists in the desired C_P value based on parasitic capacitance or process variation in the CMOS process. Thus, the $\omega C_P R_L$ value cannot maintain 0.1836 with fixed R_L at a given frequency. When the $\omega C_P R_L$ values deviate from 0.1836, there is a loss in the class-E amplifier operation, degrading the drain (or collector) efficiency.
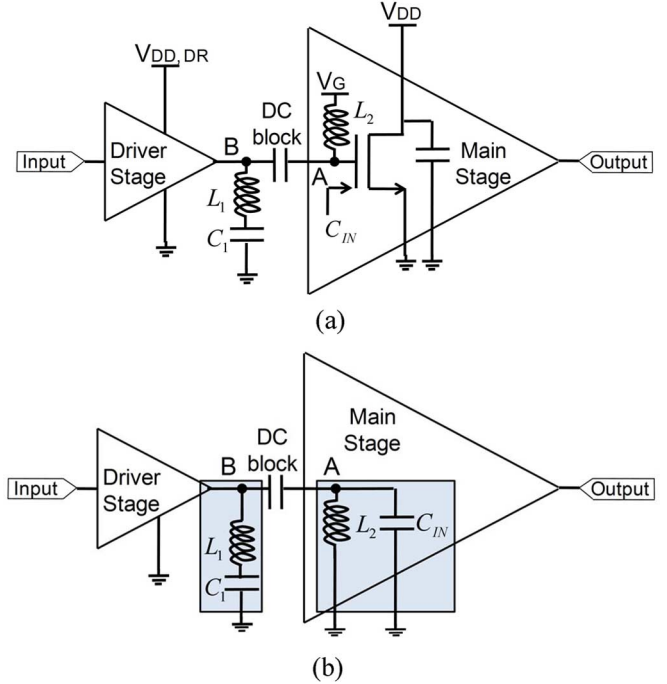

Fig. 2. Schematic of: (a) double-resonance circuit implementation and (b) its ac equivalent circuit.

Another characteristic of a class-E amplifier is a high-peak voltage swing. Maximum voltage on the drain (or collector) of the transistor in the operation conditions given above is depicted in the following equation under a supply voltage V_{DD} [28]:

$$V_{\text{MAX}} = -2\pi\varphi V_{DD} = 3.562V_{DD} \tag{6}$$

and the value of V_{MAX} threatens the transistor's reliability, especially in CMOS technology, due to its low breakdown voltage. To ensure circuit reliability, several research studies have been conducted to analyze voltage stress on CMOS transistors [15], [21]. In order to reduce voltage stress on transistors, we present a double-resonance scheme in Section III.

III. DOUBLE-RESONANCE CIRCUIT

The double-resonance circuit shapes the voltage waveform at the transistor gate of the PA at node A in Fig. 2 using harmonic control. The voltage waveform at node B in Fig. 2 is usually induced by the switching-mode driver stage because the switching-mode driver amplifier's output is adaptable to drive the class-E PA [16], [20]–[22]. Thus, the switching-mode driver amplifier operates in the nonlinear region, containing many harmonics in the output waveform. When the output signal from the driver stage is applied to the main stage, there is only a dc-bias difference between the driver stage output node and the main stage input node, which are indicated as "B" and "A," respectively, in Fig. 2. Thus, the waveform on node A in Fig. 2 can be written in general form as

$$v_G(\omega t) = a_0 + a_1\sin(\omega t) + a_2\sin(2\omega t) + a_3\sin(3\omega t)$$
$$+ a_4\sin(4\omega t) + \cdots \tag{7}$$
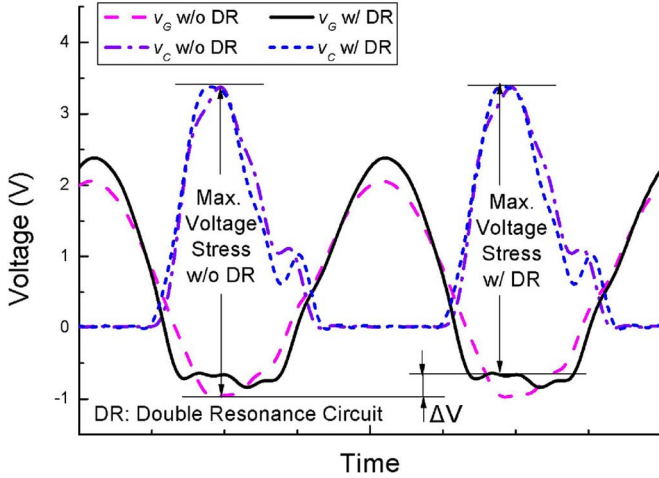
where a_i represents the coefficient of ith harmonics.

Fig. 3. Waveforms of input voltage (v_G) and output voltage (v_C) of CMOS class-E amplifier (Fig. 1), and voltage stress reduction (ΔV) by double-resonance circuit with maintaining duty cycle (transistor threshold voltage = 0.5 V and $V_{DD} = 1.0$ V).

Fig. 4. Normalized voltage v_C (on transistor drain) and current i (flowing transistor) waveforms of class E for different values of $\omega C_P R_L$ with 50% duty cycle.

The resonance frequencies of the double-resonance circuit are fundamental frequency and second harmonic. The control of these harmonics shapes the voltage waveform (v_G), as described in Fig. 3, by reducing even harmonics. The double-resonance circuit trespasses fundamental frequency and third harmonic from driver stage to the main stage and removes the second harmonic.

Since the voltage of the drain (or collector) hits its peak value (theoretically $3.562V_{DD}$ in a 50% duty cycle) when the switch is in the off state, the highest voltage stress is applied across the gate–oxide during this period (see Fig. 3). Applying the double-resonance circuit increases the dc offset of v_G and does not allow v_G to stay too far below the transistor's threshold voltage during the off state, without deteriorating the duty cycle. Therefore, a higher v_G in the off state decreases maximum voltage stress across the transistor.

This voltage shaping by the double-resonance circuit using harmonic control differs from dc-bias increasing. DC-bias increasing changes the duty cycle of the amplifier and different duty cycles have different drain (or collector) peak voltages [10]. As the duty cycle increases, the peak voltage also increases, and it worsens the voltage stress on the transistor. However, voltage shaping via harmonic control exhibits the same duty cycle in 0.5-V threshold voltage transistors in Fig. 3 and allows the PA to maintain its performance.

Above all, our double-resonance circuit using harmonic control relieves transistors from breakdowns through voltage stress reduction. In a CMOS class-E amplifier with 1.0-V supply voltage, voltage stress is reduced about 0.3 V from 4.3 to 4.0 V in simulation. Furthermore, eliminating the second harmonic and trespassing odd harmonics (fundamental frequency and third harmonic) moves v_G to have faster rising and falling times, which aids in switching the amplifier's operation.

To implement the double-resonance circuit, we used two resonators. One is the parallel LC resonator consisting of gate
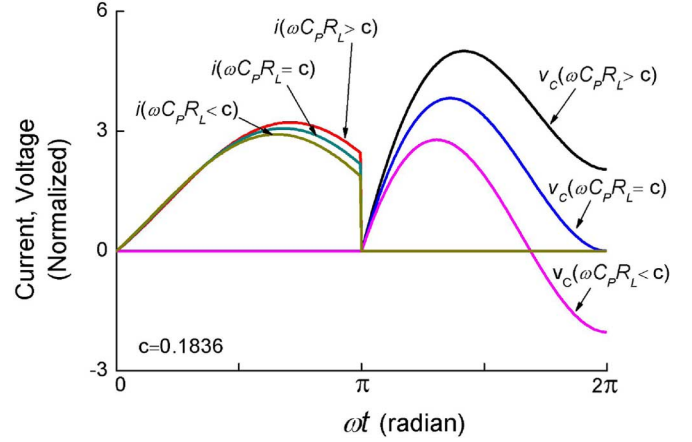
inductor (L_2) and main stage input capacitance (C_{IN}), as described in Fig. 2. It is designed to resonate at the fundamental frequency to drive the main amplifier efficiently, overcoming large input capacitance. The other resonator is a series LC resonator (L_1, C_1) attached to the output node of driver stage, rejecting the second harmonic and trespassing the fundamental frequency and third harmonic at node B in Fig. 2. With the proposed double-resonance circuit, transistors are relieved from breakdowns and obtain margins to increase supply voltage V_{DD} in the main stage of operation.

Higher supply voltage brings enhanced PA performance. Obviously, a PA with a higher supply voltage delivers a greater output power with the same load impedance. In addition, in watt-level output power CMOS PAs, load impedance is usually a few ohms, and thus, a higher ratio of impedance transformer is required to obtain higher output power. However, when a higher supply voltage can be applied using this double-resonance scheme, a higher load impedance can be implemented for the same output power with efficiency enhancement.

IV. NEGATIVE CAPACITANCE

A. Shunt Capacitance Analysis

As we stated in Section II, efficiency declines when the $\omega C_P R_L$ value deviates from its optimum value and we derived the relationship between φ and $\omega C_P R_L$ as

$$\varphi = \frac{1}{2}\left[\sin^{-1}\left(\frac{\omega C_P R_L}{\sqrt{1/4 + 4/\pi^2}}\right) - \tan^{-1}\left(\frac{4}{\pi}\right)\right] \quad (8)$$

which has an inverse proportion between φ and $\omega C_P R_L$. When $\omega C_P R_L$ increases from 0.1836, φ decreases and the transistor drain voltage is a positive value at $\omega t = 2\pi$. On the other side, when $\omega C_P R_L$ decreases from 0.1836, φ increases, resulting in a negative drain voltage at $\omega t = 2\pi$. The waveforms of $v_C(\omega t)$ and $i(\omega t)$ in a single period are shown in Fig. 4 for different $\omega C_P R_L$ values when 50% duty cycle is applied. The transistor is on for $0 \leq \omega t < \pi$ and off for $\pi \leq \omega t < 2\pi$. When

the ZVS condition is not satisfied ($\omega C_P R_L$ is not 0.1836), the voltage and current waveforms will overlap at the beginning of the next period because transient time is required to have zero voltage across the transistor drain and source. This transition time results in a loss during the finite transient time [29]. Therefore, with the given frequency and fixed R_L, C_P value should be maintained with optimum value to achieve high efficiency in the class-E amplifier.

B. Negative Capacitance

In the field of a CMOS PA, a large gatewidth is inevitable in delivering watt-level output power. The gatewidths are some millimeters wide and these wide transistors contain picofarad capacitance on the drain node. This adds parasitic capacitance on C_P, increasing C_P from its desired optimum value and resulting in drain efficiency (DE) degradation. In addition, in the class-E CMOS amplifier, cascode topology is preferred for its reliability due to the characteristic of high-peak voltage. The additional common-gate (CG) amplifier usually has a large gatewidth to reduce on-resistance and it also contributes to the increase of C_P. Thus, as C_P increases, compensation for surplus capacitance is more significant for efficiency restoration.

To maintain the optimum C_P value, surplus capacitance should be tuned out. One of the techniques used to tune out surplus capacitance is to place an inductor on the same node with a dc block [21]. However, the inductor requires a large area to be implemented into an integrated circuit. Moreover, it contains parasitic components, such as parasitic capacitance and resistance in itself, and has a low quality factor (Q factor). Therefore, we use negative capacitance to tune out surplus C_P in cascode topology.

Basically, negative capacitance works in the same manner as polarity-inversed Miller capacitance. Miller capacitance is stated as

$$C_M = (1 - K) \cdot C_n \qquad (9)$$

where K indicates the voltage gain of the C_n's nodes. Conventional C_M is applied with negative K, increasing capacitance to $(1 - K)$ times C_n. On the contrary, we applied positive K to obtain negative capacitance. The realization of negative capacitance is shown in Fig. 5(a), as noted by C_n. Since C_n is connected between the input and output CG amplifier, which has positive gain K, it generates negative capacitance C_M on node A, as described in Fig. 5(b). This negative capacitance compensates for surplus capacitance on node A in Fig. 5, adjusting C_P to optimum value and restoring nominal class-E PA operation.

Negative capacitance using a capacitor benefits the integrated CMOS PA. A capacitor demands a much smaller area than an inductor and has a higher Q factor with less parasitic components than an inductor. Moreover, it can be tuned by arraying parallel capacitors with switches and requires a very small value thanks to CG amplifier gain K.

Parasitic capacitance on node B is not as much of a concern as that of node A because the value of parasitic capacitance on
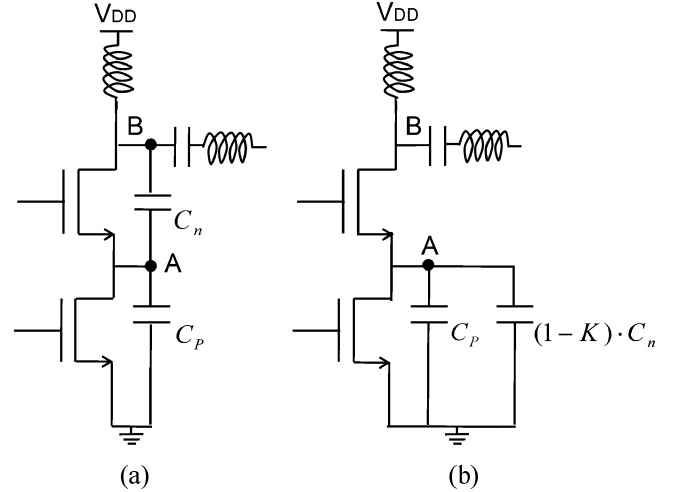

Fig. 5. Schematic of: (a) negative capacitance realization and (b) its equivalent circuit.

node B is smaller than that on node A in Fig. 5. In addition, the CG amplifier is always turned on to reduce on-resistance so most of the capacitor charging/discharging occurs at node A in Fig. 5 based on the switching operation.

V. CIRCUIT DESIGN

A. Main Stage

A class-E amplifier has high peak voltage across the transistor so the voltage stress on CMOS transistors should be considered carefully. For this reason, we adopt cascode topology to ensure freedom from breakdowns because the cascode structure divides large output voltage swing into two series transistors [15].

For the given standard 0.13-μm CMOS process, the foundry provided two different types of transistors, which are: 1) a thin gate–oxide transistor, which has a 0.13-μm gate length for 1.2-V supply voltage and 2) a thick gate–oxide transistor, which has a 0.34-μm gate length for 3.3-V supply voltage. We used a thin gate–oxide transistor as the common source (CS) amplifier and a thick gate–oxide transistor as the CG amplifier to ensure the best performance.

This combination works better than two thick gate–oxide transistors because the thin gate–oxide transistor demonstrates a better RF performance and has smaller on-resistance than the thick gate–oxide transistor. Better RF performance alleviates the complexity of the driver amplifier and leads to higher operation efficiency. Furthermore, it contains fewer parasitic components such as drain capacitance, which affects increase of the C_P value. In this study, we used 4000-μm gatewidth transistors for the CS amplifier.

For the CG amplifier, we used a thick gate–oxide transistor for its sustainability. In class-E cascode topology, large voltage swing is applied on the CG amplifier [21]. Thick gate–oxide transistors prevent breakdowns and they are biased to be on-state all the time, lowering on-resistance to maintain high efficiency.
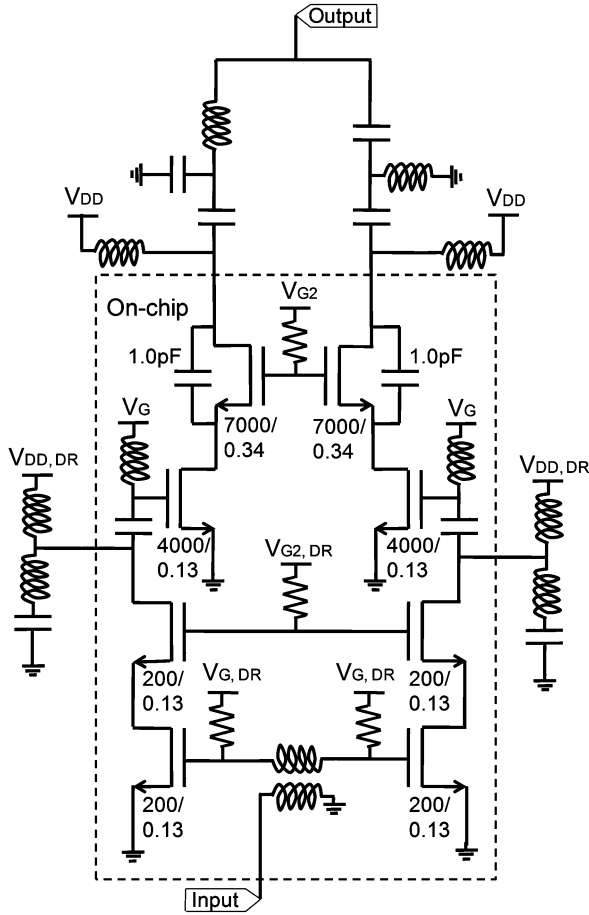
Fig. 6. Schematic of proposed differential PA with cascode topology, including driver amplifiers and input balun, realized in a 0.13-μm CMOS technology.

Fig. 7. Chip photograph of proposed CMOS class-E PA.

For the CG amplifier, total gatewidths of 7000-μm transistors were implemented. The entire schematic is described in Fig. 6.

B. Driver Stage

For the driver stage, a class-E amplifier is implemented. Since a class-E amplifier has a large voltage swing on its output, it can drive the main amplifier sufficiently with low supply voltage. Low supply voltage on the driver amplifier consumes low dc power so it reduces efficiency degradation from DE to power-added efficiency (PAE). Double-resonance circuit is also considered for designing load impedance of the driver stage. In this study, the difference in efficiency between DE and PAE is only 3–4 %-points. We also chose cascode topology to prevent break-downs of the thin gate–oxide transistors, which have 200-μm gatewidths.

In addition, a transformer was implemented on a chip as an input balun. This transformed the single-ended structure to a differential structure in order to drive differential amplifiers.

C. Double-Resonance Circuit

Shaping the voltage waveform at the input of the main amplifier was accomplished by using a double-resonance circuit. As described in Section III, an inductor on the main amplifier gate was used as part of the resonance circuit and it resonated with the main amplifier input capacitance at the operation frequency.
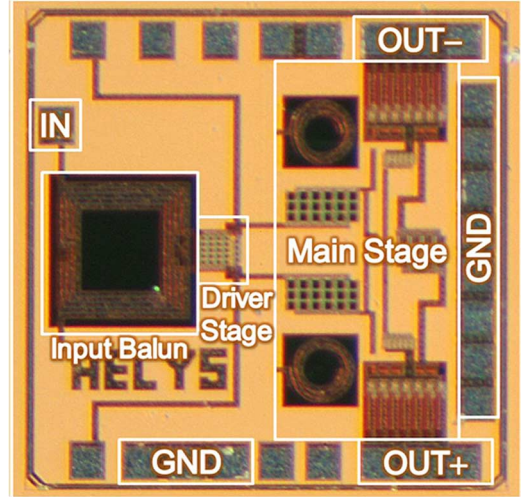
The other resonator is attached on the output of driver amplifier using the series LC resonator. This series resonator deprives the second harmonic from the signal flowing to the main amplifier input and allows the third harmonic to trespass into the main amplifier.

The proposed double-resonance circuit reduces voltage stress on the CS amplifier implemented with a thin gate–oxide transistor on the main stage cascode structure, and shapes the voltage waveform without deteriorating the PA performance and duty cycle. We simulated its effectiveness using the Advanced Design System (ADS) and 0.2-V voltage stress was relieved from the CMOS transistor.

D. Negative Capacitance

The negative capacitance (C_n) is connected to the input and output of the CG amplifier in the main stage. It compensates for surplus capacitance on C_P, restoring it to its optimum value. This scheme provides negative capacitance simply with a capacitor, without an additional circuit, to generate negative capacitance.

There is tradeoff between the value of C_n and stability because C_n provides a feedback path on the CG amplifier. However, thanks to the CG amplifier gain K, the required capacitance value of C_n is small and a 1.0-pF capacitor was inserted in our design. On simulation assisted by ADS, stability degradation was not observed. In addition, this negative capacitance compensated about 10.0 pF of C_P and PAE was enhanced by about 6 %-points in simulation.

VI. MEASUREMENT AND RESULTS

The proposed PA, including the driver stage and input balun, is fabricated using the 0.13-μm standard CMOS process. The chip photograph is shown in Fig. 7. The die area, including the bonding pads, is 1.0 mm^2. We used multiple bonding pads to minimize the effects from bonding inductance variation. Twelve pads were implemented to reduce ground resistance and provide PA heat sink. Off-chip passive components were implemented on an FR4 printed circuit board (PCB).
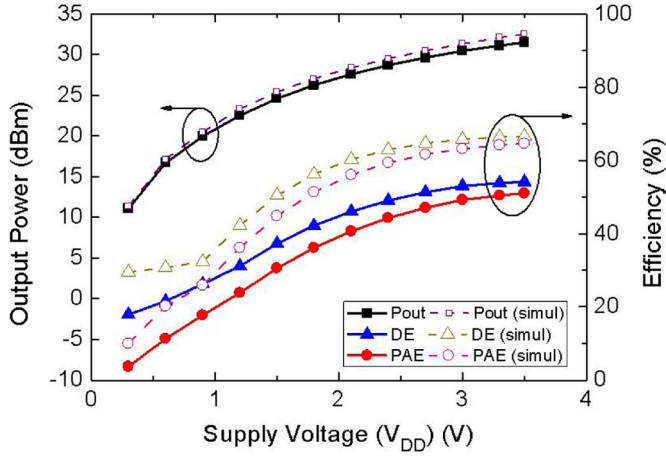
Fig. 8. Measured (solid line) and simulated (dashed line) output power (P_{out}), DE, and PAE versus supply voltage V_{DD}.
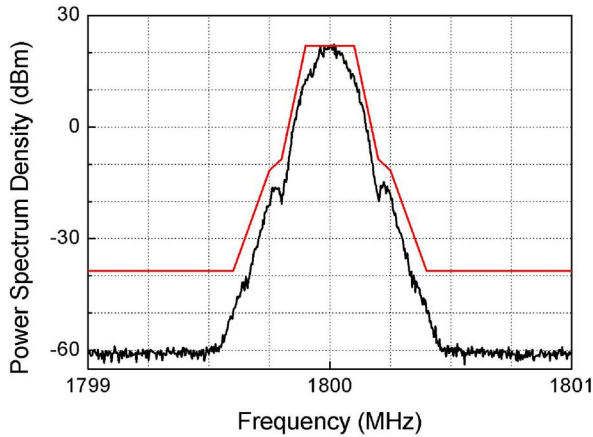

Fig. 10. Measured output power (P_{out}), DE, and PAE versus operating frequency.

Fig. 9. Measured output spectrum and emission mask of GSM.
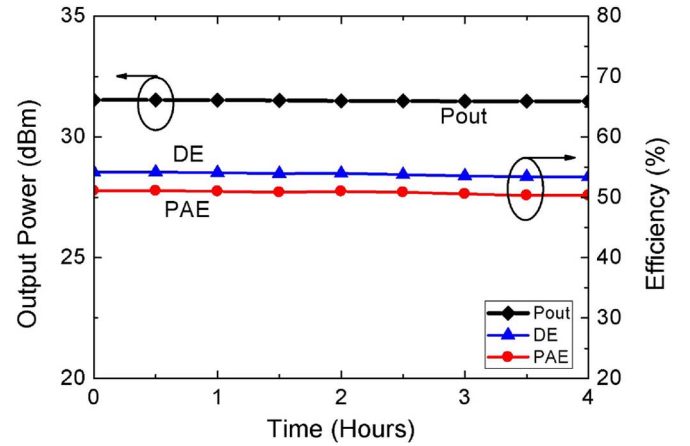
Fig. 11. Measured output power (P_{out}), DE, and PAE versus time.

The measured and the simulated DE and PAE versus main supply voltage V_{DD} are plotted in Fig. 8, along with output power, at 1.8 GHz. V_{DD} varies from 0.3 to 3.5 V with maintained 2.5-V CG amplifier gate bias during the sweep. 31.5-dBm output power, and DE and PAE were measured as 54% and 51%, respectively, with $V_{DD} = 3.5$ V. V_{DD} increasing from 3.3 to 3.5 V resulted in 0.4-dB output power increment on measurement. For the test, input signal was set as 6.5 dBm and a 25-dB power gain was achieved.

The class-E PA is a switching amplifier, thus, constant envelope modulation signals are suitable. To test this PA, the GMSK modulated signal with 0.3 bandwidth time (BT) product is applied, and the measured spectrum is shown in Fig. 9. With average output power of 31.5 dBm, this PA satisfies the given spectrum mask with 0.6% error vector magnitude (EVM). The second and third harmonic suppressions were obtained as 52 and 29 dBc, respectively. Due to the differential architecture, the second harmonic is clearly suppressed.

Fig. 10 shows DE, PAE, and output power according to operating frequency. Maximum output power was measured as 31.5 dBm at 1.8 GHz. The maximum DE and PAE were measured as 58% and 54%, respectively, at 1.9 GHz with 31-dBm
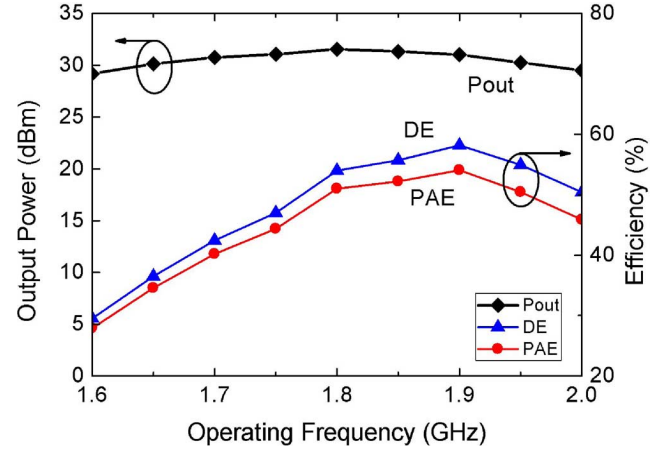
output power. Over the range from 1.6 to 2.0 GHz, more than 29-dBm output powers were measured.

Fig. 11 demonstrates the reliability of our cascode class-E PA. We operated the PA at maximum output power for 4 h. Over the course of 4 h, we checked output power, DE, and PAE, maintaining $V_{DD} = 3.5$ V. We could not observe obvious output power and efficiency degradation during the test. Output power dropped only 0.05 dB, and DE and PAE were dropped 0.7% and 0.8%, respectively, after 4-h operation.

Finally, to compare the performance of this study against state-of-the-art CMOS PAs, we used the figure of merit (FoM) introduced by the International Technology Roadmap for Semiconductor (ITRS), which normalizes major performances such as output power (P_{out}), PAE, power gain (G), and the square of operating frequency (f_0^2) [30]

$$\text{FoM}_{\text{PA}} = P_{\text{OUT}} \cdot \text{PAE} \cdot G \cdot f_0^2. \tag{10}$$

FoM_{PA} with relative works, differential structure CMOS PAs around watt-level output power, are plotted in Fig. 12 according to maximum output power. This proposed PA shows high performance compared to other studies.
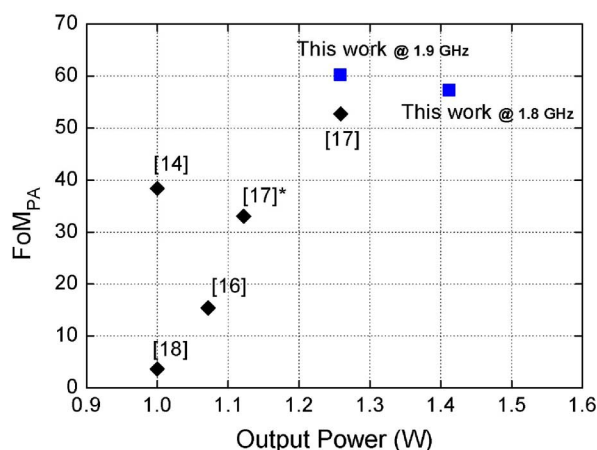
Fig. 12. Comparison of watt-level CMOS PAs (differential structure) through ITRS $\mathrm{FoM_{PA}}$. * indicates integrated output balun.

VII. CONCLUSION

In this paper, we presented a differential class-E PA, including a double-resonance circuit using harmonic control, and it reduced voltage stress on the transistors. We also used a negative capacitance to compensate for surplus capacitance on the drain of a class-E amplifier in order to achieve high efficiency with cascode topology. This amplifier delivers 31.5-dBm output power with 54% DE and 51% PAE at 1.8 GHz using the 0.13-μm standard CMOS process. There was almost no performance degradation during 4-h maximum power operation.

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