A 28-GHz Class-J Power Amplifier with 18-dBm output power and 35% peak PAE in 120-nm SiGe BiCMOS

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***Abstract*— A 28-GHz Power Amplifier (PA) designed in 120-nm SiGe BiCMOS for potential use in mobile millimeter-wave phased arrays is presented in this paper. The core of the PA is a cascode amplifier operated in class-J mode. A multi-harmonic load-pull analysis was used to determine the optimum harmonic output impedances (up to third harmonic) resulting in improved efficiency. The PA has a measured 15.3-dB small signal gain, 18.6-dBm saturated output power and 35.3% peak power added efficiency (PAE) at 28GHz. At 1-dB compression the PA has a 15.5-dBm output power and 31.5% PAE.**

***Index Terms*— Power amplifiers, class J, SiGe, millimeter-wave.**

I. Introduction

The available bandwidth and reduced wavelengths at Ka band (27-40 GHz) enable gigabit-per-second communications for mobile millimeter-wave broadband (MMB) networks, providing an alternative approach to realize next-generation cellular systems [1]. These MMB systems require moderate beamforming which in turn require extremely efficient transmitter and receiver circuitry. In this paper, a 28-GHz Class-J PA is presented which achieves a state-of-the-art peak efficiency as well as favorable back-off efficiency to allow operation with complex-modulated signals. The main objective of this PA design was to achieve >30% peak efficiency, greater than 16-dBm output 1-dB compression point (oP_{1dB}) and a small-signal gain greater than 15dB across the band. Finally, a compact area was desired to allow the PA to be easily integrated into a small Ka-band phased array. As will be shown, all of these goals can be met with a SiGe cascode amplifier operating in class-J. The paper is organized as follows: Section II discusses the design methodology and optimization of multiple device and circuit parameters for peak performance, Section III presents the layout details and measurement results, and Section IV presents the summary.

II. Class-J PA design

A simplified schematic of the PA is shown in Fig. 1. The core of the PA is a cascode amplifier, chosen because of its higher gain, better reverse isolation and higher output voltage swing. The linear voltage swing at the collector is maximized by allowing the peak collector voltage across Q2 to approach the BV_{CBO} limit. The peak collector to emitter voltage across Q2 is given by $2(V_{CC}-V_k)$ where V_{CC} is the supply voltage and V_k is the knee voltage. As a result, a high V_{CC} of 3.6 V was used for the PA. A benefit of higher voltage swing for a given linear output power is that the current swing is reduced, allowing smaller transistors with lower parasitic capacitances. The total emitter area of the transistors (emitter width:120nm, emitter length:10um, fingers:4) was found from the current amplitude requirements dictated by the linear output power specification and the voltage amplitude.

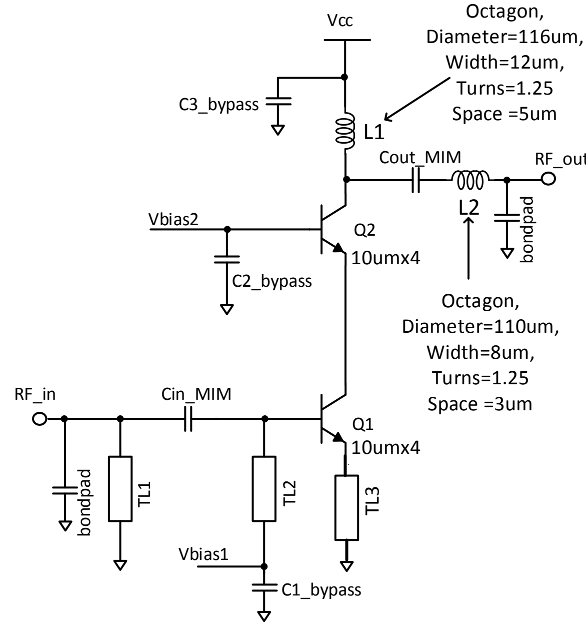

Fig. 1. Class-J PA schematic

The starting point for the design of a class-J PA is a class-AB PA. The bias current density of the transistors were initially set to the peak-f_T current density and then scaled down to operate the PA in class-AB mode. Reduction of the bias current density reduces the gain while improving drain efficiency. Furthermore, the linear output power stays constant or slightly improves up to light class-C modes, after which excessive non-linearity in form of gain expansion starts showing up. In this design, we choose the bias current density that would be sufficient to provide

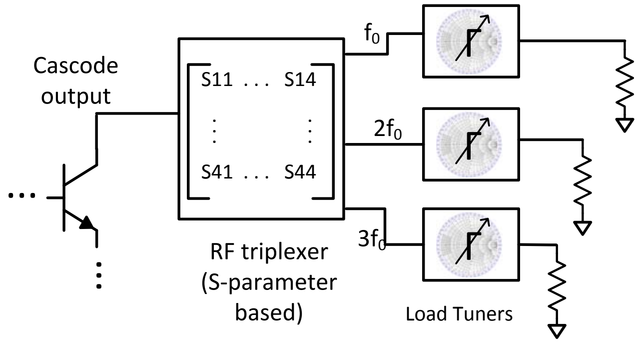

Fig. 2. Multi-harmonic load pull set up

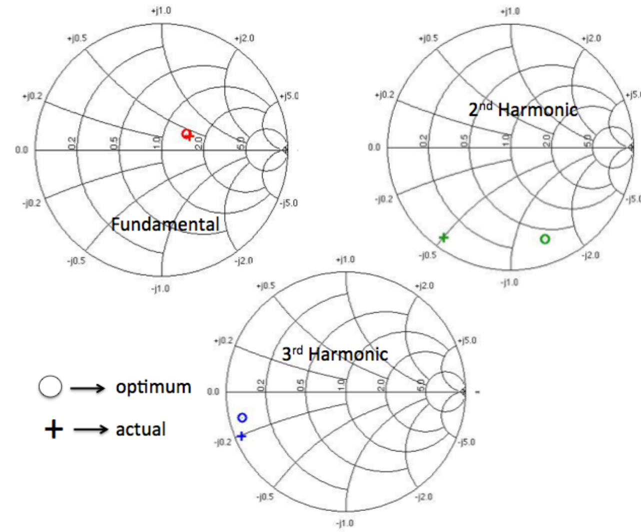

Fig. 3. Optimum harmonic impedances

a small signal gain of 17-dB and would operate the PA in deep class-AB mode near 1-dB compression.

Matching of the PA was optimized for maximum power transfer at the input and peak power-added efficiency at the output. The input match was conjugate matched to 50Ω using a π- network of shunt microstrip lines and series MIM capacitor. For the output match, a multi-harmonic load-pull simulation was performed, where an ideal triplexer is used to separate the signal into fundamental, 2^{nd}, and 3^{rd} harmonics(Fig. 2). Load pulls are then performed successively at each harmonic to determine the optimum harmonic matching conditions. The resultant harmonic loads are depicted in Fig. 3, showing the optimum condition as well as the achieved match. The optimum fundamental impedance was complex with a small reactance and the optimum second harmonic impedance was mostly reactive, both of which are indicative of a class-J mode of operation. Further the class-J mode eliminates the necessity of harmonic shorts, as in conventional class-AB PAs, or harmonic opens, as in class-F switching PAs, resulting in broadband operation and reduced chip area [2]-[4]. In our design, the output matching network was designed to provide the near optimum impedance at both the fundamental and 3^{rd} harmonic. The second harmonic impedance was allowed to be sub-optimum because matching both the fundamental and second harmonic impedance needed a higher order matching network which would have increased both chip area and output losses. Simulation results of the PA showed a 17.8-dB gain, 18-dBm saturated output power (P_{sat}), 41% peak PAE and 17-dBm oP_{1dB}.

III. Layout and Measurement Results

The technology used was IBM 120-nm SiGe BiCMOS 8HP featuring NPN transistors with peak f_T/ f_{MAX} of 200/ 265 GHz, BV_{CEO} = 1.5 V, and BV_{CBO}= 5.5 V. The PA transistors were laid out in CBEBC (C-collector, B-base, E-emitter) style with 4 parallel devices. Multiple fingers/devices were necessary to meet electromigration current density for the interconnects at 100° C. Microstrip transmission lines with side shields were used to realize inductances less than 150 pH, whereas small spiral inductors with patterned ground shields were used to realize

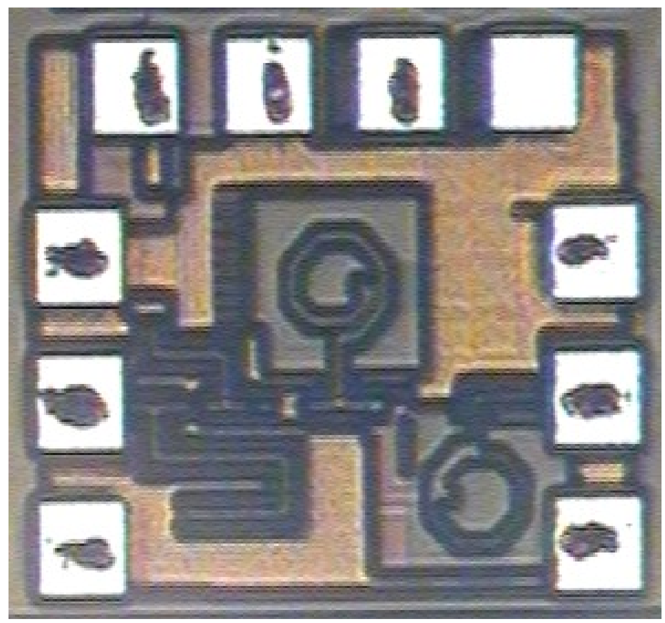

Fig. 4. Chip microphotograph

inductances higher than 200 pH. The existing inductor models in the 8HP design kit showed good agreement with HFSS electromagnetic simulations and no further passive modelling was required. The chip microphotograph is shown in Fig 4. The chip measures .61 mm by .73 mm including pads.

The PA measurements were performed with a collector supply voltage of 3.6 V and a collector bias current of 17 mA. S-parameter simulation and measurement results of the PA are shown in Fig 5. The input match S_{11} shows close agreement with the simulations whereas S_{22} is slightly offset. The gain at 28-GHz is 15.3 dB, about 2-dB lower than the simulated result due to additional parasitic inductance in Q1's emitter. The gain is very broadband

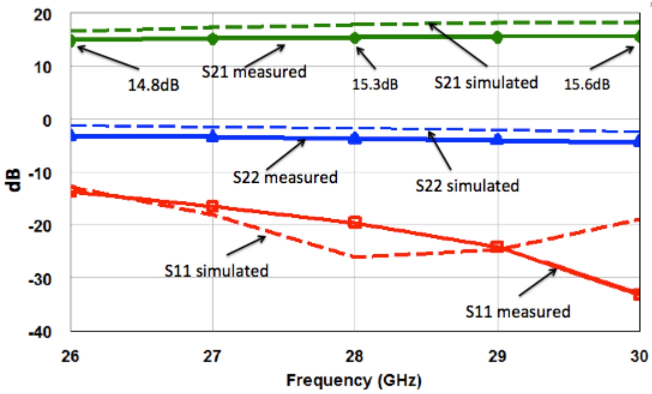

Fig. 5. Measured and simulated S-parameters of the PA

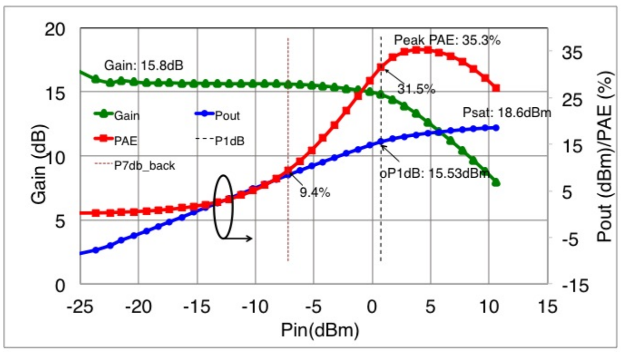

Fig. 6. Swept power measurement results of the PA

with less than 0.8-dB variation in the 26-30 GHz frequency range. Fig 6 presents the measured gain, output power and PAE versus input power at 28 GHz. The saturated output power is 18.6dBm, oP_{1dB} is 15.5dBm, peak PAE is 35.3% , PAE at 1-dB compression is 31.5% and PAE at 7-dB back-off is 9.4% at 28 GHz. This backed-off PAE is particularly important for when the PA is used to linearly and efficiently amplify signals having complex modulation, as is envisioned for the 28-GHz mobile millimeter-wave broadband system. Table I shows the performance of the PA across the 27-29 GHz band. The gain, P_{sat} and oP_{1dB} show small variation across the band.

IV. Summary

A fully integrated class-J PA working in the 28-GHz band was presented in this paper. The performance metrics summarized in Section III show that the class-J PA could be a good alternative to other PA modes at millimeter-wave frequencies for achieving a good PAE without sacrificing linearity and bandwidth. A performance comparison with state-of-the-art millimeter-wave PAs is shown in Fig. 7. Due to non-availability of recently published results in the 26-30 GHz frequency range, results from Ka-band, Q-band and V-band are also included for comparison. To the best of our knowledge, the PA achieves the highest peak PAE and 1-dB compression PAE in Silicon technologies.

TABLE I
Performance of the class-J PA across band

Frequency (GHz)	27	28	29
Gain (dB)	15	15.3	15.5
P_{sat} (dBm)	18.9	18.6	18
oP_{1dB} (dBm)	15.1	15.5	15.9
Peak PAE (%)	33.8	35.3	34.7
PAE 1-dB comp. (%)	27.6	31.5	33.2
PAE 7-dB-back-off (%)	9	9.4	11.3

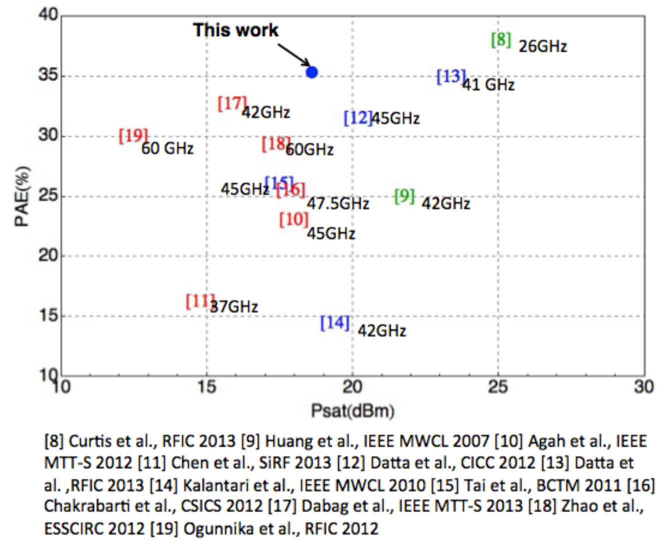

Fig. 7. Comparison with state-of-the-art PA results in CMOS(red), SiGe(blue), GaAs(green) technolgies

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References

[1] Z. Pi and F. Khan, "An introduction to millimeter-wave mobile broadband systems," *IEEE Comm. Mag.*, June 2011, pp. 101-107.

[2] Steve C. Cripps, "RF Power Amplifiers for Wireless Communications," 2nd ed. Boston, MA: Artech House, 2006.

[3] P. Wright, J. Lees, J. Benedikt, P. J. Tasker and S.C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a linear and broadband PA," *IEEE Transactions on Microwave Theory and Techniques*, vol.57, no.12, pp.3196-3204, Dec. 2009.

[4] N. Tuffy, A. Zhu, T. J. Brazil, "Class-J RF Power Amplifier with Wideband Harmonic Suppression," *2011 IEEE MTT-S Int. Microwave Symp. Dig.*, vol.1, no.4, pp.5-10, June 2011.

[5] C. M. Grens, Peng Cheng, and J. D. Cressler, "Reliability of SiGe HBTs for Power Amplifiers-Part I: Large-Signal RF Performance and Operating Limits," *IEEE Trans. Device Mater. Rel.* , vol.9, no.3, pp.431-439, Sept. 2009.

[6] Junghwan Moon, Juyeon Lee, R. S. Pengelly, R. Baker, and Bumman Kim, "Highly Efficient Saturated Power Amplifier", *IEEE Microwave Magazine*, vol.13, no.1, pp.125-131, Jan.-Feb. 2012

[7] T. Yao, M. Gordon, K.K.W Tang, K.H.K Yau, M. Yang, P. Schvan and S.P. Voinigescu , "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE J. Solid-State Circuits*, vol.42, no.5, pp.1044-1057, May 2007