A Power-Efficient 4-element Beamformer in 120-nm SiGe BiCMOS for 28-GHz cellular communications

Anirban Sarkar, Kevin Greene and Brian Floyd
Department of Electrical and Computer Engineering
North Carolina State University, Raleigh, NC 27606
Email: {asarkar3, kbgreen2, bafloyd}@ncsu.edu

***Abstract*—A 4-element beamformer designed in 120-nm SiGe BiCMOS technology for 28-GHz mobile millimeter-wave broadband system is presented in this paper. Each element of the beamformer consists of a 4-bit active phase shifter and a two-stage Power Amplifier (PA). A two-stage PA design with a Class-C pre-driver and a 2nd-harmonic-tuned Class-AB driver stage is adopted for high gain and high efficiency at both peak and backed-off power levels. The active phase shifter employs in-phase/ quadrature phase current steering and digital control of transconductance (Gm). Measurement results show a 33-dB gain, 16.5-dBm saturated output power, 15.7-dBm oP_{1dB}, 27.5% peak PAE and 8.2% 7-dB back-off PAE at 27 GHz for a single element. The minimum (maximum) RMS gain and phase errors across the 27-29 GHz band were 0.5 dB (3 dB) and 1.5°(12°). The beamformer also includes a 1:4 power splitter and a serial interface for digital control and occupies a die area of 5.32mm^2.**

***Index Terms*—phased array, 28-GHz, SiGe, millimeter-wave.**

I. Introduction

The ever-increasing demand for high speed mobile data has encouraged the use of millimeter-wave frequency bands for future cellular communication systems. In [1] and [2] the feasibility of a 1-Gbps data rate mobile millimeter-wave broadband(MMB) system using the LMDS bands around 28 GHz was studied. The uplink (handset to base-station) budget suggests the necessity of moderate beamforming, high output power, power efficient and linear transmitter circuitry. Although phased array transmitters have been demonstrated in Ka-band, there has been little effort on improving the efficiency of the overall system at backed-off power levels. This paper demonstrates a fully integrated 4-element array working in the 27-29 GHz band that achieves efficiency and linearity performance that is suitable for use in a mobile handset with a compact area.

We target an EIRP greater than 20 dBm for a 1-Gbps link at 500 m with a 4-element array assuming 0 dBi unit antenna gain. Considering 7-dB back-off for good linearity performance, this translates to a 16-dBm 1-dB compressed output power (oP_{1dB}) per element. To limit the total dc power consumption of the array to 320 mW, a front-end efficiency greater than 10% at 7-dB back off is required. To achieve the oP_{1dB} and PAE targets, we adopt a two stage PA design with a 2nd-harmonic-tuned Class-AB driver stage delivering a high saturated output power with good Power-Added Efficiency(PAE) and a class-C pre-driver stage improving the linearity and gain of the PA while having a minimum effect on PAE. An active vector interpolator based topology is chosen for the phase shifter in order to achieve full 360° phase shift, low gain and phase errors, additional gain and high oP_{1dB} to linearly drive the PA. The next section presents the circuit design techniques adopted to achieve high performance. Section IV presents the measurement results followed by a summary.

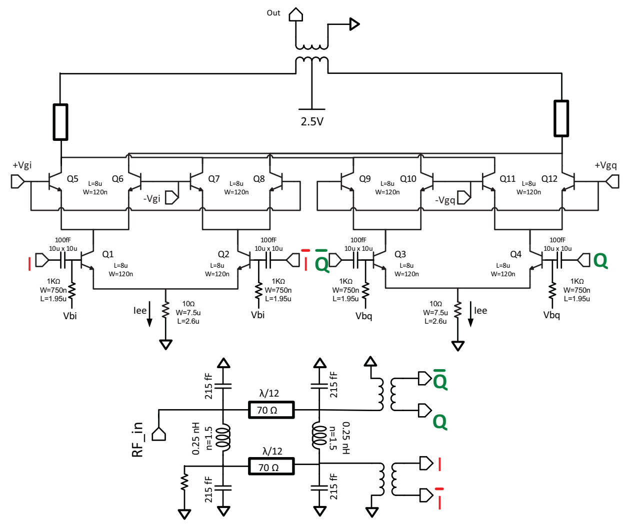

Fig. 1: Phase Shifter schematic.

II. Circuit Design

The beamformer has three stages: a power splitter, a phase shifter and a two-stage PA. The 1:4 power splitter consists of two levels of cascaded 1:2 Wilkinson power splitters. The quarter-wave resonators of the Wilkinson splitter are implemented as single section T-networks of two series MIM capacitors and one shunt spiral inductor for compact area and low loss.

A. Phase Shifter

The phase shifter is realized using a vector-interpolator topology, as shown in Fig. 1. In-phase and quadrature-phase RF signals are created using a lumped-element equivalent of a branchline coupler. The $\sqrt{2}Z_0$ quarter-wave lines have been realized with 70-Ω $\lambda/12$ series transmission lines and 115-fF shunt capacitors. The Z_0 quarter-wave lines have been realized

978-1-4799-7230-2/14/$31.00 ©2014 IEEE

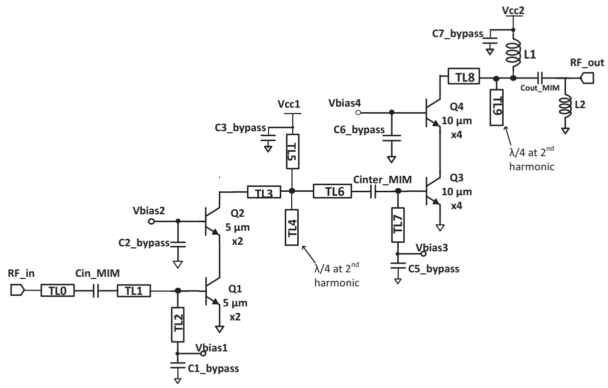

Fig. 2: Two stage PA schematic.

with 0.25-nH series inductors and 100-fF shunt capacitors. Differential I and Q signals are created using two single-turn transformers each with 150-μm diameter. The coupler was simulated using a combination of SONNET [13] and design-kit models, and showed less than 2.5° rms phase error and < 0.3-dB rms gain error across 27-29 GHz. The total area of the differential quadrature hybrid is 430x530-μm^2, and this area includes space for all of the active circuitry within the vector interpolator.

The active portion of the phase shifter uses a differential current-steered (or Gilbert-cell) design [3],[4]. A *tanh*-based current steering function is implemented using cross-coupled cascode devices. These cross-coupled devices are controlled through an inverse-*tanh* pre-distortion circuit driven by sin-weighted DACs targeting 4-bit accuracy. The input transconductance (Gm) is ideally fixed to provide constant impedance loading to the coupler; however, Gm can be compensated to calibrate the gain and phase response across phase settings and frequency if needed. Simulations for the phase shifter indicate 8.8-dB gain, 11-dB noise figure, and -6.6 dBm oP_{1dB}, while consuming 36 mW from 2.5-V supply.

B. 2-stage Power Amplifier

A simplified schematic of the two-stage PA is shown in Fig. 2. The driver stage is similar to the single-stage PA presented in [5] with improvements to the output match and base bypass network of the common-base transistor. A cascode amplifier is used with devices having an emitter length of 10 μm and 4 fingers biased in class-AB mode with an approximate conduction angle of 240°. The optimum harmonic terminations at fundamental $(70 + j25)\Omega$, 2nd harmonic $(8 - j60)\Omega$ and 3rd harmonic $(-j10)\Omega$ were determined using a multi-harmonic load pull as described in [5] and indicate a continuous mode class-B/J operation as the optimum one for maximum PAE. In this work the output matching network is designed to have the ability to tune the 2nd-harmonic impedance independently of the fundamental impedance. This is accomplished by using a 2nd-harmonic-quarter-wave open stub(TL9) [8]. The 2nd harmonic impedance can be tuned using the series microstrip line TL8; the fundamental can be tuned using the portion of the network to the right side of TL9. The fundamental and second harmonic impedances provided by the matching network are $(76-j8)\Omega$ and $(40-j83)\Omega$ respectively. Note that the fundamental and second harmonic impedances provided by this network have a different relationship compared to the continuous modes discussed in [6]-[7] because both have a capacitive reactance part. This causes the voltage swing to move into the knee region which would theoretically result in loss of linearity, output power and efficiency[7]; however the efficiency and output power improve because the network has a higher quality factor compared to the one with inductive fundamental reactance.

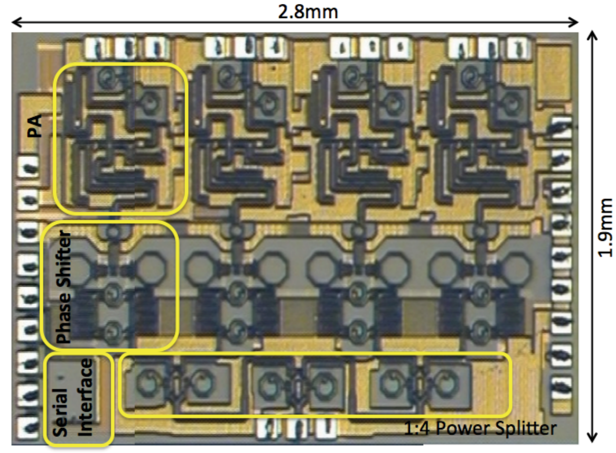

Fig. 3: Chip microphotograph.

A class-C pre-driver stage was added to improve the overall gain and linearity of the PA. The pre-driver stage is also a cascode amplifier with four times smaller devices, half the collector supply voltage compared to the driver stage and an approximate conduction angle of 170° to minimize dc power consumption and have less impact on overall efficiency. The class-C PA shows a tunable gain expansion characteristic versus swept input power which can be used to partially compensate for the gain compression of the driver-stage PA and improve the oP_{1dB}. The compensation is imperfect because the overall gain in the compensated region is not flat but shows some expansion/compression limited to +/-1dB. As such the PA would benefit from digital pre-distortion to improve its EVM in this region. The input of the pre-driver is conjugately matched to 50-Ω whereas the interstage matching network design between the pre-driver and the driver stage involves a trade-off between gain, bandwidth and PAE. We design the interstage matching network for maximum PAE at 28 GHz with the restriction that the gain variation in the 27-29 GHz band is limited to one decibel. The optimization of PAE while maintaining a certain gain flatness involved the simultaneous use of load pull contours and gain circles.

Simulation results of the PA show a 30-dB gain, 18-dBm saturated output power (P_{SAT}), 17-dBm oP_{1dB}, 37% peak PAE and 15% 7-dB-back-off PAE at 28 GHz. Simulation results of the array show a 33-dB gain, full 360°phase shift, RMS gain and phase errors less than 0.3 dB and 3° in the 27-29 GHz band for 4-bit phase shift, 17-dBm oP_{1dB}, 32% peak PAE and 12% 7-dB-back-off PAE.

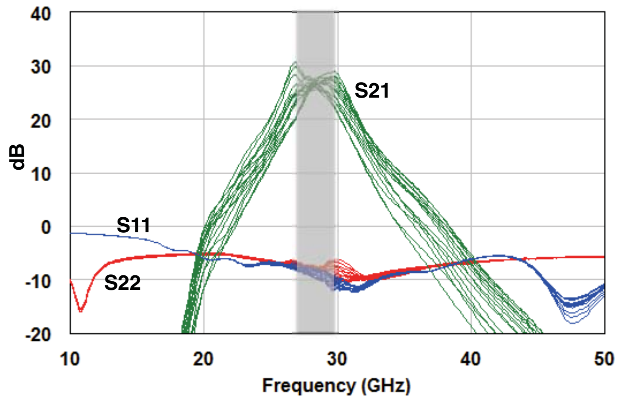

Fig. 4: Measured S-Parameters of a single beamformer element.

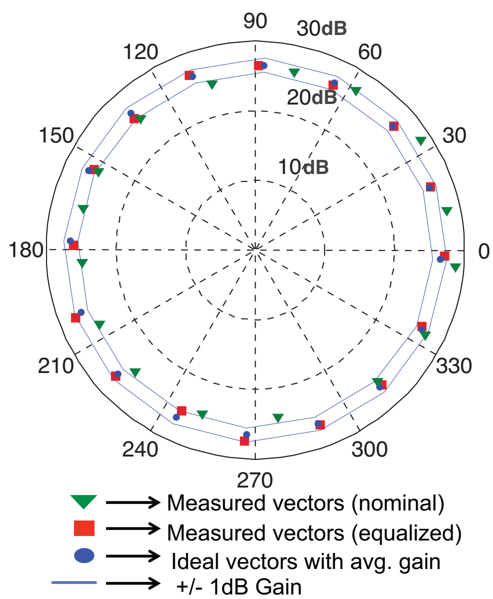

Fig. 5: Measured vectors of a single beamformer element at 28.14 GHz.

III. Layout and Measurement Results

The design is implemented in IBM 120-nm SiGe BiCMOS 8HP technology featuring NPN transistors with peak f_T/ f_{MAX} of 200/ 265 GHz, BV_{CEO} = 1.5 V, and BV_{CBO}= 5.5 V. The full chip meets electromigration current density requirements at 100°C. Passive elements used for matching networks were microstrip lines, MIM capacitors and spiral inductors. Additional loss was incorporated into the design kit models of microstrip lines and spiral inductors based on EM simulations. The base bypass capacitances at the common base transistors were realized using a combination of MOS capacitors and custom designed Metal-Oxide-Metal capacitors for low resistance and high capacitance density. The die photo is shown in Fig. 3. The chip measures 2.8mm by 1.9mm including RF and dc pads.

All measurements were performed with collector supply voltages of 2.5 V, 1.8 V and 3.6 V for the phase shifter,

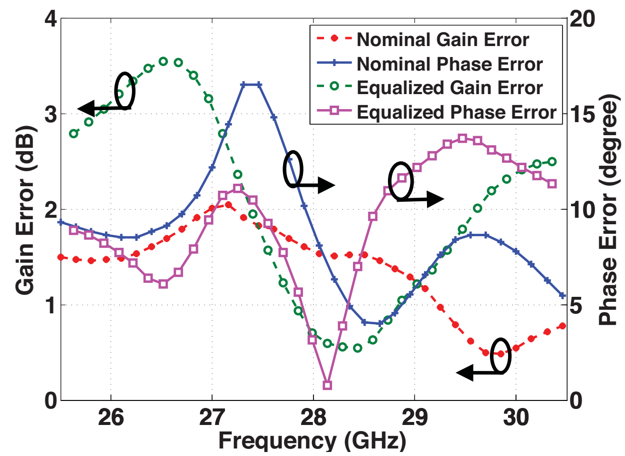

Fig. 6: Measured RMS gain and RMS phase errors for nominal and equalized cases.

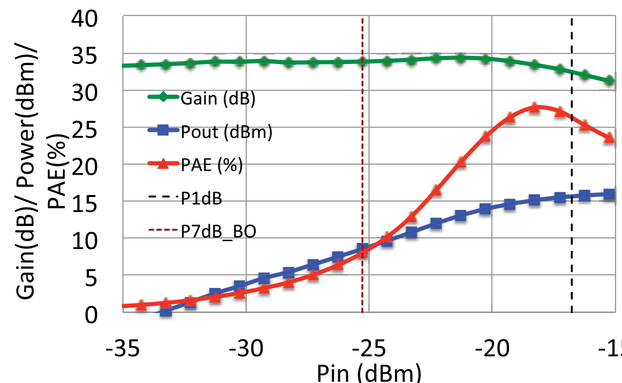

Fig. 7: Swept power measurements at 27 GHz.

pre-driver and driver stages respectively. S-parameter measurements of the beamformer showed a gain variation across frequency and phase setting, indicating a quadrature gain/phase error within the phase shifter. Revised EM simulations of the transformers used in the quadrature generation circuit in HFSS [14] indicated a nearly 3-dB gain difference between the differential components of both I and Q vectors. Using the additional control settings within the phase shifter Gm and current-steering DACs, it is possible to calibrate out the I/Q gain error at a particular frequency to obtain an equalized phase shifter gain and phase response. Fig.4 shows the s-parameters with these equalized phase-shifter settings for 28.14 GHz. The polar plot in Fig. 5. shows the measured vectors for nominal and equalized settings along with the ideal vectors at 28.14 GHz. RMS gain error and phase error across the band are presented in Fig. 6. The beamformer achieves a 27-dB end-to-end gain, full 360° phase shift, 3-dB bandwidth of 26-30 GHz, RMS gain error of 0.5-3 dB and RMS phase error of 1°-11.5° in the 27-29 GHz band. Measured gain variation across the four-elements of the array for a given phase and frequency was +/-3dB, which is due to a cross-chip variation of a supply voltage used within the bias circuit of the PAs.

Swept power measurement results of a single element at

27 GHz and 337.5° phase shift are shown in Fig. 7. The beamformer element achieves a 33.2-dB gain, 16.5-dBm P_{SAT}, 15.7-dBm oP_{1dB}, 27.5% peak PAE, 25.6% 1-dB-compression PAE and 8.2% 7-dB back-off PAE. Swept power performance across the band for a phase shift of 337.5° is summarized in Table I. P_{SAT} and oP_{1dB} show less than 1-dB variation, whereas PAE metrics show less than four percentage point variation. Measurements across the 16 phase settings for a fixed frequency show less than 1.5-dB variation in power metrics and less than four percentage point variation in PAE metrics. Measurements for 2 other chip samples show similar results.

IV. Summary

The 4-element beamformer presented in this work has shown the capability to generate an EIRP greater than 21 dBm assuming 0 dBi unit antenna gain with a total dc power consumption less than 380 mW at 7-dB-back-off using a commercial SiGe BiCMOS technology. The circuit design techniques mentioned in Section II, namely, optimum harmonic terminations, analog pre-distortion using pre-driver stage enabled high performance. The efficiency and linearity achieved makes it an useful solution for mobile devices using MMB for Gbps communications. A performance comparison with some of the phased array results from different millimeter-wave frequency bands is shown in Table II. To the best of our knowledge, this beamformer achieves the highest peak and back-off PAE among the millimeter-wave beamformers/ phased arrays designed in Silicon-based technologies.

Acknowledgment

This work was partially funded by Samsung Electronics. The authors wish to thank F. Aryanfar, Z. Pi for helpful discussions and Y. Takeda, T. Fujibayashi for their assistance in layout and measurement.

TABLE I: Performance of the beamformer across band

Frequency (GHz)	27	28	29
Gain (dB)	33.2	30.6	29.8
P_{sat} (dBm)	16.5	16.5	16.9
oP_{1dB} (dBm)	15.7	15.8	16.9
Peak PAE (%)	27.5	24.3	26.2
PAE 1-dB comp. (%)	25.6	22.3	26.1
PAE 7-dB-back-off (%)	8.2	8.5	10.3

TABLE II: Performance comparison with millimeter-wave beamformers

Reference	Frequency (GHz)	Gain (dB)	RMS Gain Error (dB)	RMS Phase Error (°)	oP_{1dB} per element (dBm)	Peak PAE (%)	PAE at 7-dB-back-off(%)	Technology
This work	27-29	33.2	0.5-3	1.5-11.5	15.7	27.5	8.2	SiGe 120nm
[9] Koh *et. el.*	40-45	12.5	<1.5	<8.8°	-3.5	-	-	SiGe 180nm
[10] Tabesh *et. el.*	57.9-65.6	-	-	-	-1.5	20	-	CMOS 65nm
[11] Valdes-Garcia *et. el.*	58-65	35	1dB	<5	15	8	-	SiGe 120nm
[12] Mortazavi *et. el.* (PA only)	26-30	9	-	-	15	40	5	SiGe 120nm

References

[1] Z. Pi and F. Khan, "An introduction to millimeter-wave mobile broadband systems," *IEEE Comm. Mag.*, June 2011, pp. 101-107.

[2] F. Khan, Z. Pi and S. Rajagopal, "Millimeter-wave Mobile Broadband with Large Scale Spatial Processing for 5G Mobile Communication," *Proc. 50th Annual Allerton Conference on Communication, Control, and Computing*, Oct. 2012, pp.1517-1523

[3] Ming-Da Tsai and A. Natarajan, "60GHz passive and active RF-path phase shifters in silicon," *IEEE RFIC Symp. Dig. Tech. Papers*,June 2009, pp.223-226

[4] Kwang-Jin Koh and G. M. Rebeiz, "0.13-μm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays"*IEEE Journal of Solid State Circuits*, Nov 2007, vol.42, no.11, pp.2535-2546

[5] A. Sarkar and B. Floyd, "A 28-GHz Class-J Power Amplifier with 18-dBm output power and 35% peak PAE in 120-nm SiGe BiCMOS," *IEEE SiRF Dig. Tech. Papers*, Jan. 2014

[6] Steve C. Cripps, "RF Power Amplifiers for Wireless Communications," 2nd ed. Boston, MA: Artech House, 2006.

[7] T. Canning, P. J. Tasker and S. C. Cripps, "Continuous Mode Power Amplifier Design Using Harmonic Clipping Contours: Theory and Practice,"*IEEE Transactions on Microwave Theory and Techniques*, Jan. 2014,vol.62, no.1, pp.100-110

[8] J. Moon, J. Lee, R. S. Pengelly, R. Baker, and B. Kim, "Highly Efficient Saturated Power Amplifier", *IEEE Microwave Magazine*, Jan.-Feb. 2012, vol.13, no.1, pp.125-131

[9] Kwang-Jin Koh, J. W. May, G. M. Rebeiz, "A Millimeter-Wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18-μm SiGe BiCMOS Technology", *IEEE Journal of Solid State Circuits*, May 2009, vol.44, no.5, pp.1498-1509

[10] M. Tabesh et. al.,"A 65 nm CMOS 4-Element Sub-34 mW/Element 60 GHz Phased-Array Transceiver",*IEEE Journal of Solid State Circuits*, Dec 2011, vol.46, no.12, pp.3018-3032

[11] A. Valdes-Garcia et. al., "A 16-element, SiGe BiCMOS phased-array transmitter for 60-GHz communications",*IEEE Journal of Solid State Circuits*, Dec 2010, vol. 45, no. 12, pp. 2757-2773

[12] S. Y. Mortazavi et. al., "A Class F^{-1}/F 24-to-31GHz Power Amplifier with 40.7% Peak PAE, 15dBm OP1dB, and 50mW Psat in 0.13μm SiGe BiCMOS", *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014

[13] Sonnet ver. 12.56, Sonnet Software Inc., Syracuse, NY, 1986-2011.

[14] Ansoft HFSS ver. 15, Ansoft Corporation, Pittsburgh, PA, 2013.