A Charging Acceleration Technique for Highly Efficient Cascode Class-E CMOS Power Amplifiers

Ockgoo Lee, *Student Member, IEEE*, Jeonghu Han, *Member, IEEE*, Kyu Hwan An, *Student Member, IEEE*, Dong Ho Lee, *Member, IEEE*, Kun-Seok Lee, *Student Member, IEEE*, Songcheol Hong, *Member, IEEE*, and Chang-Ho Lee, *Senior Member, IEEE*

***Abstract*—A cascode configuration in class-E CMOS power amplifiers (PAs) provides high reliability with respect to breakdown considerations. However, it causes a power loss due to the slow transition of a common-gate device from the triode region to the cut-off region. To minimize the power loss of cascode class-E CMOS PAs, we propose a charging acceleration technique, CAT. This method incorporates a capacitive element between the drain and the source of a common-gate device in a cascode configuration, accelerating the charging speed responsible for turning off a common-gate device instantly after a common-source device is turned off and thus minimizing power loss from the device. We compared the performance of the proposed cascode class-E PA to that of the conventional cascode class-E PA using a 0.18-μm CMOS process. With a 3.3-V power supply, the proposed fully-integrated CMOS PA achieves 30.7 dBm of maximum output power and 45.6% of power-added efficiency (PAE) with a dynamic range of 40 dB at 1.6 GHz. According to measurements, the proposed cascode class-E PA shows improvement in PAE over the conventional class-E PA of between 5% and 9% in a 1.5 to 2.0 GHz range.**

***Index Terms*—Cascode, class-E, CMOS, impedance matching, power amplifier (PA), power-combining, transformer.**

I. Introduction

RECENTLY, the demand for CMOS PAs has increased due to their good thermal characteristics, low cost, and capability of high-level integration with various functional blocks. Although several efforts have successfully demonstrated the capabilities of watt-level PAs [1]–[5], the design of a fully integrated CMOS PA with high efficiency and high output power has posed a formidable challenge. Such a highly-efficient PA is desirable because it is responsible for major power consumption in the front-end. Due to its high DC-to-RF conversion efficiency, a switching-mode PA is attractive. Theoretically, class-D, -E, and -F switching mode PAs can achieve 100% efficiency. In the switching operation, at no time in the cycle do the current and the voltage coexist with nonzero values, which implies that no energy is wasted as heat in the devices. A class-D PA employs a pair of devices driven in a push-pull mode and an output network to tune the fundamental frequency. However, the output capacitance can cause a discharge power loss, so a class-D PA is rarely used for GHz-range applications [6]. A class-F PA requires several lumped elements that perform harmonic terminations, resulting in a complicated and large size circuitry for the integration. A class-E PA, which has a strong switching operation, has been used for widespread wireless applications. Since class-E topology incorporates an output parasitic capacitance as part of the switching operation, the power loss due to the output

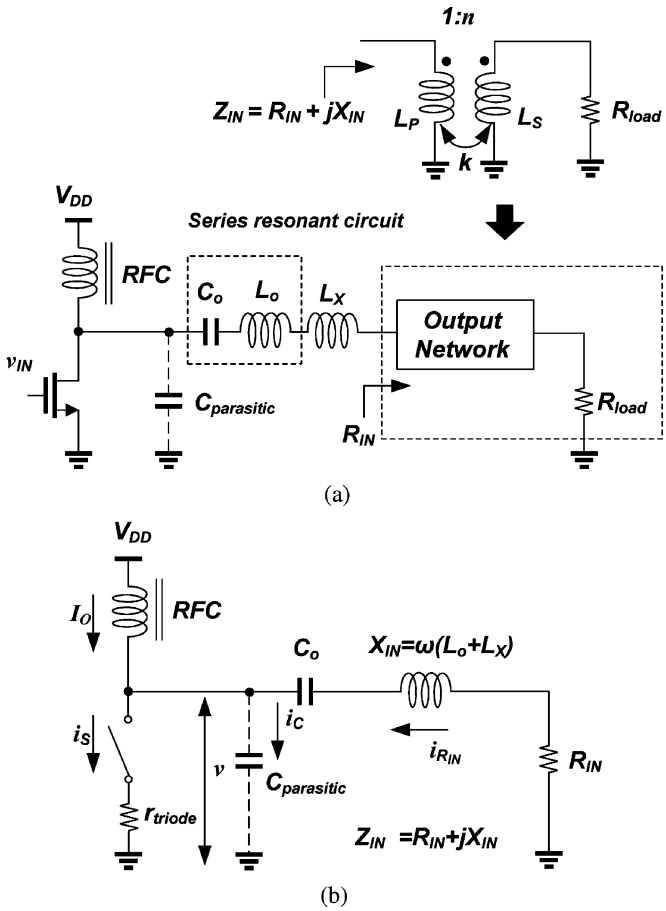

Fig. 1. (a) Schematic of a class-E PA with an output network. (b) Schematic of an equivalent class-E PA network.

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O. Lee was with Georgia Institute of Technology, Atlanta, GA 30308 USA. He is now with Qualcomm, San Diego, CA 92121 USA (e-mail: olee@qualcomm.com).

J. Han was with Georgia Institute of Technology, Atlanta, GA 30308 USA. He is now with Samsung Design Center, Atlanta, GA 30308 USA.

K. H. An and K.-S. Lee are with Georgia Institute of Technology, Atlanta, GA 30308 USA.

D. H. Lee was with Georgia Institute of Technology, Atlanta, GA 30308 USA. He is now with Skyworks Solutions, Inc., Cedar Rapids, IA 52411 USA.

S. Hong is with Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea.

C.-H. Lee is with Samsung Design Center, Atlanta, GA 30308 USA.

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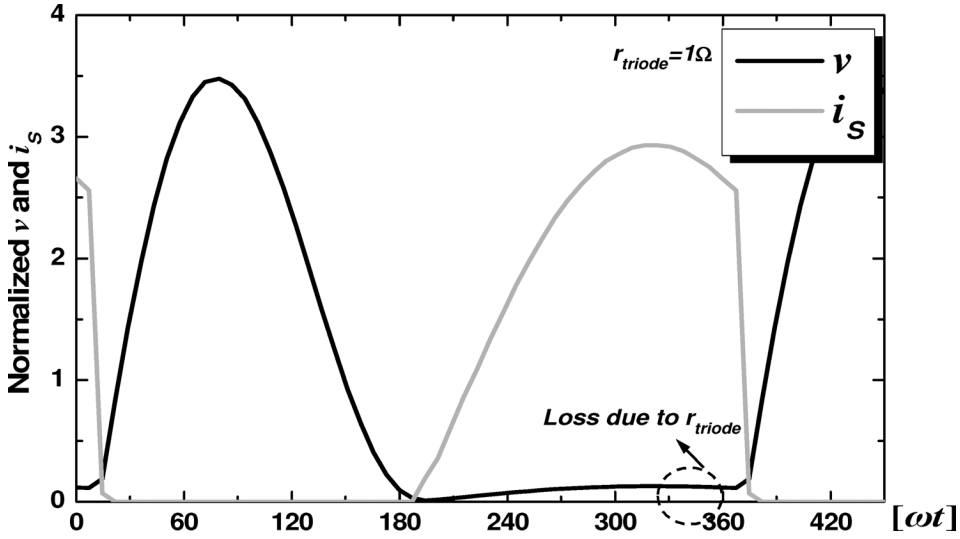

Fig. 2. Normalized voltage and current waveforms of a common-source class-E PA.

parasitic capacitance is eliminated. In addition, its implementation is simple, so the form factor of the class-E PA is more compact than that of the class-F PA.

The output power is proportional to the square of the supply voltage, so the high supply voltage is desirable for high output power. Therefore, PAs are operating under high voltage stress, especially in the class-E operation. Voltage stress between two terminals will seriously impair CMOS devices. For example, high voltage stress across the device can cause reliability issues such as gate-oxide breakdown, hot carrier degradation, punchthrough, and junction breakdown [7]. Reliability issues should be a main concern in CMOS PA design because breakdown voltages of CMOS devices are relatively small compared to those of GaAs devices. In common CMOS PA design practice, the maximum voltage drop across the device at any node should be below twice the nominal supply voltage [8]. However, as CMOS technology has progressed, its supply voltage has been scaled down, reducing breakdown voltage. One way to divide voltage stress across each device without decreasing supply voltage is to use device stacking in series. One example of device stacking is cascode topology [8]–[11]. To the best of the authors' knowledge, for the design of a cascode class-E CMOS PA, the body of the common-gate device is commonly grounded (BG-cascode). In this configuration, two devices should be turned on or turned off simultaneously to minimize the power loss due to the overlapping of the voltage and the current. However, in practical implementation, the common-gate device cannot be instantly switched from the triode region to the cut-off region. Although this effect is significant in loss, it has not been well studied except in two studies pertaining to the analysis of reliability and efficiency in [8] and [9], which proposed the application of the tuning inductor technique that minimizes the power loss in the common-gate device. On the other hand, the additional tuning inductor requires a large die area. In addition, this technique may have degraded performance across the bandwidth due to a resonant characteristic.

This work proposes a technique in which the common-gate device turns off instantly after the common-source device in a class-E CMOS PA structure is turned off. This technique, which accelerates a capacitor charging through an additional current path, is called CAT. We suggest a body-source-tied cascode (BS-cascode) topology for the cascode configuration in which a body of the common-gate device is tied to its source. The BS-cascode class-E PA that embeds CAT due to a parasitic capacitance improves efficiency. To demonstrate its effectiveness, we use simulations and measurements on a prototype cascode class-E CMOS PA.

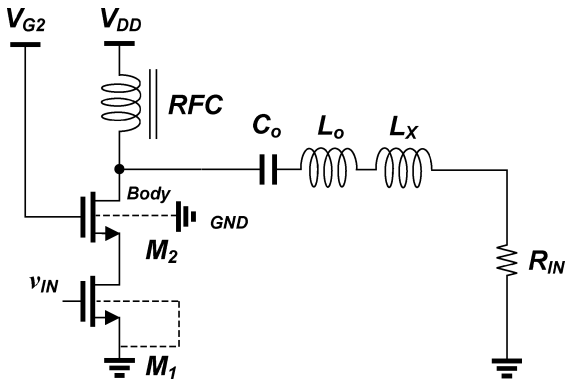

Fig. 3. Conventional cascode class-E PA (BG-cascode class-E PA).

The paper is organized as follows. Section II addresses device power losses of the cascode class-E CMOS PA using a proposed simplified model. Section III introduces a scheme for minimizing the power loss of the common-gate device, which will improve the overall efficiency of the PA. Section IV presents measurement results, and Section V draws conclusions.

II. Power Losses of the Cascode Class-E PA

Power losses of PAs are mainly caused by active devices and lossy passive elements. Several studies have addressed power losses in class-E PAs, including power losses due to the loss resistances of devices and passive elements [2], [8], [9], [12]–[15]. However, with the exception of [8], [9], most studies have not

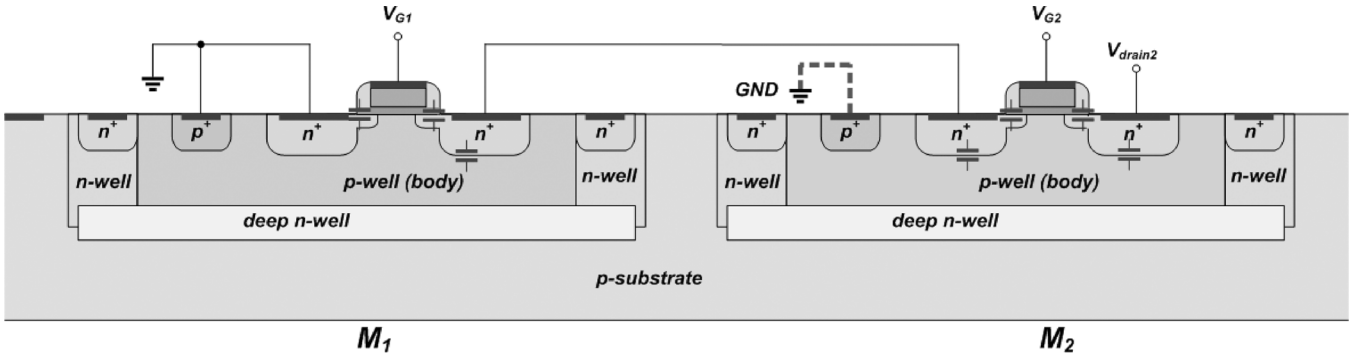

Fig. 4. Capacitance composition of a BG-cascode structure in a deep N-well process.

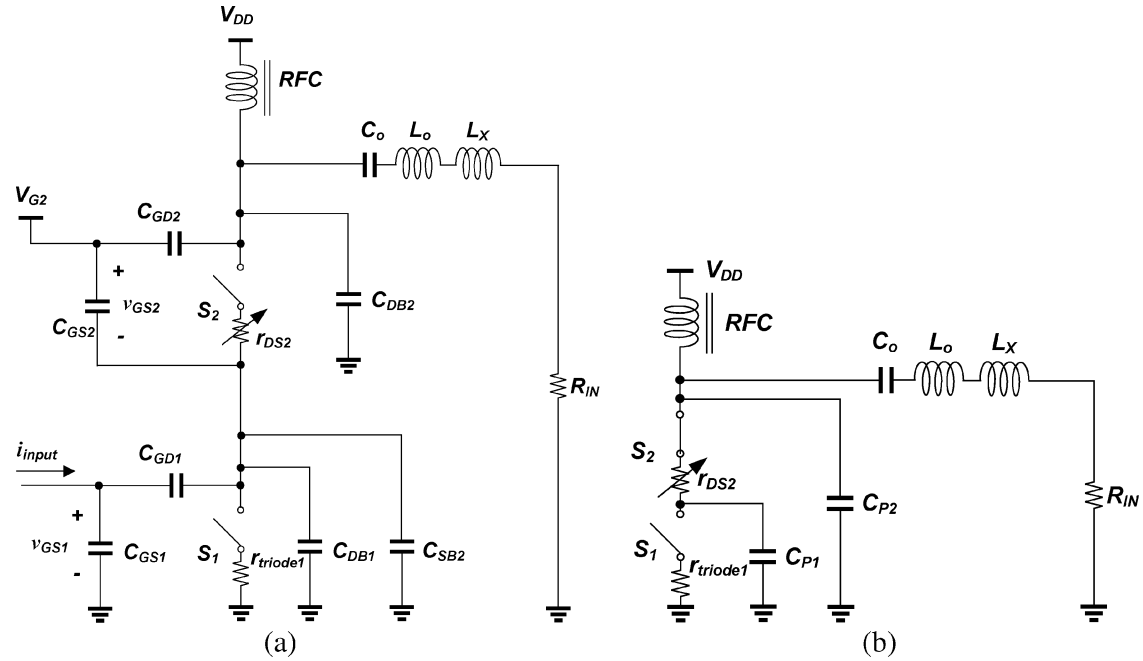

Fig. 5. (a) Complete equivalent BG-cascode class-E PA circuit model. (b) Simplified BG-cascode class-E PA model.

considered the power loss of a device due to device stacking, such as a cascode configuration. Using a high-Q passive is one way to minimize the losses of passive elements. If passive efficiency were maximized, the power loss due to such devices could serve as the dominant source of power dissipation. In this paper, we focus on the device power loss and suggest a method of minimizing the device power loss in a cascode configuration.

A. Power Losses of the Common Source Class-E PA

Fig. 1(a) shows the circuit schematic of a typical common-source class-E PA with an output network. C_O and L_O are designed to form a series resonator, and the device output capacitance, $C_{parasitic}$ and L_X are designed based on two class-E switching conditions [16]–[18].

1) Voltage across the switch returns to zero at the end of the off-state (i.e., $v(\omega t) = 0$).
2) The first derivative of the voltage across the switch is zero at the end of the off stage (i.e., $dv(\omega t)/d(\omega t) = 0$).

The output network in Fig. 1(a) provides the necessary impedance transformation from optimum impedance, $R_{\rm IN}$, to R_{load} for the class-E operation. The output network can be implemented by a transformer [1]–[4] for on-chip implementation. The transformer can be modeled with the equivalent net inductances, L_P and L_S, for the primary and secondary windings. n is the turn ratio, and k is the coupling factor. When the transformer is a part of a class-E network, L_O and L_X can be eliminated by reflective inductance from the transformer, $X_{\rm IN}/\omega$, resulting in a more simplified circuit, shown Fig. 1(b) [2]. For optimum class-E design conditions, the following design parameters can be determined as [16]–[18]

$$R_{\rm IN} = 0.5768 \frac{{V_{\rm DD}}^2}{P_{\rm IN}} \tag{1}$$

$$L_X = 1.1525 \frac{R_{\rm IN}}{\omega} \tag{2}$$

$$C_{parasitic} = \frac{0.1836}{\omega R_{\rm IN}}. \tag{3}$$

Because the device is driven by a large signal in a switching operation, it operates in either the triode region or the cut-off region during most of the cycle. Thus, the core device can be modeled as a switch with an equivalent low triode-resistance, r_{triode}. When the device operates in the cut-off region, it acts as

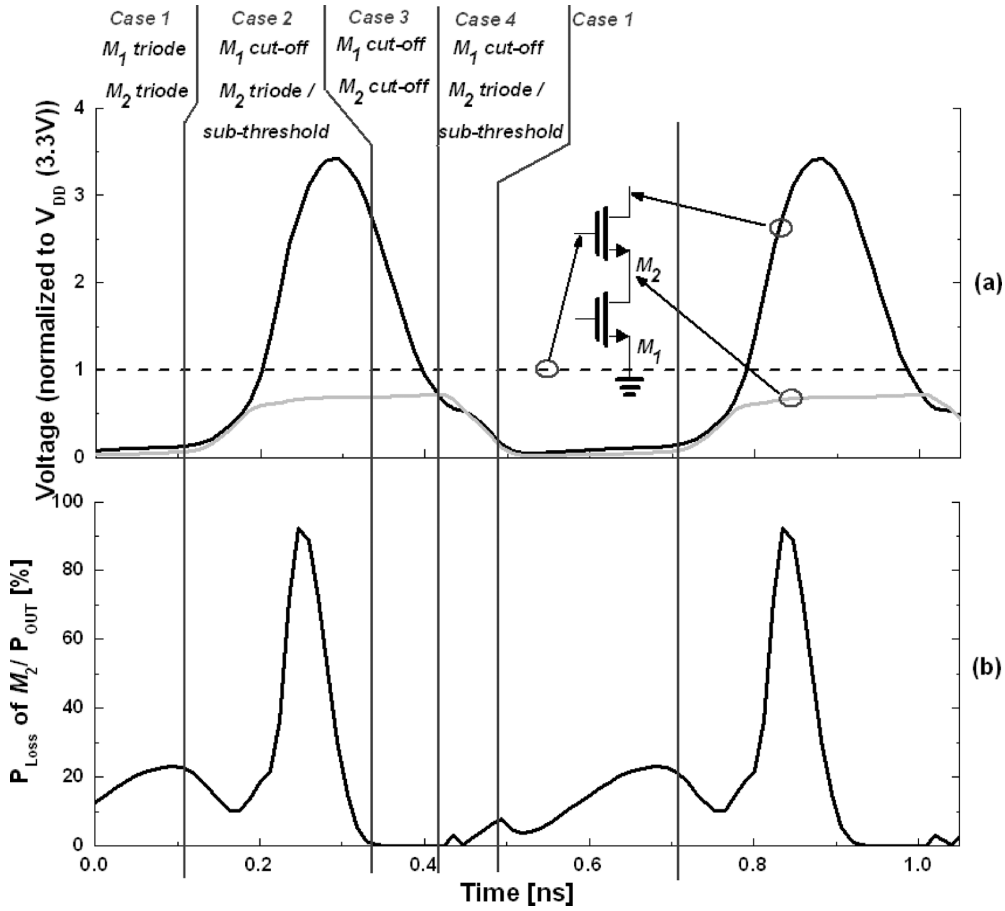

Fig. 6. (a) Voltage waveforms at each terminal the drain, the source and the gate of M_2. (b) Normalized power loss in M_2. (frequency $= 1.7$ GHz).

an open switch. When the device operates in the triode region, it acts as a closed switch with a series r_{triode}. If $V_{DS} \ll 2(V_{GS} - V_{TH})$, r_{triode} in the triode region is given by [19]

$$r_{triode}(\omega t) = \frac{1}{\mu_n C_{OX} \frac{W}{L}(v_{GS}(\omega t) - V_{TH})} \tag{4}$$

where L is the gate length, W is the gate width, C_{OX} is the gate oxide capacitance per unit area, μ_n is the electron mobility, and V_{TH} is the threshold voltage. This conductive resistance in the device generates a power loss. Because an input matching network is generally designed to form a resonator that tunes out an input gate capacitance of the power device, the waveform of an input signal, v_{GS}, is sinusoidal, not a square wave. Therefore, r_{triode} will vary as a function of v_{GS} in (4). However, it is difficult to calculate the power loss by varying r_{triode}, so a constant value has typically been assumed for an analytical solution [2], [12]–[15]. Fig. 2 shows the simulated voltage and current waveforms of a common-source class-E PA with constant r_{triode}. The voltage and the current are simultaneously positive in the on-state due to r_{triode}, which causes a power loss in the device. This power loss can be minimized by increasing device size $_W$ in (4). Generally, to minimize the power loss due to r_{triode}, the device size needs to be increased until the device output parasitic capacitance, $C_{parasitic}$, seen from the drain, can replace the required parallel capacitance for the class-E switching condition. However, device size should not be excessively increased in order to compensate for the driving loss since the accompanying large input capacitance would only exacerbate the problem [20], [21].

B. Power Losses of the Cascode Class-E PA

For watt-level output power, a large impedance ratio is generally required to reduce $R_{\rm IN}$ in (1) at the given $\rm V_{DD}$. However, a large impedance transformation results in a large power loss. Generally, the higher the impedance transformation ratio is, the higher the loss of the impedance transformation network is [22]. One way of obtaining watt-level output power without increasing the impedance transformation ratio is to increase $\rm V_{DD}$, which reduces the burden caused by necessary impedance transformation. In addition, the battery voltage of a mobile terminal is fixed and does not scale down, and PAs in mobile terminals have been built mostly using 3.6-V lithium ion batteries. However, this high supply voltage increases stress, causing reliability problems in the device. Using a cascode topology is a way to sustain a high supply voltage using a sub-micron standard CMOS device.

However, in addition to the power loss due to r_{triode}, a property of the cascode class-E CMOS PA generates another loss in the device. Because two devices cannot be turned on or turned off simultaneously, the voltage and the current coexist, causing a power loss in the device. Fig. 3 shows a cascode

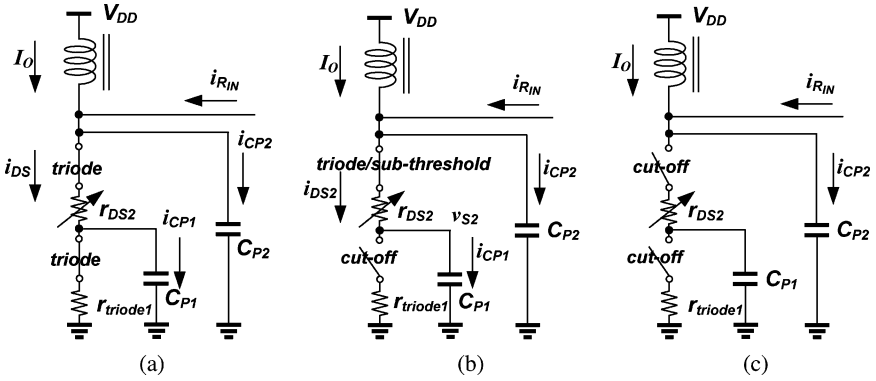

Fig. 7. (a) Equivalent circuit model for case 1. (b) Equivalent circuit model for case 2 and case 4. (c) Equivalent circuit model for case 3.

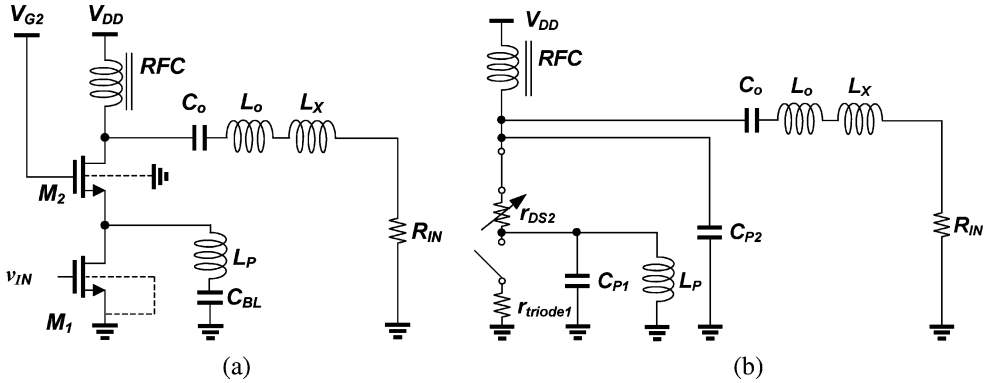

Fig. 8. (a) Schematic of a BG-cascode class-E PA with a tuning inductor. (b) Equivalent circuit model of a BG-cascode class-E PA with a tuning inductor.

class-E PA using a conventional cascode structure. The body of a common-gate device is commonly connected to the ground (BG-cascode) in the design of a cascode class-E PA. Traditionally, before foundries supported the deep N-well process, the body of a common-gate device had been connected to the ground. Fig. 4 shows the parasitic capacitance composition of a BG-cascode structure in a typical deep N-well technology. In a class-E PA design, device parasitic capacitances should be incorporated into the switching operation if these capacitances are not tuned out. Fig. 5(a) shows the equivalent circuit model for the BG-cascode structure with the relevant parasitic capacitance composition. For the core model of the devices, the common-source device, M_1, can be replaced by a switch with a constant low r_{triode} like that in the common-source class-E PA. However, the common-gate device, M_2, should be modeled as a switch with variable drain-source resistance r_{DS}, whose value varies with each node voltage in the time cycle, illustrated in Fig. 5(a). Unlike M_1, M_2 cannot be switched instantly from the triode region to the cut-off region, so the transient time of M_2 cannot be neglected. In this case, the device can operate in the subthreshold region during a large fraction of the cycle, and its equivalent resistance r_{DS} will vary from low r_{triode} to very high impedance before turning off.

Junction capacitances such as the drain-body capacitance of M_1, C_{DB1}, the drain-body capacitance of M_2, C_{DB2}, and the source-body capacitance of M_2, C_{SB2}, dominate in the cut-off region of the device and have voltage dependence. The gate-source capacitance of M_1, C_{GS1}, the gate-drain capacitance of M_1, C_{GD1}, the gate-source capacitance of M_2, C_{GS2}, and the gate-drain capacitance of M_2, C_{GD2}, depend on the operation region of the device. To simplify the analysis, C_{GD1} can be separated into the input referred capacitance of C_{GD1} and the output referred capacitance of C_{GD1} [23]. In addition, the input referred capacitance of C_{GD1} and C_{GS1} can be tuned out using an additional tuning inductor that minimizes the driving loss. When several capacitors are combined, a simple BG-cascode class-E PA model can finally be obtained, shown in Fig. 5(b). The triode-resistance of M_1, $r_{tridoe1}$ and the variable drain-source resistance of M_2, r_{DS2} are connected in series. The output capacitance of M_2, C_{P2}, is the sum of C_{DB2} and C_{GD2}. If an additional lumped capacitor is not added, C_{P2} should satisfy the condition in (3). The output capacitance of M_1, C_{P1}, is the sum of C_{DB1}, C_{GS2}, C_{SB2}, and the output referred capacitance of C_{GD1}. This total capacitance is directly related to the transition loss of the cascode class-E operation.

In an ideal class-E operation, only two states exist in the cycle, on- and off-states. In the on-state, both M_1 and M_2 operate in the triode region, and the current flows through two series conductive channel resistances, $r_{triode1}$ and $r_{DS2} = r_{triode2}$. In the off-state, both M_1 and M_2 operate in the cut-off region, and the currents flow through C_{P2}. Thus, these two currents generate a sinusoidal current at the output. However, due to the cascode property, M_1 and M_2 cannot be turned off simultaneously, which generates a significant power loss. Fig. 6(a) shows the simulated voltage waveforms of a conventional BG-cascode class-E PA using TSMC 0.18-μm process. The cascode struc-

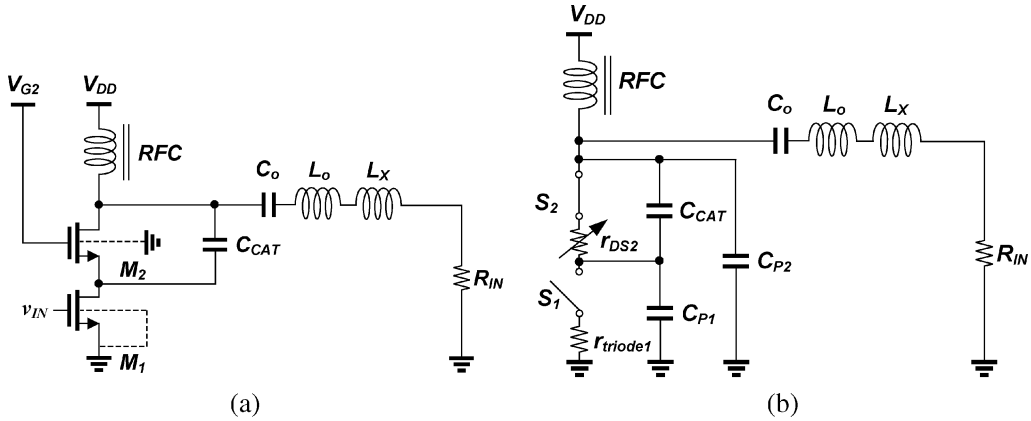

Fig. 9. (a) Schematic of a BG-cascode class-E PA with a charging acceleration capacitor. (b) Equivalent circuit model of a BG-cascode class-E PA with a charging acceleration capacitor.

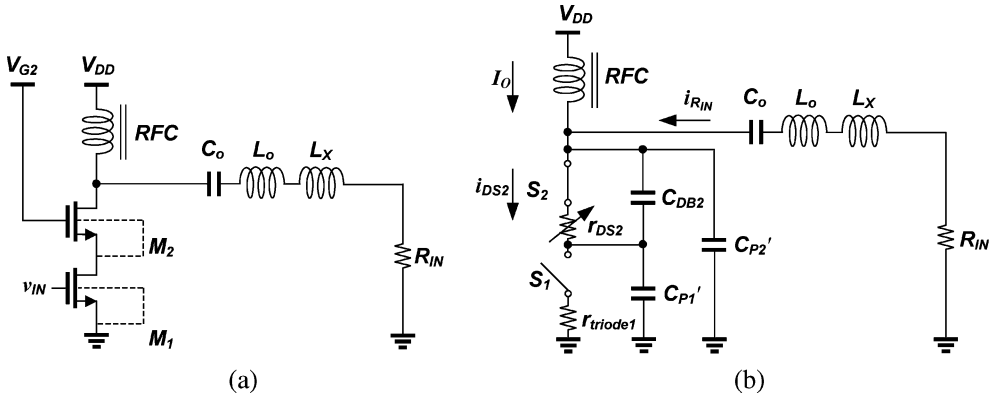

Fig. 10. (a) Schematic of a BS-cascode class-E PA. (b) Equivalent circuit model of a BS-cascode class-E PA.

ture has a stacked configuration of 0.18-μm for M_1 and 0.35-μm for M_2. ADS harmonic balance simulations were performed using an RF BSIM3v3 device model provided by the foundry, which includes parasitic lumped elements for high frequency characterizations. Fig. 6(b) shows an instantaneous power loss of M_2, normalized to the output power.

The instantaneous power loss can be defined as

$$P_{Loss} = i_{DS}(\omega t)v_{DS}(\omega t) = {i_{DS}}^2(\omega t)r_{DS}(\omega t). \quad (5)$$

$v_{DS}(\omega t)$ is the voltage difference between the drain and the source, and $i_{DS}(\omega t)$ is the current through the conductive channel. In addition, the average dissipated power can be defined as

$$\begin{aligned} P_{average\ loss} &= \frac{1}{2\pi}\int i_{DS}(\omega t)v_{DS}(\omega t)d(\omega t) \\ &= \frac{1}{2\pi}\int {i_{DS}}^2(\omega t)r_{DS}(\omega t)d(\omega t). \end{aligned} \quad (6)$$

The power loss in the transition state is much larger than that in the triode region of both M_1 and M_2, shown in Fig. 6(b) and introduced in [8]. The power loss can be as much as 20% of the output power, which is five times as much as that due to r_{triode} in the triode region of both M_1 and M_2 [8].

The loss mechanism of a cascode class-E CMOS PA can be explained using the suggested simplified model. The main cause of the power loss of a device is currents, $i_{DS}(\omega t)$, flowing through each conductive channel of the stacked cascode devices. We distinguish four cases according to the operation ranges of M_1 and M_2 and consider the power loss in each case:

1) The operations of both M_1 and M_2 are in the triode region, shown in Fig. 7(a). In this case, the current flows through two switches, and r_{DS2} is equal to triode-resistance $r_{triode2}$. The power losses due to each r_{triode} of the device can be expressed as

$$\begin{aligned} P_{Loss} &\approx {i_{DS1}}^2(\omega t)r_{triode1} + {i_{DS2}}^2(\omega t)r_{triode2} \\ &= {i_{DS1}}^2(\omega t)[r_{triode1} + r_{triode2}] \end{aligned} \quad (7)$$

where $i_{DS}(\omega t) \cong i_{DS1}(\omega t) \cong i_{DS2}(\omega t)$ and $i_{CP1}(\omega t) \cong i_{CP2}(\omega t) \cong 0$.
This power loss is relevant to the dominant device power loss in a common-source class-E PA.

2) M_1 operates in the cut-off region while M_2 is still on. When the angle of a large signal input is negative, M_1 is completely turned off, but M_2 operates in the triode region or subthreshold region. Fig. 7(b) shows the equivalent circuit model in this transition state. During this time period, the DC current I_O and output load current i_{RIN} flow into two paths, the r_{DS2}-to-C_{P1} path and the C_{P2} path, based on the magnitude ratio of $R_{DS2} + 1/\omega C_{P1}$ to $1/\omega C_{P2}$. Therefore, the drain and source voltages of M_2 rise due to

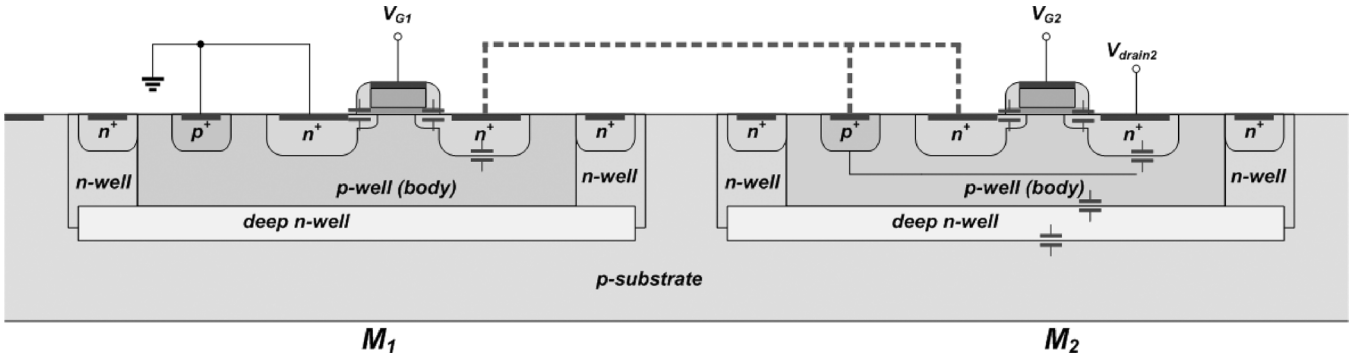

Fig. 11. Capacitance composition of a BS-cascode structure in a deep N-well process.

C_{P2} and C_{P1} charging, respectively. The source voltage of M_2, V_{S2} , can be expressed as

$$V_{S2}(\omega t) = \frac{1}{\omega C_{P1}} \int i_{CP1}(\omega t) d(\omega t). \tag{8}$$

Right after M_1 is turned off, r_{DS2} of M_2 is small during this time period, and the voltage difference between the drain and the source is small, shown in Fig. 6(a). With the increasing source voltage of M_2, r_{DS2} will be much larger than the magnitude of $1/\omega C_{P2}$, and the small fraction of $I_O + i_{RIN}$ will flow into the r_{DS2}-to-C_{P1} path. Then C_{P1} slowly charges. In contrast, the drain voltage of M_2 rises sharply because a relatively large fraction of $I_O + i_{RIN}$ flows into the C_{P2} capacitor. Thus, the slow charging of the C_{P1} increases the power loss of the device. Even though this conductive channel current, i_{DS2}, is small, the power loss can be large due to the large voltage drop between the drain and the source of M_2. The power loss by r_{DS2} continues until M_2 is turned off. Its loss can be described as

$$P_{Loss} \approx i_{DS2}(\omega t) v_{DS2}(\omega t) = {i_{DS2}}^2(\omega t) r_{DS2}(\omega t) \tag{9}$$

where $i_{DS2}(\omega t) \cong i_{CP1}(\omega t)$ and $i_{DS1}(\omega t) \cong 0$. Turning off M_2 requires that the source voltage of M_2 be larger than $V_{\rm G}$ minus V_{TH2}. $V_{\rm G}$ is the gate voltage of M_2, and V_{TH2} is the threshold voltage of M_2.

3) Both M_1 and M_2 operate in the cut-off region, shown in Fig. 7(c). In this case, no power dissipation through the conductive channels exists.
4) Before two devices go back to case 1, M_1 operates in the cut-off region, and M_2 is in the triode region, or sub-threshold region. The mechanism of the power loss is similar to that of case 2. However, its loss is much smaller than that of case 2 because the voltage difference between the drain and the source of M_2 is relatively smaller.

III. Charging Acceleration Technique

To minimize i_{DS2} generating the power loss of M_2 in the transition state, the voltage difference between the gate and the source, V_{GS2}, should be less than V_{TH2} after M_1 is turned off. Decreasing the gate voltage of M_2, $V_{\rm G2}$, also helps to turn off M_2 when M_1 is turned off. However, a decrease in $V_{\rm G2}$ raises the voltage stress between the gate and the drain of M_2. Because the drain voltage of M_2 reaches about 3.56 times $V_{\rm DD}$ in the off-state in an ideal operation, it is desirable that the gate of M_2 connect to the highest DC voltage to minimize the voltage stress between the gate and the drain of M_2. Because the gate voltage of M_2 is at a fixed bias voltage, the source voltage of M_2 needs to rise immediately to turn off M_2 after M_1 is turned off. One way to increase the source voltage of M_2 is to reduce the parasitic capacitance, C_{P1}. In the past, the inductor tuning technique was proposed to minimize the effect of C_{P1} [8], [9]. In this technique, a tuning inductor is connected in parallel to the source of M_2 to resonate out C_{P1}, as shown in Fig. 8. Blocking capacitor C_{BL} is located between the tuning inductor and the ground. Because the amount of C_{P1} is tuned out, the source voltage of M_2 rises rapidly after M_1 is turned off. However, the additional tuning inductor requires a large die area. In addition, the loss resistance of the on-chip inductor can be an additional source of power dissipation although its effect is negligible compared to the loss in the common-gate device. Furthermore, this technique may have degraded performance across the bandwidth due to a resonant characteristic.

In this paper, we propose an effective method of expediting the source voltage increase of M_2. As shown in Fig. 9(a), adding an additional current path through a capacitor between the drain and the source of M_2 increases the source voltage of M_2 by accelerating the charging of C_{P1}. This capacitor is called a charging acceleration capacitor, C_{CAT}. Immediately after M_1 is turned off with a large signal input, M_2 is still in the triode region, and r_{DS2} is small. Upon increasing the source voltage of M_2, r_{DS2} becomes high. In this region, an additional current path through C_{CAT} in Fig. 9(b) helps to increase the charging speed of C_{P1}. Because this additional capacitance is a part of the necessary output capacitance satisfying class-E switching conditions, the total output capacitance ($C_{P2}+(C_{P1}//C_{CAT})$) at the drain of M_2 should conform to (3), which is the case in which the additional lumped capacitor is not added to the drain of M_2 in Fig. 9(b).

A simple but more efficient method can also be suggested. By optimizing the device design, the lumped capacitor C_{CAT} can be eliminated. If the body of the common-gate device is tied to its source (BS-cascode) for the design of a class-E CMOS PA, as shown in Fig. 10, this structure has its own capacitor connection property between the drain and the source without an additional lumped element. Fig. 11 shows the capacitance composition of the BS-cascode structure in a deep N-well technology. When the

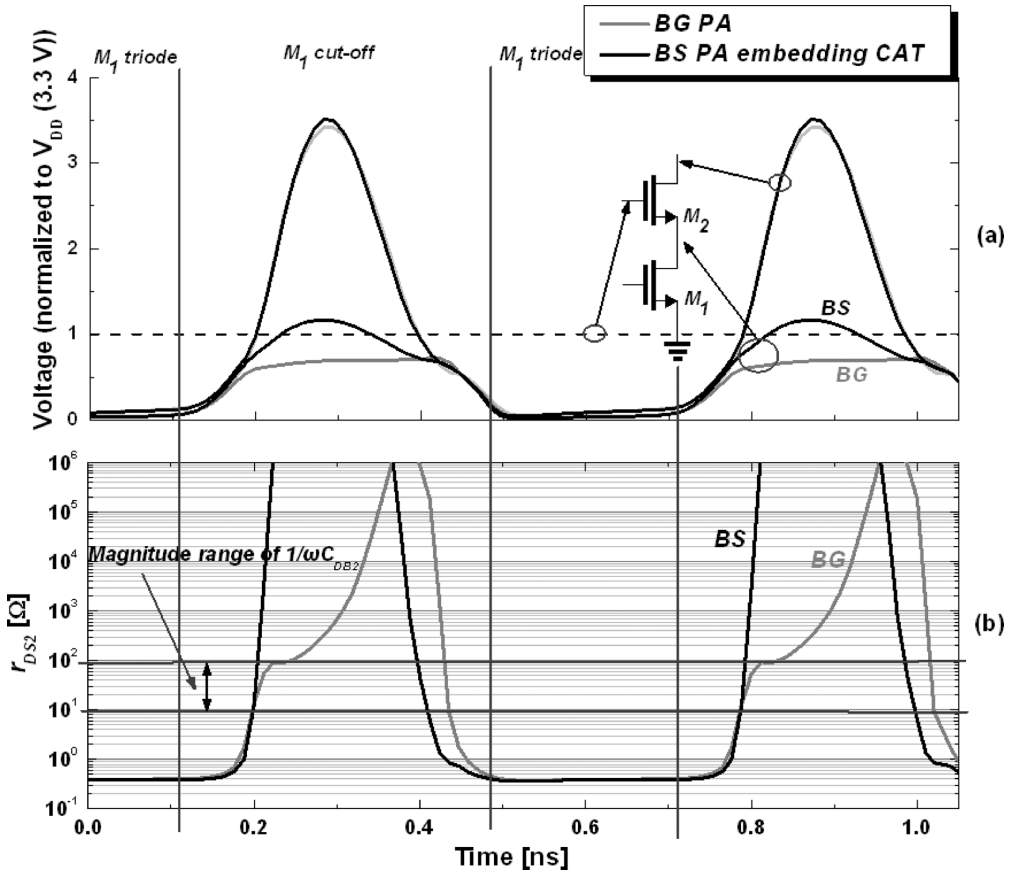

Fig. 12. (a) Voltage waveforms at the drain, the source, and the gate of M_2. (b) Equivalent source-drain resistance of M_2. (frequency = 1.7 GHz.)

body and source are tied together, they generate a series connection between the drain and the source of M_2. Fig. 10(b) shows its equivalent circuit model based on the parasitic capacitance composition. Like that of the BG-cascode, the triode-resistance of M_1, $r_{triode1}$, and the drain-source resistance of M_2, r_{DS2}, are connected in series. C'_{P2} is the gate-drain capacitance of M_2, C_{GD2}. The output capacitance of M_1, C'_{P1}, is the sum of the drain-body capacitance of M_1, C_{DB1}, the gate-source capacitance of M_2, C_{GS2}, the output referred capacitance of the gate-drain capacitance of M_1, and the capacitance between the body of M_2 and the well connection. The source-body capacitance of M_2, C_{SB2}, does not exist since the source of M_2 is tied down to the body of M_2. The drain-body capacitance of M_2, C_{DB2}, and C'_{P1} are connected in series.

Fig. 12(a) shows the simulated voltage waveforms at the drain and the source of M_2 for both the body-grounded cascode (BG-cascode) and the body-source-tied cascode (BS-cascode) class-E PA. Each of the cascode structures has a stacked configuration of 0.18-μm for M_1 and 0.35-μm for M_2. Fig. 12(b) shows the simulated r_{DS2} in the cycle. When M_1 is turned off, M_2 still operates in the triode region. In this region, r_{DS2} is expressed as the triode-resistance of device $r_{triode2}$. The magnitude of $r_{triode2}$ will be much smaller than that of $1/\omega C_{DB2}$ at operation frequency bands of typical wireless applications because C_{DB2} is typically in the range of a few pico-farad (pF) for a few millimeter device width, illustrated in Fig. 12(b). Therefore, DC currents I_O and output load current i_{RIN} flow into two paths, the $r_{triode1}$-to-C'_{P1} path and the C'_{p2} path, just as they do in the BG-cascode class-E PA. The output capacitance of M_1, C'_{P1} starts charging, and the source voltage of M_2 rises due to the current in the r_{DS2}-to-C'_{P1} path. When the source voltage of M_2 increases, the magnitude of r_{DS2} will be comparable to that of $1/\omega C_{DB2}$. Then, the currents start to flow through C_{DB2}, accelerating the charging of C'_{P1} as the magnitude of r_{DS2} increases. This raises the source voltage of M_2, and then further increases the magnitude of r_{DS2}, which enhances the current through C_{DB2}. This process of charging acceleration causes a further increase in the source voltage of M_2, resulting in a rapid transition from the triode region to the cut-off region of M_2 after M_1 is turned off, shown in Fig. 12. This rapid transition minimizes the power loss due to the overlapping of the voltage and the current in M_2. The source voltage of M_2 in the BS-cascode class-E PA, unlike that in the BG-cascode class-E PA, rises more than $V_{\rm G}$ minus V_{TH2} because C_{DB2} and C'_{P1} are connected in series, and AC current flows though the series capacitors. Therefore, in the cut-off region of M_1, V_{GS} of M_2 in the BS-cascode class-E PA is much smaller than that in the BG-cascode class-E PA, resulting in a much smaller conductive channel current of the BS-cascode class-E PA than that of BG-cascode class-E PA. Thus, the power loss is minimized without adding an additional lumped element. Because the magnitude of r_{DS2} will vary from less than one ohm to the mega ohm range, the performance variation of CAT resulting from a variation in the magnitude of

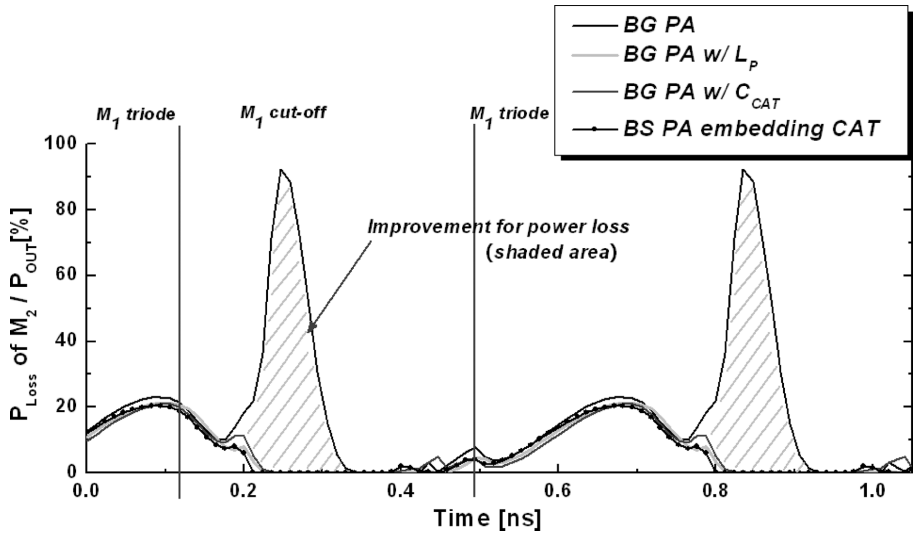

Fig. 13. Power loss of M_2 for cascode class-E PAs (frequency $=$ 1.7 GHz).

$1/\omega C_{DB2}$ will be negligible as long as C_{DB2} lies within the range of a few pF for a few-millimeter device width.

In the BS-cascode class-E PA, the total output capacitance ($C_{GD2}+(C'_{P1}//C_{DB2})$) at the drain of M_2 should satisfy (3) if the additional lumped capacitor is not attached. C_{DB2}, and C'_{P1} are connected in series, so the total output capacitance in the BS-cascode class-E PA will be smaller than that in the BG-cascode class-E PA ($C_{P2} = C_{GD2} + C_{DB2}$). However, C'_{P1} is roughly 4 times as large as C_{DB2}, so the total output capacitance of the BS-cascode class-E PA is close to that of the BG-cascode class-E PA for the same size device.

Fig. 13 shows the instantaneous power losses, normalized to each output power, for the BG-cascode class-E PA, the BG-cascode class-E PA with a tuning inductor, the BG-cascode class-E PA with C_{CAT}, and the BS-cascode class-E PA embedding CAT. The BG-cascode class-E PA with a tuning inductor, the BG-cascode class-E PA with C_{CAT}, and the BS-cascode class-E PA embedding CAT significantly reduce the power loss in the transition state. However, the BS-cascode class-E PA embedding CAT improves efficiency without adding a lumped element. The improvement in efficiency resulting from the reduced $r_{triode2}$ in the BS-cascode structure is relatively negligible compared to that resulting from the reduced transition loss, as shown in Fig. 13. Simulated load-lines of M_2 for the BG-cascode class-E PA and the BS-cascode class-E PA embedding CAT are shown in Fig. 14. The load-line of the BS-cascode class-E PA embedding CAT is similar to a typical load-line of a class-E PA while the overlapping the voltage and the current in the BG-cascode class-E PA causes a significant power loss in the transition state.

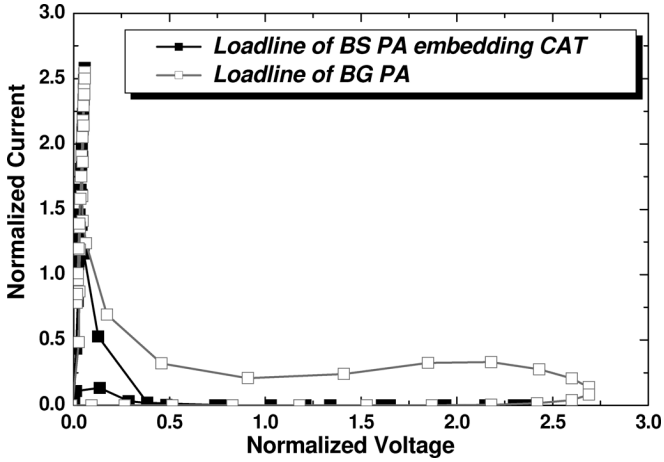

Fig. 14. Simulated load-lines of M_2 for the BG PA and the BS PA embedding CAT.

IV. Design and Implementation

To demonstrate the advantage of the body-source-tied cascode (BS-cascode) class-E PA embedding CAT over the body-grounded cascode (BG-cascode) class-E PA topology, we designed two types of 1.7-GHz CMOS Class-E PAs using 0.18-μm CMOS technology. Because the two PAs share the same layout except for the body connection of the common-gate device, the geometry-dependent parameter variation between them can be ignored. The BG-cascode class-E PA also adopted a deep n-well process for a fair comparison even though it does not necessarily require the deep n-well. Since we use only one deep n-well covering the entire power cell area, the overall area of the BG-cascode, including the deep n-well, is similar to that of the power cell without the deep n-well. The deep n-wells for both PAs are floated in this design to prevent junction diodes from turning on in the large signal at the source of the common-gate device [24]–[26].

The designed PAs consist of two driver stages and a power stage, illustrated in Fig. 15. An input on-chip balun is employed for the differential operation of the PAs. The input capacitance of the common-source device is tuned out by a parallel inductor, L_d. The quality factor, Q of L_d, is selected to be 7, considering bandwidth performance of the PA. For the cascode configuration of the PA, the devices in common-source stages m_1 and m_3 and

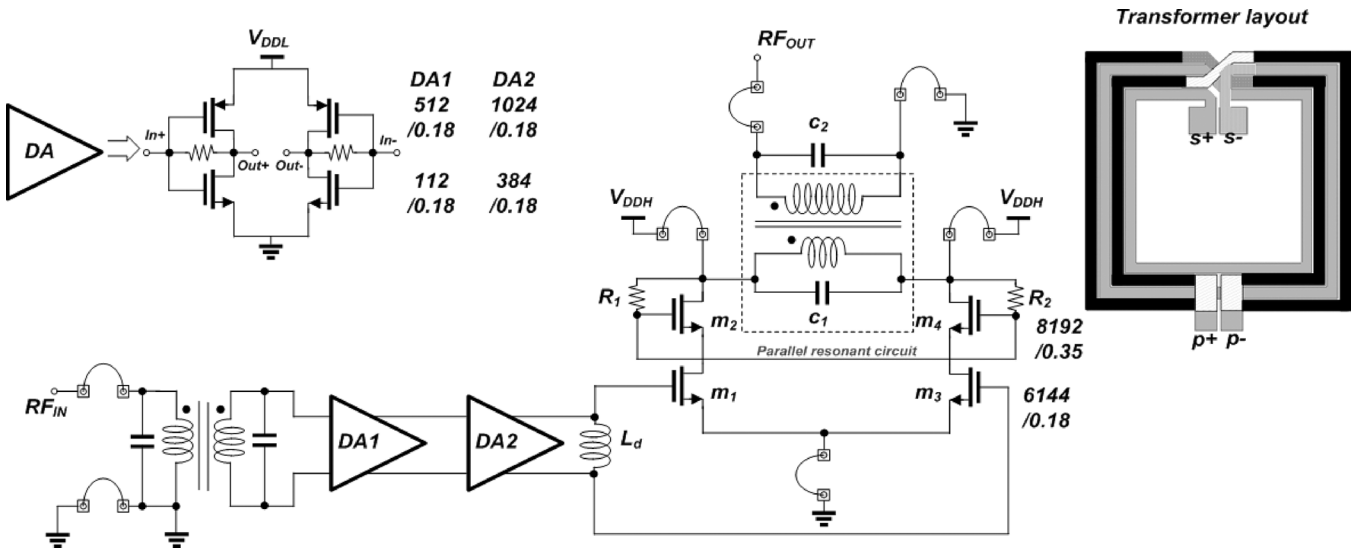

Fig. 15. Schematic of the CMOS cascode class-E PA with a 1:2 transformer.

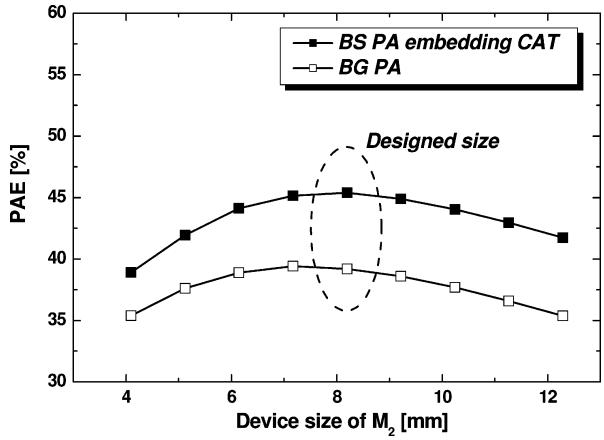

Fig. 16. PAE performance with an increasing device size of M_2.

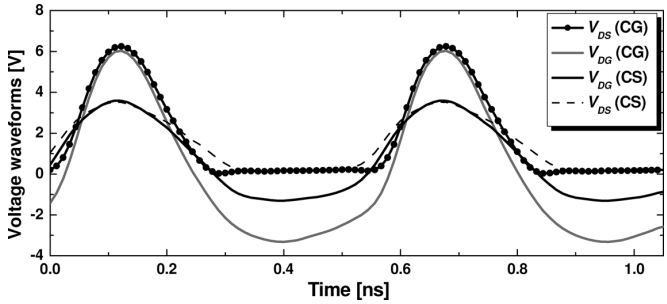

Fig. 17. Simulated voltage waveforms of power devices.

common-gate stages m_2 and m_4 have gate lengths of 0.18-μm and 0.35-μm, respectively.

For the size optimization of the common-source device, the gate driving loss due to the input capacitance and the power loss due to triode-resistance, $r_{triode1}$, are considered. The selected size of the common-source device is 6144 μm for both the BG- and BS-cascode class-E PAs. For the common-gate device selection, the device size needs to be increased to reduce $r_{triode2}$. However, because the total output capacitance of the cascode structure should satisfy the condition in (3), and is mainly determined by the size of the common-gate device, the device size should not be excessively increased. Fig. 16 shows the performance variation when the device size of the common-gate device increases. The optimum size of the common-gate device in the BG-cascode class-E PA (7168 μm) is smaller than that in the BS-cascode class-E PA (8192 μm) because the total output capacitance of the BG-cascode class-E PA will be larger than that of the BS-cascode class-E PA if the device size is the same in both cases. However, the variation in PAE performance of the BG-cascode class-E PAs with sizes of 7168 μm and 8192 μm is just about 0.5% because the difference between the total output capacitance of the two cases is small. Thus, the selected size of the common-gate device is 8192 μm for both the BG- and BS-cascode class-E PAs for minimizing variation between two PAs due to geometry-dependent parameters. In this case, the extracted effective total output capacitances for the BG- and BS-cascode class-E PAs from simulations are about 4.8 pF and 4.2 pF, respectively. The total output capacitance of the BG-cascode class-E PA is only 12.5% larger than that of the BS-cascode class-E PA. Despite the difference of the total output capacitances of the two PAs, both are well optimized for the operation of the class-E PA, shown in Fig. 16. The power loss reduction in the common-gate device mainly leads to an improvement in the efficiency in the BS-cascode class-E PA.

To minimize the voltage stress between the gate and the drain of the common-gate device, the gate of the common-gate device needs to connect to the highest DC voltage (3.3 V). In this design, to reduce the number of pads, each gate of the common-gate device is tied to its corresponding drain through a 5-kΩ resistor. The gate nodes of differential devices are tied together, so the gates of common-gate devices have no fundamental signal. Thus, the gate voltage of the common-gate device is always around 3.3 V. For reliable circuit operation over time, the maximum voltage stress across the single device is maintained at about twice as high as that of the nominal supply voltage without sacrificing performances. The maximum voltage stress across

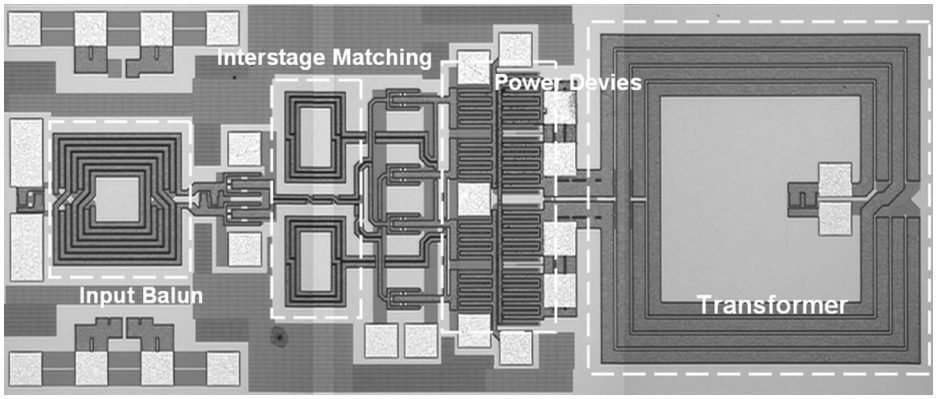

Fig. 18. Microphotograph of the PA (Chip size: 2.15 mm × 0.8 mm).

the common-gate (CG) and common-source (CS) devices are 6.3 V and 3.6 V, respectively, as shown in Fig. 17. Thus, the circuit operation might be marginally safe in the reliable range.

For the power stage design, we adopt a differential topology to desensitize the effect of bond-wire inductance and combine powers from two power devices driven in a differential mode. Then we employ a parallel-tuned circuit class-E PA [27], [28] to reduce number of elements instead of using a series-tuned circuit class-E PA. This topology requires one parallel resonant circuit while a series-tuned circuit requires two series resonant circuits. Therefore, this structure can reduce the size and number of elements, resulting in a more simplified circuit.

To transform the low impedance of the switching network to a 50-ohm load and combine the power from the power devices in a differential mode, we designed a transformer with a two-segment primary and two-turn secondary, adopting an Al process in this work. Compared to the Cu process, the Al process requires more careful attention to the design of a highly efficient output network because of the relatively lower Q of a passive component with Al-metal. A multi-turn secondary transforms impedance while a multi-segment primary increases passive efficiency. An Agilent ADS™ simulator was used for total PA simulation. At 1.7 GHz, the transformer efficiency is 70% when the input is driven differentially with a single-ended output and 76% with a differential output. Simulated Qs of the primary and secondary windings in the output transformer are 9.3 and 9.4, respectively. The simulated k-factor between the two windings is 0.72. The tuning capacitors of the transformer, C_1 and C_2, are optimized to satisfy the class-E switching condition and minimize the passive loss of the transformer for each PA. The large signal S-parameter simulation and the transient response were checked for stability.

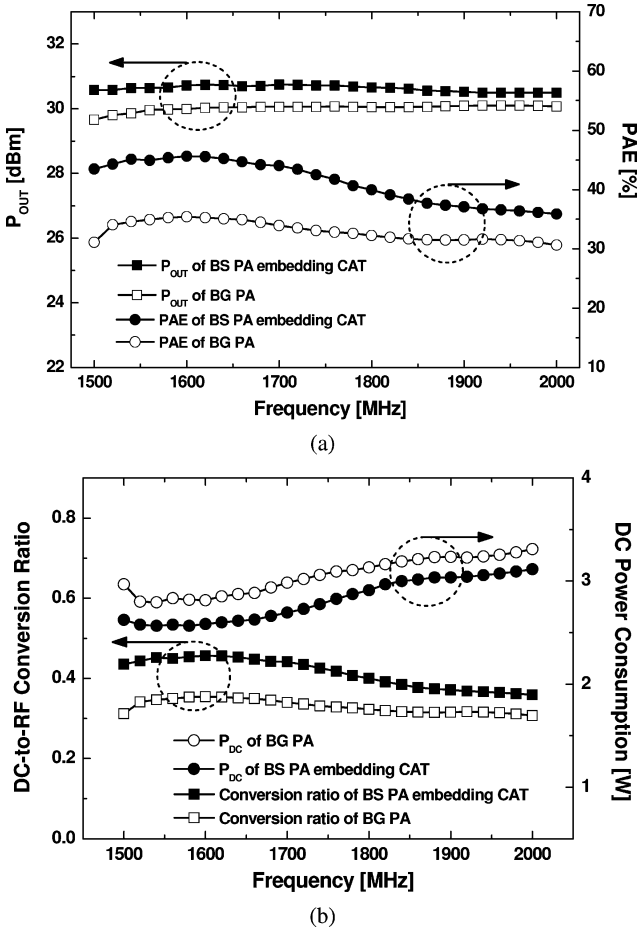

Fig. 19. (a) Measured output power and PAE as a function of the operation frequency. (b) Measured DC-to-RF conversion ratio and DC power consumption as a function of the operation frequency.

V. Measurement

Fig. 18 shows a microphotograph of the fully-integrated BS-cascode class-E PA embedding CAT fabricated in 1P6M 0.18-μm CMOS technology. The designs of the two PAs appear to be identical because the unique body connections of the M_2 cannot be recognized in a large-scale view. The die area is 2.15 mm × 0.8 mm, including the test pads. The bare die was mounted on the ground heat sink of a printed circuit board (PCB). The input and output pads were wire-bonded to a single 50-Ω micro-strip line. All the pads, including the input and the output, were wire-bonded on the PCB. The voltage drops of the bias cables and losses of the PCB lines have been carefully de-embedded in the calculation of the output power and the PAE, but the pad and bond-wire losses are included in the measurement results. The bias voltages of the power stage, V_{DDH}, and the driver stage, V_{DDL}, are set to 3.3 V and 1.8 V, respectively.

We measured the performance of each PA as a function of the frequency for an input power of 1.5 dBm. Maximum efficiency is achieved at a 1.6-GHz frequency in both cases, as shown in

TABLE I
A COMPARISON OF THE PERFORMANCE OF THE PAS

Power Amplifier	Technology	Power Consumption	Pout		PAE
		[W]	[W]	[dBm]	[%]
BG PA	CMOS 0.18 μm 1P6M	2.76	1.00	30.02	36.31
BS PA embedding CAT		2.58	1.18	30.72	45.62

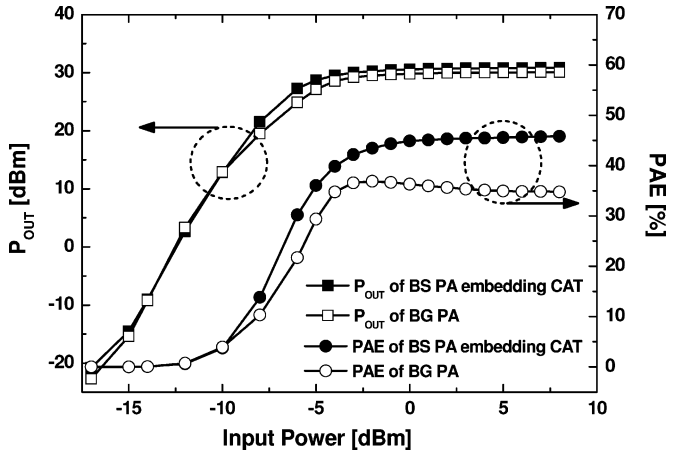

Fig. 20. Measured output power and PAE versus input power.

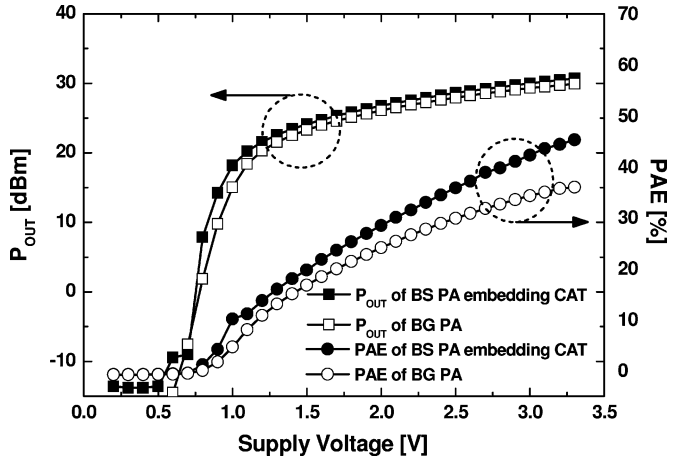

Fig. 21. Measured output power and PAE as a function of the supply voltage.

Fig. 19(a). It is likely that an underestimation of parasitic capacitances in the layout of routing line and transformer winding causes a 100-MHz downshift of the bandwidth. The maximum output power obtained from the BS-cascode class-E PA embedding CAT is 30.7 dBm with a PAE of 45.6% and a gain of 29 dB. Simulated power gains of driver and power stages are 19.05 dB and 10.58 dB, respectively. The output power, $\mathrm{P_{OUT}}$, and the PAE of the BS-cascode class-E PA improve 0.4 to 0.7 dB and 5 to 9%, respectively, across a range of 1.5 to 2.0 GHz. As shown in Fig. 19(a)–(b), although the DC power consumption of the BS-cascode class-E PA is smaller than that of the BG-cascode class-E PA, the $\mathrm{P_{OUT}}$ of the BS-cascode class-E PA is higher than that of the BG-cascode class-E PA. These findings indicate that a significant power loss reduction in the common-gate device results in high DC-to-RF conversion efficiency. Fig. 20 shows the measured $\mathrm{P_{OUT}}$ and PAE versus the input power at 1.6 GHz. The BS-cascode class-E PA shows a higher $\mathrm{P_{OUT}}$ and PAE with increasing input power than the BG-cascode class-E PA. Fig. 21 shows the performance of $\mathrm{P_{OUT}}$ and PAE with a supply voltage sweep. The output power increases proportionally to the square of $\mathrm{V_{DD}}$. More than 40 dB of the dynamic range was achieved with an adjustment of the power supply from 0.5 to 3.3 V. Table I summarizes a comparison of the PAs. To verify its potential in wireless communication applications, we tested the fabricated BS-cascode class-E PA by applying a Gaussian minimum shift keying (GMSK) modulated signal with $\mathrm{BT} = 0.3$. Fig. 22 shows the measured spectrum at the maximum output power with the GSM mask. The output spectrum of the PA was confined in the GSM spectral emission mask over the entire output power range.

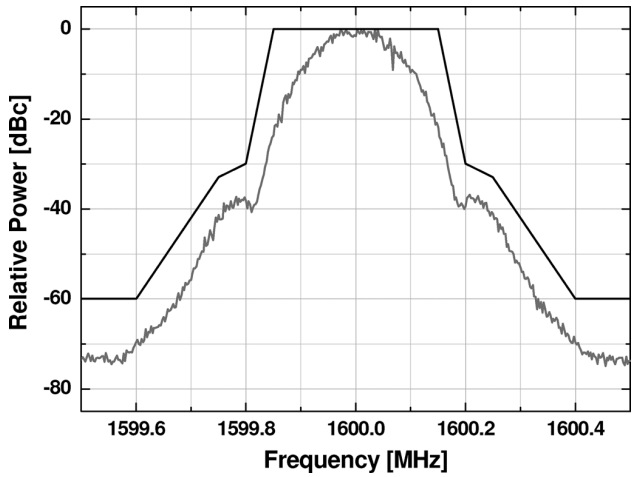

Fig. 22. Amplified GMSK modulated signal and the GSM spectrum emission mask of the BS-cascode class-E PA at 1.6 GHz ($\mathrm{BT} = 0.3$).

VI. CONCLUSION

In this work, we have fully analyzed the device power loss of cascode class-E CMOS PAs using the proposed equivalent model and provided an efficiency-enhancement technique that minimizes the power loss without adding any additional lumped elements. In a cascode configuration, proper capacitance between the drain and the source of a common-gate device significantly improves efficiency due to the minimization of the power loss. To demonstrate the CAT, we implemented two prototypes of CMOS PAs in a 0.18-μm CMOS process including input and output matching networks. The BS-cascode class-E

PA embedding CAT shows an improvement of 0.4 to 0.7 dB in output power and 5 to 9% in PAE. With the proposed CAT, a compact highly efficient class-E CMOS PA that provides high reliability can now be realized.

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Ockgoo Lee (S'05) received the B.S. degree in electrical engineering from Sungkyunkwan University in 2001, and the M.S. degree in electrical engineering from Korea Advanced Institute of Technology (KAIST), Daejeon, Korea, in 2005, and the Ph.D. degree in electrical and computer engineering at Georgia Institute of Technology, Atlanta, in 2009.

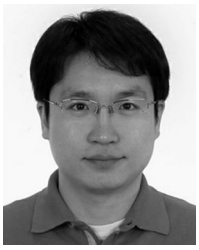
In the spring and summer of 2008, he was an intern with Qualcomm. Inc., San Diego, CA, where he worked on the investigation on inductors over active circuitry. He is currently with Qualcomm Inc., San Diego, CA. His current research interests include analysis and development of PAs and integrated passive circuit for multi-standards in sub-micron CMOS technologies.

Jeonghu Han (S'02–M'07) received the M.S. and Ph.D. degrees in electrical engineering and computer science from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2002 and 2006, respectively.

He has been a research staff at Georgia Institute of Technology, Atlanta, where he researched on CMOS power amplifier for wireless communication systems. He is currently working for Samsung Design Center, Atlanta. His research interests include RF device modeling and CMOS power amplifier development.

Kyu Hwan An (S'05) received the B.S. degree (*magna cum laude*) from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 1997, and the M.S. degree from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1999, both in electrical engineering, and the Ph.D. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, in 2009.

From 1999 to 2005, he was a research engineer with RF Lab, Samsung Electro-Mechanics Co. Ltd., Suwon, Korea, where he was involved with the development of power amplifier modules for CDMA, PCS, and GSM applications and physical layers for IEEE 802.15.3a/4 standards. His research interests include CMOS RF power amplifiers and switches for cellular applications and implementation of passive circuits on silicon substrate.



Dong Ho Lee received the B.S., M.S., and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2000, 2002, and 2007, respectively. His doctoral dissertation concerned the design of RF power amplifiers for linear and polar applications.

From 2007 to 2009, he was in the Microwaves Applications Group, Georgia Institute of Technology, where he was a Post-Doctoral Fellow and developed CMOS power amplifiers for mobile communications. Since 2009, he has been with Skyworks Solutions, Inc., Cedar Rapids, IA, where he has been involved with the design of power amplifiers and front end modules for cellular handsets. His research interests include RF power amplifier design, low power RF circuit design, and active device modeling in CMOS, GaAs HBT, and SiGe HBT processes. He holds eleven U.S. patents issued or pending.

Kun-Seok Lee (S'10) received the B.S. and M.S. degrees in electronics engineering from Korea University, Seoul, Korea, in 1999 and 2001, respectively. He is currently working toward the Ph.D. degree in electrical and computer engineering at Georgia Institute of Technology, Atlanta.

From 2001 to 2008, he was with the Samsung Electronics Company Ltd., Kyungki-Do, Korea, where he was a Senior Engineer involved in the design of sigma-delta FN PLLs and PLL-based transmitters for CDMA/GSM/GPRS/EDGE transceivers. His current research is focused on CMOS power amplifiers and RF/analog integrated-circuit design supporting multiple standard options for wireless applications.

Mr. Lee was the recipient of the Best Design Award at the First National Semiconductor IC Design and Layout Contest, Korea, in 2000.

Songcheol Hong (S'87–M'88) received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan at Ann Arbor in 1989.

In May 1989, he joined the faculty of the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. In 1997, he has held short visiting professorships with Stanford University, Palo Alto, CA, and Samsung Microwave Semiconductor, Suwon, Korea. His research interests are microwave integrated circuits and systems including power amplifiers for mobile communications, miniaturized radar, millimeter-wave frequency synthesizers, and novel semiconductor devices.

Chang-Ho Lee (S'97–M'01–SM'06) received the B.S. and the M.S. degrees in electrical engineering from Korea University, Seoul, Korea, in 1989 and 1991, respectively, and the M.S. and Ph.D. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, in 1999 and 2001, respectively.

He was a research engineer with DACOM Corporations, Korea, from 1994 to 1996. In 2000, he joined RF Solutions, Inc. Norcross, Georgia, where he was a staff engineer. In 2003, he joined Georgia Institute of Technology as a research faculty. From 2005, he is a head of the RF group in Samsung Design Center, as well as an Adjunct Professor at Georgia Institute of Technology. He has more than 100 technical conference presentations and journal publications, a book publication, and over 50 patents filing in the area of RFIC and module development.

Dr. Lee is a TPC member of IEEE IMS, RFIC, RWS, and ISCAS. He is a recipient of the third place of the best paper award at 2001 IEEE IMS, a co-recipient of the finalist of the best paper award at 2003 IEEE IMS, and a co-recipient of the finalist of 2004 ECWT Young Engineer Prize Award.