Investigation into SiGe HBT Class E/F PA Efficiency at 2 GHz for VDD From 1 to 1.8 V

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***Abstract*—This letter presents a 2-GHz SiGe heterojunction bipolar transistor fully integrated class E/F power amplifier (PA) design operating at low supply voltage. A maximum measured power added efficiency (PAE) of 39% is achieved for a supply voltage of 1.8 V. At 1 V, a maximum PAE of 36% is measured. The PA was fabricated using an advanced 0.18-μm BiCMOS process.**

***Index Terms*—Class E/F, heterojunction bipolar transistor (HBT), RFIC power amplifier (PA).**

I. Introduction

A primary aim of the BiCMOS integrated circuit (IC) industry is the complete integration of a transceiver circuit [1]. A major impediment to the achievement of this goal is the complete integration of power amplifiers (PAs). The advent of BiCMOS integration and the emergence of SiGe heterojunction bipolar transistors (HBTs) has reshaped the integrated circuit landscape. Although the silicon substrate offers the advantage of increased thermal conductivity, its lossy nature makes the design of high quality passive components difficult. Many PA solutions involve the active elements of the PA being fabricated *on*-chip while some, or all, of the critical matching networks are implemented *off*-chip. Making progress toward the single chip BiCMOS solution necessitates a migration from *off*-chip passive elements to a completely integrated architecture. Coupled with this factor is the need to implement PA designs with lower supply voltages. This work focuses on the analysis of the key elements that have been difficult to overcome in the drive for a single chip BiCMOS transceiver, namely *on*-chip spiral inductors and low supply voltages (1 to 1.8 V). To this end, a completely integrated low supply voltage class E/F PA, for operation at 2 GHz, has been fabricated in an advanced 0.18-μm SiGe:C RFBiCMOS technology [2].

II. Class E/F design

The origin of class F operation can be traced back to Tyler's classic paper [3], published in 1958, which introduced load resonant techniques to improve upon the efficiency and output power performance. The class E/F design procedure can be broken into two separate stages. First, the parameters of the active device are modified in order to give an effective switching action, while, at the same time maintaining enough gain for the particular frequency of operation. Second, the critical load network design is undertaken.

TABLE I
SiGe:C HBT Device Parameters for Minimum Sized Emitter [2]

Bipolar Parameter	Unit	SiGe:C HBT
Emitter Area	μm^2	0.25x0.5
Peak Current Gain	–	120
Intrinsic Base Resistance	Ω/□	1600
V_a	V	60
BV_{CEO}	V	3.3
$C_{je}(0)$	fF	1.2
$C_{jc}(0)$	fF	2.2
$C_{js}(0)$	fF	6.5
Peak f_T @ $V_{ce} = 2V$	GHz	50
Peak f_{MAX} @ $V_{ce} = 2V$	GHz	90

A. HBT Optimization

Table I presents the key HBT parameters for a minimum sized emitter geometry. The breakdown voltage, BV_{CEO}, of the HBT device is 3.3 V. However, in practical circuit applications the base terminal is usually not an open circuit, leading to increases in BV_{CER} [4]. The active device in a class F PA is generally operated as a current source. However, in this case the active device is operated as a switch. This produces a switching-mode operation similar to class E operation and for this reason the design is defined as class E/F. The emitter geometry, the main design variable, of the HBT device is modified to give a low *on*-resistance and a large *off*-resistance so that its operation approximates a perfect switch to the best degree possible. It was found that an emitter area of 19.2 μm^2 ($L_e = 12.25$ μm, $W_e = 1.57$ μm) provided the desired performance for both gain and switching action. With sufficient input drive the *on*-resistance of the HBT device reduces to 2.5 Ω. The saturation voltage, V_{cesat}, of the device is 0.214 V ($I_b = 25$ μA, $I_c = 5$ mA).

B. Load network design

The PA has no external passive components. The amplifier occupies 0.722 mm^2 ($L = 0.95$ mm, $W = 0.76$ mm) of die area. The class E/F schematic is shown in Fig. 1, while the corresponding chip layout is shown in Fig. 2. The load network consists of two resonant tank circuits and an output matching network. As the fundamental aim of this research was to investigate the efficiency of the HBT device and the influence of the load network on this, it was decided not to include an input matching network so that an isolated analysis of the load and the HBT could be carried out. Table II summarizes the component values

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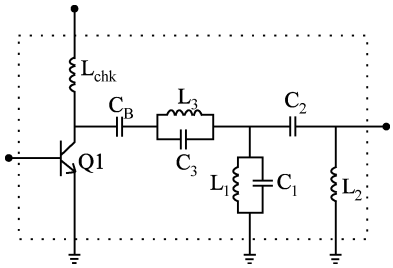

Fig. 1. Fabricated class E/F PA.

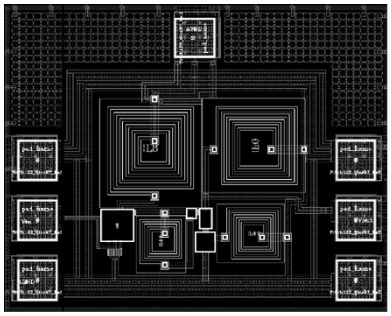

Fig. 2. Layout of fabricated PA.

TABLE II
SUMMARY OF COMPONENT VALUES FOR FABRICATED DESIGN OF FIG. 1

Passive Component	Value	Q @ 2 GHz
L_1	1.205 nH	14.33
C_1	3.64877 pF	-
L_2	3.39 nH	14
C_2	2.25 pF	-
L_3	597.863 pH	11.59
C_3	817.49 fF	-
L_{chk}	4.02 nH	13.93
C_B	10 pF	-

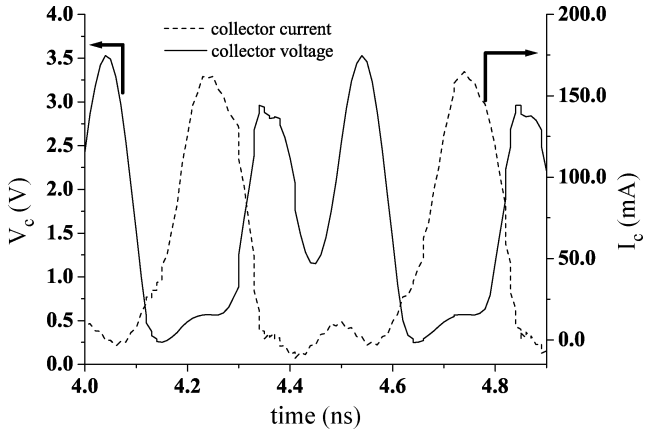

Fig. 3. Simulated collector voltage and current waveforms at 2 GHz for 1.8-V supply.

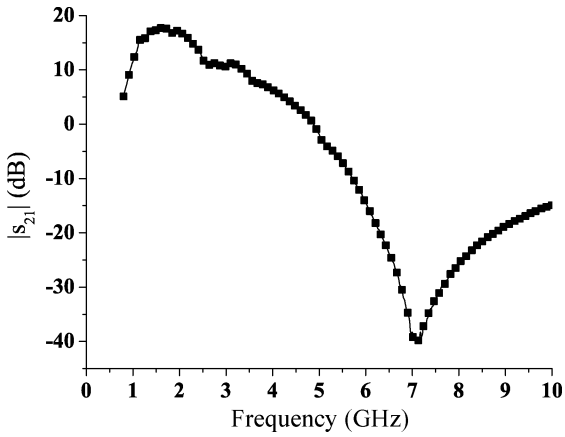

Fig. 4. Small signal measurement of PA gain.

of Fig. 1. L_{chk} ($R_{dc} = 1.76\,\Omega$), a basic spiral inductor, and C_B are simply RF and dc blocking components, respectively. The resonant circuit, L_3/C_3, presents a high impedance to the third harmonic of the fundamental, trapping it at the collector terminal. The parallel resonant tank, L_1/C_1, is tuned to the fundamental frequency and creates a sinusoidal output signal. Bondwire inductances were not an option for L_1, L_2, or L_3 given the load network layout so *on*-chip inductors were used. At 2 GHz, the entire load network presents an impedance of 27 Ω to the collector terminal.

The result of the combination of this two stage design procedure, which could be defined as an overdriven third harmonic peaking class E/F stage, can be seen from Fig. 3, which shows the collector voltage and current waveforms. As can be seen an effective switching action has been achieved. The shape of the collector voltage waveform is the result of the summation of the fundamental signal and its third harmonic [3].

III. MEASUREMENTS

In this discussion, the results presented are based on the utilization of the power on the base of the transistor as the input power. Knowledge of the nature of the load network impedance over a broad range of frequencies is critical for the determination of the optimum frequency of operation of a class F PA. This can be obtained by analysing the small signal gain, s_{21}, of the amplifier as shown in Fig. 4. It is critical that a small signal measurement is performed in this particular case so that the active device is kept in the linear region. As shown there is large attenuation in the gain at frequencies above approximately 4.5 GHz. Although the frequency response of the HBT device would have started to roll-off at this point, it is not responsible for such large levels of attenuation, especially considering that the gain begins to increase again once the frequency has gone beyond that region where the third harmonic tank has such a strong influence. The gain curve peaks in the region from 1.5 to 2.5 GHz. The third harmonics of all frequencies in the range from 1.5 to 2.5 GHz fall in the region of high attenuation. The optimum power added efficiency (PAE) performance is achieved at 2 GHz. Fig. 5 shows a set of measured PAE and output power (delivered to a 50-Ω load) results for various supply voltages at a base bias voltage of 0.45 V. Operating the PA at low base bias voltages enables an increased efficiency from class A type bias conditions to be achieved when the device is overdriven. For a supply voltage of 1.8 V and input power of 0.12 dBm, a PAE of 39% for a corresponding output power of 11.8 dBm (gain of 11.68 dB) is achieved. Coupled with achieving high efficiency for a completely integrated design was the desire to implement an amplifier that provides good performance at low supply voltages. Fig. 5 also shows the PAE and output power performance of the

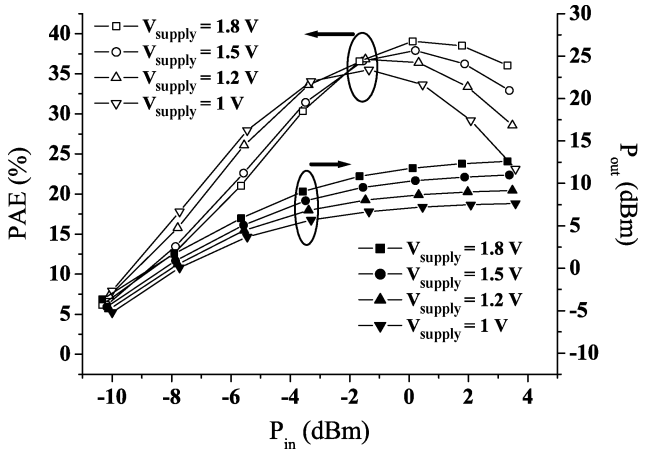

Fig. 5. Measured PAE and output power for various supply voltages.

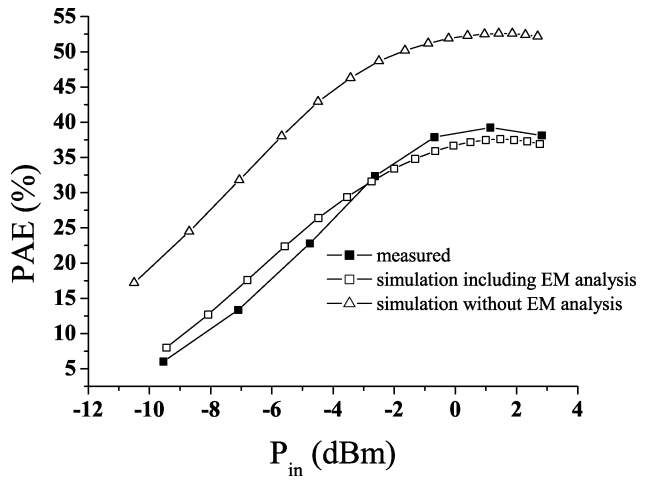

Fig. 6. Measured PAE versus simulation's with and without EM analysis.

amplifier at supply voltages of 1.5, 1.2, and 1 V. In all three cases, peak efficiencies of 36% and above are achieved. The maximum efficiency at 1 V, for an input power of -1.35 dBm, is 36% for an output power of 6.7 dBm (gain of 8.05 dB). This level of performance shows the potential for the compatibility of this design with low supply voltage digital CMOS circuits.

Of critical importance to a successful design effort is the accuracy of the simulation results. Fig. 6 shows a plot of simulated versus measured results for a supply voltage of 1.8 V and a base bias voltage of 0.45 V. The effects of layout parasitics have been incorporated into the simulation procedure through the use of electromagnetic (EM) analysis. Without EM analysis the maximum simulated value of PAE is 52%. However, once EM analysis of the layout is considered the maximum measured PAE is within 2% of the simulated value.

TABLE III
COMPARISON WITH PREVIOUSLY PUBLISHED RESULTS [5]–[10]

	Technology	Freq	PAE	Supply Voltage	Complete Integration
2005 [5]	CMOS	2.4 GHz	40%	3.3 V	No
2005 [6]	SiGe BiCMOS	WCDMA	44%	2.7 – 1.2 V	No
2001 [7]	CMOS	1.9 GHz	42%	3 V	No
2002 [8]	CMOS	1.4 GHz	49%	1.5 V	No
2001 [9]	CMOS	1.4 GHz	43%	1.8/3.0 V	No
2003 [10]	CMOS	1.4 GHz	70%/ 10%	2/1 V	Yes
This Work	SiGe BiCMOS	2 GHz	39%/36%	1.8/1 V	Yes

IV. CONCLUSION

The goal of this research was to investigate the main issues pertaining to complete BiCMOS PA integration. The design achieves a maximum measured PAE of 39%. The amplifier operates at a supply voltage of 1 V at which a PAE of 36% is measured. Reference [11] presents a fully integrated CMOS PA operating at 1 V with a PAE of 38% at 8 GHz that occupies 1.35 mm^2 of die area. However, the output matching networks are implemented using $\lambda/4$ lines which would not be practical from an area perspective at 2 GHz. Table III considers the merits of the presented work in comparison with recently published results in the same field and as can be seen very competitive performance has been achieved.

REFERENCES

[1] A. Hajimiri, "Fully integrated RF CMOS power amplifiers—a prelude to full radio integration," in *IEEE RFIC Symp. Dig.*, Jun. 12–14, 2005, pp. 439–442.
[2] J. Kirchgessner *et al.*, "A 0.18 μm SiGe:C RFBiCMOS technology for wireless and gigabit optical communication applications," in *Proc. BCTM'01 Conf.*, Sep. 30–Oct. 2 2001, pp. 151–154.
[3] V. J. Tyler, "A new high-efficiency high-power amplifier," *Marconi Rev.*, vol. 21, no. 130, pp. 96–109, Fall 1958.
[4] J. D. Cressler *et al., Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA: Artech House, 2003, p. 135.
[5] V. Saari *et al.*, "Integrated 2.4 GHz class-E CMOS power amplifier 2005," in *IEEE RFIC Symp. Dig.*, Jun. 12–14, 2005, pp. 645–648.
[6] I. A. Rippke *et al.*, "A single-chip variable supply voltage power amplifier," in *IEEE RFIC Symp. Dig.*, Jun. 12–14, 2005, pp. 255–258.
[7] F. Fortes *et al.*, "A second harmonic class-F power amplifier in standard CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1216–1220, Jun. 2001.
[8] A. Shirvani *et al.*, "A CMOS RF power amplifier with parallel amplification for efficient power control," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 684–693, Jun. 2002.
[9] T. C. Kuo *et al.*, "A 1.5 W class-F RF power amplifier in 0.2 μm CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 6, 2001, pp. 154–155.
[10] C.-C. Ho *et al.*, "A fully integrated Class-E CMOS amplifier with a class-F driver stage," in *IEEE RFIC Symp. Dig.*, Jun. 8–10, 2003, pp. 211–214.
[11] S. Hamedi-Hagh *et al.*, "A 1 V, 8 GHz CMOS integrated phase shifted transmitter for wideband and varying envelope communication systems," in *Proc. IEEE 2003 Custom Integrated Circuits Conf.*, Sep. 21–24, 2003, pp. 447–450.