Impedance Optimization of Linearizer to Suppress Intermodulation Distortion in 2.45GHz SiGe WLAN Power Amplifier

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***Abstract* — An RF power amplifier (PA) for IEEE 802.11g WLAN terminals is implemented with 33 GHz-f_T, 0.8-μm-SiGe bipolar technology. This paper demonstrates a linearizer consisting of a varactor diode and a base-emitter junction diode of a bias transistor. Intermodulation distortion (IMD) is suppressed by optimized impedance of the linearizer. The reactance of the varactor diode is minimized at low output power level to eliminate IMD3, and maximized near 1-dB compression point (P1dB). IMD3 is improved as much as 0.2~6 dB up to 20 dBm output power. The IMD3 value is less than – 34 dBc at 3 dB back-off from P1dB. The power amplifier exhibits P1dB of 24 dBm, with power-added efficiency (PAE) of 31%, and power gain of 17 dB under 3.3V power supply.**

***Index Terms* — SiGe bipolar technology, power amplifier, WLAN, varactor diode, linearizer, IEEE 802.11g, intermodulation distortion (IMD), error vector magnitude (EVM).**

I. INTRODUCTION

Silicon technology with useful advantages such as low manufacturing cost and high thermal conductivity is very attractive in power amplifier areas. A Si-based RF power device technology has been rapidly progressed for replacing GaAs HBTs due to its high integration and cost benefits. As well, SiGe HBTs have lower base-emitter turn on voltage (~0.75V) and comparable device performance (f_T/f_{max}:25/80 GHz, BV_{CEO}:6.5V) [1]. Therefore, recent research efforts have focused on linear power amplifiers using Si or SiGe technology for WLAN and CDMA applications [2]-[4].

In particular, the IEEE 802.11g standard supports a high data rate of up to 54Mbps using orthogonal frequency division multiplexing (OFDM) modulation. As this standard guarantees high data transmission, the OFDM signal has large peak-to-average power ratio (PAR) of 8~10 dB. So, the required output power for satisfying the stringent linearity characteristic is added to the PAR value. Mostly the amplifier is operated at back-off output power levels, thus sacrificing efficiency.

Therefore, a linearization scheme should be necessarily adapted to the power amplifier for improving nonlinearity such as intermodulation distortion. The on-chip linearizer is a good candidate since it does not require additional DC power consumption and die area. Recently, the linearizer, composed of a base-emitter junction diode and bypass capacitor or reverse biased diode, has been successfully adapted to the PA for CDMA handsets or WLAN terminals [5]–[9].

The linearizers of the applied active bias circuits introduce coupling components such as the bypass capacitor and reverse biased diode. Previously reported linearizers have improved P1dB well. However, at low and medium output power level, active bias circuits of the current mirror structure without any coupling components is the better choice to minimize third-order IMD since the base-emitter junction voltage of the power stage is well compensated in the weakly nonlinear region. Coupling components rather deteriorate third-order IMD characteristics than improve nonlinearity since these play a dominant role in noise elements. So, minimized reactance of the linearizer is required at low and medium output regions.

Reactance of the bypass capacitor is fixed regardless of the output power range [4]-[7]. On the other hand, the reverse biased diode serves as variable impedance, which is composed of constant capacitance and resistance up to a specific input power. While the large RF input signal is applied to the linearizer, equivalent capacitance drastically increases and equivalent resistance dynamically decreases resulting in more RF input signal for improving P1dB [8]-[9]. The requirement of a linearizer close to P1dB is similar to the reverse biased diode characteristic.

Consequently, the effective coupling component for a linearizer should maintain reactance value as low as possible at low and medium output regions to eliminate intermodulation distortion, rapidly increase equivalent capacitance and decrease equivalent resistance near P1dB.

In this paper, a varactor diode is selected to implement the effective coupling component, which can provide a wide range of capacitance compared to the reverse biased diode. Most of all, simulated varactor diode capacitance in accordance with output power is obtained to suppress

third-order IMD. By comparing two different reverse bias conditions of a varactor diode, the optimized impedance of the linearizer is realized.

II. SiGe Power Device Technology

The SiGe bipolar technology in this work is a 0.8-μm lithography double-poly hetero-bipolar technology for the linear power amplifier. The maximum BV_{ceo} is 6.5V for the NPN non-selectively implanted collector (SIC) HBT with a high breakdown voltage. The f_T/f_{max} is 33/90 GHz in the NPN non-SIC HBT. The thickness of the SiGe substrate material is selected to be as small as 180 μm to minimize the emitter inductance degeneration effect.

III. Impedance Optimization of Linearizer

The active bias circuit with the varactor diode is illustrated in Fig. 1. The cathode of the varactor diode is connected to the base node of the bias transistor HBT_2. The varactor diode is available to provide a different impedance configuration with a linearizer. The coupling component free structure for better IMD is suitable at low and medium power range. However, the S_{21} value of the coupling component must be necessarily increased to improve linearity at high output power. The equivalent capacitance of the varactor diode is plotted as a function of reverse voltage in Fig. 2. The capacitance value of the varactor diode with an area of 186 μm^2 varies from 0.048 pF to 0.218 pF depending on the applied reverse voltage.

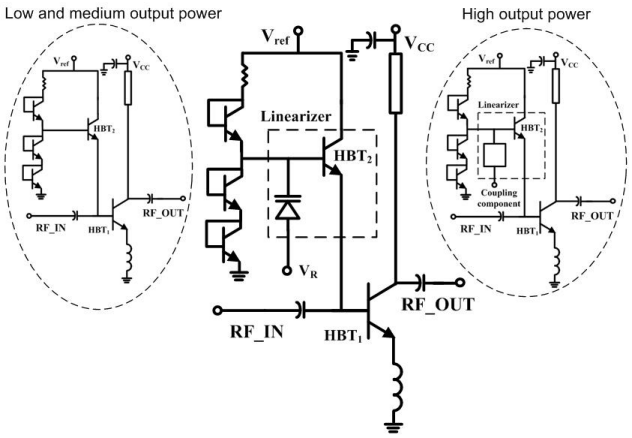

Fig. 1. Active bias circuit including the varactor diode.

When partial RF input power is applied to the varactor diode, the capacitance deviation of the applied reverse voltage V_{R2} more adaptively increases compared to the slowly varied capacitance of V_{R1}: ($|V_{R2}|>|V_{R1}|$) depending on the input power of the power stage in Fig. 3. The slope of V_{R1} is 0.2pF/dB and that of V_{R2} is 0.34pF/dB. The rapid slope of capacitance deviation represents that reactance value effectively increases for improving P1dB. In order to eliminate third-order IMD at low and medium power range, minimized reactance is preferable to constant reactance.

A bypass capacitor type of linearizer needs a fixed value of 1.2 pF regardless of RF input power. So, more rectified average DC current is provided with a bias transistor despite the low and medium output power level. In order to improve efficiency and third-order IMD, the optimized linearizer retains as low as possible reactance at low and medium power and dynamically increases reactance near P1dB.

From the simulation result, equivalent capacitance in the case of V_{R2} is almost constant up to 14 dBm and then drastically increases up to a value of 1.2 pF. The consumed average DC current is proportional to the variation of varactor capacitance. Therefore, the power-added efficiency of V_{R2} is better than that of V_{R1}.

The gain deviation depending on input power is shown in Fig. 4. The gain variation of V_{R2} is relatively low compared with that of V_{R1}, due to the varactor capacitance behavior.

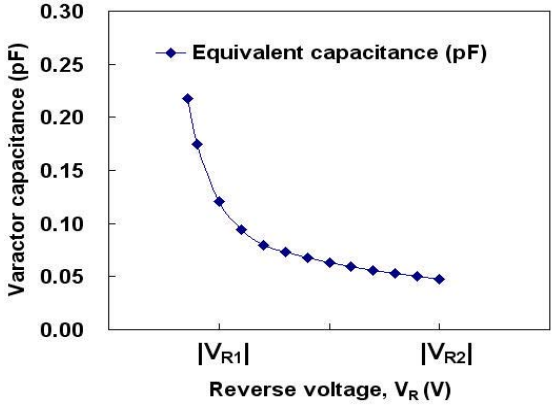

Fig. 2. Simulated equivalent capacitance of the varactor diode as a function of reverse voltages.

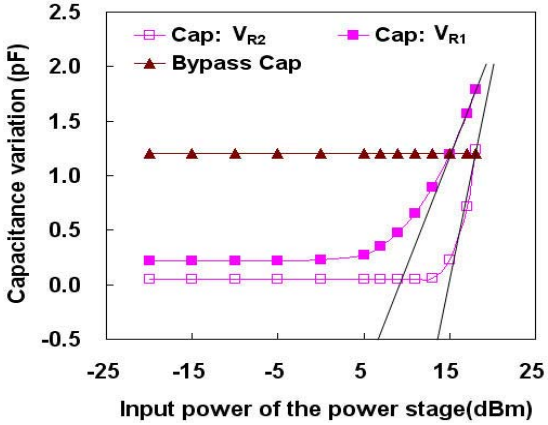

Fig. 3. Simulated capacitance variation of the varactor diode depending on input power of the power stage.

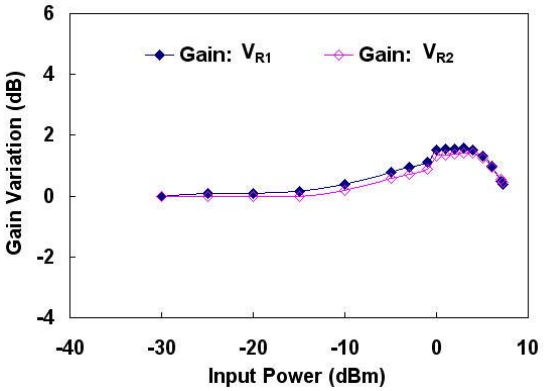

Fig. 4. Measured gain deviation depending on input power.

IV. Design Of The Power Amplifier

Fig. 5 shows a schematic of the two-stage SiGe bipolar power amplifier. The emitter area of the power stage is 2471 μm^2, while that of the driver stage is 160 μm^2. The two-stage PA operates with 73 mA of a low quiescent current. In order to improve stability and prevent thermal runaway, an emitter-ballasting resistor is employed for each unit HBT in the driver amplifier and the power amplifier. The off-chip output matching network is composed of two shunt capacitors, a series capacitor and a microstrip line for harmonic suppression.

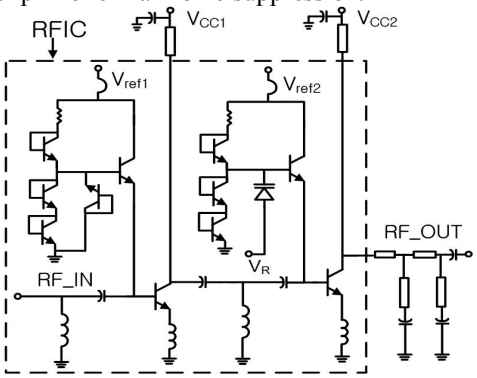

Fig. 5. Schematic of the two-stage SiGe bipolar power amplifier for IEEE 802.11g WLAN application.

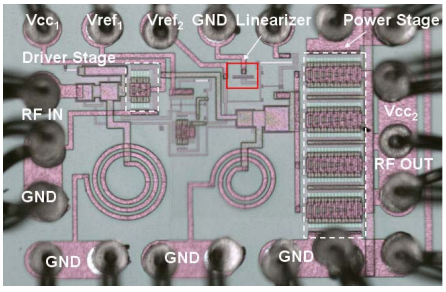

Fig. 6. Chip photograph of the SiGe bipolar PA.

The fabricated prototype SiGe bipolar PA is illustrated in Fig. 6. The overall chip size is 1x0.7 mm².

V. Measured Performance

The PA reveals 1-dB compression point of 24 dBm with PAE of 31% and power gain of 17 dB as shown in Fig. 7. Fig. 8 shows that the measured IMD3 in the case of applied reverse voltage V_{R2} is improved as much as 0.2~6 dB up to 20 dBm output power.

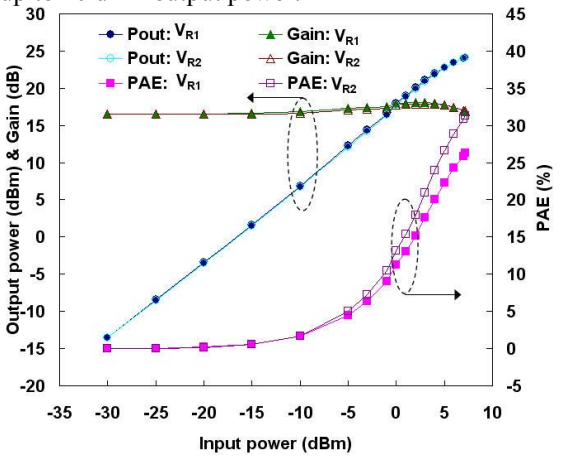

Fig. 7. Measured output power, power gain, and power-added efficiency versus input power (V_{R1}, V_{R2}).

The P1dB value of the power amplifier is the same as 24 dBm since the varactor capacitance increases more than 1.23 pF in both the V_{R1} and V_{R2} cases. However, the third-order IMD of V_{R2} is effectively improved over that of V_{R1} due to smaller varactor capacitance as shown in Fig. 3. The consumed collector current of V_{R2} is less than that of V_{R1} since the varactor capacitance of V_{R2} (V_{R1}) is relatively low, 1.2 (1.78) pF at P1dB.

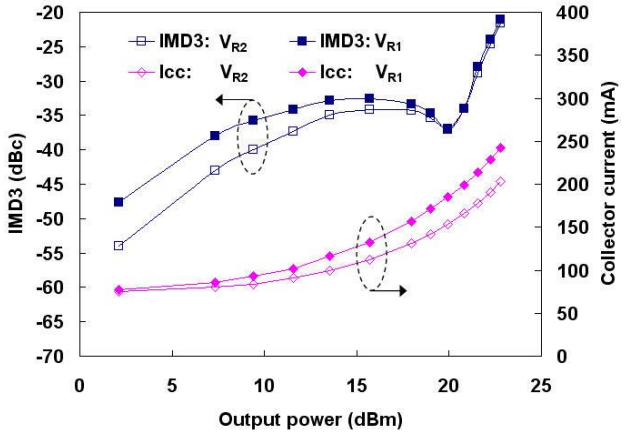

Fig. 8. Measured third-order IMD as a function of output power (V_{R1}, V_{R2}).

The value of error vector magnitude (EVM) is measured as a function of output power. Fig. 9 shows that the maximum average output power is 17.8 dBm to obtain less than the EVM value of 4.2 % rms in the case of V_{R2}. The EVM values of V_{R2} show better performance than those of V_{R1} in the same manner of IMD3 as shown in Fig. 8.

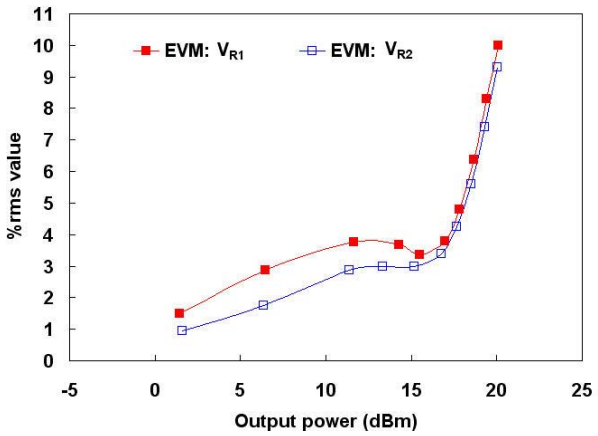

Fig. 9. Measured EVM values for V_{R1} and V_{R2}.

Performance Summary

Parameter	Measured Results
Frequency	2.45 GHz
Supply Voltage	3.3 V
Quiescent current	73 mA
Gain	17 dB
Output P_1dB	24 dBm
PAE	31%
Third-order IMD	> 34 dBc at 3 dB back off from P_1dB
EVM	4.2 %rms at 17.8 dBm
Reverse Isolation (S12)	> 35 dB

VI. Conclusion

We designed a linear SiGe bipolar power amplifier with an on-chip varactor diode linearizer. This linearizer effectively improves the nonlinearity of the PA. The power amplifier exhibits P1dB of 24 dBm, with a PAE of 31%, and power gain of 17 dB under 3.3V power supply. The third-order IMD value is less than -34 dBc at 3 dB back-off from P1dB at a frequency of 2.45GHz. The linearization technique employing a varactor diode is very helpful to provide optimized impedance configuration with an active bias circuit, requires no additional DC current, and has little insertion loss.

Acknowledgements

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