A Ka-Band Highly Linear Power Amplifier with a Linearization Bias Circuit

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***Abstract*—A Ka-band highly linear power amplifier (PA) with a linearization bias circuit implemented in 0.25 um SiGe BiCMOS for 5G millimeter-wave (mm-wave) phased arrays is presented in this paper. The PA demonstrates a measured 12.5-dB small signal gain, 16.5-dBm saturated output power and 31.1% peak power added efficiency (PAE) at 27 GHz. At 27.5 GHz, the proposed PA is tested with an 800 MHz bandwidth 64-QAM signal without digital predistortion, which achieves a PAE of 18.55%, error vector magnitude (EVM) of −29.6dB, and adjacent channel leakage ratio (ACLR) of −30.05dBc at an average output power of 11.44dBm.**

***Keywords*—Power amplifier (PA), SiGe, 5G, mm-wave, linearization bias circuit, linearity.**

I. Introduction

The 5th generation (5G) millimeter-wave (mm-wave) systems are expected to provide extremely high communication rate and spectral efficiency in order to face more complex application scenarios. To fulfil the increasing demand for high data-rates, the future 5G mobile networks will use more complex modulation schemes and massive multiple-input multiple-output (MIMO) technique. However, complex modulation with high peak to average power ratios (PAPRs) and large RF bandwidths will require higher performance of power amplifier (PA) especially the linearity [1]. The traditional approach is to use digital predistortion (DPD), but for a massive MIMO system, the application of DPD on each channel will result in higher complexity and digital power consumption [2]. In addition, 5G signal bandwidth may be up to 800MHz, and the high ADC sampling rate also leads to high power consumption. So the burden of DPD may be reduced if an auxiliary design is applied to the circuit.

To alleviate these challenges, we propose a highly linear power amplifier with a linearization bias circuit in this paper, and this linearization bias circuit is first demonstrated in mm-wave silicon-based PA [3]. By applying the linearization bias circuit, the PA achieves a power added efficiency (PAE) of 18.55%, error vector magnitude (EVM) of −29.6dB, and adjacent channel leakage rate (ACLR) of −30.05dBc at an average output power of 11.44dBm with an 800 MHz bandwidth 64-QAM signal. To the best of the author's knowledge, the proposed PA achieves the highest average output power and good average efficiency for the same linearity criterion.

II. Circuit Analysis and Design

The nonlinearity of PA based on heterojunction bipolar transistor (HBT) is mainly caused by the nonlinearity of base-emitter diode of the input amplification transistor.

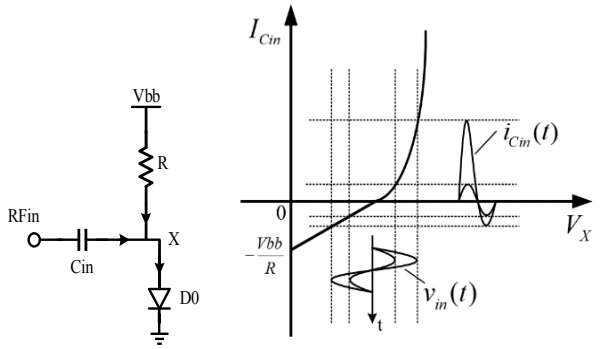


Fig. 1. The equivalent circuit of the conventional resistance bias circuit and its input IV characteristic curve.

The input IV characteristic curve of the conventional resistance bias circuit is asymmetrical, as shown in Fig. 1, it is linear in low input voltage range, while exponential in high input voltage range. The capacitor's state is steady when the average current flowing through it is zero. Therefore, when the input voltage is increased, in order to satisfy the steady-state condition of the capacitor, the dc operating point will decrease, resulting in a decrease in the transconductance and gain.

To solve this problem, we propose a linearization bias as shown in Fig. 2, which consists of a resistor, a bypass capacitor, two diodes, and a compensation diode. Because of the bypass capacitor C1, the dc voltage at the Y point is approximately constant, and its value is determined by the resistance R and the two diodes D2 and D3. The IV characteristic curves of D0 and D1 are given by

$$I_{D0} = f(V_X) \tag{1}$$

$$I_{D1} = f(V_Y - V_X). \tag{2}$$

(1) and (2) are symmetric about the voltage $\frac{V_Y}{2}$. The current flowing through the capacitor is given by

$$I_{Cin} = I_{D0} - I_{D1} = f(V_X) - f(V_Y - V_X). \tag{3}$$

(3) indicates that the current I_{Cin} is centrally symmetric about the voltage of $\frac{V_Y}{2}$. Since the input IV characteristic curve is centrosymmetric, when the input voltage is increased, the steady-state condition of the capacitor is not affected, so the dc operating point does not change, thereby achieving good linearity at a large signal.

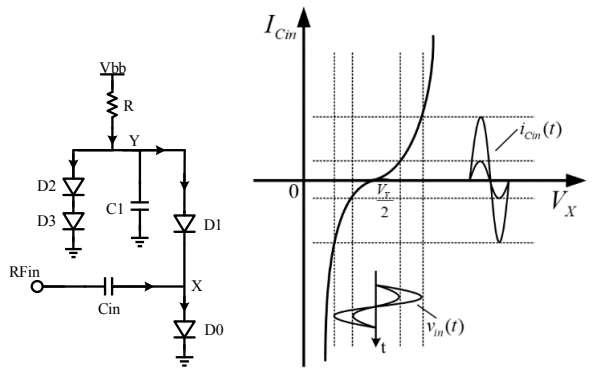
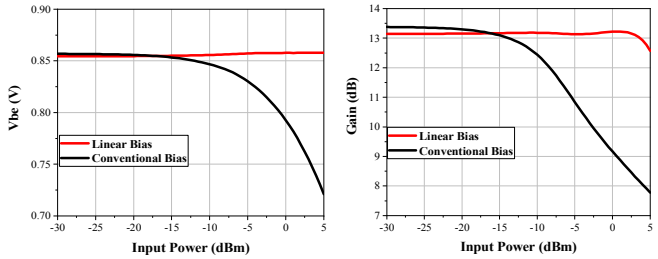


Fig. 2. The equivalent circuit of the linearization bias circuit and its input IV characteristic curve.



(a) (b)

Fig. 3. Simulation comparison between conventional resistance bias and linearization bias (a) DC operating point (b) Gain.

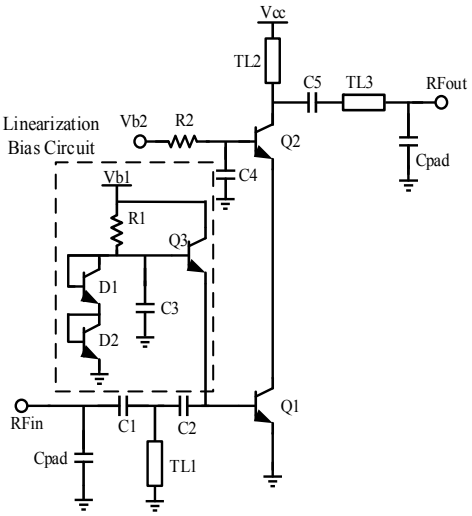


Fig. 4. Schematic of the designed PA with a linearization bias circuit.

Fig. 3 compares the dc operating point voltage and gain with conventional resistance bias and linear bias. It can be seen from the comparison results that the dc operating point almost unchanged with the input power after adopting linear biasing, and the gain of 1dB compression is greatly expanded. Therefore, the linearity of the circuit has been greatly improved. Fig. 4 shows the schematic of the proposed PA with the linearization bias circuit.

III. Measurement Results

The designed PA is implemented in IHP 0.25um SiGe BiCMOS process with a chip size of 0.625×0.439mm^2, as shown in Fig. 5. S-parameter simulation and measurement results of the PA are depicted in Fig.6. The forward gain S_{21} shows a good agreement with the simulation and achieves 12.5 dB gain at 27 GHz.

The measured and simulated large-signal performances at 27 GHz are illustrated in Fig. 7. A peak output power of 16.5dBm with a PAE of 31.1% can be achieved. Also, the amplifier shows a P1dB of 15.9dBm with an associated PAE of 30.6%. It should be emphasized that an excellent PAE up to 16% is obtained at 7 dB back-off output power. This back-off PAE is particularly important when the PA is used for complex modulation signals, as demanded for mobile mm-wave phased arrays system.

Fig. 8 and Fig. 9 show the measured ACLR and EVM at 27.5 GHz. The PA achieves PAE of 18.55%, EVM of −29.6 dB, and ACLR (upper band) of −30.05dBc at an average output power of 11.44dBm for a 64-QAM signal with 800 MHz bandwidth. When tested with an 800 MHz bandwidth 256-QAM signal, the PA achieves PAE of 16.67%, EVM of −33.3 dB, and ACLR (upper band) of −31.06dBc at an average output power of 10.55dBm.

Table I compares this work with the state-of-the-art silicon-based PAs around Ka-band frequencies. For the same linearity criterion, the proposed PA achieves the highest average output power and good average efficiency.

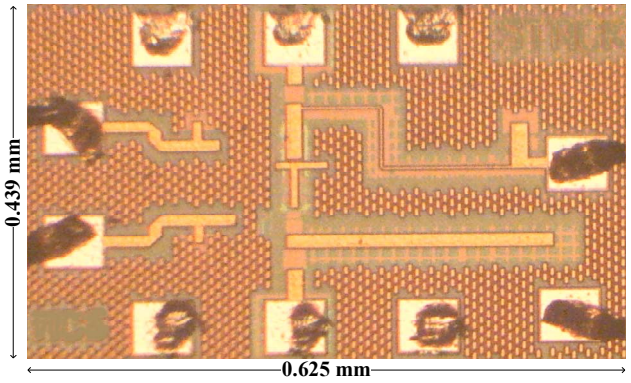


Fig. 5. The chip photo of the presented power amplifier.

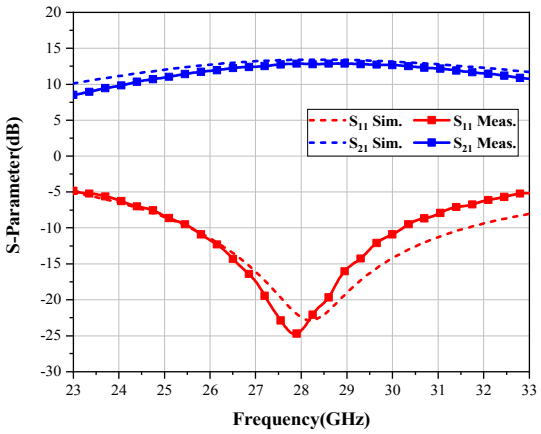


Fig.6. Measured and simulated S-parameters.

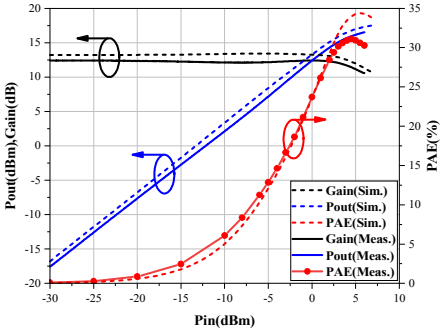


Fig.7. Measured and simulated Gain, Pout, and PAE at 27 GHz.

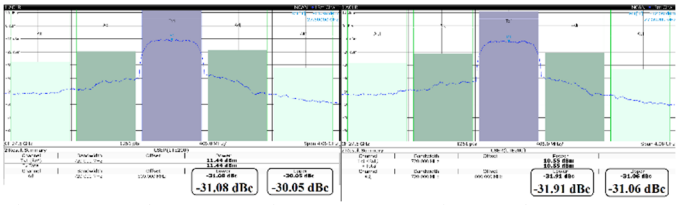


Fig.8. Measured ACLR waveforms at 27.5 GHz for 64 and 256-QAM, 800-MHz signals.

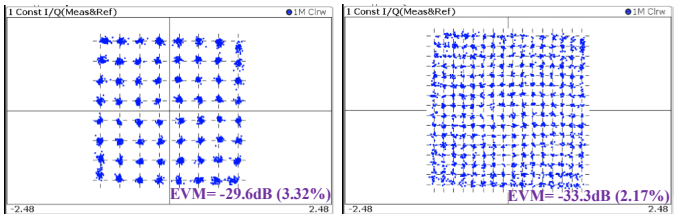


Fig.9. Measured constellation and EVM at 27.5 GHz for 64 and 256-QAM, 800-MHz signals.

IV. Conclusion

This paper presents a highly linear power amplifier with a linearization bias circuit using a 0.25um SiGe BiCMOS process. At 27 GHz, the PA achieves 12.5 dB small signal gain, 16.5-dBm saturated output power and 31.1% peak PAE. The PA achieves PAE of 18.55%, EVM of −29.6 dB at an average output power of 11.44dBm with an 800 MHz bandwidth 64-QAM signal. When tested with an 800 MHz bandwidth 256-QAM signal, the PA achieves PAE of 16.67%, EVM of −33.3 dB at an average output power of 10.55dBm. Compared with the reported silicon-based PAs around Ka-band frequencies, the PA presented in this paper achieves the highest average output power and good average efficiency.

Acknowledgment

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Table 1. Comparison with state-of-the-art mm-wave silicon PAs.

Reference	Freq. (GHz)	Gain (dB)	Po.1dB (dBm)	Po.sat (dBm)	PAE 1dB (%)	PAE sat (%)	Modulated Signal	RF BW (MHz)	Data rate (Gb/s)	ACLR (dBc)	EVM (dBc)	Po@ EVM (dBm)	PAE@ EVM (%)	Active Area (mm2)	Topology	Tech.
This work	**27.5**	**12.5**	**15.9**	**16.5**	**30.6**	**31.1**	**64-QAM**	**800**	**3.6**	**-30.05**	**-29.6**	**11.44**	**18.55**	**0.27**	**1-Stage Cascode**	**0.25um SiGe**
							256-QAM	**800**	**4.8**	**-31.06**	**-33.3**	**10.55**	**16.67**			
[1] JSSC 16	30	15.7	13.2	14	34.3	35.5	64-QAM	250	-	-	-25	4.2	9	0.16	2-Stage Diff.	28nm CMOS
[4] MTT 17	28	15.3	15.5	18.6	31.5	35.3	16-QAM	800	-	-	-22	10.6	-	0.45	1-Stage Cascode	0.13um SiGe
[5] ISSCC 17	28	18.2	15.2	16.8	19.5	20.3	64-QAM	-	3	-28.4	-27	9.2	8.5	1.76	Doherty	0.13um SiGe
[6] ISSCC 18	28.5	20	15.2	17	39.3	43.5	64-QAM	-	6	-	-27.6	10.7	21.4	0.29	2-Stage Diff.	0.13um SiGe
							256-QAM		4	-	-31.3	8.8	16.2			
[7] MTT 18	28	8.9	13.6	14.4	37.2	40.1	64-QAM	250	-	-	-26.6	7	14.1	0.11	1-Stage CS	65nm CMOS