A 3-V Monolithic SiGe HBT Power Amplifier for Dual-Mode (CDMA/AMPS) Cellular Handset Applications

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***Abstract*—A dual-mode (CDMA/AMPS) power amplifier has been successfully implemented by using a monolithic SiGe/Si heterojunction bipolar transistor (HBT) foundry process for cellular handset (824–849 MHz) applications. The designed two-stage power amplifier satisfies both CDMA and AMPS requirements in output power, linearity, and efficiency. At $V_{cc} = 3$ V, the power amplifier shows an excellent linearity (first ACPR < -44.1 dBc and second ACPR < -57.1 dBc) up to 28 dBm of output power for CDMA applications. Under the same bias condition, the power amplifier also meets AMPS handset requirements in output power (up to 31 dBm) and linearity (with second and third harmonic to fundamental ratios lower than -37 dBc and -55 dBc, respectively). At the maximum output power level, the worst power-added efficiencies (PAEs) are measured to be 36% for CDMA and 49% for AMPS operations. The power amplifier also tolerates severe output mismatch (VSWR $>12:1$) up to $V_{cc} = 4$ V, with spurs measured to be < -22 dBc in CDMA outputs at two specific tuning angles, but with no spur in AMPS outputs at any tuning angle.**

***Index Terms*—Dual-mode cellular handset, monolithic integration, power amplifier, SiGe HBT.**

I. Introduction

FOR THE past several years, AlGaAs/GaAs heterojunction bipolar transistor (HBT) power amplifiers have dominated the CDMA handset transmitter market due to their excellent linearity and power-added efficiency (PAE). However, GaAs-based integrated circuits are relatively expensive and must be thinned for optimum performance in power amplification. Compared with AlGaAs/GaAs HBTs, SiGe/Si HBTs are more attractive primarily due to their high substrate thermal conductivity (150 W/m-° C), comparable device performance (f_t ~30 GHz and $f_{\max}$ ~50 GHz), lower emitter/base turn-on voltage (~0.75 V), and substantially lower production cost. Unfortunately, SiGe/Si HBTs have their own disadvantages: the substrate is very conductive, adding significant parasitics to both active and passive components of the power amplifier. SiGe HBTs also have relatively low breakdown voltages (BV_{ceo}~5 V; BV_{ces}~14.5 V) and low Early voltage (~140 V) versus >1000 V in GaAs HBTs. These characteristics are detrimental to the gain, linearity, and dynamic range of the power amplifier.

Recently, efforts have been made in making SiGe/Si HBT power amplifiers for DECT and GSM handset transmission applications [1]–[4]. However, the output power of the DECT is relatively low (24 dBm) and the linearity requirement of the GSM is far less restrictive than that of the CDMA. To further demonstrate the linearity and PAE of the SiGe HBT power amplifier at a significant power level, we have designed and characterized a monolithic SiGe/Si HBT power amplifier for dual mode (CDMA/AMPS) cellular handset applications.

The power amplifier design specifications are:

1) **Maximum output power**: 28 dBm for CDMA and 31 dBm for AMPS;
2) **Linearity for CDMA**: first ACPR < -44.1 dBc and second ACPR < -57.1 dBc with offset frequencies set at 885 kHz and 1980 kHz, respectively. The detailed measurement specifications are described in [5];
3) **Linearity for AMPS**: with second and third harmonic to fundamental ratios < -30 dBc at any output power level;
4) **Power-Added Efficiency (PAE)**: >35% for CDMA and >45% for AMPS measured at the peak output power level.

II. Circuit Design

We use a two-stage amplifier configuration to fulfill the dual-mode design goals. A simplified schematic of the designed power amplifier is shown in Fig. 1, which comprises driver and power amplification stages, input, interstage and output matching networks, and bias circuits for the driver and power stages, respectively. To satisfy the output power requirement, total emitter areas of the driver and power HBTs are chosen to be 480 μm^2 and 3360 μm^2, respectively. Each HBT unit cell has an emitter size of 20 μm^2.

For power HBTs at extremes of voltage and current, a thermal–electrical feedback mechanism may constrict the emitter current to localized hot spots and eventually lead to second breakdown (or "thermal runaway") and catastrophic failure [6]. Emitter and base ballasting resistors are often used to counter this regenerative effect and force uniform current and temperature distributions across large-size transistors. In our design, only base ballasting resistors are used [7]. Emitter-ballasting resistors are excluded for directly reducing the output signal swing at the collector node. The minimum base ballasting resistance required to reverse the onset of

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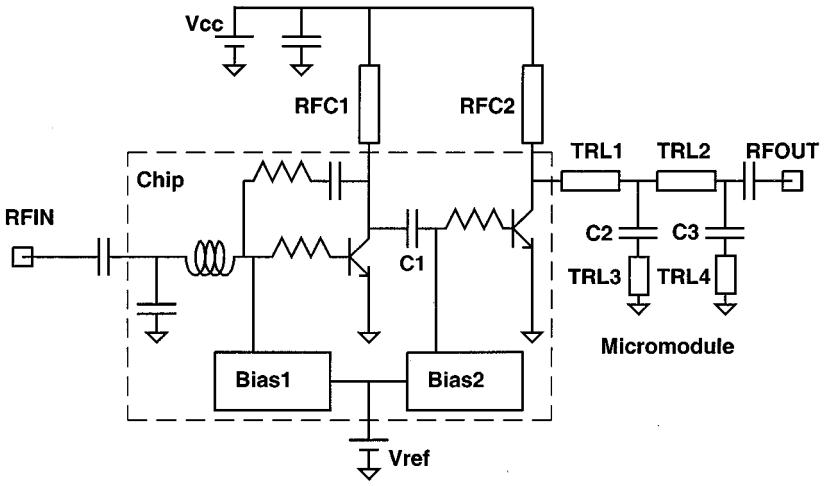


Fig. 1. Simplified schematic of a cellular handset power amplifier. On-chip components are surrounded by the dashed line.

thermal runaway can be calculated according to the dependence of collector current on the junction temperature [8], as follows:

$$I_c = I_{so} \cdot \exp\left(\frac{qV_{be} - qI_c[r_e/\alpha + (r_b + R_{\text{base\_ballast}})/\beta] - E_g}{kT_j}\right) \tag{1}$$

where

I_c	collector current;
V_{be}	base–emitter dc bias voltage;
T_j	junction temperature of the device;
r_e	transistor emitter resistance;
r_b	transistor base resistance;
$R_{\text{base\_ballast}}$	external base ballasting resistance;
I_{so}	reverse saturation current of the emitter–base junction;
α	common base current gain;
β	$= \alpha/(1-\alpha)$;
E_g	energy gap of the SiGe base material.

With low Germanium content (average 4%) in the base, the temperature dependence of E_g can be approximated by that of pure silicon [9],

$$E_g(T_j) = E_g(0) - \frac{4.73 \times 10^{-4} T_j^2}{(T_j + 636)} \tag{2}$$

and the temperature dependence of the HBT current gain can be represented by

$$\beta(T_j) = \beta(T_A^0)\left(\frac{T_j}{T_A^0}\right)^{XTB} \tag{3}$$

where $T_A^0 = 298$K and $XTB = -0.5$ from [10]. The threshold for the onset of thermal runaway is

$$(\partial J_c/\partial V_{be})^{-1} = 0. \tag{4}$$

Fig. 2 shows the collector current density J_c as a function of base–emitter bias V_{be}, calculated based on (1)–(4) with various base ballasting resistances. It is obvious from Fig. 2 that

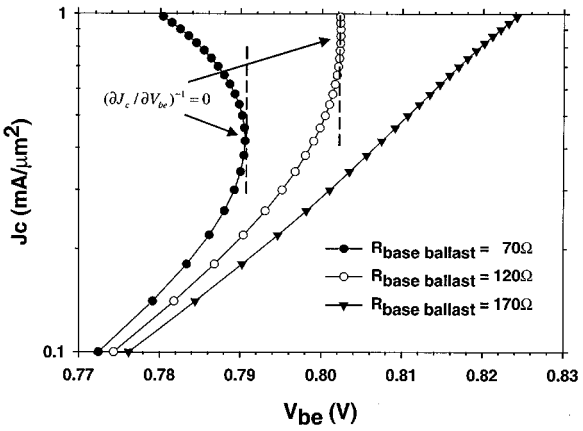


Fig. 2. Calculated collect current density versus base–emitter bias voltage for power HBTs constrained by various base ballasting resistances at $T_A = 358$ K.

the base ballasting resistance must exceed 120 Ω per unit cell to reach a thermal stable operation of the power HBT at the highest ambient temperature ($T_A = 358$ K) required for cellular handset operation. To be conservative, we have chosen the base resistance to be 170 Ω per unit cell. Since it is significantly higher than the intrinsic base resistance (12 Ω per unit cell) of the HBT, the base ballasting resistance also provides a relatively high and stable input impedance for the second-stage amplifier to be easily matched to the output of the first-stage amplifier.

The interstage matching network in our design contains a coupling capacitor C1 and an RF chock made of an off-chip transmission line (RFC1), which links between the V_{cc} and the collector of the first-stage amplifier. The RFC1 (<150 mil long) is chosen to minimize the gain variation over the frequency band and the capacitor C1 (<30 pF) is used to cut off the low-frequency gain and eliminate amplifier oscillation. The input matching of the first-stage amplifier is achieved by using an on-chip *LC* network. The inductor (about 5 nH) has a Q of 4 at 0.9 GHz; on-chip capacitors which are made of MOS devices enjoy very high capacitance per area (1.5 fF/μm^2) with a Q of 33 at 0.9 GHz.

To design a power amplifier with both high linearity and high PAE, we use an *RC* feedback network to linearize the first stage

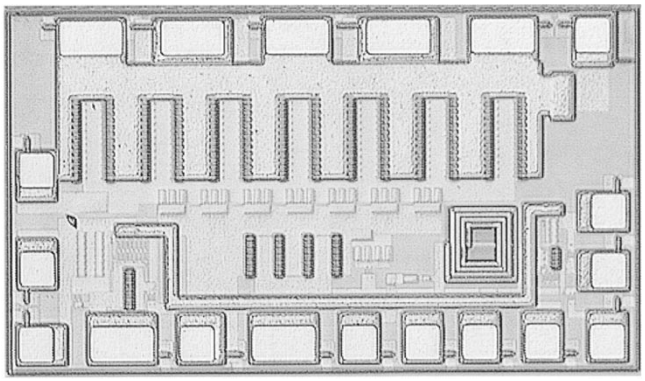


Fig. 3. Microphotograph of a fabricated CDMA/AMPS SiGe HBT power amplifier.

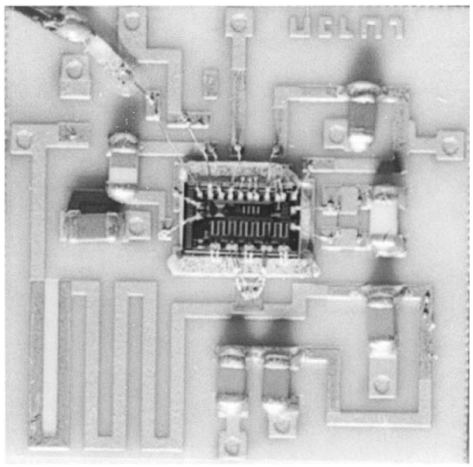


Fig. 4. Fabricated SiGe HBT power amplifier micromodule.

and bias the second stage at a rather low quiescent point to trade for high PAE. In the micromodule, two microwave transmission lines, TRL1 and TRL2 (110 mil and 250 mil long, respectively), are implemented on alumina substrate to transform low output impedance of the second-stage power HBT (about 3 Ω) to the standard 50-Ω output. Harmonic tuning techniques are also employed to suppress the second and third harmonics at the output by using shunt resonators made of microwave transmission lines (TRL3 and TRL4) in series with shunt capacitors. For instance, TRL3 (38 mil long) is designed to resonate with a serial capacitor C2 (10 pF) to reflect the second harmonic signal. Similarly, TRL4 (8 mil long) is designed to resonate with the capacitor C3 (5.6 pF) to reflect the third harmonic signal. Since primary harmonic components are mostly eliminated from the amplifier output, the linearity and efficiency of the power amplifier are significantly enhanced.

Bias circuits for both driver and power stages are designed with current mirrors to regulate their quiescent currents. Current mirror ratios are chosen for the delicate tradeoff between the thermal stability and PAE of the power amplifier. Bias circuits with lower current mirror ratios are more effective in regulating the bias of large power HBTs, but at greater expense of PAE. Bias circuits with excessively high current mirror ratios have the adverse effects. In addition, the specific value of the current mirror ratio is also constrained by the detailed layout considerations. A moderate current mirror ratio of 8 : 1 is chosen to balance the demands in both PAE and the thermal stability of the amplifier.

Based on our design, a fabricated SiGe/Si HBT power amplifier IC is shown in Fig. 3. The chip is very compact (2.0×1.0 mm^2) in size and can be easily housed in a micromodule, as shown in Fig. 4. Emitter bonding pads are enlarged to incorporate more bonding wires to minimize the potential feedback inductance. Through-substrate via-holes are also avoided for achieving an easy manufacturing. With input and interstage matching networks and bias circuits built on-chip, the amplifier leaves very few extra components (mainly the output matching stage and RF chokes) to the micromodule for handset transmitter insertion.

Extensive simulations are conducted by using both time and frequency domain simulators to optimize the power amplifier performance. HP-Advanced Design System (ADS) is used for circuit simulations; Gummel–Poon model is employed for large-signal device simulations. Comparisons between simulated and measured results are presented in Section IV.

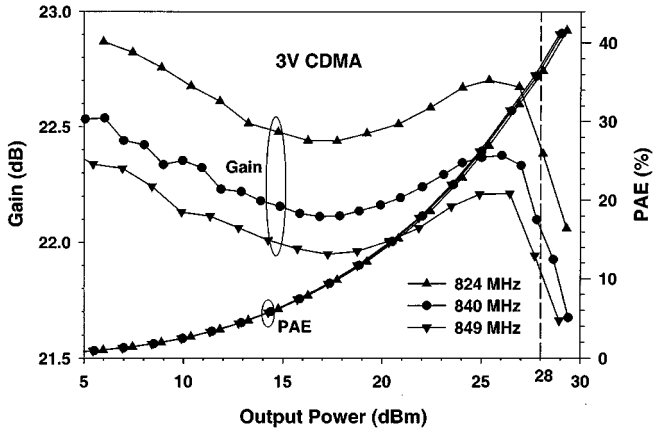


Fig. 5. Gain and PAE versus CDMA power amplifier output power as a function of operating frequency.

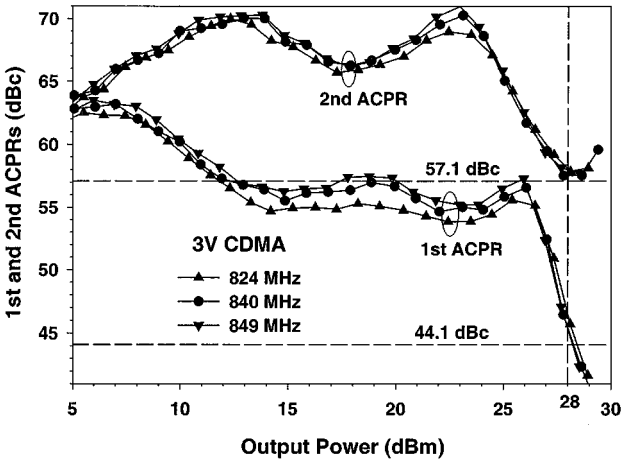


Fig. 6. First and second ACPRs versus CDMA power amplifier output power as a function of operating frequency.

III. Circuit Performance Measurement

We have characterized the power amplifier for both CDMA and AMPS applications. Figs. 5 and 6 show the gain, PAE (%)

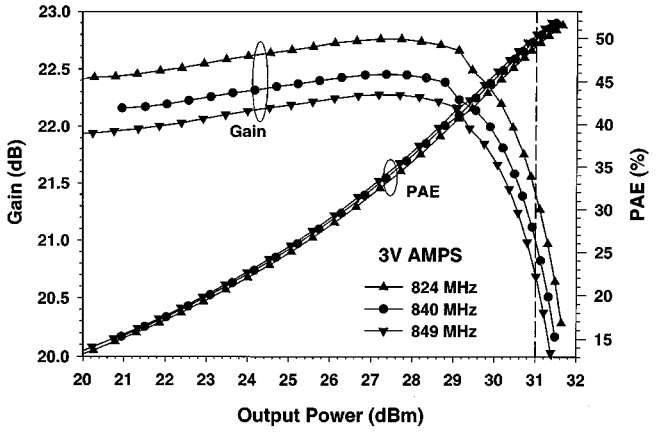


Fig. 7. Gain and PAE of versus AMPS power amplifier output power as a function of operating frequency.

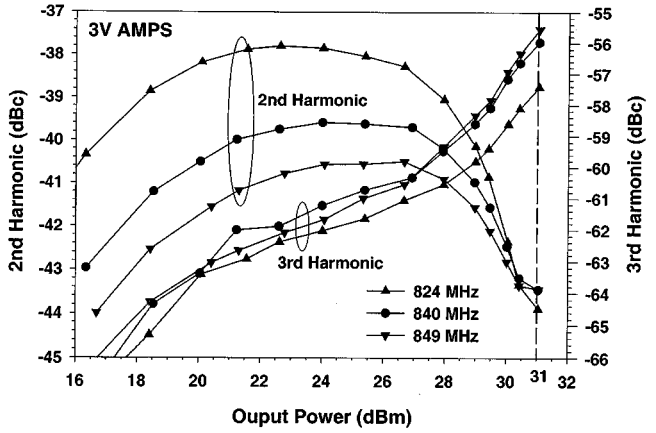


Fig. 8. Second and third harmonics versus AMPS mode output power as a function of operating frequency.

and the linearity (represented by first and second ACPRs) versus the output power over the frequency band (824–849 MHz). For CDMA operation, the amplifier satisfies linearity requirements at $V_{cc} = 3$ V with first ACPR better than -44.1 dBc and second ACPR better than -57.1 dBc with output power up to 28 dBm. The amplifier gain varies between 22–23 dB with PAEs of 36%–37% at 28 dBm output power.

Fig. 7 shows the gain and PAE (%) versus the output power for AMPS operation. The amplifier satisfies the maximum output power requirement of 31 dBm at $V_{cc} = 3$ V with 21 dB gain and 49%–51% PAE. As shown in Fig. 8, the amplifier shows very low second and third harmonics, measured to be lower than -37 dBc and -55 dBc, respectively. The input return loss is always measured below -12 dB at any input level in Fig. 9.

The power amplifier even meets dual-mode linearity specifications at $V_{cc} = 2.7$ V over the operating frequency band. At this collector-supply voltage, the PAE slightly decreases to 33% for CDMA and 48% for AMPS operation. The maximum input return loss slightly increases to -10 dB. These results are carefully compared with that of simulations in Section IV.

An infrared scanning camera is used to characterize the thermal property of the power amplifier IC. A dome-shaped temperature profile is evenly distributed across the HBT power

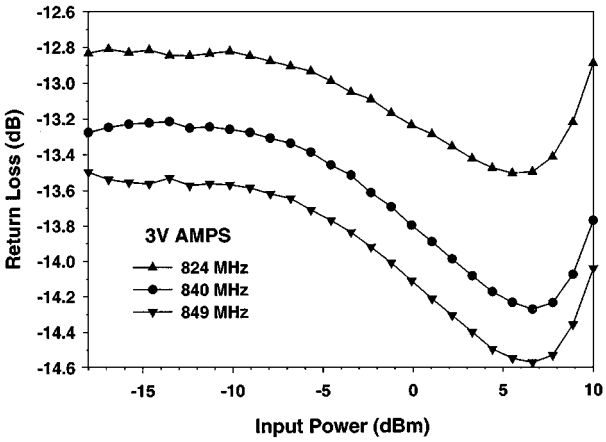
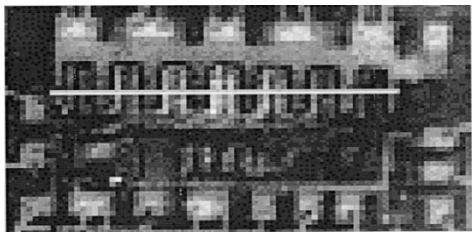
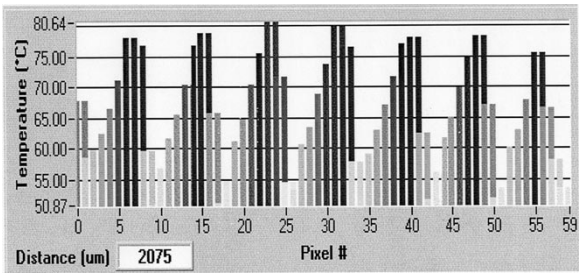


Fig. 9. Input return loss as a function of operating frequency.



(a)



(b)

Fig. 10. (a) Infrared image of a SiGe HBT power amplifier under 1 W output power operation (the ambient temperature is set at $40°$ C). (b) Temperature distribution of a multicell power HBT as a function of cell location.

stage as shown in Fig. 10. At 1 W output power, the maximum chip temperature is measured to be $40°$ C above the ambient. The peak temperature of individual SiGe HBT cells varies only within $5°$ C from the center to the edge of the power HBT. The outstanding thermal characteristics of SiGe power HBTs may be attributed to the excellent thermal conductivity of the silicon substrate and the use of base ballasting resistors in power transistor design.

The ruggedness of SiGe power amplifiers is tested by deliberately mismatching the output port. Power amplifiers are first adjusted to their maximum output levels for both CDMA and AMPS operations. We then replace the 50-Ω load by connecting the output port to a load tuner. By tuning the output load impedance, we can test the power-amplifier robustness under severe mismatch conditions. Under a high standing-wave ratio of VSWR $>12:1$, we find that SiGe

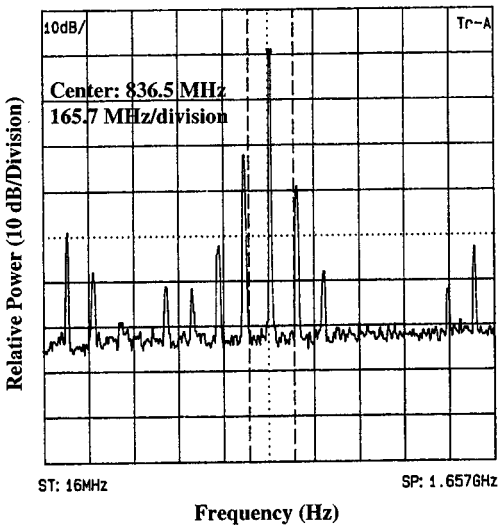


Fig. 11. (a) Low spurs (< -22 dBc) appeared at only two specific tuning angles in CDMA output (at 28 dBm). (b) No spur appeared at the rest of tuning angles in CDMA output (at 28 dBm)

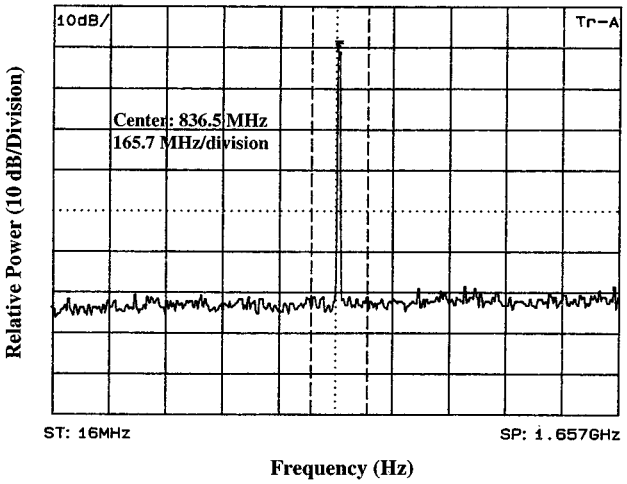


Fig. 12. No spur observed at any angle in AMPS output (at 31 dBm).

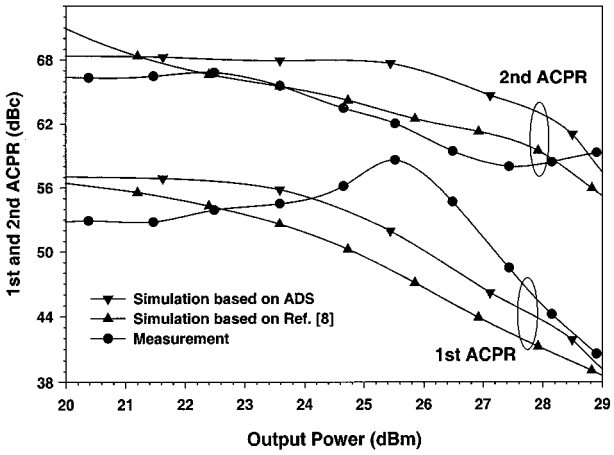


Fig. 13. Comparison between the simulated and measured first and second ACPRs versus output power at $V_{cc} = 2.7$ V for CDMA operation at 840 MHz.

power amplifiers survive well at all tuning angles up to $V_{cc} = 4.0$ V, but die instantly as $V_{cc} > 4.5$ V. The worst spurs observed in CDMA outputs are about -22 dB below the output signal level, at two specific tuning angles [Fig. 11(a)]. However, no spur is observed at the rest of tuning angles in CDMA output [Fig. 11(b)]. There is also no spur observed in AMPS output at any tuning angle (Fig. 12), even without a spur-suppression circuit configuration.

IV. Discussion

Fig. 13 compares simulated and measured results of first and second ACPRs versus the output power at $V_{cc} = 2.7$ V. Two simulators are used for ACPR evaluation. One is HP-ADS based on the envelope modulation analysis and the other is a time-domain ACPR-calculator developed by the authors based on a bandpass nonlinearity algorithm proposed by Chen and coworkers [11]. Based on this algorithm, large-signal S-parameters of the power HBT are calculated by using a SPICE model provided by the foundry vendor. AM–AM and AM–PM distortions, obtained directly from variations of S_{21} in magnitude and phase, are multiplied into the complex CDMA input waveform (generated by a Rohde and Schwarz WinIQSIM software) to produce the final power amplifier output. As shown in Fig. 13, simulated ACPRs agree well with measured ones within 5 dB in the most critical output power region (around 28 dBm). The small discrepancy in simulation is caused by assigning fixed large-signal S-parameters to a nonlinear device, which in reality vary according to operating frequency, power, and external circuit configurations for harmonic terminations. The power amplifier is also not a memoryless system as assumed in [11]. Nevertheless, the time-domain ACPR calculator has made a faster and reasonably accurate prediction of the amplifier linearity, and consequently has led to a more efficient power-amplifier design.

Fig. 14 illustrates both simulated and measured gain and PAE of the HBT power amplifier at $V_{cc} = 2.7$ V for CDMA and AMPS operations. The gain and PAE are simulated by

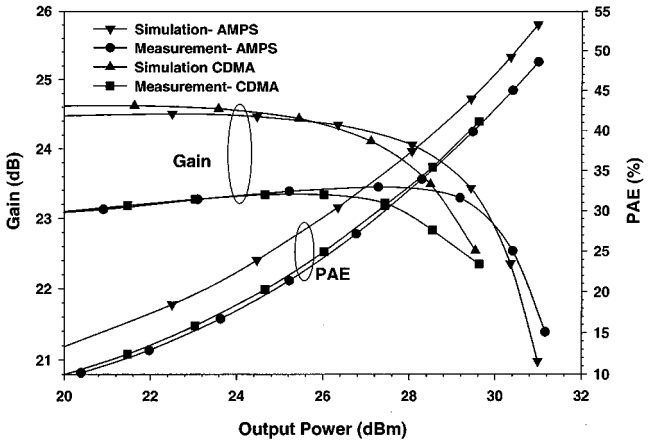


Fig. 14. Comparison between the simulated and measured amplifier gain and PAE versus output power at $V_{cc} = 2.7$ V for CDMA and AMPS operations at 840 MHz.

HP-ADS according to envelope modulation and harmonic balance analyses. The measured transducer gain is 1.5 dB lower than the simulated. The measured PAE is at most 5% lower than that of simulation. The discrepancies in gain and PAE may be attributed to imperfect circuit modeling and matchings of HBTs at high frequencies.

We have been conservative in selecting power amplifier architecture and components to warrant the first-time design success, which inevitably sacrifices the HBT power-amplifier performance. With more experience in thermal management and using better device modeling, we may further improve the power-amplifier performance at lower collector-supply voltages (< 2.7 V).

V. Conclusion

We have successfully designed and characterized a 3-V monolithic dual-mode (CDMA/AMPS) power amplifier IC on silicon substrate based on a standard SiGe/Si HBT foundry technology. The dual mode power amplifier meets all linearity and output power requirements down to 2.7 V with an outstanding performance that is comparable to that of GaAs HBTs. We are in the process to further optimize the power amplifier performance at lower collector-supply voltages (< 2.7 V) by using more accurate large signal device modeling at high frequencies.

Acknowledgment

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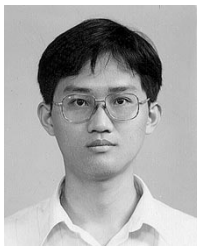

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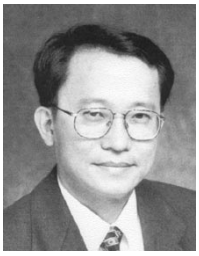
Dr. Gao was awarded the title of Distinguished National Scientist of China in 1986, and received the National Invention Prizes from the Science and Technology Committee of China in 1983 and 1984. He received the Science and Technology Prizes ten times from the Beijing Science and Technology Committee and the Ministry of Electronic Industry from 1979 to 1988, and the Best Paper Awards from the Beijing and Chinese Institute of Electronics in 1980, 1986, 1987, and 1989 in recognition of his distinguished contributions to power transistors and semiconductor device reliability.



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Dr. Chang was honored with Rockwell's Leonardo Da Vinci (Engineer of the Year) Award in 1992, the Chinese Computer Association's Outstanding Academic Achievement Award in 1994, and National Chiao-Tung University's Outstanding Alumnus Award in 1997. Currently, he is a Co-Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES (in compound semiconductor devices). He served as a Guest Editor for the Special Issue on GaAs Integrated Circuits of IEEE JOURNAL OF SOLID-STATE CIRCUITS in 1991 and 1992. He was named an IEEE Fellow in 1996 for his pioneering work in HBT processing technology for manufacturing HBT integrated circuits.