Dynamic Stack-Controlled CMOS RF Power Amplifier for Wideband Envelope Tracking

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***Abstract*—In this paper, a dynamic stack-controlled CMOS FET RF power amplifier (PA) is developed to enhance the efficiency of the envelope tracking power amplifier (ET PA) system for low-voltage operation. The power cell used in the two-stage PA is a quadruple-stacked FET structure with dynamic stacking controller to reconfigure the power cell into the quasi-triple or quasi-double stacks according to the magnitude of the input envelope signal. The proposed power cell boosts the peak efficiency in the low $V_{\rm DD}$ region by bypassing the stack entering the triode region and reoptimizing the load impedance so that all the FETs operate under the saturation and the optimum load conditions. A detailed analysis is presented to understand the gain and phase step discontinuities at the stack switching points, and the circuit techniques to equalize the gain and phase between the adjacent stack configurations are developed. The proposed two-stage stack-controlled PA is fabricated with a 0.32-μm silicon-on-insulator (SOI) CMOS process together with the envelope amplifier (EA). Full long-term evolution (LTE) characterization is performed using LTE signals with a peak-to-average power ratio (PAPR) of 6.7 dB and signal bandwidths (BW) of 10 and 20 MHz. With 10-MHz signals, dynamic stacking provides 3.5% power added efficiency (PAE) improvement over the static stack at 25.7 dBm, resulting in 47.5% PAE with 26.6-dB gain. A 20-MHz LTE test shows an overall PAE of 45.9% with an evolved universal terrestrial radio access (E-UTRA) adjacent channel leakage ratio (ACLR) of -33 dBc with memoryless digital predistortion. Even with the lower efficiency of the EA compared with the state-of-the-art results, the measured overall system efficiency with 3.4 V maximum voltage is comparable with those reported using GaAs HBT's with 5 V supplies, which clearly demonstrates the advantages of the proposed dynamic stack control.**

***Index Terms*—CMOS, dynamic stacking, envelope tracking (ET), long-term evolution (LTE), power amplifier (PA), wideband.**

I. Introduction

As THE communication era is evolved from third-generation wideband code division multiple access (3G W-CDMA) to fourth-generation long-term evolution (4G LTE), the demand for highly efficient power amplifiers (PAs) for mobile phones increases to extend the battery life. However, designing a highly efficient PA for LTE is a challenging work due to a high peak-to-average-power ratio (PAPR) of the modern modulation scheme and the stringent linearity requirements.

To overcome this problem, various efficiency enhancement techniques have been investigated so far, including Doherty PA, out-phasing PA, digital mode PA, and so on [1]–[3]. However, each configuration has its own disadvantages respectively. For example, although the authors in [1] demonstrated a high power added efficiency (PAE) of 43.6% using a CMOS Doherty amplifier with good linearity, they used a bulky $\lambda/4$ transformer in the output matching network, which restricts the RF bandwidth of the amplifier. Likewise, out-phasing PA suffers from the similar problems due to the reactive compensation components inside the power combiner [2]. The maximum continuous wave (CW) output power of the digital mode PA is limited to 25 dBm [3].

An envelope tracking PA (ET PA) has been given much attraction because of its superior efficiency performance, in particular, for high PAPR signals such as LTE [4]–[16]. Because the overall efficiency of ET PA is a weighted product of the efficiency of the envelope amplifier (EA) and RF PA, both components should be optimized to deliver the best system efficiency. To address the efficiency enhancement of the EAs, a number of papers have recently been published. For example, Hassan *et al.*, demonstrated excellent 48% overall PAE ET PA using 83% efficiency dual-switching EA in [4]. Likewise, an ac-coupled multilevel regulator is introduced in [5], resulting in 86% EA efficiency. Moreover, the potential for a single ET PA to cover broad RF bandwidth (BW) has been demonstrated in [6].

ET PAs for mobile phones have been recently demonstrated using GaAs HBTs and BiCMOS transistors, showing very high overall system efficiencies [4], [7], [8]. Most of these works employed advances in the EA design and used a 5 V voltage drive, which requires a separate boost dc–dc converter to work in a mobile phone with 3.7 V nominal battery. CMOS-based ET PA has also been demonstrated with a 5 V maximum supply using the thick-gate oxide FETs in the cascode FETs [9]. However, the efficiency was not as high as GaAs counterparts. Considering the breakdown voltage limitation of CMOS devices and the battery voltage requirement from mobile phones, it is preferred to develop a CMOS ET PA for 3.4 V maximum supply operation. However, a relatively large knee voltage in CMOS and the limitation of FET stacking limit RF PA performance.

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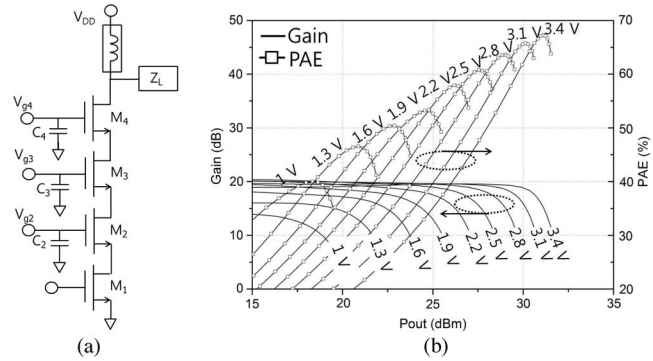

Fig. 1. (a) Schematic of the quadruple-stack power cell. (b) Simulated CW gain and PAE as the drain biases are swept from 1 to 3.4 V in 0.3 V steps.

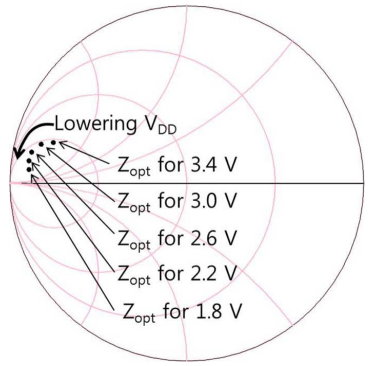

Fig. 2. Simulated optimum load impedance ($Z_{\rm opt}$) of the quadruple-stack power cell as a function of $V_{\rm DD}$.

In this paper, low-voltage operation of stacked CMOS ET PA is demonstrated using a new concept of dynamic stack control. A two-stage dynamic stack-controlled ET PA operating with 3.4 V maximum voltage maintains high efficiencies down to 5-dB backed-off power region, and shows overall PAE higher than 47% for a 10-MHz LTE signal with 6.7-dB PAPR.

This paper is organized as follows. Section II presents the operation principle of dynamic stack control as well as the detailed analysis to solve the potential linearity issues arising from the dynamic stack control. In Section III, the detailed circuit design of the two-stage RF PA using silicon-on-insulator (SOI) CMOS process is explained together with the design of the envelope amplifier implemented using the same process. The measurement results are shown in Section IV, which includes CW data, dynamic AM–AM/AM–PM data, as well as full LTE characterization data using both 10- and 20-MHz bandwidth LTE signals.

II. Operation Principle of the Proposed Power Cell

A. Dynamic FET Stack Control

Fig. 1(a) shows the circuit schematic of a single-stage quadruple-stack power cell, and the simulated CW gain and PAE are plotted in Fig. 1(b) as the drain biases ($V_{\rm DD}$) are swept from 1 to 3.4 V in 0.3 V steps. The peak PAE gradually decreases as the $V_{\rm DD}$ is lowered, which results in the degraded overall system efficiency of 3G/4G ET PAs because most of the power is concentrated in $5 \sim 6$ dB backed-off power levels from the maximum output power for modern communication schemes, such as LTE.

The lowering of the peak PAEs at lower $V_{\rm DD}$ is attributed to the nonoptimal load impedance as $V_{\rm DD}$ is lowered [17]. Fig. 2 shows the optimum load impedance ($Z_{\rm opt}$) for PAE, calculated from the load-pull simulation of the quadruple-stack CMOS FET cell as $V_{\rm DD}$ is reduced from 3.4 to 1.8 V in 0.4 V steps. $Z_{\rm opt}$ is $6.1 + j7.3\Omega$ at $V_{\rm DD} = 3.4$ V, which is the predetermined impedance that the PA load matching circuit is designed for. As $V_{\rm DD}$ is lowered, $Z_{\rm opt}$ moves counterclockwise roughly along the constant-G circle due to the sharp increase of junction capacitance in the knee region, which results in severe PAE degradation at low voltages. A similar problem can also happen in GaAs HBTs. However, the problem is much more serious in CMOS FETs due to its stacked cell structure and relatively large knee voltage region. Also, ET PAs using GaAs HBTs often employ the boost converter to crank up the voltage levels up to 5–6 V [10], which is not effective for CMOS FETs due to the low breakdown voltage.

This problem can be overcome by operating each FET in the saturation region to stay away from the knee voltage, where the junction capacitance increases sharply. For example in [9] and [11], a dynamic gate bias control circuit is employed in the CG FET of the cascode PA to prevent the PA from operating in the triode region. However, the measured PAE improvement was limited to only 0.5% [9] due to the insufficient $V_{\rm DD}$ headroom. Instead, we have proposed dynamic FET stack control for effective efficiency enhancement for ET PA operation [12]. The key idea is to control the number of active FET stacks in the power cell according to the instantaneous drain voltage level, and synthesize the optimum load impedance for each stack configuration.

Fig. 3 shows the operation principle of dynamic stack control. When the drain bias is in the highest state, all four FETs are activated in the saturation region, corresponding to quadruple-stack operation in Fig. 3(a). Since all the FETs operate in the saturation region, the predetermined load impedance matches the optimum loadpull impedance, resulting in the highest peak PAE. As the drain bias is lowered [quasi-triple-stack state in Fig. 3(b)], the uppermost FET (M_4) goes into the triode region, generating load impedance mismatch. To prevent the efficiency degradation, the uppermost FET is bypassed, resulting in a quasi-triple-stack operation. In this mode, the uppermost FET does not produce any gain. Finally, when the drain bias level is further reduced [quasi-double-stack state in Fig. 3(c)], M_3 also operates into the triode region. To avoid the efficiency degradation, M_3 is also bypassed on top of M_4, resulting in a quasi-double stack operation.

For optimum efficiency operation, the PA should be designed carefully to satisfy two conditions. First, the proper bias has to be applied to the bypassed FET so that the ON-state resistance and the voltage across the bypassed FET are negligible. Second, the load impedance presented to the reduced stack should be adjusted to provide the optimum load impedance. To satisfy the first condition, we should determine the drain bias level to trigger FET bypassing and then, find the gate bias of the FETs to be bypassed. Based on CW simulation results using different number of stacks [similar to Fig. 1(b)], we have determined the

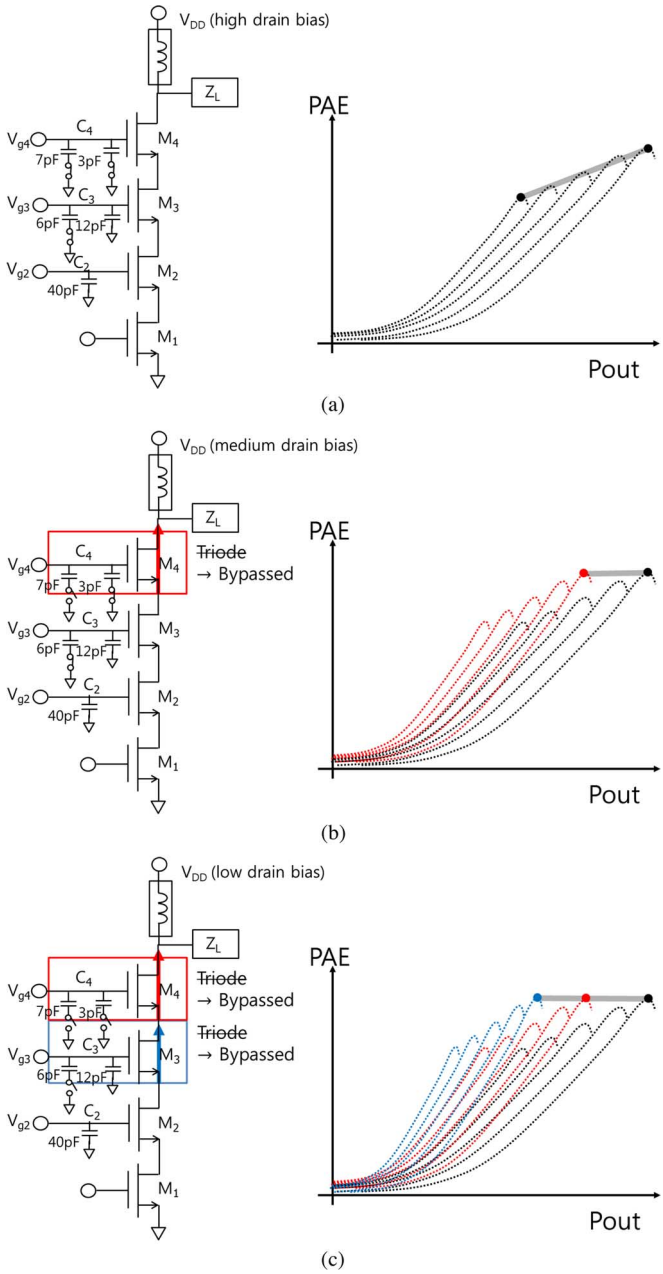

Fig. 3. Schematic and PAE trajectory of the quadruple-stacked power cell in (a) Quadruple-stack state (b) Quasi-triple-stack state (c) Quasi-double stack state.

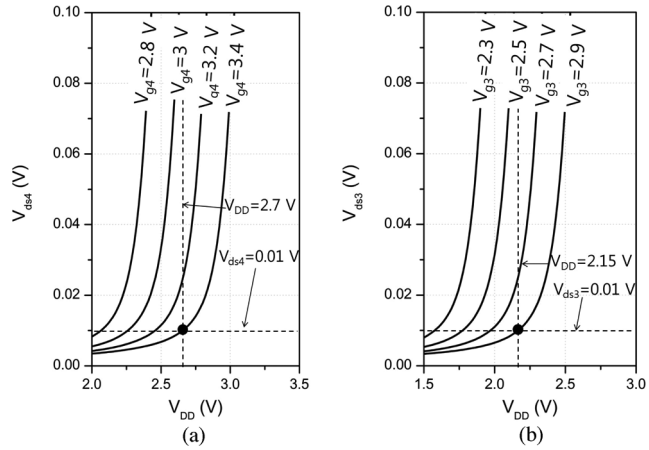

Fig. 4. Simulated voltage drop across (a) M_4 and (b) M_3 to determine the gate bias levels.

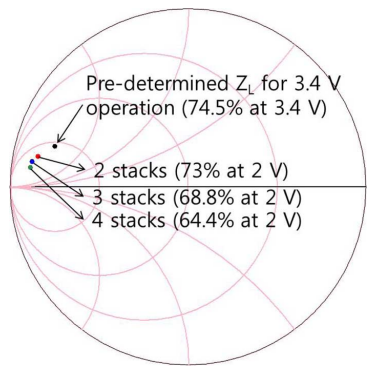

Fig. 5. Simulated $Z_{\rm opt}$ for PAE as the stack is reconfigured from quadruple to quasi-triple and to quasi-double stack. The loadpull simulation is performed at 2 V VDD.

first switching point to reduce the number of stacks from four to three is 2-dB back-off from the maximum power. The corresponding $V_{\rm DD}$ level to bypass M_4 is calculated to be 2.7 V. The gate bias to the M_4 (V_{g4}) is then determined based on the voltage drop requirement across M_4 (V_{ds4}). Fig. 4(a) shows the calculated V_{ds4} as a function of $V_{\rm DD}$ with various V_{g4}. If we set the maximum allowable voltage drop of M_4 at 0.01 V, V_{g4} should be higher than 3.4 V. Following the same logic, the second switching power is determined to be 4-dB back-off from the maximum power, which corresponds to the second $V_{\rm DD}$ switching point of 2.15 V. Based on the dc simulation results for M_3 shown in Fig. 4(b), the gate bias to M_3 (V_{g3}) is determined to be 2.9 V, which guarantees less than 0.01 V voltage drop of the M_3 (V_{ds3}).

The second condition of load impedance adjustment is fulfilled by reducing the capacitance at the gate terminal of the bypassed FET. For example, the load impedance for the quasi-triple stack is adjusted by disconnecting one of the two shunt capacitors attached to the gate terminal of M_4. The total capacitance at the gate terminal of M_4 (C_4) is reduced from 10 to 3 pF by floating 7 pF shunt capacitor using a switch as shown in Fig. 3(b). Likewise, the capacitance at the gate terminal of M_3 is reduced from 18 to 12 pF while the remaining capacitance at the gate terminal of M_4 is totally floated from the ground when M_3 is bypassed for quasi-double stack operation. The actual capacitance ratio for C_4 and C_3 are determined based on the gain discontinuity analysis, which is explained in the next section.

The load-pull simulation is performed using the proposed dynamic power cell to verify the efficiency enhancement. Fig. 5 shows the optimum load point ($Z_{\rm opt}$) in reference to the predetermined load impedance (Z_L) of $6.1 + j7.3\Omega$ as the number of the stack is reduced from 4 to 2. The drain bias used for this simulation is 2 V, which corresponds to the average bias for 6.7-dB PAPR LTE signal. It can be found from Fig. 5 that the optimum load impedance moves toward the predetermined Z_L as we decrease the number of the stacks. As a result, the efficiency at the predetermined Z_L increases from 45.5% in the quadruple stack to 55.4% in the quasi-triple stack, and finally reaches 62.3% in the quasi-double stack, even at a low $V_{\rm DD}$ of 2 V.

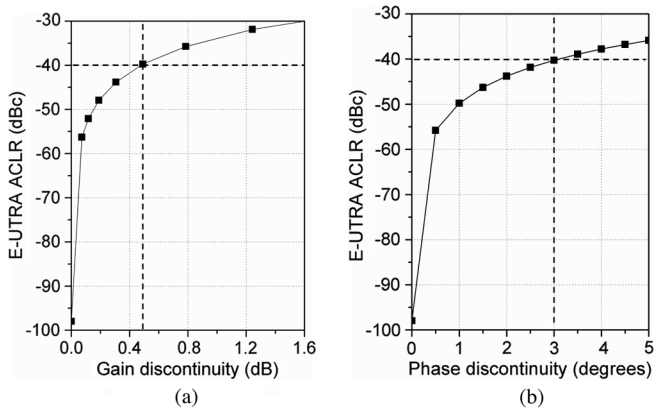

Fig. 6. Simulated E-UTRA ACLR as a function of (a) gain and (b) phase step discontinuity. The input signal is a 20-MHz BW 6.7-dB PAPR LTE signal.

B. Gain and Phase Step Discontinuities

When the capacitors at the gate of CG FETs, M_3 and M_4, are switched in and out dynamically, there can be abrupt step discontinuities in gain and phase. Fig. 6 shows the simulated evolved universal terrestrial radio access adjacent channel leakage ratios (E-UTRA ACLRs) when various levels of AM and PM discontinuities are introduced. The signal used in the simulation is a 20-MHz BW, 6.7-dB PAPR, QPSK LTE signal. To show the effect most effectively, the discontinuities are introduced in the highest probability power levels ($\sim$ 6-dB back off). From these figures, it can be concluded that one should avoid the gain step larger than 0.45 dB and phase step larger than 3° to meet -40 dBc criteria. Gain and phase discontinuities should be compensated in the analog domain since digital methods such as memoryless digital predistortion cannot correct for the abrupt discontinuities.

To this end, we have performed analytical analysis to derive the gain and phase discontinuities as the number of FET stacks is reduced using the simplified equivalent circuit of Fig. 7(a). It is simplified from Fig. 3(a) by assuming that all the FETs operate in the saturation region so that $R_{\rm ds}$ may be assumed large enough, and $C_{\rm gd}$ and $C_{\rm ds}$ small enough to be ignored [18]. Through KCL node equations, the following voltage transfer function is derived:

$$A_{v,Q} = \frac{g_{m1}Z_L}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)\left(1+\frac{j\omega C_{gs3}}{g_{m3}}\right)\left(1+\frac{j\omega C_{gs4}}{g_{m4}}\right)}. \quad (1)$$

The subscript Q in $A_{v,Q}$ represents quadruple-stack operation. This result is identical to that derived in [19], and can be used to derive the gain and phase discontinuity. If we assume that the size of each CG and CS FET is identical (i.e., $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$, and $C_{gs1} = C_{gs2} = C_{gs3} = C_{gs4} = C_{gs}$), then (1) can be simplified as follows:

$$A_{v,Q} \cong \frac{g_m(r_L + jx_L)}{\left(1+\frac{j\omega C_{gs}}{g_m}\right)^3}. \quad (2)$$

where r_L and x_L are real and imaginary part of Z_L, respectively.

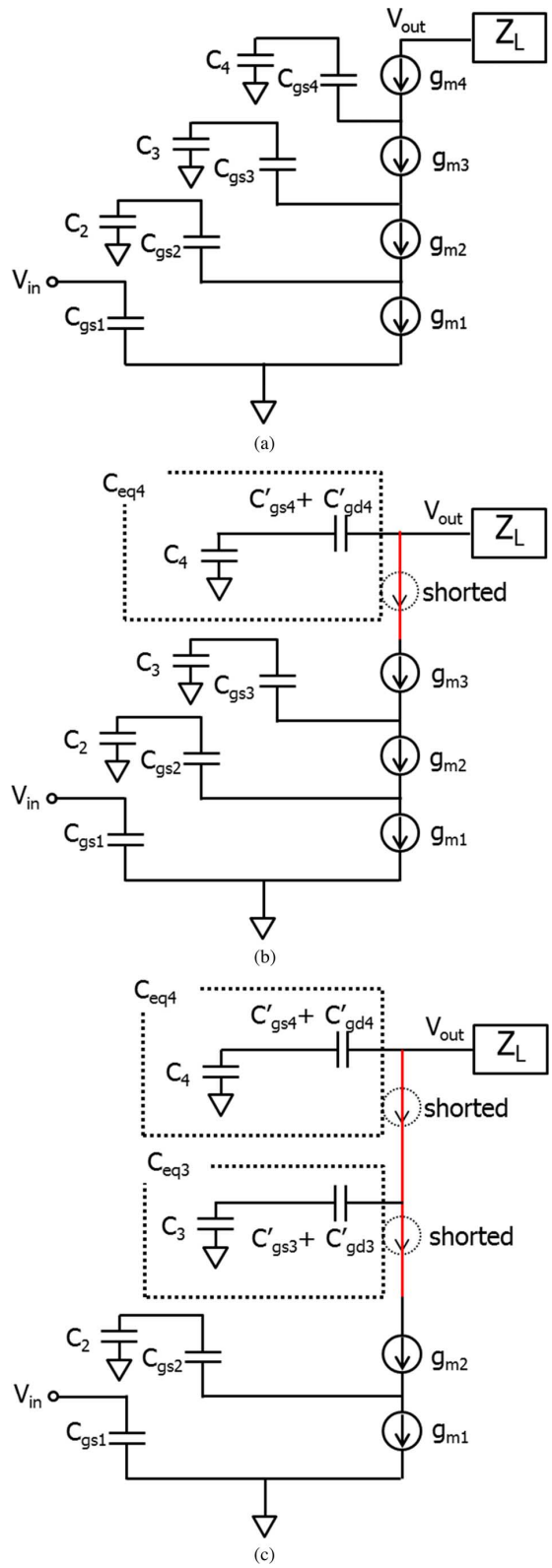

Fig. 7. Simplified equivalent circuit model of the power cell. (a) Quadruple-stack operation. (b) Quasi-triple-stack operation. (c) Quasi-double stack operation.

When M_4 is bypassed for quasi-triple-stack operation, the equivalent circuit of the power cell reduces to that shown in Fig. 7(b). The transfer function in this mode can be easily

derived from (1) by replacing $Z_L/(1+j\omega C_{gs4}/g_{m4})$ with $Z_L \| (1/j\omega C_{eq4})$ as

$$A_{v,T} = \frac{g_{m1}Z_L}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)\left(1+\frac{j\omega C_{gs3}}{g_{m3}}\right)(1+j\omega C_{eq4}Z_L)} \cong \frac{g_m(r_L+jx_L)}{(1-\omega x_L C_{eq4})\left(1+\frac{j\omega C_{gs}}{g_m}\right)^2\left(1+\frac{j\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right)} \tag{3}$$

where C_{eq4} is the total capacitance at the gate of M_4 ($C_{eq4} = (C'_{gs4}C_4 + C'_{gd4}C_4)/(C'_{gs4} + C'_{gd4} + C_4)$). The subscript T in $A_{v,T}$ represents the quasi-triple stack. Likewise, the transfer function of the quasi-double stacked state is

$$A_{v,D} = \frac{g_{m1}Z_L}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)(1+j\omega C_{eq3}Z_L)(1+j\omega C_{eq4}Z_L)} \cong \frac{g_m(r_L+jx_L)}{(1-\omega x_L C_{eq3})(1-\omega x_L C_{eq4})\left(1+\frac{j\omega C_{gs}}{g_m}\right)} \times \frac{1}{\left(1+\frac{j\omega r_L C_{eq3}}{1-\omega x_L C_{eq3}}\right)\left(1+\frac{j\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right)} \tag{4}$$

where C_{eq3} is the total capacitance at the gate of M_3 ($C_{eq3} = (C'_{\mathrm{gs3}}C_3 + C'_{gd3}C_3)/(C'_{gs3}C_3 + C'_{gd3} + C_3)$). Again, the subscript D in $A_{v,D}$ denotes quasi-double stack. From (3) and (4), it can be seen that the gain is a function of C_3 and C_4 in the double- and triple-stacked operation. Therefore, one can minimize gain and phase step discontinuity at the switching points by carefully determining the values of C_3 and C_4.

The magnitude of the voltage gain at each state can be easily derived from (2), (3), and (4) by assuming $\omega C_{gs} \ll 1$, and the results are

$$|A_{v,Q}| \cong g_m\sqrt{r_L^2 + x_L^2} \tag{5}$$

$$|A_{v,T}| \cong \frac{|A_{V,Q}|}{\sqrt{(\omega r_L C_{eq4})^2 + (1-\omega x_L C_{eq4})^2}} \tag{6}$$

$$|A_{v,D}| \cong \frac{|A_{V,T}|}{\sqrt{(\omega r_L C_{eq3})^2 + (1-\omega x_L C_{eq3})^2}}. \tag{7}$$

To minimize the gain step during the dynamic switching of M_4, we need to understand the dependence of the gain step between $|A_{V,T}|$ and $|A_{V,Q}|$ on C_4 under various load impedance conditions. Fig. 8 shows $|A_{V,T}|$ normalized to $|A_{V,Q}|$ as a function of C_4. For this simulation, the frequency is 0.837 GHz, r_L is fixed at 5Ω, $C_{gd4} + C_{gs4}$ is 15 pF while x_L is swept from 0 to 1Ω in 0.25Ω steps. When $x_L = 0\Omega$, there is no chance to equalize the gain due to M_4 switching. This means that conventional PAs such as Class AB PAs cannot support proposed dynamic switching scheme. However, since most of the high-efficiency PAs utilize finite reactance for waveform shaping as in the case of Class-F and Class-J, this does not pose any practical issues. As x_L is increased, the normalized gain shows a peak higher than 1 at a certain C_4, which means that there are potentially two C_4 values at which the gain step vanishes. Moreover, by proper selection of x_L such as $x_L = 0.5\Omega$, we can obtain almost flat gain response regardless of C_4. The choice of x_L is thus a trade-off between the efficiency and the linearity. In this work, we have chosen x_L of 2.7Ω to achieve almost no gain step while compromising the efficiency by 2.2%. The gain step discontinuity between quasi-triple and quasi-double stacks is also minimized following the same method.

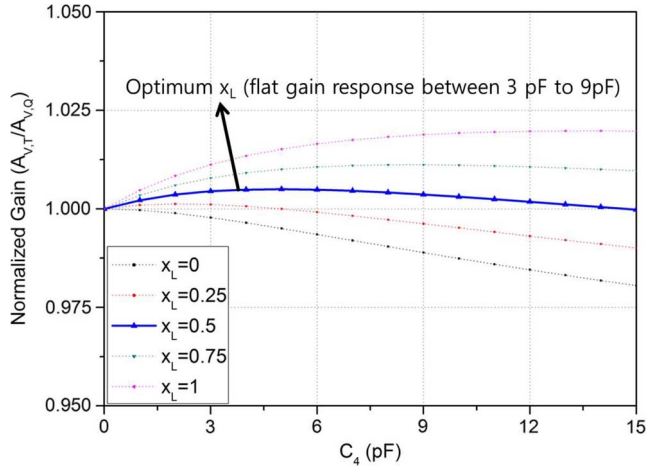

Fig. 8. The gain ratio between the quadruple stack and quasi-triple stack as a function of the capacitance at the gate terminal of M_4 (C_4) for different reactance of the load impedance.

The phase of the voltage transfer function at each stack operation is derived using (2), (3), and (4) as follows:

$$\angle A_{v,Q} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - 3\tan^{-1}\left(\frac{\omega C_{gs}}{g_m}\right) \tag{8}$$

$$\angle A_{v,T} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - \tan^{-1}\left(\frac{\omega C_{gs}}{g_m}\right) - \tan^{-1}\left(\frac{\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right) \tag{9}$$

$$\angle A_{v,D} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - \tan^{-1}\left(\frac{\omega C_{gs}}{g_m}\right) - \tan^{-1}\left(\frac{\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right) - \tan^{-1}\left(\frac{\omega r_L C_{eq3}}{1-\omega x_L C_{eq3}}\right). \tag{10}$$

It can be found from (9) that changing the gate capacitance by partially floating C_4 during stack switching will cause abrupt phase discontinuity. The amount of phase discontinuity during the M_4 switching is

$$\triangle\angle A_{V,T} = -\tan^{-1}\left(\frac{\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right) + \tan^{-1}\left(\frac{\omega r_L C'_{eq4}}{1-\omega x_L C'_{eq4}}\right) \tag{11}$$

where C'_{eq4} is equivalent gate terminal capacitance of the M_4 after a portion of C_4 is disconnected from the ground. Because ωC_{eq4} is much lower than unity in most cases, we can use $\tan^{-1} x \cong x$ approximation to simplify (11) as

$$\triangle\angle A_{V,T} \cong \tan^{-1}\left(\omega r_L(C'_{eq4} - C_{eq4})\right). \tag{12}$$

Likewise, the step discontinuity in quasi double state can be derived in the same way by using (10):

$$\triangle\angle A_{V,D} \cong \tan^{-1}\left(\omega r_L(C'_{eq3} - C_{eq3} - C'_{eq4})\right). \tag{13}$$

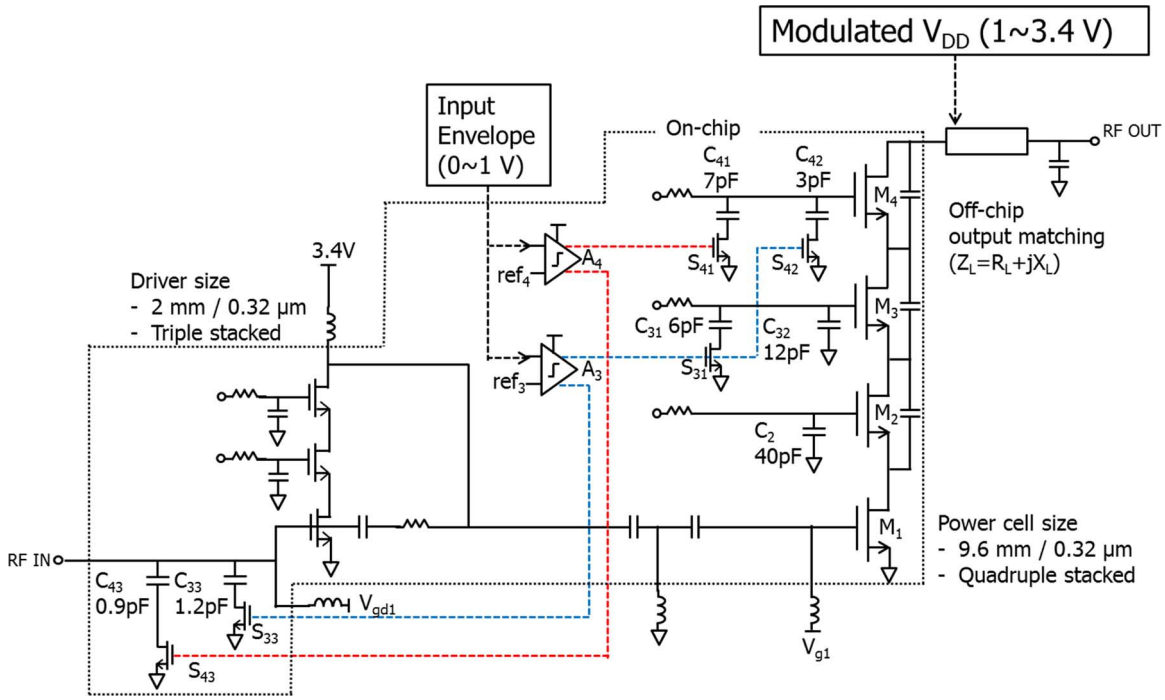

Fig. 9. Detailed circuit schematic of the entire two-stage RF PA with dynamic stack control circuits.

The phase step discontinuity during M_4 switching is calculated to be $-5.26°$ using (12) while that during M_3 switching is $-6°$ using (13).

The phase step discontinuity is compensated in this work by changing the shunt capacitance in the input matching network instead of changing the capacitance of the load matching network since the latter results in the degradation in the overall PA efficiencies. The detailed circuit design is presented in the next section.

III. Design and Implementation

A. Power Amplifier Design

Fig. 9 is the complete circuit schematic of the proposed two-stage RF PA. The unit FET size in the power cell is 9.6 mm, and that of the driver stage is 2 mm. Miller capacitors are inserted between the drain and source node of CG FET in the power cell to provide appropriate second harmonic termination [6], [20]. Two comparators, A_3 and A_4, turn on and off the switches, S_{41}, S_{42}, and S_{31}, to change the total capacitance loading at the gate terminals of M_3 and M_4. The FET size used for S_{41}, and S_{42} is designed to be 1 mm. That for S_{31} is 0.5 mm, considering ON-state resistance and OFF-state capacitance. Instead of using the minimum gate length of 0.32 μm allowed by the foundry process, the gate length of S_{41} and S_{42} is extended to $1.4-\mu$m while that of S_{31} to $0.8-\mu$m to avoid the device breakdown due to large voltage swing. For phase step compensation, two additional switches, S_{43} and S_{33}, are used in the input matching circuit. When these switches are turned on, the input matching circuit presents additional phase delay to compensate for the phase discontinuity at the stack switching points. The transistors used for these input switches have the gate width of 0.1 mm and the gate length of $0.8-\mu$m.

The proposed RF PA takes two input signals, the modulated RF input signal and the envelope signal itself. The magnitude of the input envelope signal mirrors that of the dynamic drain bias, since it is the same one used to generate the modulated drain bias by the ET modulator. When the magnitude of the input envelope is in its highest state, namely greater than ref_4, two comparators (A_4 and A_3) turn on all the switches, S_{41}, S_{42}, and S_{31}, to operate the power cell in the quadruple-stack mode. Two switches, S_{43} and S_{33}, in the input matching circuit are turned off to disconnect the shunt capacitors, C_{43} and C_{33}, so that no additional phase delay is provided by the input matching circuit.

When the magnitude of the input envelope falls below a certain level, which is set by the reference voltage input (ref_4) to the comparator, A_4, the power cell is reconfigured to a quasi-triple stack. In this state, A_4 turns off S_{41} and turns on S_{43}, while A_3 maintains the same state as the quadruple-stack mode. By floating C_{41}, the total capacitance loading at the gate terminal of M_4 is reduced from 10 to 3 pF, which effectively bypasses M_4 and adjusts the optimum load impedance to recover the efficiency. Besides, with S_{43} turned on, the input matching circuit is loaded with C_{43} shunt capacitor, which provides the additional phase shift to compensate for the phase step discontinuity at the switching point.

When the magnitude of the input envelope is reduced further, the power cell is reconfigured again to a quasi-double stack. In this state, the comparator A_3 turns off S_{42} and S_{31} while turning on S_{33}. The reduced total capacitance at the gate terminal of M_3 and M_4 effectively recovers the efficiency. In this way, optimum efficiencies can be achieved over a wide range of V_{DD}. The phase step discontinuity between quasi-triple and quasi-double stacks is compensated for by turning on the additional shunt capacitance, C_{33}, in the input matching circuit.

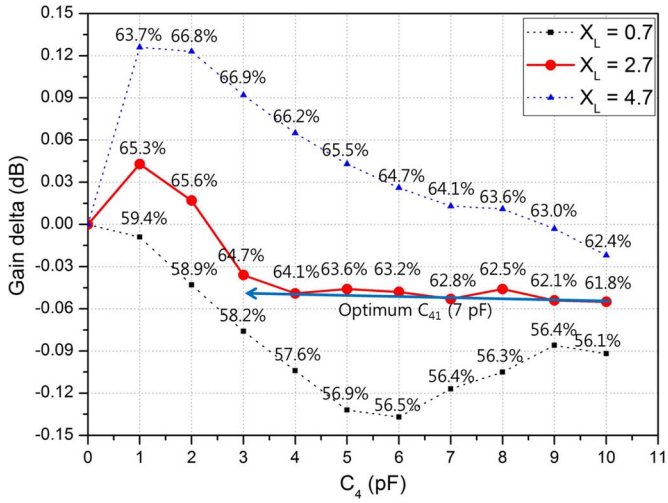

Fig. 10. Simulated gain step and drain efficiency as a function of C_4 for three different load reactance (X_L) values.

The values of the gate terminal capacitances of CG FETs (C_2, C_3, and C_4) are carefully chosen based on the analysis in the previous section. According to the simulation, 10 pF, 18 pF, and 40 pF for C_4, C_3, and C_2, respectively, provide the peak efficiency of 63% at 3.4 V drain bias while ensuring safe operation avoiding voltage breakdown. The gate biases of CG FETs are supplied through a resistive divider while those of CS FETs are applied through the external chip inductor for reduced memory effect.

As explained in the previous section, the choice of reactance of the load impedance (X_L) affects not only the overall efficiency but also the gain step discontinuity in conjunction with the choice of C_4. This effect has been simulated using the harmonic balance simulation of the entire circuit. Fig. 10 shows the simulated gain step in decibel scale as a function of C_4, for three different X_L values, 0.7, 2.7, and 4.7Ω. The drain efficiency at each point is also specified in the label. The drain bias used for the simulation is 2.8 V, which corresponds to a switching reference voltage, ref_4, of the M_4. Even if the actual values are different between the simplified analysis of Fig. 8 and the complete circuit simulation of Fig. 10, the gain step curves follow the similar characteristics, showing peaky behavior as X_L is increased. Although the $X_L = 4.7\Omega$ case shows better efficiency, we have selected a lower X_L of 2.7Ω considering a flat and minimal gain step for a wide range of C_4. This load condition provides 2.9% efficiency enhancement from 61.8% to 64.7% with negligible gain step discontinuity by floating 7 pF out of total C_4 of 10 pF. A similar simulation has been performed to find the gate terminal capacitance values to minimize the gain step discontinuity when switching from quasi-triple to quasi-double stack modes at 2.2 V. The simulated phase discontinuity during M_4 switching is $-7°$ while that during M_3 switching is $-9°$. These values are in good agreement with the theoretical predictions based on (12) and (13) presented in the previous section. The capacitor values in the input matching circuit, C_{43} and C_{33}, are determined to 0.9 and 1.2 pF, respectively, which effectively compensate for the phase step discontinuity during dynamic stack switching. Switching the input matching capacitor may degrade the input return loss of the RF PA. However, the worst-case return loss of the RF PA even after phase step compensation is still better than 10 dB.

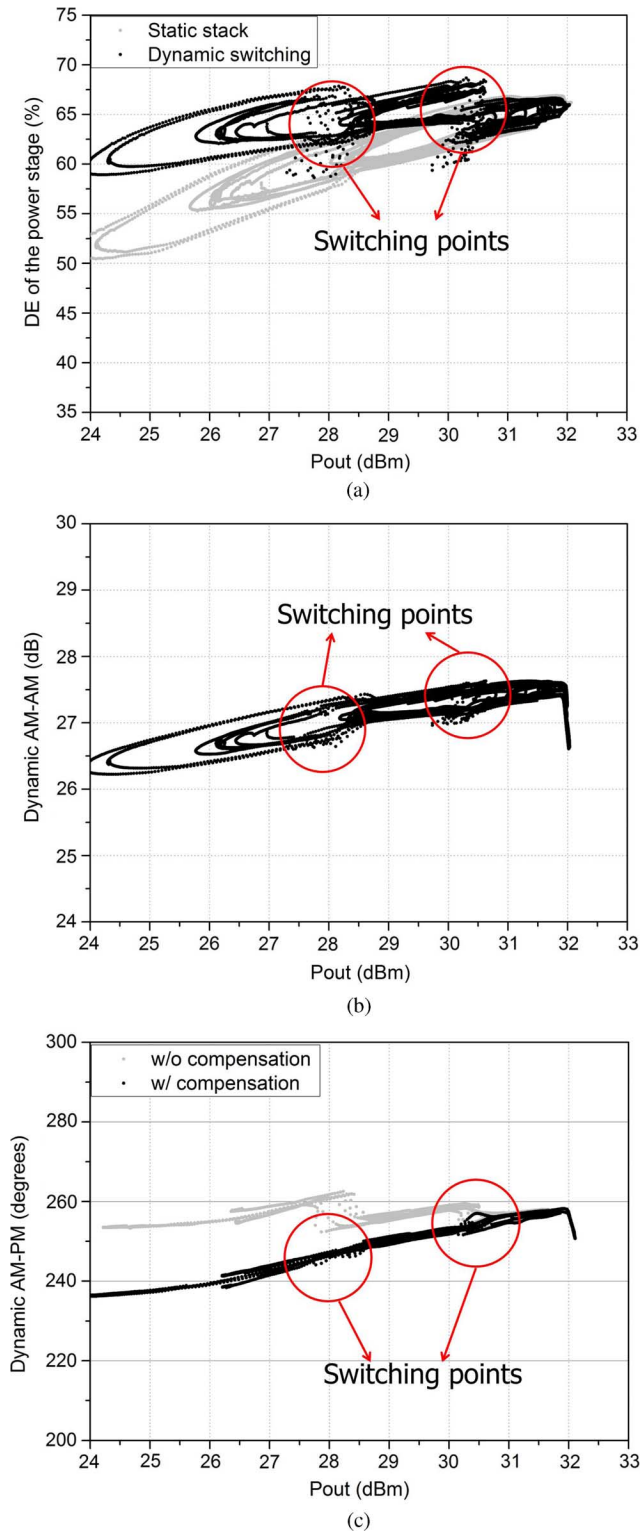

Fig. 11. Simulated dynamic characteristics of the entire ET PA. (a) Instantaneous drain efficiency of the power stage. (b) Dynamic AM–AM plot. (c) Dynamic AM–PM plot.

To verify the dynamic performance of the entire two-stage PA, envelop simulation is performed using ADS, and the results are plotted in Fig. 11. The input signals used in the simu-

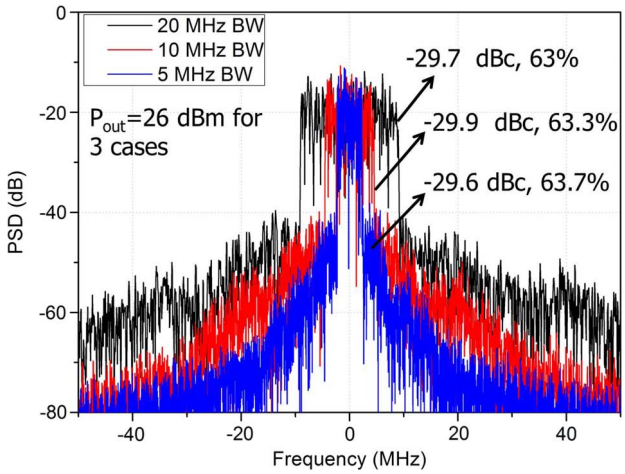

Fig. 12. Simulated output spectrum of the entire ET PA with various modulation signal bandwidths (5/10/20 MHz). No predistortion is applied for this simulation.

lation are based on W-CDMA waveform at 837 MHz, and only the drain voltage of the power stage is modulated by the envelope amplifier. Fig. 11(a) compares the instantaneous drain efficiency (DE) of the proposed dynamic stack with that of the static stack, where all four FET stacks are used across the entire $V_{\rm DD}$ range. In the dynamic stack scheme, M_4 is bypassed around the output power of 30.5 dBm while both M_3 and M_4 are bypassed around 28 dBm. Dynamic stack control provides $\sim$7% efficiency enhancement at 6-dB back-off power (32 dBm $-$ 6 dB $=$ 26 dBm). Fig. 11(b) and (c) shows the simulated dynamic AM–AM and AM–PM characteristics, the smoothness and tightness of which are critical in achieving the adequate linearity after digital predistortion. No abrupt gain and phase steps are observed near the switching points. Slightly wider dispersion is observed near the switching points, which is attributed to the capacitive feed-through of the switch control signal from the comparator. For reference, dynamic AM–PM without phase step correction is shown in Fig. 11(c) as well. It can be seen that the use of the input capacitance switching effectively compensates for the phase step discontinuity at the switching points.

To verify the circuit performance over a wide signal bandwidth, the envelope simulation is performed to calculate the output spectrum using 6.7-dB PAPR QPSK LTE signals with various signal bandwidths up to 20 MHz. No linearization using digital predistortion is used for this simulation. Calculated ACLR degradation is negligible going from 5- to 20-MHz bandwidth as shown in Fig. 12. This is due to the fact that the gain and phase steps are corrected and maintained consistently over a wide switching voltage range. It is worthwhile to note that the efficiency drops slightly as the signal bandwidth increases. This is attributed to the dynamic switching loss caused by nonzero rise/fall time of the switch control signals generated by the comparator.

B. Envelope Amplifier Design

A simple envelope amplifier is also designed using the same SOI CMOS process to demonstrate the complete ET PA system. Since the main purpose of this paper is to present the new ET PA concept not the envelope amplifier, the circuit is based on a widely used hybrid approach composed of a linear stage and switching stage [13], as shown in Fig. 13. The gate length of all the FETs, except for output NMOS FET, is 0.32 μm for standard 2.5 V I/O operations. Instead of using a cascode configuration to avoid the breakdown, the gate length of the output NMOS FETs is extended from 0.32 μm to 0.7 μm, which allows 3.4 V $V_{\rm DD}$ operation.

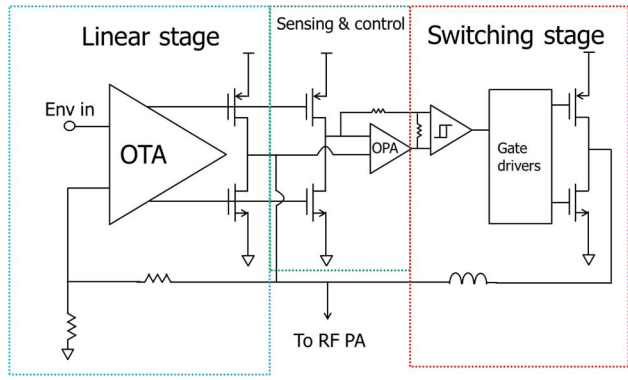

Fig. 13. Circuit schematic of the designed envelope amplifier.

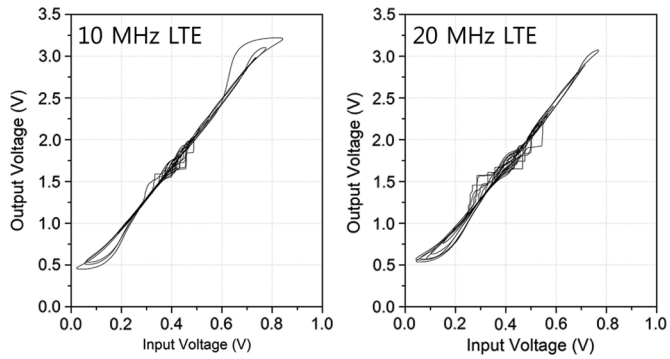

Fig. 14. Simulated input and output voltage response of the envelope amplifier using LTE signals with different signal bandwidths (10/20 MHz). More pronounced cross-over distortion is observed with a 20-MHz signal.

According to the small signal ac simulation, the open loop dc gain of the linear stage exceeds 50 dB under $8\Omega//80$ pF load condition. The unity gain bandwidth is about 250 MHz with 50° phase margin in the same load, which is sufficient for supporting 20-MHz BW LTE operation [14]. Fig. 14 is the simulated I/O voltage response using a 10- to 20-MHz QPSK envelope signal after the delay adjustment. The crossover distortion centered around the midpoint of $V_{\rm DD}$ range is observed, which can cause AM and PM dispersion in the ET PA system and degrade the linearity [21]. This effect is more pronounced as the signal bandwidth is increased, as in the case of the 20-MHz test. More sophisticated EA design is required to further improve the linearity [15]. Measured efficiency of the envelope amplifier with a fully loaded 10-MHz BW QPSK LTE envelope signal with 7.5Ω resistive load is 77% [12], which is 6–9% lower than the state-of-the-art dual-switching envelope amplifier ($\sim$83% [4], [16]), and multiple regulator ($\sim$86% [5]).

IV. Measurement Results

Both envelope amplifier and proposed RF PA are fabricated using the same 0.32-μm SOI CMOS process. Fig. 15(a) and (b)

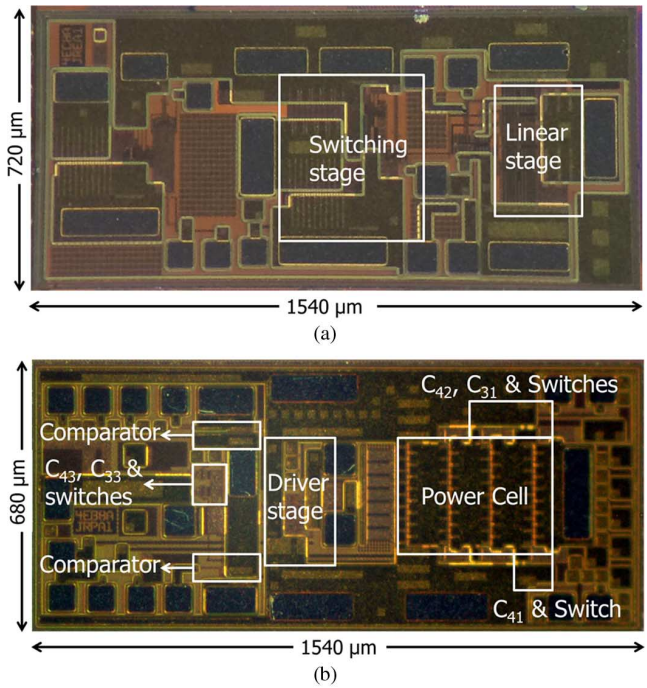

Fig. 15. Chip and test module photographs. Die photographs of (a) the envelope amplifier and (b) two-stage RF PA. (c) Photograph of the test module.

shows the chip photographs of envelope amplifier and RF PA, respectively, and Fig. 15(c) is the photograph of the evaluation board containing both chips on $5\ \text{cm} \times 5\ \text{cm}$ sized FR4 substrate. Multiple ground pads are placed to reduce the inductance of grounding wire bonds for both RF PA and EA.

Fig. 16 is a measured CW performance of the proposed two-stage RF PA with 837-MHz sinusoidal input signal by sweeping the drain bias of the power stage from 1 to 3.4 V in 0.3 V steps. The output power reaches 30.3 dBm with 64% peak PAE. The corresponding DE of the power stage is 68.5% at 3.4 V. By reducing the number of operating stacks at 2.8 V and 2.2 V, overall PAE is boosted for a wide range of V_{DD}s, showing higher than 60% PAE down to 5-dB back-off from maximum output power. Total current consumption in the comparators is less than 1 mA

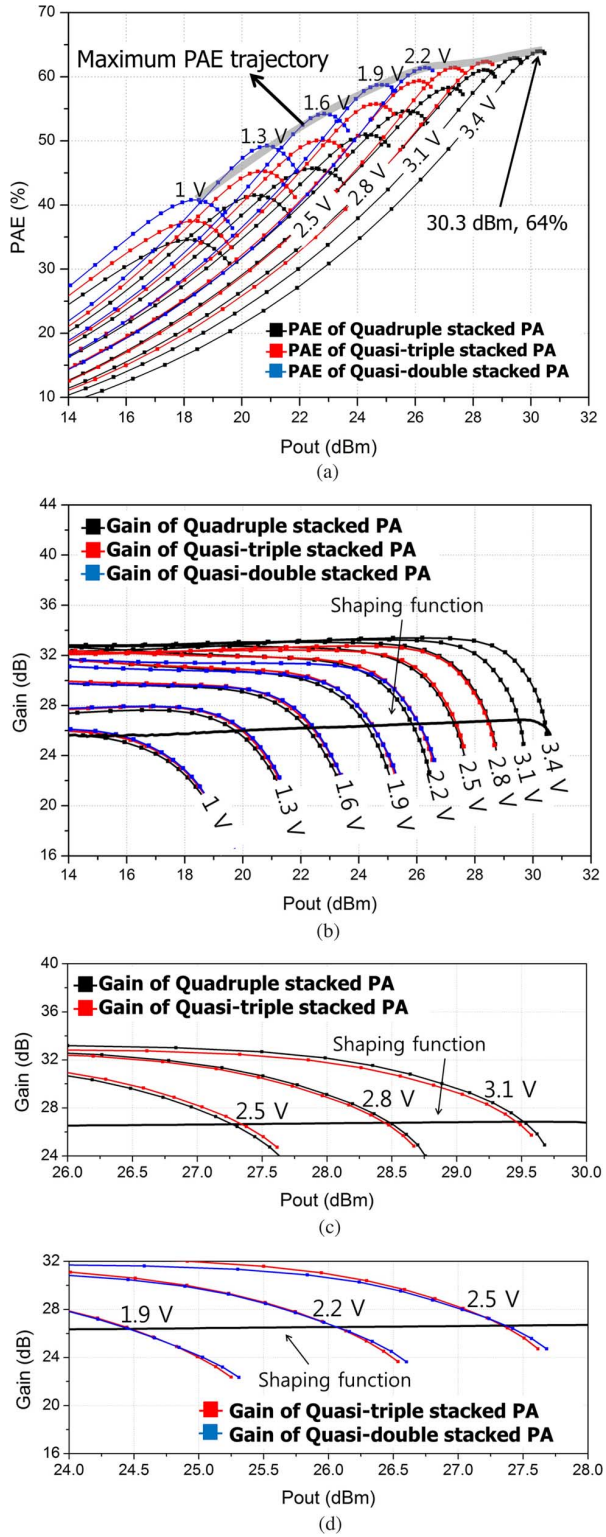

Fig. 16. Measured 837-MHz CW performance of the proposed two-stage RF PA by sweeping the drain bias from 1 to 3.4 V. (a) PAE. (b) Gain. (c) Expanded gain plot to show the gain discontinuity between the quadruple stack and quasi-triple stack. (d) Expanded gain plot to show gain discontinuity between quasi-triple stack and quasi-double stack.

with a 2.5 V supply. It can be also seen from Fig. 16(a) and (b) that the peak efficiencies occur near the same compression level for different stack configurations. For example, at 2.8 V V_{DD}, peak efficiencies for both quadruple-stack state and quasi-triple-

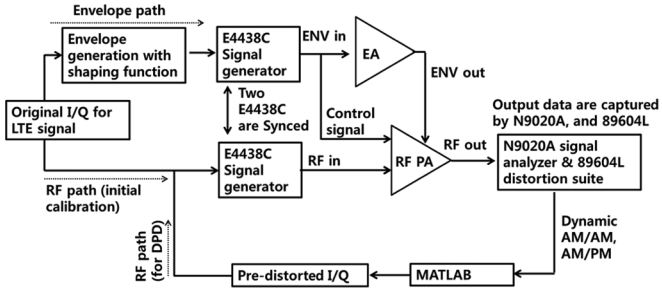

Fig. 17. Block diagram of the ET PA measurement setup.

stack state occur at P5 dB. Likewise, at 2.2 V V_{DD}, peak efficiencies for three cases occur at P4.5 dB. The details of the gain steps at the switching points are shown in Fig. 16(c) and (d). When the overall ET system tracks a predefined shaping function, the gain step discontinuity between the quadruple-stack state and quasi-triple-stack state is less than 0.08 dB for a wide range of V_{DDS} from 2.5 to 3.1 V. Likewise, the gain discontinuity between the quasi-triple-stack state and quasi-double stack state is less than 0.04 dB for a wide range of V_{DDS} from 1.9 to 2.5 V. This verifies the design methodology presented in the previous section to determine the load impedance (x_L) and the switching capacitance ratio (C_{41}:C_{42}).

Fig. 17 is a block diagram for the ET PA system test setup. A modulated RF signal is generated by up-converting the in-phase and quadrature baseband signal (I/Q), which are sampled at 245.76 MHz. The input signal to EA and the control signal to PA are generated from the same I/Q with an exponential shaping function [15] depicted in Fig. 16. These signals are then downloaded to two synchronized Agilent's E4438C signal generators. The output RF signal of the ET PA is captured by Agilent's N9020A signal analyzer, and then an 89604L distortion suite is used to measure the dynamic AM–AM and AM–PM characteristics as shown in Fig. 17. Once the output data are read from the signal analyzer, the predistorted I/Q is generated by MATLAB. Since an iso-gain shaping function is used to flatten the gain of the ET PA, the order of the polynomial used for gain predistortion is limited to 3. On the other hand, a ninth-order polynomial is employed for phase predistortion, since AM–PM distortion in the top 20-dB power range is as high as 20°. The predistorted I/Q is then downloaded back to the RF signal generator for testing with predistortion.

Fig. 18 shows the measured performance of the overall ET PA system using fully loaded LTE signals with bandwidths of 10 and 20 MHz. The QPSK-modulated LTE signal is centered at 837 MHz and shows a PAPR of 6.7 dB with 0.01% probability. The measured PAE includes the power consumption from the envelope amplifier, the driver stage, and the control circuit as well as the loss from the load matching network, whereas DE of the power stage excludes the power consumption of the driver stage. To investigate the efficiency enhancement effect of the proposed power cell, four different cases are compared: an ET PA with two dynamic stacks, an ET PA with one dynamic stack, an ET PA with static stack PA, and a non-ET PA with a fixed bias of 3.4 V. Since the peak efficiencies occur at the same compression point for all three stack configurations, it is fair to use the same shaping function to compare the

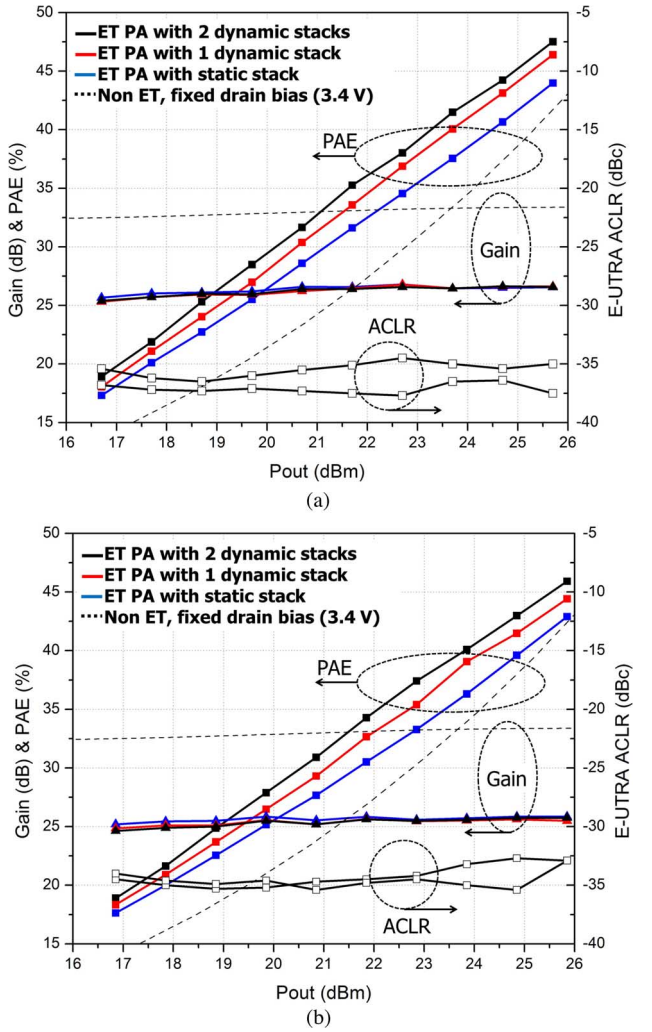

Fig. 18. Measured performance of the dynamic stack-controlled ET PA in comparison with static stack and partially stack-controlled PA using (a) 10-MHz LTE and (b) 20-MHz LTE signals. Non-ET PA data are also shown as a reference.

overall ET PA efficiency. For the 10-MHz LTE case shown in Fig. 18(a), dynamic stacking provides 3.5% PAE improvement at the maximum linear output power of 25.7 dBm, resulting in 47.5% PAE and 51.4% DE of the power stage with 26.6-dB gain. The measured E-UTRA ACLR after digital predistortion is −35 dBc, and EVM is 3.34% for two-dynamic-stack control. Both E-UTRA ACLR and EVM show sufficient margin against system requirements. The proposed ET PA is also tested using a 20-MHz LTE signal to verify wideband operation as shown in Fig. 18(b). In 20-MHz LTE testing, PAE and DE at the maximum linear output power of 25.9 dBm are 45.9% and 50.8%, respectively, with 25.8-dB gain, which is 3% higher than static-stack ET PA. The measured E-UTRA ACLR after digital predistortion is −33 dBc, and EVM is 2.81%. The degraded ACLR for the 20-MHz LTE signal is mainly attributed to the pronounced cross-over distortion of the EA with larger signal bandwidth (see Fig. 14).

The PAE gap between 10-MHz and 20-MHz LTE for two-dynamic-stack control is 1.6%, which is slightly higher than the gap of the static-stack case (1.1%). This is attributed to nonzero

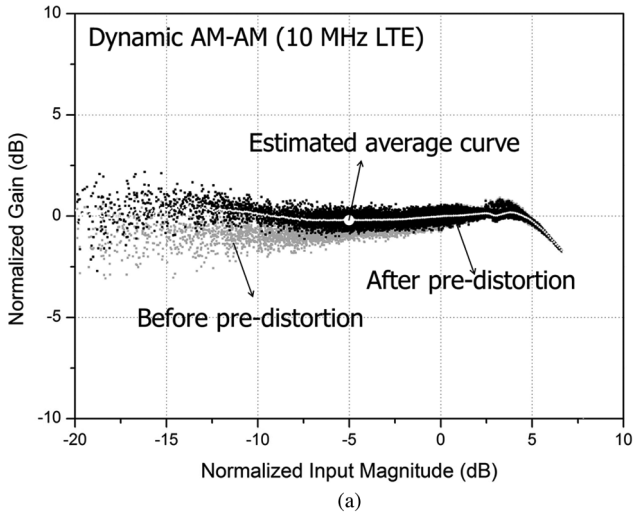

Fig. 19. Measured dynamic characteristics of the ET PA using 10-MHz LTE signal at 25.7 dBm output power. (a) Dynamic AM–AM. (b) Dynamic AM–PM.

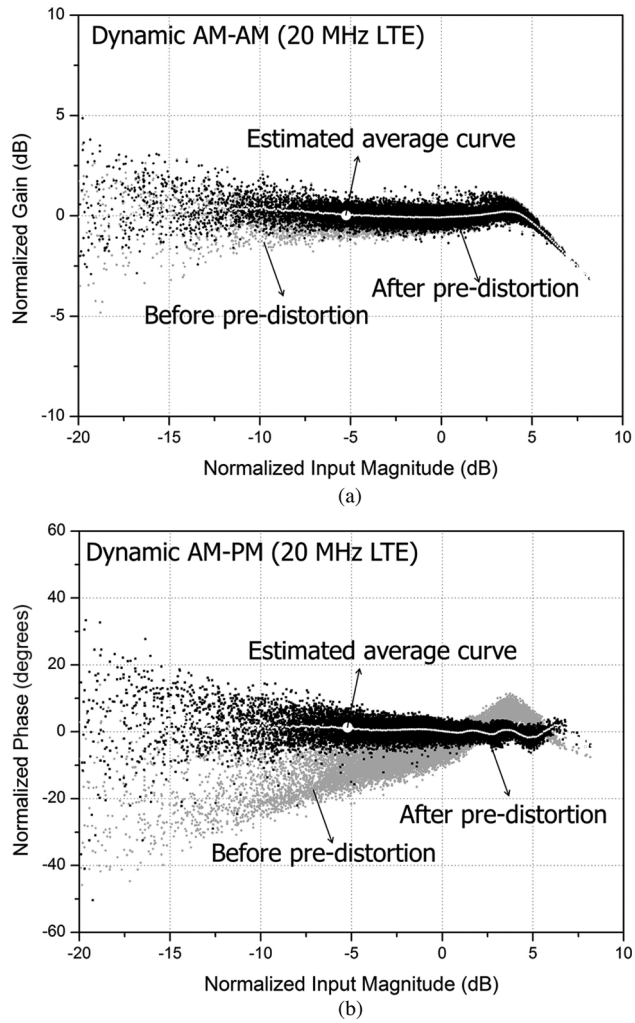

Fig. 20. Measured dynamic characteristics of the ET PA using 20-MHz LTE signal at 25.9 dBm output power. (a) Dynamic AM–AM. (b) Dynamic AM–PM.

rise/fall time of the comparator, as explained in Section III-A. This can be improved by employing a deep-submicron CMOS process for faster switching.

Further investigation of the linearity impact due to dynamic switching has been performed by measuring dynamic AM–AM/AM–PM characteristics of the ET PA after digital predistortion using 10-MHz (Fig. 19) and 20-MHz LTE (Fig. 20) signals. The curves showing the statistical average at each power level are also shown with white dots to clearly reveal the step discontinuities, if any. As shown in Fig. 19(a) and Fig. 20(a), the gain step discontinuities are contained to less than 0.1 dB for both signal bandwidths. Phase step discontinuities are effectively compensated to less than 2° for both signal bandwidths as shown in Fig. 19(b), and Fig. 20(b). Fig. 21 is the output spectrum of the entire ET PA system with 10- and 20-MHz BW LTE signals measured with a 200-MHz span. Compared with the static-stack case, the out-of-band noise increases from -131 dBm/Hz to -128.6 dBm/Hz when M_4 is switched in and out due to the additional quantization noise and dynamic effects.

Table I is a comparison table of the state-of-the-art ET PAs for a mobile LTE terminal. Without any efficiency enhancement techniques in the envelope amplifier and crest factor reduction

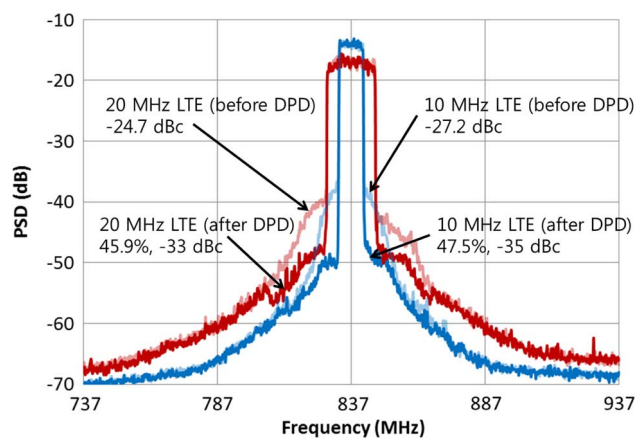

Fig. 21. Measured output power spectrum of the entire ET PA with dynamic stack control using 10-MHz and 20-MHz LTE signals.

techniques, our work shows overall system efficiencies comparable with the state-of-the-art ET PAs using dual switcher [4], [16] and ac-coupled multilevel regulators [5]. In particular, the power stage efficiency demonstrated in our work is the highest among the reported silicon-based PAs. It is also worthwhile to

TABLE I
PERFORMANCE COMPARISON TABLE OF ET PA SYSTEMS FOR MOBILE LTE TERMINALS

Reference	Frequency (GHz)	BW (MHz)	PAPR (dB)	PA Technology	P_{out} (dBm)	Overall PAE (%)	E-UTRA ACLR (dBc)	V_{DD} (V)	Output matching
[4]	2.535	20	6.7	GaAs HBT	28.3	48	–41.4	5.5	Off-chip
[5]	N/A	10	6.7	N/A	26.4	39	–37.3	3.8	N/A
[8][1]	0.7	10	7.5	0.35-μm SiGe BiCMOS	27.6	36.4 37.1[2]	N/A	5	Off-chip
	0.7	20	7.5	0.35-μm SiGe BiCMOS	27.4	35.6 36.3[2]	N/A	5	Off-chip
[9][1]	1.85	10	7.5	0.18-μm CMOS	26.5	34.1 37.9[2]	–34.2	5	Off-chip
[16][1]	0.782	10	6.6	0.35-μm SOS CMOS	29.3	50.1 50.6[2]	–46.5	N/A	Off-chip
[7]	1.71	10	7.44	GaAs HBT	28	44.3	–35.1	5	Off-chip
This Work	0.837	10	6.7	0.32-μm SOI CMOS	25.7	47.5 (44)[3] 51.4[4]	–35	3.4	Off-chip
	0.837	20	6.7	0.32-μm SOI CMOS	25.9	45.9 (42.9)[3] 50.8[4]	–33	3.4	Off-chip

[1] single stage PAs; [2] estimated DE; [3] PAE of the static stack ET PA; [4] measured DE of the power stage only

note that the PA of this work operates with a supply modulator with a maximum voltage of 3.4 V instead of 5 V as in the case of [4], [8], [9], and [10], which means that the ET PA system can be operated directly from the battery and can thus avoid the potential issues by the boost converter.

V. CONCLUSIONS

In this paper, we have developed a new concept of dynamic stack control to enhance the efficiencies of CMOS stacked FET PAs for low-voltage ET operation. The potential issues due to the dynamic stack control have been identified as the gain and phase step discontinuities, and the circuit designs to compensate for the step discontinuities are developed using the detailed circuit analysis.

A two-stage dynamic stack-controlled PA is designed and fabricated using SOI CMOS process for operation at 837 MHz. CW characterization shows that the dynamic stack-controlled PA maintains PAEs higher than 60% down to 5-dB back-off from the maximum output power. To verify the linearity impact from dynamic stacking, dynamic AM–AM and AM–PM have been measured, which showed negligible gain and phase steps at the stack switching points. Full LTE characterization is performed using fully loaded LTE signals with a PAPR of 6.7 dB and signal bandwidths of 10 and 20 MHz. With 10-MHz LTE signals, dynamic stacking provides 3.5% PAE improvement over the static stack at the maximum linear output power of 25.7 dBm, resulting in 47.5% PAE with 26.6-dB gain. DE of the power stage is as high as 51.4%. A 20-MHz LTE test shows that the proposed PA is capable of handling wideband signals.

Even if the measured efficiency of the EA is lower than the state-of-the-art EA results, the measured overall system efficiency with 3.4 V supply is comparable with those reported using GaAs HBTs with 5 V operation, which clearly demonstrates the advantages of the proposed concept.

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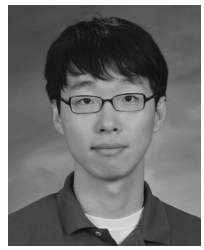

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