

A Concurrent $Ku/K/Ka$ Tri-Band Distributed Power Amplifier With Negative-Resistance Active Notch Using SiGe BiCMOS Process

Kyoungwoon Kim, *Student Member, IEEE*, and Cam Nguyen, *Fellow, IEEE*

Abstract—A new tri-band power amplifier (PA) on a 0.18- μm SiGe BiCMOS process, operating concurrently in Ku -, K -, and Ka -band, is presented. The concurrent tri-band PA design is based on the distributed amplifier structure with capacitive coupling to enable large device size, while maintaining wide bandwidth, gain cells with the enhanced-gain peaking inductor, and negative-resistance active notch filters for improved tri-band gain response. The concurrent tri-band PA exhibits measured small-signal gain around 15.4, 14.7, and 12.3 dB in the low band (10–19 GHz), midband (23–29 GHz), and high band (33–40 GHz), respectively. In the single-band mode, the PA has maximum output powers of 15, 13.3, and 13.8 dBm at 15, 25, and 35 GHz, respectively. When the PA is operated in dual-band mode, it has maximum output powers of 11.4/8.2 dBm at 15/25 GHz, 13.3/3 dBm at 15/35 GHz, and 8.7/6.7 dBm at 25/35 GHz. In the tri-band mode, it exhibits 8.8/5.4/3.8-dBm maximum output power at 15/25/35 GHz. The concurrent tri-band PA exhibits relatively flat responses in gain and output power across its three frequency bands and good matching up to 40 GHz.

Index Terms—Active notch filter, BiCMOS, CMOS, distributed amplifier (DA), multi-band, multi-band power amplifier (PA), PA, RF integrated circuit (RFIC).

I. INTRODUCTION

MULTIBAND RF systems provide numerous advantages as compared to their single-band counterparts for communications and sensing. Multiband operation is doubly attractive when all of the multiband functions can be realized within a single system hardware using concurrent design principle for all constituent components, thus making the entire system not much more complicated than a single-band counterpart. Achieving concurrent functions over multiband enables one single system to be used in multiple bands simultaneously—avoiding the need of physically combining separate systems, each working in an individual band together. A multiband system that incorporates several different systems increases the size and complexity, and is difficult and expensive to realize in practice—particularly when more bands are involved and many systems, such as in large networks,

are needed. The concurrency approach integrates multiband together electrically besides physically. Consequently, the total RF components in a concurrent system employing truly concurrently components remain essentially the same as those for a single-band counterpart, leading to optimum size, cost, power consumption, and ease in realization for the system. Concurrent functions also eliminate some usual components in multiband systems, such as those needed for combining and splitting signals in different bands as used in conventional system architectures, thus enhancing the performance and further reducing the system size, cost, and complexity.

Concurrent multiband power amplifiers (PAs) are the most important component in concurrent multiband transmitters. Concurrent multiband PAs are designed to support multimode (or concurrent modes) in which multiband signals occur simultaneously; yet they can also support single mode in which only the signal in one band occurs at each time. Various approaches for multiband PAs have been reported [1]–[6]. In [1] and [2], individual PAs were designed for different frequency bands and combined in parallel to achieve multiband operation for the composite PA. This type of multiband PA achieves better performance than other multiband PAs since each individual PA is optimized for each frequency band. However, these PAs have large size, are not cost efficient, and have more complex circuitry due to the employed combining structures, matching networks, and biasing and switching circuits. Moreover, these PAs cannot support concurrent modes because they operate using bias switching for selected frequency mode. In [3] and [4], reconfigurable matching networks were implemented to realize multiband PAs. These PAs can reduce the number of active devices and have smaller chip size as compared to those in [1] and [2]. The approach in [3] and [4], however, also has the same drawbacks of [1] and [2], in which different control voltages are needed to adjust reconfigurable elements, and hence cannot be operated simultaneously for different signal bands, thereby not supporting concurrent modes.

Concurrent multiband PAs were proposed using multiband input and output matching networks [5], [6]. Using multiband matching reduces the circuit complexity and chip size as compared to the approaches in [1]–[4]. Multiband matching networks consist of passive elements, such as inductors, capacitors, and resistors, which lead to increased insertion loss, especially for inductors in silicon substrates, and large size when many of them are used. Concurrent multiband PAs with less passive elements in the matching networks are preferred for optimum performance.

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The authors are with the Electrical and Computer Engineering Department, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: kyoungwoon.kim@tamu.edu; cam@ece.tamu.edu).

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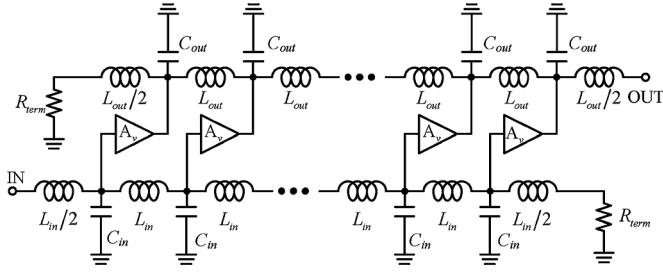


Fig. 1. Schematic of a conventional DA.

In this paper, we report a new tri-band PA operating concurrently in three different bands of 10–19, 23–29, and 33–40 GHz. The concurrent tri-band PA is based on the distributed amplifier (DA) structure and realized using a 0.18- μm SiGe BiCMOS process. Specifically, the concurrent tri-band PA implements the active notch filters having negative-resistance property, instead of tri-band matching networks, to achieve the concurrent tri-band operation with a better tri-band gain response resulted from increased quality factor (Q). The simulated and measured small- and large-signal results demonstrate the concurrent tri-band PA's workability not only in tri-band, but also in dual- and single-band.

II. GENERAL DISTRIBUTED PA DESIGN

The proposed concurrent tri-band PA is based on the DA structure. Therefore, the design of distributed PAs is briefly discussed first in this section.

A. Capacitively Coupled DA for Enhanced Power-Handling Capability

Fig. 1 shows a basic topology of the DAs, which consists of an input synthetic transmission line represented by inductors (L_{in} , $L_{in}/2$) and capacitors (C_{in}), output synthetic transmission line represented by inductors (L_{out} , $L_{out}/2$) and capacitors (C_{out}), terminating resistors (R_{term}), and gain cells (A_v 's). The cutoff frequency of the input and output synthetic transmission lines can be written as

$$f_c = \frac{1}{\pi\sqrt{L_{in}C_{in}}} = \frac{1}{\pi\sqrt{L_{out}C_{out}}} \quad (1)$$

accounting for the required phase matching between these transmission lines. The bandwidth of the DA is proportional to this cutoff frequency, which is, in turn, reversely proportional to the capacitance of the synthetic transmission lines. Since the power handling capability of the DA is proportional to the size of the employed active devices, large devices are needed for high power. Large devices, however, produce large parasitic capacitances, hence inadvertently limiting the DA's bandwidth. The design of a PA based on the distributed topology thus requires a tradeoff between the output power and bandwidth. One possible solution for improving the power-handling capability without compromising the bandwidth of the distributed PA is implementing a capacitively coupled structure by adding a series capacitor at the input of the gain stage, as proposed in [7].

Fig. 2 shows the equivalent circuits of a single-cell DA and capacitively coupled DA employing a capacitor in series

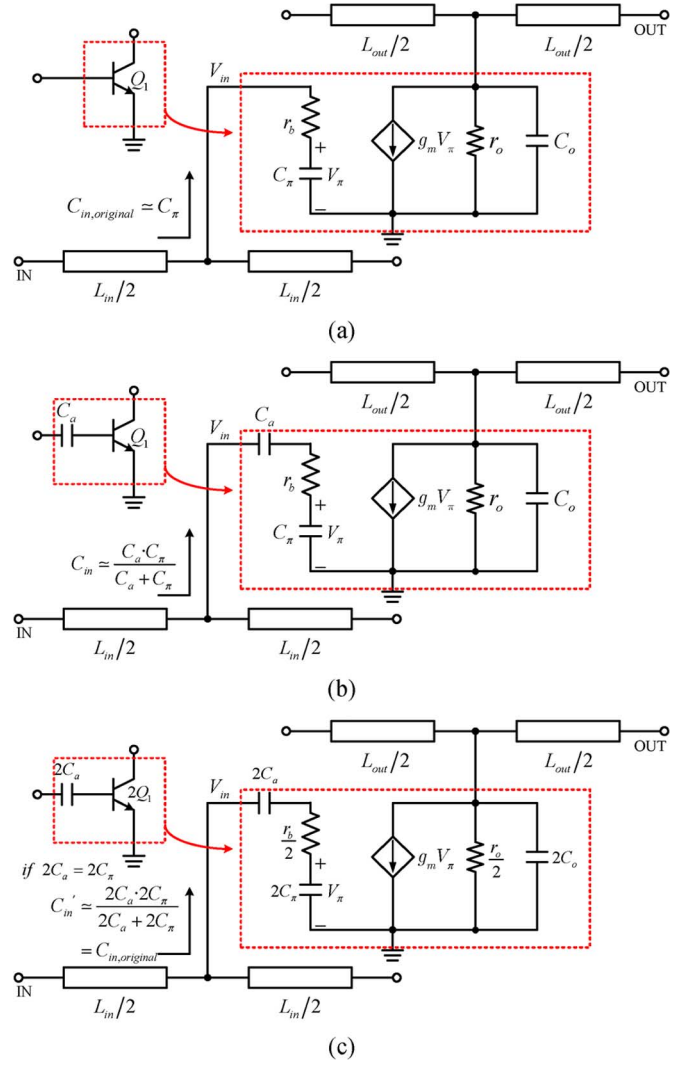


Fig. 2. Equivalent circuits of a single-cell DA (a) and capacitively coupled DA: (b) without and (c) with the transistor size and series capacitance doubled.

with a common-emitter bipolar junction transistor (BJT) for two different BJT sizes (Q_1 , $2Q_1$) and capacitance values (C_a , $2C_a$). r_b , C_π , r_o , C_o , g_m , represent the series base resistance, emitter-base capacitance, output resistance, output capacitance, and transconductance of the BJT, respectively, that constitute a simplified small-signal equivalent-circuit model for the BJT. For good BJTs, r_b is negligibly small, and hence the input capacitance of the BJT's equivalent circuit [see Fig. 2(b)] can be approximately obtained as

$$C_{in} \simeq \frac{C_\pi C_a}{C_a + C_\pi}. \quad (2)$$

The added capacitance (C_a) is in series with the parasitic capacitance (C_π) of the BJT, causing a reduction in the total input capacitance (C_{in}) of the device, as can be seen in (2). The added capacitance also causes a voltage drop across the base terminal as

$$V_\pi = \frac{C_a}{C_a + C_\pi} V_{in}. \quad (3)$$

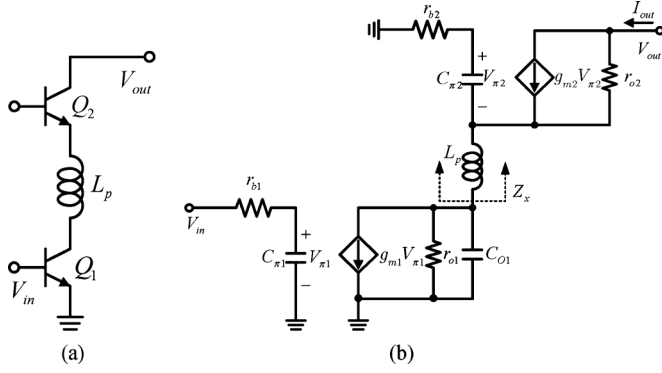


Fig. 3. (a) Peaking cascode gain-cell with peaking inductor L_p and (b) its equivalent small-signal model.

When the transistor size is doubled, as shown in Fig. 2(c), its parasitic capacitance also increases approximately twice as much ($2C_{\pi}$). If an external capacitor having a capacitance of $2C_a = 2C_{\pi}$ is added to the transistor's input, then the total input capacitance (C'_{in}) would remain the same as the original input capacitance ($C_{in,original}$) of the original device as seen in

$$C'_{in} = \frac{2C_{\pi} \cdot 2C_a}{2C_a + 2C_{\pi}} = C_{in,original}. \quad (4)$$

Equation (4) shows that the transistor's size can be increased along with a properly adjusted series capacitor to maintain the overall input capacitance. In other words, increasing the device periphery for high power along with a proper series capacitor does not affect the loading capacitance of the DA's input synthetic transmission line, and hence its bandwidth. Each gain cell of the capacitively coupled DA with its transistor size doubled can handle higher input power and produce more output power, while does not affect the DA's operating bandwidth. As seen in (3), the series capacitor (C_a) acts as a voltage divider and reduces the amplitude of the RF signal at the base terminal, consequently increasing the input power-handling capability. For typical BJTs, the output parasitic capacitance is smaller than the input parasitic capacitance, resulting in different phase velocities for the two synthetic transmission lines, and hence unmatched phases. A larger device, as desired here, would generate larger output parasitic capacitance, thereby enabling better phase matching between the input and output synthetic transmission lines [7].

B. Inductive Peaking in Gain Cell for Bandwidth Enhancement

Practical DAs employ a finite number of gain cells to minimize the loss of the passive elements and the parasitics of the active devices, which lead to the optimal number of gain cells for DAs [8]. Four or five gain cells are typically used in recent DAs designed in silicon technology [9]. Several types of gain cells can be used for DAs [10]. The cascode structure has better reverse isolation than the common-emitter and common-source structures, and is chosen as the core for the gain cell in the proposed distributed concurrent tri-band PA.

The cascode structure, however, has a drawback in which the parasitic capacitance at the internal node of the cascode structure creates a pole affecting the bandwidth of the gain cell.

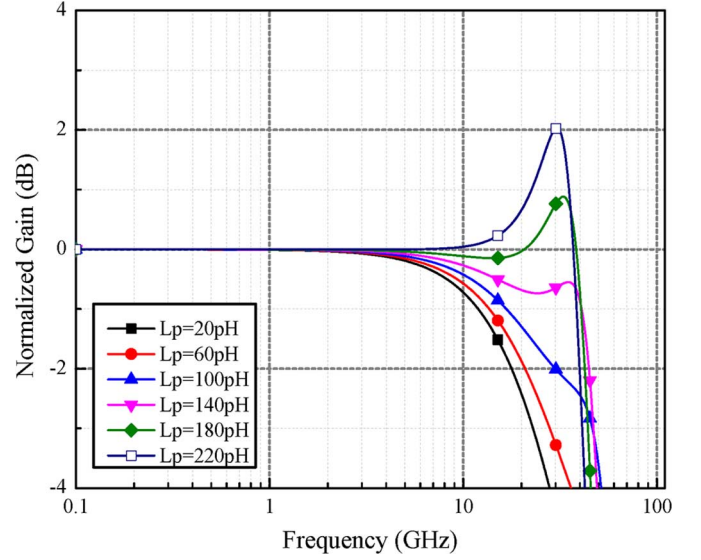


Fig. 4. Normalized gain versus frequency for various series peaking inductor values.

To resolve this problem, we utilize the inductive peaking technique [11], [12] to form a peaking cascode gain cell consisting of the basic cascode structure with a series peaking inductor between the common-emitter and common-base transistors. Fig. 3(a) shows this peaking cascode gain cell and Fig. 3(b) shows its small-signal equivalent circuit. The transfer function can be written as

$$\begin{aligned} G_m(s) &= \frac{I_{out}(s)}{V_{in}} \\ &= -g_{m1} \cdot \left(\frac{1}{sC_{O1}} \parallel Z_x \right) \\ &\quad \cdot \left(\frac{g_{m2}}{s^2 L_p C_{\pi 2} + s L_p g_{m2} + 1} \right) \\ &= -g_{m1} \cdot \frac{1}{1 + sC_{O1}Z_x} \cdot \frac{1}{1 + s \frac{C_{\pi 2}}{g_{m2}}} \end{aligned} \quad (5)$$

where

$$Z_x(s) = sL_p + \frac{1}{1 + s \frac{C_{\pi 2}}{g_{m2}}}. \quad (6)$$

This transfer function is based on a BJT; a similar expression using a MOSFET is presented in [12]. According to (5), the transfer function of the peaking cascode gain cell has a pole at $\omega_o = g_{m2}/C_{\pi 2}$ and depends on the impedance Z_x . Due to the existence of L_p , Z_x can cause a resonance with C_{O1} , the output capacitance of Q_1 , and produces gain peaking at the resonant frequency ω_p of Z_x and C_{O1} [12]. Fig. 4 shows the simulated performance of the peaking cascode gain cell with various inductance values for L_p . As can be seen, using a large peaking inductor increases the bandwidth and gain peaking. These simulation results show that the cascode gain cell with an induc-

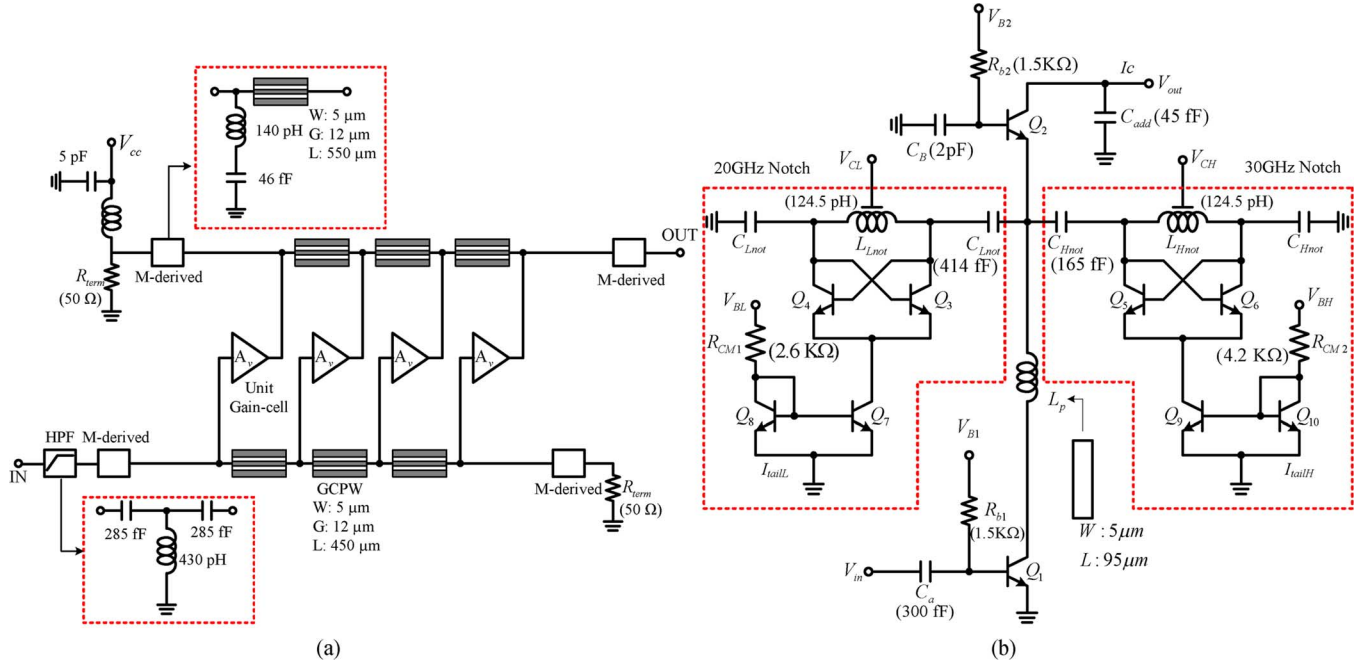


Fig. 5. (a) Schematic of the concurrent tri-band PA and (b) its gain-cell unit.

tive peaking technique enables flatter gain response and compensates for the gain drop due to the parasitic elements at high frequencies for the DAs.

III. DESIGN OF THE CONCURRENT TRI-BAND PA

A tri-band PA operating concurrently in three separate bands of 10–19, 23–29, and 33–40 GHz is designed based on the DA approach discussed in Section II and fabricated using the Jazz 0.18- μm SiGe BiCMOS process [13]. Fig. 5 shows the schematic of the concurrent tri-band PA and one of its gain cells. The concurrent tri-band PA consists of a high-pass filter (HPF) at the input and multiple gain cells, each consisting of a peaking cascode gain cell and two active notch filters at 20 and 30 GHz, and grounded conductor-backed coplanar waveguide (GCPW) simulating inductive transmission lines.

A. GCPW

Fig. 6 shows the GCPW used to realize the inductive transmission lines in the concurrent tri-band PA. The lowest metal layer (M1) is used as the back conductor and substrate shielding. The top metal layer (M6) is used for the signal line and two-sided ground planes. The sided ground planes are tied together with the back conductor through vias connecting all the metal layers (M1–M6).

As compared to microstrip line, the GCPW lends itself more freedom in optimizing the transmission-line parameters, such as characteristic impedance and loss, using the width of the signal line and the gaps between the signal and coplanar ground lines, as well as provides more isolation between adjacent lines due to the existence of the coplanar ground lines. The GCPW is also more preferred than the conventional CPW, as it can shield the transmission line from the high-conductivity silicon substrate, hence leading to lower dielectric loss, which could be substantial at millimeter-wave frequencies.

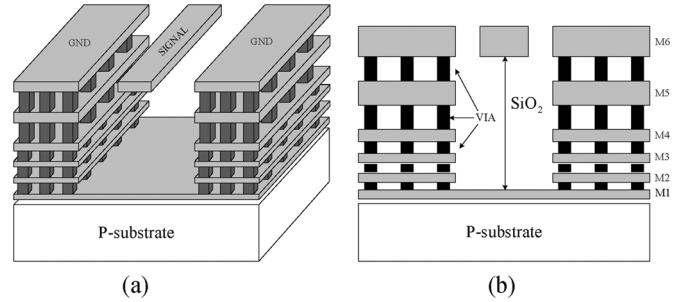


Fig. 6. GCPW: (a) side view and (b) cross section view.

As compared to the conventional CPW, the GCPW has lower loss, yet also lower characteristic impedance. Moreover, the GCPW implemented on a CMOS/BiCMOS process should have a larger gap between the signal and ground lines to maintain the same signal-line width for a given characteristic impedance, and hence the same conductor loss, thereby resulting in a slightly increased size.

Fig. 7 compares the attenuation constant and characteristic impedance, simulated using IE3D [14], for the CPW and GCPW having the same physical dimensions of 5- μm width, 12- μm gap, and 500- μm length, showing the expected results of less loss and lower characteristic impedance for the GCPW. Such GCPW is used as the inductive transmission lines in the concurrent tri-band PA.

B. HPF

A simple HPF is used in front of the input synthetic transmission line, as shown in Fig. 5(a), to suppress undesired gain at low frequencies below 10 GHz. The HPF has a cutoff frequency of 10 GHz and consists of three elements: a 430-pH inductor and two 285-fF capacitors.

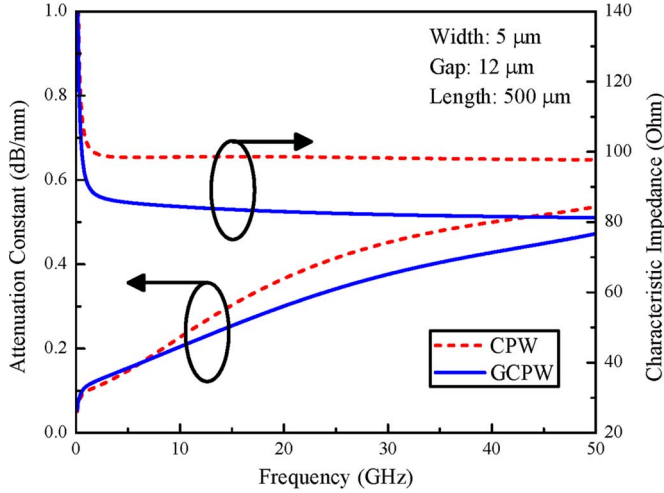


Fig. 7. Attenuation constant and characteristic impedance of GCPW and CPW.

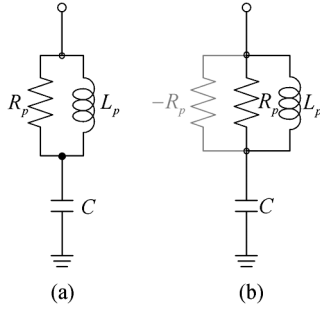


Fig. 8. (a) LC notch filter model with lossy inductor and (b) active notch filter with lossy inductor and negative resistance.

C. Active Notch Filter With Negative Resistance

The tri-band response can be realized by incorporating notch filters at the desired stopbands. Passive notch filters with high orders can produce large rejection ratios, yet also leading to high insertion loss and large size on silicon. Moreover, as passive notch filters typically consist of inductors and capacitors, the Q of the inductors primarily affect the attenuation characteristics of the notch filters at the notch frequency. Design of high- Q integrated inductors in current CMOS and BiCMOS technologies, however, is challenging, which hinders the design of high-rejection passive notch filters. One possible solution to enhance the Q of integrated inductors is incorporating a negative-resistance circuit whose negative resistance compensates for the loss, and hence improves the Q of the inductors. Fig. 8(a) shows a simple LC notch filter model with a lossy inductor represented by inductance L_p and resistance R_p accounting for the inductor's loss. The Q of the inductor, and hence the notch filter, is proportional to R_p and can thus be enhanced significantly by adding a negative resistance close to $-R_p$ in parallel with R_p to form an active notch filter, as shown in Fig. 8(b).

To generate a negative resistance needed to enhance the inductor's Q , a cross-coupled pair of two BJTs is used as shown in Fig. 5(b). The real part of the input impedance between the two

collectors' nodes of the cross-coupled circuit can be derived as [15]

$$R_{in} = -\frac{2}{g_m} \quad (7)$$

which shows that a negative resistance can be produced with a cross-coupled transistor pair. Two active notch filters with negative-resistance cross-coupled BJT circuits were designed to have resonance frequencies of 20 and 30 GHz, as shown in Fig. 5(b). To facilitate the formation of a symmetrical structure with the cross-coupled pair, an identical capacitor (C_{Lnot} or C_{Hnot}) is used at each side of a differential inductor (L_{Lnot} or L_{Hnot}) for each negative g_m cell. 414 and 165 fF are used for C_{Lnot} and C_{Hnot} of the 20- and 30-GHz notch filters, respectively. Proper device size and tail current of the cross-coupled pairs need to be determined to produce desired g_m . To that end, devices having $0.15\text{-}\mu\text{m}$ emitter width and $2.54\text{-}\mu\text{m}$ emitter length are chosen for both notch filters. The tail current is set by using a current mirror so that the reference current can be duplicated at the common node of cross-coupled cell using the same device size ($Q_7 = Q_8, Q_9 = Q_{10}$). The tail currents for the cross-coupled pairs in the 20- and 30-GHz notch filters are 587 and $388\text{ }\mu\text{A}$, respectively. With these devices and tail currents, 10.5 and 7 mS of transconductance are generated for the 20- and 30-GHz notch filters, respectively.

The design center frequencies of the tri-band PA are about 15, 25, and 35 GHz per our system's specifications. The notch frequencies are around 20 and 30 GHz, which are not chosen arbitrarily. This choice is made to produce a symmetrical stopband at 20 GHz between the first (15 GHz) and second (25 GHz) passbands and at 30 GHz between the second (25 GHz) and third (35 GHz) passbands, to reject the first passband's second harmonic at 30 GHz, and to achieve approximately the same passband bandwidth for the three passbands (11–19, 21–29, and 31–40 GHz).

Fig. 9 shows the simulation ports and results for the designed passive and active notch filters at 20.3 and 30.1 GHz. It is apparent that the active notch filters having negative resistance improves the depth as well as the sharpness of the notches as compared to the conventional LC notch filters. The negative resistance generated in the active notch filter by the negative-resistance cell reduces substantially the effect of the inductor loss, and consequently enhances the Q of the notch filters.

D. Concurrent Tri-Band PA

Fig. 5(a) shows the schematic of the concurrent tri-band PA. Four identical gain-cells, A_v , are employed along with the GCPW to form the required input and output synthetic transmission lines.

To provide better matching for the synthetic transmission lines, an m-derived half section is used at each side of the transmission lines. The series inductors of the m-derived half sections are also designed using the GCPW for better integration with the GCPW of the synthetic transmission lines. The shunt inductors, however, are realized using spiral inductors to reduce the overall chip size. Fig. 5(b) shows the schematic of each designed gain cell. The gain cell is based

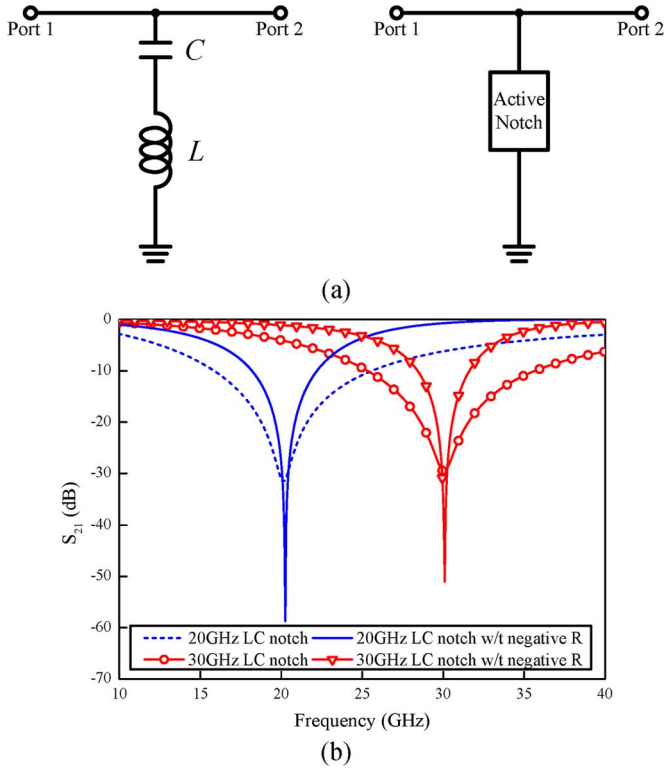


Fig. 9. 20- and 30-GHz LC passive and active notch filters. (a) Test ports and (b) simulated insertion losses.

on a cascode structure with a gain-peaking series inductor incorporating two active notch filters at 20 and 30 GHz. The employed SiGe HBT transistors have breakdown voltages of $BV_{CEO} = 1.9$ V and $BV_{CBO} = 5.8$ V with peak f_t of 200 GHz and f_{max} of 180 GHz. Table I shows the sizes, configurations, and bias voltages and currents of the employed transistors. The transistors (Q_1, Q_2) of the cascode cell have an emitter area of $0.15 \times 9.04 \mu\text{m}^2$ and the current density of the device is $4 \text{ mA}/\mu\text{m}^2$. The active notch filters provide the necessary tri-band function with good response for the concurrent tri-band PA. The gain-peaking inductor is implemented using a microstrip line. The input series capacitor (C_a) helps reduce the total input capacitance of the gain-cell unit and enables large device periphery to be used, hence resulting in improved power-handling capability. The value of C_a is 300 fF and almost the same as the overall input capacitance of Q_1 . Four transistors, each having $0.15\text{-}\mu\text{m}$ emitter width and $4.52\text{-}\mu\text{m}$ emitter length, are combined to generate each device (Q_1 or Q_2) in the cascode cell. The additional shunt capacitor (C_{add}) is used at the output node to achieve phase matching between the input and output synthetic transmission lines. This is necessary since the output parasitic capacitance of BJTs is typically smaller than the input parasitic capacitance. C_{add} is absorbed into the parasitic of the output synthetic transmission line.

All of the passive elements were simulated and optimized using the electromagnetic (EM) simulator IE3D [14]. Fig. 10 shows a photograph of the concurrent tri-band PA, which occupies a die size of $2 \text{ mm} \times 1 \text{ mm}$ including the RF and dc

TABLE I
TRANSISTOR SIZES AND CONFIGURATIONS AND BIAS CONDITIONS

Transistor	Emitter width \times length – E, B, C finger	Multiplier
Q_1, Q_2	$0.15\mu\text{m} \times 4.52\mu\text{m} - 2, 3, 2$	4
$Q_3\text{--}Q_{10}$	$0.15\mu\text{m} \times 2.54\mu\text{m} - 1, 2, 1$	1

V_{B1}	V_{B2}	V_{BL}	V_{BH}	V_{CC}	V_{CL}	V_{CH}
1.2 V	2.4 V	2.4 V	2.5 V	3 V	2.4 V	2.4 V

I_C	I_{tailL}	I_{tailH}
21.5 mA	587 μA	388 μA

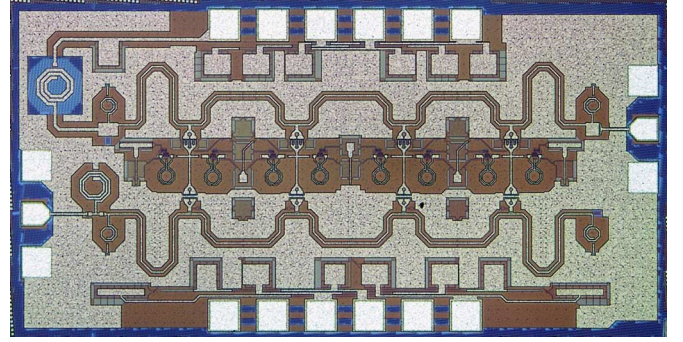


Fig. 10. Photograph of the fabricated concurrent tri-band PA.

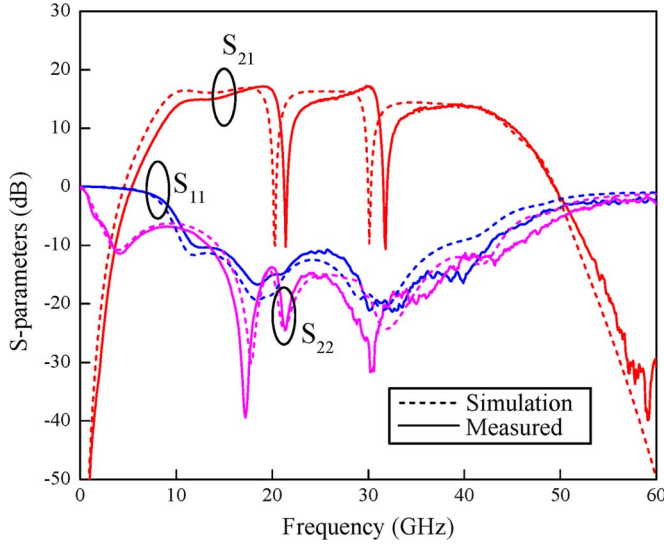
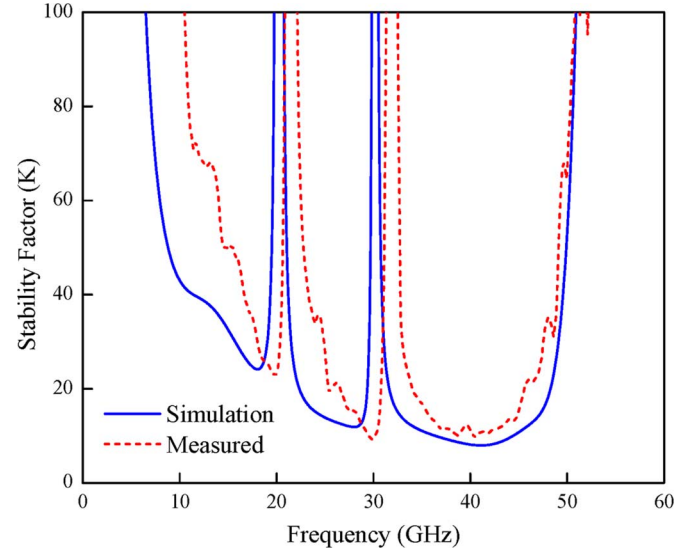
pads. The RF pad has $90 \mu\text{m} \times 75 \mu\text{m}$ for the signal pad and $100 \mu\text{m} \times 100 \mu\text{m}$ for each of the ground pads with $150\text{-}\mu\text{m}$ pitch. The ground pad is implemented with six metal stacks (M1–M6), while the signal pad uses only the two topmost metals (M5 and M6). The size of the dc pads is $100 \mu\text{m} \times 100 \mu\text{m}$ for each pad with $150\text{-}\mu\text{m}$ pitch.

IV. SIMULATION AND MEASUREMENT RESULTS

Small-signal performance based on S -parameters and large-signal responses were simulated and measured on-wafer. The large-signal characterizations include single-, dual-, and triple-band mode in which signals in one, two, and three bands were used as the input, respectively.

A. Small-Signal Performance

Fig. 11 shows the simulated and measured S -parameters of the concurrent tri-band PA, which are well matched to each other. Table II summarizes the results. The gain differences between the simulation and measured results are due to the change of the notch frequencies. The simulated notch frequencies are 20.3 and 30.1 GHz, whereas those measured are 21.4 and 31.8 GHz. Since the resonance frequencies of the two notch filters shift up, the gain responses for the midband and high-band also move to slightly higher frequencies. Decent gains and input and output matching are obtained in all three frequency bands. It is noted that, in general, DAs normally have good input and output matching from dc up to a high frequency. The designed concurrent tri-band PA, however, has a different matching behavior due to the HPF located at the input of the input synthetic transmission line and the on-chip choke inductor that supplies bias at the collector of the upper BJT of each cascode gain cell. At low frequencies, the input matching follows that of the HPF, whereas the output matching

Fig. 11. Measured and simulated S -parameters.Fig. 12. Measured and simulated K factor.TABLE II
SUMMARY OF MEASURED AND SIMULATED S -PARAMETERS

	Gain (S_{21})		
	Low-Band (10-19 GHz)	Mid-Band (23-29 GHz)	High-Band (33-40 GHz)
Simulation (dB)	15.5-16.1	15.3-16.1	13.9-14.2
Measured (dB)	13.7-17.1	13-16.4	10.6-13.9
Gain Variation	< 1.8 dB 0.9dB at 15GHz	< 2.3 dB 1.4dB at 25GHz	< 3.3 dB 1.2dB at 35GHz

Measured Input and Output Matching	
S_{11}	< -10 dB between 11.8 GHz and 42.6 GHz
S_{22}	< -10 dB between 13 GHz and 46 GHz

	Notch Frequency	
	Low-Band	High-Band
Simulation	20.3 GHz	30.1 GHz
Measured	21.4 GHz	31.8 GHz

is affected by the choke inductor. Fig. 12 shows the simulated and measured stability factor (K) of the concurrent tri-band PA, demonstrating its unconditional stability up to 60 GHz. The measured and calculated K 's also behave similarly.

B. Large-Signal Characteristics for Single-Band Mode

The large-signal performance of the concurrent tri-band PA under the single-band mode was characterized by using an input signal in one of the three frequency bands at a time. Fig. 13(a)–(c) shows the simulated and measured output power (P_{out}), power gain, and power-added efficiency (PAE) as a function of input power level at 15, 25, and 35 GHz, respectively. As shown in Fig. 13(a), at 15 GHz, the concurrent tri-band PA exhibits measured maximum output power ($P_{out,max}$) of 15 dBm, 11.4-dBm output power at 1-dB compression point (P_{1dB}), and maximum PAE of 10% at around a 5-dBm input power level. The measured power gain and output power are almost the same as the simulation results, but the measured PAE is lower than the simulated one. For the case of

25 GHz, as shown in Fig. 13(b), 13.3-dBm $P_{out,max}$, 3.3-dBm P_{1dB} , and maximum PAE of 6.5 % at around 4-dBm input power were measured. At 35 GHz, the measured results show 13.8-dBm $P_{out,max}$, 0-dBm P_{1dB} , and 7.5% PAE at 6.5-dBm input power. As can be seen at 25 and 35 GHz, the measured and simulated power gain and output power match reasonably well, while the measured PAE decreases from the simulated one.

Fig. 13(d)–(f) shows the simulation and measurement results for $P_{out,max}$ and P_{1dB} versus frequency in three separate bands. In the low band (10–19 GHz), the measured $P_{out,max}$ and P_{1dB} are between 14.4–15.4 dBm and 8.2–13.1 dBm, respectively. In the midband (23–29 GHz), the measured $P_{out,max}$ is between 14–14.7 dBm from 25 to 29 GHz, and 9.2–11.8 dBm at 23 and 24 GHz, respectively. It is also observed that the P_{1dB} at 23 and 24 GHz are smaller than those at other frequencies. This power-drop phenomenon occurs when the input signal gets closer to the stopband of the notch. The active notch circuit can degrade the linearity of the amplifier due to the nonlinear characteristics of the active devices, and therefore, P_{out} and P_{1dB} can be reduced within the active notch circuit's operating region. The P_{1dB} of the PA actually follows the responses of the constituent active notch filters. This phenomenon is also observed at the high-band frequencies, as shown in Fig. 13(f). If the input signal moves closer to 31.8 GHz, which is the designed notch frequency, P_{1dB} decreases. The measured $P_{out,max}$ across the high band (33–40 GHz) is 13–14 dBm. As can be seen, the measured and simulated $P_{out,max}$ are in good agreement for all bands, except in the midband below 25 GHz.

The measured results particularly show that the variation of the $P_{out,max}$ of the designed concurrent tri-band PA over the three different bands is relatively small. It is noted that the measurements of the concurrent tri-band PA in single bands are only for references; this PA is not designed for single-band operation.

C. Large-Signal Characteristic for Dual-Band Mode

In the dual-band mode, two signals in two different bands are combined internally in the vector network analyzer (VNA) and

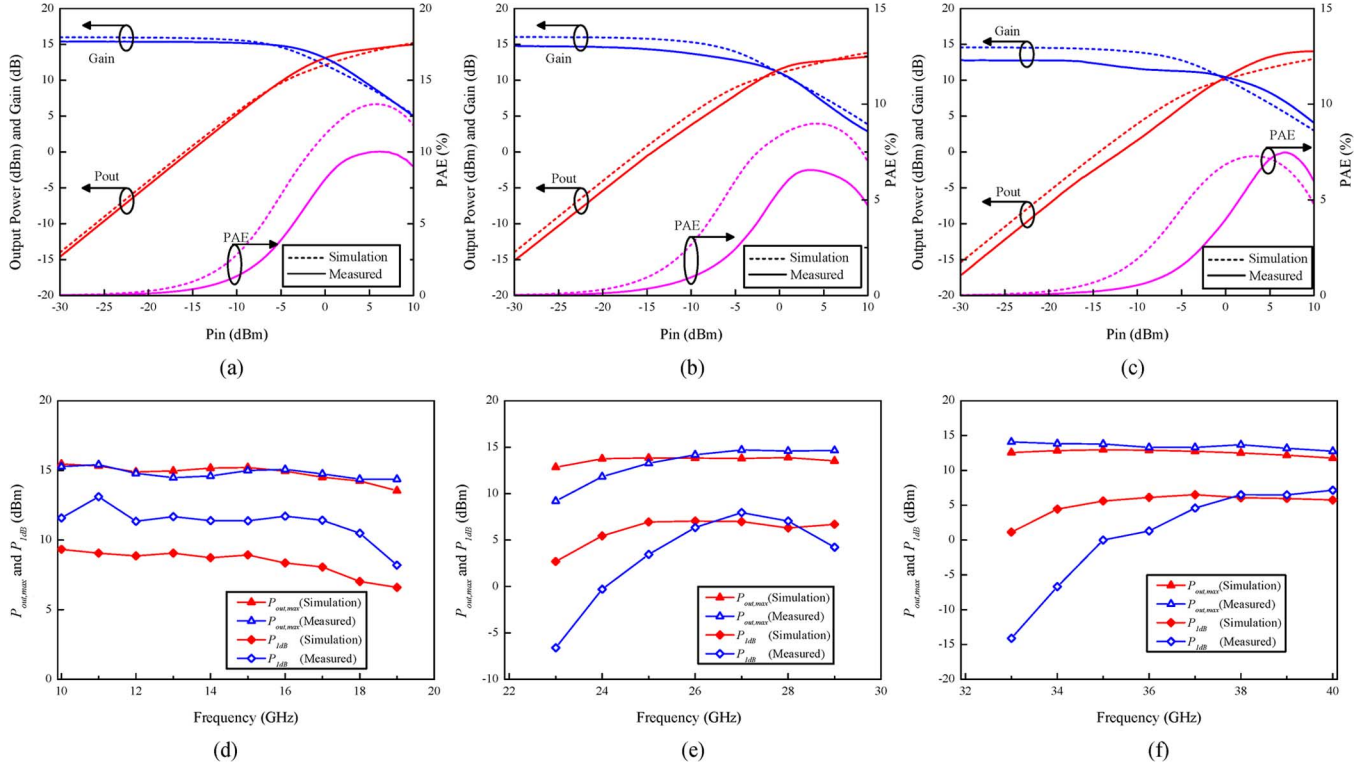


Fig. 13. Simulation and measurement results for the single-band mode: P_{out} , gain and PAE at: (a) 15, (b) 25, and (c) 35 GHz, and $P_{out,max}$ and P_{1dB} for: (d) low-band, (e) midband, and (f) high-band.

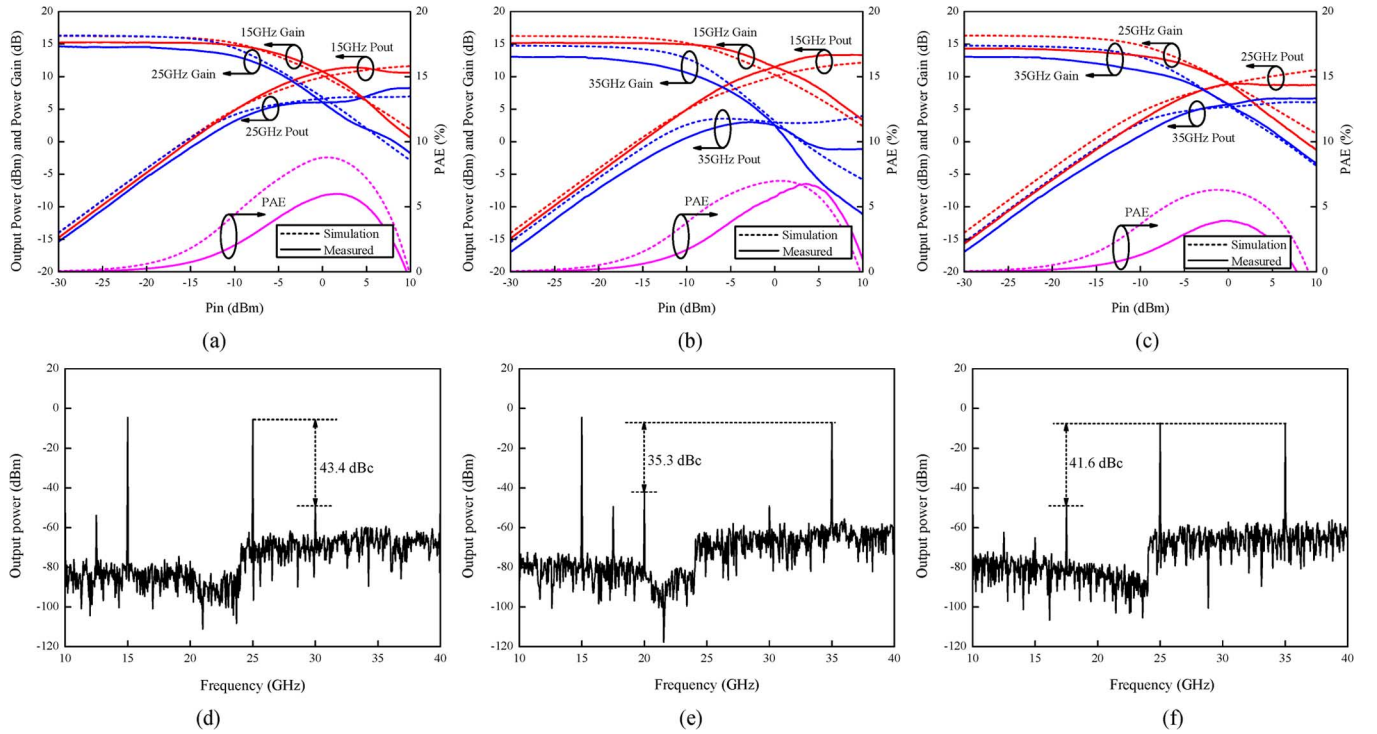


Fig. 14. Results for dual-band operations: simulated and measured P_{out} , power gain, and PAE for: (a) 15/25, (b) 15/35, and (c) 25/35 GHz, and measured output spectrum at -20 -dBm input power for: (d) 15/25, (e) 15/35, and (f) 25/35 GHz.

injected into the input of the concurrent tri-band PA simultaneously. The composite signals used in the measurements are at 15/25, 15/35, and 25/35 GHz. Fig. 14 shows the performance for three cases.

Fig. 14(a) shows the results for the P_{out} , power gain, and PAE for the first case of the dual-band mode at 15/25 GHz. It is noted that P_{in} in the abscissa is the (equal) input power at each frequency. At 15 and 25 GHz, the measured $P_{out,max}$ are 11.4 and

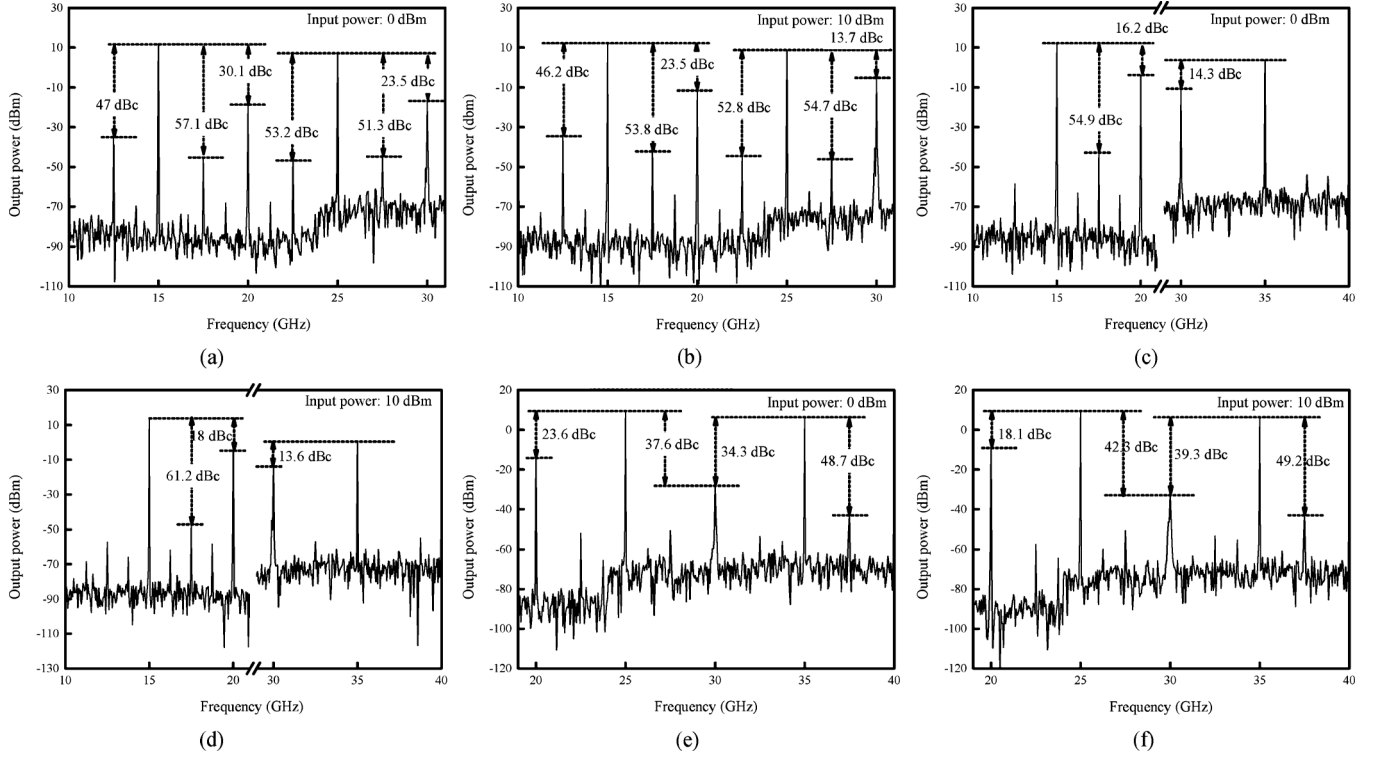


Fig. 15. Frequency spectra for dual-band operation modes with 0- and 10-dBm input power at: (a) and (b) 15/25, (c) and (d) 15/35, and (e) and (f) 25/35 GHz.

TABLE III
SUMMARY OF DUAL-BAND PERFORMANCE

		15/25 GHz	15/35 GHz	25/35 GHz
$P_{out,max}$ (dBm)	Simulation	11.6 / 6.7	12.2 / 3.5	11 / 6.1
	Measured	11.4 / 8.2	13.3 / 3	8.7 / 6.7
P_{1dB} (dBm)	Simulation	4.9 / 3	4.9 / 1.1	3.5 / 1.1
	Measured	7.1 / 1.7	8.7 / -2.6	2.6 / -2.9
Max. PAE (%)	Simulation	8.8	7	6.3
	Measured	6	6.8	3.9

8.2 dBm, and the P_{1dB} are 7.1 and 1.7 dBm, respectively. As can be seen, the measured and simulated results agree reasonably well. At 1.5-dBm input power, the measured PAE for the 15/25-GHz dual-band mode reaches a maximum value of 6%. The PAE for multi-band mode is calculated, taking into account the multiple concurrent signals, as

$$PAE(\%) = 100 \times \frac{\sum_{n=1}^N (P_{out,n} - P_{in,n})}{P_{DC}} \quad (8)$$

where N is the number of the concurrent input signals, $P_{out,n}$ and $P_{in,n}$ are the output and input powers for signal n , respectively, and P_{DC} is the dc power. Fig. 14(d) displays the output frequency spectrum under the 15/25-GHz dual-band operation when the power for each input signal is -20 dBm. It is observed that undesired signals are suppressed by at least 43 dB from the 15/25-GHz signal.

In the second case, the input signal is formed by two concurrent signals at 15 and 35 GHz. Fig. 14(b) shows the simulation and measured results. The concurrent tri-band PA achieves measured $P_{out,max}$ of 13.3 and 3 dBm and P_{1dB} of 8.7 and -2.6 dBm at 15 and 35 GHz, respectively, and maximum PAE of 6.8% at 3.5-dBm input power. The measured output frequency spectrum is shown in Fig. 14(e) with -20 dBm for each input signal. The suppression of unwanted signals is more than 35 dB.

The third case has 25- and 35-GHz signals combined for the input signal. Fig. 14(c) shows the simulation and measured results. The measured $P_{out,max}$ and P_{1dB} are 8.7 and 2.6 dBm at 25 GHz, while those at 35 GHz are 6.7 and -2.9 dBm, respectively. The maximum PAE is 3.9% at -0.2 -dBm input power. The output frequency spectrum is shown in Fig. 14(f) at an input power of -20 dBm, indicating at least 41-dB suppression for undesired signals. Table III summarizes the simulation and measurement results.

Fig. 15 shows the frequency spectra for the three dual-band operation modes at 15/25, 15/35, and 25/35 GHz for 0- and 10-dBm input power. As can be seen, the amplitudes of the intermodulation tones increase as the input power is increased. The 20- and 30-GHz intermodulation signals are also larger than others. This is due to the fact that the measured notch frequencies actually occur at 21.4 and 31.8 GHz, hence causing less rejection at 20 and 30 GHz.

D. Large-Signal Characteristics for Tri-Band Mode

Finally, the tri-band mode for the concurrent tri-band PA was measured using the concurrently combined 15/25/35 GHz as the input signal. The 25- and 35-GHz signals provided by the

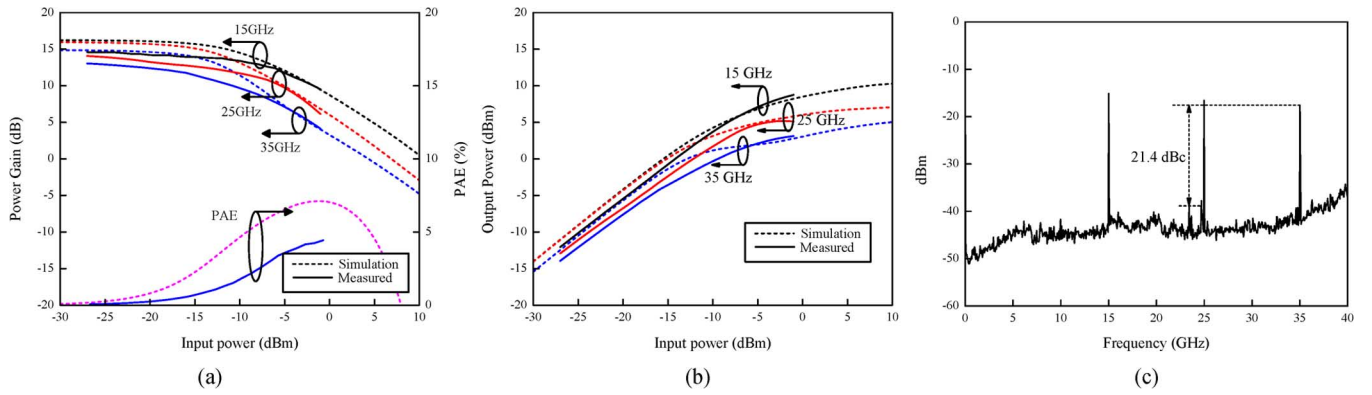


Fig. 16. Performance for the 15/25/35 GHz tri-band mode: measured and simulated (a) power gain and PAE and (b) output power, and (c) measured frequency spectrum at -27 -dBm input power.

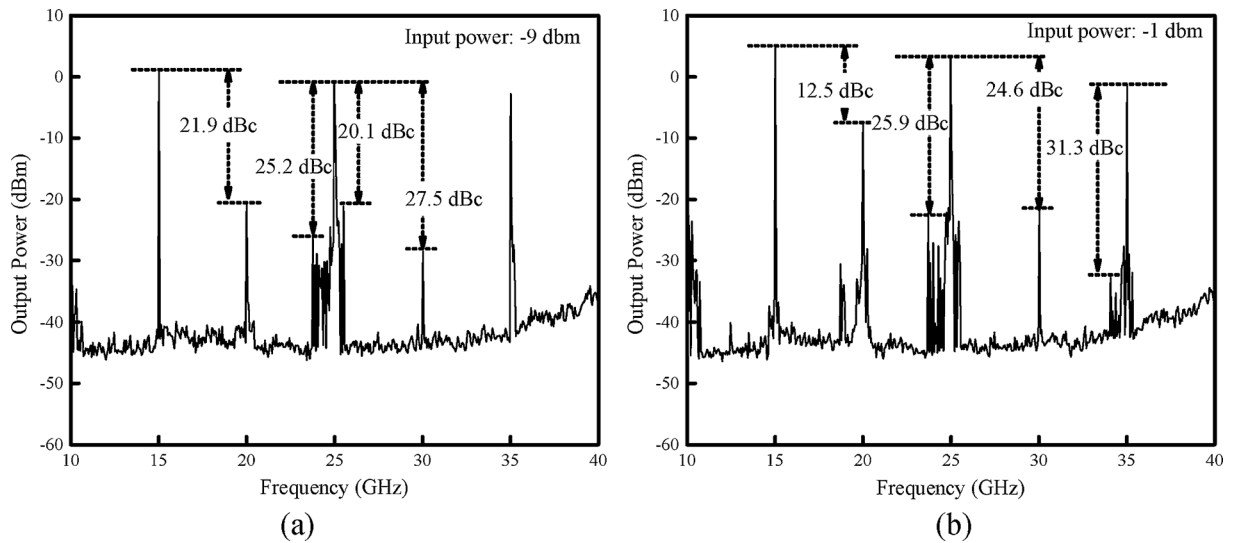


Fig. 17. Frequency spectrum for tri-band operations with respect to input power with: (a) -9 -dBm input power and (b) -1 dBm input.

TABLE IV
SUMMARY OF TRI-BAND PERFORMANCE

		15GHz	25GHz	35GHz
$P_{out,max}$ (dBm)	Simulation	10.3	7.1	5
	Measured	8.8	5.4	3.8
P_{1dB} (dBm)	Simulation	2.5	0.9	-1
	Measured	2.9	-5	-4.9
Max. PAE (%)	Simulation	7.1 at -1 dBm input		
	Measured	4.4 at -1 dBm input		

VNA are combined with the 15-GHz signal from an external synthesizer through a 2–50-GHz 13-dB directional coupler.

The simulation and experimental results are shown in Fig. 16. The measured results show $P_{out,max}$ of 8.8, 5.4, and 3.8 dBm, P_{1dB} of 2.9, -5 , and -4.9 dBm at 15, 25, and 35 GHz, and maximum PAE of 4.4% at -1 -dBm input power, respectively.

Fig. 16(c) shows the measured frequency spectrum of the output signal, showing more than 21-dB suppression of unwanted signals. It is noted that the maximum available input power is limited at -1 dBm due to the limited output power

from available sources and use of the 13-dB coupler for signals combination, hence resulting in less output power and PAE. Table IV summarizes the performance under the tri-band operation. Fig. 17 shows the frequency spectrums for the tri-band operation at 15/25/35 GHz for -9 and -1 -dBm input power. Similar to the dual-band operations mentioned earlier, we can see that many unwanted signals are generated and the amplitudes of the 20- and 30-GHz intermodulation tones are larger than others.

Table V compares the measured performance of the designed concurrent tri-band PA for different operating modes.

The designed concurrent tri-band PA does not achieve high PAE performance as compared to single-band PAs operating in the same frequency ranges, mainly due to the fact that it is not optimized for single-band operations. Moreover, the design of multi-band PAs having high output power over the entire multiple bands with decent PAE is very challenging. The PAE of the proposed tri-band PA, however, could be improved by modifying its topology and design—for instance, using different appropriate values for the series capacitor (C_a) for different gain cells [16], which result in equal input signal at each gain cell, leading to more constructive addition of the powers from the outputs of the gain cells, and hence improved PAE;

TABLE V
COMPARISON OF MEASURED PERFORMANCE FOR DIFFERENT OPERATING MODES

Parameters	Single-band mode			Dual-band mode			Tri-band mode
Frequency (GHz)	15	25	35	15/25	15/35	25/35	15/25/35
Gain (dB)	15.4	14.8	12.8	15.4/14.8	15.4/12.8	14.8/12.8	15.4/14.8/12.8
$P_{out,max}$ (dBm)	15	13.3	13.8	11.4 / 8.2	13.3 / 3	8.7 / 6.7	8.8/5.4/3.8
P_{1dB} (dBm)	11.4	3.3	0	7.1 / 1.7	8.7 / -2.6	2.6 / -2.9	2.9/-5/-4.9
Max. PAE (%)	10	6.5	7.5	6	6.8	3.9	4.4

TABLE VI
COMPARISON OF PROPOSED TRI-BAND PA AND SINGLE-BAND PAs

Ref	Technology	Operation Mode	Frequency (GHz)	Gain (dB)	Psat (dBm)	PAE (%)	Structure
[16]	0.25- μ m BiCMOS	Single-mode	1-12	12	16.2-19.5	10.3-22.1	Distributed Amplifier
[18]	0.18- μ m CMOS	Single-mode	DC-35	20.5	7-12.4 11@ 15 GHz 10@ 25 GHz 7@ 35 GHz	N/A	Distributed Amplifier
[19]	0.18- μ m CMOS	Single-mode	27	14.5	14	13.2	Narrow-band Amplifier
[20]	65 nm CMOS	Single-mode	27-34	>22.8	9.7-10.8	19.1-23.5	Medium-band Amplifier
[21]	0.18- μ m CMOS	Single-mode	31	6.1	12.3	N/A	Narrow-band Amplifier
This Work	0.18- μ m BiCMOS	Single-mode	10-19	13.7-17.1	14.4-15.4	10@ 15 GHz	Distributed-based Concurrent Amplifier
			23-29	13-16.4	9.5-14.7	6.5@ 25 GHz	
			33-40	10.6-13.9	12.8-14.1	7.5@ 35 GHz	
		Dual-band mode	15/25	15.4/14.8	11.4 / 8.2	6	
			15/35	15.4/12.8	13.3 / 3	6.8	
			25/35	14.8/12.8	8.7 / 6.7	3.9	
		Tri-band Mode	15/25/35	15.4/14.8/12.8	8.8/5.4/3.8	4.4	

using transistors with different periphery with tapered transmission line [17]; and implementation of a mechanism to suppress the intermodulation products. Suppression of the intermodulation products in multi-band PAs, however, is very challenging due to many unwanted signals resulting from multi-band operations—many of which could fall within the desired passbands.

Table VI compares the performances of the designed concurrent tri-band PA to some recently reported silicon-based single-band PAs at similar operating frequencies. It is noted that our PA is designed for multi-band operation, not for single-band operations as those it is compared to. Therefore, this comparison should not be taken strictly.

V. CONCLUSION

The development of the concurrent 10–19-, 23–29-, and 33–40-GHz tri-band PA on a 0.18- μ m SiGe BiCMOS process has been presented. The concurrent tri-band PA utilizes the DA topology with capacitive coupling to increase the power-handling capability. It also implements gain cells with series peaking inductor for enhanced gain peaking. Particularly, the concurrent tri-band PA incorporates two active notch filters having negative resistance in each gain cell to enhance the Q of the notch filters to produce better tri-band gain response. The GCPW is used to form the needed synthetic transmission lines to minimize the loss from the Si substrate. The concurrent tri-band PA exhibits fairly flat responses in gain and output

power across the designed three bands and good input and output matching up to 40 GHz. It can operate in tri-band as well as dual- and single-band modes. The concurrent tri-band PA should be attractive for tri-band communication and sensing systems operating in Ku -, K -, and Ka -bands. The concurrent tri-band design technique is extendable for other multiband distributed PAs and circuits involving more than three bands.

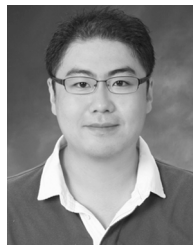
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Kyoungwoon Kim (S'10) received the B.S. degree in electronic and computer engineering from Hanyang University, Ansan, Korea, in 2004, the M.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2006, and is currently working toward the Ph.D. degree in electrical engineering at Texas A&M University, College Station, TX, USA.

His current research interests include CMOS and BiCMOS RF, microwave, and millimeter-wave integrated circuits and systems.



Cam Nguyen (F'05) joined the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX, USA, in December 1990, where he is currently the Texas Instruments Endowed Professor, after working for over 12 years in industry. From 2003 to 2004, he was Program Director with the National Science Foundation (NSF), where he was responsible for research programs in RF electronics and wireless technologies. From 1979 to 1990, he held various engineering positions in industry, including being a Microwave Engineer with the ITT Gilfillan Company, a Member of Technical Staff with the Hughes Aircraft Company (now Raytheon), a Technical Specialist with the Aerojet ElectroSystems Company, a Member of Professional Staff with the Martin Marietta Company (now Lockheed-Martin), and a Senior Staff Engineer and Program Manager with TRW (now Northrop Grumman). While in industry, he led numerous microwave and millimeter-wave activities and developed many microwave and millimeter-wave integrated circuits and systems up to 220 GHz for communications, radar, and remote sensing. His research group at Texas A&M University currently focuses on Si RF integrated circuits (RFICs) and systems for wireless communications, radar, and sensing. He is the Founding Editor-in-Chief of *Sensing and Imaging: An International Journal* (a Springer publication).