A Wideband Efficiency-Enhanced Class-G Digital Power Amplifier for IoT Applications

Tong Li, Yun Yin, Yiting Zhu, Liang Xiong, Yangzi Liu, Na Yan, Hao Min, and Hongtao Xu

***Abstract*— This letter presents a wideband digital power amplifier (DPA) with Class-G technique to enhance back-off efficiency for Internet-of-Things (IoT) applications. The switched-capacitor power amplifier topology is adopted for high linearity performance. A wideband matching network is proposed to achieve 0.54–0.95-GHz frequency coverage for 802.11ah and narrowband IoT standards. The measurement results demonstrate a flat frequency response with only 0.5-dB power deviation over 0.54–0.95 GHz. The DPA achieves the peak output power of 23.5 dBm with 42.7% peak PAE and 32.8% PAE at 6-dB back off. When amplifying an 8-MHz 64 quadratic-amplitude modulation 802.11ah signal at 800 MHz, it obtains −28.4-dB error vector magnitude and 30.1% average PAE at 16.5-dBm average output power.**

***Index Terms*— 80211ah, class-G, digital power amplifier (DPA), efficiency enhanced, narrowband Internet of Things (NB-IoT), wideband.**

I. Introduction

THE emergence of Internet-of-Things (IoT) facilitates people's life enormously, which draws extensive attention from academia and industry in recent years. IEEE 802.11ah and narrowband IoT (NB-IoT) are newly proposed protocols for IoT applications, which are characterized by low cost, high energy efficiency, and wide sub-GHz frequency band (699–930 MHz) [1]. Besides, 470–698 MHz is recognized as a new band for 5G applications in U. S. In order to increase data rate and spectrum efficiency, orthogonal frequency division multiplexing modulations with high peak-to-average-power-ratio are widely adopted in IoT applications, making it necessary to enhance the back-off efficiency so as to extend battery life.

The power amplifier (PA) is a key component in the RF front end and is highly desired to be integrated on-chip for low-cost system-on-chip implementation. Compared with traditional analog PAs with high linearity but low efficiency [2], digital PAs (DPAs) benefit from the CMOS technology scaling, offer higher efficiency and are compatible with digital baseband. The current-mode DPA has been widely adopted [3], but it has the linearity issue due to the varying output impedance. In contrast, the voltage-mode switched-capacitor PA shows better linearity [4], [5]. Moreover, it is worth mentioning that the flatness of PA output power over operation band is critical for efficiency enhancement, since no bandwidth compensation technique or design margin is required, such as channel equalization or static power control, which makes the design challenging.

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The authors are with the State Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China (e-mail: yiny@fudan.edu.cn).

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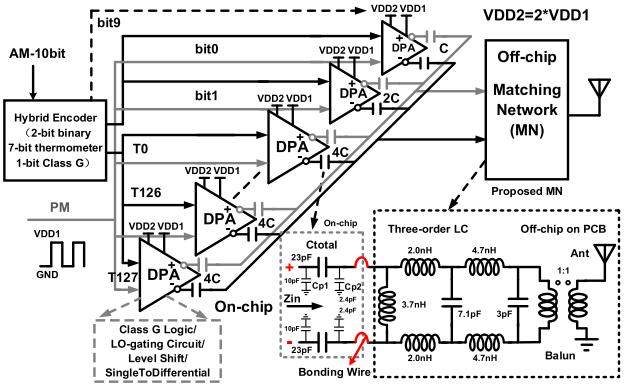

Fig. 1. Block diagram of the proposed wideband class-G DPA.

A wideband efficiency-enhanced DPA is proposed in this letter, which covers the whole sub-GHz band and boosts the back-off efficiency with class-G technique. In addition, the local oscillator (LO) gating is introduced to further improve the back-off efficiency. Detailed analysis and implementation are discussed in Section II. Section III shows the measurement results and makes a comparison with prior works, with Section IV drawing the conclusion.

II. Wideband Class-G Digital Power Amplifier

Fig. 1 shows the block diagram of the proposed wideband DPA with class-G technique. The switched-capacitor structure is adopted due to its good linearity. Taking into account, the noise floor and mask requirements of 802.11ah and NB-IoT, a 10-bit class-G DPA is implemented, where bit 9 is used to realize class-G operation between VDD1 and VDD2 to boost the 6-dB back-off efficiency, bit 8–bit 2 are thermometer-coded and bit 1–bit 0 are binary coded for fine resolution. The matching network is realized off-chip to avoid large inductance at sub-GHz band, and achieves wide bandwidth coverage and high-Q for better efficiency.

A. Wideband Matching Network

The fundamental voltage V_1 at the drain terminal of the DPA can be expressed as

$$V_1 = \frac{2}{\pi}\left(\frac{i}{N}\right)\mathrm{VDD2} \tag{1}$$

where N is the total number of unit cells in the array and i is the number of switched-ON cells. According to the Thevenin

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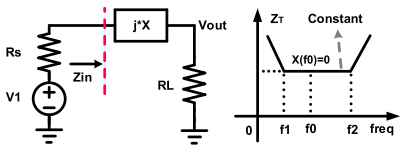

Fig. 2. Wideband matching network design based on the Thevenin equivalent circuit of the switched-capacitor PA.

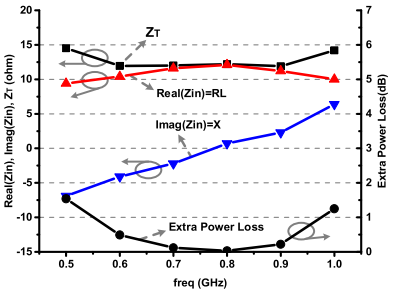

Fig. 3. Simulation results of output matching network over the frequency.

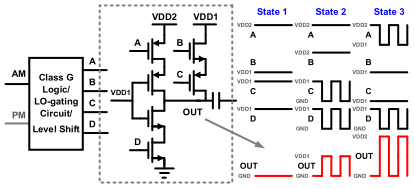

Fig. 4. Simplified single-ended schematic of the unit DPA cell and its three operation states.

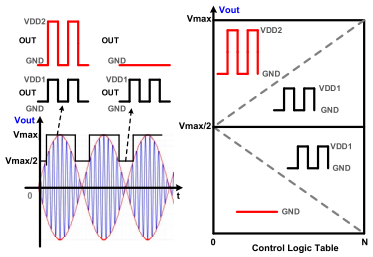

Fig. 5. Conceptual diagram of the class-G operation.

theorem of voltage-mode circuits, the DPA active part can be modeled as a voltage source V_1 with an internal resistor Rs, where Rs is the ON-resistance of all unit cells. The passive matching network is equivalent to a reactance $X(f)$ in series with a resistive load RL, as illustrated in Fig. 2. When $i = N$, the DPA peak output power can be derived as

$$P\text{out} = \frac{V\text{out}^2}{RL} = \frac{RL}{(Rs + RL)^2 + X(f)^2} \cdot V_1^2. \tag{2}$$

With $RL \geq 10Rs$ and substituting V_1, the DPA peak output power can be expressed as

$$P\text{out} \cong \frac{V_1^2}{2Rs + RL + \frac{X(f)^2}{RL}} = \left(\frac{2}{\pi}\right)^2 \cdot \frac{\text{VDD2}^2}{2Rs + RL + \frac{X(f)^2}{RL}}. \tag{3}$$

If $Z_T(f) = RL + (X(f)^2/RL)$ keeps constant between f_1 and f_2, the DPA output power would be flat over the frequency. But extra power loss and efficiency degradation are sacrificed, which can be calculated as

$$\text{Loss}_{\text{extra}} = 10 \cdot \log 10 \left[\frac{2Rs + Z_T(f)}{2Rs + RL}\right]. \tag{4}$$

As shown in Fig. 3, the extra power loss is <0.5 dB over 0.6–0.93 GHz and <1 dB over 0.55–0.95 GHz in comparison to an efficiency only optimized design.

Owing to area overhead and higher loss of on-chip matching network at sub-GHz, the proposed wideband matching network is implemented off-chip, as shown in Fig. 1. It consists of the parasitic capacitor ($Cp1$ and $Cp2$), the switched capacitors (C_{total}), three-order LC components that are tradeoff between bandwidth and efficiency, and a balun. By considering the parasitics of bondwire and printed circuit board (PCB) routing, the matching network is simulated and optimized through the Advanced Design System tool. As shown in Fig. 3, the equivalent resistance Z_T only varies from 12.1 to 11.4 Ω over 0.55–0.95 GHz, which corresponds to 400-MHz frequency span with only 0.5-dB deviation based on (3) in theory. The passive loss of the matching network is <1.45 dB over 0.5–1 GHz with only 0.15-dB deviation.

B. Class-G Switched-Capacitor DPA With LO Gating

It is well known that dynamic load modulation (DLM), Doherty, and class-G [5]–[8] techniques are widely employed to improve back-off efficiency. DLM requires switches and capacitor banks, and Doherty needs transmission lines or more than two transformers in the output matching network. Both techniques require various load impendence with power level, it is difficult to constantly maintain wideband operation at all power levels. The class-G technique boosts the back-off efficiency with supply switching and the wideband matching network can be optimized independently. It is the optimal choice to achieve the back-off efficiency enhancement and wideband operation simultaneously in our work. Fig. 4 shows the simplified single-ended schematic of the unit DPA cell, which consists of a class-G logic block to switch between different supply domains, an LO gating circuit, a level shifter that converts the input signal from low-voltage domain (GND-VDD1) to high-voltage domain (VDD1–VDD2). As shown in Fig. 4, each unit cell has three operation states depending on the output power.

State 1: When the OUT is held at GND, the A/B/C/D signals are held at VDD2/VDD1/VDD1/VDD1, respectively.

State 2: When the OUT is switched between GND and VDD1, the A/B signals are held at VDD2 while the C/D signals are switched synchronously between GND and VDD1.

State 3: When the OUT is switched between GND and VDD2, the A signal is switched between VDD1 and VDD2, the B/C signals are both held at VDD1, and the D signal is switched between GND and VDD1.

As shown in Fig. 5, the class-G operation is performed as follows: when output voltage $V\text{out}$ is less than $V\text{max}/2$, part of the unit cells will operate at state 1 while the others are at state 2; when $V\text{out}$ is larger than $V\text{max}/2$, the unit cells will be partitioned into states 2 and 3 accordingly. Moreover, the LO gating technique is employed between digital control words and LO signal to reduce the power dissipation of LO drivers to further enhance efficiency.

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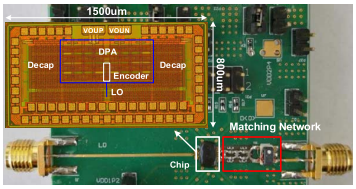

Fig. 6. PCB evaluation board and chip microphotograph.

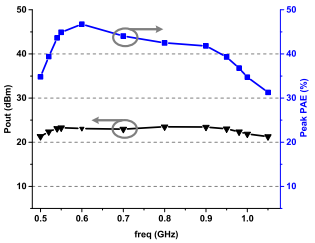

Fig. 7. Measured DPA frequency response.

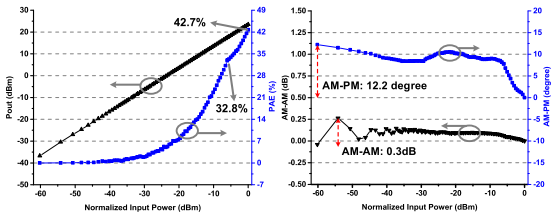

Fig. 8. Measured P_{out}, PAE, AM–AM, and AM–PM versus normalized P_{in} at 0.8 GHz.

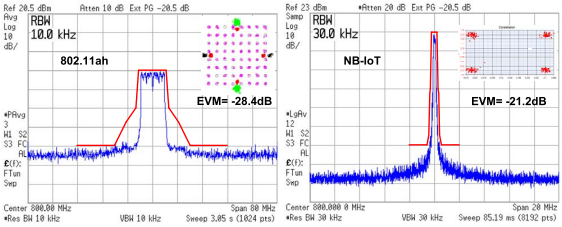

Fig. 9. Measured DPA spectral masks and constellations in 802.11 ah and NB-IoT.

III. Measurement Results

The proposed wideband class-G DPA has been implemented in 55-nm CMOS process. As shown in Fig. 6, it occupies an area of 1.5×0.8 mm^2 including all electro-static discharge I/O pads and is chip on board packaged on an FR-4 evaluation board. The DPA is powered by a pair of supplies 1.2/2.4 V. In the PAE calculation, the power dissipation of all drivers, logics, and DPA cells is included.

Figs. 7 and 8 show the measured DPA frequency response, output power, PAE, AM–AM, and AM–PM performance. The DPA achieves wide frequency coverage of 0.54–0.95 GHz with only 0.5-dB power deviation. Besides, it obtains the maximum peak PAE of 46.0% at 0.6 GHz and the maximum peak P_{out} of 23.5 dBm at 0.8 GHz. Owing to the class-G technique, an efficiency peaking at 6-dB back off is achieved, enhancing the average efficiency. The DPA obtains only 0.3-dB AM–AM distortion and 12.2° AM–PM distortion, which can be corrected by the digital predistortion (DPD).

In modulation tests, memory-less DPD lookup tables are used to linearize the DPA. As shown in Fig. 9, at 800 MHz, for an 8-MHz 64 quadratic-amplitude modulation 802.11ah signal, the DPA achieves an error vector magnitude of −28.4 dB with an average output power of 16.5 dBm and PAE of 30.1%. For a 180-kHz bandwidth 12-subcarrier NB-IoT signal, it achieves 34.0% average PAE at 18.8-dBm average output power, and satisfies the spectral mask requirement with enough margin.

TABLE I
COMPARISON WITH PRIOR IOT/CLASS-G PAS

	[2]	[3]	[4]	[5]	**This work**
RF Freq. (GHz)	0.75-0.93	0.75-0.96	0.75-0.93	1.75-2.25	**0.54-0.95**
0.5dB Bandwidth (MHz)	180**	210**	180**	150*	**410**
Matching Network	On-chip	Off-chip	Off-chip	Off-chip	**Off-chip**
Peak Pout (dBm)	13.6	24.2	8	24.3	**23.5**
Peak PAE (%)	25.5	28.9	45	44	**42.7**
6dB Back-off PAE (%)	8*	18*	25*	36*	**32.8**
Modulation Signal	LTE	π/ 4-DQPSK	802.11ah	802.11g	**802.11ah/ NB-IoT**
Average Pout (dBm)	8.9	19.1	0	16.8	**16.5/18.8**
Average PAE (%)	10*	NA	20*	33	**30.1/34.0**
EVM (dB)	-30.4	-26.1	-27.1	-30.7	**-28.4/-21.2**
Supply (V)	NA	2	1	1.4/2.8	**1.2/2.4**
Technology	180nm CMOS	180nm CMOS	40nm CMOS	65nm CMOS	**55nm CMOS**
DPD	Yes	Yes	No	No	**Yes**

* read from reported figures. ** estimated from supported RF frequency.

Table I makes a comparison with prior IoT/class-G PAs. This letter obtains the widest frequency coverage of 55% with only 0.5-dB power deviation. The PAE performance is also competitive at both peak and back-off powers when compared to other competitors.

IV. Conclusion

A wideband efficiency-enhanced DPA for IoT applications is presented in this letter. The class-G technique is introduced to enhance back-off efficiency, together with the LO gating to further improve the efficiency. With the optimized wideband matching network, the DPA achieves 0.54–0.95-GHz frequency coverage with only 0.5-dB power deviation. Moreover, it obtains superior performance in terms of output power, efficiency, and linearity.

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