Dynamic Feedback Linearizer of RF CMOS Power Amplifier

Seunghoon Kang, *Member, IEEE*, Eun-Taek Sung, *Student Member, IEEE*, and Songcheol Hong, *Member, IEEE*

***Abstract*— A dynamic feedback linearizer for an RF CMOS power amplifier (PA) is presented, which consists of a negative feedback network and a dynamic feedback control circuit to inject a reshaped envelope signal to the network. The linearizer compensates for the gain compression of the RF CMOS PA in high-power region by reducing the feedback dynamically, and it also reduces the amplitude-to-phase modulation (AM-PM) distortions. The PA including the linearizer was fabricated using a 0.18-μm RF CMOS process, which has an output transmission-line transformer on a printed circuit board. It delivers an output power of 28.1 dBm at 1.7 GHz with power added efficiency of 40.9%, and adjacent channel leakage ratio ($ACLR_{E-UTRA}$) of under −30 dBc for a 10-MHz 16-QAM long-term evolution signal without digital predistortions.**

***Index Terms*— CMOS, feedback, linearization, power amplifier (PA).**

I. Introduction

AS THE demand for cost-effective handheld systems with a rapid high-data-rate increase, there is a huge interest in CMOS PAs. However, designing a watt-level power amplifier (PA) with CMOS transistors is very challenging due to their low breakdown voltage, low substrate resistivity, and no substrate via hole to the ground. Differential cascode structures are commonly used in RF CMOS PAs to overcome these shortcomings. However, when nonconstant envelope signals such as quadrature amplitude modulation (QAM) signals enter the input of a PA, PA nonlinearities generate amplitude–amplitude modulation (AM–AM) and amplitude–phase modulation (AM–PM) distortions. These degrade its adjacent channel leakage ratios (ACLRs). Therefore, the linearization methods are introduced to make highly linear and efficient RF CMOS PAs, which include feedbacks, feedforwards, and digital predistortions [1]. While these are quite effective, additional complexity, chip area, and power consumption are not negligible for a handset PA. To overcome these problems, analog/RF predistortion linearizers are widely used because of their simplicity and low-power consumptions [2], [3]. These include nMOS transistors that operate as variable resistors according to average input power. In [2], the linearizer compensates for the AM–PM distortion caused by a nonlinear gate–drain capacitance (C_{gd}) of a common-gate (CG) amplifier in the high-output power region, but it does not improve the AM–AM distortion. In [3], the linearizer compensates for the gain compression that occurs in the high-output power region by reducing the feedback of a PA, but it does not affect the AM–PM distortion. This is because the linearizers are not adaptable to change their feedback resistances dynamically according to instantaneous input powers.

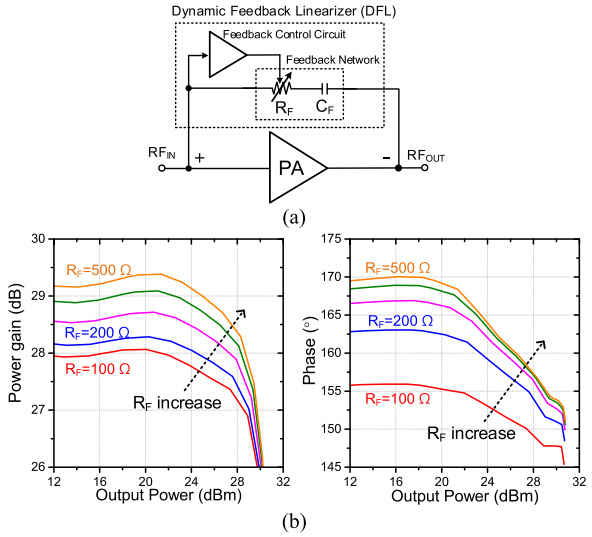

Fig. 1. (a) Conceptual block diagram of the PA with a DFL. (b) Gain and phase characteristics of the PA according to the R_F control.

In this letter, a dynamic feedback linearizer (DFL) is proposed to reduce the nonlinearity of a PA. It consists of a feedback network and a feedback control circuit, as shown in Fig. 1(a). The increase of R_F in the feedback network increases the power gain and phase of a PA, as shown in Fig. 1(b). Therefore, the appropriate control of R_F according to the input power can effectively linearize the gain compression and phase lag of a PA.

II. Dynamic Feedback Linearizer

A. Linearization of AM–AM

The proposed DFL consists of a negative feedback network and its control circuit, as shown in Fig. 2. Although the DFL looks similar to the previous feedback linearizer presented in [3], the method used to control the feedback voltages is different. Unlike the previous linearizer where V_{F1} is fixed, V_{F1} in the proposed linearizer is dynamically controlled by the RF input power. The control circuit, which consists of a nMOS

Manuscript received April 15, 2018; revised July 9, 2018; accepted July 27, 2018. Date of publication August 21, 2018; date of current version October 5, 2018. This work was supported in part by the Korea Government (MSIP) through IITP (Development on millimeter-wave beamforming IC for 5G mobile Communication) under Grant 2017-0-00409, in part by the Korea Government (MEST) under Grant 2017R1A2A1A05001361, in part by Samsung Electro-Mechanics Company Ltd., and in part by the IC Design Education Center. *(Corresponding author: Seunghoon Kang.)*

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Digital Object Identifier 10.1109/LMWC.2018.2861881

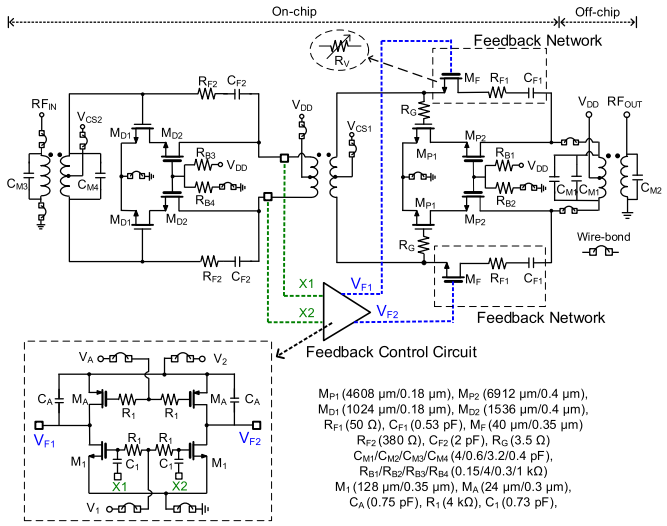

Fig. 2. Schematic of the PA with the proposed DFL.

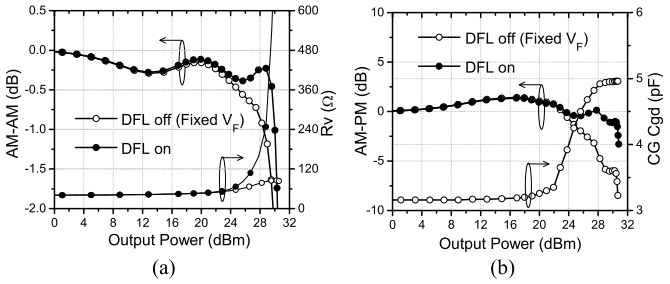

Fig. 3. (a) AM–AM and R_V versus output power with and without the DFL. (b) AM–PM and CG C_{gd} versus output power with and without the DFL.

transistor (M_1) with an R–C low-pass filter, detects the envelope of an RF input signal. When V_{F1} becomes lower than the source voltage (V_2) of the pMOS transistor (M_A) in the control circuit, it is designed to control the equivalent resistance (R_V) of M_F. The M_A helps the V_F to change faster when the input power increases. As a result, as shown in Fig. 3(a), the DFL achieves a steep slope of the R_V–P_{OUT} curve, which enables significant AM–AM linearity improvements.

To reduce the AM–AM distortion, predistortion linearizers are often implemented with cold-mode FETs due to their simple configurations and zero-power consumptions [3], [4]. The increase of the input power changes the operation modes of the cold-FETs from a triode to a saturation/cutoff mode, which leads to an increase in the equivalent resistance of the FETs. This increases the gain of a PA at a high output power, and its AM–AM distortion can be compensated. Here, large resistance variations of the control FETs are preferred to have enough linearization effects. However, because it is hard for previous linearizers to achieve drastically increasing resistances with the output powers, the resistance variations have to be designed to occur over a wider power range. This usually causes unwanted gain expansion (gain peaking) at a low output power.

B. Linearization of AM–PM

In a typical cascode CMOS PA, C_{gd} of a CG amplifier is the major nonlinear source to generate AM–PM distortions [5]. The nonlinear C_{gd} of a CG amplifier is

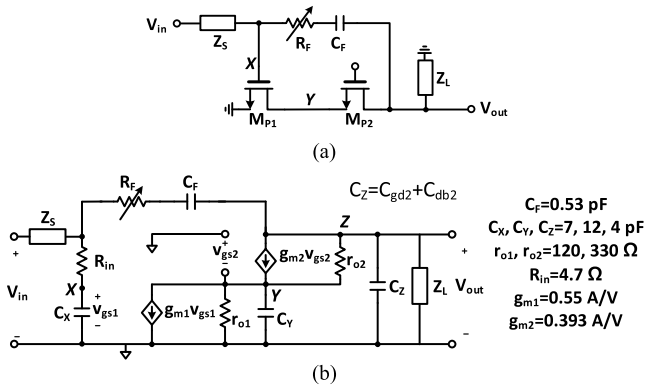

Fig. 4. (a) Simplified single-ended cascode PA with a negative feedback network. (b) Equivalent model of the circuit (a).

expressed as

$$C_{gd} = WC_{ov} \quad \text{(saturation)}$$
$$= WC_{ov} + WL_{eff}C_{ox}/2 \quad \text{(triode)} \tag{1}$$

where W, L_{eff}, C_{ox}, and C_{ov} are the width, effective channel length, gate oxide capacitance per unit area, and overlap capacitance per unit width, respectively. The average C_{gd} increases with the increase of the output power because the CG device enters the triode region, as shown in Fig. 3(b). An AM–PM distortion with steep phase lagging caused by the increased average C_{gd} degrades the ACLR.

As shown in Fig. 1(b), the increase of R_F makes a phase lead in the entire power range. To compensate a PA with a phase lag, the control circuit has to gradually inject a decreasing envelope signal to the gate of the feedback transistor M_F as the output power increases. This is exactly the same feedback control as in the AM–AM distortion control. Therefore, the proposed DFL can also greatly reduce both AM–PM and AM–AM distortions at the same time, as shown in Fig. 3(a) and (b).

Fig. 4 shows a simplified single-ended PA of a differential PA with a negative feedback network and its equivalent circuit model. The input and output matching networks are modeled by Z_L and Z_S, respectively. The common-source (CS) and CG amplifiers are modeled by voltage-controlled current sources $g_m V_{gs}$ and output resistances r_o. C_X, C_Y, and C_Z are the node capacitances. R_{in} is an input resistance. It is found in Fig. 4(b) that the dominant zero frequency of the cascode PA with the negative feedback network is the same as that of a CS amplifier with the feedback, which is given as

$$\omega_z = \{C_F(R_F - 1/g_m)\}^{-1} \tag{2}$$

where g_m is about 0.5 A/V in watt-level PAs, and R_F is in the tens to hundreds of Ohms (Ω). Because the R_F is greater than $1/g_m$, the zero appears in the left half-plane. In this letter, because the R_F gradually increases as the output power increases, the zero moves to the lower frequencies. In other words, the increase in R_F at a certain frequency causes phase-lead characteristics as shown in Fig. 5(a), which compensates for a PA with a phase-lag AM–PM. Fig. 5(a) shows the comparison of the transfer functions from the circuit simulation and its analytic model, which show a good agreement. From Fig. 5(b), the AM–PM distortion due to the increase of C_{gd} of CG amplifier can be minimized by the increase of R_F with output power.

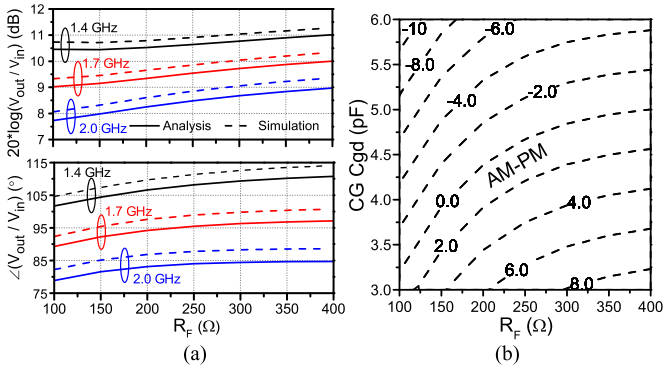

Fig. 5. (a) Magnitude and phase of the transfer function ($V_{\text{out}}/V_{\text{in}}$) of simplified PA in Fig. 4 versus feedback resistances (R_F) with various frequencies. Simulations with the analytical model (solid line) and the simulator model (dashed line). (b) AM–PM contours (dashed line) according to CG C_{gd} and R_F using the analytical model.

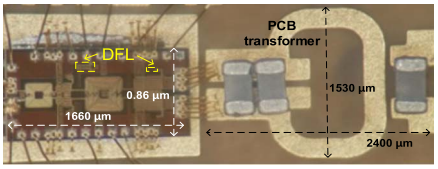

Fig. 6. Photographs of the proposed CMOS PA IC with the DFL and PA modules with a PCB transformer.

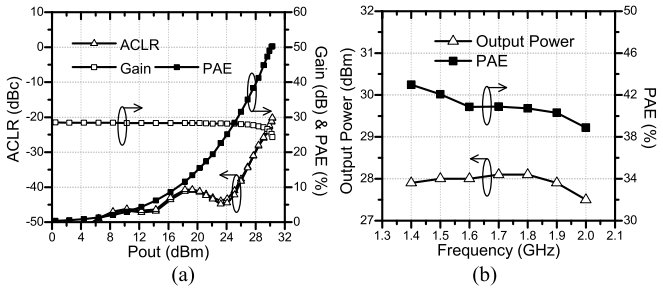

Fig. 7. Measurements using a 16-QAM 10-MHz LTE signal. (a) $\text{ACLR}_{\text{E-UTRA}}$, gain, and PAE versus the average output power at 1.7 GHz. (b) Output power and PAE satisfying an $\text{ACLR}_{\text{E-UTRA}} < -30$ dBc from 1.4 to 2.0 GHz.

III. Implementation and Measurement Results

Fig. 2 shows the schematic of the proposed PA with the DFL. The PA is designed as a two-stage amplifier to ensure a sufficient power gain. A differential cascode topology is used to reduce the ground bond-wire effect and to mitigate excessive voltage stresses on the power MOSFETs. The output network is implemented using a transmission-line transformer in a six-layer printed circuit board (PCB) transformer and surface mount device capacitors. Series resistors (R_G) at the gate of the CS amplifier not only stabilize the PA but also help the interstage matching because it reduces the required turn ratio of the matching transformer by increasing the PA input impedance. Fig. 6 shows the photographs of the fabricated RF CMOS PA integrated circuit (IC) with a 0.18-μm CMOS process and the PA module with the PA IC and the output PCB transformer.

Fig. 7(a) shows the measured $\text{ACLR}_{\text{E-UTRA}}$, gain and power-added efficiency (PAE) versus the average output power using a 16-QAM 10-MHz long-term evolution (LTE) signal at 1.7 GHz. The small signal gain is 28.5 dB, and the maximum output power that satisfies an $\text{ACLR}_{\text{E-UTRA}}$ under -30 dBc is 28.1 dBm with a PAE of 40.9%. Fig. 7(b) shows the measured performances of the PA using a 16-QAM 10-MHz LTE signal from 1.4 to 2.0 GHz. The PA achieves an output power of 27.5–28.1 dBm, a PAE of 38.9% to 43% with an $\text{ACLR}_{\text{E-UTRA}} < -30$ dBc from 1.4 to 2.0 GHz without any digital predistortions. Table I shows the comparison of the performance with those of the recently reported CMOS PAs for LTE applications.

TABLE I

Performance Comparisons of Recently Reported LTE CMOS PAs

Ref.	PA Process	Freq. (GHz)	P_{OUT} / PAE (dBm / %)	ACLR (dBc)	V_{DD} (V)	Feature
[6]*	180 nm	1.85	27.5 / 42.4	-36.5	4.0	Envelope Tracking
[7]+	40 nm	1.9	23.4 / 23.3	-30	1.5	Dual-mode Doherty
[8]*	90 nm	1.95	26.0 / 34.0	-33	3.7	EER
[9]+	130 nm	2.4	27 / 22.2	-32.1	3.3	Class-O
[10]*	130 nm SOI	0.7-0.9	26-28 /29-32	-33	3.3	Reconfigurable MMPA
This work*	180 nm	1.4-2.0	27.5-28.1 / 38.9-43	-30	3.3	Dynamic feedback linearizer

Measured with 16-QAM 10* / 20+ MHz bandwidth signal.

IV. Conclusion

A linearization method with DFL for an RF CMOS PA is proposed, which reduces the AM–AM and AM–PM distortions at the same time. The proposed PA has an output power of 28.1 dBm with a PAE of 40.9% and an $\text{ACLR}_{\text{E-UTRA}}$ under -30 dBc, which is comparable to the state-of-the-art CMOS PAs.

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