CMOS RF Power Amplifier for UHF Stationary RFID Reader

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***Abstract*—A CMOS power amplifier (PA) for a UHF (860–960 MHz) stationary RFID reader is presented. To design a high power and power efficient CMOS PA, quasi four pair structure and integrated passive device (IPD) transformers are used. An amplitude modulation is performed through the cascode gate with a pulse shaping filter. The chips are fabricated in a 0.18 μm CMOS process and IPD. Measurements show output power of 32.8–33.37 dBm and the power added efficiency (PAE) of 51.8–56.1% with the supply voltage 3.0 V.**

***Index Terms*—Class-E, CMOS RF power amplifier, integrated passive device (IPD), quasi four pair, stationary RFID reader.**

I. Introduction

With the recent increase in demand for stationary RFID readers that are used in logistics, shipping, and inventory control, there is a need to reduce their cost and size. To satisfy these industrial demands, power amplifiers (PAs) are required to be manufactured with the CMOS process because it is beneficial to integrate them with various digital control circuits in transmitters.

Stationary RFID readers require power efficiency as well as high output power since the PA consumes the highest power in the transmitter. Additionally, a high output power PA should have low harmonics in the desired frequency band to suppress interference with other application bands. In previous researches, the possibility of a CMOS PA has been successfully demonstrated [1], [2]. However it is still difficult to obtain high power and power efficiency with low harmonics compared with GaAs-based PAs due to the disadvantage of CMOS devices.

To overcome this problem, we chose a two chip solution of a CMOS PA and an integrated passive device (IPD) output transformer. An output transformer based on IPD technology has high quality factor. The advantage of IPD could successfully make up for the disadvantages of CMOS technology. Also, conventional RFID readers are based on I/Q transmitters with ASK modulation schemes with linear PA [Fig. 1(a)].

However, linear PA, especially in CMOS technology, suffers from poor efficiency. Therefore to have an efficient RFID reader, we designed a polar transmitter with a class E switching PA to have binary ASK modulation. Here, an analog pulse shaping filter to meet output spectral mask is introduced at the cascode common gate of the switching PA. This allows for a power efficient transmitter. [3] [Fig. 1(b)]

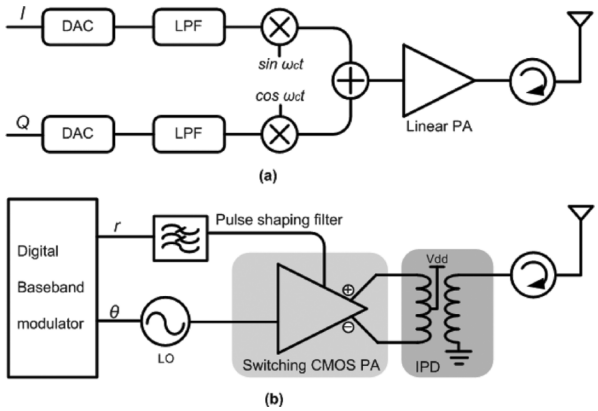

Fig. 1. (a) Conventional I/Q based RFID transmitter and (b) proposed polar RFID transmitter.

The presented CMOS PA has 54.9% PAE when the output power is 33.10 dBm at the center frequency of 910 MHz with 3.0 V V_{DD}. Also, the PA satisfies EPC global class-1 gen-2 [10] transmit mask regulation. The output power and power efficiency above 30 dBm and 50% are achieved when the binary ASK modulated signal is applied in common gate. To the best of the author's knowledge, the CMOS PA satisfies the requirements for stationary RFID reader application.

II. Implementation

A. CMOS Power Amplifier

The output power $P_{\rm OUT}$ of an ideal class-E amplifier is determined as follows by load impedance R_T, the supply voltage $V_{\rm DD}$, the number of amplifiers N, with efficiency of PA η [4]

$$P_{\rm out} = 1.365 \times \frac{V_{\rm DD}^2}{R_T} \times N \times \eta. \quad (1)$$

The increase in the number of amplifiers (N) seems to be the simplest way to achieve high output power. But if one increases N in conventional cascode PA structure, it results in complexities of input matching and large chip area. We designed the CMOS PA in a quasi four pair structure to achieve high power with low circuit complexity [5].

Fig. 2(b) shows designed CMOS PA schematics. Differential topologies (M1–M4) are used to suppress the source degeneration inductance effect by forming a virtual ground. Output nodes

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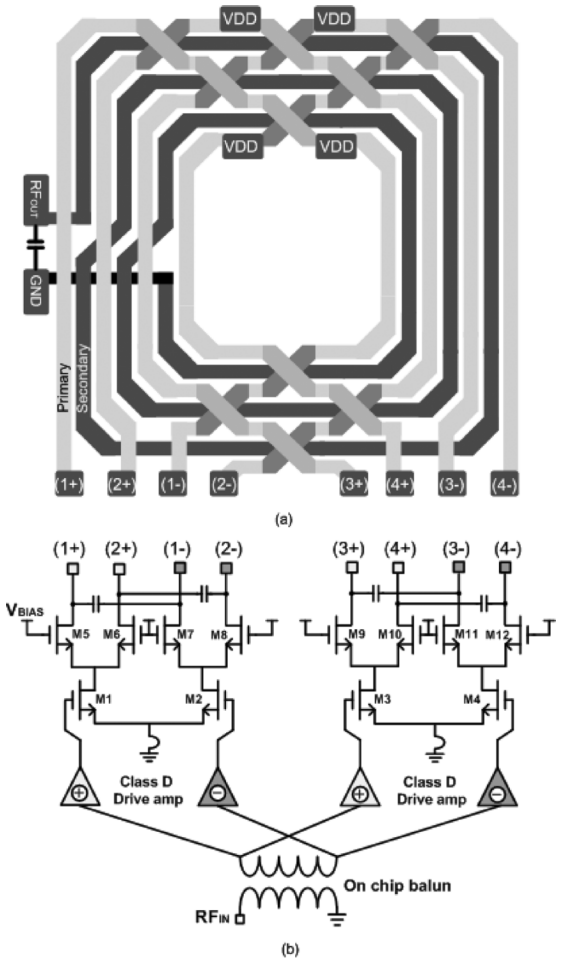

Fig. 2. (a) Output transformer in IPD technology. (b) Schematics of the power amplifier.

$(1+) \sim (4-)$ are connected by bonding wires with output transformer. All transistors, M1–M12, have the same transistor width of 4096 μm.

In the quasi four pair structure, paired CG stages have the same polarity. Therefore, it has difficulty in the layout of matching capacitors for the class-E amplifiers. In previous designs, capacitors are implemented in IPD and these cause additional poles with wire bonding inductance. As a result, it degrades the balance of power amplifier operation. The balance is a key factor in the design of differential PA because it is responsible for second harmonics rejection. In this work, the drain capacitors are laid as close to the drain of power transistors as possible in the Si chip. This structure improves the balance of switching amplifiers and allows low harmonic performances. Three stage class-D switch mode amplifiers configurations are used in drive amplifier design to reduce power consumption [6].

B. Output Transformer

Fig. 2(a) shows the designed output transformer. We designed the output transformer with the IPD process to obtain high efficiency at high power. This provides a high quality factor; therefore, the transformer design allows high transforming ratio with compact size. The current in the primary line of the output transformer connected to the drain of the cascode power amplifier induces current in the secondary line [7]. Each primary line has the same length and surrounds the transformer to keep the symmetry of differential amplifiers. $V_{\rm DD}$ pads implemented in the middle of the primary transformer line and output matching capacitor are implemented between output and the *GND* pad. The 2.5D EM simulator is used to obtain the optimum impedance of transformer. The maximum available gain (MAG) is simulated to check its performance. The simulated MAG is -0.37 dB at 910 MHz.

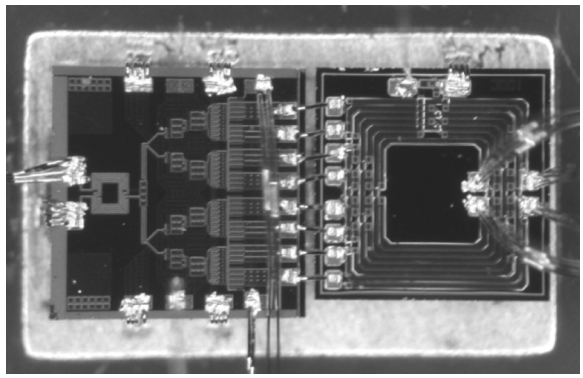

Fig. 3. Photograph of the implemented overall PA.

C. Pulse Shaping Filter (PSF)

RFID symbols, which come from digital baseband modulator, are represented by binary ASK modulation. However, digitally modulated on-off binary ASK signal induces high adjacent channel power of a desired band that restricts EPC global spec. To meet the specifications and obtain good, efficient performance with low complexity, the PSF is designed in Bessel fifth order low pass type that suppresses out of band component without distortion [3]. CMOS 0.25 μm process is used to implement and output voltage switching from 0.3 to 3.0 V.

III. Measurement Results

The chip photograph fabricated overall PA with 0.18 μm RF CMOS process and IPD process is shown in Fig. 3. Total chip area including bonding wire pads is 1470×1350 μm^2 for CMOS PA and 1300×1300 μm^2 for the output transformer. Fig. 4 shows the measured output power and PAE in the desired frequency 860–960 MHz with 3.0 V $V_{\rm DD}$ and 3.0 V cascode common gate bias with 5 dBm input power. Peak power is 33.37 dBm with 56.1% PAE at 860 MHz. The frequency band measurement shows output power above 32 dBm and 51% PAE, as shown in Table I [8], [9]. Fig. 5 represents the measured harmonics under the same input/output power level shown in Fig. 4. The 3rd harmonics show $-26 \sim -32$ dBc and the second harmonics are $-38 \sim -40$ dBc. It implies the harmonics are suppressed compared with previous work [5] by changing drain capacitor layout.

To confirm operation in RFID application, measurements are performed by binary ASK modulated signal, which was generated by a signal generator. A square like input signal is shaped by PSF and it enters cascode gate node. Fig. 6 shows the ACPR

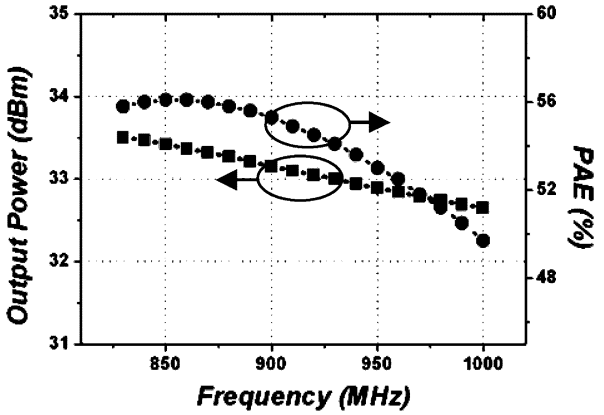

Fig. 4. Measurement of output power and PAE.

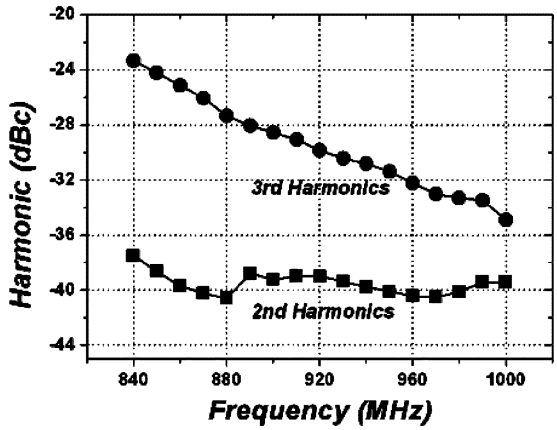

Fig. 5. Harmonics measurement.

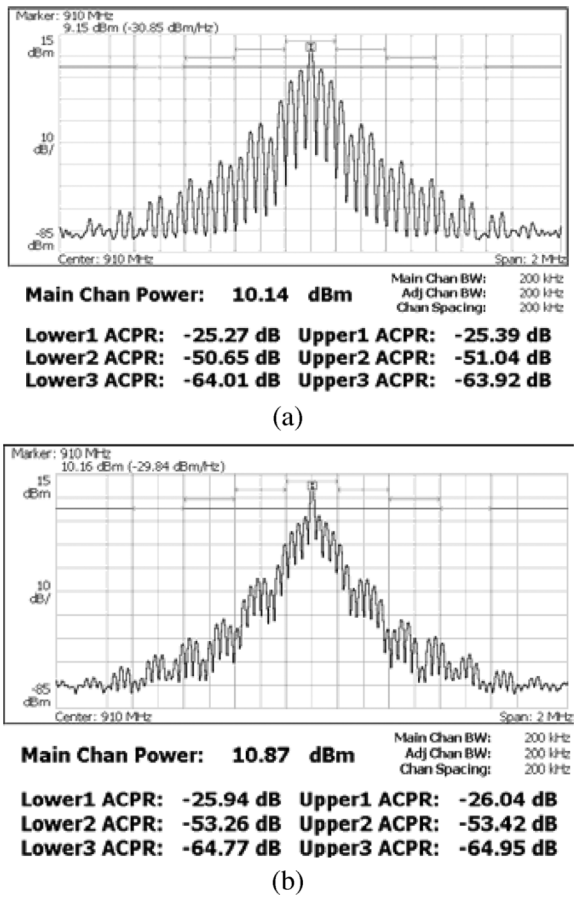

Fig. 6. Measured ACPR (a) data 0 input (b) data 1 input at 910 MHz.

TABLE I
COMPARISON OF OTHER PAS

Frequency (MHz)	P_{OUT} (dBm)	PAE (%)	Gain (dB)	Harmonics (dBc)	Tech	Ref
1710	33.7	50	20.7	-29	CMOS 0.18 μm	[5]
875	31.7	62.4	30.3	-33.9	CMOS 0.18 μm	[6]
900	29.5	41	-	-	CMOS 0.25 μm	[8]
960	32.5	55	-	-45	InGaP/GaAs HBT	[9]
860	33.37	56.1	28.37	-40	CMOS 0.18 μm	This work

and main channel power when data 0 and data 1 are applied to the input, respectively. As shown in the measurement results, all ACPR transmit mask specifications for RFID protocols are satisfied [10]. 30.13 dBm/30.86 dBm output powers and 53.47%/53.7% PAE are measured at center frequency with modulation. (data '0'/data '1').

IV. CONCLUSION

A CMOS power amplifier for a stationary UHF RFID reader is presented. High power and high efficiency are achieved by using a polar transmitter with CMOS switching PA. By considering capacitor layout, we can improve the balance of differential CMOS PA. PSF is introduced to the input to satisfy stationary RFID transmit mask. We obtain 54.9% PAE at 33.1 dBm output power. Also, 53.47% PAE, 30.14 dBm output power performances are achieved with data "0" input.

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