A 20-30 GHz High Efficiency Power Amplifier IC with an Adaptive Bias Circuit in 130-nm SiGe BiCMOS

Cuilin Chen[1], Xiao Xu[1], Xin Yang[1], Tsuyoshi Sugiura[2], Toshihiko Yoshimasu[1]

[1] The Graduate school of information, production and systems, Waseda University,
2-7 Hibikino Wakamatsu-ku, Kitakyushu-city, 808-0135 JAPAN

[2] Samsung R&D Institute Japan
2-7 Sugasawa-cho, Tsurumi-ku, Yokohama 230-0027, JAPAN

***Abstract* — A high efficiency broadband power amplifier IC is proposed for wireless communication systems. The power amplifier IC integrates an adaptive bias circuit which can adjust the collector current of SiGe HBT under large signal operation to improve the efficiency and temperature performance. The power amplifier IC is designed, fabricated and fully measured in 130-nm SiGe BiCMOS. The fabricated power amplifier IC has exhibited an output power of 14.6 dBm with a PAE of 43.8 % at a supply voltage of 1.4 V at 26 GHz. In addition, the power amplifier IC has an output power of over 12 dBm with a PAE of over 31.1 % from 20 to 30 GHz.**

***Index Terms* — SiGe BiCMOS technology, broadband power amplifier, adaptive bias circuit.**

I. INTRODUCTION

RF power amplifier (PA) ICs were reported with several technologies such as Si CMOS, GaAs and SiGe BiCMOS. Although Si CMOS is a cost effective technology, Si MOSFET suffers from the problems of low Johnson limit and low current density, which limits power handing capability and efficiency in high frequency PA ICs. GaAs HBTs and HEMTs have excellent performance at high frequency and high power applications. The fabrication cost, however, is much higher than those of Si and SiGe. The SiGe BiCMOS technology is attractive because of 1) higher performance than Si CMOS, 2) capability of high integration with Si CMOS digital circuits, 3) lower cost than GaAs process. Thus, SiGe BiCMOS technologies are suitable for microwave and millimeter-wave PA ICs. With a cut-off frequency of over 180 GHz, GLOBALFOUNDRIES 130-nm high-performance SiGe8HP technology is applied to design and fabricate the broadband PA IC proposed in this paper.

The voltage regulator as an adaptive bias circuit for SiGe HBT PA IC was previously reported in [1], [2]. However, the performance of the adaptively biased PA IC over the variation of temperature was not analyzed. In this work, a novel adaptive bias circuit is proposed by adding temperature compensation circuit to the voltage regulator reported in [2]. In addition, the output matching network is designed with Load-Pull simulations for high efficiency and broadband operation.

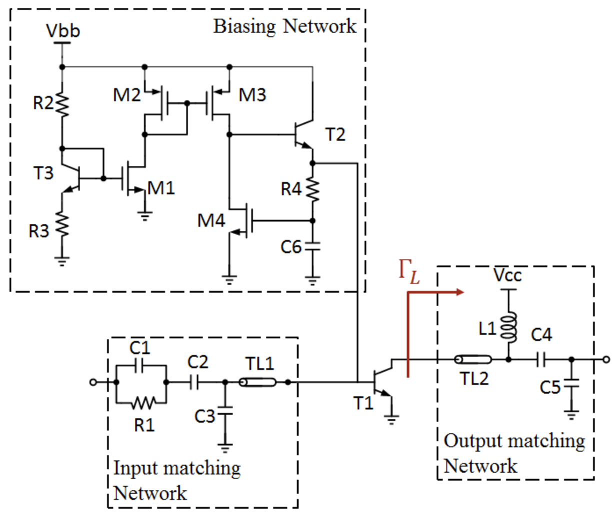


Fig. 1. Schematic of proposed PA IC with the novel adaptive bias circuit.

II. CIRCUIT DESIGN

A. Adaptive bias circuit with temperature compensation

Fig. 1 shows the schematic of the proposed PA IC with novel adaptive bias circuit. MOSFET M4 with a current source load M3 forms a feedback amplifier to keep the base-to-emitter voltage of RF HBT T1 constant [2]. With RF input power increasing, the base-to-emitter resistance of HBT decreases owing to the rectification of the base current. Since the bias circuit provides constant base-to-emitter voltage, the base and collector current of HBT T1 adaptively changes with input power changing.

MOSFETs M2 and M3 form the current mirror circuit to provide suitable bias current to M4. HBT T3 is employed to compensate the temperature performance of the power gain of HBT T1. The base-to-emitter bias voltage of HBT T1 (Vbe_T1) can be calculated as:

$$V_{be\_T1} = V_{TH} + (V_{gs\_M1} - V_{TH})\sqrt{W_1W_3L_2L_4 / L_1L_3W_2W_4} \quad (1)$$

where L1 - L4 and W1 - W4 are the gate length and the gate width of M1 - M4, respectively. VTH is the threshold voltage of nMOSFET. Vgs_M1 is the gate-to-source voltage of M1.

For simplicity, HBT T3 base current is neglected and the base-to-emitter voltage of T3 (Vbe_T3) satisfies that:

$$I_{C\_T3}(\mathrm{R}_2+\mathrm{R}_3)+V_{be-T3}=I_S exp\frac{V_{be-T3}}{V_T}(\mathrm{R}_2+\mathrm{R}_3)+V_{be-T3}=V_{bb}\quad(2)$$

where IC_T3 is the collector current of T3. When the temperature increases, IS significantly increases and Vbe_T3 decreases to meet the equation (2). Thus, IC_T3 increases and Vgs_M1 decreases. Resistor R3 is employed as emitter degeneration to control the Vbe variation of T3 with temperature variation.

It is well known that the transconductance of HBT is expressed as:

$$g_m=\frac{I_S}{V_T}exp\frac{V_{be}}{V_T}\quad(3)$$

When temperature increases, IS significantly increases and Vbe_T1 is decreased by the novel bias circuit. Thus, the gm of RF HBT T1 is kept constant and the gain of PA is flattened over the variation of temperature.

Fig. 2 shows the simulated Vgs_M1, Vbe_T1 and the gain of PA with sweeping the temperature from -25 to 125 ℃. It is confirmed that Vgs_M1 and Vbe_T1 decreases when temperature increases and the gain is almost constant.

Fig. 3 shows the simulated Vgs_M1, Vbe_T1 and the gain of PA over the variation of supply voltage of bias circuit (Vbb in Fig. 1). When Vbb increases from 2.4 V to 2.8 V, Vbe_T1 is slightly increased from 0.831 to 0.850 V.

B. Matching Network Design

The output impedance matching network is designed by Load-pull simulation, as shown in Fig. 4(a). In the output matching network, L1 and C4 are designed to be large size and C5 and TL2 have the main contribution to impedance transformation at 30 GHz. Fig. 4(b) shows the constant PAE contours (PAE=48 %) at frequencies of 20, 25 and 30 GHz. The black solid line is the impedance of the output network (Γ_L) from 20 to 30 GHz. Hence, it is expected that the PA has high efficiency performance at broad band operation.

A compact broadband network is designed for the input impedance matching of the PA IC. A low pass filter with a parallel capacitor C3 and a series transmission line TL1 is utilized for the 30-GHz band impedance matching. Considering that the current gain of HBT at several-GHz is high and may cause the PA unstable, a high pass filter with R1 and C1 is employed to stabilize the PA and to flatten the gain.

Fig. 5 shows the chip microphotograph of PA IC fabricated in GLOBALFOUNDRIES 130-nm high-performance SiGe8HP technology. The chip area is 0.60 mm2 including all pads.

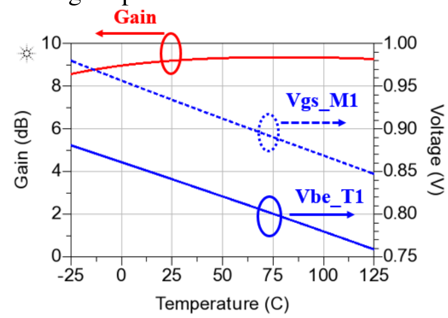


Fig. 2. Simulated Vgs_M1, Vbe_T1 and gain of PA with sweeping the temperature from -25 to 125 ℃.

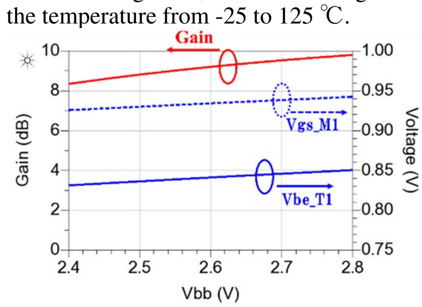
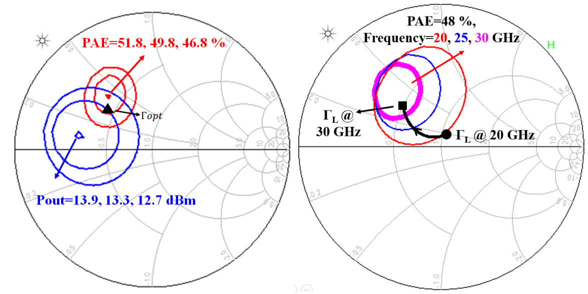


Fig. 3. Simulated Vgs_M1, Vbe_T1 and gain of PA with sweeping Vbb from 2.4 to 2.8 V.



(a) (b)

Fig. 4. (a) Load-pull simulation of PA under the input signal of 6 dBm and 30 GHz. (b) Constant 48 % PAE contours of PA with Pin=6 dBm at frequencies of 20, 25, and 30 GHz.

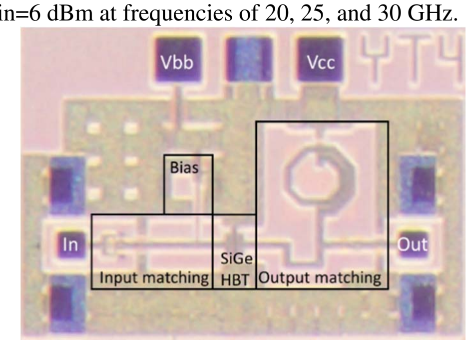


Fig. 5. The PA chip micrograph.

III. Measured Performance

Fig. 6(a) shows measured small-signal S-parameters of the PA IC at a Vcc of 1.2 V and a Vbb of 2.6 V. At 26

GHz, the forward gain is equal to 7.6 dB and the input and output return losses are 6.4 dB and 8.3 dB, respectively. The 3-dB gain bandwidth is from 6.0 to 37.7 GHz. Fig. 6(b) depicts the measured input-output response at 26 GHz. At a Vcc of 1.2 V, the PA IC exhibits a peak PAE of 40.9 % with an output power of 13.6 dBm. At a Vcc of 1.4 V, a peak PAE of 43.8 % with an output power of 14.6 dBm is obtained. Fig. 6(c) illustrates measured frequency response of the peak PAE and the output power at the peak PAE. From 20 GHz to 30 GHz, the peak PAE is higher than 31.1 % and the output power is over 12 dBm at a Vcc of 1.2 V.

The dependence of measured forward gain ($|S_{21}|2$) on Vbb is shown in Fig. 6(d). The forward gain changes from 6.3 to 8.5 dB with sweeping Vbb from 2.4 to 2.8 V. This gain variation is well agreed with simulated one shown in Fig. 3.

Table I summarizes measured performance of the proposed PA IC with previously reported broadband PA ICs [3-6]. The PA IC presented in this paper has exhibited wider 3-dB gain bandwidth with higher PAE and low supply voltage.

IV. Conclusion

A high efficiency broadband power amplifier IC has been demonstrated in 130-nm SiGe BiCMOS. From 20 to 30 GHz, the PA IC has an output power of over 12 dBm with a PAE of over 31.1 %. Moreover, the PA IC exhibits a peak PAE of 43.8 % at a low supply voltage of 1.4 V.

Acknowledgement

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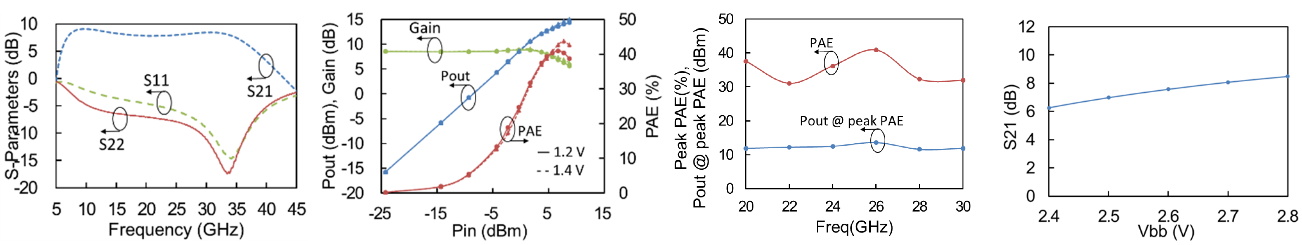

(a) (b) (c) (d)

Fig. 6. (a) Frequency response of measured S-parameters of the PA IC at a Vcc of 1.2 V and a Vbb of 2.6 V. (b) Measured output power, gain and PAE of the PA IC versus Pin at a Vbb of 2.6 V at 26 GHz. (c) Measured peak PAE and output power at the peak PAE from 20 GHz to 30 GHz at a Vcc of 1.2 V. (d) Measured S_{21} at 26 GHz with Vbb changing from 2.4 to 2.8 V.

TABLE I
SUMMARY OF MEASURED PERFORMANCE OF PROPOSED PA IC WITH PREVIOUS WORKS

Reference	Technology	3-dB gain band (GHz)	Gain (dB)	Pout @ peak PAE (dBm)	Peak PAE (%)	Supply voltage (V)	Supply voltage /#Device (V)	Chip area (mm^2)
This work	130 nm SiGe BiCMOS	6.0-37.7	5.5-8.5	13.6 @ 26 GHz	40.9 @ 26 GHz	1.2	1.2	0.60
		5.9-37.5	6.1-9.1	14.6 @ 26 GHz	43.8 @ 26 GHz	1.4	1.4	
[3]	130 nm SiGe BiCMOS	4.5-18	12.8-15.7	22.5 @ 8.5 GHz	31.9 @ 8.5 GHz	3.6	1.8	0.70
[4]	45 nm SOI CMOS	6-26*	5-6	21.7 @ 18 GHz	20.5 @ 18 GHz	4.5	0.75	0.52
[5]	130 nm GaAs mHEMT	10-23**	N/A	26.4 @ 18 GHz	33 @ 18 GHz	7.6	1.9	3
[6]	150 nm GaAs HEMT	17-35	9-12	22.2 @ 24 GHz***	40 @ 24 GHz	4	2	1.5

* 1-dB gain band ** 3-dB Output power band *** Output P1dB