Concurrent L- and S-Band Class-E Power Amplifier in 65nm CMOS

Ronghui Zhang[1], Mustafa Acar[1], Melina Apostolidou[1], Mark P. van der Heijden[1], Domine M. W. Leenaerts[1,2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

***Abstract*— A 65nm CMOS concurrent dual-band two-stage class-E power amplifier (PA) using high voltage extended-drain devices is presented. To implement sub-optimum class-E load impedance at L-band (1.0-1.3GHz) and S-band (2.8-3.1GHz), a concurrent transmission-line based dual-band output matching network is designed. The measurements show a drain efficiency (η) $> 61\%$ and a power-added efficiency (PAE) $> 50.5\%$ for L-band (1.0-1.3GHz) with a output power $P_{out} > 30.4dBm$. For S-band (2.8-3.1GHz) a $\eta > 42.6\%$ and a PAE $> 30\%$ with a $P_{out} > 28.9dBm$ are achieved. The output power variations are within 0.8dB and 1.6dB, respectively.**

***Index Terms*— Class-E, CMOS power amplifier, Dual-band**

I. Introduction

Modern radar systems need to operate at multiple bands, typically at L-band and S-band. In order to fulfill the multi-band requirements, current transmitter implementations are based on parallel power amplifier (PA) line-ups. New radar systems aim for single PA line-up to reduce size and cost. Although conceptually simple, practical design considerations place severe constraints and technology challenges on designing multi-band highly efficient PAs. In the last few years, various reconfigurable multi-band PAs have been reported. Some of them are based on electronic tunable components, such as voltage controlled varactors [1] or micro-electromechanical system (MEMS) devices [2] to implement a tunable matching network. However, varactor implementations suffer from distortion problems and MEMS usage is limited due to reliability issues. To address these issues, concurrent PAs with multi-band matching networks have been proposed [3], [4]. The PA can operate in all bands of interest simultaneously without any tuning components which reduces system complexity.

In this paper, a PA solution for dual-band operation is proposed using a concurrent class-E topology. Section II describes the design of the CMOS driver and power device. Then section III explains a design methodology that introduces a range of efficient sub-optimum class-E load conditions at L- and S-band. In section IV a concurrent dual-band output matching network is developed. Section V shows the overall circuit implementation and measurement results. Section VI concludes the proposed design.

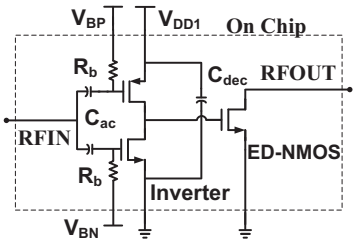


Fig. 1. Schematic of the realized CMOS PA.

II. CMOS power device and driver

Fig. 1 shows the schematic of the realized CMOS driver and power device. The output stage is formed by a dedicated high voltage, extended-drain, thick-oxide device (ED-NMOS), which is implemented in a standard 65nm CMOS technology without extra masks or processing steps [5]. The ED-NMOS transistor has an OFF-state breakdown voltage (BV_{DS}) of 15V. The total gate width of the ED-NMOS transistor is 7.68mm and the channel length is 0.28μm yielding an ON-resistance R_{on} of 0.7Ω, an OFF-resistance R_{off} of 10$k\Omega$, and an OFF-state output capacitance C_{ds} of 4.14pF. To drive the power output stage as a switch for class-E operation, a square-wave signal is generated by an inverter-based driver implemented using standard thick-oxide MOS devices with a gate length of 0.28μm. The inverter can deliver a 2.4 V_{pp} square-wave to the ED-NMOS transistor in broad frequency range.

III. Design methodology of dual-band class-E

The main challenge in dual-band PA design is to satisfy the requirements of efficiency and output power in both frequency bands. In practice it is not always possible to satisfy the optimum load conditions in all frequency bands considering a realistic matching network. Therefore the design space needs to be enlarged to obtain a required performance in both bands. One way to expand the design space is to use the sub-optimum class-E operation, i.e., non-zero switching voltage [6] and non-zero switching slope [7]. For sub-optimum class-E operation, the switch voltage $V_C(t)$ must satisfy the following two conditions:

$$V_C(t)|_{t=T} = \alpha V_{DD} \quad (1)$$

$$\left.\frac{dV_C(t)}{dt}\right|_{t=T} = k\omega V_{DD} \quad (2)$$

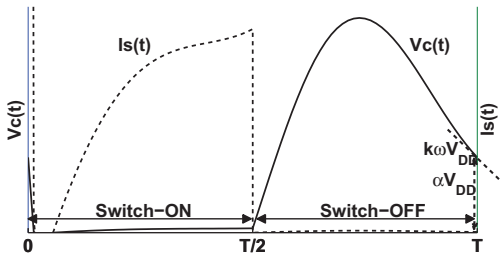


Fig. 2. Switch voltage and current of sub-optimum class-E PA.

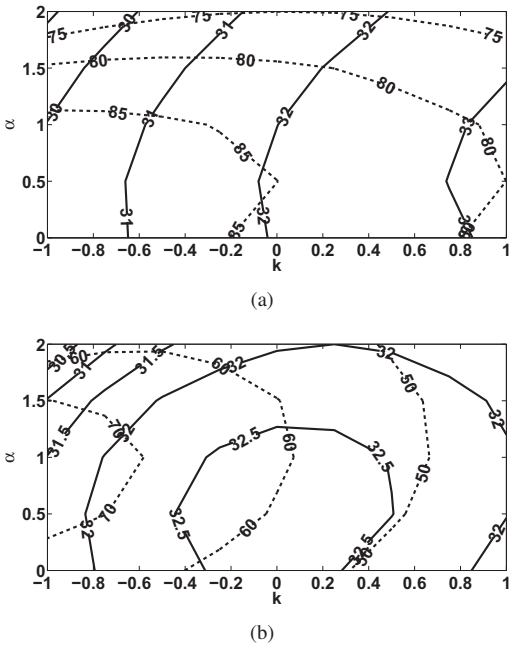


Fig. 3. Output power contours (solid lines) and drain efficiency contours (dashed lines) as functions of α and k at (a) 1.3GHz and (b) 3.1GHz.

where αV_{DD} is the voltage level of $V_C(t)$ and $k\omega V_{DD}$ is the slope of $V_C(t)$ at the moment the switch is closed ($t = T = 1/f_0$) shown in Fig. 2. Note that the operation mode is not limited to optimum class-E ($\alpha = 0$ and $k = 0$). By tuning α and k, more design space can be obtained which might relax the complexity of the matching network, especially for multi-band operation.

To effectively identify the expanded design space, which satisfies the requirements, the analytical design approach is applied [6], [7]. A design set K can be obtained[1], which enables us to calculate the values for the class-E circuit elements, by substituting the device parameters (R_{on}, R_{off} and C_{ds}), and the design targets (f_0, P_{out}) together with the class-E parameters (α and k) into the analytical design equations. The predicted RF performance

[1] $K_L = \frac{\omega L}{R}$, $K_C = \omega CR$, $K_P = \frac{P_{out}R}{V_{DD}}$, $K_X = X/R$

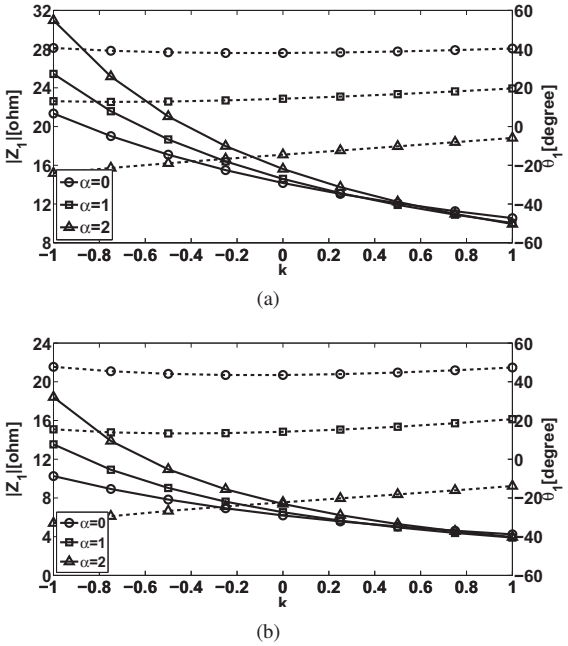


Fig. 4. Magnitude (solid lines) and phase (dashed lines) of Z_1 as functions of α and k at (a) 1.3GHz and (b) 3.1GHz.

is used to evaluate the usefulness of α and k for concurrent multi-band high-efficiency PA design.

For this design, the target output power and efficiency are +30dBm and 60% at 1.3GHz and 3.1GHz, respectively. Fig. 3 shows the simulated drain efficiency and output power as functions of α and k. At both frequencies, the circular contour lines of output power and efficiency are intersecting. Therefore, for the target efficiency and output power, a useful range of α and k can be defined, which is $0 < \alpha < 2$ combined with $-1 < k < 0$.

Fig. 4 shows the load impedances as functions of α and k. When tuning α, the phase of load impedance is changing while the magnitude remains constant. When α increases from 0 to 2, the load impedance changes from inductive loading to capacitive loading, which results in lower efficiency. Parameter k mainly controls the magnitude. As k increases, the magnitude of load impedance decreases which leads to higher output power. The magnitude for class-E operation at 1.3GHz is approximately two times larger than that at 3.1GHz, which is about their frequency ratio. Based on the analytical solutions in Figs. 3-4 and accounting for an optimal combination of output power (>30dBm), drain efficiency(>60%), and peak drain voltage, the optimum fundamental load impedance Z_1 range can be defined as

$$\begin{aligned} 8 < |Z_1| < 22 \\ -30^\circ < \theta_1 < +30^\circ. \end{aligned} \quad (3)$$

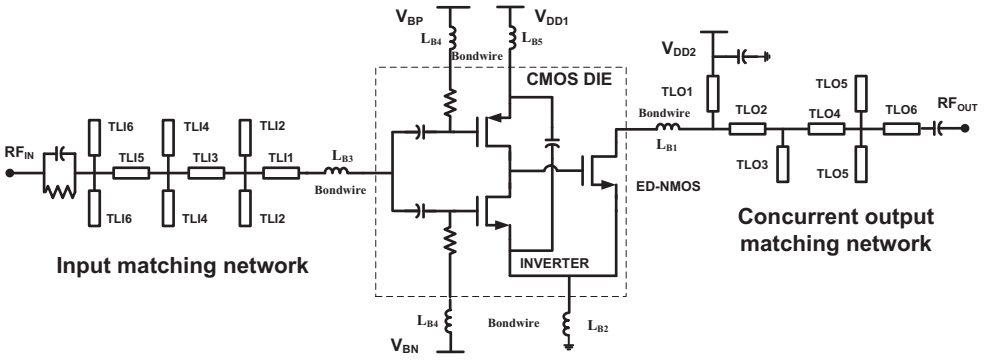


Fig. 5. Schematic of the concurrent dual-band PA.

TABLE I
SYNTHESIZED FUNDAMENTAL IMPEDANCE

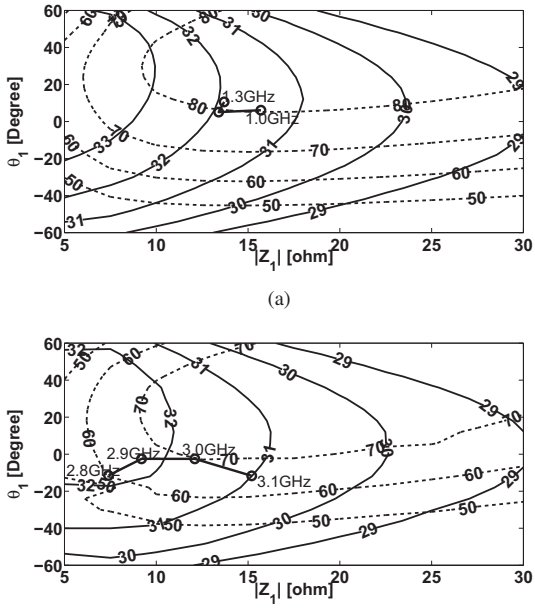
Freq. [GHz]	1.0	1.15	1.3	2.8	2.95	3.1
Z_1 [ohm]	16∠6	13∠5	14∠11	7∠-11	11∠-1	15∠-12

IV. Dual-band output matching network

The schematic of the concurrent dual-band PA is shown in Fig. 5. A two-stage transmission-line based output matching network is used to implement the required load impedance. The size of transmission lines is optimized using the harmonic-balance simulator in ADS. The optimization strategy is to set the optimization goal of magnitude and phase to the optimum range in (3) for both bands. In addition, the second harmonic impedances of both bands are controlled for a capacitive loading. Table I shows the synthesized fundamental load impedance. The performance of the synthesized PA can be verified by large-signal harmonic-balance simulations. Fig. 6 shows the simulated output power and drain efficiency without loss of the matching network in both frequency bands. For L-band, the synthesized PA can deliver more than 31dBm output power with a drain efficiency of 80%. For S-band, it can also obtain an output power of 31dBm with more than 60% drain efficiency.

V. Implementation and experimental results

Fig. 7 shows the photograph of the manufactured dual-band PA. The PCB size is 51×35 mm^2. The CMOS chip is mounted on a Rogers substrate with $\epsilon_r = 3.66$ and a thickness of 0.101mm. The bond wires are kept as short as possible to limit their influence on the desired load impedances. The power stage is biased at $V_{DD2} = 5.5V$ and the driver stage is biased at $V_{DD1} = 2.4V$. For L-band, +18dBm RF input power is used to drive the PA with fixed bias voltage of $V_{BN} = 1.4V$ and $V_{BP} = 1.2V$. To fully drive the PA at S-band due to lower gain, +22dBm RF input power is used with adjusted biasing: $V_{BN} = 1.2V$ and $V_{BP} = 1.4V$.



(a)

(b)

Fig. 6. Output power contours (solid lines) and drain efficiency contours (dashed lines) as functions of magnitude and phase of Z_1 at (a) 1.3GHz and (b) 3.1GHz. Line with circles shows the synthesized load impedance.

Fig. 8 shows the measured and simulated output power, power gain, drain efficiency, and PAE versus frequency at L- and S-band. For L-band, the measured output power shows an expected broadband characteristic from 1.0GHz to 1.3GHz, at a value between 30.4-31.2dBm. A power gain between 12.4-13.2dB is observed over the same frequency band. The drain efficiency and PAE stay above 61.2% and 50.5% across the same bandwidth. The peak drain efficiency of 63.5% and peak PAE of 53.2% are measured at 1.1GHz with 30.9dBm output power. At S-band from 2.8-3.1GHz, the output power varies from 28.9-

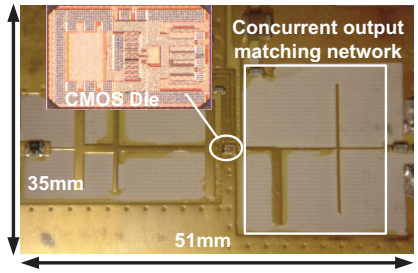
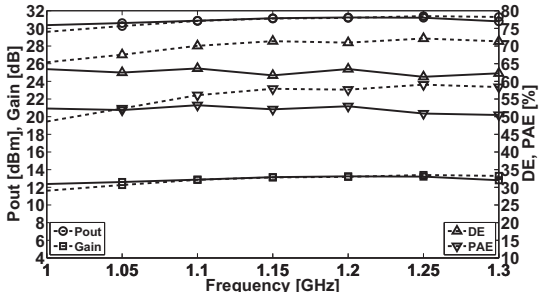


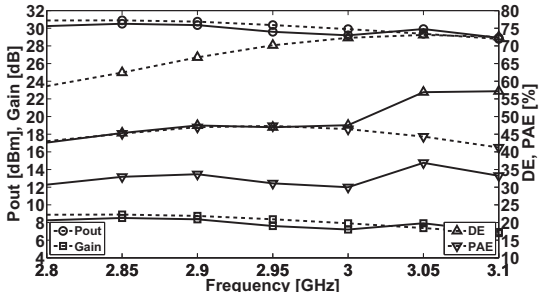
Fig. 7. Photograph of the concurrent dual-band PA.

TABLE II
COMPARISON DUAL-BAND PAS

	2011[3]	2008[4]	2009[8]	This work
Freq.[GHz]	1.4-1.6 3.0-3.9	2.4-2.6 3.3-3.4	2.45 3.8	1.0-1.3 2.8-3.1
P_O[dBm]	36.4-37.3 33.4-37.4	29.4-33 31.4-32.5	23.4 24.5	30.4-31.2 28.9-30.5
Gain[dB]	15.4-18 10.8-12	3-6.6 5-6.1	N.A.	12.4-13.2 6.9-8.5
DE[%]	43-48 41-56	40-53 40-46	42 39	61.2-63.5 42.6-57.0
PAE[%]	42-47 38-52	N.A.	N.A.	50.5-53.2 30.0-37.0
Technology	GaN	GaN	0.18um CMOS	65nm CMOS



(a) $V_{BN} = 1.4V$, $V_{BP} = 1.2V$, $P_{in} = 18dBm$



(b) $V_{BN} = 1.2V$, $V_{BP} = 1.4V$, $P_{in} = 22dBm$

Fig. 8. Measured (solid lines) and simulated (dashed lines) output power, power gain, drain efficiency, PAE versus frequency (a) L- and (b) S-band.

30.5dBm with a drain efficiency of more than 42.6% and a PAE of more than 30%. The peak drain efficiency of 57% and peak PAE of 37% are found at 3.05GHz with 29.9dBm output power. Over the second harmonic band of 2.0-2.6GHz at least 17dBc of harmonic suppression is obtained with respect to L-band (1.0-1.3GHz). The second harmonics outputs of S-band are 70dBc lower than the fundamental components. The discrepancy between simulation and measurement might be due to the limitation in ED-NMOS and bondwire model, especially at high frequency. Comparison of the realized PA's performance to state-of-the-art results for dual-band PAs is shown in Table II. The reported PAs in [3] and [4] make use of GaN devices for the implementation of a power stage, whereas in this study, a watt-level RF output power is drawn from standard CMOS devices with high drain efficiency at two frequency bands. The proposed design outperforms the dual-band CMOS solution in [8].

VI. CONCLUSION

A 65nm CMOS concurrent dual-band class-E PA is presented. The sub-optimum class-E operation is applied to broaden the optimum load impedance range. With a straightforward two-stage transmission-line based output matching network, the implemented PA achieves an output power of more than 30.4dBm and 28.9dBm with a drain efficiency of more than 61.2% and 42.6% at L- and S-band, respectively. The high efficiency at both bands makes the proposed concurrent CMOS PA very attractive for the reconfigurable phased-array transmitter solutions.

ACKNOWLEDGMENT

This research is conducted as part of the Sensor Technology Applied in Reconfigurable systems for sustainable Security (STARS) project (www.starsproject.nl). The authors gratefully acknowledge this support.

REFERENCES

[1] W. Neo *et al.*, "Adaptive Multi-Band Multi-Mode Power Amplifier Using Integrated Varactor-Based Tunable Matching Networks," *IEEE J. Solid-State Circuits,* vol. 41, no. 9, pp. 2166-2176, sept. 2006.

[2] L. Larcher, R. Brama, M. Ganzerli *et al.*, "A MEMS Reconfigurable Quad-Band Class-E Power Amplifier for GSM Standard," *in IEEE Micro Electro Mechanical Systems,* pp. 864-867, Jan. 2009.

[3] R. Liu, D. Schreurs, W. De Raedt *et al.*, "Concurrent dual-band power amplifier with different operation modes," *in IEEE MTT-S Int. Microw. Symp. Dig.,* pp. 1-4, Jun. 2011.

[4] P. Colantonio, F. Giannini *et al.*, "A Design Technique for Concurrent Dual-Band Harmonic Tuned Power Amplifier," *IEEE Trans. Microw. Theory Tech.* vol. 56, no. 11, pp. 2545-2555, Nov. 2008.

[5] J. Sonsky, A. Heringa *et al.*, "Innovative High Voltage transistors for complex HV/RF SoCs in baseline CMOS," *in IEEE VLSI Technology, Systems and Applications*, pp. 115-116, 2008.

[6] M. Acar *et al.*, "Variable-Voltage Class-E Power Amplifiers," *in IEEE MTT-S Int. Microw. Symp. Dig.,* pp. 1095-1098, Jun. 2007.

[7] M. Acar *et al.*, "Generalized Analytical Design Equations for Variable Slope Class-E Power Amplifiers," *in IEEE ICECS*, pp. 431-434, Dec. 2006.

[8] Y. Yoon, H. Kim, J. Cha *et al.*, "Fully-integrated concurrent dual-band CMOS power amplifier with switchless matching network," *Electronics Letters,* vol. 47, no. 11, pp.659-661, May 2011.