Voltage Mode Doherty Power Amplifier

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***Abstract*— This paper presents a new wideband Doherty amplifier technique that can achieve high efficiency while maintaining excellent linearity. By modifying a "forgotten" topology originally proposed by Doherty, a new Doherty amplifier architecture is realized with two voltage mode power amplifiers (PAs) and transformers, thus eliminating a narrowband impedance inverter. The voltage mode PA is implemented using switched capacitor PA techniques. The PA is fabricated in 65-nm low-leakage CMOS and achieves 24-dBm saturated power (at the standard supply voltage) with PAE of 45% at peak power and 34% at 5.6-dB back-off over 750 to 1050 MHz 1 dB bandwidth. With memoryless linearization, the PA can transmit 40 MHz 256-QAM 9 dB peak-to-average power ratio 802.11ac modulation centered at 900 MHz meeting the spectral mask with measured EVM of −34.8 dB and 22% PAE without backing off or equalization.**

***Index Terms*— Broadband, CMOS integrated circuits, Doherty power amplifier (PA), linearity, polar modulation.**

I. Introduction

IN MODERN communication systems, the need for high spectral efficiency and wide bandwidth has led to the use of high peak-to-average power ratio (PAPR) modulation approaches. With these signals, conventional power amplifier (PAs), having only high efficiency at peak power level, are no longer sufficient to maintain high overall efficiency [1]. Moreover, achieving an acceptable bit-error rate for spectrally efficient modulation puts a stringent linearity requirement on the PA. For example, the 802.11ac standard requires overall transmitter error-vector magnitude of better than −32 dB when transmitting 256-QAM symbols [2].

Efficiency enhancement techniques, such as envelope tracking [3], outphasing [4], and Doherty [5], have been developed to address the back-off efficiency problem. All of these techniques typically require significant memory-based polynomial correction [6] for use with modern wideband standards, limiting up to now their practical use to base stations.

The goal of this paper is to achieve wideband high back-off efficiency while maintaining excellent linearity, suitable for modern modulations, using only simple memoryless correction. This paper describes a CMOS PA implemented as a voltage mode Doherty (VMD) to address the issues of back-off efficiency enhancement. To meet these goals in CMOS technology, the architecture eliminates the narrowband impedance inverter used in a conventional Doherty PA. In the following, prior work in high efficiency PA architectures is briefly described, followed by a description of the VMD architecture proposed here and its detailed analysis. Experimental implementation and measurement results are then presented.

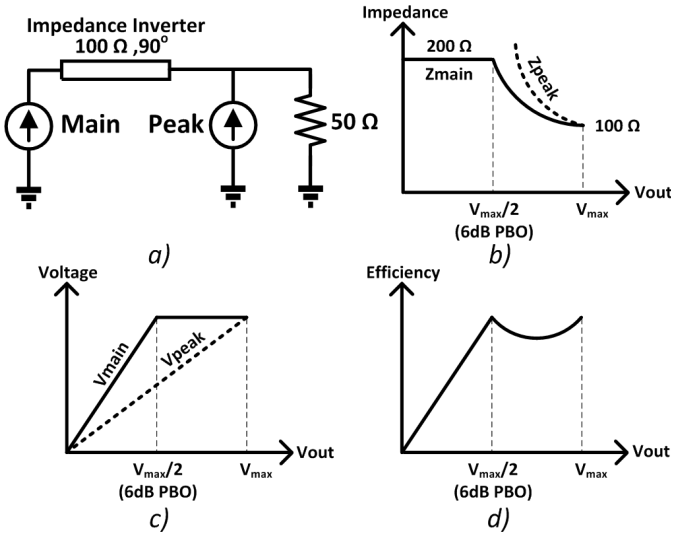

Fig. 1. (a) Classical Doherty PA. (b) Impedance seen by main and peaking PAs. (c) Voltage swing at main and peaking PAs. (d) Overall efficiency versus voltage swing at the load.

II. Previous Architectures

The classical Doherty PA [5] is composed of main PA, peaking PA, and impedance inverter, as shown in Fig. 1(a). At low power, the peaking PA is OFF, and the impedance inverter presents a high impedance [Fig. 1(b)] to the main PA. This causes it to saturate "early" resulting in an efficiency peak at 6-dB back-off [Fig. 1(c) and (d)]. From 6-dB back-off to full power, the peaking PA starts to turn on, and the active load modulation of the peaking PA and impedance inverter causes the impedance presented to the main PA to decrease [Fig. 1(b)]. This allows the main PA to provide more power to the load, while it remains in saturation, and thus, high efficiency is maintained from 6-dB PBO to peak power, as shown in Fig. 1(d).

A well-known problem in the classical Doherty PA is its relatively narrow bandwidth. At peak power, the impedance inverter behaves like a through-transmission line and thus does not limit the overall bandwidth of the PA [7]. At 6-dB back-off, however, the impedance inverter inverts the impedance from 50 to 200 Ω. This significantly limits the bandwidth of the 6-dB efficiency peaking [7]. Several techniques [7]–[9] have been shown to improve the bandwidth of impedance inverter. A different approach is taken in this paper, eliminating the impedance inverter to improve the overall bandwidth.

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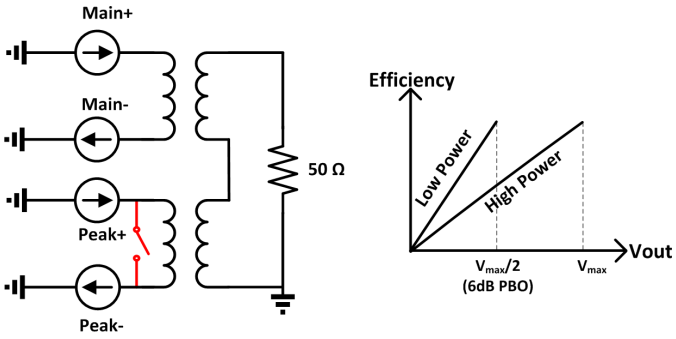


Fig. 2. Circuit for Doherty-like efficiency enhancement using transformers and switch, and its schematic efficiency vs output voltage swing at the load.

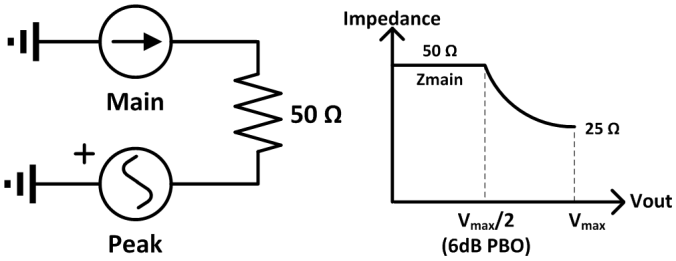


Fig. 3. "Forgotten" schematic (current–voltage Doherty) and its corresponding load modulation for the main PA.

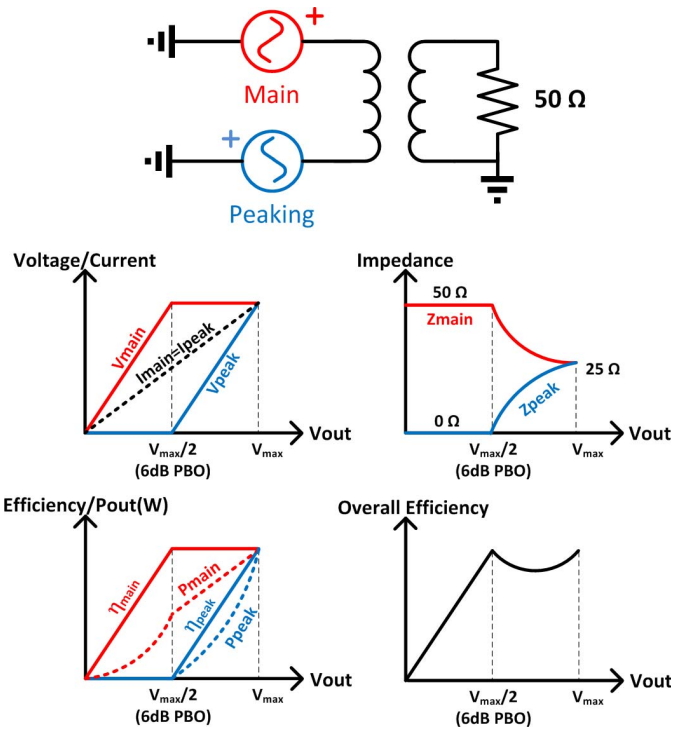


Fig. 4. Voltage mode Doherty schematic, and corresponding voltage and current trajectories, and impedances for the main/peaking PAs. Also shown is the overall efficiency vs output voltage swing at the load.

A number of alternative Doherty-related PA architectures have been proposed in CMOS to improve back-off efficiency utilizing baluns to perform power combining as well as load modulation. These techniques typically require the use of a large switch (Fig. 2) to move from low power to high power [10], [19], or a small core inductance in one of the balun transformer's primaries [11]. A large switch can limit bandwidth and also introduces discontinuities in the dc current of both amplifiers leading to memory effects. A small core inductance will work in place of a switch at low power levels, but forms a low impedance shunt element for the peaking PA, limiting the peak power bandwidth [12].

In Doherty's seminal paper [5], he begins by showing that active load modulation between a current source (main PA) and voltage source (peaking PA), in series with a load (Fig. 3) can provide back-off efficiency enhancement. We term this architecture the current–voltage Doherty. At low power, the voltage source is fixed at 0 V, and the current source sees the load impedance directly. When the voltage swing of the current source saturates, the voltage source begins to produce an antiphase voltage with increasing magnitude. This voltage swing on the opposite side of the load allows the current, and hence power, of the current source to continue to increase, while its output voltage remains at the saturation level, maintaining high efficiency. This architecture offers two potential benefits over the conventional Doherty PA, particularly in CMOS. Namely, there is no bandwidth-limiting impedance inverter, and the voltages of the two amplifiers are added in series, allowing for increased output power in scaled technologies without additional impedance matching.

While this architecture achieves the same active load modulation as the classical Doherty PA, a high efficiency RF voltage source was not realizable at the time. Doherty then proceeded to introduce an impedance inverter to allow implementation with only current sources. His initial architecture, however, inspires the VMD architecture, which only contains voltage sources as described here.

III. Proposed Architecture

By replacing the main PA in the current–voltage Doherty with another voltage source, we arrive at the VMD architecture, which contains only voltage sources. This is shown in Fig. 4, where the series load is replaced by a transformer balun driving a single ended load. The principle of operation is as follows: at low power, the peaking PA is OFF providing a short circuit at the bottom side of the primary of the balun. Under this condition, the main PA sees the load impedance R_L and saturates at 6-dB back-off. The peaking PA is then turned on, driving the balun in antiphase relative to the main PA and giving $V_{\text{load}} = V_m + V_p$ (where V_{load}, V_m, and V_p are voltage amplitudes at the fundamental for load, main, and peaking PAs), as well as increasing the current through the main PA. While the current provided by the main PA increases due to the peaking PA, the voltage the main PA presents to the balun does not increase, so the impedance seen by the main PA decreases as $R_m = R_L/(1 + V_p/V_m)$. This allows the main PA to provide more power to the load while remaining in saturation, and maintains overall high efficiency from 6-dB back-off to peak power. The efficiency versus output power is similar to the classical Doherty PA when Class-B back-off is assumed for the voltage-mode PAs.

Since this architecture does not rely on frequency-dependent components to provide active load modulation, the voltage

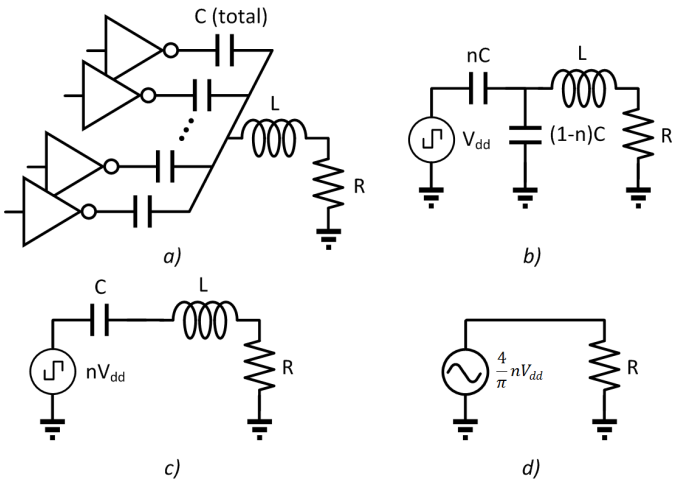


Fig. 5. (a) Circuit schematic for switched capacitor PA, and simplified equivalent circuits (b-d) as described in text. n is the fraction of ON unit cells.

mode Doherty has the potential to achieve wide bandwidth, limited by the voltage mode PA and transformer implementation. Moreover, since the output voltage of the voltage mode PA can be precisely controlled all the way to saturation, the turn-on point of the peaking PA for efficiency peaking is well defined and unchanged across frequency. This is unlike a typical current-mode PA, which exhibits compression near saturation of the main amplifier at 6-dB back-off, and at peak power. Additionally, in the classical Doherty, the saturation level is indirectly controlled by current, thus as the impedance seen by main PA changes across frequency, the optimal peaking PA turn-on point and gain also change [13].

The voltage-mode amplifier can be efficiently realized at gigahertz frequencies with a switched capacitor PA (SCPA) [14]. In an SCPA, the voltage-mode class-D PA is segmented into smaller unit cells, and the output voltage is digitally controlled by turning on a subset of the unit cells, as shown in Fig. 5(a).When a unit cell is ON, its voltage switches between ground and supply via the low impedance paths of a CMOS inverter. When the unit cell is OFF, the capacitor is tied to ground via the nMOS transistor of the inverter. If n is the fraction of "ON" unit cells, the SCPA circuit can be simplified to a capacitive divider, as shown in Fig. 5(b). The circuit can be further simplified to Fig. 5(c), which reveals that the impedance looking into the capacitor bank is constant regardless of the state of the SCPA. Resonating out this capacitor bank with a series inductor gives an ideal voltage mode PA at center frequency, as shown in Fig. 5(d).

The loaded quality factor of the series resonator $Q_L = 1/(\omega C R)$ [with C and R defined in Fig. 5(a)] can be designed to be about unity, which provides wide bandwidth, and slightly better than class-B power-added efficiency (PAE) at back-off [14]. Excellent capacitor matching in the CMOS technology provides the SCPA architecture with superior linearity [14], making it an ideal choice for voltage sources in a VMD implementation.

IV. Detailed Analysis

We first present generalized equations for efficiency and output power with arbitrary amplitude for each of the two SCPAs in the structure of Fig. 6(a). From this, we examine the specific cases of a differential SCPA and a VMD, to demonstrate the back-off efficiency enhancement realized with the VMD.

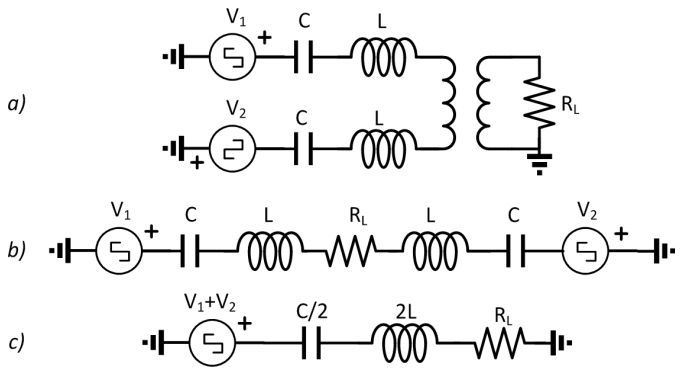


Fig. 6. (a) Circuit schematic for two SCPAs connected across a transformer, and simplified equivalent circuits (b-c) as described in text.

A. Generalized Efficiency

We will assume that regardless of amplitude, SCPA1 and SCPA2 operate in antiphase. The loss due to ON-resistance, switching loss of the capacitor bank driver, and matching network insertion loss will be ignored in this section. The output voltage and power can be written as

$$V_{\text{out}} = \frac{2}{\pi} V_{\text{dd}} (n_1 + n_2)$$
$$P^0_{\text{out}} = \frac{V^2_{\text{out}}}{2R_L} = \frac{2}{\pi^2} \frac{V^2_{\text{dd}}}{R_L} (n_1 + n_2)^2$$

where n_1 and n_2 are the fraction of "ON" unit cells in SCPA1 and SCPA2, respectively. At the voltage transitions, the inductor in Fig. 5(b) appears as an open circuit due to the fast rising/falling edges of the driver. Thus, the capacitance being charge/discharged by each SCPA is $n(1-n)C$ [14]. This gives a capacitive divider loss of $n(1-n)CV^2_{\text{dd}}f$.

Then, the overall loss can be written as

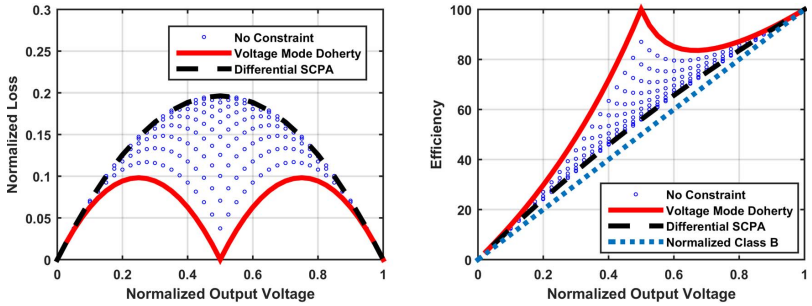
$$P_{\text{cd}} = P_{\text{cd},1} + P_{\text{cd},2} = [n_1 (1-n_1) + n_2(1-n_2)]\, CV^2_{\text{dd}} f$$

and the efficiency is

$$\eta = \frac{P^0_{\text{out}}}{P^0_{\text{out}} + P_{\text{cd}}} = \frac{1}{1+\frac{P_{\text{cd}}}{P^0_{\text{out}}}} = \frac{1}{1+\frac{\pi}{2}\frac{1}{Q_L}\frac{n_1(1-n_1)+n_2(1-n_2)}{(n_1+n_2)^2}}.$$

Here, the term $\omega R_L C$ is replaced by loaded quality factor $Q_L = 1/(\omega R_L (C/2))$ of the overall structure as shown in Fig. 6(c), which is independent of the state $(n_1,\ n_2)$. Note that the capacitive divider loss relative to the output power is independent of process technology and operating frequency.

The efficiency equation indicates that increasing Q_L reduces the capacitive divider loss in SCPAs resulting in reduced efficiency droop between peak power and 6-dB back-off, and better efficiency roll-off beyond 6-dB back-off. However, increasing Q_L reduces bandwidth, increases voltage swing in the capacitor bank, and produces higher insertion loss due to finite inductor quality factor. To maintain wideband operation and low insertion loss (if on-chip transformer was to be used) and to reduce voltage stress in the MIM capacitor bank, a low value of Q_L is favored; Q_L is held near 1 in this design.



a) *b)*

Fig. 7. (a) Capacitive divider loss normalized to peak output power and (b) corresponding efficiency versus normalized output voltage for different choices of ACWs n_1 and n_2 with $Q_L = 1$. Choices corresponding to the differential SCPA and the VMD are shown in bold; additional choices are shown with open circles.

B. Back-Off Efficiency Enhancement of VMD

For simple differential operation of the SCPA pair, both SCPAs present the same voltage to the load, and $n_1 = n_2 = n$. The above equation can be readily simplified to yield the efficiency versus output power.

For VMD, the choices of n_1 and n_2 are made to ensure SCPA1 reaches saturation first, at which point SCPA2 turns on (Fig. 4). More precisely

$$n_1 = \begin{cases} 2n \text{ for } n \leq 0.5 \\ 1 \text{ for } 0.5 < n < 1 \end{cases}$$

and

$$n_2 = \begin{cases} 0 \text{ for } n \leq 0.5 \\ 2(n-0.5) \text{ for } 0.5 < n < 1 \end{cases}$$

As shown in Fig. 7(a), the choice of (n_1,n_2) affects the loss in the capacitive dividers. The VMD reduces the peak loss in the capacitive divider by half. We can see that the loss in capacitive divider vanishes at half output voltage, and as shown in Fig. 7(b), this results in efficiency peaking at 6-dB back-off, similar to the class-G SCPA architecture [15]. As indicated by the circles of Fig. 7, amongst all arbitrary combinations of (n_1, n_2), the VMD provides the lowest capacitive divider loss and, thus, the optimum choice of (n_1, n_2) for two SCPAs across a transformer.

C. Voltage Mode Doherty With Nonideal Components

At gigahertz frequencies, in addition to the capacitive divider loss of the SCPAs, it is important to consider matching network insertion loss, conduction loss, and switching loss.

The conduction loss can be modeled as the ON-resistance of the SCPA drivers, R_{ON} (Fig. 8). The added resistance reduces the voltage amplitude seen at the input to the matching network by a factor of $1/(1 + 2R_{\text{ON}}/R_L)$, which reduces the power presented to the matching network, relative to ideal driver with $R_{\text{ON}} = 0\Omega$, to $P'_{\text{out}} = P^0_{\text{out}}/(1 + (2R_{\text{ON}}/R_L))^2$. However, the conduction loss in the switch is less than the output power reduction, as the addition of R_{ON} reduces the current through the switching transistors. Since R_{ON} is in series with the load, the power loss in the ON-resistance of the SCPA drivers relative to the power delivered to the matching network is $P_{\text{cond}}/P'_{\text{out}} = 2R_{\text{ON}}/R_L$.

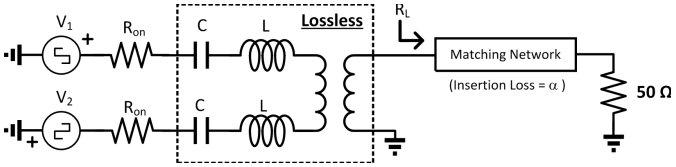


Fig. 8. Equivalent circuit used in efficiency analysis. Here, the losses of SCPA capacitor bank, inductor, and transformer are lumped into the matching network.

Insertion loss will attenuate the power delivered to the load and can be written as $P_{\text{out}} = \alpha P'_{\text{out}}$, where α is the insertion loss factor.

The switching loss is due to the charging/discharging of capacitors and crowbar current in SCPA unit cells. This loss can be represented by an equivalent loss capacitance $C_{\text{sw}} \equiv (P/V_{\text{dd}}^2 f)$, where P is the power dissipated by the SCPA unit cells including their predrivers, when all cells are switching, driving no load, and switching at frequency f. The switching loss can be written as $P_{\text{sw}} = C_{\text{sw}} V_{\text{dd}}^2 f(n_1 + n_2)$, which is proportional to the number of drivers switching, and decreases linearly with output voltage. This allows the VMD to achieve high efficiency at back-off.

The conduction loss and the switching loss represent a tradeoff in the SCPA unit cell design. Since $R_{\text{ON}} \propto (1/W)$, and $C_{\text{sw}} \propto W$, where W is the effective width of the switching transistors, the product $R_{\text{ON}}C_{\text{sw}}$ is constant. Therefore, we can define the totem pole driver figure of merit $f_{\text{SW}} = 1/(2\pi R_{\text{ON}}C_{\text{sw}})$. Advanced process technologies, such as scaled CMOS, circuit topologies (e.g., antishoot through current), and good layout practice, can all help to improve f_{SW}. With this, we can relate the switching loss to the power delivered to the matching network as

$$\frac{P_{\text{sw}}}{P'_{\text{out}}} = \frac{\pi}{2}\frac{f}{f_{\text{sw}}}\frac{1}{n_1 + n_2}\frac{R_L}{2R_{\text{ON}}}\left(1 + \frac{2R_{\text{ON}}}{R_L}\right)^2.$$

It should be noted that as the output voltage decreases, the relative switching loss increases. This is because even though the switching loss reduces linearly with output voltage $(n_1 + n_2)$, the output power is proportional to the square of output voltage $(n_1 + n_2)^2$. This implies that the efficiency at 6-dB back-off will always be lower than the efficiency at peak power in this architecture due to a doubling of the relative switching loss. A similar problem (but more pronounced) occurs in outphasing PAs where the switching loss is constant

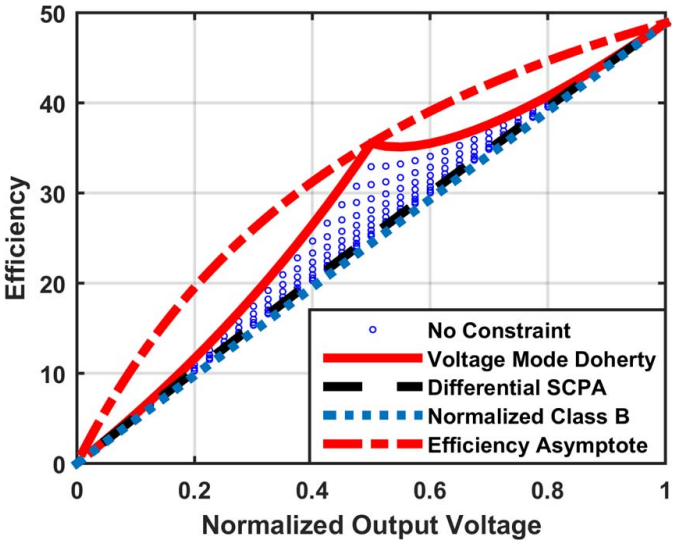


Fig. 9. Efficiency versus output voltage for voltage mode Doherty and differential SCPA including nonideal components ($Q_L = 1, \alpha = 0.9$, $(2R_{\rm ON}/R_L) = 0.15$, $f_{\rm SW} = 10$GHz, and $f = 1$GHz).

regardless of output power [16]. In outphasing, the two switch-mode PAs are fully on regardless of output voltage, resulting in a fourfold increase in relative switching loss at 6-dB back-off. In the conventional Doherty PA, the doubling of the main PA load impedance at 6-dB back-off and the soft turn-on characteristic of the transistor causes the efficiency to be lower at the 6-dB back-off point [21].

We can now write the overall output power and efficiency as

$$P_{\rm out} = \alpha P_{\rm out}^{'} = \frac{\alpha P_{\rm out}^{0}}{\left(1+\frac{2R_{\rm on}}{R_L}\right)^2} = \frac{\frac{2\alpha}{\pi^2}\frac{V_{\rm dd}^2}{R_L}(n_1+n_2)^2}{\left(1+\frac{2R_{\rm on}}{R_L}\right)^2}$$

$$\eta = \frac{\alpha P_{\rm out}^{'}}{P_{\rm out}^{'} + P_{\rm cond} + P_{\rm sw} + P_{\rm cd}} = \frac{\alpha}{1+\frac{P_{\rm cond}}{P_{\rm out}^{'}} + \frac{P_{\rm sw}}{P_{\rm out}^{'}} + \frac{P_{\rm cd}}{P_{\rm out}^{'}}}$$

where

$$\frac{P_{\rm cd}}{P_{\rm out}^{'}} = \frac{\pi}{2}\frac{1}{Q_{\rm SCPA}}\left(1+\frac{2R_{\rm on}}{R_L}\right)^2 \frac{n_1(1-n_1)+n_2(1-n_2)}{(n_1+n_2)^2}.$$

Fig. 9 shows the efficiency versus output voltage of VMD including the nonidealities for a specific set of design parameters. Here, we can see that insertion loss, conduction loss, and switching loss form an asymptote of efficiency (dashed-dotted line), which limits the achievable efficiency at any back-off point. When the capacitive divider loss is included, the efficiency drops from the asymptote. In the case of VMD, the capacitive divider loss vanishes at 6-dB back-off causing the efficiency line to touch the asymptote and resulting in back-off efficiency peaking.

V. Implementation

A. Load Modulation Network

A pseudodifferential architecture is used in this design to mitigate the effect of wirebond inductance on the supply and ground. The virtual ground provides the large fundamental current component, and the remaining even-harmonic ripple is filtered by on-chip decoupling capacitors. Since the VMD architecture needs low impedance looking into the supply network at both baseband and RF, wide RF bandwidth as well as wide modulation bandwidth can be achieved simultaneously with the VMD. This is unlike a conventional current-mode PA where the size of the RF choke presents a tradeoff between RF and modulation bandwidth [1].

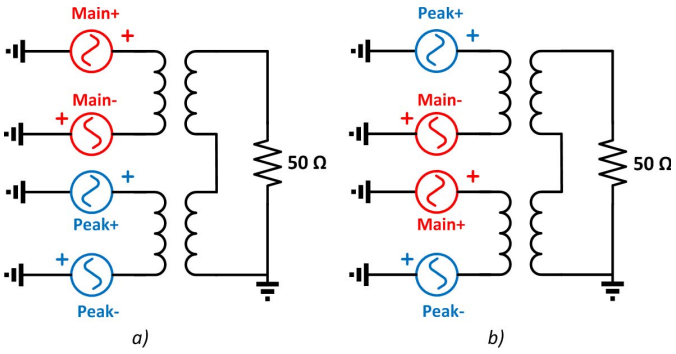


Fig. 10. (a) Secondary and (b) primary load modulated pseudodifferential voltage mode Doherty.

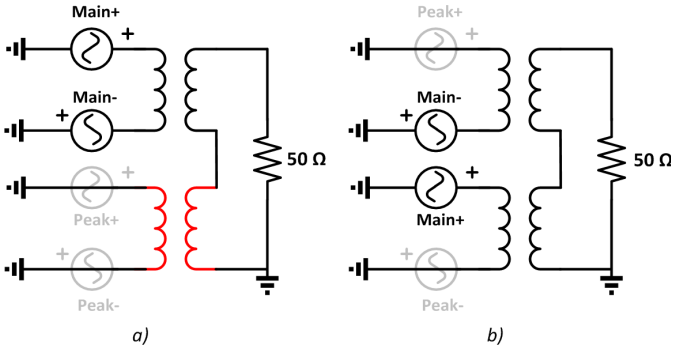


Fig. 11. (a) Secondary and (b) primary load modulated pseudodifferential voltage mode Doherty operation at 6-dB back-off (the parasitic transformer is indicated in red).

Two possible implementations of the VMD utilizing two pseudodifferential SCPAs are shown in Fig. 10. The two structures are identical at peak power. However, at 6-dB back-off, the secondary load modulation architecture [Fig. 11(a)] utilizes only half of the transformer structure (the other half merely provides a short circuit shown in red), while the primary load modulation architecture [Fig. 11(b)] still utilizes the whole structure. Since the primary load modulation architecture fully utilizes the transformer structure at 6-dB back-off, it provides low passive loss at any power level [17]. An additional benefit of primary load modulation is that the secondary only provides power combining. This allows flexibility between the choice of series and parallel combining, as shown in Fig. 12. For ease of experimentation, a lumped-element balun implementation of Fig. 12(b) is used in this design.

The lumped-element balun [1] is shown in Fig. 13(a). It can be shown by superposition [Fig. 13(b) and (c)] that the voltage at the load is the difference between the two input

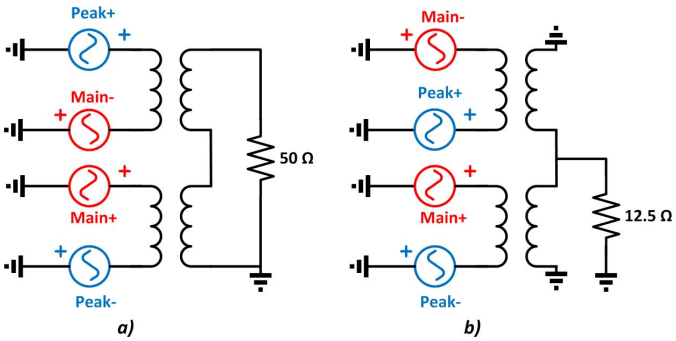


Fig. 12. (a) Series combined and (b) parallel combined load modulated pseudodifferential voltage mode Doherty (load is adjusted to provide the same output power).

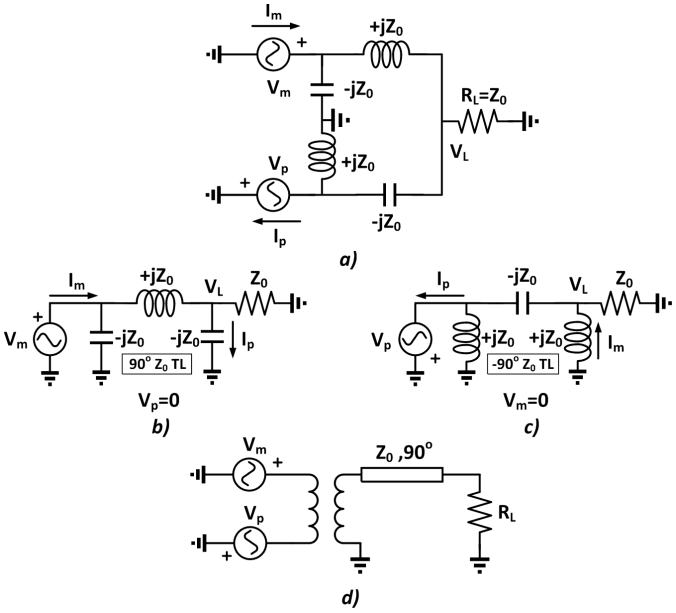


Fig. 13. (a) Lumped-element balun circuit. (b) Equivalent circuit when $V_p = 0$. (c) Equivalent circuit when $V_m = 0$. (d) Overall equivalent circuit.

voltages with 90° phase delay, $V_L = -j(V_m + V_p)$, and the load impedance seen by the main PA is

$$Z_m = \frac{V_m}{I_m} = \frac{V_m}{\frac{V_m}{Z_0} + \frac{V_p}{Z_0}} = \frac{Z_0}{1 + \frac{V_p}{V_m}}.$$

An equivalent representation for the balun, which holds for any load impedance R_L, is shown in Fig. 13(d).

The implemented load modulation network operating at peak power and 6-dB back-off is shown in Fig. 14. Since the impedance inverter embedded in the balun design can severely limit the bandwidth, the characteristic impedance of each lumped-element balun is designed to be equal to its load impedance (Fig. 14), such that the impedance inverter behaves like a through, providing wide bandwidth. In addition to transforming 50–12.5 Ω, the T-network following the baluns also compensates the impedance at frequency offsets from the balun center frequency, further extending the bandwidth.

B. Dual Pseudodifferential SCPA

The dual pseudodifferential polar SCPA is implemented in 65-nm bulk CMOS, and the overall floorplan and chip

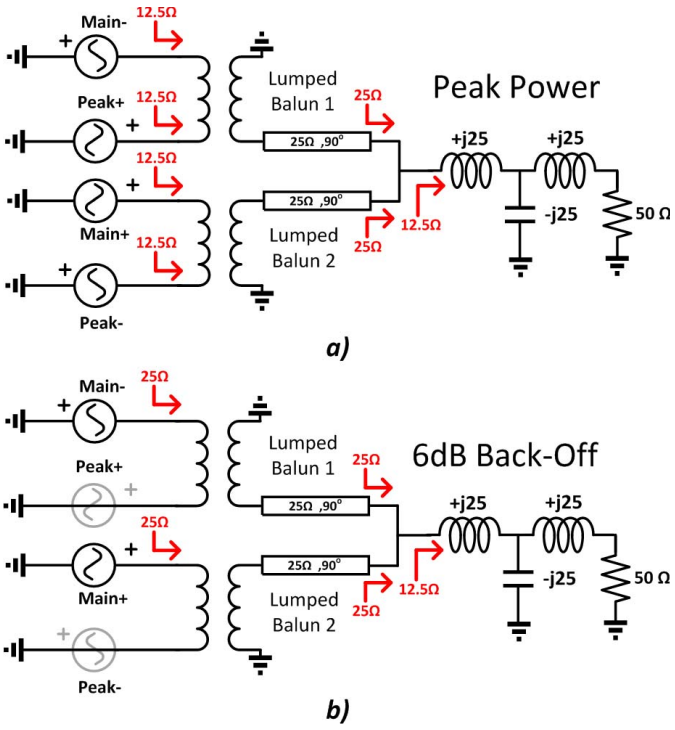
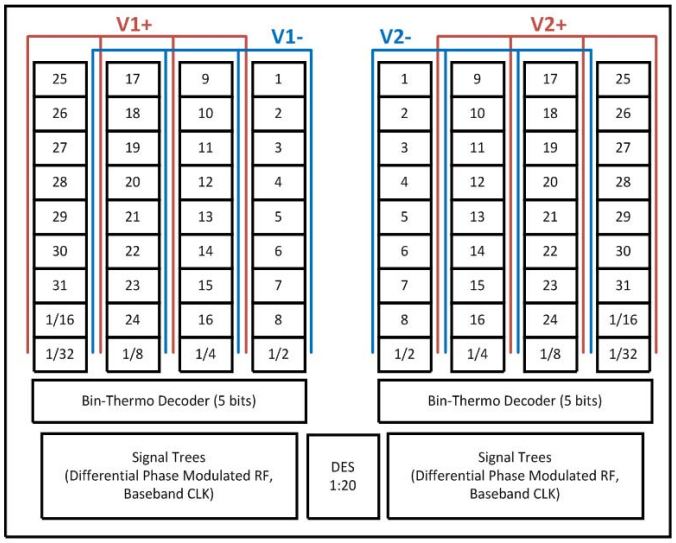


Fig. 14. Implemented load modulation network with annotated impedance for operation at (a) peak power and (b) 6-dB back-off.

micrograph is shown in Fig. 15. The drivers in each side of pseudodifferential SCPA are designed, such that at peak power, the drain–source voltage drop over the cascode structure when the transistor is ON is about 10% of the supply voltage, keeping the SCPA linear. This gives $R_{\mathrm{ON}} = 0.1(\pi/2)12.5\Omega = 1.9\Omega$ for each SCPA. The capacitor bank is designed for $Q_L = 1$, which gives $C = 12.8$ pF at 1 GHz in each side of each pseudodifferential PA. Each SCPA uses a 5-bit unary, 5-bit binary segmented DAC architecture. The unit cell is designed to be pseudodifferential, providing virtual ground locally within the unit cell and minimizing lossy fundamental current flow. The turn-on sequence is shown in Fig. 15, where cells are enabled in increasing numbering as the output voltage increases. The relatively large difference in location between some cells with adjacent numbers, e.g., cells 8 and 9, leads to kinks in the AM–PM characteristic (to be described in the following, Fig. 19), and can be improved with a modified layout in future implementations. The signal distribution trees provide balanced timing for phase-modulated RF and baseband CLK to each column of unit cells.

The unit cell is designed with a cascoded switch final stage (Fig. 16) to double voltage swing, delivering 6 dB higher power to the load. The buffers are designed to have a fan-out of about 4, providing sharp transitions and helping to minimize the crowbar current. The level shift that drives the high side transistor is based on the architecture presented in [18]. The D-Flip-Flop at the unit cell synchronizes the enable signal with the baseband clock providing excellent AM–PM characteristics. The MIM capacitor size is $(12.8\mathrm{pF}/32) = 400$ fF for each unary cell, and is scaled down accordingly for binary cells.



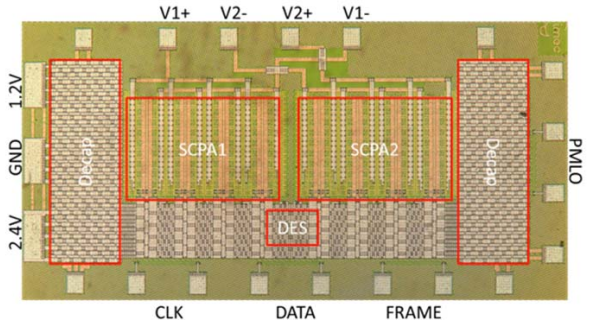


Fig. 15. Voltage mode Doherty floor plan. The unary unit-cell turn-on sequence of each SCPA is shown with increasing integers; the binary weighted unit cells are shown with their corresponding fractional weights. The chip micrograph (1.8 mm × 0.9 mm) is also shown.

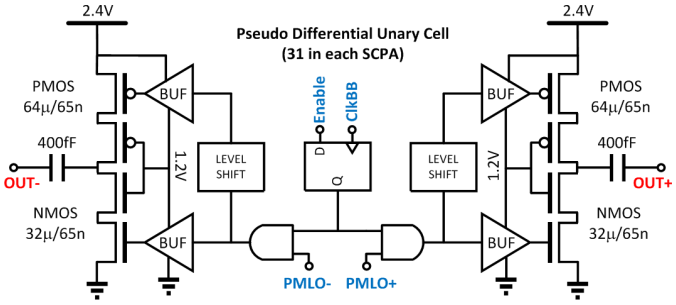


Fig. 16. Pseudodifferential SCPA unit cell.

VI. Measurement Setup and Result

The measurement setup is shown in Fig. 17. It is composed of RF vector signal generator to provide the PM-LO, high-speed serial pulse pattern generator to provide amplitude control word (ACW), spectrum analyzer for spectrum and narrowband EVM measurement (VSA Mode), high speed oscilloscope for wideband EVM measurement, and RF power meter for accurate power measurement. PAE includes all power consumption on-chip, as well as insertion loss of the output load modulation network to the edge of the PCB (50 Ω). The external PM-LO and Serial Data/Clk/Frame power is excluded, because most of the power is consumed in termination resistors. In an integrated implementation, these will be about the power needed to drive a few minimum size CMOS inverters, which is negligible.

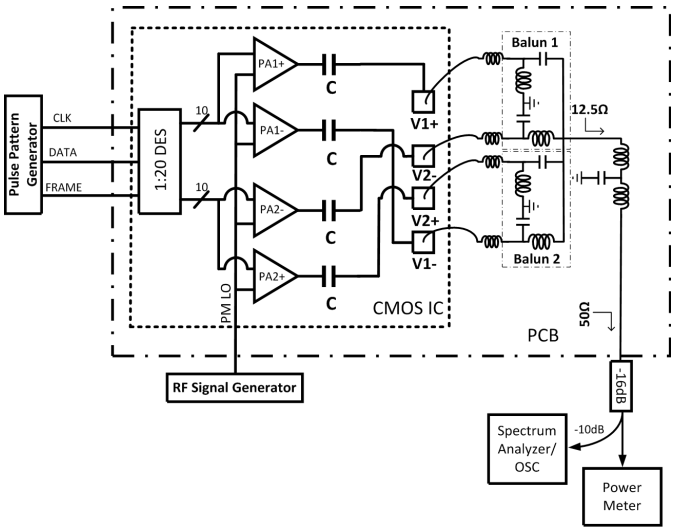
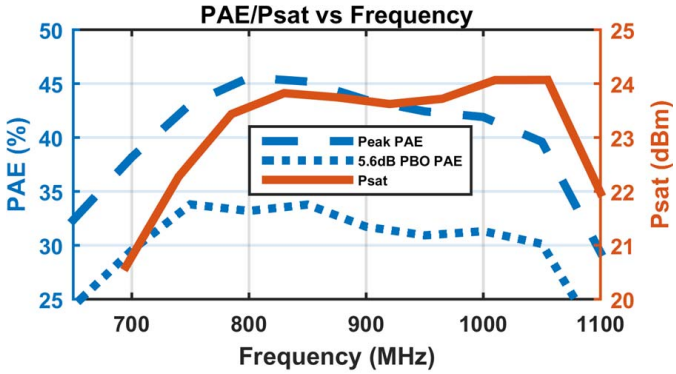


Fig. 17. Overall implementation and measurement setup.



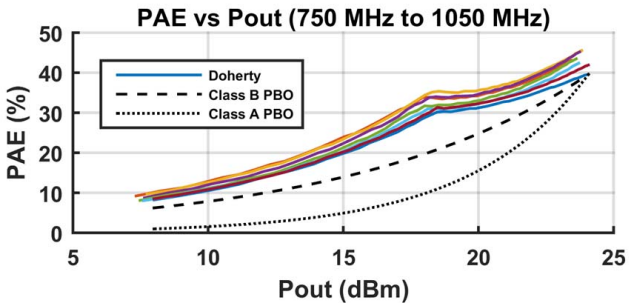


Fig. 18. Measured performance of VMD: PAE and P_{sat} versus frequency and PAE versus P_{out} for different frequencies (750-1050 MHz with 50 MHz steps).

The baseband signal generation and linearization is performed in MATLAB with the baseband sampling frequency of 360 MHz. Since there is no on-chip interpolation filter [19], digital replicas are expected at multiples of 360-MHz offset.

A. CW Measurement Result

The CW measurement with standard power supply (1.2/2.4 V) is shown in Fig. 18, the peak power, peak PAE, and 6-dB back-off PAE are 24 dBm, 45%, and 34%, respectively. With a boosted power supply of 1.5/3 V, the measured peak power is 26 dBm with the same PAE; no degradation was observed over laboratory testing time scales. The 1-dB P_{sat}

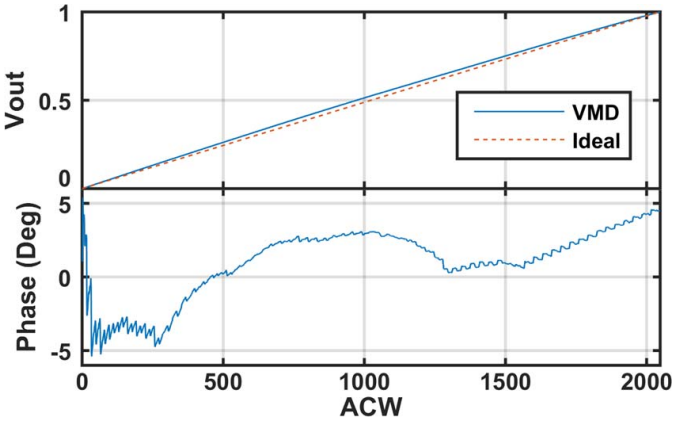


Fig. 19. Measured ACW-AM and ACW-PM at 900 MHz.

bandwidth ranges from 750 to 1050 MHz, a fractional bandwidth over 33%. The efficiency peaking point located around 5.6-dB back-off rather than 6-dB back-off due to slight increase in the passive network loss. The efficiency at 6-dB back-off is lower than the peak efficiency as expected from efficiency asymptote analysis. At 6-dB back-off, the relative switching loss (P_{sw}/P_{out}) doubles similar to the class-G SCPA case [15].

B. Modulation Measurement

In this measurement, the PA is linearized with a memoryless lookup table (LUT). The LUT was generated using an input signal at 10 kHz, amplitude modulated with 100% modulation index. As shown in Fig. 19, the ACW-AM relationship is highly linear even before correction; minor imperfection results from small nonlinear on resistance. The ACW-PM relationship appears as a weighted average of ACW-PM behaviors of each SCPA. Its peak-to-peak deviation is comparable with that of a single SCPA, which could be improved with better layout as noted earlier.

1) Narrowband Modulation: A 9-MHz 1024-QAM, 32 Carrier OFDM signal hard-clipped to 8.6-dB PAPR and centered at 900 MHz is used. The result shows 15.1-dBm P_{out}, 22.9% PAE, −41.2 dB EVM, and better than 45-dBc ACPR [Fig. 20(a)]. This demonstrates excellent linearity without the need to back-off the output power ($P_{sat} - P_{out}$ =PAPR). The dynamic AM–AM and AM–PM [Fig. 21(a)] show minimal memory effects.

2) Wideband Modulation: A 40-MHz 256-QAM 802.11ac modulation (108 Data, 6 Pilot OFDM) hard-clipped to 9-dB PAPR is used. The result shows 14.7-dBm P_{out} with 22% PAE and −34.8 dB EVM, meeting the EVM spec and Tx mask [Fig. 20(b)]. No equalization or back-off is required. The dynamic AM–AM and AM–PM [Fig. 21(b)] show moderate amounts of memory effect. This is mainly due to passband P_{sat} ripple and nonideal baseband supply decoupling. After equalization, the EVM is −36.5 dB, very close to the measurement noise floor of −38 dB (limited by the oscilloscope).

The out-of-band spectra for the 9- and 40-MHz modulations are shown in Fig. 22. The digital replicas due to zero-order

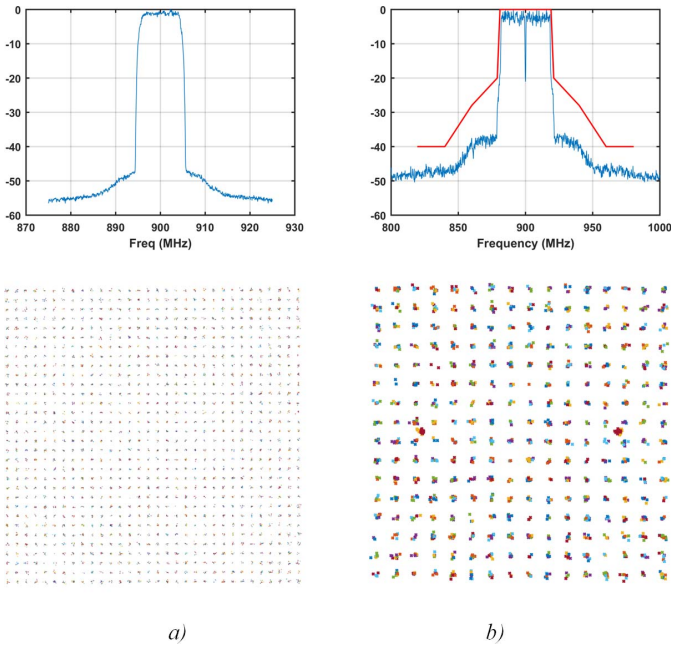


Fig. 20. (a) Measured spectrum and constellation of 9-MHz 1024-QAM OFDM modulation. (b) Measured spectrum and constellation of 40-MHz 256-QAM 802.11ac modulation.

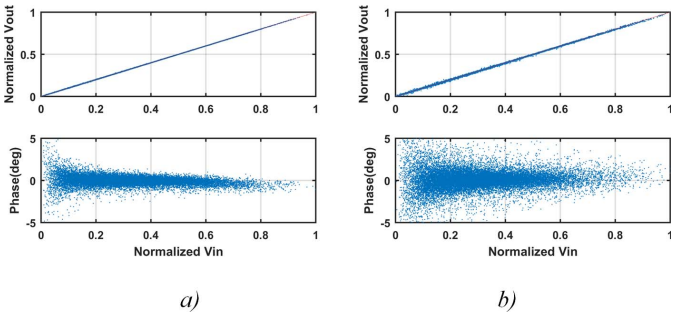


Fig. 21. Dynamic AM–AM and AM–PM for (a) 9-MHz modulation and (b) 40-MHz modulation.

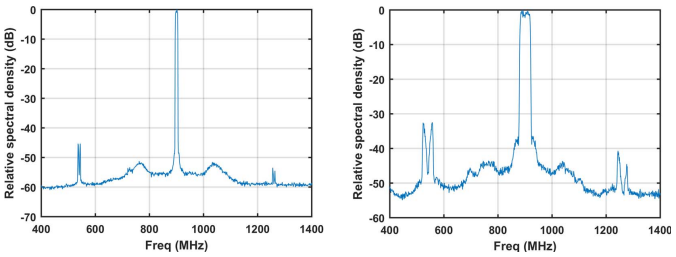


Fig. 22. Out-of-band spectrum for 9-MHz modulation (left) and 40-MHz modulation (right).

hold operation of the digital inputs are located at 360 MHz offset as expected; the higher frequency replica is smaller due to matching network attenuation. An on-chip interpolation filter [19] can increase the offset frequency and greatly attenuate the digital replicas. A ground bounce-related spurious output is observed at 120-MHz offset in both cases due to bondwire inductance on supply/ground.

The measurement showed that this PA achieves superior linearity suitable for modern and future modulation standards while maintaining similar efficiency as the current state of the art (Table I). To account for PAPR differences in the

TABLE I
COMPARISON WITH CMOS PA WITH BACK-OFF EFFICIENCY ENHANCEMENT

	This Work	**[15]**	**[20]**	**[19]**	**[13]**	**[17]**
Freq(MHz)	900	2000	2000	2200	3500	1900
1dB Psat BW(%)	**33**	15	10	29	25	17
Psat (dBm)	24	24.3	20	23.3	27.3	28
Technology	65(LP)	65(LP)	65	65	65	40
Vdd	1.2/2.4	1.4/2.8	-	1.2	1.2/3	1.5
Peak/6dB Eff(%)	45/34 (PAE)	44/37[5] (PAE)	22/17 (PAE)	43/33 (DE)	33/34 (DE)	34/26 (PAE)
Topology	VMD	ClassG	ClassG	XFMR	Doherty	Doherty
Modulation	**40MHz 802.11ac 256QAM**	20MHz 802.11g 64QAM	5MHz LTE 64QAM	20MHz 802.11g 64QAM	0.5MHz 16QAM	20MHz LTE 16QAM
PAPR(dB)[4]	**9.0**	7.5	5.8	6.5	5.5	4.6
EVM (dB)	**-34.8**[1]	-30.8[3]	-28[1]	-28[1]	-25[2]	-23[3]
Avg Eff(%)	22	33[5]	12	21.8	22.1	23.3
Equivalent Eff (%)[6]	**62**	78[5]	24	46	42	40
Matching Network	Off-Chip	Off-Chip	On-Chip	On-Chip	On-Chip	On-Chip

[1]AM-AM/PM LUTs [2]AM-AM LUT [3]No LUT
[4]Output PAPR=P_{sat}-P_{out} [5]Output balun loss is excluded
[6]Peak efficiency of PA with ideal class-B power back-off that would achieve the same average efficiency

comparison of average efficiency for different modulations, we have introduced "equivalent efficiency," defined as the peak efficiency of an ideal class-B amplifier that gives the same average efficiency. This equivalent efficiency can be approximated by $\eta_{\text{eff}} = \eta_{\text{avg}}(\text{PAPR})^{(1/2)}$ with reasonable accuracy. An amplifier with class-B back-off characteristics would have $\eta_{\text{eff}} \approx \eta_{\text{peak}}$ regardless of the PAPR of the modulation and the PA with back-off efficiency enhancement would have $\eta_{\text{eff}} > \eta_{\text{peak}}$. The equivalent efficiency metric illustrates the fact that maintaining high efficiency is increasingly difficult for high back-off, although the detailed relationship between efficiency and back-off does not correspond to the Class-B case for all architectures. In Table I, it is also important to note that on-chip matching generally leads to higher insertion loss, resulting in lower output power and efficiency.

VII. CONCLUSION

This paper demonstrates a new Doherty technique that eliminates the impedance inverter, thus enabling wide bandwidth. To the best of our knowledge, this is the widest fractional bandwidth (at both peak and 6-dB PBO) Doherty amplifier demonstrated in the CMOS technology. With only simple LUT linearization, this amplifier can transmit a 256-QAM 40-MHz 802.11ac modulation meeting the specification without back-off while also maintaining excellent efficiency. Since this PA uses CMOS transistors as switches, its performance improves with CMOS technology scaling, especially with recent advances in pMOS transistor performance. This should make it possible to use this technique for even higher carrier frequencies, for example, for a 6-GHz carrier with integrated transformer, amplifying up to 160-MHz modulation (similar fractional bandwidth) with reasonable efficiency.

ACKNOWLEDGMENT

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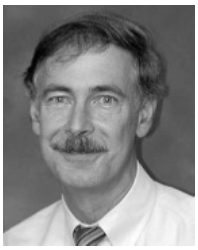

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