Broadband CMOS Stacked Power Amplifier Using Reconfigurable Interstage Network for Envelope Tracking Application

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***Abstract* — A 2-stage stacked-FET power amplifier with a reconfigurable interstage network is developed for broadband envelope tracking application using SOI CMOS. The wideband PA is based on Class-J mode of operation, where output matching is realized with two-section low-pass network. Miller capacitors are also employed across the FET stack to guarantee Class-J-like operation for inner FET stacks. To overcome the bandwidth limit due to high-Q interstage matching, reconfigurable matching network is employed using SOI switch, allowing dual frequency-mode operation. The fabricated PA shows CW efficiencies in excess of 60% from 0.65 to 1.0 GHz. When operated with an ET supply modulator, overall ET PA system shows W-CDMA efficiencies higher than 50% from 0.68 to 0.92 GHz and LTE efficiencies higher than 40% from 0.65 to 0.95 GHz.**

***Index Terms* — Broadband, CMOS, Class-J, envelope tracking (ET), high-efficiency, LTE, power amplifier (PA), SOI, stacked-FET, W-CDMA.**

I. Introduction

The rapid deployment of LTE systems across the world requires a mobile phone to support a large number of highly fragmented LTE bands for data roaming. In order to reduce the size and cost of RF front-ends, there is a strong need for a multi-band power amplifier (PA) that can cover a broad frequency bandwidth using a single PA chain. For example, due to the recent LTE deployment at 700 MHz bands, cellular band (~0.9 GHz) PAs are required to cover all the way down to 0.7 GHz. Several output matching techniques such as Class-J and continuous Class-F are introduced to achieve wideband operation [1], [2]. However, these approaches have limits for multi-stage amplifiers since the bandwidth limit often arises from the interstage matching.

Another challenge in the high-efficiency PA design is the need to support the modulation signals with a wide range of peak-to-average power ratios (PAPRs) for multi-mode operation such as W-CDMA and LTE. Envelope tracking (ET) has emerged as a most practical solution to achieve high efficiencies for multi-mode operation. However, little work has been presented to demonstrate a broadband ET PA using multi-stage design.

In this work, a two-stage stacked CMOS PA is developed for broadband ET operation using Class-J output matching and reconfigurable interstage matching. On top of Class-J output matching, a reconfigurable matching is realized at the interstage using an SOI CMOS switch to overcome the bandwidth limitation coming from high-Q impedance matching. Miller capacitors are also used across the stacked FETs for effective Class-J harmonic control. As a result, the PA achieves CW PAEs in excess of 60% from 0.65 to 1.0 GHz. When operated with an ET supply modulator fabricated on the same wafer, overall ET PA system shows W-CDMA efficiencies higher than 50% from 0.68 to 0.92 GHz and LTE efficiencies higher than 40% from 0.65 to 0.95 GHz.

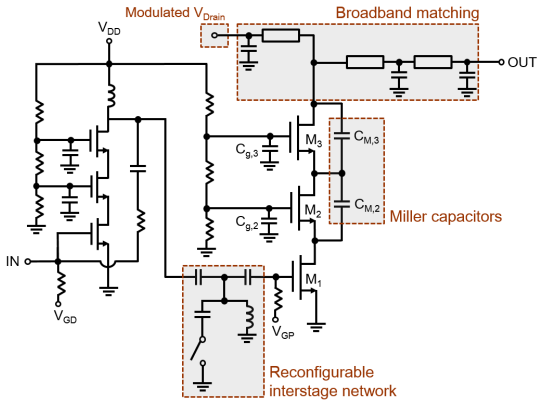


Fig. 1. Detailed circuit schematic of the proposed 2-stage CMOS stacked PA with reconfigurable interstage network.

II. 2-Stage Class-J CMOS PA Design

Overall circuit schematic of a two-stage Class-J CMOS PA is shown in Fig. 1. Triple-stacked FET structure is selected to overcome the low breakdown voltage problem of CMOS. The gate widths of each FET are 2 mm and 20 mm for driver stage and power stage, respectively. The core idea of Class-J PA is to use second harmonic control to shape the voltage waveform close to a half-sinusoid. Ideal fundamental and second harmonic impedances of the Class-J amplifier are given by $Z_1 = R_{opt} \cdot (1 + j)$, $Z_2 = -j0.5R_{opt}$ at the intrinsic drain current source [1]. In the actual PA design stage, the optimum 2nd harmonic impedance is often shifted to the inductive region due to the effect of the parasitic capacitance such as drain-to-source capacitance, C_{ds}. To confirm this, harmonic loadpull simulations are performed on the triple-stacked FET and the results are shown in Fig. 2(a), which show that

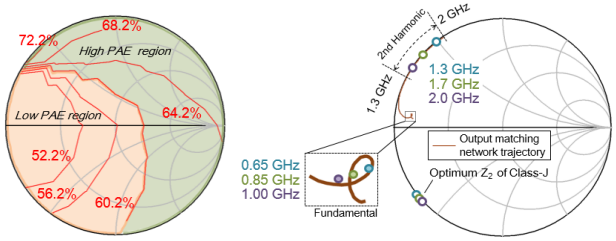


Fig. 2. Simulated load-pull contours of the triple-stacked FETs at 0.85 GHz. (a) 2nd harmonic frequency loadpull. (b) Optimum load impedance targets from 0.65 to 1.0 GHz and the simulated load impedances of two-section output matching network.

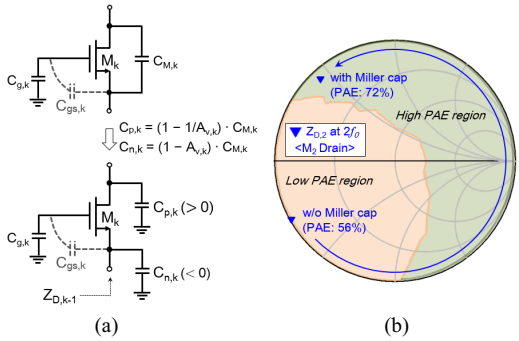


Fig. 3. (a) Effect of Miller capacitance. (b) Simulated load impedance at M_2 drain with and without Miller capacitor.

the optimum 2nd harmonic impedances are in the inductive region. For high-efficiency operation, the output matching network should provide optimum impedances at both fundamental and 2nd harmonic frequencies. In this work, a two-section low-pass network consisting of inductive lines and shunt capacitors is used to synthesize near-optimum load impedances over a wide frequency range from 0.65 to 1.0 GHz. Fig. 2(b) shows the fundamental and 2nd harmonic load impedances generated by the two-section matching network, which closely follows the optimum impedance points at both fundamental and 2nd harmonic frequencies.

For high-efficiency operation, one also needs to optimize the load impedances seen by the inner stack FETs such as M_1 and M_2 in the triple stack (see Fig. 1). The fundamental impedance at drain node of each stacked FET can be properly designed by selecting appropriate gate dividing capacitance (C_{g2} and C_{g3}). However, the second harmonic load impedances are hard to control since they approach short circuit due to the large input capacitance (~20 pF) of the upper power transistors. As one can see from the harmonic loadpull contours in Fig. 2(b), short circuit at the second harmonic frequency results in a lower efficiency. To transform the second harmonic impedance to high-efficiency (inductive) region, we have employed Miller capacitors across the source and drain terminals of CG-FETs. As shown in the Fig. 3(a), Miller capacitor can be divided into two shunt capacitors at the source ($C_{n,k}$) and

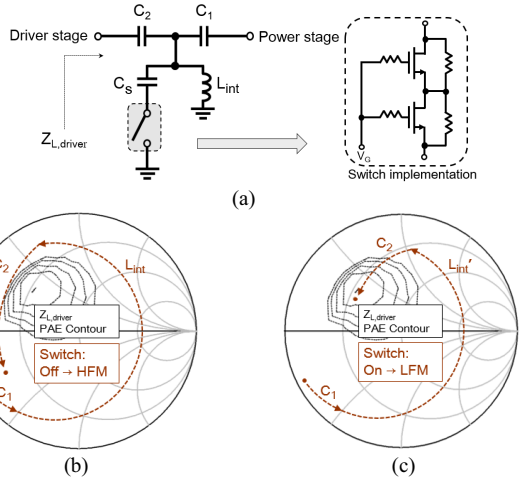
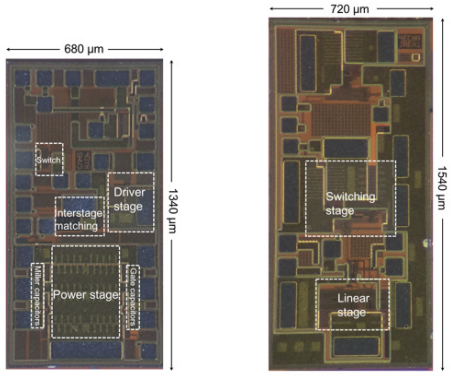


Fig. 4. (a) Reconfigurable interstage matching network using SOI switch. Driver load impedance matching trajectory at 0.7 GHz. (b) Before reconfiguration (switch off) and (c) After reconfiguration (switch on).

drain ($C_{p,k}$) terminals. As the CG-FET has a positive voltage gain greater than unity, the transformed capacitor at the source node ($C_{n,k}$) has large negative capacitance, which effectively transforms the second harmonic load impedance seen by the preceding FET to high-efficiency (inductive) region. This effect is shown in the simulated second harmonic load impedance of M_2 in Fig. 3(b). Similar effects can be seen for M_1 harmonic load impedances due to the Miller capacitor applied to M_2.

To achieve high gain (> 23 dB) required for mobile phones, the PA requires more than a single stage. In this work, two-stage design is employed, where each stage is implemented with triple-stacked CMOS FETs. Due to the mismatch of impedances between the two triple-stacked transistors, interstage matching is required, which imposes major bandwidth limitation, severer than that coming from output matching since the interstage matching is often required between high-Q impedances. To solve this problem, we have employed a reconfigurable matching network at the interstage.

Fig. 4 shows the concept of the reconfigurable matching for dual frequency-mode operation. A switch implemented using 2 mm double-stacked SOI CMOSFETs switches in and out the shunt capacitance (C_S). When the switch is in the off-state called high-frequency mode (HFM), the optimum load impedance is presented to the driver stage only at higher frequencies (0.8~1.0 GHz). Efficiency degradation below 0.8 GHz is thus inevitable. When the interstage matching network is reconfigured to the low-frequency mode (LFM) by closing the switch, the value of the inductance (L_{int}) is compensated by C_S such that $L_{int}' = L_{int} / (1 - \omega^2 \cdot L_{int} \cdot C_S)$, thus the optimum impedance is presented to the lower frequencies (0.65~0.8 GHz). As LTE bands are fragmented, one can easily find the mode-switching frequency between the deployed LTE bands. The



(a) (b)

Fig. 5. Chip photographs of the fabricated (a) PA and (b) EA.

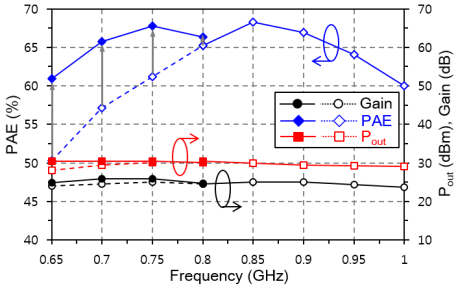


Fig. 6. Measured CW performance of the fabricated PA from 0.65 to 1.0 GHz. (filled: with reconfiguration - LFM, hollow: as is - HFM only)

effect of reconfiguration is demonstrated in Fig. 4(b) and (c) by showing the load impedance of the driver stage with and without interstage reconfiguration at 0.7 GHz. The simulated PAE improvement is as much as 9% at 0.7 GHz with reconfiguration.

III. Measurement Results

Two-stage stacked-FET PA with reconfigurable interstage matching is fabricated using SOI CMOS process. SOI CMOS process allows co-integration of PA and switches for reconfiguration. Also, fabricated on the same wafer is the ET supply modulator or envelope amplifier (EA), which is designed based on a hybrid combination of linear stage and switching stage to achieve high linearity and efficiency at the same time [5]-[7]. The gate length used for the PA is 0.32-μm. Fig. 5 shows the die photographs of the 2-stage reconfigurable PA and a hybrid EA. The chips are mounted on a 400-μm thick FR4 PCB (ε_r ~ 4.6, tanδ = 0.025) for CW and ET testing. Fig. 6 shows the measured CW performance of the reconfigurable stacked-FET PA. The applied gate and drain biases are 0.3 V and 3.5 V, respectively, resulting in a quiescent current of 50 mA. The peak PAE is 68.3% at 0.85 GHz. Over 60% PAE is achieved between 0.65 and 1.0 GHz. The measured PAE without interstage reconfiguration (HFM only) is also shown in Fig. 6 for comparison. Up to 10% boost in PAE has been achieved by switching to LFM mode below 0.8

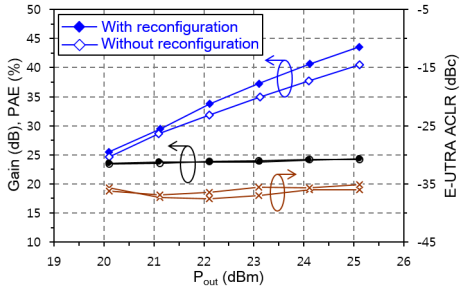


Fig. 7. Measured performance of overall ET PA system using 10 MHz LTE signal at 0.7 GHz with and without interstage reconfiguration.

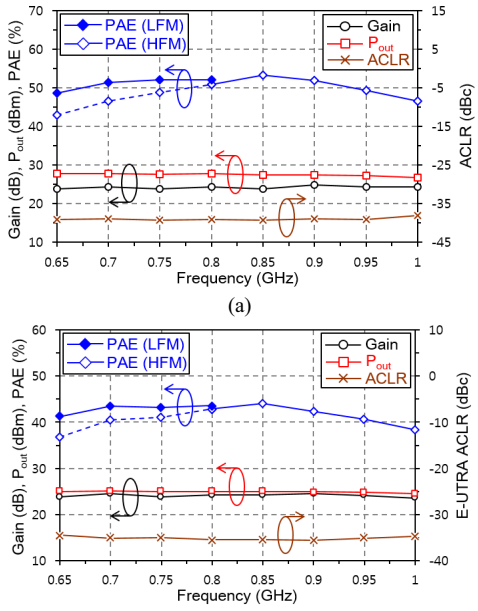


Fig. 8. Measured performance of overall ET PA system from 0.65 to 1.0 GHz. (a) W-CDMA signal. (b) 10 MHz LTE signal. (filled: with reconfiguration - LFM, hollow: as is - HFM only).

GHz, which clearly shows the benefit of reconfigurable interstage network. The measured output power ranges from 29 to 30.6 dBm across the entire band while the gain stays between 23.7 and 25.9 dB. Table I compares CW performance of the published broadband PAs showing higher than 60% PAEs. The PA of this work shows 42% fractional bandwidth (for 60% PAE or higher), which is comparable with the single-stage results using SiGe BJT's [7], but shows much higher gain due to the two-stage design.

ET performance of the broadband PA was measured using the envelope amplifier (EA) fabricated on the same wafer. For reference, the measured average efficiency of EA at 3.5 V bias is 85% using W-CDMA signals (PAPR~3.4dB), and 74.3% using 10 MHz LTE signals (PAPR~6.7 dB).

Fig. 7 shows the measured performance of ET PA with 10 MHz LTE signal at 0.7 GHz with and without interstage reconfiguration. With the reconfiguration, overall ET

TABLE I

COMPARISON OF BROADBAND HIGH EFFICIENCY (> 60% CW PAE) PAS

Ref.	PA Technology	Bandwidth		PAE	Pout	Gain
		(GHz)	(%)	(%)	(dBm)	(dB)
[3]	0.28-µm CMOS	1.4~2.0	35	60~67	23	N/A
[4]	0.35-µm SiGe BiCMOS	0.6~0.7	15	60~68.9[1] (CE)	30.9~31.5	10
[7]	0.35-µm SiGe BiCMOS	0.65~1.05	47	61.2~72.1	31.5~33.1	12.5
This work	0.32-µm SOI CMOS	0.65~1.0	42	60~68.3	29~30.6	23.6~25.9

[1] This result is graphically estimated.

TABLE II

COMPARISON OF ET PAS FOR BROADBAND LTE MOBILE TERMINALS

Ref.	PA Technology	Freq (GHz)	FB[1] (%)	LTE BW (MHz)	PAE[2] (%)	Pout (dBm)	ACLR (dBc)
[5]	GaAs HBT	1.7	16	10	39.5	27	−33.1
[6]	0.18/0.4-µm CMOS	1.85	16	10	34.1	26	−34.2
[7]	0.35-µm SiGe BiCMOS	0.7	N/A	10	41.1	28.1	N/A
This work	0.32-µm SOI CMOS	0.85	42	10	44	25	−35.5

[1] Fractional bandwidth

[2] Peak value within the frequency range

system efficiency (including the efficiency of EA) reaches 43.5% with 24.2 dB gain at 25.1 dBm output power. Compared with the case without interstage reconfiguration, this corresponds to PAE boost of 3.1%. Higher overall efficiency could have been achieved if an envelope amplifier with a higher efficiency was used in the ET testing. The measured E-UTRA ACLR of ET PA meets the system requirement with ~5 dB margin (−35.1 dBc) with memory-less digital pre-distortion (DPD).

Wideband ET performance is measured using W-CDMA and LTE signals by sweeping the carrier frequency from 0.65 to 1 GHz. Fig. 8(a) shows W-CDMA test data of the entire ET PA system. The peak PAE is 53.3% at 0.85 GHz, and PAE stays above 50% from 0.68 to 0.92 GHz. ACLR after memory-less DPD is better than −38 dBc across the entire bandwidth. Fig. 8(b) shows the measured performance of ET PA system using 10 MHz LTE signal in the same frequency range. A peak PAE of 44% is measured at 0.85 GHz with 25 dBm output power. Overall PAE of higher than 40% is achieved from 0.65 to 0.95 GHz while the efficiency drops to 38.3% at 1.0 GHz. E-UTRA ACLR is better than −35 dBc for the entire frequency range. Table II compares the overall efficiency of ET PA system for LTE mobile phones using various device technologies. Even if CMOS PA is used in this work, the measured PAE of this work is among the highest, including GaAs HBTs. Besides, it is worthwhile to note that the ET PA system of this work maintains high efficiencies over a broad (~40%) frequency bandwidth.

IV. CONCLUSION

In this work, we have developed a broadband 2-stage CMOS stacked-FET PA with reconfigurable interstage matching network for envelope tracking application. The PA is based on Class-J mode of operation, where output matching is realized using two-section low-pass network. To guarantee Class-J operation for the inner stacked FETs as well, Miller capacitors have been added across the drain terminals of the stacked FETs. To overcome the bandwidth limit from high-Q interstage matching, reconfigurable matching network is employed between the two stacked FETs. The PA circuit with the reconfigurable network is fabricated using SOI CMOS process. The fabricated PA shows CW efficiencies in excess of 60% from 0.65 to 1.0 GHz. When tested with an envelope amplifier (with an average LTE efficiency of 74%), the overall ET system efficiency higher than 40% has been achieved using 10 MHz LTE signals from 0.65 to 0.95 GHz.

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