A K-Band Differential SiGe Stacked Power Amplifier Based on Capacitive Compensation Techniques for Gain Enhancements

Xi Sung Loo[#,*], Kiat Seng Yeo [*], Moe Z. Win [#], Zhichao Li[*], Xiaopeng Yu[+] and Jer-Ming Chen[*]
[#] Massachusetts Institute of Technology, Cambridge, MA 02139, USA.
[*] Singapore University of Technology and Design, 487372, Singapore.
[+]Zhejiang University, Hangzhou 310058, P.R. China.

***Abstract*—A 20GHz differential 4-stacked power amplifier fabricated on 0.18μm SiGe technology is presented. Uniquely, 2 capacitive compensation techniques are introduced at common base stages and successfully boosting power gain by 2.56dB/stage. Inter-stage matching inductors are adopted and input biasing is achieved by emitter follower for reliability concern. It demonstrates favorable gain performance of >20dB against other stacking schemes while showing competitive saturated power of ≈22dBm with peak PAE of 26%.**

***Index Terms*— HBT, K-band, parasitic capacitance, power amplifier, stacked transistors**

I. Introduction

RF power amplifiers (PA) based on III-V compound semiconductor and SiGe HBT (Heterojunction Bipolar Transistor) technology have been popular adopted for the past decades due to its superior speed performances, breakdown voltages, and faster time-to-market as compared to silicon counterpart. Such technology has been the strong candidate in K-band applications which cover local multipoint distribution service and wide variety of high resolution radars at useful detection range. Feasible high-power generation using various series-parallel combining schemes of linear class PAs has made it suitable for used in radar applications.

The use of transformers and microstrip lines to combine power contribution from each individual PA have been popularly adopted at architecture level [1]. In conjunction with that, power amplification at individual cell is commonly implemented by mix combinations of cascading [2-4] and series connection of transistor stages [4-7]. The latter method is vital for achieving lower output matching transformation ratio while enable higher voltage swing. It could be implemented through cascode [4] or stacking [5-8] approaches. As compared to stacked PAs, the number of cascode stages is limited due to reliability concern at high voltage swing. Meanwhile, efforts to improve the gain performance of stacked PA has been restricted by requirement of extra base capacitances to confine voltage swing within device breakdown limit. The efficiency of stacked PAs could be improved through inter-node matching [7], [8] as well as integration with multi-gate drive approach for CMOS version [8]. Capacitive neutralization technique [2], [3], [10] has been widely introduced to improve isolation performance of common source PAs. It resulted in improved gain performance of PAs without further penalty in power consumption. However, the benefits of such technique have not been explored for implementation in cascode or stacked amplifiers.

In this paper, we present new circuit techniques to improve power gain performances of stacked PA through capacitive neutralization in both common base (CB) and common emitter (CE) stages and increase size ratio of base capacitances in CB stages.

II. Circuit Design

Figure 1(a) shows the circuit schematic of the proposed differential class AB stacked PA designed and fabricated based on TowerJazz 0.18μm SiGe technology. Each side of the PA is made up of a stack of 4 series-connected SiGe HBT transistors that operate from output DC voltage of 6V. The base emitter voltages of the transistors are set at 0.9V, close to biasing condition where maximum f_T occurs. Inter-stage matching is accomplished by shunt microstrip or spiral inductors based on complex considerations of area consumption and quality factors. They reside at top metal level (Metal 6) to reduce coupling loss. With differential topology, no DC blocking capacitors are needed in series with matching inductors. Thus, there is no additional loss incurred by them. Further, amplifier with differential topology is generally preferred to achieve higher stability [11]. The number of stacking transistors is restricted based on consideration of stacking efficiency, sizing of matching elements and limitation in breakdown voltages. Each amplification stage is made up of 4 HBT transistors with emitter sizing of 2 x 10.16μm x 0.15μm each to handle current consumption of >200mA. Such transistor cell exhibits optimum load impedance, R_{opt} of 9 ohms based on load-pull simulations. Figure 1(b) shows the I/O matching circuits realized using lumped LC components and FET-based biasing circuits used in CE stages. The output matching circuit is designed to match close to 4 x R_{opt}. Note that the coupling capacitors and RF choke are included as part of the matching elements. The CE biasing circuit shown also in Figure 1(b) is designed to be low impedance

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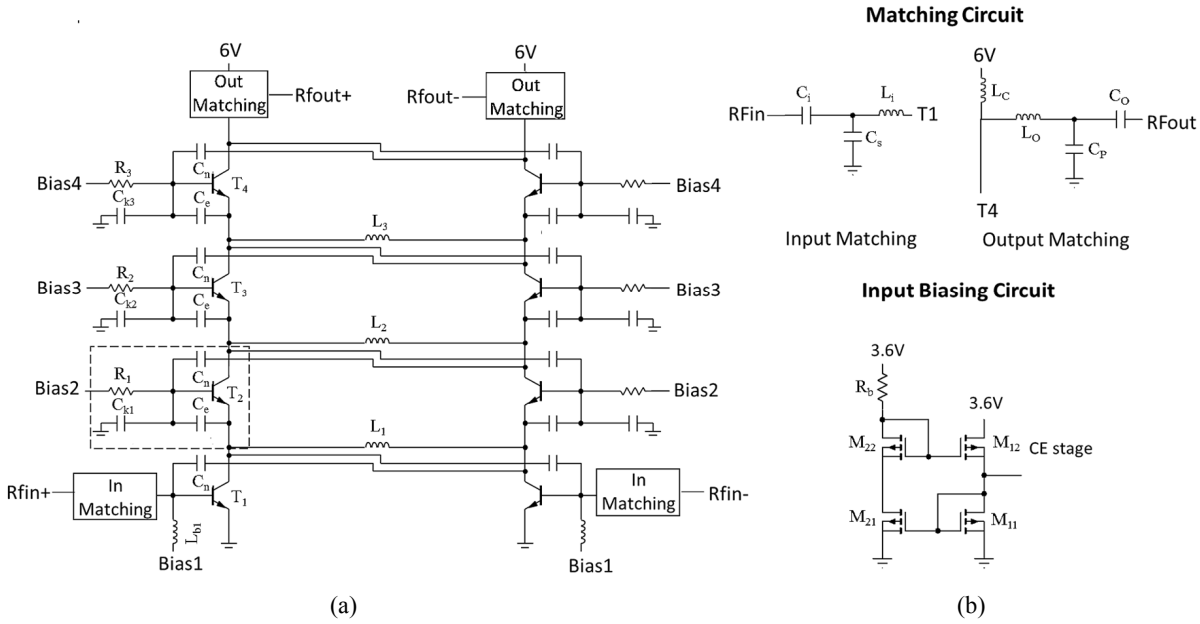


Figure 1. Simplified circuit schematic of proposed power amplifier.

using emitter follower, M_{12} to extend circuit operation beyond breakdown voltage, BV_{CEO} of 2.2V (nominal). In order to avoid potential oscillation issue, a 4pF bypassing capacitor is also connected to 6V supply node. The voltage swing at each device is limited to approximately 3V for breakdown concern. Next, the operation principle of common base stage highlighted by dotted box in Figure 1(a) is described. As compared to conventional approaches, two capacitive elements (C_e, C_n) are introduced in the transistor

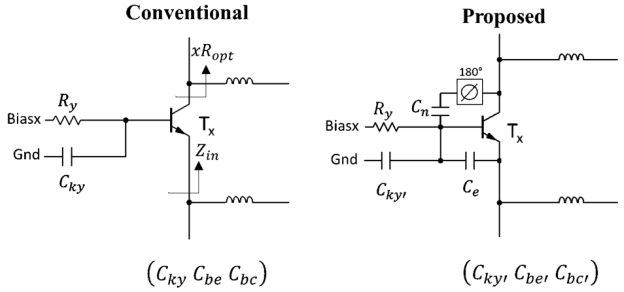


Figure 2. Schematic of conventional and proposed common base stage of stacking PA.

cell to improve gain and isolation performance of the PA. Figure 2 shows the enlarged schematic view of conventional and proposed CB transistor stage in stack PA where the optimum input impedance, Z_{in} for power matching of previous stage is controlled by adjusting the base capacitor, C_{ky} (1).

$$Z_{in} \approx \frac{1+C_{be}/(C_{ky}+C_{bc})}{g_m} + \frac{xR_{opt}}{1+C_{ky}/C_{bc}} \quad (1)$$

$$C_{ky} \approx \frac{C_{be}+C_{bc}[1+g_m R_{opt}]}{g_m R_{opt}(\mathrm{x}-1)-1} \quad (2)$$

$$Y_{12} = sC_{ce} + \frac{g_m+sC_{be}}{1+(C_{ky}+C_{be})/C_{bc}} \quad (3)$$

$$A_{v-CB} \approx 1 + \frac{g_m/sC_{bc}-1}{(1/sC_{ky})(g_m+sC_{be})+1} \quad (4)$$

$$A_{i-CB} \approx 1 - \frac{sC_{be}}{(1+C_{bc}/C_{ky})(g_m+sC_{be})} \quad (5)$$

Where, $y = 1, 2\ or\ 3$, C_{bc} and C_{be} are the parasitic base capacitances whereas g_m is the transistor transconductance.

The value of C_{ky} increases inversely with optimum load impedance, R_{opt} and stacking stage x. However, finite C_{ky} translates directly to poorer reverse isolation admittance, Y_{12} and voltage gain, $A_{v\text{-}CB}$ as revealed in the equations (3), (4). Nevertheless, it has much less impact on current gain, $A_{i\text{-}CB}$ particularly for the case where $C_{bc}/C_{ky} << 1$ in (5). Intuitively, it is desirable to reduce parasitic base collector capacitance, C_{bc} and increase C_{ky} to reduce Y_{12}, improve voltage gain, $A_{v\text{-}CB}$ and thus power gain. The resulted differences in capacitive components of proposed PA are denoted by symbols with prime notations. Comparatively, the issue mentioned is less pronounced in cascode stage since the base terminal is coupled to ground through very large C_{ky}. Decreasing effective base collector capacitance, $C_{bc'}$ for gain considerations is achieved by cross-coupling capacitors, C_n. The cross-coupling path is equivalent to series connection of C_n and a 180-degree phase shifter in single ended version of amplification stage. Meanwhile, increasing base capacitors, C_{ky} require proportional increase in base emitter capacitances, C_{be} to maintain similar input impedance, Z_{in}. This could be visualized from their relationship shown in Figure 2. Therefore, additional capacitors, C_e is added across base and emitter terminals to boost the effective base emitter capacitance, $C_{be'}(C_{be} + C_e)$ with $C_{ky\prime} > C_{ky}$. Its value should be sufficiently small to

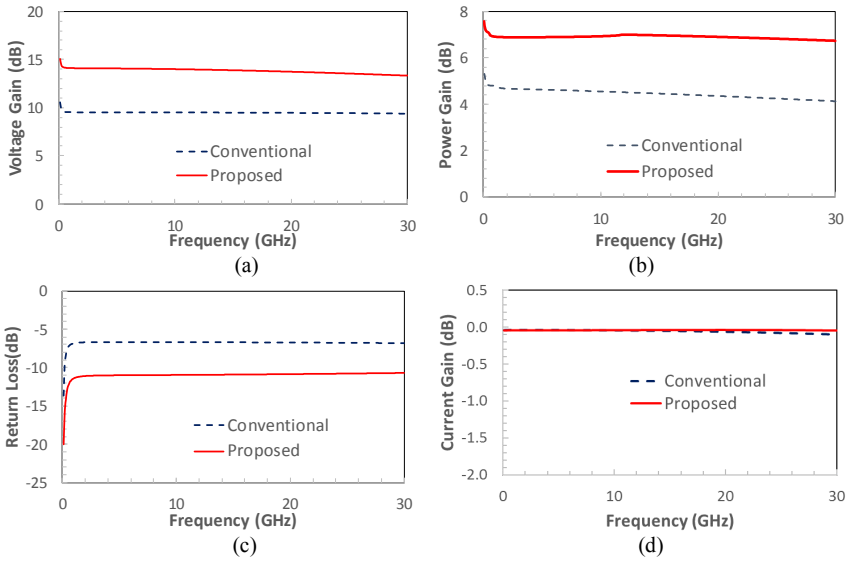


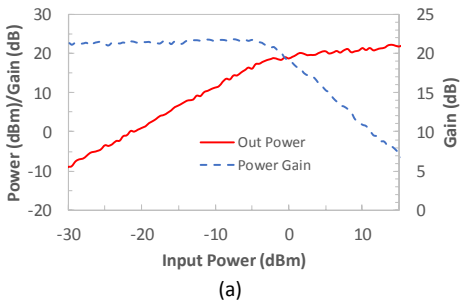
Figure 3. Performance comparison of conventional and proposed CB transistor stage in stack PA versus frequencies.

have minimal impact on current gain performance at frequency of interest.

Further study by simulation is performed to examine the theoretical inference derived from parametric equations of performance metrics. Figure 3(a)-(d) shows performance comparison of both CB transistor stages discussed by simulation based on same Z_{in}. Note that both reversed isolation, voltage and max power gain performance has been improved (4.09dB, 4.21dB and 2.56dB) with negligible impact on current gain (<0.1dB) at 20GHz. The results successfully validate the circuit concepts applied for performance improvement of stacked PAs. Relatively, the negative influence of C_{BE} on gain performances due to extra C_e chosen (200fF) could be neglected at frequencies below 30GHz.

III. Results and Discussion

The probing interfaces of the PA is designed to support on-wafer power and RF measurements by Keysight E8267D signal generator, R&SFSW67 spectrum analyzer and N5247A PNA-X. Figure 4(a)-(c) shows various simulated power and RF performance metrics of stacked PA presented. It achieves impressive power gain of 21.7dB at linear region with saturated power, Psat of 22.2dBm and peak PAE of 26% at Pout=26.8dBm. Also, max voltage gain of 34.4dB, max insertion gain, S_{21} of 20.3dB and max current of 21.3dB are attained within K-band.



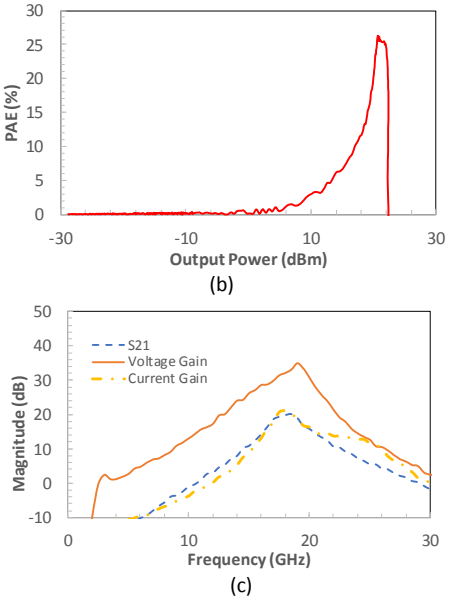


Figure 4. (a) Output power and large signal power gain, (b) PAE at 20GHz and (c) small signal gains versus frequencies.

As shown in Figure 5, the SiGe PA presented occupies area of 0.71x0.75mm^2 where both RF ports are fed by differential signals through GSGSG pads and external baluns. All transistors are biased independently through DC pads to promote precision control.

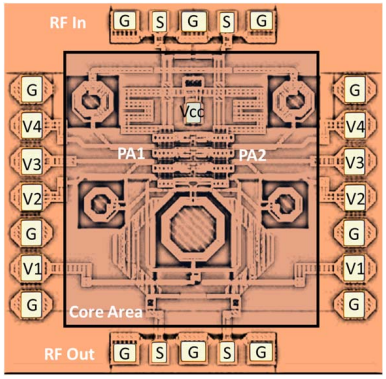


Figure 5. Circuit layout of 0.18µm SiGe PA presented.

Table 1 shows benchmark comparison of PA presented against recent state of art PAs that operate approximately around K-band (18GHz to 29GHz). It shows more favorable gain performance against stacked PAs compared while achieving competitive PAE and Psat. Meanwhile, 25% more area is required by cascode PAs [1] to attain power>20dBm and high gain of >20dB using parallel power combining technique.

IV. Conclusion

A K-band stacked SiGe power amplifier that is based on new design of common base amplification stages is presented. The design proposed encompasses both capacitive neutralization and compensation methods introduced at the base-collector junction and base-emitter junction respectively. The impact of such circuit techniques on improvement in gain performance has been proven theoretically and validated by simulations. It demonstrates output power of >22dBm and employs differential topology for stability concern. Further comparisons show that it exhibits the best power gain performance among stacked power amplifiers in similar band.

TABLE I

Performance comparison with recent PAs that operate around K-band (18GHz to 29GHz)

Reference	Freq (GHz)	Architecture	Area/mm^2	Gain (dB)	P_{1dB} (dBm)	Psat (dBm)	Peak PAE (%)	Technology
This work	20	Differential 4-stacked	0.53	21.17	20.8	22.2	26	0.18µm SiGe
[1]	28	2 stages cascode, 4-way parallel combined	0.71	28.6	23.2	23.7	32.7	0.18µm SiGe
[2]	24	3-stacked, 3-way series combined	0.28	13	23.8	25.3	20	45nm CMOS SOI
[3]	27	2 stages common source	0.23	22.4		15.1	33.7	40nm CMOS
[5]	18	Dynamically-biased 3-stacked cascode (6 FETs)	0.16	≈5.5	13.7	26.1	11	45nm CMOS SOI
[6]	29	4-stack multigate-cell	0.30	13	≈24	24.8	29	45nm CMOS SOI
[7]	24	3-stacked	Unavailable	12.2	≈13.5	17.5	20.5	0.13µm CMOS

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