A 65nm CMOS 30dBm Class-E RF Power Amplifier with 60% Power Added Efficiency

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Abstract — **A 30dBm single-ended class-E RF power amplifier (PA) is fabricated in 65nm CMOS technology. The PA is a cascode stage formed by a standard thin-oxide device and a high voltage extended-drain thick-oxide device. Both devices are implemented in a standard sub-micron CMOS technology without using extra masks or processing steps. The proposed PA uses an innovative self-biasing technique to ensure high power-added efficiency (PAE) at both high output power (Pout) and power back-off levels. At 2GHz, the PA achieves a PAE of 60% at a Pout of 30dBm and a PAE of 40% at 16dB back-off.**

Index Terms — **CMOS PA, class-E, cascode, PAE, self-biasing technique, driver stage, HV device.**

I. Introduction

Implementing a watt-level highly efficient PA in deep sub-micron CMOS is a challenging task due to the low breakdown voltage and the lossy substrate that characterize these technologies. There are currently two main PA architectures proposed by the design community to generate high output power. In the first architecture, the output power levels of several low to medium power PAs are combined to generate a total high output power while at a low supply voltage [1]-[3]. However, the efficiency of these power combining designs is lower than 40% due to the highly lossy substrate of the CMOS technology [1, 3] unless high quality external transformers are used [2]. In the second architecture, thick-oxide transistors are stacked in a cascode configuration to eliminate the effects of oxide breakdown voltage and make use of a larger supply voltage. [4, 5]. The disadvantage in using thick-oxide transistors in a cascode is its limited RF performance. However, at constant output power levels, the alleviated supply voltage allows for a larger load impedance, which relaxes the requirements on the impedance transformation.

In this paper, we present a 65nm CMOS RF PA that is able to deliver 30dBm power with 60% PAE at 2GHz. The proposed fast-switching PA is a cascode class-E topology. The maximum frequency of operation is increased by using a standard thin-oxide transistor as the common-source (CS) device and the output power is extended by making use of a high voltage extended-drain MOSFET device (ED-NMOS) as the common-gate (CG) device. The ED-NMOS can sustain drain voltages as high as 15V. Additionally, we make use of the self-bias cascode topology in [6] to improve the efficiency. We extend this topology to improve PAE at large back-off power levels, hence addressing applications that make use of polar modulation or linearization techniques such as envelope tracking (ET) and envelope elimination and restoration (EER).

II. Technology and ED-NMOS Device

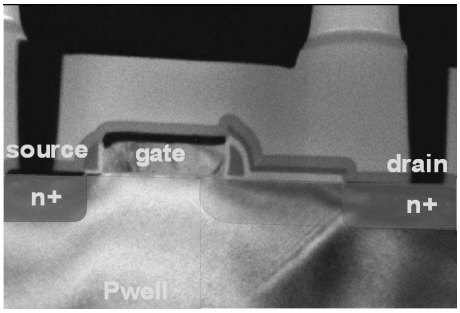

Figure 1. Cross sections of the innovative ED-NMOS device.

The PA is fabricated in the standard 65nm LP CMOS technology that offers dual gate oxide and up to 7 metal layers. The large number of process steps and masks, the fine lithography dimensions and alignment, and the CMOS scaling features allow construction of novel transistors, including high voltage extended-drain MOSFETs [7]. Such structures can be mixed with both 1.2V and 2.5V gate oxides. The high voltage NMOS transistor used in our class-E PA circuit features a non-silicided drain-extension (see Fig. 1) and 2.5V gate oxide. This ED-NMOS has an off-state breakdown voltage of 15V and operates safely up to at least 8V in on-state. It has a threshold voltage of 0.8V and low conduction losses with an on-resistance of 2.8mΩ.mm^2. The measured f_T and f_{max} exceed 30 and 50GHz, respectively.

III. Circuit Design

The class-E PA consists of a driver stage and a main cascode stage.

A. Cascode Class-E PA

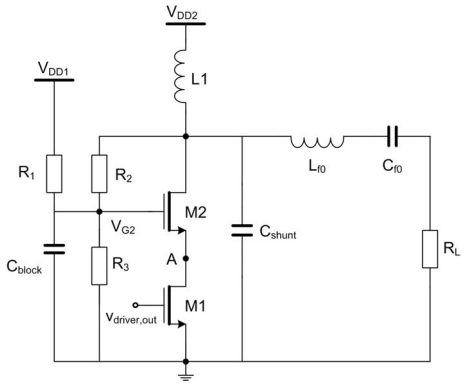

Figure 2. Schematic of the cascode class-E PA with a self-biasing and output matching network.

Since efficiency and high output power are of primary concern, we chose to implement a class-E PA which delivers theoretically the maximum output power at a fixed current as compared to other switch-mode amplifier classes [8]. The conditions of operation in class-E (hard switching operation and zero-voltage switching condition [8]) allow for a great reduction in power losses, and the tuning of harmonic load impedances is far less sophisticated than in classes relying on tuning of harmonic impedances.

Thanks to the ED-NMOS device, we can increase the supply voltage to reach high P_{out} levels (i.e., 30dBm). By going to higher supply voltages, one decreases the power loss in both the driver and the matching network [5]. Although the ED-NMOS can be stressed to high voltages as a stand-alone device, we chose to implement a cascode stage, see Fig. 2. The cascode topology combines the best of two worlds: the switching capability of the thin-oxide device M1, used as the CS transistor, and the high voltage sustainability of the novel ED-NMOS device M2, used as the CG transistor. M1 has better RF characteristics and therefore it simplifies the design of the driving stage. Additionally, M1 presents lower values of parasitic capacitances at node A. Hence, it introduces smaller losses associated with the charging and discharging of these capacitances as compared to the cascode build up by two thick-oxide devices. The width of the CS device is set to deliver the required switching current and to match its output impedance to the input impedance of the CG device. The required output power level and the breakdown voltage of the ED-NMOS device set the maximum load impedance R_L. The value of R_L fixes the value of the total current and the shunt capacitance C_{shunt} [8] required for class-E operation.

The CG transistor is biased so as to be always ON. That keeps the values of on-resistance low, thus limiting the losses and improving efficiency. Traditionally, the self-biased cascode configuration [6] was introduced to optimally divide the voltage swing across the CS and CG transistors for higher output power and efficiency within the breakdown limits of the device. However, in architectures that require envelope tracking, the output power, efficiency and gain become a function of the supply voltage. At lower supply voltages V_{DD2} (see Fig. 2), the linearity and efficiency drop because the voltage applied at the gate of the CG transistor is insufficient and hence the cascode device turns off. This problem can be solved by biasing the gate of the cascode transistor separately using a fixed gate supply voltage, see Fig. 2. Fig. 3 depicts the power

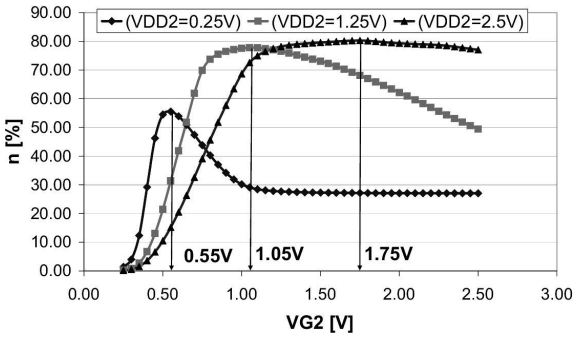

Figure 3. Simulated power efficiency as function of cascode gate voltage V_{G2} for three different drain supply voltages V_{DD2}.

efficiency of the PA as a function of the gate voltage of the CS transistor V_{G2} and for different drain supply voltages V_{DD2}. The graphs reveal that there is an optimum V_{G2} for each V_{DD2}. In fact, the optimum V_{G2} changes linearly with the output supply voltage V_{DD2}. In Fig. 2, V_{G2} is linearly related to V_{DD2} by means of the 3-resistor voltage divider circuit, R_1, R_2 and R_3. Furthermore, the capacitor C_{block}, together with the total effective resistance, realizes a low pass filter with a pole at V_{G2} chosen for optimum self-biasing [6].

B. Driver Stage

To drive the cascode efficiently, one needs to drive the thin-oxide device into saturation with a square-wave signal. We implement an inverter-based driver, see Fig. 4, which has sufficient drive capability and an input impedance of 50Ω, to minimize the return loss.

IV. Implementation and Measurements

The proposed cascode class-E PA including the driver was implemented in a 65nm CMOS technology. We implemented two versions of this cascode PA, one using the standard thick-oxide (GO2) device and another using the

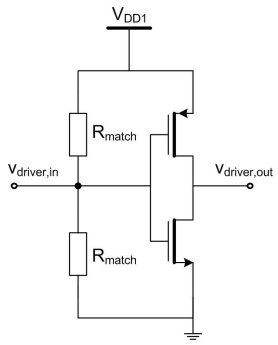

Figure 4. Schematic of the driver.

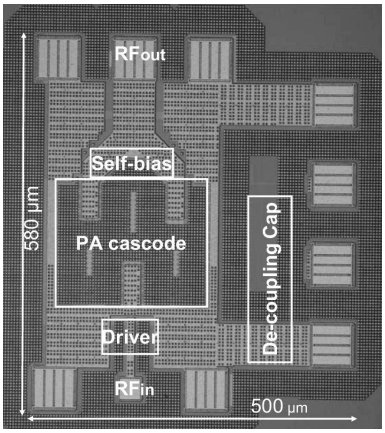

Figure 5. Chip photo of the class-E PA.

ED-NMOS device as the CG transistor. This was done to verify the advantages in using the ED-NMOS instead of the GO2 NMOS device. Further, we decided to avoid integrating passive components, so as to allow the maximum freedom in experimenting with the cascode PA and its breakdown and frequency limits. Fig. 5 shows a photo of the fabricated chip. The die size is 0.3mm^2. The output capacitance required for class-E operation was simulated to be 2.5pF. There was no need to include a shunt capacitor on the chip, since the output capacitance of the cascode PA (including interconnect parasitics) matched the required value.

Using our active load-pull measurement set-up similar to [9], we first characterize the operation of both PA versions in terms of P_{out} and PAE. Fig. 6 plots P_{out} and PAE as functions of supply voltage V_{DD2} at 2GHz continuous wave operation. The sharp reduction in PAE of the GO2 implementation at $V_{DD2} = 3$V marks the device's breakdown limit. On the other hand, the ED-NMOS implementation reaches 30dBm output power at $V_{DD2} =$ 4.8V and with a PAE as high as 60%, under the same conditions of operation (input frequency f_{in} =2GHz and driving power $P_{in} = 5.5$dBm). In the following we concentrate on the performance of the ED-NMOS implementation only. Fig. 6 also demonstrates that the PA exhibits a 58% PAE at 8dB back-off and a 40% PAE at 16dB back-off. Fig. 7 depicts the power gain G_p and PAE of the ED-NMOS PA as a function of P_{in}. Maximum efficiency is achieved at $P_{in} = 5.5$dBm, where G_p is greater than 25dB. Fig. 8 shows that at fixed $P_{in} = 5.5$dBm and for 14dBm $\leq P_{out} \leq$ 30dBm, P_{out} is linearly related to $\log V_{DD2}$ which is required for polar modulation.

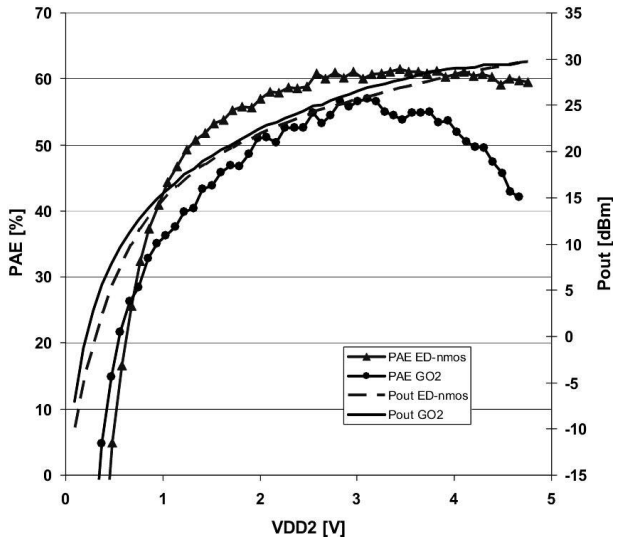

Figure 6. P_{out} and PAE as function of V_{DD2} at 2GHz.

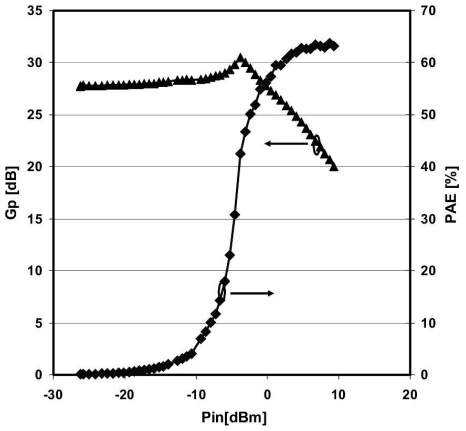

Figure 7. G_p and PAE as function of P_{in} at $V_{DD2} = 4.75$V and 2GHz.

To further demonstrate the reliability of the ED-NMOS cascode PA implementation, we operate the PA at high V_{DD2} levels for a long time. We measure continuously the PAE and P_{out} performance while gradually increasing V_{DD2} from 3V up to 5V every 8.5 hours. Fig. 9 shows that after 34 hours of operation, the PA still operates at 5V supply without any observable degradation in P_{out} and

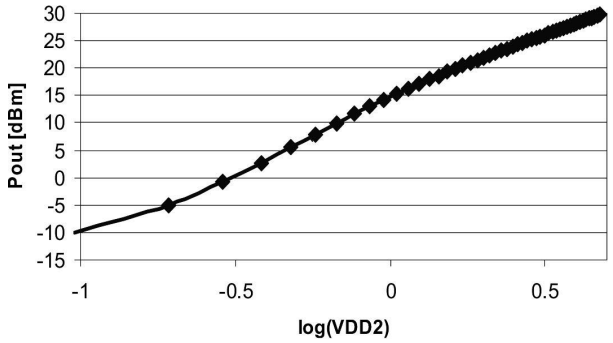

Figure 8. P_{out} as function of $\log V_{DD2}$ at P_{in} = 5.5dBm and 2GHz.

PAE. The minor decrease in PAE is due to contact degradation. When we restore the contact by scratching instantly the probe on the bondpad, the PAE returns to its values at the start of this experiment (see the jump in PAE when going from 4V to 5V supply). The reliability at high voltage supplies allows us to directly connect this PA to lithium battery.

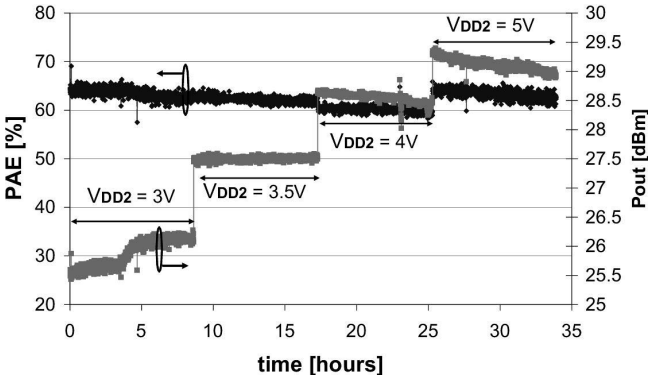

Figure 9. Output power and power added efficiency as function of supply levels at 2 GHz of operation.

Finally the performance of the class-E ED-NMOS based PA of this work is compared to published state-of-the-art watt-level CMOS PAs at different frequencies of operation, see Table 1.

V. Conclusions

The cascode class-E PA described utilizes an innovative extended-drain NMOS device ED-NMOS to permit the use of high supply voltages and a thin-oxide device for relaxing the requirements on the driver. To the best of our knowledge, this is the first 1-Watt PA implemented in the standard sub-micron 65nm CMOS technology. The PAE is greater than 60% when delivering 1-Watt output power for frequencies in the range of 0.8-2GHz. The proposed innovative self-biasing technique ensures a high PAE at large power back-off levels. At 2GHz operation, the PA achieves PAE of 40% at 16dB back-off. We did not observe any performance degradation after stressing the device at supply voltages as high as 5V and for 34 hours.

Table 1. COMPARISON OF CMOS PAs.

Design	Freq. (MHz)	Pout (W)	PAE (%)	Gain (dB)	process (nm)
[10]	855	1	60	$N.A.$	350
[2]	875	1.48	62	30.3	180
[3]	1900	1.6	40	27	180
[4]	1700	1.26	58	$N.A.$	130
this work	800	1	70	27	65
this work	2000	1	60	25	65

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