

**Gebze Technical University
Computer Engineering**

CSE 331 - 2018 Fall

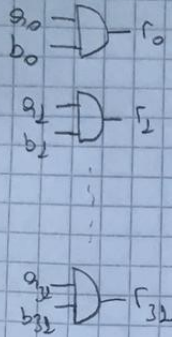
HOMEWORK 2 REPORT

**EMİRHAN KARAGÖZOĞLU
151044052**

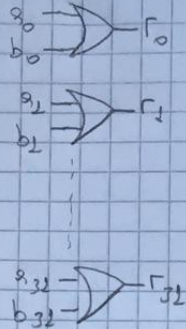
Course Assistant: Fatma Nur Esirci

Schematic Desings for all Modules

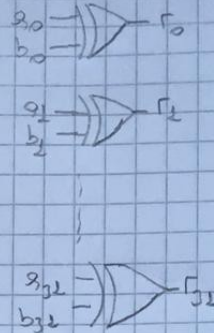
AND



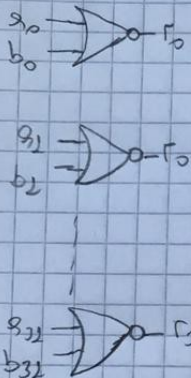
OR



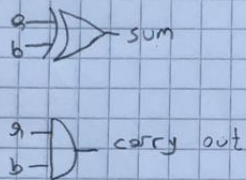
XOR



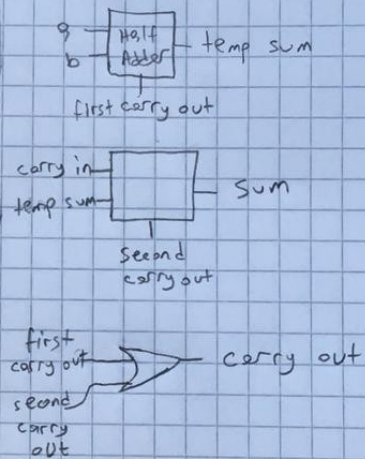
NOR



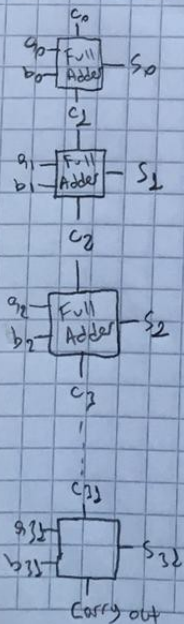
Half Adder



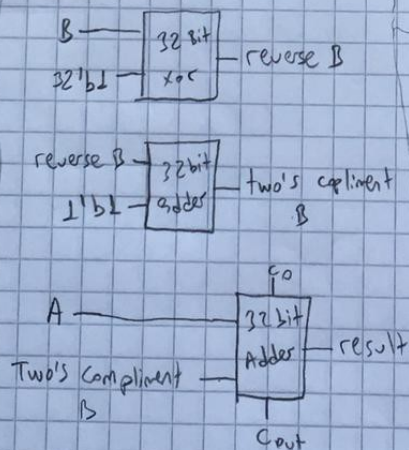
Full Adder



32 Bit Adder



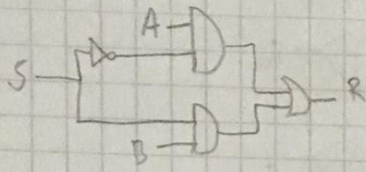
32 Bit Subtractor



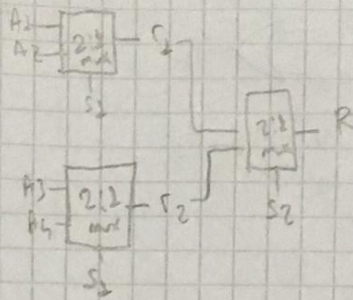
⇒ 32 Bit Adder's carry out
1 is overflow verdict.

⇒ 32 Bit Subtractor's carry out
0 is overflow verdict.

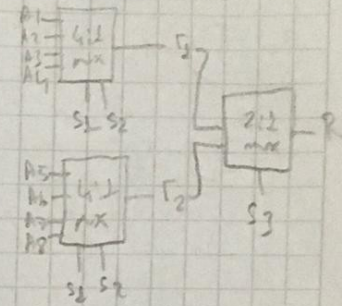
2:1 Mux



4:1 Mux

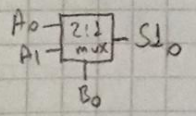
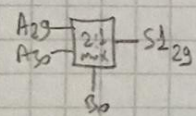
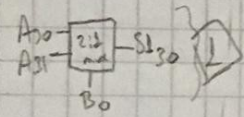
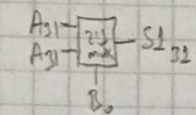


8:1 Mux

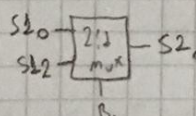
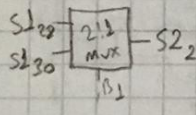
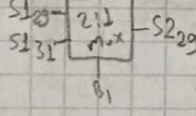
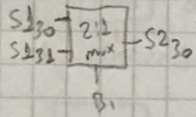
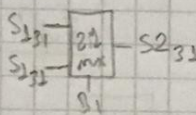


Arithmetic Right Shift

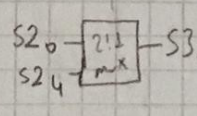
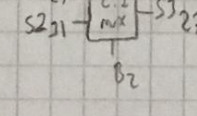
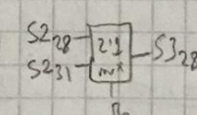
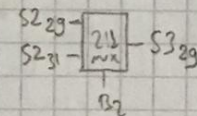
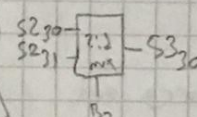
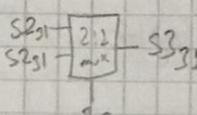
Level 0



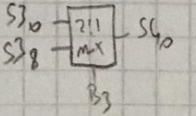
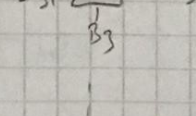
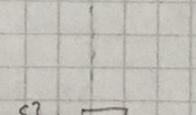
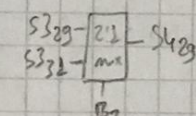
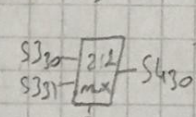
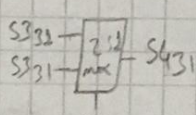
Level 1



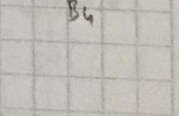
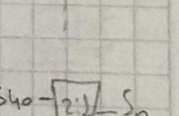
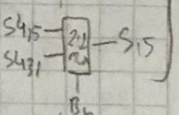
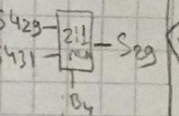
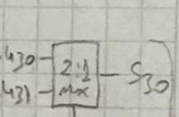
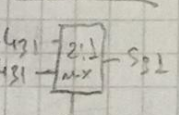
Level 2

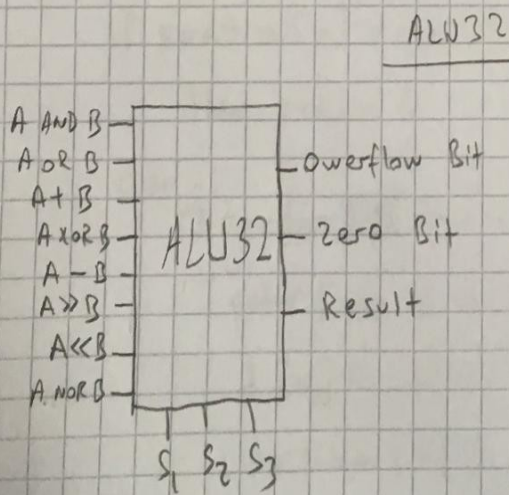
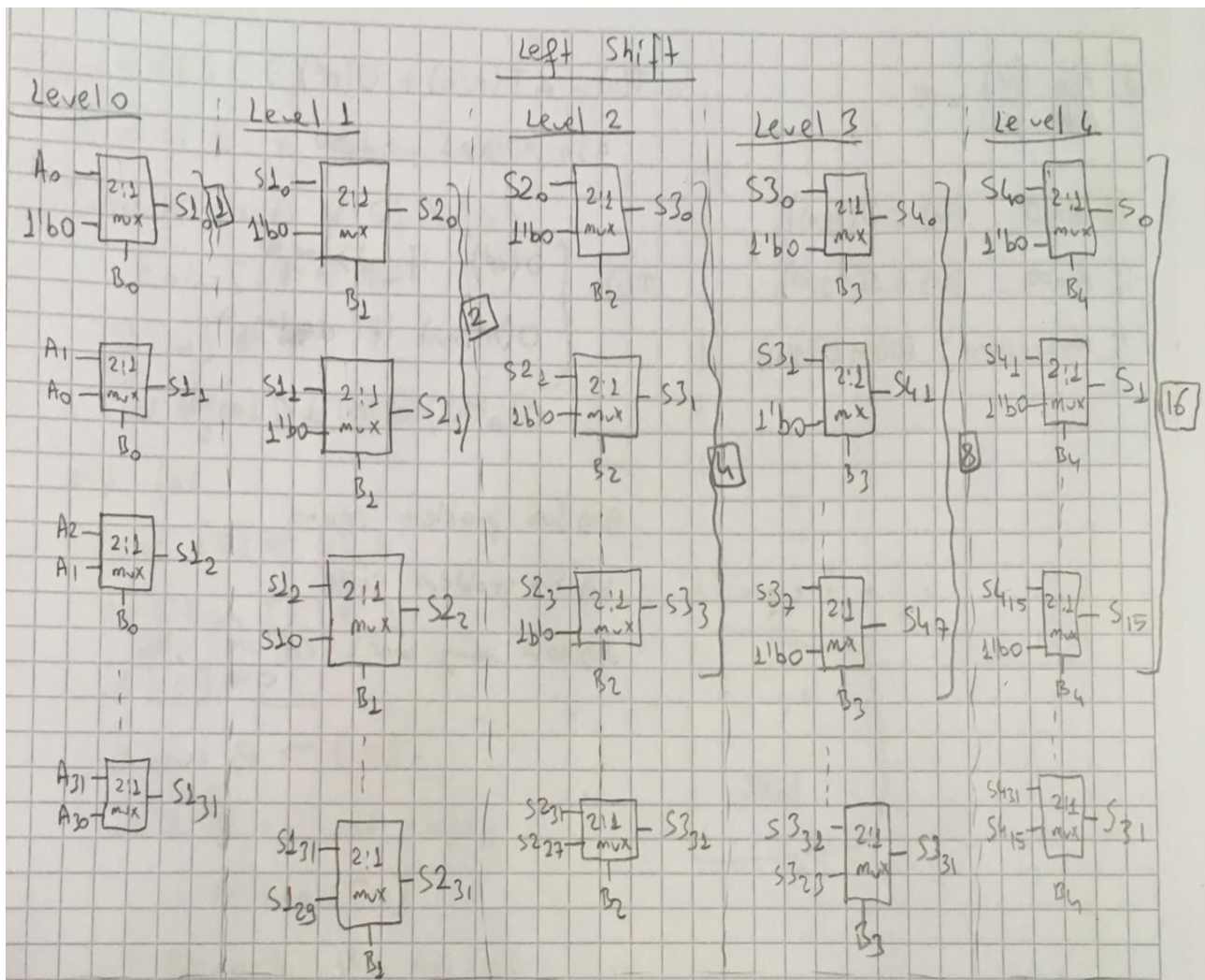


Level 3



Level 4





Verilog Modules and Their Description

AND : 32 bit 2 adet sayı alır AND işlemi yapar ve 32 bit sonuç return eder.

OR : 32 bit 2 adet sayı alır OR işlemi yapar ve 32 bit sonuç return eder.

NOR : 32 bit 2 adet sayı alır NOR işlemi yapar ve 32 bit sonuç return eder.

XOR : 32 bit 2 adet sayı alır XOR işlemi yapar ve 32 bit sonuç return eder.

+ operator : 32 bit 2 adet sayı alır toplama işlemi yapar ve 32 bit sonuç return eder.

- operator : 32 bit 2 adet sayı alır çıkarma işlemi yapar ve 32 bit sonuç return eder.

>> operator : 32 bit 2 adet sayı alır ilk sayıyı ikinci sayı kadar aritmetik olarak sağa kaydırır.

<< operator : 32 bit 2 adet sayı alır ilk sayıyı ikinci sayı kadar sola kaydırır.

Alu32: 32 bit 2 sayı ve 3 bit seçici alır, seçiciye göre gerekli işlemin sonucunu ,**overflow bitini ve zero bitini** döndürür.

Modelsim Simulation Results

VSIM 5> step -current

```
# time = 0, Operation: 000, A =01010111000000001010000000101110, B=00101010100011100101000101100011, R=00000010000000000000000000100010 Overflow=0, ZeroBit=0
# time = 20, Operation: 000, A =10101010101010101010101010101010, B=01010101010101010101010101010101, R=00000000000000000000000000000000 Overflow=0, ZeroBit=1
# time = 40, Operation: 000, A =11110111000001101000010100100001, B=10110001001000110101000101111010, R=10110001000000100000000100100000 Overflow=0, ZeroBit=0
# time = 60, Operation: 001, A =01010111000000001010000000101110, B=00101010100011100101000101100011, R=01111111100011101111000101101111 Overflow=0, ZeroBit=0
# time = 80, Operation: 001, A =11010111001001001010000000001010, B=10100110010001000010000101101001, R=11110111011001001010000101101011 Overflow=0, ZeroBit=0
# time = 100, Operation: 001, A =11110111000001101000010100100001, B=10110001001000110101000101111010, R=11110111001001111101010101111011 Overflow=0, ZeroBit=0
# time = 120, Operation: 010, A =01000000000000000000000000000000, B=01000000000000000000000000000000, R=10000000000000000000000000000000 Overflow=1, ZeroBit=0
# time = 140, Operation: 010, A =11010111001001001010000000001010, B=10100110010001000010000101101001, R=01111101011010001100000101110011 Overflow=1, ZeroBit=0
# time = 160, Operation: 010, A =11110111000001101000010100100001, B=10110001001000110101000101111010, R=10101000001010011101011010011011 Overflow=0, ZeroBit=0
# time = 180, Operation: 011, A =01010111000000001010000000101110, B=00101010100011100101000101100011, R=01111101100011101111000101001101 Overflow=0, ZeroBit=0
# time = 200, Operation: 011, A =11010111001001001010000000001010, B=10100110010001000010000101101001, R=01110001011000001000000101100011 Overflow=0, ZeroBit=0
# time = 220, Operation: 011, A =11110111000001101000010100100001, B=10110001001000110101000101111010, R=01000110001001011101010001011011 Overflow=0, ZeroBit=0
# time = 240, Operation: 100, A =11010111001001001010000000001010, B=10100110010001000010000101101001, R=00110000111000000111111010100001 Overflow=1, ZeroBit=0
# time = 260, Operation: 100, A =0000000000000000000000000000100000, B=00000000000000000000000000000010, R=00000000000000000000000000001110 Overflow=0, ZeroBit=0
# time = 280, Operation: 100, A =000000001001000000000000001110000, B=00000000000000010000000000000000, R=0000000010001111100000001110000 Overflow=0, ZeroBit=0
# time = 300, Operation: 101, A =01010111000000001010000000101110, B=00000000000000000000000000000001, R=00101011100000000101000000010111 Overflow=0, ZeroBit=0
# time = 320, Operation: 101, A =11010111001001001010000000001010, B=00000000000000000000000000000001, R=11111010111001001001010000000001 Overflow=0, ZeroBit=0
# time = 340, Operation: 101, A =11110111000001101000010100100001, B=00000000000000000000000000001011, R=111111111111111101110000011010000 Overflow=0, ZeroBit=0
# time = 360, Operation: 110, A =01010111000000001010000000101110, B=00000000000000000000000000000001, R=10101110000000010100000001011100 Overflow=0, ZeroBit=0
# time = 380, Operation: 110, A =11010111001001001010000000001010, B=00000000000000000000000000000001, R=10111001001001010000000001010000 Overflow=0, ZeroBit=0
# time = 400, Operation: 110, A =11110111000001101000010100100001, B=00000000000000000000000000001011, R=00110100001010010000100000000000 Overflow=0, ZeroBit=0
# time = 420, Operation: 111, A =01010111000000001010000000101110, B=00101010100011100101000101100011, R=10000000011100010000111010010000 Overflow=0, ZeroBit=0
# time = 440, Operation: 111, A =11010111001001001010000000001010, B=10100110010001000010000101101001, R=000010001001101010111010010100 Overflow=0, ZeroBit=0
# time = 460, Operation: 111, A =11110111000001101000010100100001, B=10110001001000110101000101111010, R=00001000110110000010101010000100 Overflow=0, ZeroBit=0
```

VSIM 6>