Gebze Technical University
Computer Engineering

CSE 331 - 2018 Fall

HOMEWORK 3 REPORT

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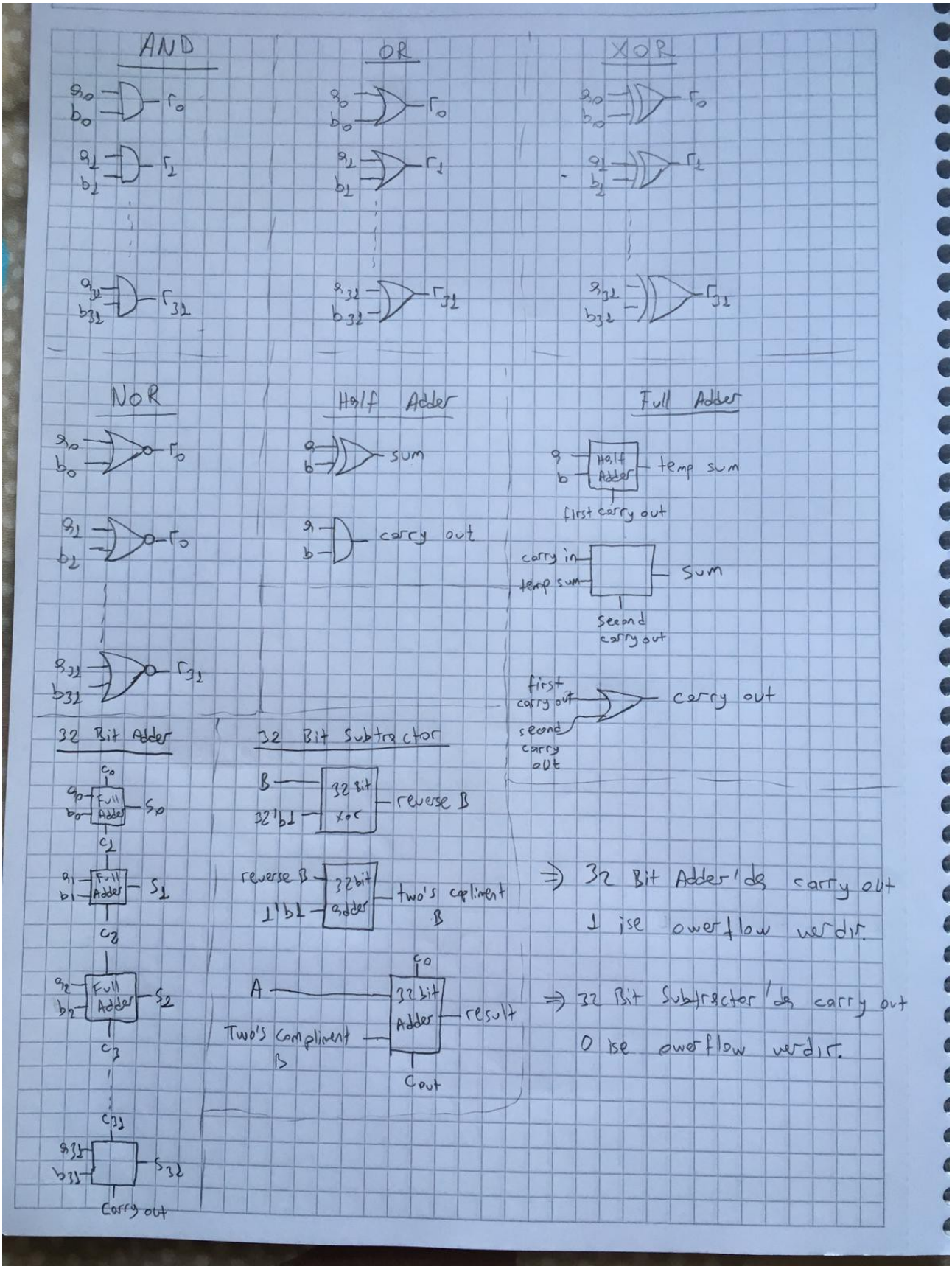
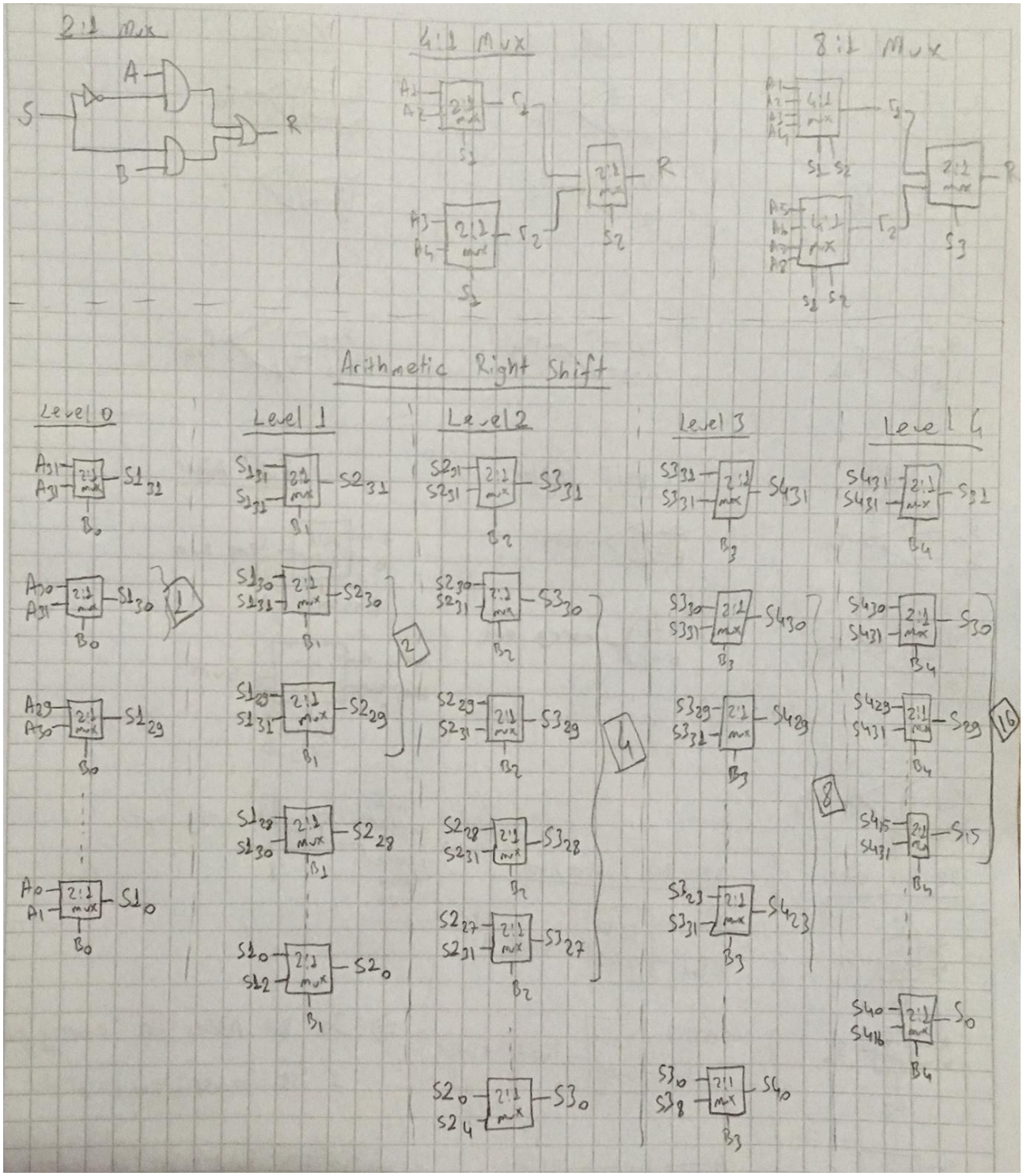
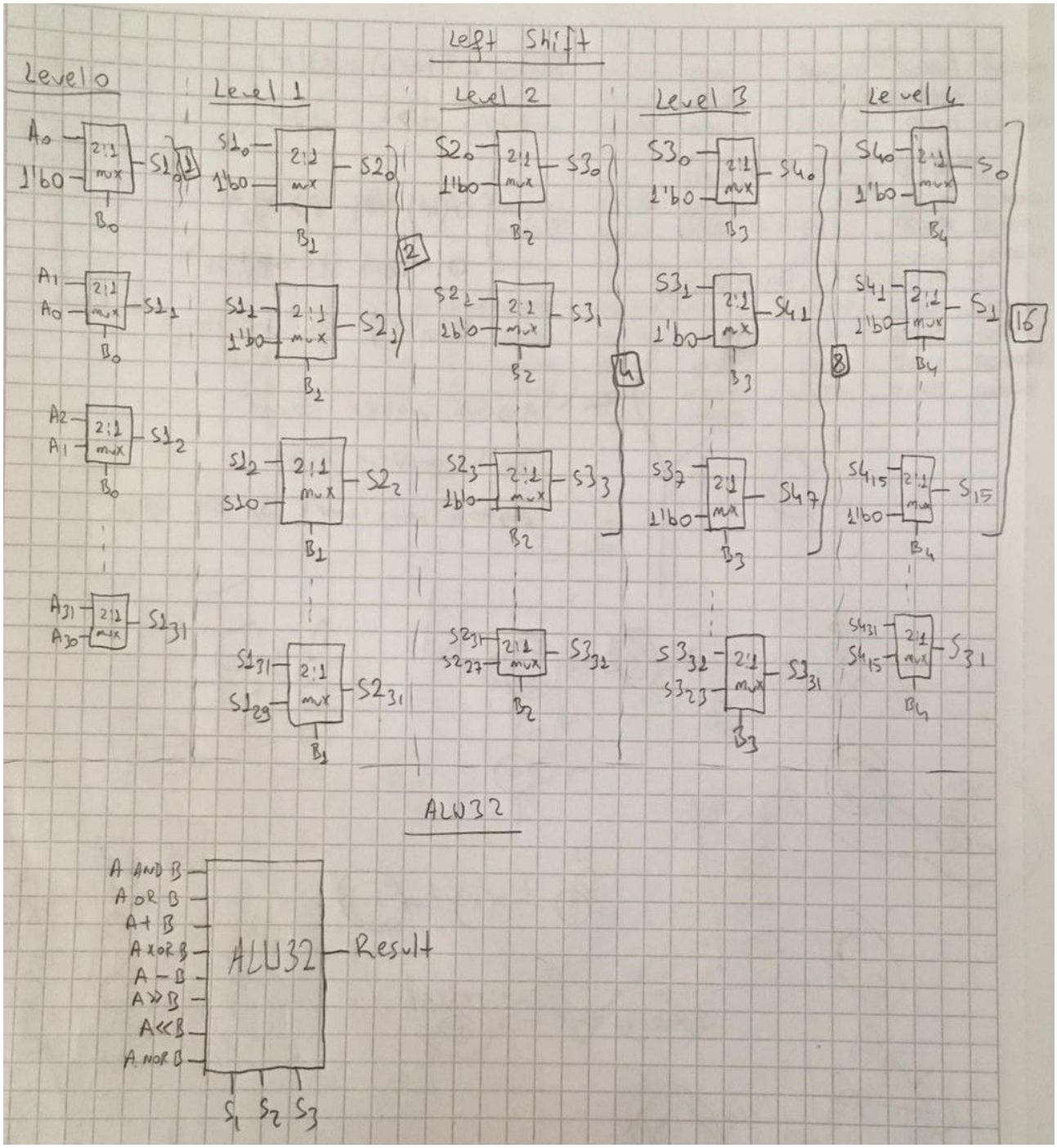
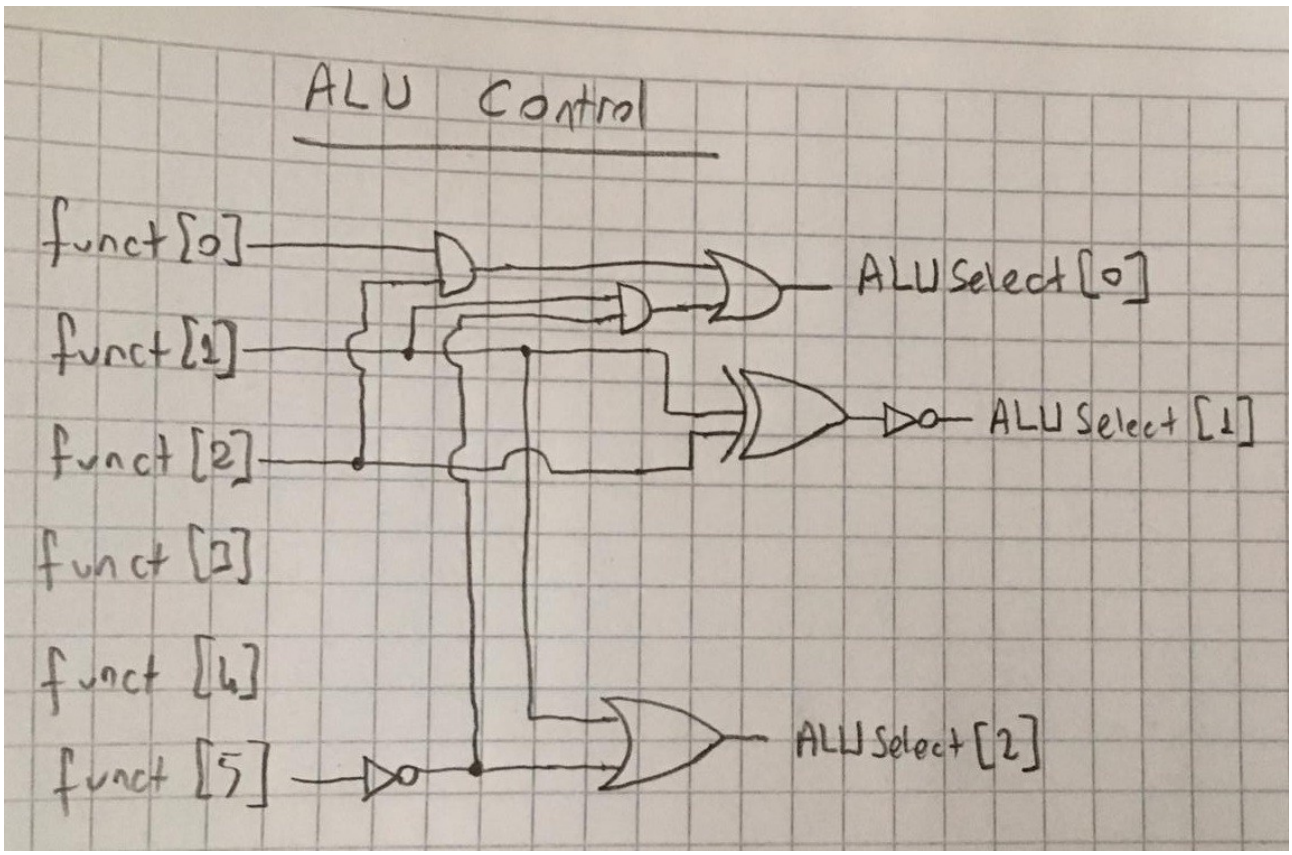
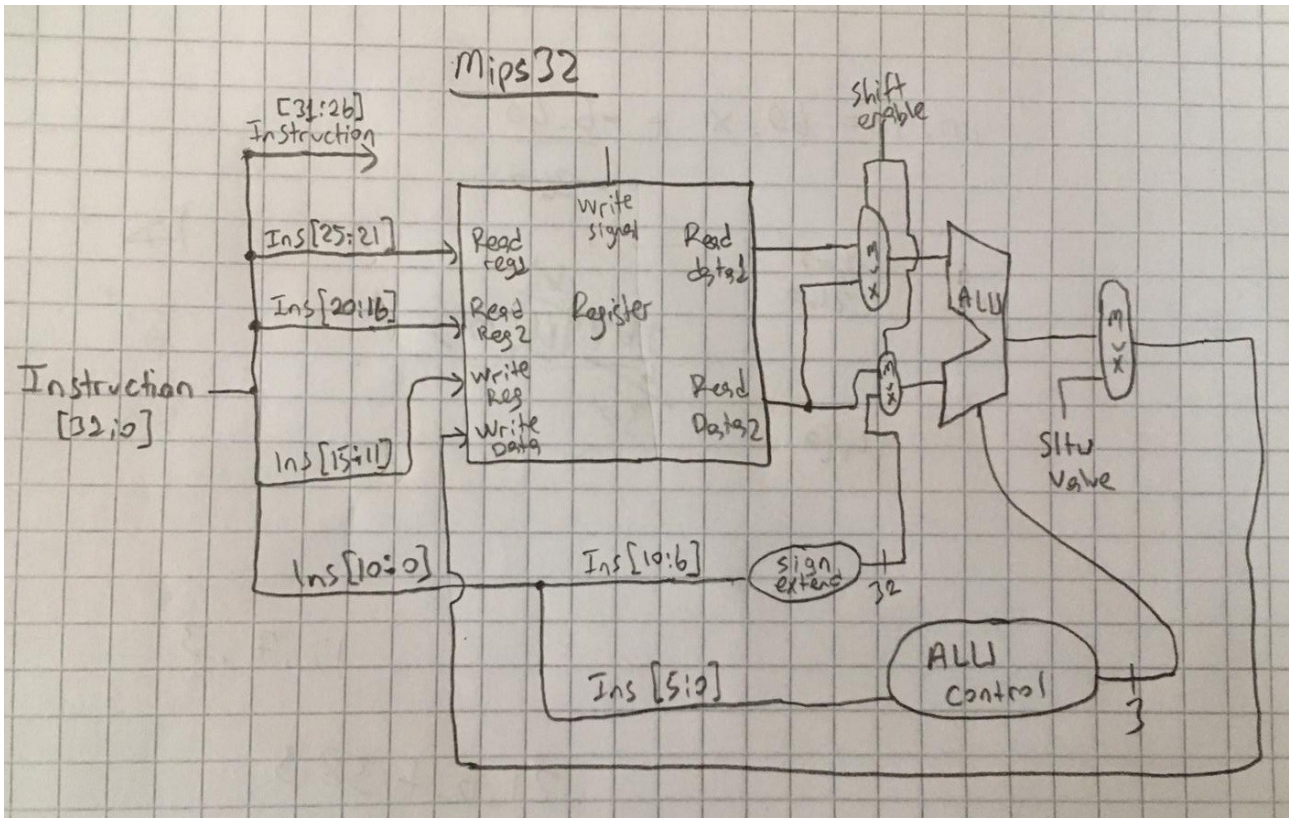
Schematic Desings for all Modules




2:1 mux
A
S
R
B
4:1 MUX
8:1 MUX
Arithmetic Right Shift
Level 0
Level 1
Level 2
Level 3
Level 4
1
2
4
8
16


Left Shift
Level 0
Level 1
Level 2
Level 3
Level 4
ALU32
A AND B
A OR B
A + B
A XOR B
A − B
A >> B
A << B
A NOR B
ALU32
Result
S1
S2
S3


ALU Control
funct [0]
funct [1]
funct [2]
funct [3]
funct [4]
funct [5]
ALU Select [0]
ALU Select [1]
ALU Select [2]


Mips32
[31:26]
Instruction
Ins[25:21]
Ins[20:16]
Instruction
[32:0]
Ins[15:11]
Ins[10:0]
Write signal
Read reg1
Read Reg2
Register
Write Reg
Write Data
Read data1
Read Data2
Shift enable
ALU
Situ Value
Ins[10:6]
sign extend
32
Ins[5:0]
ALU Control
3

Verilog Modules and Their Description

AND : 32 bit 2 adet sayı alır AND işlemi yapar ve 32 bit sonuç return eder.
OR : 32 bit 2 adet sayı alır OR işlemi yapar ve 32 bit sonuç return eder.
NOR : 32 bit 2 adet sayı alır NOR işlemi yapar ve 32 bit sonuç return eder.
XOR : 32 bit 2 adet sayı alır XOR işlemi yapar ve 32 bit sonuç return eder.
+ operator : 32 bit 2 adet sayı alır toplama işlemi yapar ve 32 bit sonuç return eder.
- operator : 32 bit 2 adet sayı alır çıkarma işlemi yapar ve 32 bit sonuç return eder.
>> operator : 32 bit 2 adet sayı alır ilk sayıyı ikinci sayı kadar aritmetik olarak sağa kaydırır.
<< operator : 32 bit 2 adet sayı alır ilk sayıyı ikinci sayı kadar sola kaydırır.
Alu32: 32 bit 2 sayı ve 3 bit seçici alır, seçiciye göre gerekli işlemin sonucunu döndürür.
AluControl: 6 bit function field alır 3 bit alu select döndürür.
RegisterBlock: 5'er bit rs, rt ve rd adresleri alır. Bu adreslerideki rs ve rt contentlerini okuyup döndürür. Ayrıca 32 bit write data ve 1 bit write sinyal alır. Write sinyaline göre rd nin adresine write datayı yazar.
Mips32: 32 bit instruction alır. Bunu R type instruction şeklinde parçalara ayırıp gerekli modüllere gerekli parçaları yollar. Sonuç olarak 32 bit bir result döndürür.

Modelsim Simulation Results

```
VSIM 5> step -current
# time =  0, instruction =00000000100001101010000000100100, result=00000000000000000000000000000010
# time = 10, instruction =00000000100001101011000000100111, result=11111111111111111111111111111100
# time = 20, instruction =00000000100001101100000000100101, result=00000000000000000000000000000011
# time = 30, instruction =00000000100001010110100000100000, result=00000000000000000000000000001001
# time = 40, instruction =00000000100001010111000000100001, result=00000000000000000000000000001001
# time = 50, instruction =00000000101001000111100000100010, result=00000000000000000000000000000001
# time = 60, instruction =00000000101001001000000000100011, result=00000000000000000000000000000001
# time = 70, instruction =00000000100001011000100000101011, result=00000000000000000000000000000001
# time = 80, instruction =00000000110001111001000010000010, result=00000000000000000000000000000001
# time = 90, instruction =00000000110001111001100010000000, result=00000000000000000000000000011100

VSIM 6>
```