CSE 433 Embedded Systems Project 0

Due Date April 3, 2019

Sequence Detector

Detect a sequence of 10111. Assume you will detect only one sequence for 101110111 as the two sequence are intermixed. So you will ignore inter mixed sequences. When the sequence is detected the output will be made 1, otherwise the output will be 0.

- First Draw your State Diagram
- Then draw your State (Truth) Table
- Then design your circuit using structural Verilog.
- Show the accuracy of your design by Modelsim simulation.

BONUS: Implementing on FPGA Board (25pts).

- No FSM = no grade
- Use Quartus II for your Verilog and Modelsim for your simulations.
- State Diagram, State Transition Table, Boolean Expressions must be included in a report.
- Submit your results to Moodle.
- Cheating is at least punished by -100.
- It is NOT a group project.