

Part 1

Part 1

CLK Freq = 100MHz
Period = 10 ns
16 bit Timer = 65536 count

$65536 \cdot 10 \cdot 10^{-9} \cdot X = 500 \cdot 10^{-3}$
↓
 $X = 763$ (min value)

$763 \cdot 10 \cdot 10^{-9} \cdot y = 500 \cdot 10^{-3}$
↓
65530 (we choose min prescaler value so timer count is so close 2^{16})

Additional Software

TIM3 Mode and Configuration

Mode

Slave Mode	Disable
Trigger Source	Disable
Clock Source	Internal Clock
Channel1	Disable
Channel2	Disable
Channel3	Disable
Channel4	Disable
Combined Channels	Disable

☐ Use ETR as Clearing Source

Configuration

Reset Configuration

● NVIC Settings	● DMA Settings
● Parameter Settings	● User Constants

Configure the below parameters :

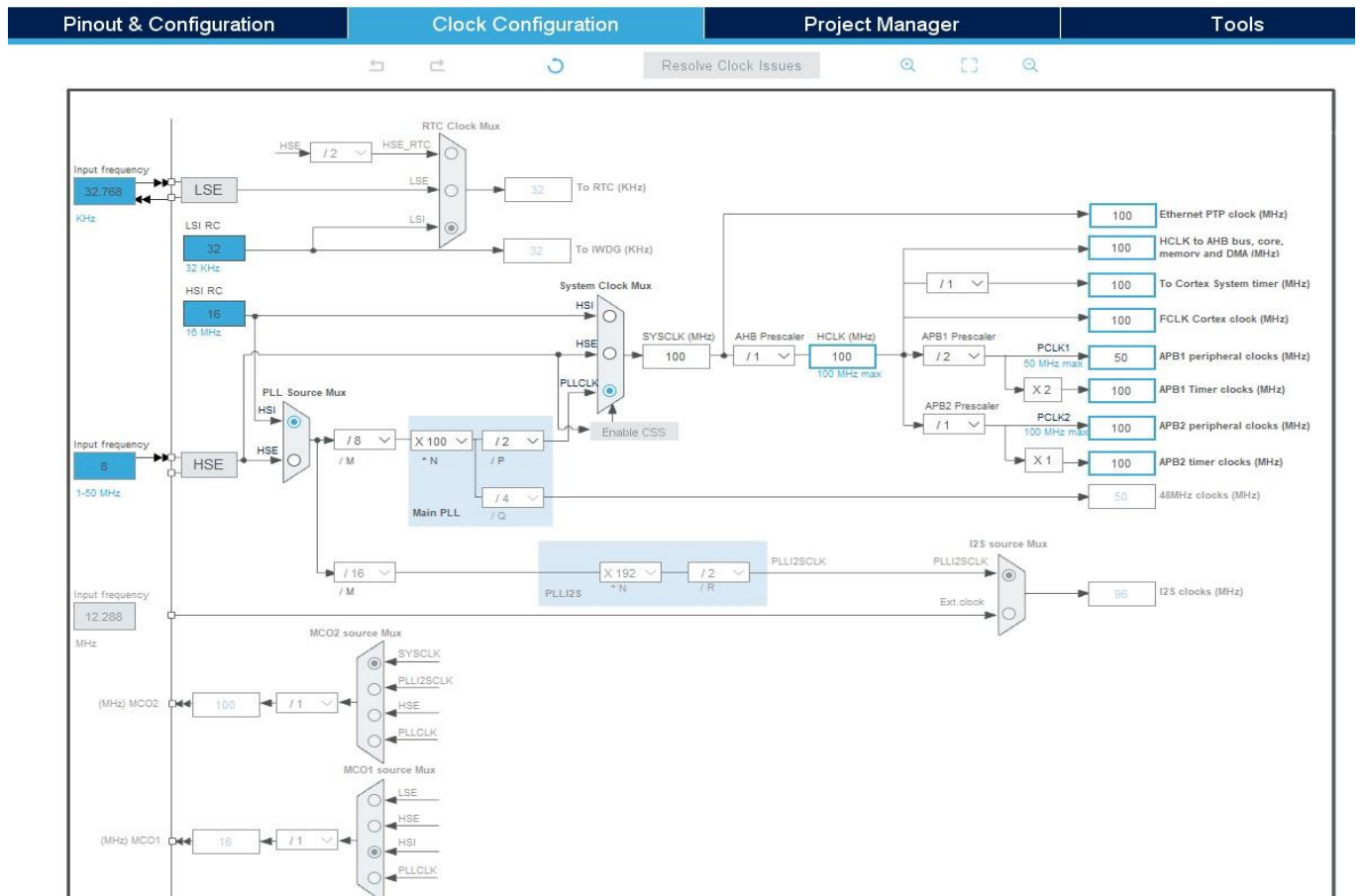
Search (Ctrl+F)

Counter Settings

Prescaler (PSC - 16 bits ...)	763
Counter Mode	Down
Counter Period (AutoRelo...)	65530
Internal Clock Division (C...	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters

Master/Slave Mode (MS...	Disable (Trigger input effect not dela...
Trigger Event Selection	Reset (UG bit from TIMx_EGR)



You can see result of part 1 by watching led blinking.

Part 2

Part 2

CLK Freq = 100 MHz
Prescaler = 10 } 10 MHz \rightarrow Period = 100 ns

$$100 \cdot 10^{-2} \cdot x = 1 \cdot 10^{-3} (1 \text{ ms})$$
$$x = 10000 \text{ pulse}$$

with this clock, every 10000 pulse means 1ms. Every time measured 10000 pulse with output compare, clock make 1 toggle. 1 toggle rise + 1 toggle fall = 1 period. Input capture gets in interrupt when rising edge. Output compare gets in interrupt when rising and falling edge. In output compare interrupt callback function increases pulse value. In one period pulse value will be increased two time but input capture read it one time. So we have to divide by 2 difference between two input capture value.

$$F_{reg} = C \cdot LK / (diff/2)$$

Pinout & Configuration
Pinout
Project Manager
Tools

Categories A->Z

- System Core >
- Analog >
- Timers >
- RTC
 - TIM1
 - ▲ TIM2
 - ▼ TIM3
 - ▼ TIM4
 - ▲ TIM5
 - ▲ TIM9
 - TIM10
 - TIM11
- Connectivity >
- Multimedia >
- Computing >
- Middleware >

TIM4 Mode and Configuration

Mode

Slave Mode Disable

Trigger Source Disable

☒ Internal Clock

Channel1 Disable

Channel2 Disable

Channel3 Output Compare CH3

Channel4 Input Capture direct mode

Combined Channels Disable

☐ XOR activation

Configuration

Reset Configuration

● NVIC Settings
● DMA Settings
● GPIO Settings

● Parameter Settings

▼ Counter Settings

Prescaler (PSC - 16 bits value) 10

Counter Mode Up

Counter Period (AutoReload ...) 50000

Internal Clock Division (CKD) No Division

auto-reload preload Disable

▼ Trigger Output (TRGO) Parameters

Master/Slave Mode (MSM bit) Disable (Trigger input effect not d

Trigger Event Selection Reset (UG bit from TIMx_EGR)

▼ Output Compare Channel 3

Mode Toggle on match

Pulse (16 bits value) 10000

Output compare preload Disable

CH Polarity High

▼ Input Capture Channel 4

Polarity Selection Rising Edge

IC Selection Direct

Prescaler Division Ratio No division

Input Filter (4 bits value) 0

Pinout view

System view

PINS

PB8 OUTPUT COMPARE
PB9 INPUT CAPTURE

VarViewer1		
Variable Name	Address/Expression	Read Value
IC_Value1	0x20000028	10000
IC_Value2	0x2000002c	30000
difference	0x20000030	10000
frequency	0x20000034	1000

Part 2 and part 3 tested together. Generated 1ms square wave was given to input capture and calculated frequency. Implemented code segments are in main.c and stm32f4xx_it.c (TIM4_IRQHandler and TIM3_IRQHandler functions).