CSE 433 Embedded Systems

Project 2

Due Date June 5, 2020

FSM Number Analyzer

In this project you will design an FSM controller using Verilog with Quartus II. The FSM will be able indicate whether a given 32-bit number is an odd or an even number, a Fibonacci number. It will also understand if it is a palindromic number.
(https://en.wikipedia.org/wiki/Palindromic_number)

Simulate your design using Modelsim and Verilog testbench.

- No FSM No grade
- No simulation No grade
- Demo is a MUST.
- Cheating is at least punished by -100.
- It is NOT a group project.