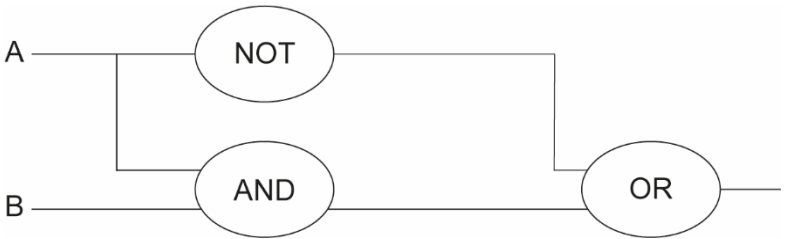
3. *Award **[3 max]**.*

*Award **[1]** for a logic diagram representing A OR B with 2 inputs, 1 output and 3 logic gates.*
*Award **[1]** for the OR gate having 2 inputs, one of which is NOT A.*
*Award **[1]** for another input to the OR gate, which is A AND B.*



[3]