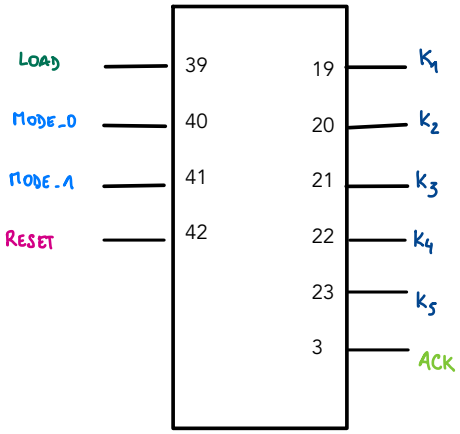
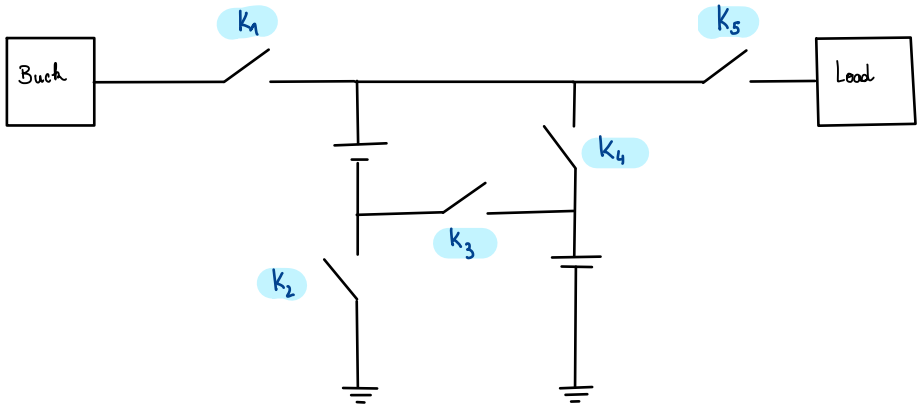
CPLD architecture

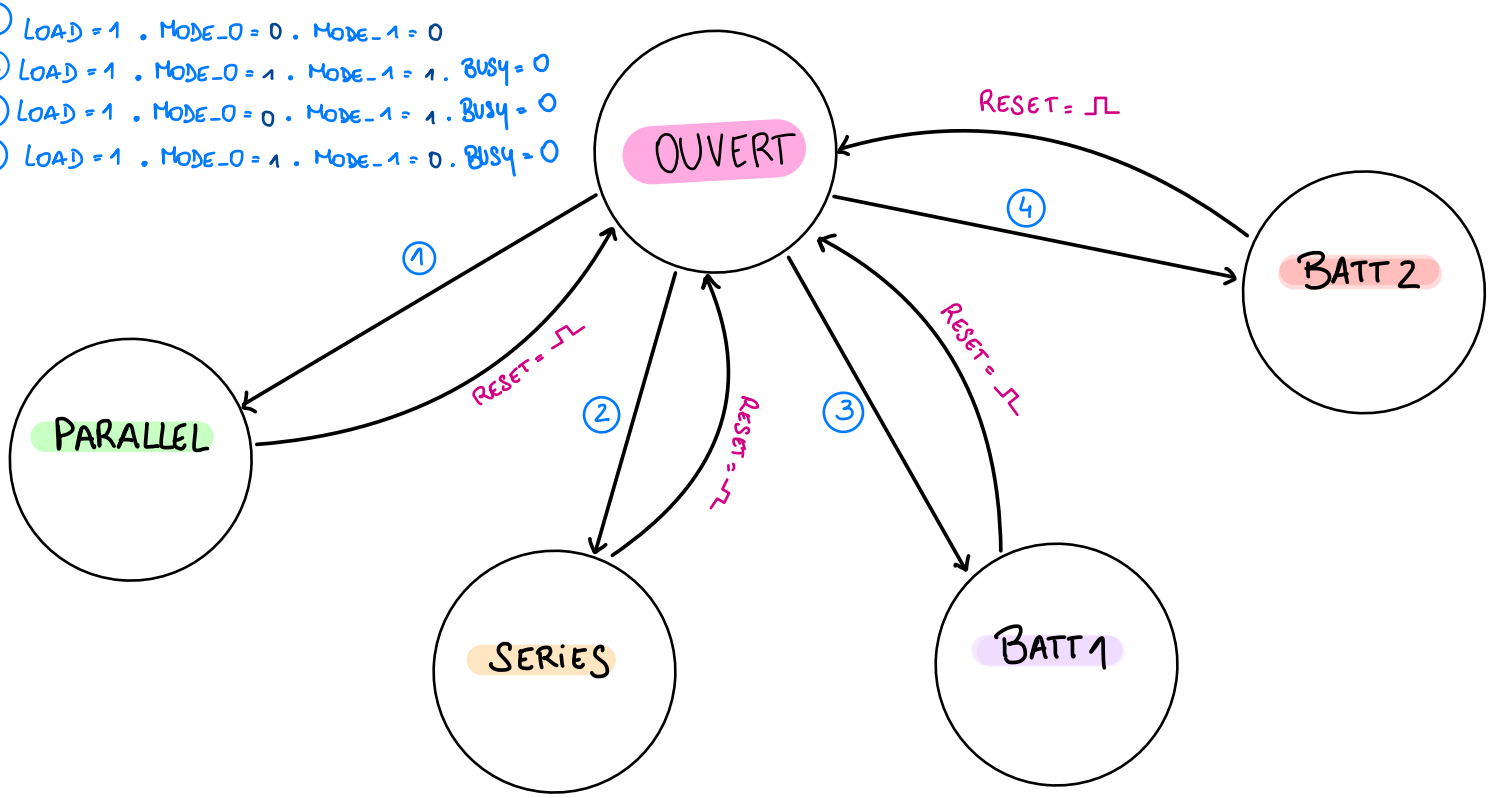
1) CPLD Inputs/Outputs



2) Switches schema



① LOAD = 1 . MODE_0 = 0 . MODE_1 = 0
② LOAD = 1 . MODE_0 = 1 . MODE_1 = 1 . BUSY = 0
③ LOAD = 1 . MODE_0 = 0 . MODE_1 = 1 . BUSY = 0
④ LOAD = 1 . MODE_0 = 1 . MODE_1 = 0 . BUSY = 0



OPEN: open all switches

ACK = 0
K_1 = 0
delay 1 ms
K_5 = 0
delay 1 ms
K_3 = 0
delay 1 ms
K_2 = 0
K_4 = 0
ACK = 1

PARALLEL: closing of some switches in order to put the two batteries in parallel

ACK = 0
K_2 = 1
K_4 = 1
delay 1 ms
K_1 = 1
ACK = 1

SERIES : closing of some switches in order to put the two batteries in series

ACK = 0
K_3 = 0
delay 1 ms
K_1 = 0
delay 1 ms
K_5 = 0
ACK = 1

BATT1 : closing of some switches in order to connect only the battery 1

ACK = 0
K_2 = 1
delay 1 ms
K_1 = 1
ACK = 1

BATT2 : closing of some switches in order to connect only the battery 2

ACK = 0
K_4 = 1
delay 1 ms
K_1 = 1
ACK = 1