 University of the Philippines

 Microelectronics and Microprocessors Laboratory

Lab Module 01 – Answer Sheet

Name: Estallo, Emmanuel Jesus

Student #: 2018-02355

Class: SATURDAY AM

SCORE: XX/40

Instructions:

This is answer sheet is a format only. You may answer using any word processor (i.e. Microsoft Word, Libre Office, Latek, Google docs … etc.) but you need to submit either a pdf or docx file so we can comment on it. Make sure to put your name, student number, and indicate what lab class you are in. This is given in the format above. Name your file “coe197\_class\_lastname\_studentnumber”. For the class write “satam” or “satpm” if you’re in the morning or afternoon class, respectively. For example: “coe197\_satam\_antonio\_201101474”.

When you make your document please maintain the order of the main sections (PART I, PART II, PART III, and PART IV) and stick to the numbering provided in this answer sheet. You may use this word document if you like.

Answer with clear and concise solutions. Indicate your final answer (box it, bold it, change its color but please do not use red font color). For problems that require explanations, elaborate your thoughts. Any unclear answers will be marked wrong. There will be partial points.

**Have fun and learn by heart!**

Part I: Review

Let’s recall a few concepts from the lecture. Answer the following questions below.

1. List 3 differences between long-channel and short-channel devices. Excluding the length of the transistor.

|  |  |
| --- | --- |
| Short – channel | Long – channel |
|  |  |
|  |  |
|  |  |

1. What’s the equation for the saturation current for both long-channel and short-channel devices?
2. What’s a suitable circuit model of a MOSFET acting as a switch?
3. What’s an inverter? Draw the schematic of a CMOS inverter.

Part II: Training

## Question Q2.1:

Can you tell where VDS,SAT is?

## Question Q2.2:

1. Does the PMOS transistor switch on with increasing or decreasing VSG?
2. With the given figures, does the current move from source to drain (SD) or drain to source (DS)? (Hint: Recall how LTspice defines current direction from Lab01. LTspice sets the + terminal to be at the drain and the – terminal to be at the source. Therefore?).
3. Use the “eye-ball” method to estimate VTHP. What is VTHP?

## Question Q2.3:

What is the effective RNMOS? (Hint that leads to the answer: you know that the propagation delay is at 1.75 ns. You also know that the load capacitance is 1pF. You also know the simple equation to compute the propagation delay.)

## Question Q2.4:

Change the transistor width to 250 nm, then get the effective RNMOS. Do it again for a width of 1000 nm. How would you describe the relation of the width size and the effective resistance RNMOS?

## Question Q2.5:

What is the effective CIN,NMOS? (Hint that leads to the answer: you know that the propagation delay is at 4.63 ps. You also know that the resistance is 5kΩ. You also know the simple equation to compute the propagation delay.)

## Question Q2.6:

Change the transistor width to 250 nm, then get the effective CIN,NMOS. Do it again for a width of 1000 nm. How would you describe the relation of the width size and the effective capacitance CIN,NMOS?

## Question Q2.7:

Match the points!

|  |  |
| --- | --- |
| A | 5 |
| B |  |
| C |  |
| D |  |
| E |  |

## Question Q2.8:

Determine the effective RPMOS and RNMOS from the tPHL and tPLH results. (Hint: look at our circuit, we used a 1pF capacitor)

Part III: Exercise

Let’s go a bit further with these exercises. We will be re-using most of the circuits we made earlier. Answer and solve the following problems.

## A. Short-Channel vs. Long-Channel

For comparison, Figure 3 shows a side-by-side comparison between the short-channel and long-channel transistors.

Questions:

1. Originally, the short-channel NMOS has a VTHN,short-channel of roughly 0.3V (the real VTHN,short-channel = 0.28 V) and it was difficult to extract due to the linear vs. saturation separation not being clear. As for the long-channel NMOS, what is VTHN,long-channel?
2. Compare the current values for both. Why do you think the long-channel has less current?
3. Compare the slope of the saturation region of the short-channel and long-channel currents. What’s so different between the two? Can you name something that causes this? (You may need to research a bit).
4. With the new setup, compare the currents between the short-channel and long-channel MOSFETS. Try to elaborate why this happens and compare it to your results and answers from the original setup (i.e. VGS, VDS = 1V).

## B. CMOS Tug-of-War

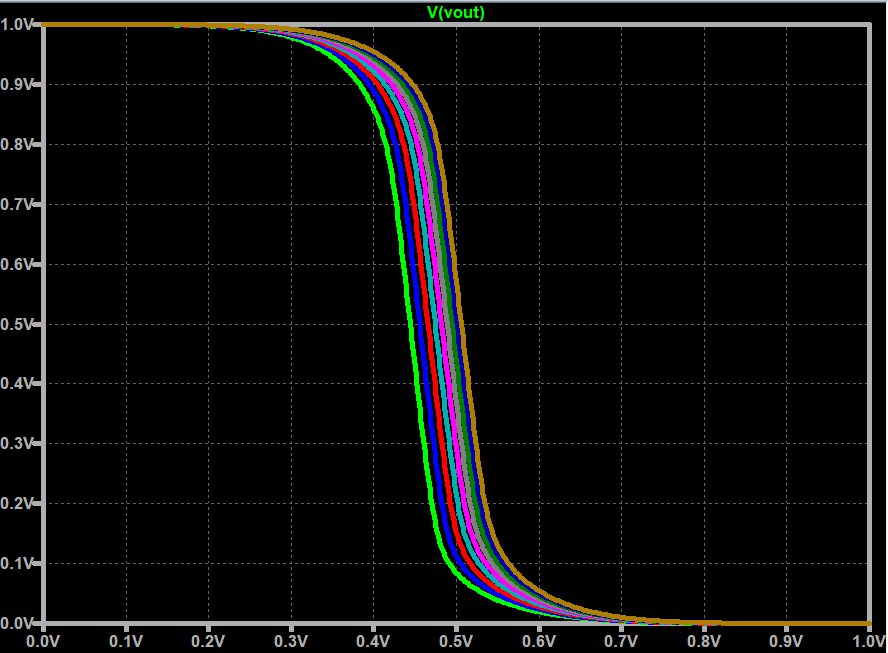


Figure 5 Parametric analysis of the VTC curve for varying PMOS widths

Questions:

1. What can you observe with the increasing widths of the PMOS? How does the VTC move with increasing PMOS widths?
2. Can you interpret what happens when the widths of the PMOS increase? Answer in terms of, what happens to the PMOS and NMOS currents.
3. What do you think is the best multiplier for the PMOS width such that VOUT is close to 0.5V when Vin = 0.5V? With you answer, what’s the best PMOS width to NMOS width ratio?
4. Using the width, you selected in #4, simulate Figure 2.24. Extract the new tPHL and tPLH and compare it to the original results. Did it improve? Make sure to record your tPHL and tPLH readings.

Part IV: Supplementary Notes

## Other inverter configurations

1. Inverter circuit 1

2. Inverter circuit 2

3. Inverter circuit 3