EEE192 Final Presentation

EMG-Based Design Project

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Contents

Introduction

Introduction

For the final presentation, we have the following goals:

- Runthrough of the entire design project
- Briefly discuss the function of each unit
- Discuss the methodology for each unit
- Discuss the results, conclusions, limitations

Design Project

EMG-based system

The task is to design, implement, present, and document an open-loop EMG-based system as shown in the figure below:

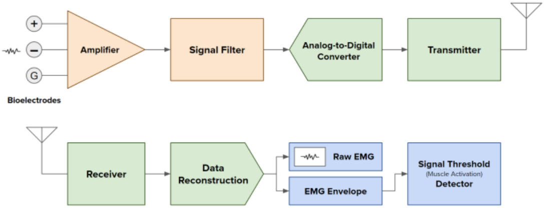


Figure: EMG-Based System Block Diagram

The system consists of three main units: the Analog Front-End unit (orange), the Transceiver unit (green), and the Signal Processing unit (blue). Note: The block diagram shown has been modified in the actual implementation of the system (with the use of simulation softwares).

EMG-based system

- For a successful implementation, the constructed EMG-based system should meet the desired specifications stated by the instructors.
- The implementation also includes the outputs and the integration of the main units as follows:
    1. The outputs of the Analog Front-end unit using the test data sets given by the instructors as input.
    2. The output of the Analog-to-Digital Converter (ADC) of the Transceiver unit
    3. The output of the BFSK Modulator and Demodulator of the Transceiver unit using a square wave as input.
    4. The data reconstruction and thresholding of the Signal Processing unit using the test data sets given by the instructors as input.
    5. The data reconstruction and thresholding of the Signal Processing Unit using the outputs of the Analog Front-End unit as input.

Analog Front-End

Analog Front-End

- The analog front-end unit's main goal is to produce a usable signal, that can be post-processed in the later stages, from the raw EMG data.
- A usable signal means:
  - A signal free of noise and distortion (i.e. Good Signal-to-Noise Ratio (SNR))
  - A signal with a reliable signal strength

Analog Front-End

- To achieve this goal, the analog front-end unit is thus composed of:
  - Intrumentation Amplifier
    - For common-mode rejection
  - Signal Filter
    - To achieve better SNR
    - Removes movement artifacts, ambient noise (i.e. powerline interference and electromagnetic radiation.
  - Second Amplifier
    - To achieve a desirable signal level
    - In this case, desirable signal level means a $5\mathrm{V}_{\mathrm{pp}}$ output range

Instrumentation Amplifier

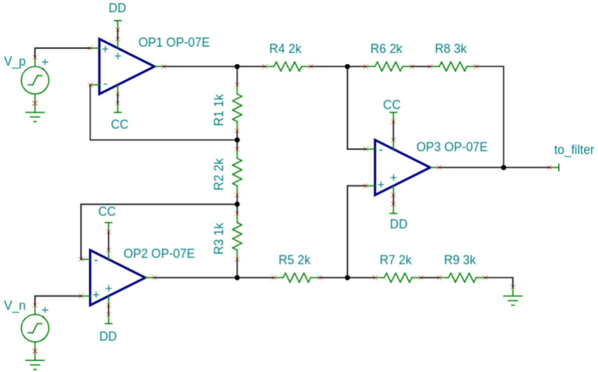


Figure: Instrumentation Amplifier Implementation

Signal Filter

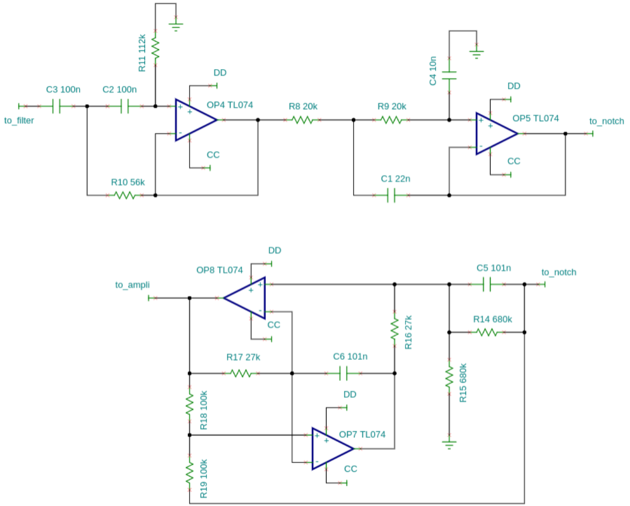


Figure: Band Pass Filter (above) and Notch Filter (below)

Second Amplifier Stage

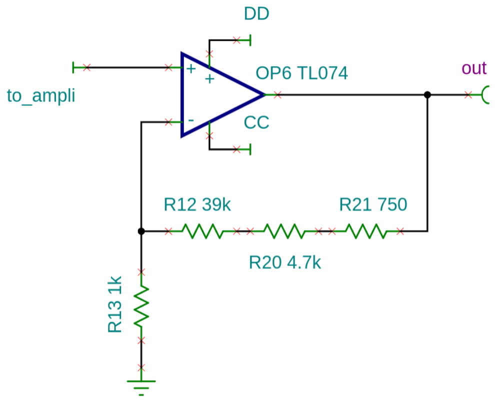


Figure: Second Amplifier Stage Implementation

Transceiver

Transceiver

- The Transceiver unit's collective task is to digitize the analog signal from the front-end unit and transmit that data to be received by the signal processing unit. It is composed of three main parts:
  1. Analog-to-Digital Converter
  2. BFSK Modulator with Antenna
  3. BFSK Demodulator

Analog-to-Digital Converter

- The analog-to-digital converter is used to digitize the analog EMG signal for further signal processing and analysis in the succeeding stages.
- The specific design specifications are:
    - ADC resolution of 10-bits
    - 16-bit data packet, with error detection using a parity bit P
    - A sampling frequency that satisfies the Nyquist Thorem.

Analog-to-Digital Converter

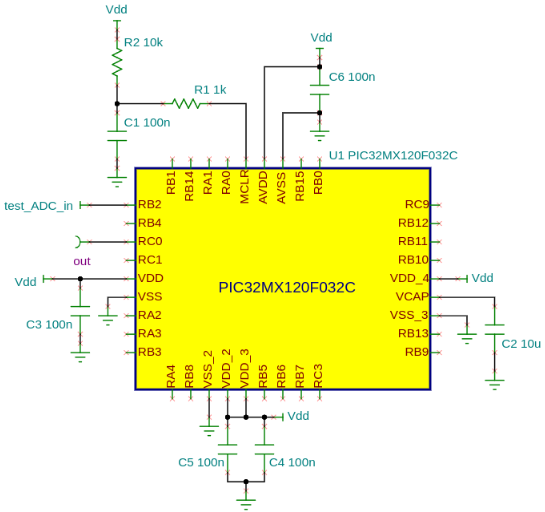
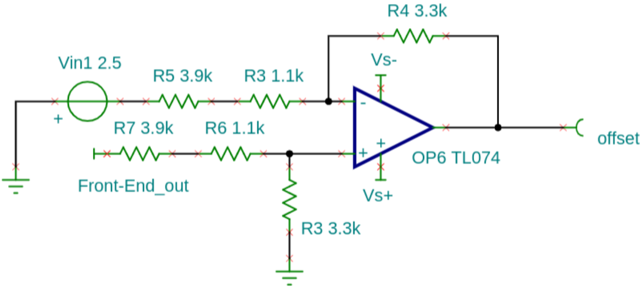


Figure: ADC Implementation

Analog-to-Digital Converter



$$\text{ADC\_in} = \frac{3.3k}{5k}(\text{Front-End\_out} + 2.5)$$

Figure: ADC bipolar-to-unipolar cirucit

Analog-to-Digital Converter Tests

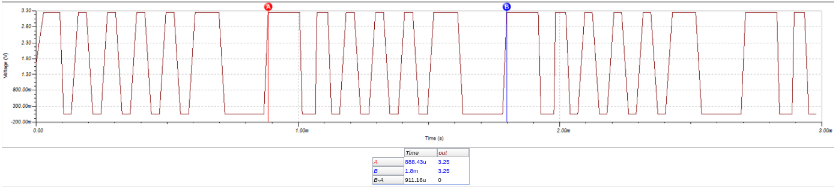


Figure: ADC output with a $1.1\mathrm{V}$ input

Figure: ADC output with a $500\mathrm{Hz}$ Square Wave

Analog-to-Digital Converter Tests

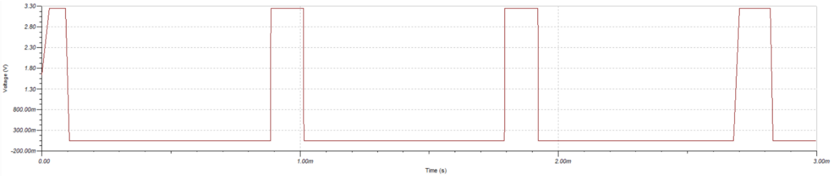


Figure: ADC output with a $0\mathrm{V}$ input

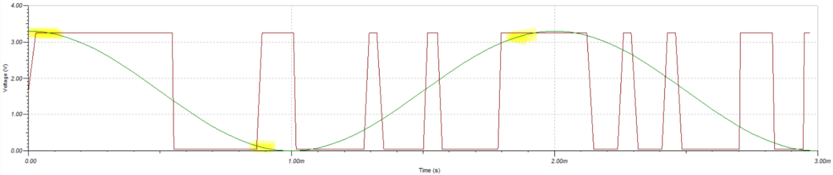


Figure: ADC output with a $500\mathrm{Hz}$ cosine Wave

BFSK Modulator with Antenna

- The Binary Frequency-Shift Keying (BFSK) Modulator shifts the frequency of the signal based on the ADC output for data transmission through the Power Antenna. The frequencies to be used will be specified as the f_{mark} and f_{space} frequencies which will correspond to the values Binary 1 and 0 respectively in demodulation.
- The values for the f_{mark} and f_{space} frequencies were computed as the ends of the bandwidth (BW) through the equation below:

$$BW = 2(f_d + f_b)$$

  where the f_d is the deviation from the center frequency f_c and f_b is the bit rate taken from the ADC.
- With the use of a modulation index h and the effective ADC bit rate of $18kHz$, the f_{mark} and f_{space} frequencies were calculated as $270kHz$ and $90kHz$ respectively with a total BW of $180kHz$.

BFSK Modulator with Antenna

- The BFSK Modulator was implemented using an XR-2206 Monolithic Function Generator whose pins were configured for the designed specifications:
  1. The f_{mark} and f_{space} frequencies of $270kHz$ and $90kHz$ respectively.
  2. The shifted frequencies in a sine wave output.
- The BFSK Modulator output was then connected to the Power Antenna to be amplified for the simulation of data transmission to the demodulator. Its schematic was based on the configuration given by the instructors. Its output is then connected as the input for the demodulator.

BFSK Modulator with Antenna

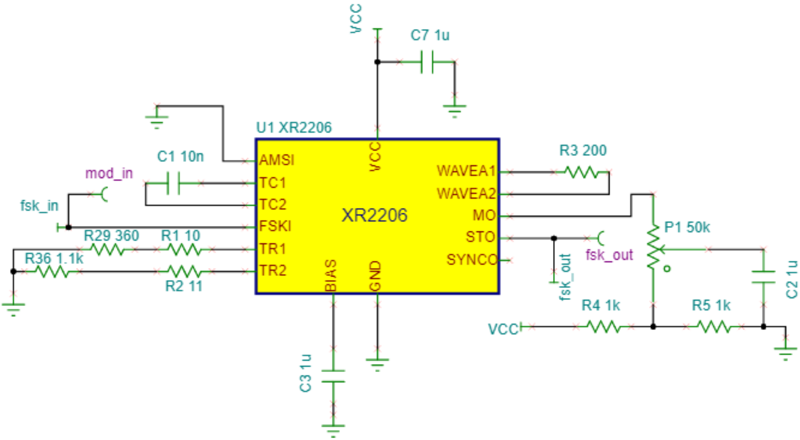
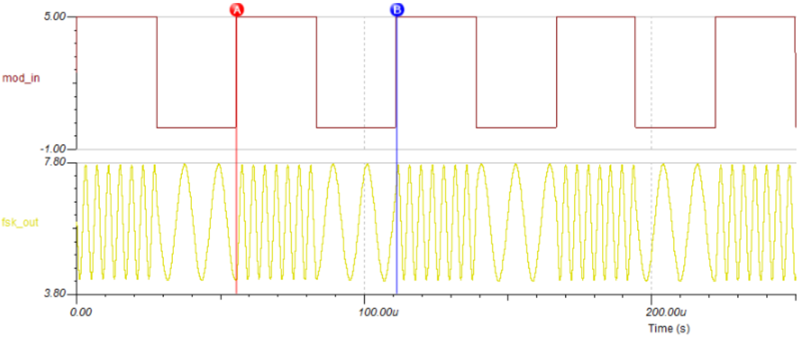


Figure: XR-2206 Monolithic Function Generator Configuration

BFSK Modulator with Antenna



	Time	mod_in	fsk_out
A	55.8u	5	4.28
B	111.6u	5	7.49
B-A	55.8u	0	3.22

Figure: Modulator Output

BFSK Modulator with Antenna

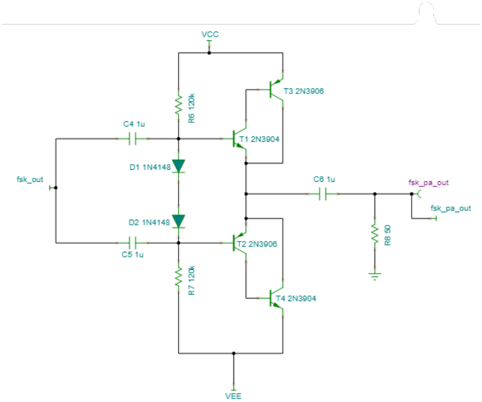


Figure: Power Amplifier and Antenna Configuration

BFSK Modulator with Antenna

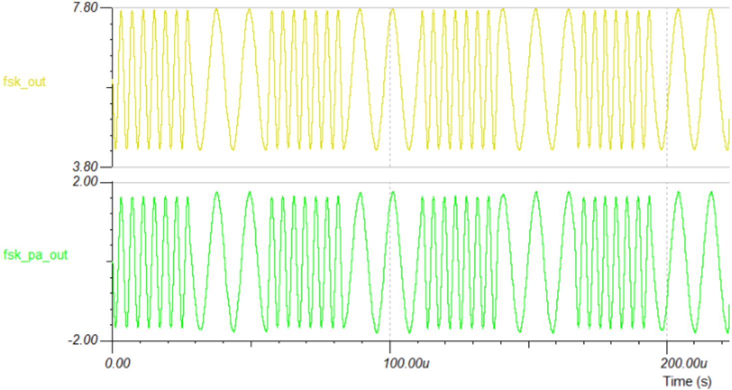


Figure: Antenna Output

BFSK Demodulator

- The BFSK Demodulator is used for the filtering of the shifted frequencies from the modulator. It is done by using bandpass filters and envelope detectors connected to a comparator to generate the desired output for signal processing.
- Two 4th order active bandpass filters were used with cutoff frequencies of f_{mark} and f_{space} respectively. This was achieved by cascading 2nd order lowpass and highpass filters using the Sallen-Key topology.

BFSK Demodulator

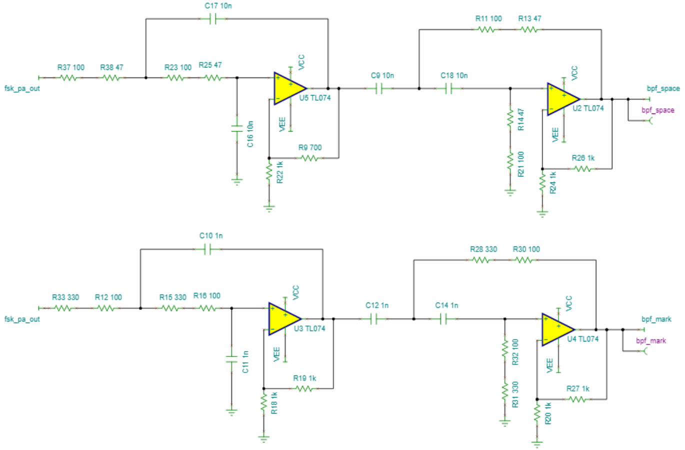
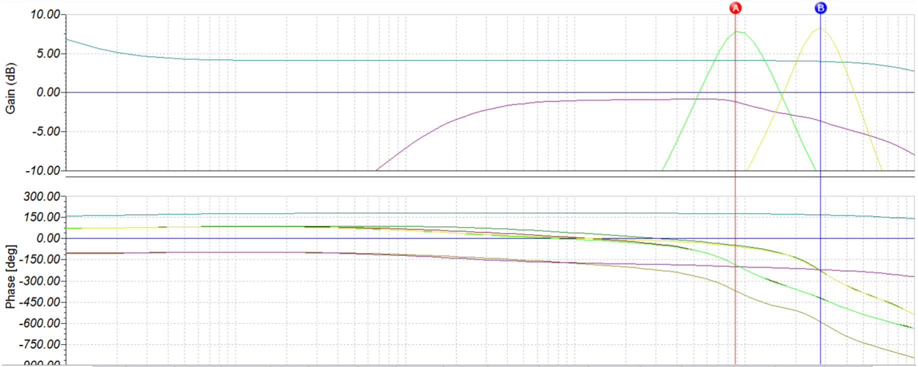


Figure: 4th Order Bandpass Filters

BFSK Demodulator



	Frequency	env_space (dB)	env_mark (dB)	demod_out (dB)	mod_in (dB)	fsk_pa_out (dB)	fsk_out (dB)	bpf_space (dB)	bpf_mark (dB)	env_space (deg)	env_mark (deg)	demod_out (deg)	mod_in (deg)	fsk_pa_out (deg)	fsk_out (deg)	bpf_space (deg)	bpf_mark (deg)
A	88.78k	-39.99	-62.09	-40.8	0	-1.21	4.11	7.81	-12.5	-185.9	-47.94	-368.8	0	-198.8	176.3	-187.5	-54.33
B	282.57k	-59.09	-41.21	-41.5	0	-3.68	4.01	-11.3	8.28	-423.8	-230.5	-592.4	0	-219.2	168.3	-424.4	-232.5
B-A	193.8k	-19.1	20.88	-700m	0	-2.46	-101m	-19.11	20.78	-237.9	-182.56	-223.6	0	-20.4	-8	-236.9	-178.17

Figure: Bandpass Filters AC Analysis

BFSK Demodulator

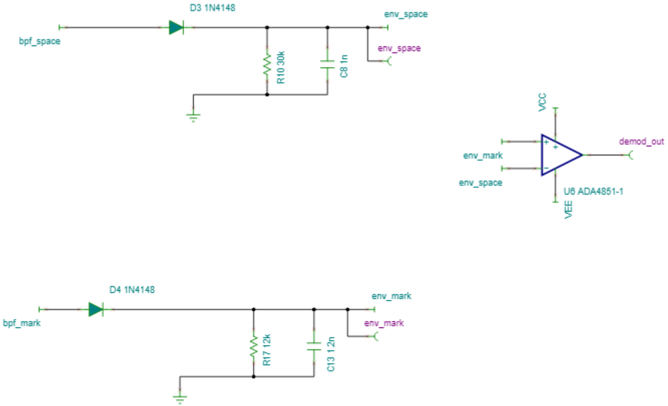


Figure: Envelope Detectors and Comparators

BFSK Demodulator

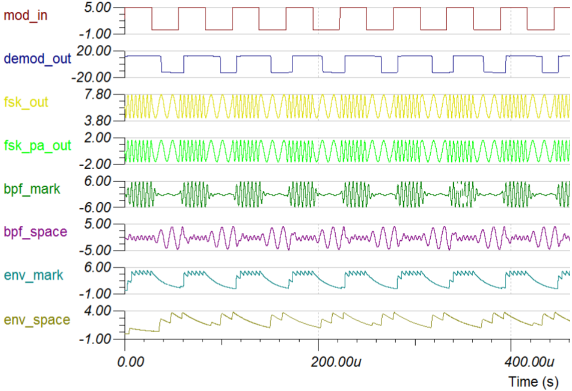


Figure: Demodulator Output

Signal Processing

Data Reconstruction

The data reconstruction unit is essentially a digital to analog converter (DAC).

$$input = 1 - ADC\ Data - P - 0001$$

where P is the parity bit, and the ADC data is made up of 10 bits. To reconstruct the data, the steps are as follows:

1. Iterate over the entire binary data and group it into 16 - bit packets.
2. Check the parity of the packet by solving the modulo 2 of the sum of each packet.
3. If the packet is of odd parity, the corresponding analog data is 0.
4. If the packet has an even parity, get the decimal equivalent of the ADC data by

$$y = \frac{1}{2^{N-1}} \begin{bmatrix} x_{N-1} & x_{N-2} & \dots & x_0 \end{bmatrix} \begin{bmatrix} 2^{N-1} \\ 2^{N-2} \\ \vdots \\ 1 \end{bmatrix}$$

Data Reconstruction

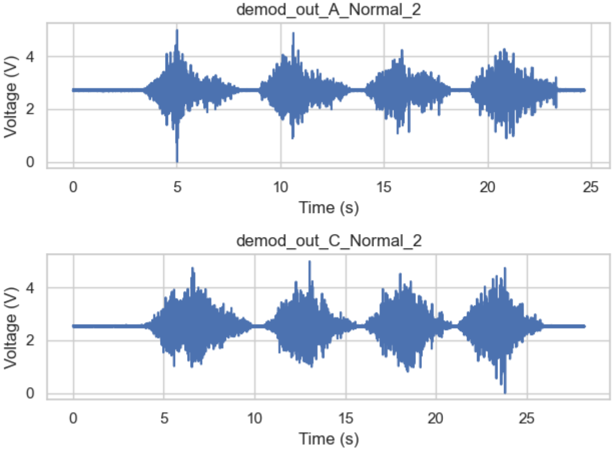


Figure: Reconstructed Signal, A Normal 2, C Normal 2

Data Reconstruction

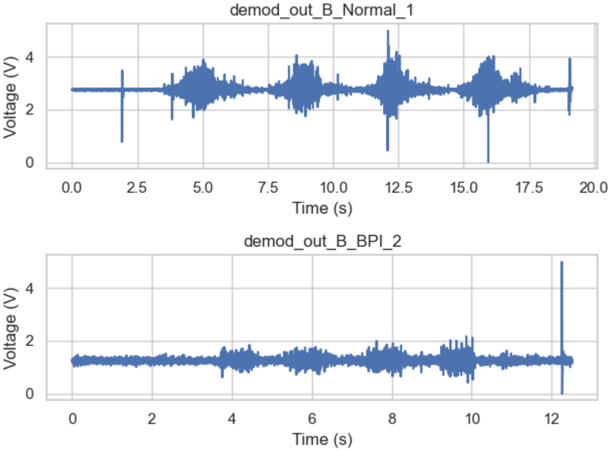


Figure: Reconstructed Signal, B Normal 1, B BPI 2

Signal Analysis

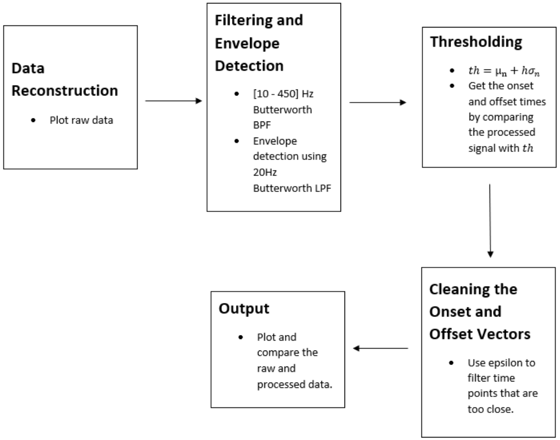


Figure: Signal Analysis Pseudocode

Signal Analysis

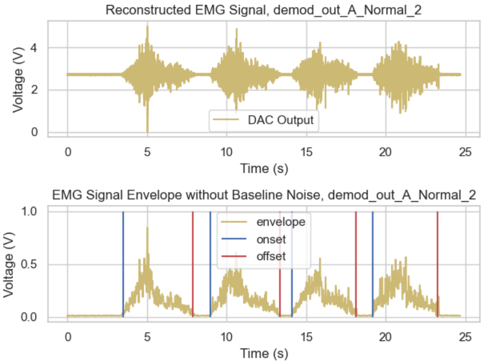


Figure: Processed Sample EMG, A Normal 2

Results, Conclusion, Limitations

Results

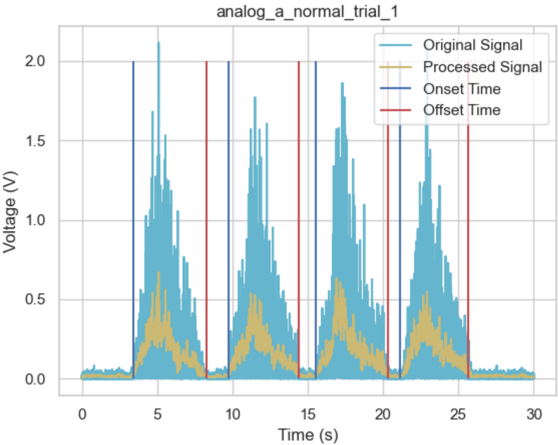


Figure: Processed Analog Front-End Output, A Normal 1

Results

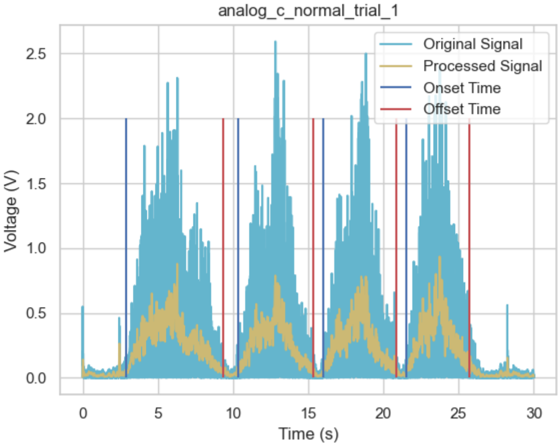


Figure: Processed Analog Front-End Output, C Normal 1

Results

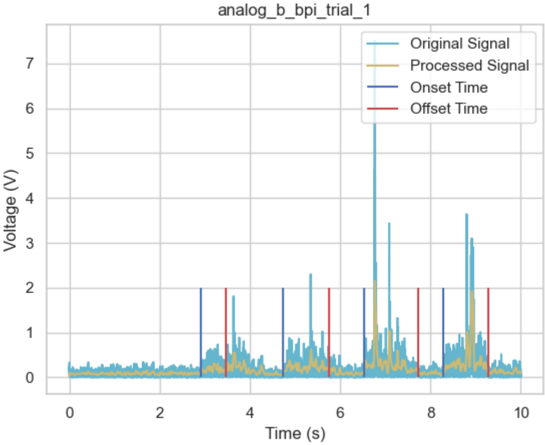


Figure: Processed Analog Front-End Output, B BPI 1

Conclusion

- The specifications for each unit of the EMG-based system were met as seen from the results.
- Although the specifications were met, some errors were encountered. The design of each unit can still be improved with better resources.
- An EMG-based system can be implemented using this project as a guide.

Limitations

- For the ADC, the software does not allow a longer simulation time
- The envelope detector can be designed to provide a better detection of the specific frequencies for a better demodulator output.
- For the signals labeled with "BPI", more sophisticated algorithms to detect the threshold are required

References

- R. P. De Leon, "Introduction to EMG-Based Systems Lecture 1," in EEE 192.
- M. H. Khan et al., "Design of low cost and portable EMG circuitry for use in active prosthesis applications," 2012 International Conference of Robotics and Artificial Intelligence, 2012, pp. 204-207, doi: 10.1109/ICRAI.2012.6413389.

Thank you!