Activity 8: Noise Analysis

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I. Transistor Noise

A. NMOS Noise

For the NMOS with VDS = VGS = 900mV, $I_D = 439\mu A$. Additionally, $g_m = 2.44mS$ and $v^* = 440mV$ as seen in the image below.

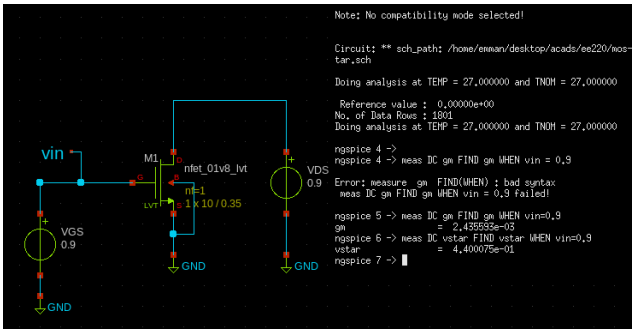

Fig. 1. g_m and v^*

The values are obtained by using the MEAS command. Note that the TT corner is used.

1) Simulations: Flicker noise dominates the range $f < 5MHz$ whereas thermal noise dominates the region where $f > 5MHz$. With this, the flicker noise corner is at around $f = 5MHz$.

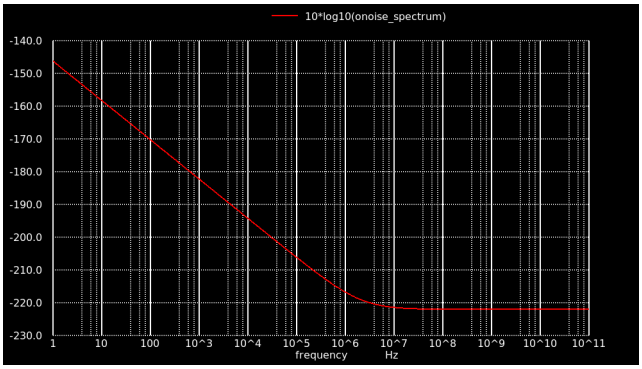

Fig. 2. Output Noise PSD

2) Estimating γ: Recall that in the absence of flicker noise, and assuming $\alpha = 1$

$$\overline{i_{dn}^2} = 4kT\gamma g_m \Delta f$$

The total integrated noise power is equal to

$$\begin{aligned} P_{o,noise} &= \int_{f1}^{f2} \overline{i_{dn}^2}\, df \\ &= \int_{f1}^{f2} 4kT\gamma g_m \, df \\ &= 4kT\gamma g_m \cdot (f_2 - f_1) \end{aligned}$$

This means that if the integrated drain current noise power is obtained at the region where thermal noise is dominant, it is possible to directly compute for γ. To estimate the value of γ, the total output noise power with 10-GHz bandwidth from 90-GHz to 100-GHz is chosen.

$$\gamma = \frac{P_{o,noise}}{4kTg_m(f_2 - f_1)}$$

In this case,

$$\gamma \approx \frac{5.57E-13}{4kT \cdot 2.44E-3 \cdot 10E+9} = 1.375$$

3) Estimating K_f/C_{ox}: We know that the total drain current noise is given by:

$$\overline{i_{dn}^2} = \frac{K_f I_D}{C_{ox} L^2} \cdot \frac{\Delta f}{f} + 4kT\gamma g_m \Delta f$$

$$\begin{aligned} P_{o,noise} &= \int_{f1}^{f2} \overline{i_{dn}^2}\, df \\ &= \frac{K_f I_D}{C_{ox} L^2} ln\left(\frac{f_2}{f_1}\right) + 4kT\gamma g_m \cdot (f_2 - f_1) \end{aligned}$$

In the simulation results, $P_{o,noise} = 6.336E-12$ By substituting the known values with $f_2 - f_1 = 100G$,

$$\frac{K_f}{C_{ox}} = 8.439E-24$$

Upon increasing the length, the integrated drain current noise power is reduced. The flicker noise corner is at almost the same frequency. The reduction might be explained by the reduction in g_m and I_D. Additionally, the flicker noise is inversely proportional to the square of the length.

B. PMOS Noise

For the PMOS device, $g_m = 967.77\mu S$, and $v^* = 596.30mV$. Additionally, $I_D = 288.53\mu A$ as obtained by the MEAS directive in NGSPICE.

1) Simulations: The PSD plot is shown below. Looking at the plot and extrapolating, it is seen that the flicker noise corner is also at around $5MHz$.

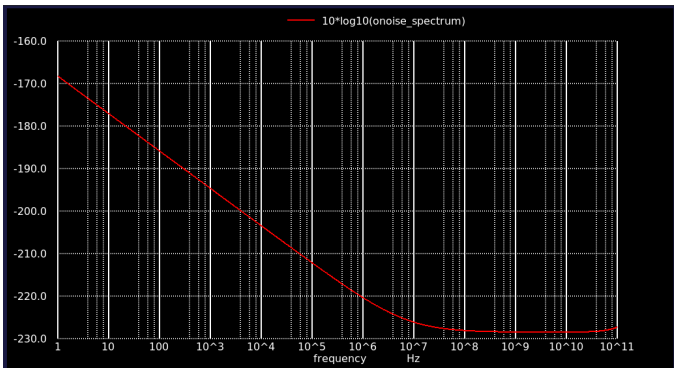

Fig. 3. Output Noise PSD

2) Estimating γ: Similar to the NMOS simulation, it is possible to estimate γ by only considering the output noise power at the region where thermal noise dominates. Ideally, the selected frequency range must be much higher than the flicker noise corner.

Using the $90 - 100GHz$ frequency range,

$$\gamma = \frac{P_{o,noise}}{4kTg_m(f_2 - f_1)} = 0.992 \approx 1$$

3) Estimating K_f/C_{ox}: Similar to the NMOS,

$$\begin{aligned} P_{o,noise} &= \int_{f1}^{f2} \overline{i_{dn}^2}\, df \\ &= \frac{K_f I_D}{C_{ox} L^2} ln\left(\frac{f_2}{f_1}\right) + 4kT\gamma g_m \cdot (f_2 - f_1) \end{aligned}$$

Since thermal noise is constant over all frequencies (at least in this case), it is possible to estimate the 1/f noise constant by just subtracting the thermal noise component from the total integrated noise power given by the simulation.

$$\frac{K_f}{C_{ox}} = 6.704E - 25$$

The PMOS 1/f noise constant is less than the NMOS. Flicker noise comes from carriers being trapped in the surface. The carriers in PMOS are holes and the carriers in NMOS are electronics. Electrons have higher tendency to be trapped than holes.

Similarly, the total output noise decreases with increasing length. This is attributed to the reduced gm and ID. Also, parasitic capacitances are increased.