Activity 8: Noise Analysis

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I. Transistor Noise

A. NMOS Noise

For the NMOS with VDS = VGS = 900mV, $I_D = 439\mu A$. Additionally, $g_m = 2.44mS$ and $v^* = 440mV$ as seen in the image below.

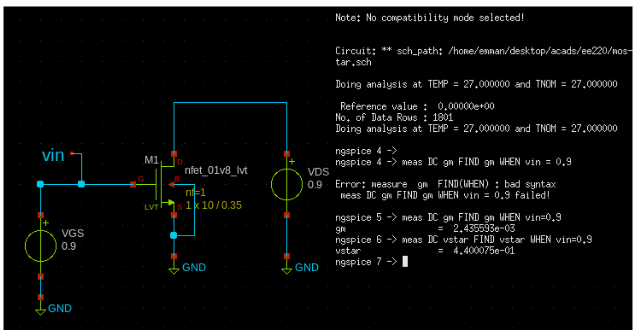

Fig. 1. g_m and v^*

The values are obtained by using the MEAS command. Note that the TT corner is used.

1) Simulations: Flicker noise dominates the range $f < 500MHz$ whereas thermal noise dominates the region where $f > 500MHz$. With this, the flicker noise corner is at around $f = 500MHz$.

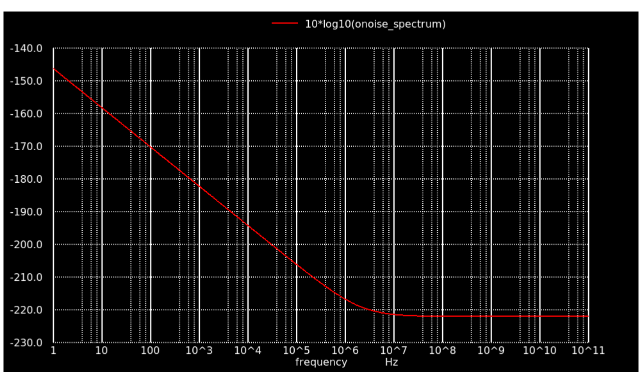

Fig. 2. Output Noise PSD

2) Estimating γ: Recall that in the absence of flicker noise, and assuming $\alpha = 1$

$$\overline{i_{od}^2} = 4kT\gamma g_m$$

The total integrated noise power is equal to

$$\begin{aligned} P_{i,noise} &= \int_{f1}^{f2} \overline{i_{od}^2}\, df \\ &= \int_{f1}^{f2} 4kT\gamma g_m\, df \\ &= 4kT\gamma g_m \cdot (f_2 - f_1) \end{aligned}$$

This means that if the integrated output noise power is obtained at the region where thermal noise is dominant, it is possible to directly compute for γ. To estimate, the total output noise power with 1-GHz bandwidth centered at around 90-GHz will be chosen. Since

B. PMOS Noise