Design of a Simple CS Amplifier

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I. CS Amplifier

The desired specs are as follows:

- $|A_v| > 40$ at $V_{DS} = V_{DD}/2 = 0.9V$
- Output swing: $400mV$
- Unity-gain frequency: $f_u = 100MHz$, $C_L = 5pF$
- $V^* = 200mV$

A. Selecting I_D

The transconductance can be obtained from:

$$g_m = 2\pi f_u C_L$$

which results to

$$g_m = 3.14\ mS$$

The current can be obtained from:

$$V^* = 2 \cdot \left(\frac{g_m}{I_D}\right)^{-1}$$

a V^* of 200 mV corresponds to a g_m/I_D of 10.

Thus,

$$I_D = 314\ \mu A$$

B. Choosing the length

To find the appropriate length, V_{GS} is swept from $0V$ to $1.8V$ and checked if the intrinsic gain at V^* is > 40.

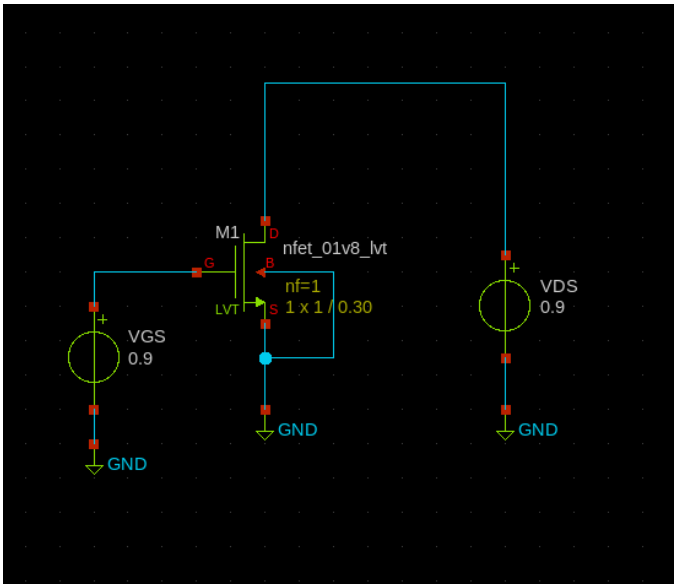

Fig. 1. Schematic diagram

At the minimum length, the intrinsic gain is lower than what is desired. $L = 0.30\mu m$ is selected since it satisfies the specifications. $L = 0.25\mu m$ also meets the specifications. However, for a greater swing, the larger length is selected.

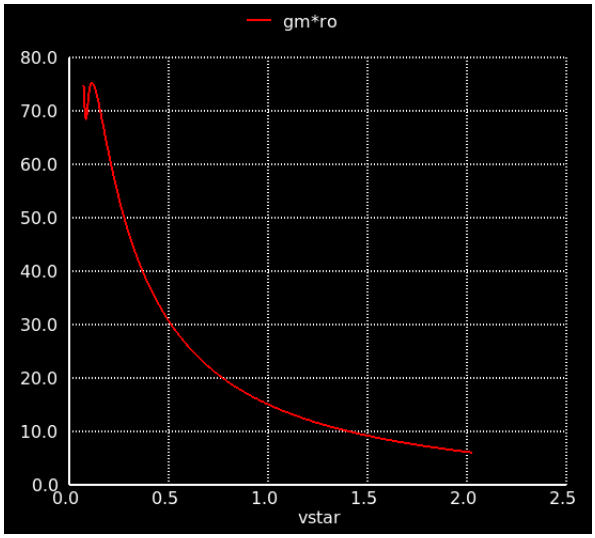

Fig. 2. Intrinsic gain

The V^* vs I_D plot for a transistor with $W = 1\mu m$, $L = 0.30\mu m$ is shown below.

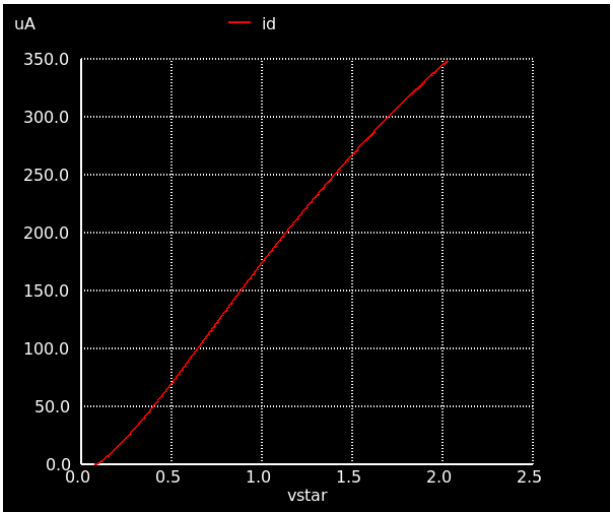

Fig. 3. I_D vs V^*, $W = 1\mu m$

C. Scaling the width

A python script is used to calculate the scale factor k_W that meets the required I_D. The width is scaled using k_W. Multiplying the width by k_W scales I_D by approximately the same factor. For this activity, $k_W = 21$. To check, a MEAS directive is used. The required current is $I_D = 314\mu A$. Due to some estimates, $I_D = 345\mu A$ is obtained.

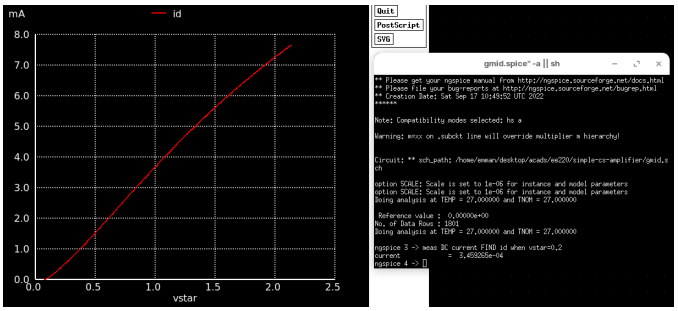

Fig. 4. I_D vs V^*, $W = 21\mu m$

D. Output and input swing

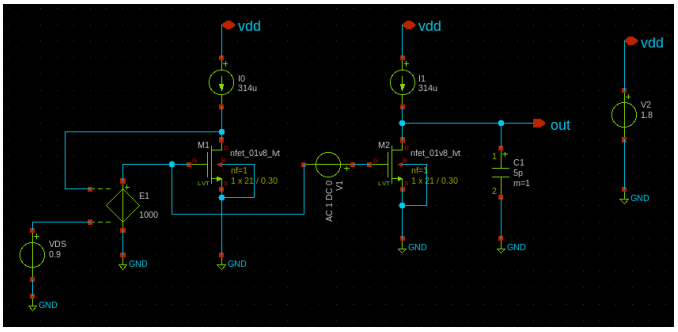

Fig. 5. Schematic

To get the input and output swing, the schematic in Fig. 5 is used. Since V_{GS} is a function of V_{DS}, a_o vs V_{DS} can be plotted to get the maximum output swing and a_o vs V_{GS} to get the corresponding input swing.

1) Output Swing: at $V_{DS} \approx 0.52$, $a_o \geq 40$.

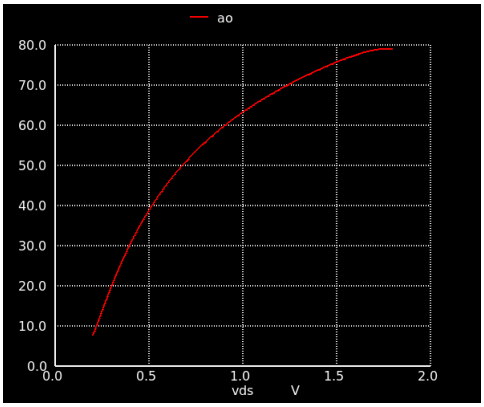

Fig. 6. a_o vs V_{DS}

2) Input Swing: at $V_{GS} \approx 0.71$, $a_o \geq 40$.

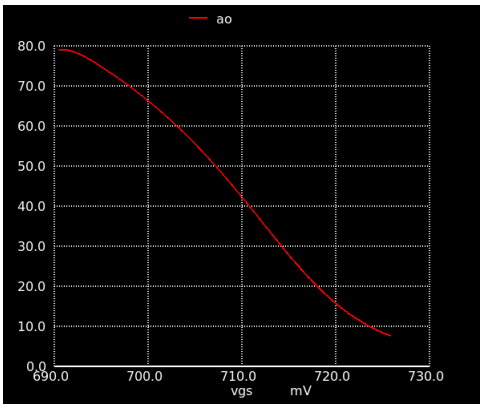

Fig. 7. a_o vs V_{GS}

Thus, the maximum symmetric output voltage is $0.52 \leq V_{DS} \leq 1.48$ for a total swing of $0.96V$. The corresponding input is $0.6946 \leq V_{GS} \leq 0.7106$ with a $16mV$ swing.

3) Input vs output: Shown in Fig. 8 is a sweep of $V1$ from $-8mV$ to $8mV$.

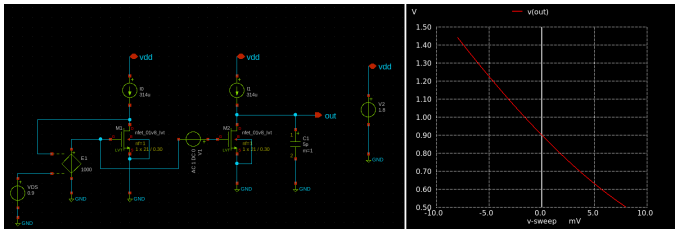

Fig. 8. a_o vs V_{GS}

E. AC analysis

Using Fig. 5, an AC sweep from $1Hz$ to $1GHz$ is performed. The resulting magnitude response plot is shown in Fig. 9. Using a MEAS directive, $f_u = 104MHz$, which is close to the desired f_u. At low frequencies, the gain is $\approx 35dB$ which is $\approx 60\ V/V$

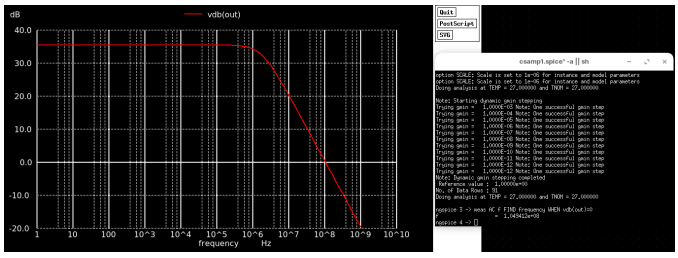

Fig. 9. Magnitude response

F. Discussions

These are my expected results. Since some values are estimated, there are slight deviations with the desired specifications.

II. CS Amplifier with High f_t

To get a high f_t, a small L and high power is required. Decreasing L increases f_t if I_D is kept constant. However, since there are no constraints on area and how high I_D could be, the limit would be related to the maximum W that can be used on the PDK.

A. Selecting the width

There is a trade-off between power and frequency. The higher the power that is used, the higher the frequency the circuit could get. Since V_{DD} is fixed, the current consumption can be increased to bring more power to the circuit — this is done by increasing the width.

For this PDK, the largest width that can be used is $W = 99.9\mu m$. This value is used to get the maximum I_D that meets the specifications. All simulations for this part will use this value.

B. Choosing the length and V^*

Ideally to get the highest f_t, the minimum length should be selected. However, the minimum length does not have sufficient intrinsic gain. Since the load is an ideal current source, the gain is only limited by the lower bound $\approx 700mV$. $V_{DS} = 0.7V$ is used for this characterization part.

1) a_o vs V^*: For $0.20\mu m \leq L \leq 0.25\mu m$, the a_o vs V^* plot is shown below.

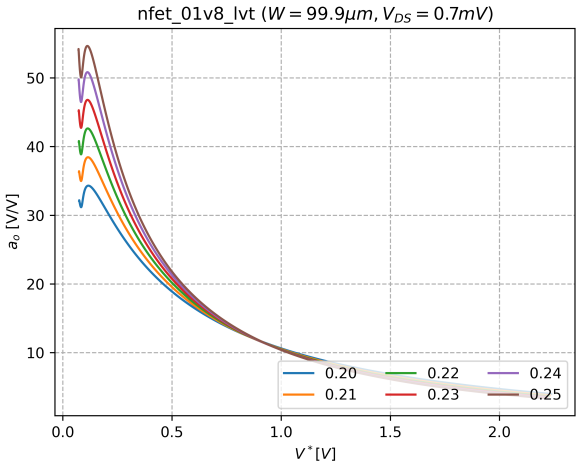

Fig. 10. Intrinsic gain

Since the desired gain is $a_o > 40$, only lengths $\geq 0.22\mu m$ can be used.

2) f_t vs V^*: To trim down the possible options, an f_t vs V^* plot is used.

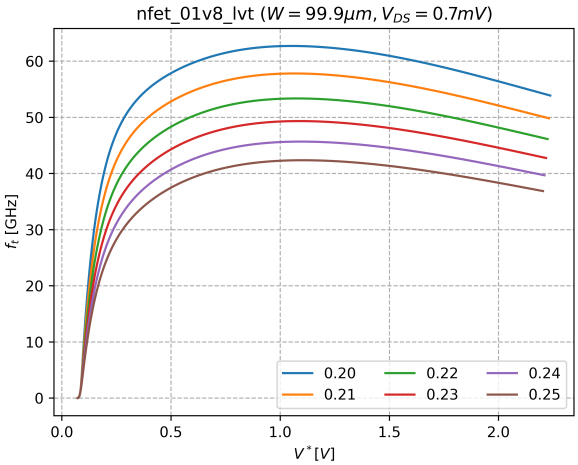

Fig. 11. Transition frequency

Considering the two plots, $V^* = 0.19V$ and $L = 0.23\mu m$ are chosen since they lead to the highest f_t. The gain and swing at these values are also within the required specifications. The obtained f_t is $28GHz$.

C. Obtaining g_m and f_u

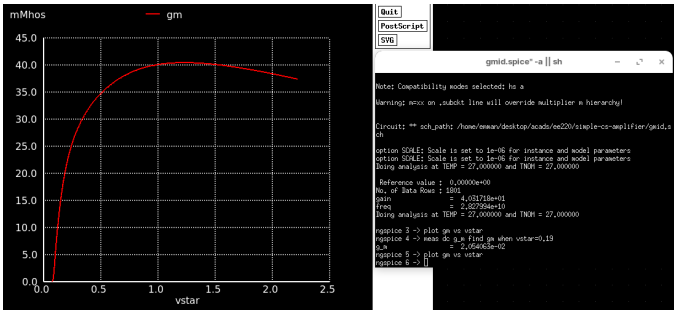

Fig. 12. g_m vs V^*

From Fig. 12, $g_m = 20.54mS$ at $V^* = 0.19V$. The target unity-gain frequency is:

$$f_u = \frac{g_m}{2\pi C_L} = 653.81MHz$$

with $I_D = 1.95mA$.

D. AC analysis

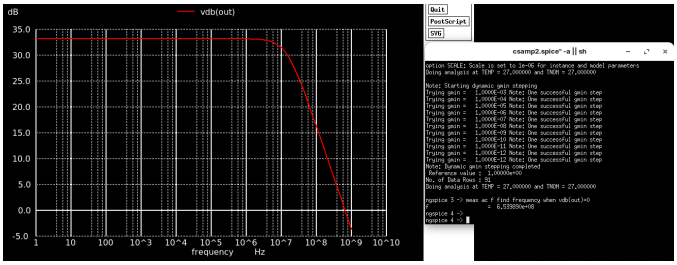

Fig. 13. Unity-gain frequency

Looking at Fig. 13, $f_u \approx 654MHz$. The desired f_u is met. At low frequencies, the gain is 33.19 dB which corresponds to 45.66 V/V.

E. Output and input swing

1) Output Swing: From the plot below, it is seen that $a_o = 40.32$ at $V_{DS} = 0.7$. At $V_{DS} = 1.1$, $a_o \approx 50$.

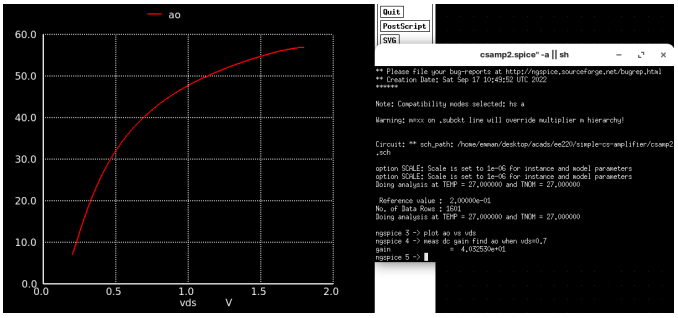

Fig. 14. a_o vs V_{DS}

2) Input Swing: Sweeping V_{DS} from $700mV$ to $1.1V$, the following a_o vs V_{GS} plot is obtained. The input V_{GS} that produces $700mV \leq V_{DS} \leq 1.1V$ ranges from $719mV$ to $727mV$. The maximum swing is $8mV$.

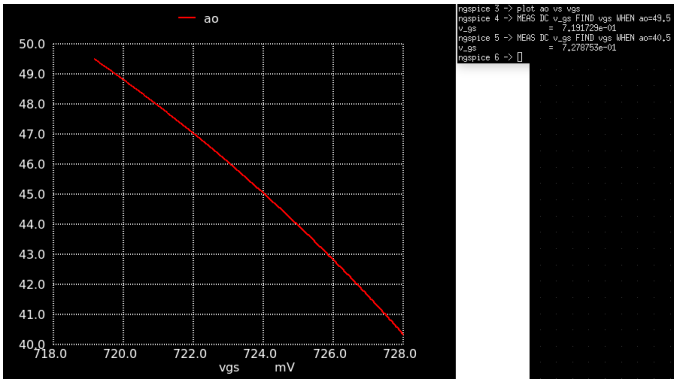

Fig. 15. a_o vs V_{GS}

3) Input vs output: v_{in} is swept from $-4mV$ to $4mV$ to get the corresponding v_{out}.

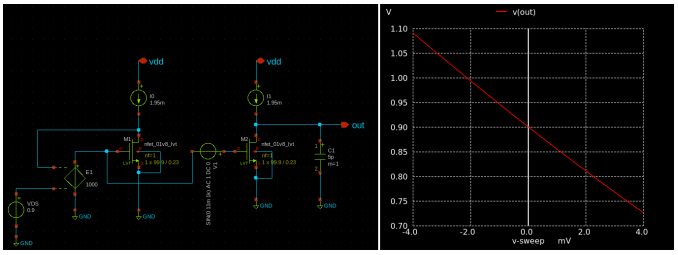

Fig. 16. v_{in} vs v_{out}

F. Discussions

First, the choice of V^* depends on both gain and desired f_t. If we increase V^*, we can get a higher f_t but the gain will decrease. To maximize f_t, the maximum V^* that satisfies both gain and swing should be chosen. This amplifier is designed to have an approximate output swing of $\pm 200mV$ with a DC level of $0.9V$ because of f_t constraints.

The first design has $I_D = 314\mu A$. For this design, $I_D = 1.95mA$. The I_D is more than 6 times higher. RF applications would benefit from a high f_u but this might not be usable at all because of very high current consumption.

III. CS Amplifier with Smallest Power Consumption

To minimize power consumption, the current should be decreased. This can be done by increasing the length.

A. Choosing the length

The maximum length that can be used for this PDK is $99.9\mu m$. The length is set to its maximum value to get the least possible current.

B. Selecting V^*

A small V^* corresponds to a more efficient circuit. V^* is chosen such that the transistor operates near the sub-threshold region. For this, we select $V^* = 100mV$.