University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 08 – Answer Sheet

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Class: SATURDAY AM
SCORE: XX/40

Instructions:

This is answer sheet is a format only. You may answer using any word processor (i.e. Microsoft Word, Libre Office, Latek, Google docs … etc.) but you need to submit either a pdf or docx file so we can comment on it. Make sure to put your name, student number, and indicate what lab class you are in. This is given in the format above. Name your file "coe197_class_lastname_studentnumber". For the class write "satam" or "satpm" if you're in the morning or afternoon class, respectively. For example: "coe197_satam_antonio_201101474".

When you make your document please maintain the order of the main sections (PART I, PART II, PART III, and PART IV) and stick to the numbering provided in this answer sheet. You may use this word document if you like.

Answer with clear and concise solutions. Indicate your final answer (box it, bold it, change its color but please do not use red font color). For problems that require explanations, elaborate your thoughts. Any unclear answers will be marked wrong. There will be partial points.

Have fun and learn by heart!

Part I: Review (3 pts)

1. What does a cascode current mirror do? (1 pt.)

- A cascode current mirror is just the same as a current mirror but uses a cascode to negate the effects of channel length modulation. Using a cascode structure also increases the output impedance without generating a large enough voltage drop.

2. What is a differential circuit? (1 pt.)

- A differential circuit is a circuit that has two inputs and generates an output voltage depending on the difference of the two inputs. Differential circuits are commonly used on stages that requires noise reduction.

3. Concisely, describe differential mode and commode mode. (1 pt.)

- The differential mode tells us how the output varies with respect to the difference of the input voltages. The common mode tells us how the output varies with respect to the average of the input voltages.

Part II: Training (29 pts)

Question Q2.1: (11 pts)

Let's see if you understood what really happens in a cascode. Answer with *increase(s)* or *decrease(s)* only. Following the same discussion in Figure 2.15.

1. As V_{OUT} decreases, V_{DS2} decreases. This decreases I_{DS2} or I_{OUT}.
2. As I_{OUT} decreases, V_{DS1} needs to decrease. Hence $V_{D1} = V_{S2}$ decreases.
3. Take note that V_{G2} is fixed, and since V_{S2} decreases, V_{GS2} increases.
4. Take note also that $V_{DS2} = V_{D2} - V_{S2}$ therefore, V_{DS2} increases.
5. Because V_{GS2} and V_{DS2} increases, then it follows that I_{DS2} increases.
6. In the end, I_{OUT} should decrease but a relatively "slower" rate.

Question Q2.2: (8 pts)

Let's see if you're paying attention. Fill in the blanks, and refer to Figure 2.9. Assume $V_{IN} = V_{IC}$ is fixed but V_{IP} is free to move. Answer with increase, decrease, or no change.

1. When V_{IP} decreases, $V_{GS,M1}$ decreases.
2. When $V_{GS,M1}$ decreases, $I_{DS,M1}$ decreases.
3. When $I_{DS,M1}$ decreases, V_{ON} increases, and $I_{DS,M2}$ increases.
4. When $I_{DS,M2}$ increases, V_{OP} decreases.

Question Q2.3: (2 pts)

Let's put on your thinking cap. When V_{IP} increases, the $I_{DS,M1}$ increases. How high can $I_{DS,M1}$ be until all the current in $I_{DS,M2}$ is "stolen"? Assume that the DP is biased by some I_{TAIL} current. Elaborate and prove your answer.

- $I_{DS,M1}$ can consume the entire I_{TAIL}. This way, all current will flow through M1 and M2 will be off. If all of I_{TAIL} goes through M1, then $V_{\mathrm{OP}} = V_{DD}$ since there is no current in M2. Still, V_{DD} is the maximum output voltage.

Question Q2.4: (7 pts)

Let's see if you're paying attention. Fill in the blanks, and refer to Figure 2.9. Assume $V_{ID} = 0$ and V_{IC} is free to move. Answer with increase, decrease, or no change.

1. When V_{IC} decreases, $V_{GS,M1}$ decreases, and $V_{GS,M2}$ decreases.
2. When V_{IC} decreases, $I_{DS,M1}$ remains the same, and $I_{DS,M2}$ remains the same.
3. When V_{IC} decreases, V_{ON} remains the same, and V_{OP} remains the same.
4. When V_{IC} decreases, V_{TAIL} decreases.

Question Q2.5: (1 pts)

What's the CMRR assuming $A_{dm} \approx 5$ and $A_{cm} \approx 600u$?

- $CMRR = \frac{A_{dm}}{A_{cm}}$
- $CMRR = \frac{5}{600\mu}$
- $CMRR = 8.33k$

Part III: Exercise (20 pts)

A. Miller Operational Amplifier (10 pts)

Figure 3.1 is a simple Miller Amplifier. Answer the following questions.

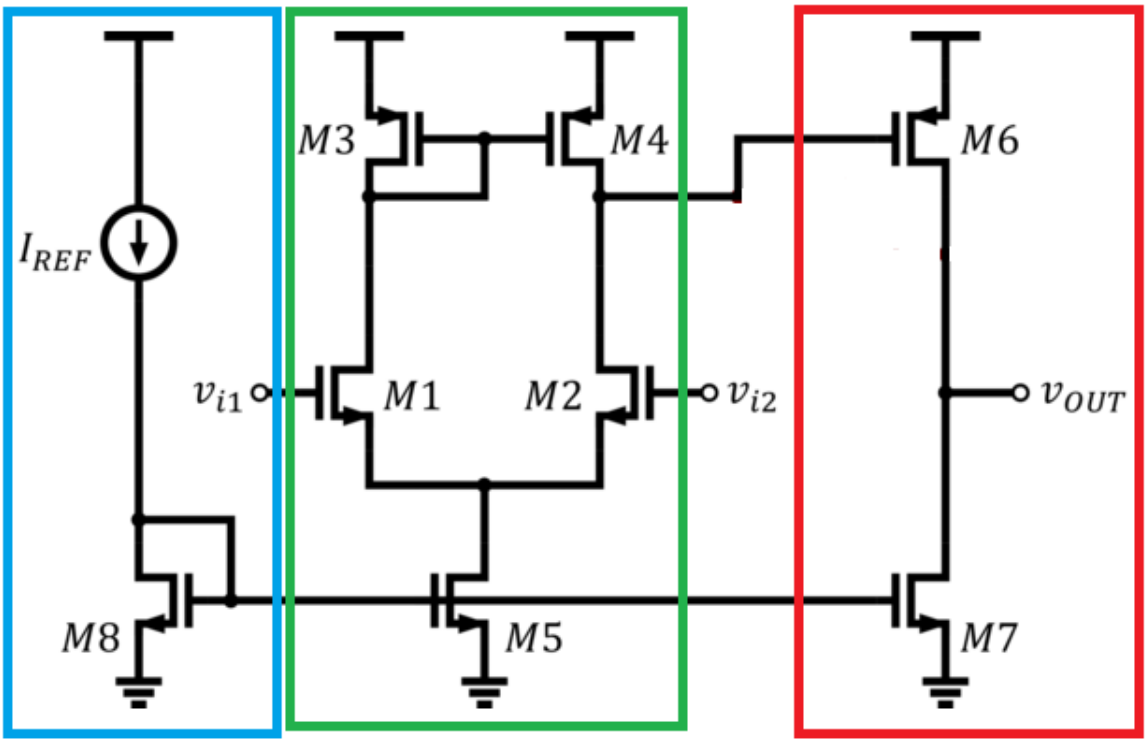

Figure 3.1 Simple Two-Stage Miller Amplifier

1. Describe what do the electrical elements in the blue section do? (1 pt)
- The circuit in the blue section acts as a current mirror biasing circuit. It biases the tail current source of the differential pair in the green section and the NMOS active load at the red section.

2. What kind of circuit is in the green section? (1 pt)
- The circuit in the green section is a differential pair with a single output node. It acts the same as the "usual" differential pair with resistors at the drain of the NMOS but this time, those "resistors" are in the form of a PMOS current mirror. Also, the PMOS current mirror copies the Vout that is supposed to be at M1. Thus, there is no loss of gain.

3. What kind of circuit is in the red section? (1 pt)
- The circuit in the red section is a PMOS common source amplifier with an active NMOS current source load.

4. In relation to #2, what is M5 for? (1 pt)
- M5 acts as the tail current source.

5. Do we want M5's output impedance to be higher or lower? Why? (1 pt)
- We want the output impedance of M5 to be higher since it gives us a lower A_{cm} and therefore, a better CMRR.

6. List at least 2 ways to increase the output impedance of M5. (1 pt)
- We can use a cascode structure or we can just add a resistor.

7. What does M3 and M4 do? (1 pt)
- M3 and M4 acts as active loads for M1 and M2, respectively. Similarly, Since the differential pair has only one output node, the current mirror M3 and M4 is used to copy the current of M1 to M2 so that there is no loss.

8. What does M6 and M7 do? (1 pt)
- M6 and M7 are amplifier stages. M6 receives the differential signal from the green circuit and M7 acts as an NMOS active load (current source).

9. If you were to design this Miller Amplifier, who would you tackle first, the red, green, or blue section? Elaborate your answer. (2 pt)
- I would tackle the green section first. It is the circuit where the input first goes and also the blue and the red circuits are just based from the needed parameters of the green circuit.

B. Summarize! (10 pts)

You will be graded how well you write/summarize your answers.

In a maximum of 3 paragraphs, can you summarize what you have learned about analog design? Be sure to include things like:

- Design philosophies
- Trade-offs to watch out for
- Design methodologies
- Ideas you think that can improve your design strategies
- Add things that may not be included in the lab discussion but you may have discovered along the way

Summary:

Overall, I realized that I should really do analog design as I feel dumb when it comes to logic gates. I finished the Razavi lectures in electronics last December, but I had no way to apply it. I did not know much about simulating those kinds of circuits. Eventually in this course, I learned how to create circuits like those. I learned how to size transistors and check the parameters. I liked how analog design revolves around the “theory -> practice -> theory” cycle.

In this course, I also realized that analog design is hard because of too many tradeoffs to be considered. You need to consider the power, the area, the stability, gain, frequency, and so much more. For example, when we use feedbacks, the stability and bandwidth are both improved but gain is reduced drastically. Trying to obtain a higher $g_m r_o$ may not be possible unless we increase the lengths of the device. If there is a limited area, then we need to consider this too.

Right now, I have a book here given to me by my father. The book is Analysis and Design of Analog Integrated Circuits. I tried to study it for a while but after the first topics (semiconductor physics) I felt so tired. Although I learned about the parasitic capacitances and how the doping affects the depth of the depletion layer. I think I still need to learn more about the basics before reading the book. I really enjoyed taking the course.

C. (BONUS) Finish Strong! (5 pts)

Sometimes it's great to not just finish a course, but to finish "strong"! What we mean by that is that, let's try to expand ourselves and do better than what was recommended in this course. With that, consider Figure 3.2 which shows an amplifier with higher complexity. Then, answer the following questions.

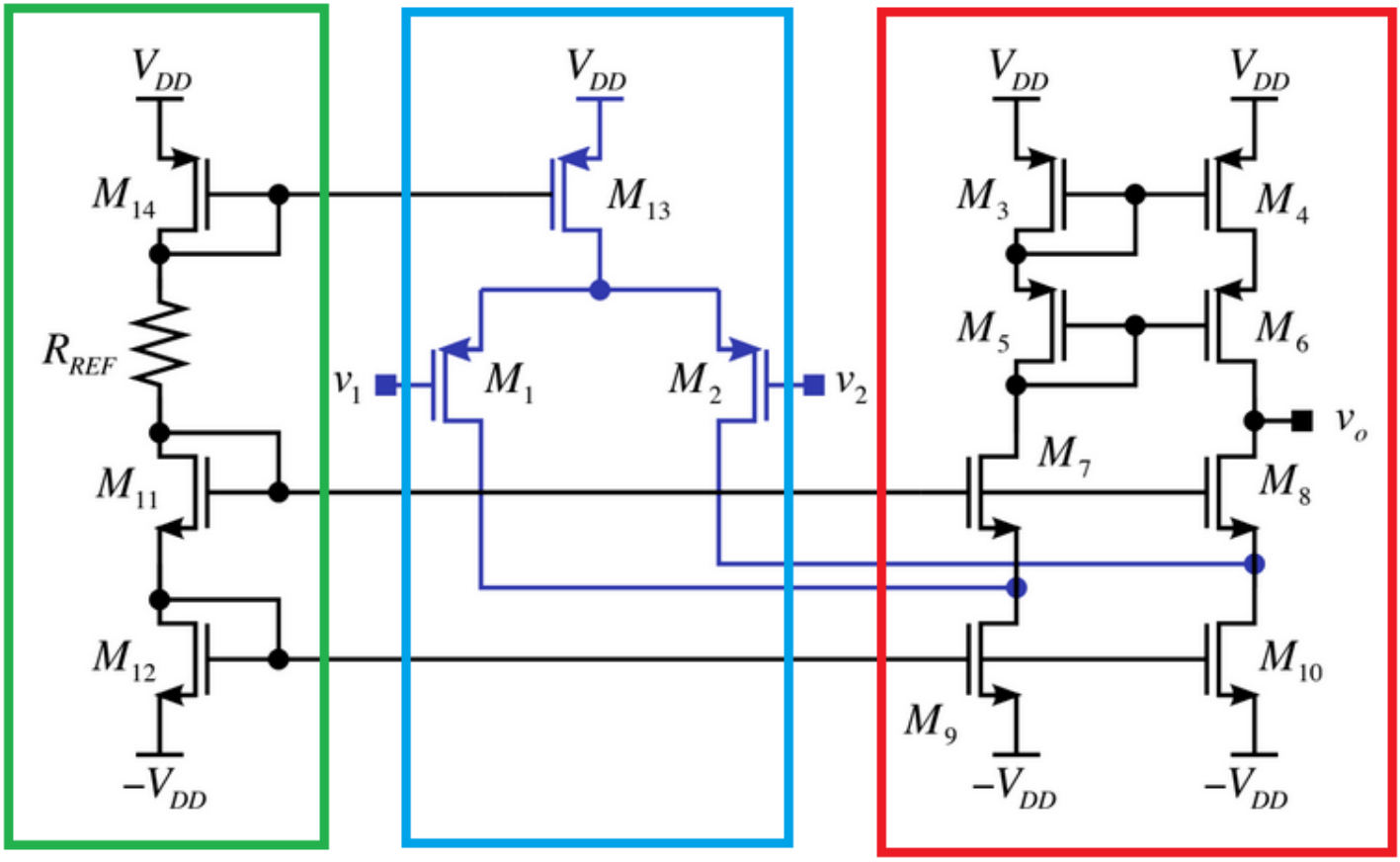

Figure 3.2 Super cool amplifier

1. What do you call this amplifier? (1 pt)
- Miller Operational Transconductance Amplifier

2. What circuit is the green section? (1 pt)
- The circuit in the green section is a modified version of the cascode current mirror. I really don't know what R_{REF} is for but I think it has something to do with the negation of channel length modulation effects.

3. What circuit is the blue section? (1 pt)
- The circuit in the blue section is a differential pair.

4. What circuit is the red section? (1 pt)
- The red section is just a telescopic cs stage.

5. This amplifier has very high gain. Why? Estimate to a first-order what that gain would be? (i.e. $A_v = ?$) (1 pt)
In general, $A_v = -G_m R_{out}$. This circuit has an $R_{out} = [(1 + g_{m,8}r_{o,8})r_{o,10} + r_{o,8}] \parallel [(1 + g_{m,6}r_{o,6})r_{o,4} + r_{o,6}]$. And $G_m \approx g_{m,10}$. Thus, this circuit will have a very high gain since it has a very high output impedance.