University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 08 – Cascode Current Mirror and Differential Pair

What will you learn from this lab?

- Important concepts to consider about differential pairs
- Summarizing everything you've learned so far

A few reminders for any lab:

Each lab will always be broken down in 3 main sections

- Prelab/Review – this section can be treated like a "pre-lab" where you need to recall some of the previous concepts in your earlier courses or those that were discussed in the lecture.
- Training – this section guides you through a skill that you must learn. This could be a method in using the tool or a concept that is new to you.
- Postlab/Exercises – are some problems that you need to solve. Sometimes you need LTspice for it, and some don't. It's there for you to test what you have learned.
- Supplementary reading – these is an optional content but for the interested students, you can read and answer some of its questions. It's to further help you appreciate what IC design is.

There will be special boxes that you need to watch out for.

BLUE BOXES: Are used for useful notes and discussions. They can help you understand and appreciate the current topic at hand.

RED BOXES: Are notes that you need to watch out for. Some of these may be warnings that pertain to some limitations of our simulator. Or possibly some warnings on how to use particular circuit models.

GREEN BOXES: Are questions for that particular training task. They are also in the answer sheet so they'll be hard to miss.

Part I: Review

1. What does a cascode current mirror do?
2. What is a differential circuit?
3. Concisely, describe differential mode and commode mode.

Part II: Training

A. Cascode Current Mirror

In the previous lab, we've seen that a single transistor working as a current source is far from ideal because the output impedance is not "infinite" enough. We keep on emphasizing that we want very high impedance to achieve very high gain. From your lecture slides, the cascode current mirror is an improvement of the single transistor current source. Figure 2.1 shows the schematic of the cascode current mirror. Here, M2 acts like a "shield" to protect the drain of M1 form changing. If that happens, then the current being delivered to the entire M1-M2 branch would want to stay constant even when the drain of M2 changes.

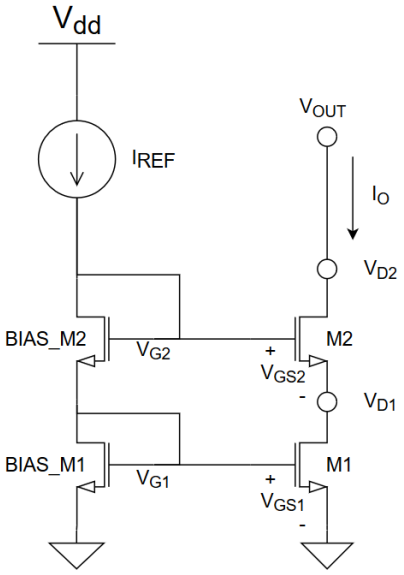

Figure 2.1 Cascode current mirror

The lecture went straight away to the derivation of the effective output impedance by small-signal analysis. Let's step back a bit and discuss what really happens and why the output impedance increases. Remember, we have a high output impedance if I_O resists any change in the V_{D2} node. Let's focus our attention on Figure 2.1 and take note of all the node voltages. Let's add the NMOS current equation (in saturation) for clarity.

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS})$$

Follow the sequence of events:

1. It is evident that $V_{OUT} = V_{D2}$. They're just the same node.
2. As V_{OUT} increases, V_{D2} increases, and therefore V_{DS2} increases. This will increase I_{DS2} or I_{OUT}.
3. $I_{OUT} = I_{DS2} = I_{DS1}$. If I_{DS1} increases but with V_{GS1} is fixed, then V_{DS1} needs to increase and therefore V_{D1} increases. Note that V_{S1} is tied to ground so if it's fixed then V_{D1} needs to adapt.
4. Because V_{D1} increases, and $V_{D1} = V_{S2}$, then V_{S2} increases.
5. Since V_{G2} is fixed due to the biasing transistor, and since V_{S2} increases, V_{GS2} decreases.
6. Note that $V_{DS2} = V_{D2} - V_{S2}$ then V_{DS2} also decreases.
7. Because V_{GS2} and V_{DS2} decrease at the same time, then it follows that the rate I_{DS2} increases slows down.
8. Essentially, when V_{D2} increases, it tries to increase I_O but because the drain of M1 increases as well, this affects the source of M2 which decreases the rate of increase in I_O.
9. Give time to study these sequences of events.

Here's a short summary of what happens:

- As V_{OUT} increases, V_{D2} increases, V_{DS2} increases and therefore I_{OUT} or I_{DS2} increases.
- I_{OUT} increasing needs to increase V_{D1}, which increases V_{DS1} to match the current.
- As $V_{D1} = V_{S2}$ increases, V_{GS2} and V_{DS2} decreases.
- The decrease in V_{GS2} and V_{DS2} slows down the rate of increase of I_{OUT}.
- Essentially, the increase in V_{OUT} resists increasing I_{OUT}.

Make sure to understand the sequence of events because it can be tricky. The strategy is to treat each node changing one at a time starting with V_{D2}. Let's look at this in the small-signal perspective as it may give an alternative view. This is another important technique to consider: *deriving the math to look for answers.* Figure 2.2 shows the small-signal model of Figure 2.1.

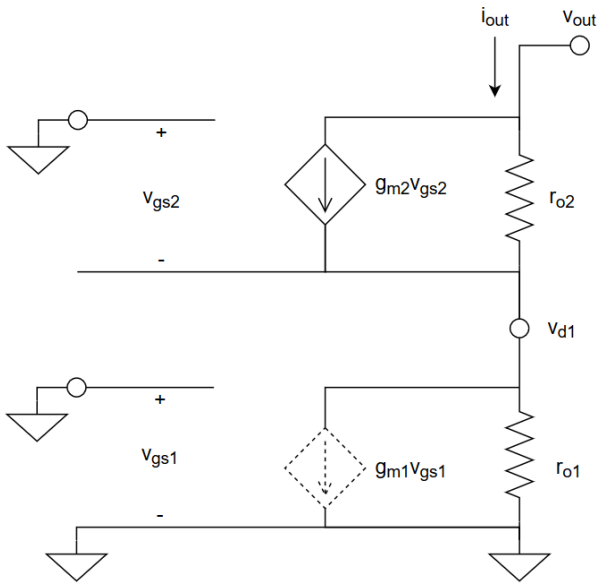

Figure 2.2 Small-signal model of Figure 2.1.

Drawing the small-signal model should be straight forward. Take note of the following points to consider:

- The small-signal model for M1 is at the bottom and M2 at the top.
- The gates of both M1 and M2 are biased by some constant voltage source from BIAS_M1 and BIAS_M2, respectively. Therefore, the gates for both M1 and M2 are shorted to ground.
- $v_{gs1} = 0$ by simple KVL. This results in $g_{m1}v_{gs1} = 0$ and therefore the dependent current source of M1 acts like an open circuit. $g_{m1}v_{gs1}$ is drawn with dotted lines instead.
- Essentially, M1 is acting like a normal current source with r_{o1} as its output impedance.
- $v_{gs2} = -v_{d1}$ by KVL. This makes $g_{m2}v_{gs2}$ still present in the circuit.
- $i_{out} = \frac{v_{d1}}{r_{o1}}$ by KCL. Remember, what comes in must also go out. This also says that $v_{d1} = i_{out}r_{o1}$.

With the established small-signal model and other important considerations, we have an alternative analysis of the cascode circuit. Remember, small-signal analysis pertains to the changes that may occur. Ultimately, we are interested how v_{out} changes i_{out}. First, let's determine what influences the output current i_{out}. If we take the KCL at the v_{out} node, we have:

$$i_{out} = g_{m2} v_{gs2} + \frac{v_{out} - v_{d1}}{r_{o2}}$$

But remember, $v_{gs2} = -v_{d1}$ and plugging this in the equation above and re-arranging terms yields:

$$i_{out} = v_{out} \cdot \left(\frac{1}{r_{o2}}\right) - v_{d1} \cdot gm_2 - v_{d1} \cdot \frac{1}{r_{o2}} \qquad (1)$$

We'll also add in:

$$v_{d1} = i_{out} r_{o1} \qquad (2)$$

Both equations already give us the hints we need to understand how the cascode works.

- In equation (1), i_{out} is controlled by both v_{out} and v_{d1} voltages.
- That means i_{out} changes whenever the drain of M2 and M1 changes.
- Equation (1) also implies that an increase in M2 drain voltage (v_{out}) increases i_{out}.
- However, an increase in M1 drain voltage (v_{d1}) decreases i_{out}.
- The increase in M1 drain voltage (v_{d1}) translates to a decrease in v_{gs2} and v_{ds2}.
    - This is evident in equation (1) by the g_{m2} and $\frac{1}{r_{o2}}$ terms.
    - The $-v_{d1} \cdot gm_2$ is actually $v_{gs2} \cdot gm_2$ but with $v_{gs2} = v_{g2} - v_{s2} = 0 - v_{d1} = -v_{d1}$.
    - Since the gate is tied to ground (due to constant voltage source) then $v_{g2} = 0$ and $v_{s2} = v_{d1}$ as evident in both Figure 2.1 and Figure 2.2.
    - The combined terms of $v_{out} \cdot \left(\frac{1}{r_{o2}}\right) - v_{d1} \cdot \frac{1}{r_{o2}}$ is technically $v_{ds2} = v_{d2} - v_{s2} = v_{out} - v_{d1}$ but these terms imply that the rate of change in v_{out} and v_{d1} are not the same.
    - A more intuitive implication for this is that the effects of increasing v_{out} (or v_{d2}) is reduced by the increase in v_{d1}. In other words, the v_{out} increase is reduced by v_{d1}.
    - This is the same as our previous analysis: as v_{out} increases, v_{gs2} and v_{ds2} also decrease.
- Equation (2) $v_{d1} = i_{out} r_o$ indicates that as i_{out} increases due to the increase in v_{out}, $v_{d1} = v_{ds1}$ needs to also increase to match the i_{out} current.
- The small-signal analysis confirms what we have just discussed previously! Cool right?

If we plug equation (2) into equation (1) and solve for i_{out}/v_{out} we get equation (3):

$$\frac{i_{out}}{v_{out}} = \frac{1}{g_{m2} r_{o2} r_{o1} + r_{o2} + r_{o1}} \qquad (3)$$

Equation (3) tells us how much a small-signal current change i_{out} is produced for a given unit of small-signal voltage change v_{out}. Take the reciprocal of this and we get the output impedance in equation (4).

$$\frac{v_{out}}{i_{out}} = R_{out,eq} = g_{m2} r_{o2} r_{o1} + r_{o2} + r_{o1} \qquad (4)$$

Typically, $g_{m2} r_{o2} r_{o1} \gg r_{o2} + r_{o1}$ and therefore $R_{out,eq} \approx g_{m2} r_{o2} r_{o1}$. Moreover, equation (4) tells us that the cascode transistor M2 multiplies the output impedance of M1 by the intrinsic gain $g_{m2} r_{o2}$. This effect is useful

in scenarios where we need to amplify the output impedance. We need to add extra transistors to bump up those impedances! Let's take time to appreciate this in action. Do the following:

1. Open "lab08_nmos_current_mirror.asc". This is our basic current mirror from the previous lab.
2. Make sure all widths are $W = 10\ um$ and all lengths are $L = 1\ um$.
3. Simulate both the drain current and output impedance. Take note of the reading at $V_{DS} = 0.6\ V$. You should get Figure 2.3.

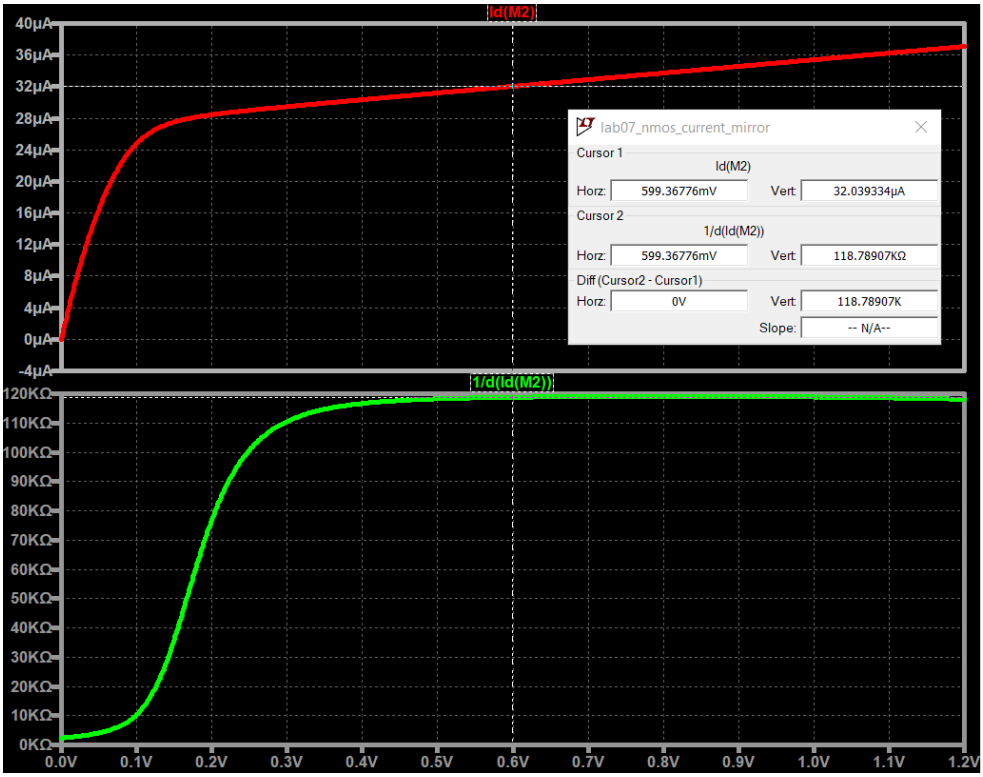

Figure 2.3 Current and output impedance for a normal current mirror

4. Open "lab07_nmos_cascode_mirror.asc". This is the cascode current mirror in Figure 2.4.
5. Make sure all widths are $W = 10\ um$ and all lengths are $L = 1\ um$.
6. Simulate both the drain current and output impedance. Take note of the reading at $V_{D4} = 0.6\ V$. You should get Figure 2.5.

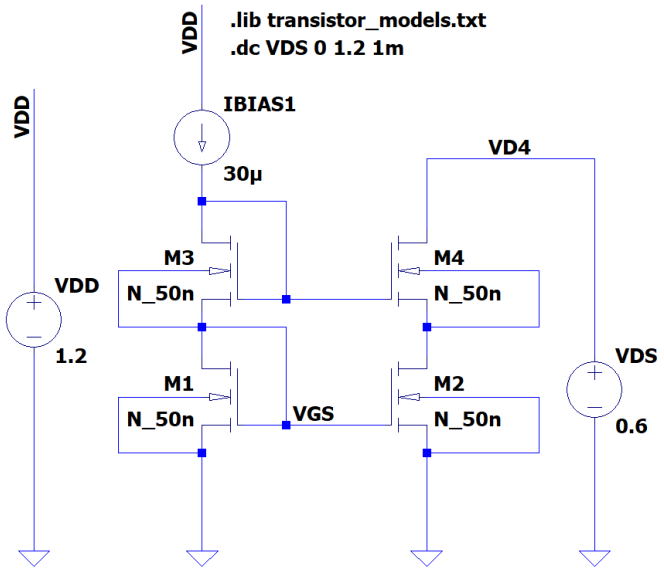

Figure 2.4 Schematic simulation for cascode current mirror

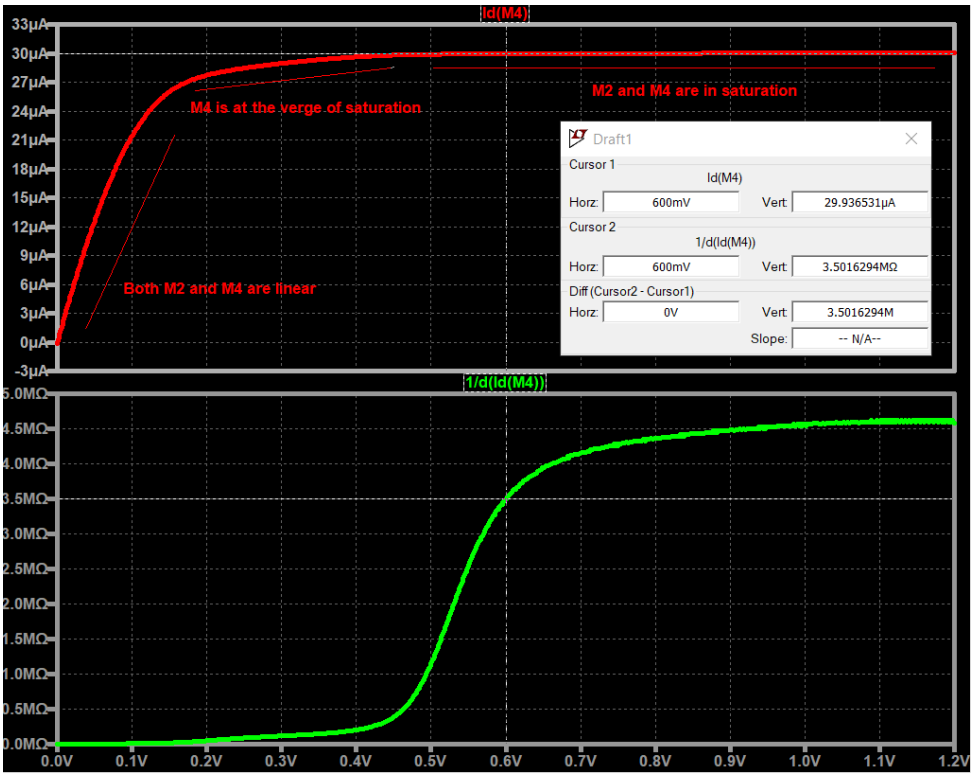

Figure 2.5 Current and output impedance for a cascode current mirror

Great! Now let's just appreciate a few things before we end this part.

- At a glance, the I-V curve of the cascode current mirror in Figure 2.5 is definitely flatter compared to the normal current mirror Figure 2.4.
- The output impedance curves also show that the cascode current mirror has an incredibly higher output impedance. If you compare the impedances, the cascode current mirror is 30 times larger.
- Looking closely at the cascode current mirror, the high impedance starts to roll off when $V_{D4} \leq 0.6\,V$. When V_{D4} is low, M4 and M2 start to operate in the linear region.
- The current plot of the cascode current mirror shows three regions:

- The flattest part is when both M2 and M4 are in saturation.
- The first point of decreasing output impedance is when M4 starts to get squeezed.
- It starts to operate in the linear region and that's roughly in the region when $0.2\ V \leq V_{D4} \leq 0.5\ V$.
- Lastly, the region when $V_{D4} < 0.2\ V$ is when both M2 and M4 are in the linear region.

Be sure to appreciate these discussions as they help understand how powerful the cascode circuit is.

QUESTION (Q2.1):
Let's see if you understood what really happens in a cascode. Answer with *increase(s)* or *decrease(s)* only. Following the same discussion in Figure 2.15.

1. As V_{OUT} decreases, V_{DS2} _____. This _____ I_{DS2} or I_{OUT}.
2. As I_{OUT} _____, V_{DS1} needs to _____. Hence $V_{D1} = V_{S2}$ _____.
3. Take note that V_{G2} is fixed, and since V_{S2} _____, V_{GS2} _____.
4. Take note also that $V_{DS2} = V_{D2} - V_{S2}$ therefore, V_{DS2} _____.
5. Because V_{GS2} and V_{DS2} _____, then it follows that I_{DS2} _____.
6. In the end, I_{OUT} should _____ but a relatively "slower" rate.

B. Differential Pair Basics: The Differential Mode

The differential pair (DP) is a powerful circuit that provides two things: (1) amplify the difference between two inputs, and (2) reject changes in the common value of the two inputs. These two features are called the differential mode and the common mode, respectively. Just like on our previous labs, our strategy is to appreciate how the circuit works from a large-signal perspective. Consider Figure 2.6 that shows the basic DP with a resistive load.

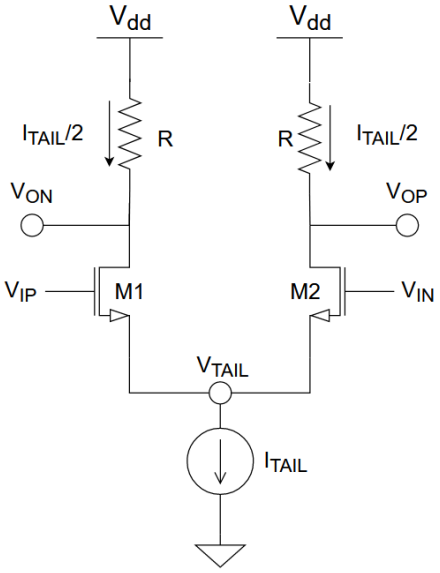

Figure 2.6 Basic Differential Pair with Resistive Loads

A quick summary from the lecture: *differential mode tells us how the difference of V_{IP} and V_{IN} changes the output V_{ON} and V_{OP} respectively. While the common mode tells us how the changes in the average of V_{IP} and V_{IN} (the common average), affects the average output of V_{ON} and V_{OP}*. Let's first focus on the differential mode. Referring to Figure 2.6, let's assume both transistors and resistances are identical, meaning their size, device parameters

and the resistive values are the same. Moreover, let's say we have some I_{TAIL} which also sets the current that goes through both transistors. Doing a critical KCL on the V_{TAIL} node gives us:

$$I_{TAIL} = I_{DS,M1} + I_{DS,M2} \qquad (5)$$

Suppose $V_{IP} = V_{IN}$ then it also implies that $V_{GS,M1} = V_{GS,M2}$. If that's the case then $I_{DS,M1} = I_{DS,M2}$ and we have:

$$I_{DS,M1} = I_{DS,M2} = \frac{I_{TAIL}}{2} \qquad (6)$$

In other words, when there is no difference between V_{IP} and V_{IN} (i.e. $V_{IP} - V_{IN} = 0 \rightarrow V_{IP} = V_{IN}$), then the current is equally divided between the two transistors. Since the currents are equal, then the voltage drop across the two resistances are also the same, because:

$$V_{ON} = V_{OP} = V_{DD} - I_{DS}R \qquad (7)$$

Take note of Equations (5), (6), and (7) since they will be our working equations. Simple right? We'll consider this as this normal state of the DP. From the lecture, differential mode happens when $V_{IP} - V_{IN} \neq 0$ and that difference gets amplified at the outputs. Let's consider different scenarios. Let's say initially $V_{IP} = V_{IN} = V_{IC}$ where V_{IC} is some *input common voltage* that is high enough to put the two transistors in saturation.

Case 1: V_{IP} increases but $V_{IN} = V_{IC}$ is fixed. The following happens:

- $V_{GS,M1}$ increases, therefore $I_{DS,M1}$ increases.
- $I_{DS,M1}$ increasing, increases the voltage drop across the resistor on its branch.
- Increasing voltage drop decreases V_{ON} because of $V_{ON} = V_{DD} - I_{DS,M1}R$ in equation (7).
- $I_{DS,M1}$ increasing also decreases $I_{DS,M2}$ because of $I_{DS,M2} = I_{TAIL} - I_{DS,M1}$ in equation (5).
- Decreasing $I_{DS,M2}$ decreases the voltage drop across the resistor on its branch.
- Decreasing voltage drop increase V_{OP} because of $V_{OP} = V_{DD} - I_{DS,M2}R$ in equation (7).
- This is visualized in Figure 2.7.

Case 2: V_{IN} increases but $V_{IP} = V_{IC}$ is fixed. The following happens:

- $V_{GS,M2}$ increases, therefore $I_{DS,M2}$ increases.
- $I_{DS,M2}$ increasing, increases the voltage drop across the resistor on its branch.
- Increasing voltage drop decreases V_{OP} because of $V_{OP} = V_{DD} - I_{DS,M2}R$ in equation (7).
- $I_{DS,M2}$ increasing also decreases $I_{DS,M1}$ because of $I_{DS,M1} = I_{TAIL} - I_{DS,M2}$ in equation (5).
- Decreasing $I_{DS,M1}$ decreases the voltage drop across the resistor on its branch.
- Decreasing voltage drop increase V_{ON} because of $V_{ON} = V_{DD} - I_{DS,M2}R$ in equation (7).
- This is visualized in Figure 2.8.

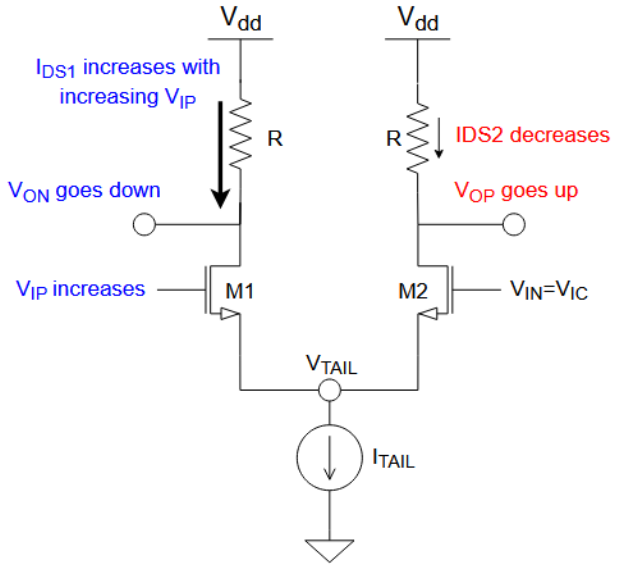

Figure 2.7 Visualization of when V_{IP} increases and V_{IN} is fixed.

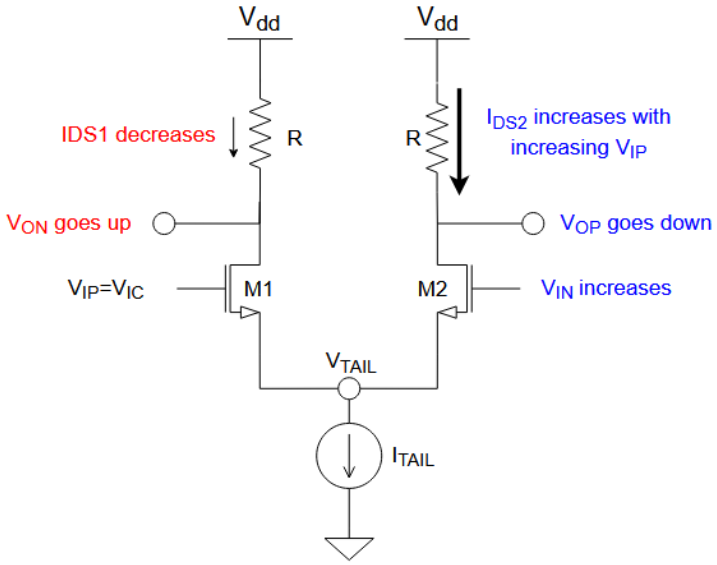

Figure 2.8 Visualization of when V_{IN} increases and V_{IP} is fixed

Case 1 and case 2 are just opposites of each other. They are elaborated further for clarity. The important sequences to be considered are:

- Increasing an input voltage increases the current on the same branch.
- The increasing current decreases the output voltage on the same branch due to the increasing voltage drop across the resistor.
- The increasing current *"steals" current from the other branch*, hence decreasing the current and decreasing the voltage drop, and the output voltage increases for the branch with the stolen current.
- The I_{TAIL} acts like the "maximum" allowable current that the main branch can steal.

Case 3: V_{IP} and V_{IN} symmetrically move away from each other

What this means is that *when V_{IP} increases, V_{IN} decreases for the same amount*. This is the standard way of defining the *differential mode* of a DP. We want to understand and characterize how the outputs change with a *symmetric* change at the inputs. The symmetric difference between V_{IP} and V_{IN} can be called the *differential input* V_{ID} such that the increase in V_{IP} is $\frac{V_{ID}}{2}$ and the decrease in V_{IN} is $\frac{V_{ID}}{2}$. The vice versa also happens when we say that V_{ID} is negative. This means, the decrease in V_{IP} is $\frac{V_{ID}}{2}$ and the increase in V_{IN} is $\frac{V_{ID}}{2}$. Previously, we also mentioned that V_{IP} and V_{IN} where initially at some starting bias V_{IC} then we can say that the total V_{IP} and V_{IN} would be:

$$V_{IP} = V_{IC} + \frac{V_{ID}}{2}$$

$$V_{IN} = V_{IC} - \frac{V_{ID}}{2}$$

Figure 2.9 visualizes this.

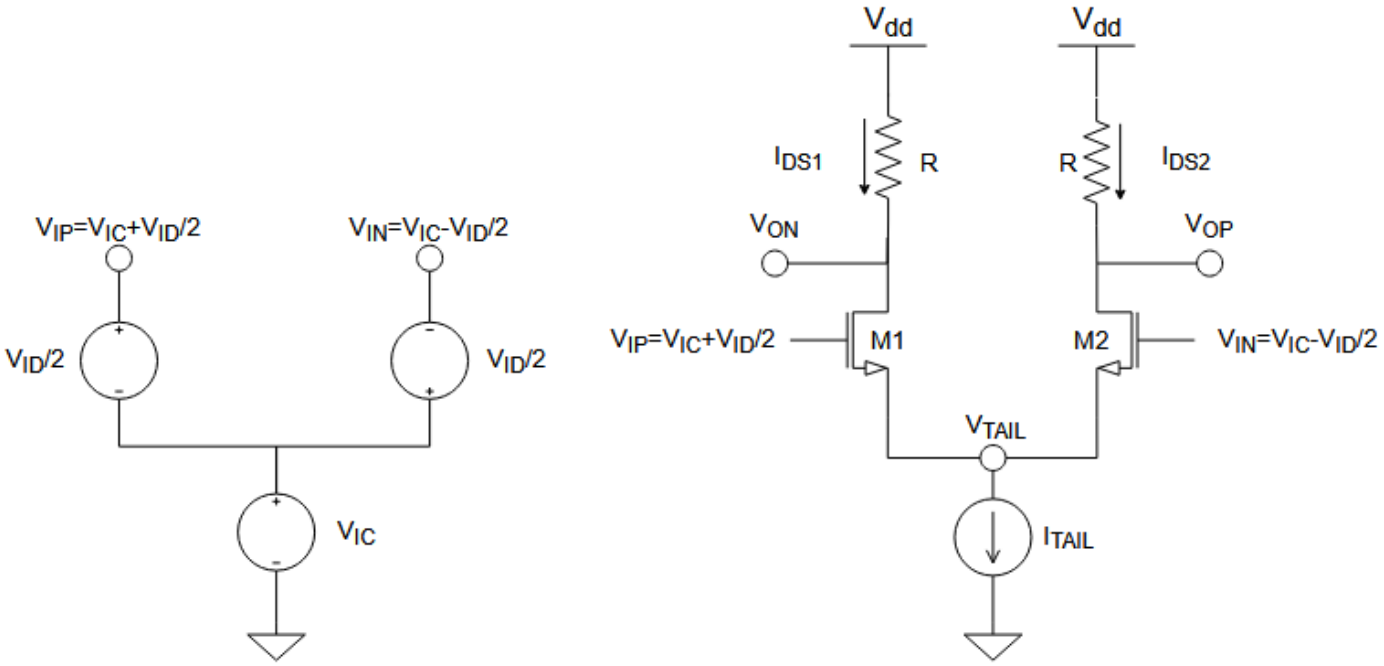

Figure 2.9 Differential pair with V_{IP} and V_{IN} visualized

The voltage source on the left side should be clear to you how they bias the DP. Again, when V_{ID} increases, that difference is equally shared between V_{IP} and V_{IN} where one side increases while the other side decreases by $\frac{V_{ID}}{2}$. Take note that this can be interchangeable but by convention, the side with V_{IP} increases while V_{IN} decreases with increasing V_{ID}. If V_{ID} is negative, the opposite happens.

How does the current change for this scenario? The effects are the same just like in cases 1 and 2 but combined. The effects of increasing and decreasing the currents on each branch being shared by I_{TAIL}, moves faster. That means when V_{IP} increases and V_{IN} decreases by the same amount, then $I_{DS,M1}$ increases and $I_{DS,M2}$ decreases

faster due to the changing voltages. Eventually, V_{ON} and V_{OP} decreases and increases, respectively. Make sure to grasp this concept as this is the easiest way to remember how a DP works in differential mode.

QUESTION (Q2.2):
Let's see if you're paying attention. Fill in the blanks, and refer to Figure 2.9. Assume $V_{IN} = V_{IC}$ is fixed but V_{IP} is free to move. Answer with increase, decrease, or no change.

1. When V_{IP} decreases, $V_{GS,M1}$ _____.
2. When $V_{GS,M1}$ _____, $I_{DS,M1}$_____.
3. When $I_{DS,M1}$ _____, V_{ON} _____, and $I_{DS,M2}$ _____.
4. When $I_{DS,M2}$ _____, V_{OP} _____.

QUESTION (Q2.3):
Let's put on your thinking cap. When V_{IP} increases, the $I_{DS,M1}$ increases. How high can $I_{DS,M1}$ be until all the current in $I_{DS,M2}$ is "stolen"? Assume that the DP is biased by some I_{TAIL} current. Elaborate and prove your answer.

Take note, whenever case 3 happens, we are more interested on how V_{ON} and V_{OP} changes, independently. That is, how V_{IP} and V_{IN} changes V_{ON} and V_{OP}, respectively. Then the overall result is taken by the difference of V_{ON} and V_{OP}. For a given *differential input V_{ID} there's an effective differential output V_{OD}*. However, we the conventional definition of *differential gain (A_v)* is the single sided change in output over the change in input. This means when V_{IP} changes it correspondingly changes V_{ON}. When V_{IN} changes it correspondingly changes V_{OP}. That's where the differential gain comes in. Do the following:

1. Open "lab08_diff_pair.asc". You should get Figure 2.10.
2. Observe the following:
   - The transistors have $W = 10\ um$ and $L = 1\ um$. All resistances are $20\ k\Omega$.
   - The differential pair is biased by some $I_{TAIL} = 60\ uA$.
   - The left side of the schematic is the biasing of V_{IP} and V_{IN} where V_{ID} and V_{IC} are the differential and common voltages that we discussed earlier.
   - The biasing is a work around of the biasing shown in Figure 2.9. The V_{IP} side is the normal branch where $V_{IP} + \frac{V_{ID}}{2}$. Take note, we're just treating the entire $\frac{V_{ID}}{2}$ as a single variable for convenience.
   - The V_{IN} side is also the same but we needed to "copy" that same $\frac{V_{ID}}{2}$ added to the V_{IP} branch and invert it by using a *voltage-controlled voltage source (VCVS)*.
   - You can find this in the components section and look for "E" which is the VCVS. The idea is to take in the VID_OVR_2 voltage as the input (observe the input side). Then the output is multiplied by -1, to invert that VID_OVR_2 voltage source. In the end, the source is superimposed on the V_{IC} source.
   - Also, observe that VID_OVR_2 source is swept only from -0.6 V to 0.6 V. That's actually a 1.2 V input sweep. This sort of hints that one benefit of using a DP is a larger input swing (and also an output swing later on).

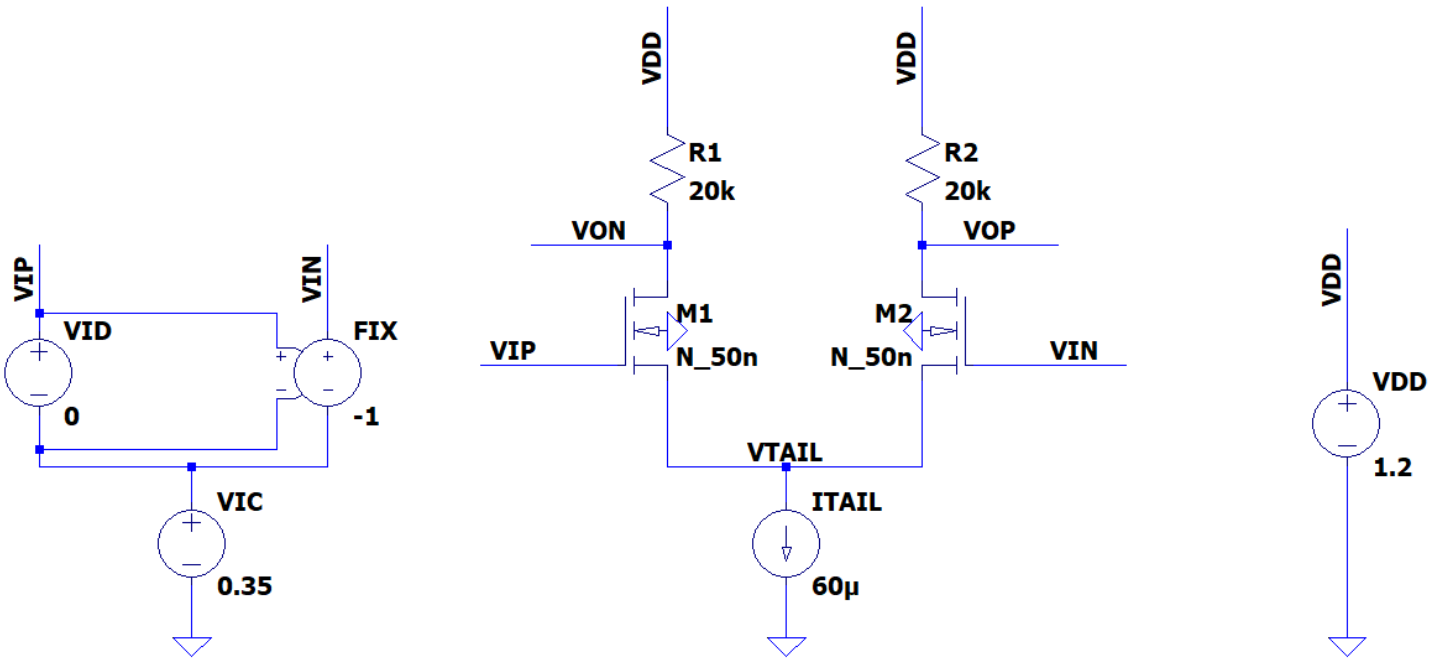

Figure 2.10 Schematic for simulating a differential pair

3. Run the simulation and plot the following:
   - Make 2 separate plotting planes.
   - On the upper plane, plot V_{ON} and V_{OP}.
   - On the lower plane, plot the current in R_1 and R_2.
   - If you did this right, you should get Figure 2.11.

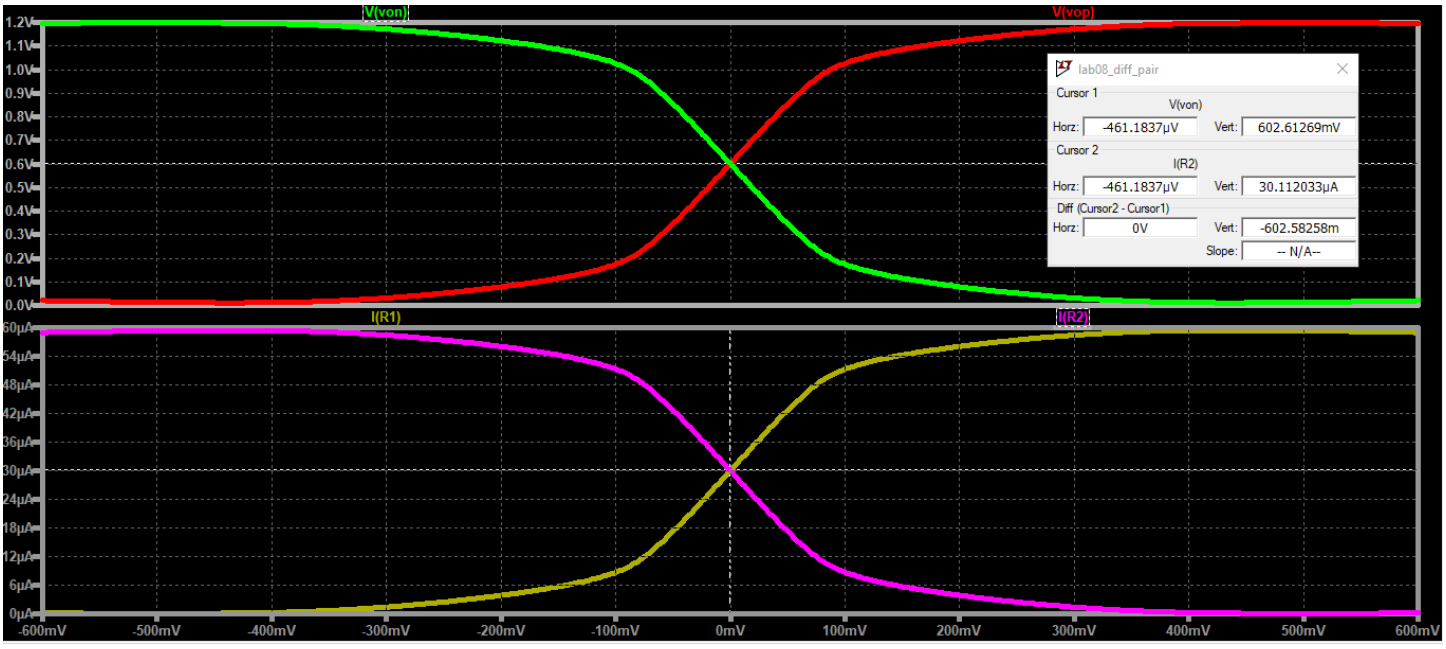

Figure 2.11 Currents and output voltages for the differential pair in Figure 2.10

Let's appreciate some of the observations with what we discussed earlier:

- When $V_{ID} = 0$ (that's the part where the cursor is pointing), we could see that $V_{ON} = V_{OP} = 0.6\,V$ and $I_{DS,M1} = I_{DS,M2} = 30\,uA$.
- This is consistent with our discussion that: "*When there is no difference between V_{IP} and V_{IN} (i.e. $V_{IP} - V_{IN} = 0 \rightarrow V_{IP} = V_{IN}$), then the current is equally divided between the two transistors".*
- When V_{ID} increases (right side of the figure), V_{IP} increases, $I_{DS,M1}$ increases (the yellow/gold like color), and V_{ON} decreases (the green color).
- On the other side when V_{ID} increases (still on the right side of the figure), V_{IN} decreases, $I_{DS,M2}$ decreases (pink color), and V_{OP} increases (red color).
- Let's go the opposite way, when V_{ID} decreases (becomes more negative and on the left side), V_{IP} decreases, $I_{DS,M1}$ decreases (the yellow/gold like color), and V_{ON} increases (the green color).
- On the other side when V_{ID} decreases (still on the left side of the figure), V_{IN} increases, $I_{DS,M2}$ increases (pink color), and V_{OP} decreases (red color).
- Overall, everything just fits our previous discussion!

Going back to our routinary analysis, we can describe how much change at the output appears if we refer to the small-signal model. Borrowing from the lecture, Figure 2.12 shows the small-signal model of the differential pair.

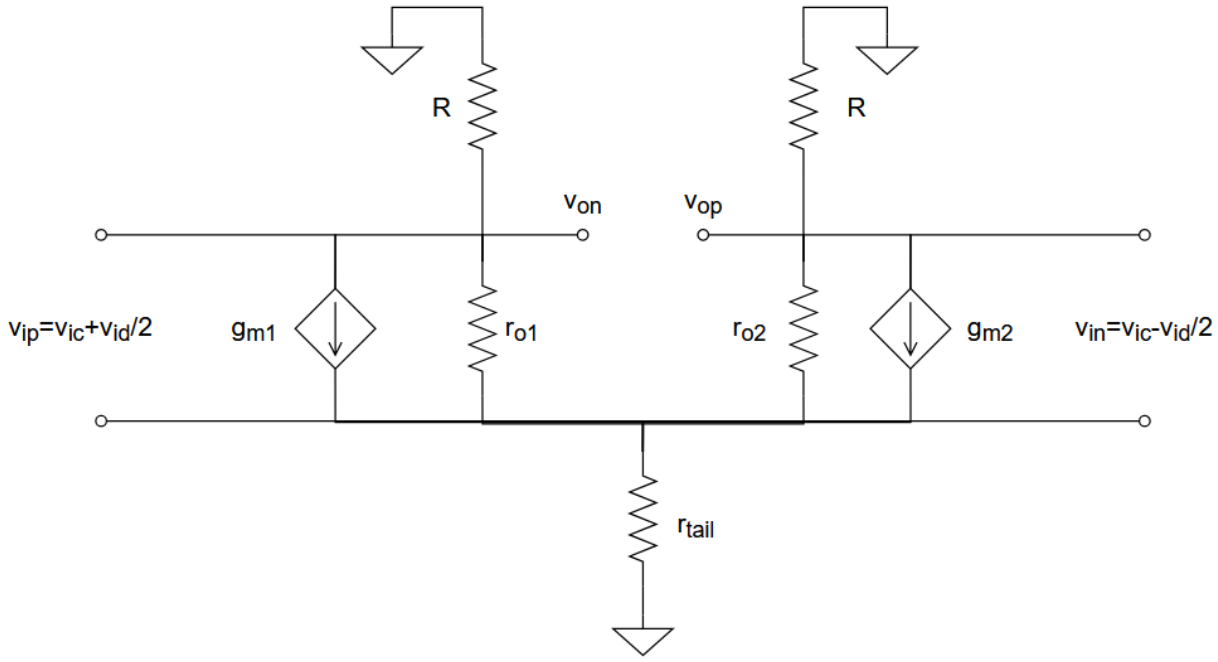

Figure 2.12 Small-signal model of the differential pair

Take note the small-signal model considers that the output impedance of the tail current source: r_{tail}. Let's inject that for now because we know it's difficult to create ideal current sources. The trick to analyzing differential pairs is to do it in half-circuit analysis. From case 1 and case 2, we know that the system is symmetric, so why not analyze the small-signal model using one side only. The idea is to cut Figure 2.12 in half and come up with a model that splits r_{tail} into 2. This results in Figure 2.13 which shows the half-circuit model and we only need to use 1 side. The r_{tail} needs to be split into two and we need to multiply both by $2r_{tail}$ because making them parallel gives the original r_{tail} such that $r_{tail} = (2r_{tail}||2_{rtail})$.

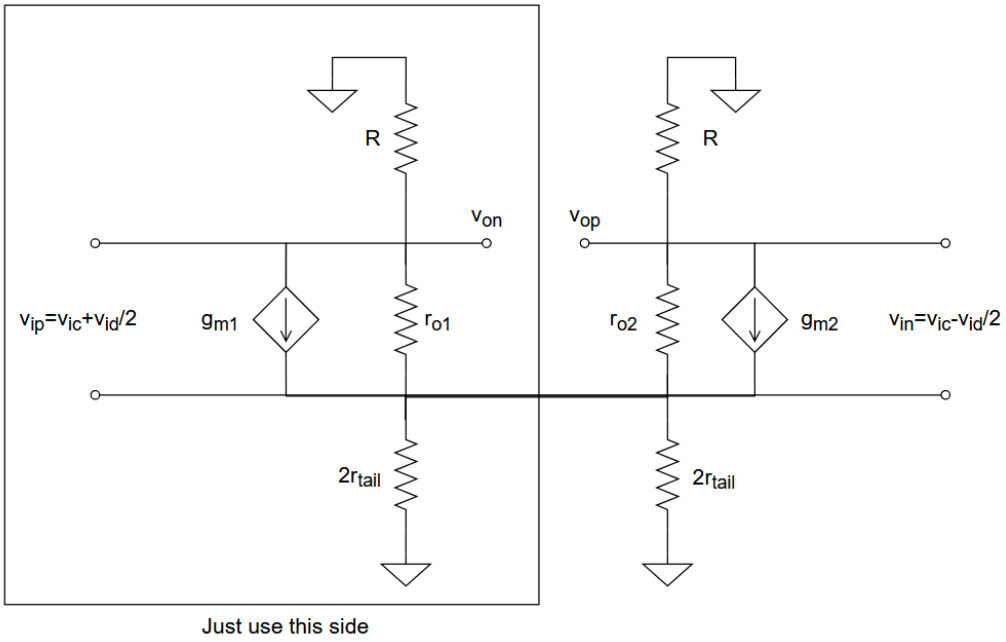

Figure 2.13 Half-circuit model of the differential pair

During differential, mode there are no changes in V_{IC} therefore the small-signal $v_{ic} = 0$. Only the small-signal differential input change v_{id} exists. If $v_{ic} = 0$, then the r_{tail} node is "virtually" ground. Accept this for now but you could also try to derive and determine why the r_{tail} node looks like a ground during differential mode. If that happens the Figure 2.13 would simplify to Figure 2.14.

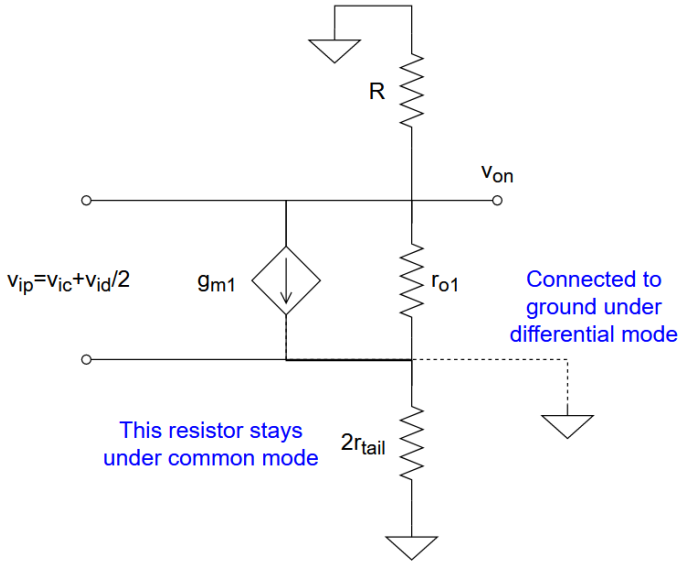

Figure 2.14 Half-circuit model depicting what happens during differential and common mode

Take note that the r_{tail} node connects to ground when we're under differential mode. This simplifies things because if you calculate the gain, it's nothing but the normal common source amplifier with a resistive load such that:

$$A_{dm} = -g_m(r_o||R)$$

Simple right! We can verify this through our simulations. We'll save you the trouble of characterizing the transistors but these currently have $g_m \approx 310\ uS$ and $r_o \approx 125\ k\Omega$. These are the characteristics we had in the previous labs. Since $R = 20\ k\Omega$ then it follows that:

$$A_{dm} = -310\ uS \cdot (125\ k\Omega \,||\, 20\ k\Omega) \approx 5.34$$

We can verify this by taking the derivative of either V_{ON} or V_{OP} when $V_{ID} = 0$. You can make two more plotting planes. Let the bottom plotting plane be the V_{GS} of both transistors. By KVL, that would be $V_{GS,M1} = V_{IP} - V_{TAIL}$ and $V_{GS,M2} = V_{IN} - V_{TAIL}$. Then on the upper plotting plane be the gains A_{dm}. Simply take the derivative of V_{ON} and V_{OP}. Take note that direction of change in V_{ON} and V_{OP} are opposite each other, so expect the gains to be negative of each other. If done correctly, you should get Figure 2.15.

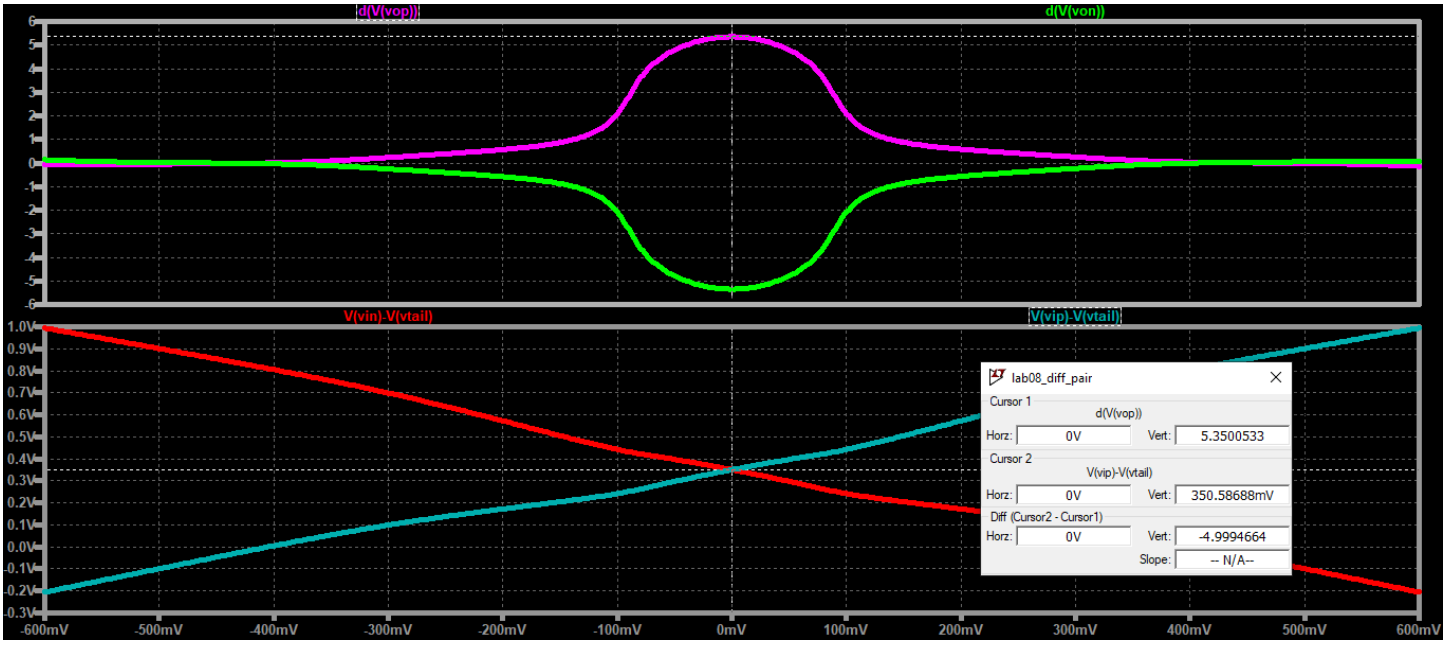

Figure 2.15 A_{dm} and V_{GS} with varying V_{ID}

It is clear that when $V_{ID} = 0$, $V_{GS} = 0.35\ V$ and the gain is consistent for both transistors. Remember, the sign just dictates the direction of change, if it's negative just like in the V_{ON} case, that means as $V_{GS,M1}$ increases, V_{ON} decreases at the rate of $A_{dm} \approx 5.35$. The same happens for V_{OP}. Great! Review these discussions to verify your understanding of the differential mode. Again, differential mode describes how the outputs change whenever there is a V_{ID} change. As a final note, we usually call the *differential output* V_{OD} as the difference between the output nodes. That is:

$$V_{OD} = V_{OP} - V_{ON}$$

C. Differential Pair Basics: The Common Mode

The common mode is easier to analyze because it focuses on what happens when V_{IC} changes while $V_{ID} = 0$. Consider Figure 2.16 which visualizes what happens when V_{IC} increases. The most intuitive trick is to remember that the I_{TAIL} imposes equal currents on the two transistors. This is true due to the KCL at the tail node: $I_{TAIL} =$

$I_{DS,M1} + I_{DS,M2}$. Moreover, we mentioned earlier that when $V_{ID} = 0$, then $I_{DS,M1} = I_{DS,M2}$ leading to $V_{ON} = V_{OP}$ by KVL.

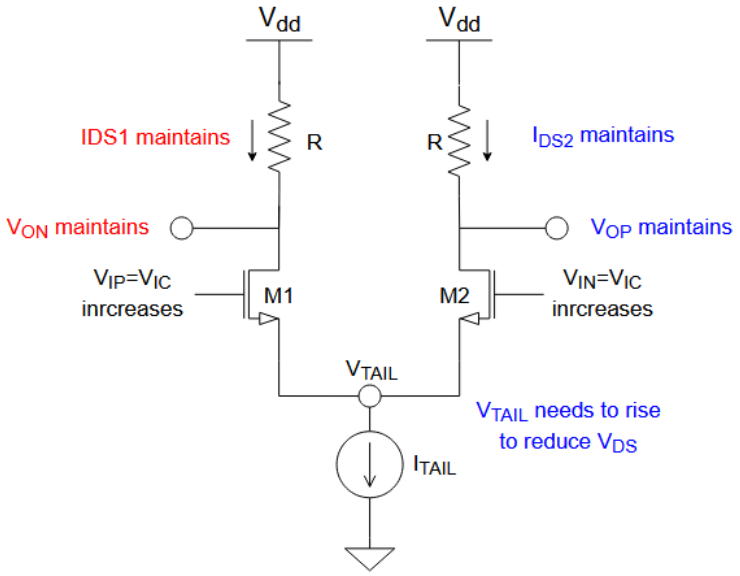

Figure 2.16 Visualization of what happens to the differential pair with increasing V_{IC}

Consider the sequence of events:

- When V_{IC} increases, $V_{GS,M1} = V_{GS,M2}$ increases.
- $I_{DS,M1} = I_{DS,M2}$ needs to increase due to increasing V_{GS}; however, it should not increase due to the I_{TAIL} imposing that $I_{DS,M1}$ and $I_{DS,M2}$ needs to be $\frac{I_{TAIL}}{2}$ because $V_{ID} = 0$.
- Recall the current equation in saturation:

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS})$$

- If I_{DS} is fixed and V_{GS} increases, to maintain that I_{DS}, V_{DS} needs to decrease.
- Hence, V_{TAIL} increases to reduce the V_{DS} of both transistors in order to maintain I_{DS} as much as possible.
- Effectively, since $I_{DS,M1} = I_{DS,M2} = \frac{I_{TAIL}}{2}$ for the entire sweep while the transistor is still in saturation, then $V_{ON} = V_{OP}$ will not change at all!
- Make sure to review these steps as this is the very reason what happens when V_{IC} changes: *it's the V_{TAIL} that absorbs the change in V_{IC} while all the rest try to remain the same.*

Let's verify this through simulations. Do the following:

1. Use the same schematic "lab08_diff_pair.asc".
2. Make sure the DC value of $V_{ID} = 0$.
3. Change the sweep to vary V_{IC} from 0.3 V to 0.5 V only. This range is purposely chosen so we won't get out of saturation.
4. Create 3 plotting planes that show the V_{TAIL} node on the top, The transistor (or resistor) currents in the middle, and, V_{ON} and V_{OP} at the bottom.
5. You should get Figure 2.17.

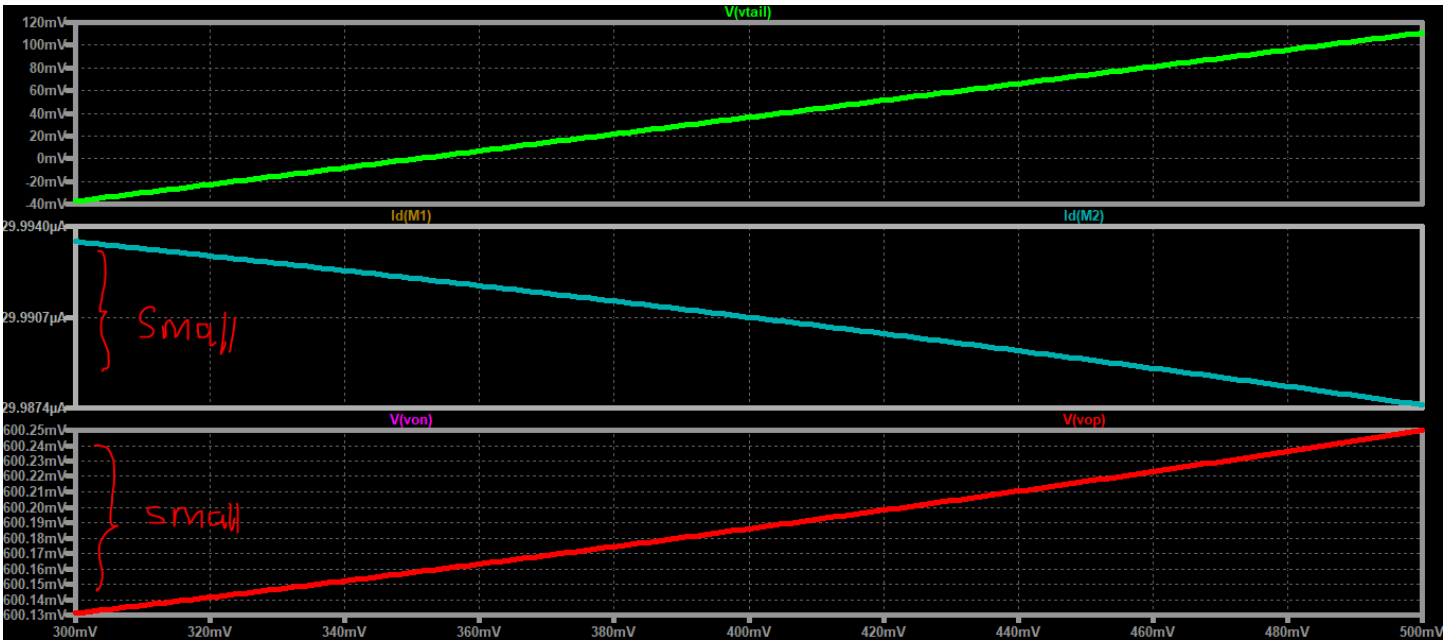

Figure 2.17 Common-mode simulation showing V_{TAIL}, the currents in each branch, and $V_{ON} = V_{OP}$.

At a glance the result is consistent with our intuitive analysis. First, when V_{IC} increase, V_{TAIL} increases as well indicating that in order to maintain the currents imposed by the I_{TAIL}, the source increases to reduce V_{DS} and counter the increase in V_{GS}. Next, the currents and voltages show a linear trend but observe that the range shown is very small as if there is no change at all. This coincides with our large-signal analysis that the currents and output voltages are maintained. Simple! Now, we're interested in the change of V_{IC} over the change in V_{ON} or V_{OP}. This is called the *common mode gain* (A_{cm}).

To speed up the discussion, referring to Figure 2.14, A_{cm} is defined as $\frac{\partial V_O}{\partial V_{IC}}$. Using the half-circuit model, during common mode, the $2r_{tail}$ resistance must be maintained. Then, if you solve $\frac{v_{on}}{v_i}$ we would have:

$$A_{cm} \approx \frac{g_m R}{1 + g_m 2r_{tail}}$$

We'll let you guys deal with the derivation as it was also discussed in the lecture. Since we have an ideal current source I_{TAIL}, then we would have $r_{tail} = \infty$. If $r_{tail} = \infty$ then the entire $A_{cm} \approx 0$ indicating that *during common mode, the output does not change with respect to any changes at the input*. Simple right? In fact, if you try to take the derivative of V_{ON} or V_{OP} you should get Figure 2.18.

The curve looks funny but don't be alarmed, because this is due to the simulator's calculations. What matters though is that the range is in the micro-range which is really close to $A_{cm} \approx 0$. This is consistent with our analysis.

In summary, the common mode rejects the changes at the input and hence the output does not change so much. This occurs due to the I_{TAIL} current that imposes the need for the two transistors to have the same currents when $V_{ID} = 0$. Again, whenever V_{IC} changes, those changes are absorbed by the V_{TAIL} node because the V_{DS} of the transistors needs to compensate the changes in the V_{GS} due to changing V_{IC}. This is probably the most intuitive interpretation of the common mode of the differential amplifier.

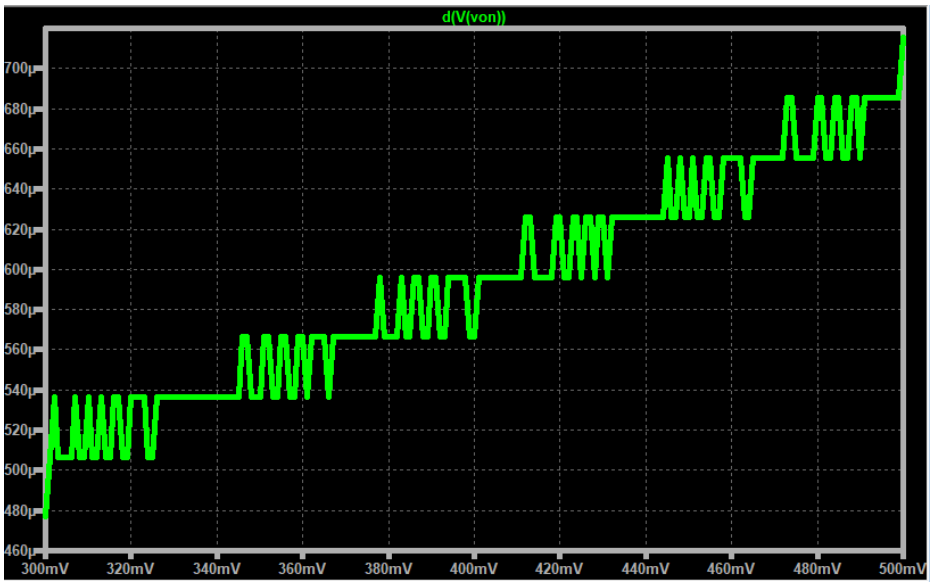

Figure 2.18 A_{cm} with varying V_{IC}

As a final note, we have this metric called the *common mode rejection ratio* or CMRR. This is a combined metric of measuring how good our differential mode and common mode gain are. We measure it as:

$$CMRR = \frac{A_{dm}}{A_{cm}}$$

Ideally, we want $CMRR \approx \infty$. That also means we want $A_{dm} \approx \infty$ and $A_{cm} \approx 0$ to achieve this. Keep this in mind as you might encounter these metrics in the near future.

QUESTION (Q2.4):
Let's see if you're paying attention. Fill in the blanks, and refer to Figure 2.9. Assume $V_{ID} = 0$ and V_{IC} is free to move. Answer with increase, decrease, or no change.

1. When V_{IC} decreases, $V_{GS,M1}$ _____, and $V_{GS,M2}$ _____.
2. When V_{IC} decreases, $I_{DS,M1}$_____, and $I_{DS,M2}$ _____.
3. When V_{IC} decreases, V_{ON} _____, and V_{OP} _____.
4. When V_{IC} decreases, V_{TAIL} _____.

QUESTION (Q2.5):
What's the CMRR assuming $A_{dm} \approx 5$ and $A_{cm} \approx 600u$?

Part III: Exercise

A. Miller Operational Amplifier

Figure 3.1 is a simple Miller Amplifier. Answer the following questions.

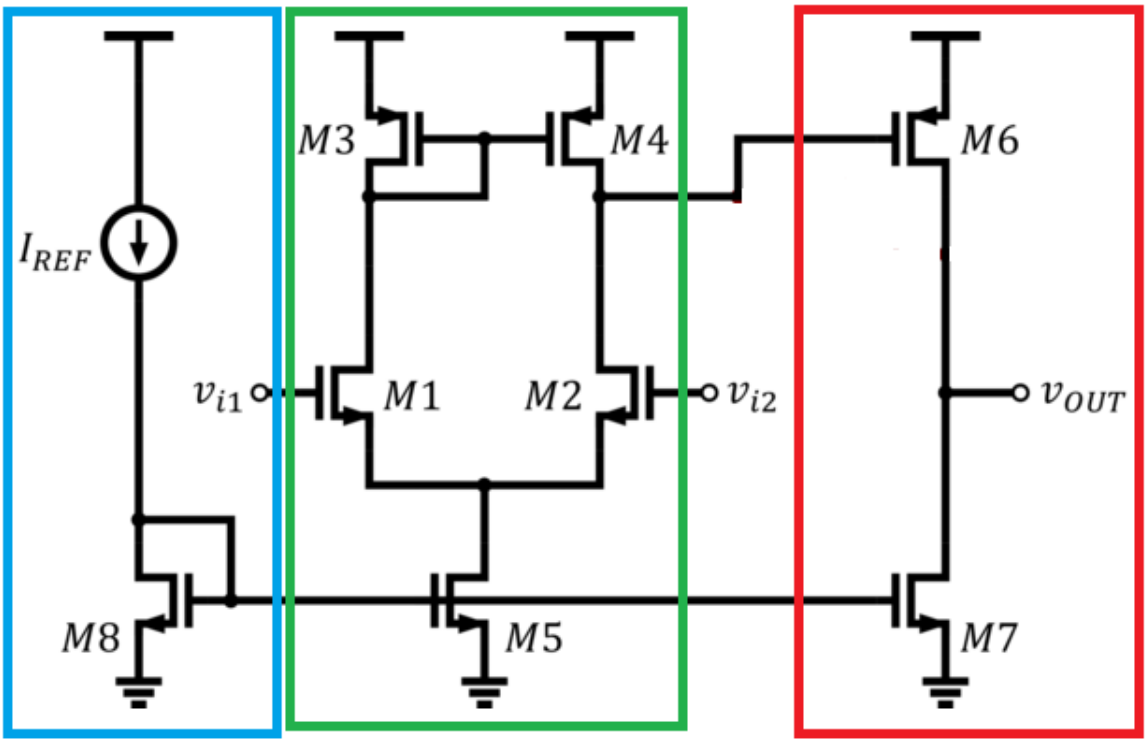

Figure 3.1 Simple Two-Stage Miller Amplifier

1. Describe what do the electrical elements in the blue section do?
2. What kind of circuit is in the green section?
3. What kind of circuit is in the red section?
4. In relation to #2, what is M5 for?
5. Do we want M5's output impedance to be higher or lower? Why?
6. List at least 2 ways to increase the output impedance of M5.
7. What does M3 and M4 do?
8. What does M6 and M7 do?
9. If you were to design this Miller Amplifier, who would you tackle first, the red, green, or blue section? Elaborate your answer.

B. Summarize!

In a maximum of 3 paragraphs, can you summarize what you have learned about analog design? Be sure to include things like:

- Design philosophies
- Trade-offs to watch out for
- Design methodologies
- Ideas you think that can improve your design strategies
- Add things that may not be included in the lab discussion but you may have discovered along the way

C. (BONUS) Finish Strong!

Sometimes it's great to not just finish a course, but to finish "strong"! Let's try to expand ourselves and do better than what was recommended in this course. With that, consider Figure 3.2 which shows complex amplifier. Then, answer the following questions.

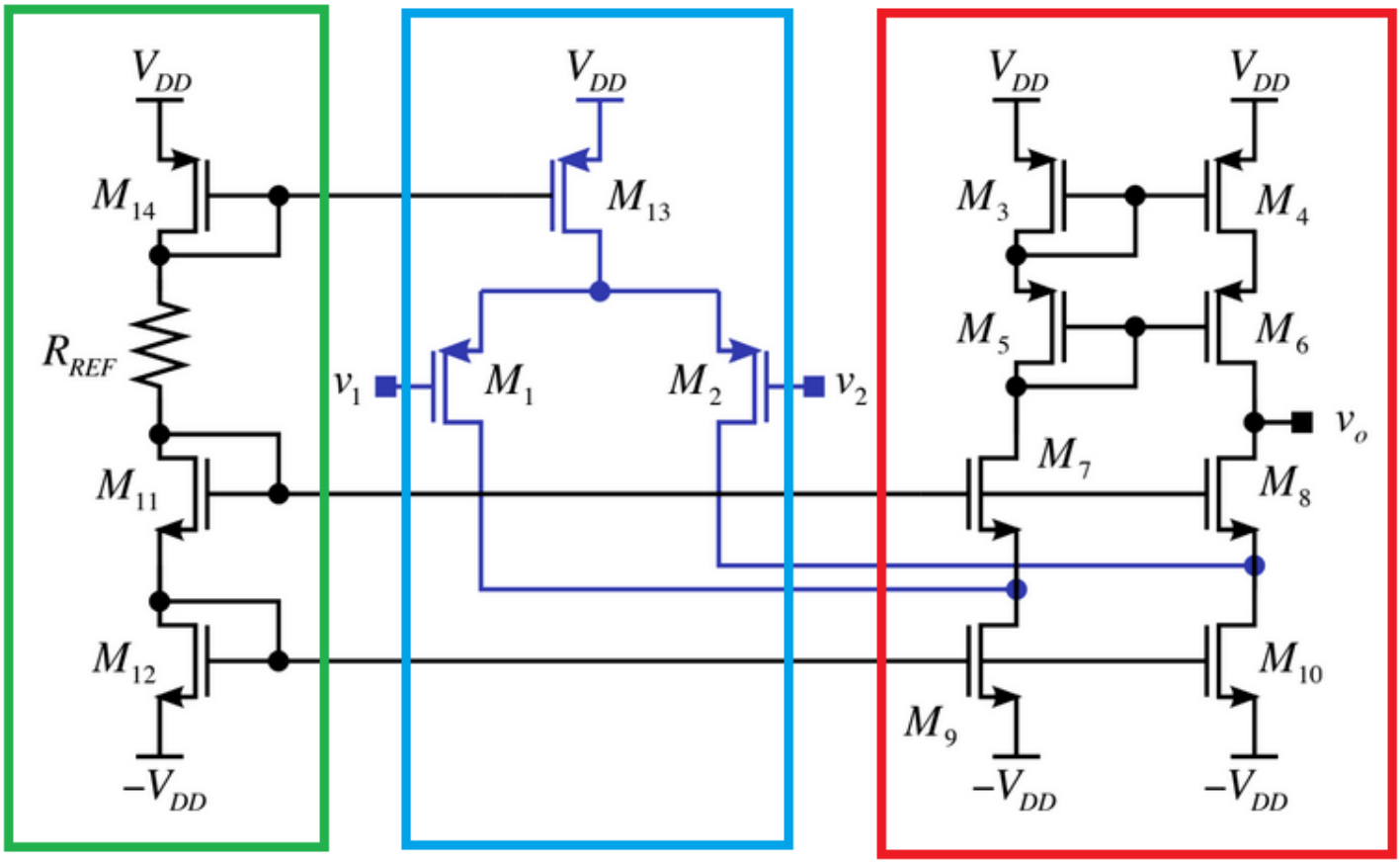

Figure 3.2 Super cool amplifier

1. What do you call this amplifier?

2. What circuit is the green section?
3. What circuit is the blue section?
4. What circuit is the red section?
5. This amplifier has very high gain. Why? Estimate to a first-order what that gain would be? (i.e. $A_v = ?$)

Part IV: Supplementary Reading / Exercises

Welcome to Microlab!

Congratulations! If you're reading this, you did a great job of sticking to this course until the end. We know it's been a difficult due to these trying times but you did great! Now that you're finished with this course, you are now officially a Microlab affiliate. We hope you learned a lot and had fun during this course. In your succeeding courses and possibly your capstone project course, you will face greater challenges and mind-boggling problems. The fundamentals taught to you are crucial to advancing your knowledge, critical thinking, and problem solving skills. With this, again, we'd like to congratulate you and welcome to Microlab 😊. Until we meet again!