University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 07 – Current Mirrors and AC Analysis

What will you learn from this lab?

- Current Mirrors Analysis
- AC Analysis and How to Simulate These

A few reminders for any lab:

Each lab will always be broken down in 3 main sections

- Prelab/Review – this section can be treated like a "pre-lab" where you need to recall some of the previous concepts in your earlier courses or those that were discussed in the lecture.
- Training – this section guides you through a skill that you must learn. This could be a method in using the tool or a concept that is new to you.
- Postlab/Exercises – are some problems that you need to solve. Sometimes you need LTspice for it, and some don't. It's there for you to test what you have learned.
- Supplementary reading – these is an optional content but for the interested students, you can read and answer some of its questions. It's to further help you appreciate what IC design is.

There will be special boxes that you need to watch out for.

BLUE BOXES: Are used for useful notes and discussions. They can help you understand and appreciate the current topic at hand.

RED BOXES: Are notes that you need to watch out for. Some of these may be warnings that pertain to some limitations of our simulator. Or possibly some warnings on how to use particular circuit models.

GREEN BOXES: Are questions for that particular training task. They are also in the answer sheet so they'll be hard to miss.

Part I: Review

1. Draw a rough sketch of the $I - V$ curves of a resistor, a current source, a non-ideal current source, and a transistor.

2. In simple terms, what does a current mirror do?

Part II: Training

A. Analysis of CS Amplifiers with Current Source Loads

This training is a continuation for developing an intuitive understanding of CS amplifiers. In Lab 06, our transistor is driving a resistive load. Figure 2.1 shows this setup again.

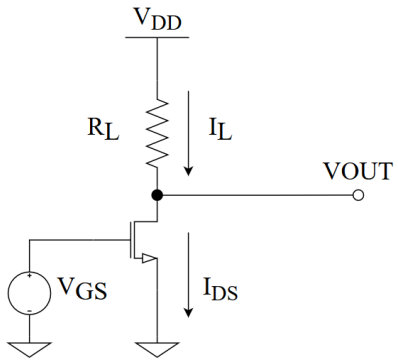

Figure 2.1 CS Amplifier with Resistive Load

Unfortunately, this method makes our transistor a very bad amplifier because the gain is limited by the resistance of the load such that:

$$A_v = -g_m \cdot (r_o || R_L)$$

We know that the maximum gain would be $g_m R_L$ if and only if $r_o \gg R_L$; however, this is difficult to achieve due to the limitations of our transistor. Instead of making r_o very large, why not change R_L to be larger so that the overall gain is higher. One effective method is to use a current source load as shown in Figure 2.2.

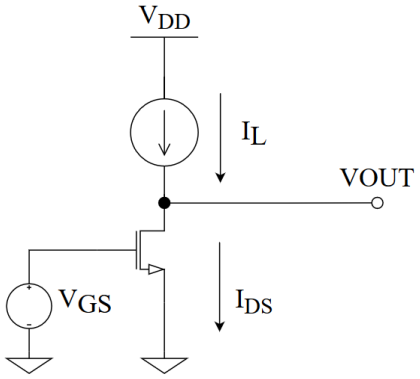

Figure 2.2 CS Amplifier with Current Source Load

An ideal current source can provide a constant current (say, I_L in our example) regardless of any voltage drop across the device. This means there is 0 change in current for any change in the voltage across the current source. This translates to infinite impedance because $\frac{\partial I}{\partial V} = 0 \rightarrow \frac{\partial V}{\partial I} = \infty$. We are interested in the small-signal gain A_v when the load resistance is "infinite". Consider Figure 2.3 which shows the small-signal model of Figure 2.2.

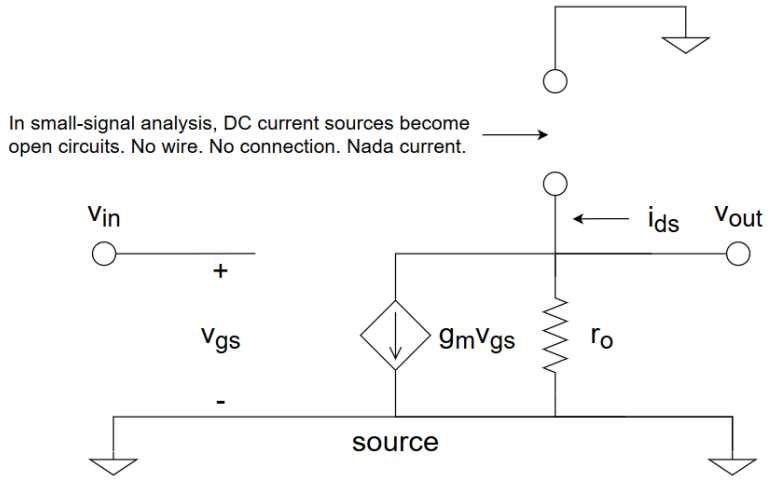

Figure 2.3 Small-signal Circuit Model for CS Amplifier with Current Source Load

Remember, in small-signal analysis, *DC voltage sources become short-circuits and DC current sources become open-circuits*. Looking at Figure 2.3, the small signal current i_{ds} produced by $g_m v_{gs}$ only drives the output impedance r_o of the transistor. i_{ds} driving r_o is not being shared with some other R_L load. In the end, the resulting small-signal would be the intrinsic gain $A_v = -g_m r_o$.

We can reproduce this result even in the DC perspective. Looking back at Figure 2.2, the critical KCL node says $I_{DS} = I_L$. The current equation for the NMOS transistor is:

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS})$$

If $I_{DS} = I_L$ and $V_{DS} = V_{OUT}$ (based on Figure 2.2) then we can write:

$$I_L = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{OUT})$$

If I_L is fixed, and all other device parameters except for V_{GS} is fixed (i.e. W, L, μ_n, C_{ox}, and V_{TH}), then as we increase V_{GS}, V_{OUT} needs to decrease in order to maintain the fixed I_L. If we decrease V_{GS}, then V_{OUT} has to increase in order to maintain I_L. This trend is similar to the CS amplifier with a resistive load such that $V_{OUT} = V_{DD} - I_{DS} R_L$. Re-arranging the above equation to solve for V_{OUT} in terms of I_L results in:

$$V_{OUT} = \frac{I_L}{\left(\frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2\right) \cdot \lambda} - \frac{1}{\lambda}$$

Taking the derivative of V_{OUT} with respective to V_{GS} gives us our voltage gain:

$$A_v = \frac{\partial V_{OUT}}{\partial V_{GS}} = -\frac{2 I_L}{V_{GS} - V_{TH}} \cdot \frac{1}{\lambda \cdot \left(\frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2\right)}$$

We'll leave it up to you to verify this. The two terms should look familiar. You should recall that:

$$g_m = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

$$r_o = \frac{1}{\lambda I_{DS}}$$

If $I_{DS} = I_L$ and let's assume that channel length modulation is negligible, then the gain results in:

$$A_v = -g_m \cdot r_o$$

Fantastic! It's consistent with the small-signal model! Bottomline, current source loads give better gain.

In reality, it is difficult to produce ideal current sources. Non-ideal current sources have very high output impedances but not infinite. T*he closest device to a good non-ideal current source is a transistor operating in saturation*. Consider 2.4 that shows the I-V curves comparing a non-ideal current source and a transistor.

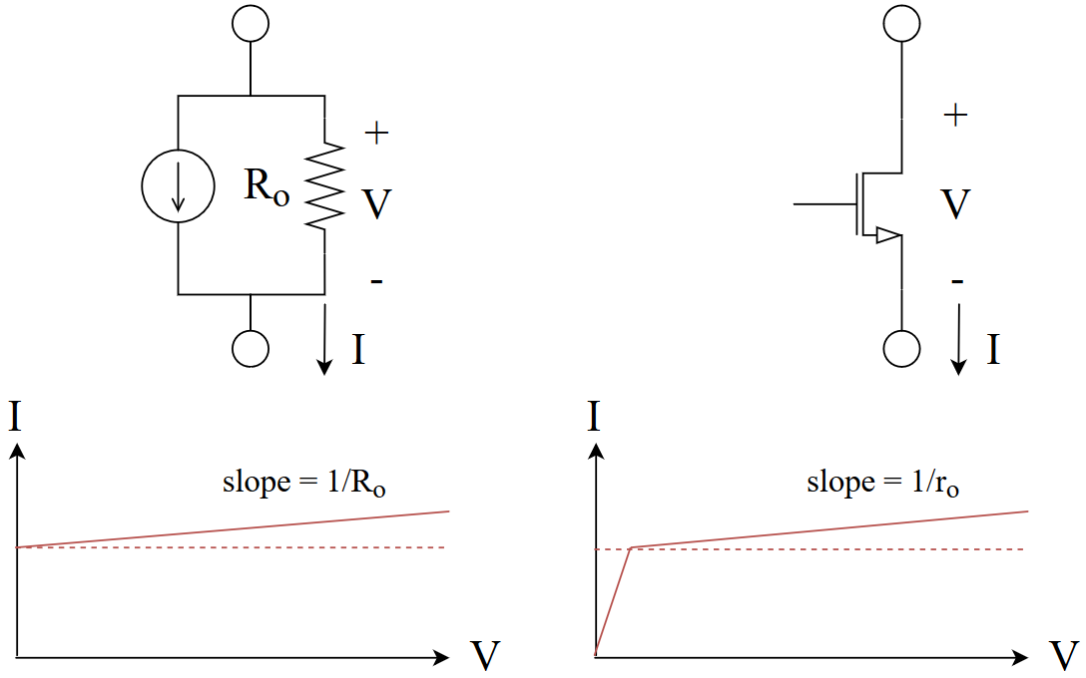

Figure 2.4 Left – non-ideal current source; Right - transistor

The dotted lines in Figure 2.4 represents the trend for an ideal current source. The left side of Figure 2.4 shows how we represent a non-ideal current source. The impedance R_O of a non-ideal current source is high and therefore, the change in current with respect to voltage is small (i.e. $\frac{\partial I}{\partial V} \rightarrow 0$). The right side of Figure 2.4 shows that the saturation region of a transistor is close to a good current source. We know that this slope is $\frac{1}{r_o}$ and as $r_o \rightarrow \infty$ we get closer to an ideal current source. *Therefore, we can use a transistor as a current source load, provided it stays in saturation*. Figure 2.2 can be modified into Figure 2.5 where the PMOS transistor acts as the current source.

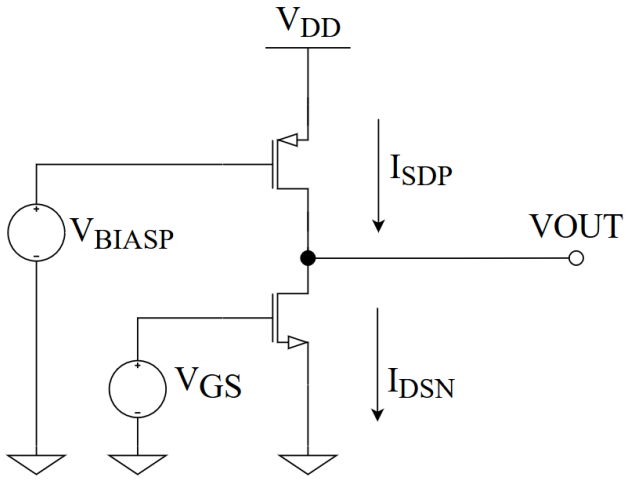

Figure 2.5 CS Amplifier with PMOS as a Current Source Load

The PMOS transistor is sized and biased such that its current matches the NMOS current the desired r_o. Most of the time PMOS transistors are "better" current sources due to its high impedance.

There are a few pointers to consider regarding Figure 2.6:

- We'll subscript n and p to indicate if it belongs to the NMOS or PMOS, respectively. For example, g_{mn} and g_{mp} pertain to the transconductances of the NMOS and PMOS, respectively.
- The polarity of voltages for the NMOS and PMOS are inverted. Whenever we say V_{GS} or V_{DS} we know this is for the NMOS, and if we say V_{SG} or V_{SD} then we pertain to the PMOS.
- The PMOS is not an amplifier. It's a "current source". This means we won't apply some small-signal input v_{in} into the gate of the PMOS. We'll only bias it such that it gives the desired current that we need.

Let's analyze the small-signal gain through the small-signal model shown in Figure 2.6.

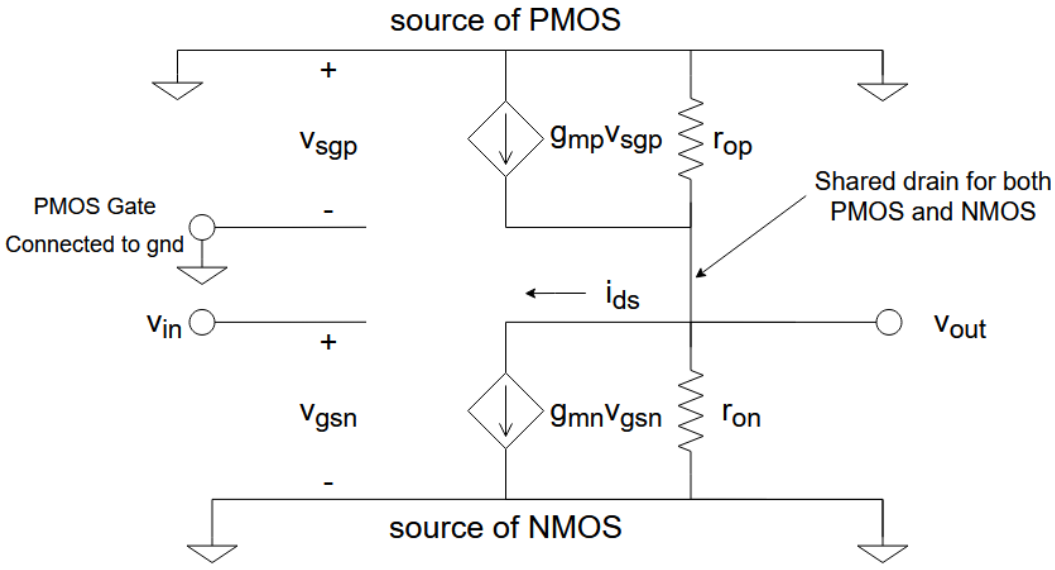

Figure 2.6 Elaborated Small-signal Model of Figure 2.6

Figure 2.6 can be easily broken down into the PMOS and NMOS components. The NMOS side is still the same as CS amplifier. On the other hand, the gate of the PMOS is connected to a DC voltage source. This means, the

DC voltage source will appear as a short circuit connected directly to ground. Since both the gate and the source of the PMOS are connected to ground, then $v_{sgp} = 0$ and $g_{mp} \cdot v_{sgp} = 0$. Hence, the small-signal current produced by g_{mp} disappears. This is consistent with the fact that DC current sources should be open circuits with respect to the small-signal perspective. However, the r_{op} should still exist and it is in parallel with r_{on}. We can simplify Figure 2.6 to Figure 2.7.

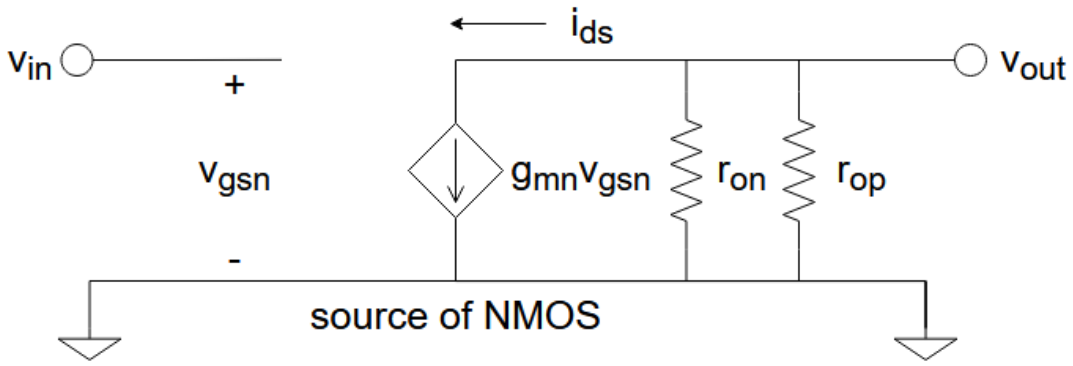

Figure 2.7 Simplification of Figure 2.7

At a glance, the r_{op} somehow looks like the same R_L when our CS amplifier is connected to a resistive load. Taking the KCL at the output node:

$$-i_{ds} = -g_{mn} \cdot v_{gsn} = \left(\frac{1}{r_{on}}\right) v_{out} + \left(\frac{1}{r_{op}}\right) v_{out}$$

Intuitively, the equation tells us is that our output current $i_{ds} = g_{mn} \cdot v_{gsn}$. i_{ds} is being distributed between r_{on} and r_{op} and the output voltage $v_{out} = -i_{ds} \cdot (r_{on} || r_{op})$. Computing for the gain results in:

$$A_v = -g_{mn} \cdot (r_{on} || r_{op})$$

One intuitive way of understanding why r_{op} shares the current produced by $g_{mn} v_{gs}$ with r_{on} is because the V_{SD} of the PMOS also affects the output current $I_{DSN} = I_{SDP}$ (i.e. recall the current equation of the PMOS). In Figure 2.5, the drain node (V_{OUT}) is common for both the PMOS and NMOS. Whenever the drain node changes, the effective current going through the PMOS and NMOS changes as well and since $I_{DSN} = I_{DSP}$. Essentially, the current changes are shared between the two transistors. Take time to internalize this concept.

QUESTION (Q2.1):
Briefly explain why a current source load is better than a resistive load.

QUESTION (Q2.2):
When is the transistor "acting" like a good current source?

QUESTION (Q2.3):
How would we size a transistor such that it becomes a better current source?

B. Simulating A CS Amplifier with Current Source Load

Let's simulate a given setup first then work backwards for designing CS amplifiers with current source loads. Figure 2.8 shows the schematic that we will use later. The PMOS is sized such that $W = 30\ um$ and $L = 1\ um$ while the NMOS is sized such that $W = 10\ um$ and $L = 1\ um$. We'll extract the small-signal parameters at the given bias, then we'll try to compute the effective gain and prove it by a V_{OUT} vs V_{IN} simulation. Take note that in the succeeding steps, we are expecting you know how to extract g_m and r_o already.

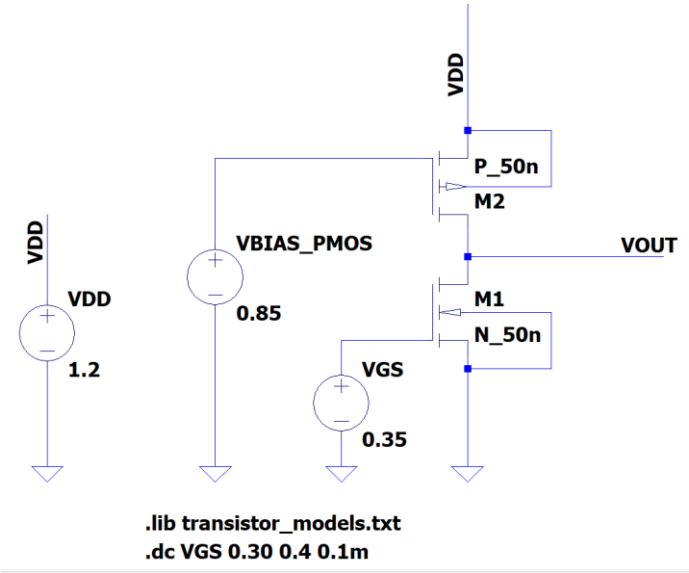

Figure 2.8 CS Amplifier with a PMOS as Current Source Load

In the previous discussion, only the output impedance r_{op} matters from the PMOS. We can extract the output impedance of the PMOS by plotting its I_{SD} vs V_{SG} curve. Do the following.

1. Go ahead and open "lab07_pmos_char.asc".
2. Make sure the PMOS has $W = 30\ um$ and $L = 1\ um$.
3. Set $V_{SG} = 0.35\ V$. Note: $V_{SG} = V_{DD} - V_{BIAS,PMOS} = 1.2 - 0.85 = 0.35\ V$. Then sweep V_{SD} from 0 to 1.2 V.
4. Plot and take note of the current I_{SD} at $V_{SD} = 0.6\ V$. You should get $I_{SD} \approx 28.66\ uA$.
5. Plot and take the output impedance when $V_{SD} = 0.6\ V$. You should get $r_o \approx 320\ k\Omega$

That's it for the PMOS device. Simple right? We do not need to get g_{mp} anymore because it does not contribute to the gain. There is no change happening at the input of the PMOS; therefore, there is no change in output current that is caused by V_{SG}. We can now proceed to extract the g_{mn} and r_{on} of the NMOS device.

1. Go ahead and open "lab07_nmos_char.asc".
2. Make sure the NMOS has $W = 10\ um$ and $L = 1\ um$.
2. Set $V_{GS} = 0.35\ V$ and sweep V_{DS} from 0 V to 1.2 V.
3. Plot and take the current and output impedance when $V_{DS} = 0.6\ V$.
4. If done correctly, you should get $I_{DS} \approx 29.74\ uA$ and $r_{on} \approx 125\ k\Omega$.
5. Extract g_{mn} by fixing $V_{DS} = 0.6\ V$ and sweep V_{GS} from 0 to 1.2 V.
6. Plot g_{mn} and get the reading when $V_{GS} = 0.35$. Get as close as possible and you should get $g_{mn} \approx 310\ uS$.

Viola! Now we gave $g_{mn} = 310\ uS$, $r_{on} = 125\ k\Omega$, and $r_{op} = 314\ k\Omega$. Using equation (12), we can solve for the small-signal gain as:

$$A_v = -g_{mn} \cdot \left(r_{op} || r_{on}\right) = -310\ uS \cdot (125\ k || 320\ k) \approx 27.87$$

Now, let's try to convince ourself that this works.

1. Go ahead an open "lab07_cs_amp.asc". This is the same schematic in Figure 2.8.
2. Observe the following:
   - The PMOS and NMOS are sized accordingly to how we characterized them.
   - The PMOS is biased with $V_{BIAS,PMOS} = 0.85\ V$. This sets $V_{SG} = 0.35\ V$
   - The NMOS is biased exactly at $V_{GS} = 0.35\ V$.
   - When you do your V_{GS} sweep, observe that the range is $0.30\ V \leq V_{GS} \leq 0.40\ V$. This is purposely chosen so that we can zoom into the region where the transition occurs. It's okay to sweep from 0 to 1.2 V, but getting closer to the transition gives us a better view. We are also using 0.1 mV steps.
3. Run the simulation and create two plotting planes. Let the top plane be A_v vs. V_{GS}. Let the bottom plane be the gain V_{OUT} vs. V_{GS}. You should get Figure 2.9 if done correctly.

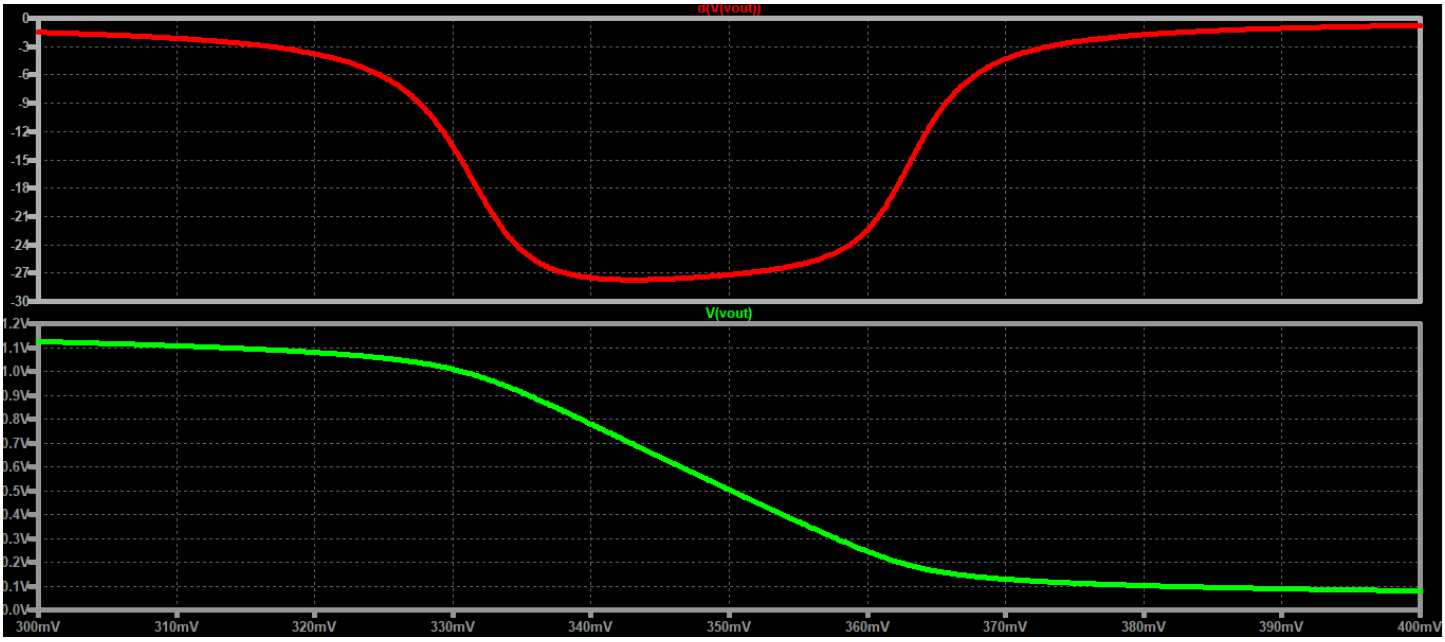

Figure 2.9 V_{OUT} and A_v versus V_{GS} or V_{IN}

Muy bien! Figure 2.9 shows the A_v vs V_{GS} plot. There are a few things to observe:

- At $V_{GS} = 0.35\ V$ we have $A_v = 27.16$ which is close to our computed gain.
- When $V_{GS} = 0.35\ V$, $V_{OUT} = 0.5\ V$ is far from the desired output. This is due to the NMOS and PMOS having unmatched currents and the *drain node needs to compensate until both could provide the same current*.
- In our characterization, we extracted the small-signal parameters of each transistor *separately*. We have completely disregarded the effects of when they share a single drain node.
- We often tweak the V_{GS} of the NMOS to fix the desired V_{OUT}. Sometimes we tweak the V_{SG} of the PMOS.
- When $V_{GS} \approx 0.346\ V$ then $V_{OUT} = 0.6\ V$ and $A_v \approx 27.59\ V$ which shows that we still have a good gain.
- Unlike the resistor load (with $A_v \approx 5$), the CS amplifier with a "current source" load is $5\times$ higher.
- The small-signal calculations are consistent with our simulations!

C. Design of CS Amplifier with Current Source Load

Designing a CS amplifier with a current source load follows a different methodology compared to a resistive load. The design process revolves around trying to find the right pieces that fit together. Before we begin, there are a few important considerations that we should think about:

- Mathematically these always hold true: $r_{on} > (r_{on}||r_{op})$ and $r_{op} > (r_{on}||r_{op})$, we'll leave the proving to you.
- Just like in the ideal current source, when $r_{op} \gg r_{on} \rightarrow (r_{on}||r_{op}) \approx r_{on}$. Let's define $(r_{on}||r_{op}) \approx r_{on}$ as the ideal maximum output impedance such that: $(r_{on}||r_{op}) \leq r_{on}$.
- Generally, we usually set $r_{op} \geq r_{on}$. It is natural for PMOS devices to have higher impedances, but r_{op} does not reach ∞. This way, we are sure that r_{op} is not the limiting impedance, but the r_{on} only.
- At the minimum, analog designers usually set $r_{op} = r_{on}$ and this leads to $(r_{on}||r_{op}) \approx \frac{r_{on}}{2} = \frac{r_{op}}{2}$.
- The information above tells us that we can pick r_{op} in the range of $r_{on} \leq r_{op} \leq \infty$ such that this gives us an effective output impedance range of $\frac{r_{on}}{2} \leq (r_{on}||r_{op}) \leq r_{on}$.

The choice of r_{op} in the range of $r_{on} \leq r_{op} \leq \infty$ is still quite broad. We can further funnel our choices by characterizing the effective output impedance for different lengths and widths. Recall that:

$$r_o = \frac{1}{\lambda I_D}$$

We know that $I_D \propto \frac{W}{L}$ and $\lambda \propto \frac{1}{L}$. This leads us to $r_o \propto \frac{L^2}{W}$. We need to characterize our circuit such that we can determine the range r_{op} that our PMOS can handle. One nice strategy is to isolate the effects of increasing r_{op} with respect to L only. We'll do this by scaling both the width and length at the same time and let the increase in output impedance be solely controlled by λ. Do the following:

1. Open "lab07_pmos_char.asc" schematic. This is the schematic for extracting PMOS small-signal parameters.
2. The schematic already has V_{SD} swept from 0V to 1.2 V. We'll be extracting r_{op}. Make sure $V_{SG} = 0.35\ V$.
3. Make sure to set the widths and lengths such that $W = L = \{500n * k\}$.
4. Add ".step param k 1 10 1" SPICE directive so that we can parametrize the increase in transistor size.
5. Plot the output impedance and you should get Figure 2.10.

Great! Figure 2.10 shows how the output impedance changes with increasing transistor size. If you plot the current for this device, they should be relatively the same. With a $\frac{W}{L} = 1$ ratio, the increase in output impedance is primarily due to the increase in length affecting the channel length modulation λ. We can consider these curves as our starting point. We can treat it as the "maximum" for that given transistor size with $\frac{W}{L} = 1$. The reason why it's a maximum is because whenever we need higher current, we need to increase W for that fixed length, and r_{op} decreases linearly. We'll see this in action in a bit. Again, the purpose of this initial characterization is to get a base point of how much r_{op} can we have for an initial transistor size.

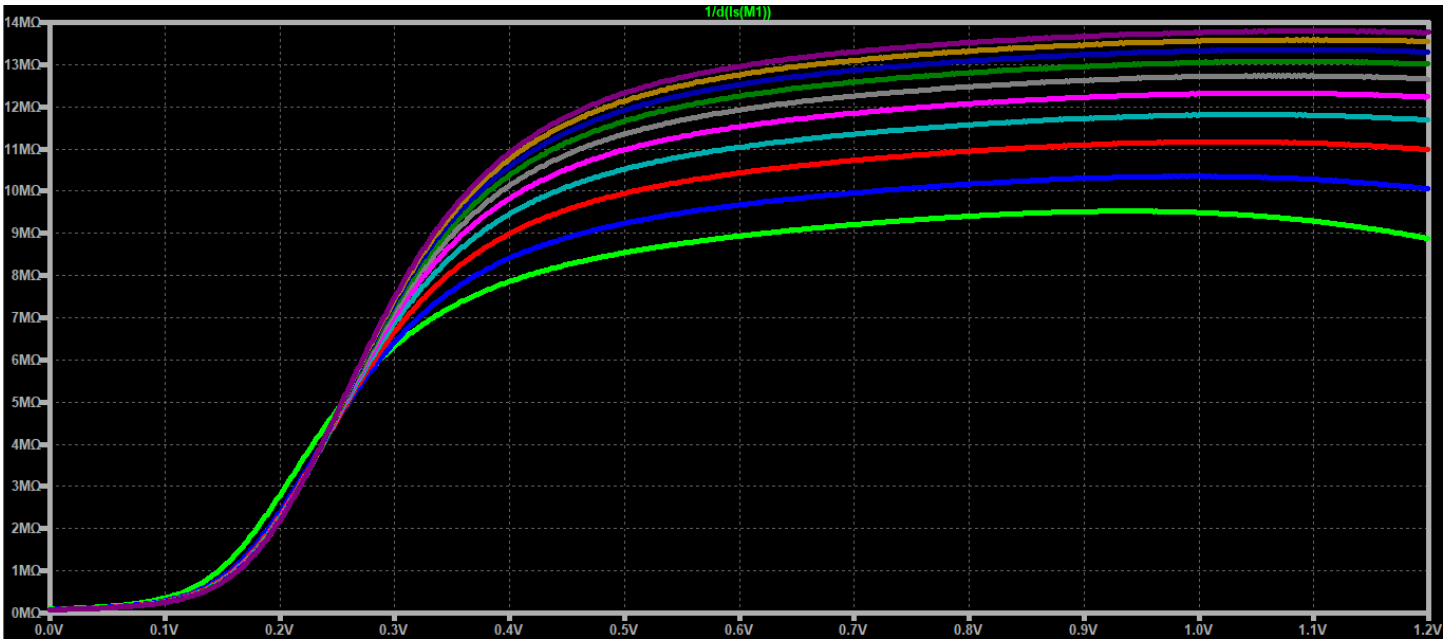

Figure 2.10 r_{op} vs V_{DS} while parametrizing W and L

The steps from the previous lab won't work for this setup anymore because now we have too much "freedom" of the choice for the transistor load. For now, consider the following specs which we will use:

- It needs to drive a transistor load as a current source
- The gain must be $A_V \geq 30$
- The speed of your amplifier must be $g_{mn,} \geq 500\ uS$
- For simplicity, let's choose $V_{GSN} = 0.35\ V$, $V_{SGP} = 0.35\ V$, and $V_{OUT} = 0.6\ V$
- Start with $W = 500\ nm$ and $L = 500\ nm$ and use multiples of $100\ nm$ for widths and $500\ nm$ for lengths.

1. *Calculate the r_{op} and r_{on} that gives the minimum $(r_{on}||r_{op})$.*

Since we are given $A_v \geq 30$ and $g_{mn} \geq 500\ uS$, we can easily calculate $r_{on}||r_{op}$:

$$A_v = g_{mn}(r_{on}||r_{op}) \rightarrow (r_{on}||r_{op}) = \frac{A_v}{g_{mn}}$$
$$(r_{on}||r_{op}) = 60k\Omega$$

From the previous discussion, we know that we have $\frac{r_{on}}{2} \leq r_{on}||r_{op} \leq r_{on}$ and the minimum $r_{on}||r_{op} = \frac{r_{on}}{2}$ happens when $r_{on} = r_{op}$. Let's start with $r_{op} = r_{on}$ since it's the minimum. This means:

$$(r_{on}||r_{op}) = \frac{r_{on}}{2} = 60k\Omega \rightarrow r_{on} \geq 120k\Omega$$

2. *Determine the L_N that gives the minimum $g_{mn}r_{on}$.*
   - *In the event that we can't reach the minimum $g_{mn}r_{on}$ due to device limitations of the NMOS transistor, we need to first pick a reasonable NMOS size then we need to re-calculate the desired r_{op} for the chosen $g_{mn}r_{on}$.*

Since we know $g_{mn} \geq 500\ uS$ and $r_{on} \geq 120\ k\Omega$ then:

$$g_{mn}r_{on} \geq 60$$

Similar to the previous lab, we can use "lab07_gmro_extract.asc" to see if our NMOS transistor can support the needed minimum gain. Do the following:

- Go ahead and open "lab07_gmro_extract.asc".
- Remember, $g_m r_o$ *is independent of* W so we just parametrize L from $500\ nm$ to $5\ um$ in $500\ nm$ steps. We'll do this just to speed up the process for scaling.
- Go ahead and run the simulation then plot $g_m r_o$ from the SPICE error log. You should get Figure 2.11.
- Scan through the $g_m r_o$ when $V_{GS} = 0.35\ V$.

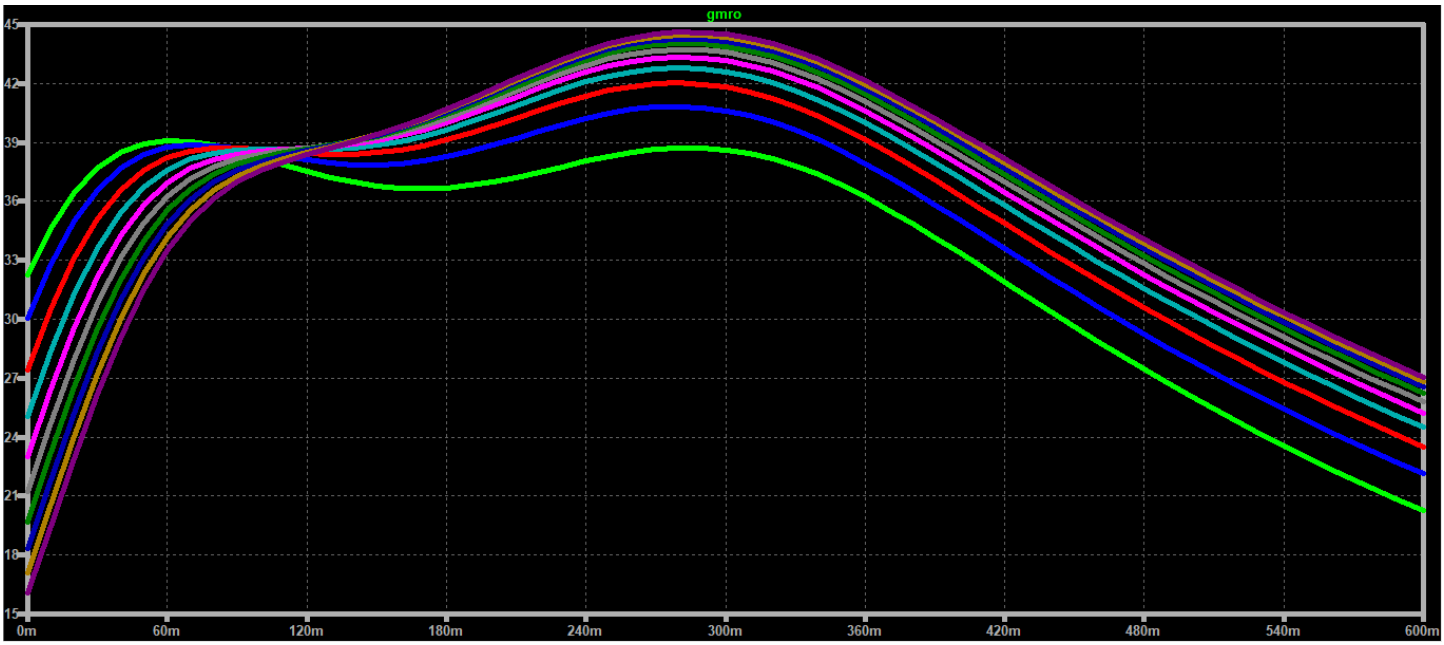

Figure 2.11 $g_m r_o$ sweep with parametrizing L

Even at $L = 5\ um$ we are still short of the minimum gain that we need ($g_{mn}r_{on} \approx 42.70$). In fact, as we increase the lengths further, the $g_{mn}r_{on}$ starts to saturate toward $g_m r_o = 44$. This imposes a limitation to our device. Choosing longer lengths is detrimental as we'll end up having to size a larger width that needs to support the required g_{mn} later. Typically, *we choose* $500\ nm \leq L \leq 10\ um$ *only*. The reason behind this is that it isn't worth increasing the length further as we have diminishing returns for increasing $g_{mn}r_{on}$ and the consequence of a larger L necessitates we need a large W to support g_{mn}.

For the sake of simplicity and just as an example with having nice numbers, let's use $L_N = 2\ um$ which gives $g_{mn}r_{on} \approx 40.5$. If we know $g_{mn}r_{on}$ then we may compute the desired r_{op} based on $A_v = g_{mn}(r_{on}||r_{op})$.

$$A_v = g_{mn}(r_{on}||r_{op}) = \frac{1}{\frac{1}{g_{mn}r_{on}} + \frac{1}{g_{mn}r_{op}}}$$

$$r_{op} \geq \frac{1}{g_{mn} \cdot \left(\frac{1}{A_v} - \frac{1}{g_{mn} r_{on}}\right)} = \frac{1}{500\ uS \cdot \left(\frac{1}{25} - \frac{1}{40.5}\right)} = 231.428\ \Omega \approx 230\ k\Omega$$

Therefore, at the minimum $r_{op} \geq 230\ k\Omega$. We'll use $230\ k\Omega$ for nice numbers.

3. Using the chosen L_N in step 3, size W_N such that we get the minimum g_{mn}. Also, determine the operating I_{DN}.

We need $g_{mn} \geq 500\ uS$. Similar to the previous lab's step, we can use "lab07_nmos_char.asc" to determine the width that we need. Remember, we scale W_N to get the g_{mn} that we need. Do the following:

- Go ahead and open "lab07_nmos_char.asc"
- Using $L = 2\ um$ and $W = 500\ nm$ as a starting point, extract g_{mn} when $V_{GS} = 0.35\ V$.
- You should get $g_m \approx 7.98\ u$.
- Calculate the scaling multiplier to get a minimum of $500\ uS$:

$$k_{multiplier} = \frac{g_{mn,target}}{g_{mn,have}} = \frac{500\ uS}{7.98\ uS} \approx 62.66$$

- Therefore, the new W_N is:

$$W_{N,new} = 500\ nm * k_{multiplier} = 500\ nm * 62.66 \approx 31.3\ um$$

- Verify if the new size gives the minimum g_{mn} that we need.
- Plugging in $W = 31.3\ um$ with $L = 2\ um$ results in $g_{mn} \approx 508\ uS$.
- For this size and at the given bias, we also have $I_{DN} \approx 50.92\ uA$.

4. Size the PMOS such that we get the desired r_{op} and I_{DP}.

It is important that I_{DP} needs to be as close as possible to the operating I_{DN} of the NMOS. Any mismatch will move V_{OUT}. Previously, we discussed that a PMOS where $\frac{W}{L} = 1$ is our "starting point" for choosing the size. Moreover, analog designers often start with the PMOS having the same length of the NMOS. Then they just reduce the size only when there is an area constraint. Naturally, we expect it to have higher base impedance. Do the following:

- Use "lab07_pmos_char.asc" to characterize r_{op} and I_{DP}.
- Get the r_{op} and I_{DP} when $V_{SGP} = 0.35\ V$ and $V_{SD} = 0.6\ V$ with $W = L = 2\ um$.
- You should get $r_{op} \approx 11\ M\Omega$ and $I_{DP} \approx 1\ uA$.
- We need scale the width to get $I_{DP} = 50.92\ uA$ as close as possible. That means we scale by:

$$k_{multiplier} = \frac{50.92\ uA}{1\ uA} \approx 50.92 \approx 51$$

- Increasing W decreases r_{op} roughly by the same factor. Therefore, we would expect $r_{op,new} = \frac{r_{op,have}}{k_{multiplier}} = \frac{11\ M\Omega}{51} \approx 216 k\Omega$. This is below our requirement of $r_{op} \geq 220\ k\Omega$. We're not happy with this.

- Because of the lack of output impedance, we can choose the next higher length for the PMOS.
- Just to speed up the process of discussion let's say we'll use $W_P = L_P = 3\ um$.
- At this size we can get $I_{DP} \approx 1\ uA$ and $r_{op} \approx 12\ M\Omega$.
- Recomputing $k_{multiplier}$ again results in $k_{multiplier} \approx 51$ and $r_{op,new} \approx 235\ k\Omega$. We're happy with this!
- This results in $W_{new} = 3\ um * k_{multiplier} = 153\ um$ and $L = 3\ um$.
- Verify if the PMOS characteristics using the new size. You should get $I_D \approx 52.45\ uA$ and $r_{op} \approx 235k\Omega$.

5. Verify your design!

Great! We now have the pieces that we need. First, let's calculate the expected result. Using:

$$A_v = g_m(r_{on}||r_{op}) = \frac{1}{\frac{1}{g_m r_{on}} + \frac{1}{g_m r_{op}}}$$

While we know that $g_{mn} \approx 508\ uS$, $g_m r_{on} \approx 40.5$, $r_{op} \approx 235\ k\Omega$ then we have:

$$A_v = g_m(r_{on}||r_{op}) = \frac{1}{\frac{1}{40.5} + \frac{1}{(508\ uS)\cdot(235k\Omega)}} \approx 30.24$$

If you get different results, they're most likely have different due to the rounding. Anything close to $A_v = 30$ should be fine. Let's verify the actual results. For the NMOS we have $W_N = 31.3\ um$ and $L_N = 2\ um$ while the PMOS has $W = 153\ um$ and $L = 3\ um$. Plug these into "lab07_cs_amp.asc" and make sure the biasing is correct. $V_{GSN} = 0.35\ V$ and $V_{SGP} = 0.35 \rightarrow V_{GP} = 0.85\ V$ with respect to ground. Plot A_v and V_{OUT} and you should get Figure 2.12.

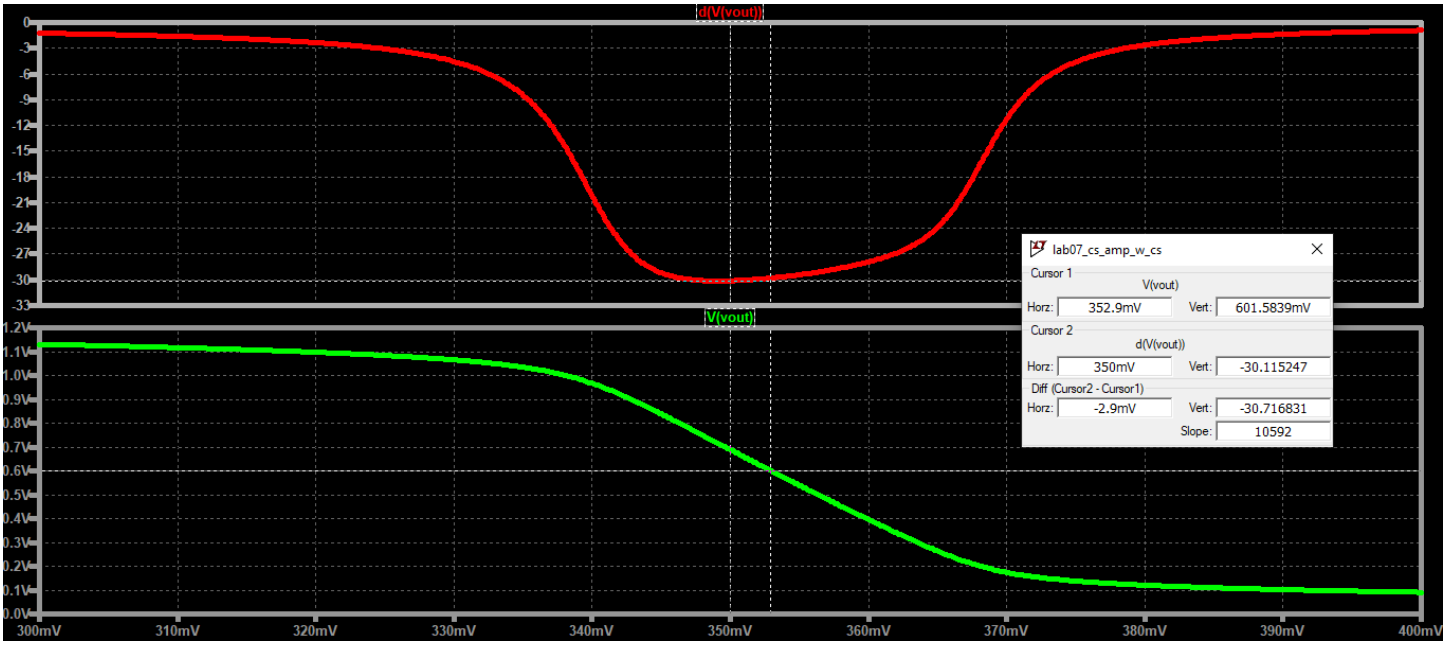

Figure 2.12 A_v and V_{OUT} vs V_{GS} with the newly design amplifier

When $V_{GSN} = 0.35\ V$ we have $A_v \approx 30.11$ which is close to our computed gain and the required gain. Fantastic! However, $V_{OUT} = 0.6$ only when $V_{GS} = 0.353\ V$. This is okay since we're really close and in reality, it's difficult to control V_{GSN}. Remember, this occurs because of the current mismatch and it's either we need to tweak V_{GSN} or V_{SGP} a little bit to get the exact $V_{OUT} = 0.6\ V$.

In summary we have the following steps:

1. *Calculate the r_{op} and r_{on} that gives the minimum $(r_{on}||r_{op})$.*
2. *Determine the L_N that gives the minimum $g_{mn}r_{on}$.*
   - *In the event that we can't reach the minimum $g_{mn}r_{on}$ due to device limitations of the NMOS transistor, we need to re-calculate the desired r_{op} for the chosen $g_{mn}r_{on}$.*
3. *Using the chosen L_N in step 3, size W_N such that we get the minimum g_{mn}. Also, determine the operating I_{DN}.*
4. *Size the PMOS such that we get the desired r_{op} and I_{DP}.*
5. *Verify your design!*

QUESTION (Q2.4):
Theoretically, we could just have sized the PMOS to get $r_{op} \gg r_{on}$ (does not need to be infinite, just really large) and not worry about what r_{op} should be. In reality, analog designers don't go too far from r_{op} being just a few magnitudes higher ($2\times - 5\times$). Why do you think this is so?

D. Current Mirrors

Current mirrors simply provide the desired current that our amplifiers need from a main current source. Hence, the term "current mirror". Let's briefly review the lecture. Consider Figure 2.13 which shows the schematic of a basic current mirror.

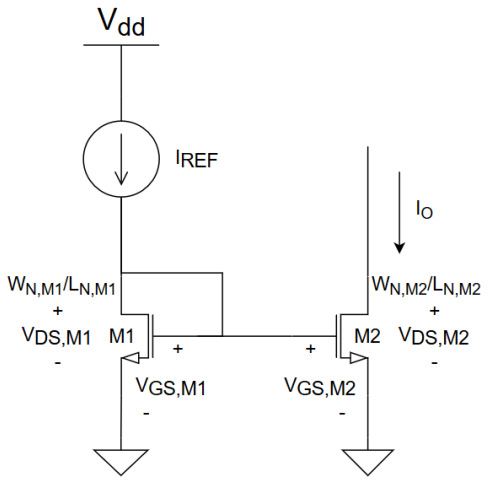

Figure 2.13 Basic Current Mirror

The entire discussion (and all the details to know) about current mirrors can be summarized as follows:

- There are two parts to a current mirror: (1) the biasing circuit and (2) the mirrored current source.
- The biasing circuit is usually a diode connected transistor (that's M1) connected to a main current source.
- The mirrored current source (that's M2) delivers the desired current to whoever needs it.
- This is possible because transistor M1 provides a V_{GS} that simply sets M2.

- By KVL, we have $V_{GS,M1} = V_{GS,M2}$.
- Assuming channel length modulation is negligible and both transistors are identical (i.e. same size, V_{TH} and all other parameters), then we have the following current equations:

$$I_{REF} = I_{DS,M1} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W_{N,M1}}{L_{N,M1}} \cdot \left(V_{GS,M1} - V_{TH}\right)^2$$
$$I_O = I_{DS,M2} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W_{N,M2}}{L_{N,M2}} \cdot \left(V_{GS,M2} - V_{TH}\right)^2$$

- We can transform the above equations to get:

$$V_{GS,M1} = \sqrt{\frac{I_{REF}}{\frac{\mu_n C_{ox}}{2} \cdot \frac{W_{N,M1}}{L_{N,M1}}}} + V_{TH}$$
$$V_{GS,M2} = \sqrt{\frac{I_O}{\frac{\mu_n C_{ox}}{2} \cdot \frac{W_{N,M2}}{L_{N,M2}}}} + V_{TH}$$

- Observe that the first equation tells us that $V_{GS,M1}$ is controlled by the I_{REF}, W, L, and the device parameters. Only I_{REF}, $W_{N,M1}$, and $L_{N,M1}$ are the "tuning-knobs" to control $V_{GS,M1}$.
- Since $V_{GS,M1} = V_{GS,M2}$ we equate the above equations and solve for I_O:

$$I_O = I_{REF} \cdot \left(\frac{\frac{W_{N,M2}}{L_{N,M2}}}{\frac{W_{N,M1}}{L_{N,M1}}}\right) = I_{REF} \cdot \left(\frac{W_{N,M2}}{W_{N,M1}} \cdot \frac{L_{N,M1}}{L_{N,M2}}\right)$$

- This is a powerful result because it tells us that *I_O is simply I_{REF} times the ratio of the widths and lengths.*
- In summary, M2 is a current source that is biased by M1. We "mirror" the current and control the I_O current by setting the width-length ratios of both transistors.
- *Special note*: It should be evident by KVL that $V_{DS,M1} = V_{GS,M1}$. Also, all diode connected circuits operate in saturation provided that $V_{GS} \geq V_{TH}$. We'll get back to this later.

Simple right? We can "parallel" more transistors to $V_{GS,M1}$ and if we set the ratio correctly, we can set provide the desired currents that we need. For example, consider Figure 2.14 which shows that we can just use a single biasing transistor M1, and mirror the current to multiple transistor "branches".

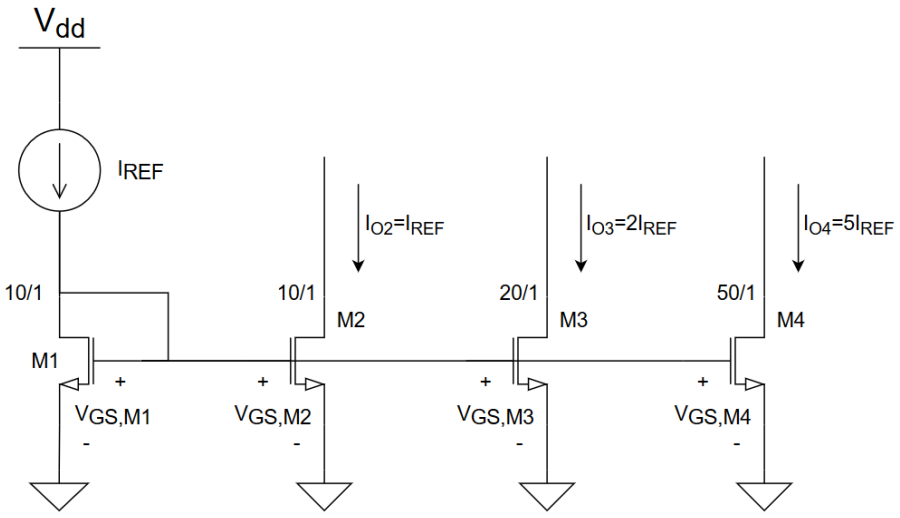

Figure 2.14 Using a current mirror to provide currents

In the Figure, the sizes used are in multiples of 1 um. For example, M1 has a 10/1 sizing and this means it has $W = 10\ um$ and $L = 1um$. Since M2, has the same width-length ratio of M1, the current $I_{O2} = I_{REF}$. The same goes for M3 and M4, who have $2\times$ and $5\times$ more width than M1 thus producing $I_{O3} = 2I_{REF}$ and $I_{O4} = 5I_{REF}$, respectively. *Generally, all lengths are often sized to be equal for both the biasing transistor and all current source transistors*. This means the length ratios are at unity and this leaves us sizing the widths only. The reason behind this has something to do with matching of the channel length modulation. The basic current also works for PMOS devices as shown in Figure 2.15.

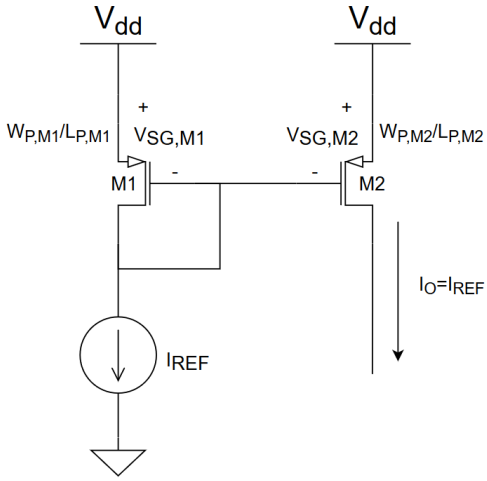

Figure 2.15 Current Mirror for PMOS

QUESTION (Q2.5):
Let's see if you're paying attention. Consider Figure 2.16 showing a set of PMOS current mirrors. Similar to Figure 2.14, fill in the table below with the correct sizes such that we can achieve the desired output currents per PMOS device. The width and lengths are in multiples of 1 um. Answer in multiples of the base width and length.

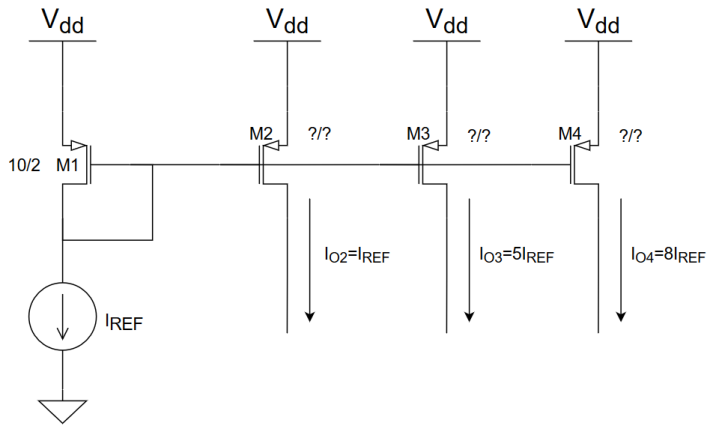

Figure 2.16 Set of PMOS current mirrors

Transistor	Width	Length
M2		
M3		
M4		

QUESTION (Q2.6):
Re-derive current mirror equation but this time, include the effects of channel length modulation. In other words, include the $(1 + \lambda V_{DS})$ terms. Be sure to add the current subscripts for each transistor.

Let's investigate Figure 2.13 in more detail. One important factor to consider is that $V_{GS,M1} = V_{DS,M1}$ for the biasing transistor but the $V_{GS,M2}$ may not be the same as $V_{DS,M2}$. Think about it carefully. The only way for the current to be perfectly mirrored is when $V_{DS,1} = V_{DS,2}$. Do the following:

1. Open the schematic "lab07_nmos_current_mirror.asc". You should see Figure 2.17.
2. Observe the following:
   - All transistors use 50 nm technology with $W = 10\ um$ and $L = 1\ um$
   - We have an external V_{DS} voltage that controls $V_{DS,M2}$
   - We are also sweeping V_{DS} to see how I_O ($I_{DS,M2}$) changes with changing $V_{DS,M2}$
   - We also have $I_{BIAS} = 30\ uA$
3. Run the simulation and plot I_{BIAS} and $I_{DS,M2}$. Combine them in one plot. You should get Figure 2.18.

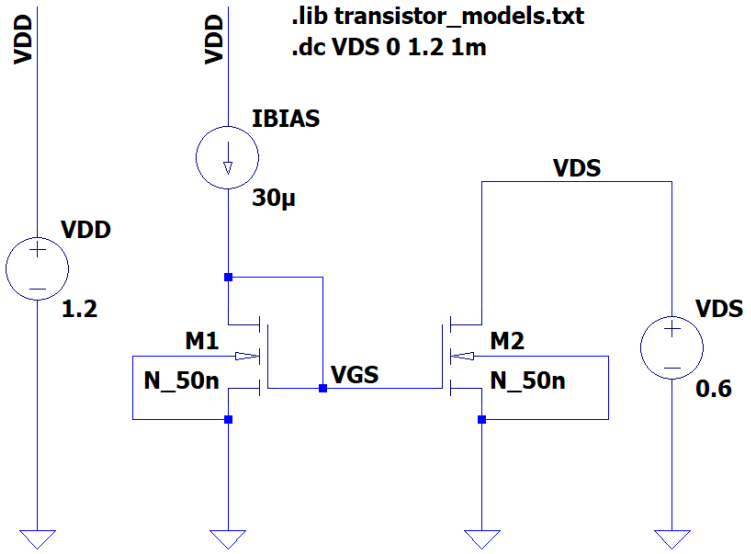

Figure 2.17 Schematic for simulating NMOS current mirror

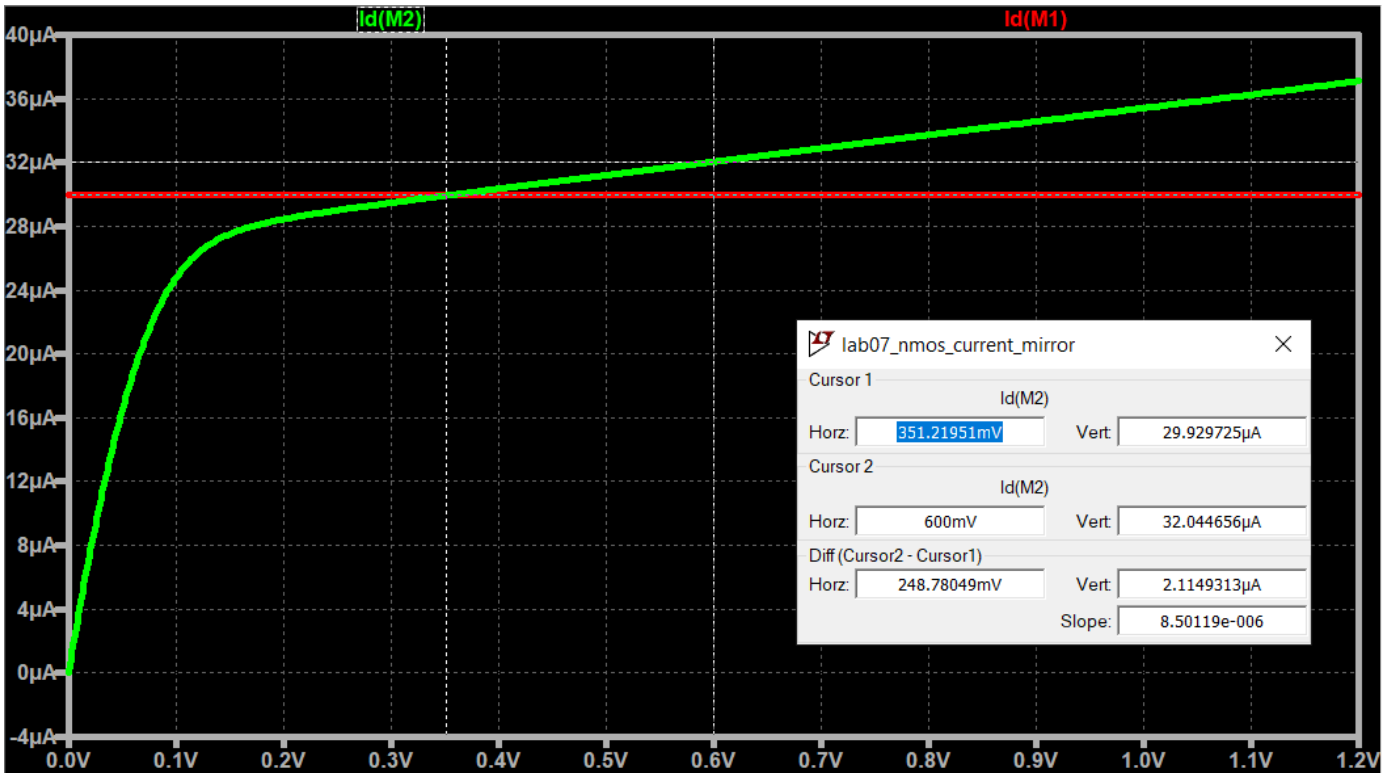

Figure 2.18 I_{BIAS} and $I_{DS,M2}$ comparison for the schematic in Figure 2.5

Consider the following observations:

- Our analysis is consistent with our simulation: *we can only get the exact* $30\ uA$ *current only if the NMOS current mirror has* $V_{DS,M2} = V_{GS,M2}$. That's the intersection of the two lines.
- Probing $V_{GS,M2}$ gives us $V_{GS,N2} \approx 357\ mV$. This is close to our biasing point in the previous discussions.
- This implies that there is a problem about the channel length modulation. Because $I_{DS,M2}$ changes with varying $V_{DS,M2}$ (by a factor of its r_o), then we cannot achieve proper current "mirror-ing"!

- What if we strictly need 30 uA when $V_{DS,M2} = 0.6\ V$? We cannot achieve this with our current setup. This necessitates some auxiliary circuits.
- There are two ways to rectify this:
    - Either find methods to increase r_o of M2
    - Adjust the widths of the biasing circuit such that it matches.
- Increasing r_o of M2 decreases the effects of changing $V_{DS,M2}$ on the $I_{DS,M2}$ current.
- Increasing the width of the biasing circuit decreases the effective mirrored current. This is evident from the current mirror equation. Increasing $W_{N,M1}$ reduces I_O. This may be bad since we can't fabricate exact widths.

For example, since $I_O \approx 32\ uA$ when $V_{DS,M2} = 0.6\ V$, if we want that $I_{O,desired} = 30\ uA$ instead, we can use re-size the biasing transistor such that $W_{N,M1}$ is $\frac{I_O}{I_{O,desired}} = 1.06667 \times$ larger than the original. That's equivalent to $W_{N,M1} = 10.667\ um$. That's an additional $667\ nm$ which is fairly significant for short-channel devices. If we use this new width and re-simulate our schematic, we get Figure 2.19.

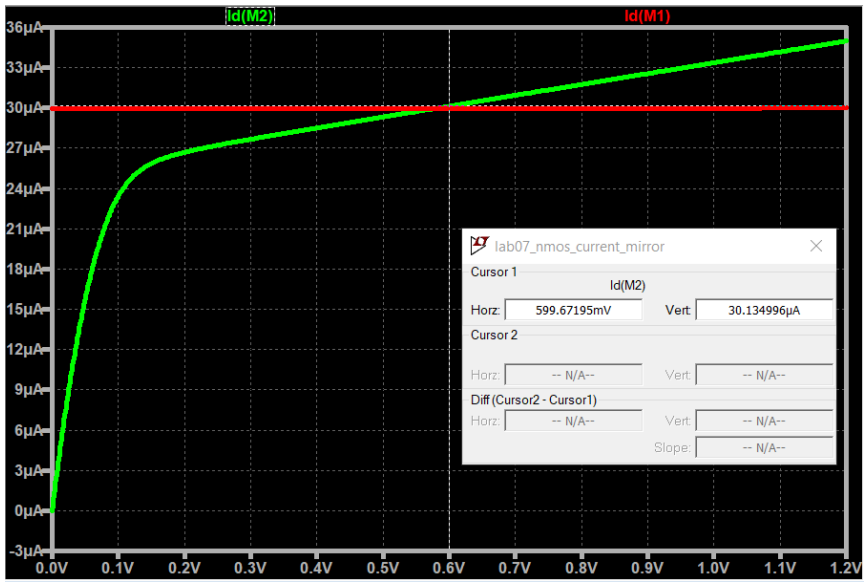

Figure 2.19 Fixed biasing width with $W_{N,M1} = 10.667\ um$

Great! We were able to get what we need. If you probe $V_{GS,M1}$ you'll see that we have approximately 351 mV which is much closer to our original 350 mV biasing from the previous lab. These discussions tell us something about how we design our biasing circuits: *It's a matter of tweaking the size of the biasing circuit such that our main current sources can achieve the desired biasing they need.* Most of the time, we design the current sources first before fixing the biasing circuit. In the previous lab, we designed the PMOS current source load such that it meets both the desired current and r_o at a given bias to support the main NMOS amplifier.

E. CS Amplifier with Current Mirror

In this section, we'll combine our biasing circuits to our simple CS amplifier with the current source load in Section B. We won't be focusing on getting exact small-signal parameters unlike before, but rather we'll focus on appreciating what happens to our amplifier. Consider Figure 2.20 which shows a simple CS amplifier with a PMOS current source load and it is biased by a current mirror.

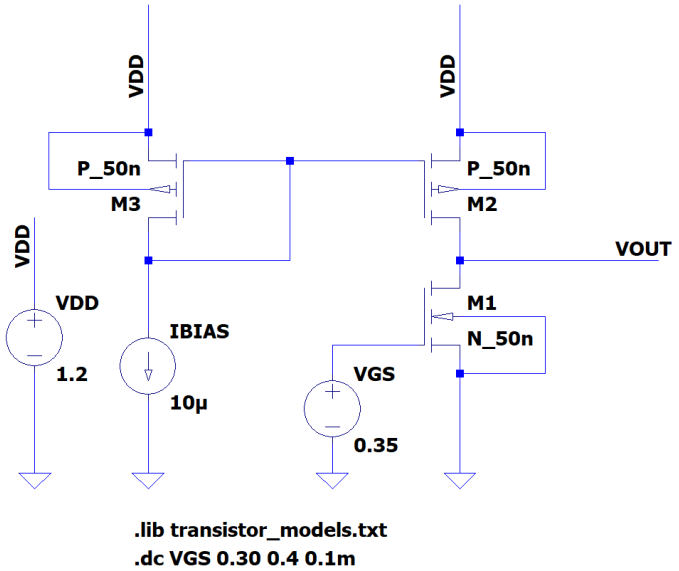

Figure 2.20 CS amplifier with the PMOS current mirror

Do the following:

1. Go ahead and open "lab07_cs_amp_w_cm.asc". This is the same as Figure 2.11.
2. Consider the following setup:
   - M1 has $W = 10\ um$ and $L = 1\ um$
   - M2 has $W = 30\ um$ and $L = 1\ um$
   - It is only the PMOS load which we are biasing with the current mirror
   - We fixed V_{GS} of the NMOS first but we'll bias this properly later
   - Recall from lab 06 that the desired operating current in the main amplifier is 30 uA
3. The PMOS biasing circuit (M3) has $W = 10\ um$ and $L = 1\ um$
   - It should follow that the current in M2 would be:

$$I_{M2} = I_{REF} \cdot \left(\frac{\frac{W_{P,M2}}{L_{P,M2}}}{\frac{W_{P,M3}}{L_{P,M3}}} \right) = 10\ uA \cdot \left(\frac{\frac{30}{1}}{\frac{10}{1}} \right) = 30\ uA$$

   - This means we are biasing M2 correctly with the current setup.
   - We are able to deliver $30\ uA$ of current to the NMOS transistor.
   - Simple right? Remember, with the desired $30\ uA$ current, all we had to do was mirror the $10\ uA$ and matching the sizes such that the delivered current is consistent.
4. Go ahead and run the simulation. Plot A_v and V_{OUT} with changing V_{GS}. You should get Figure 2.12.

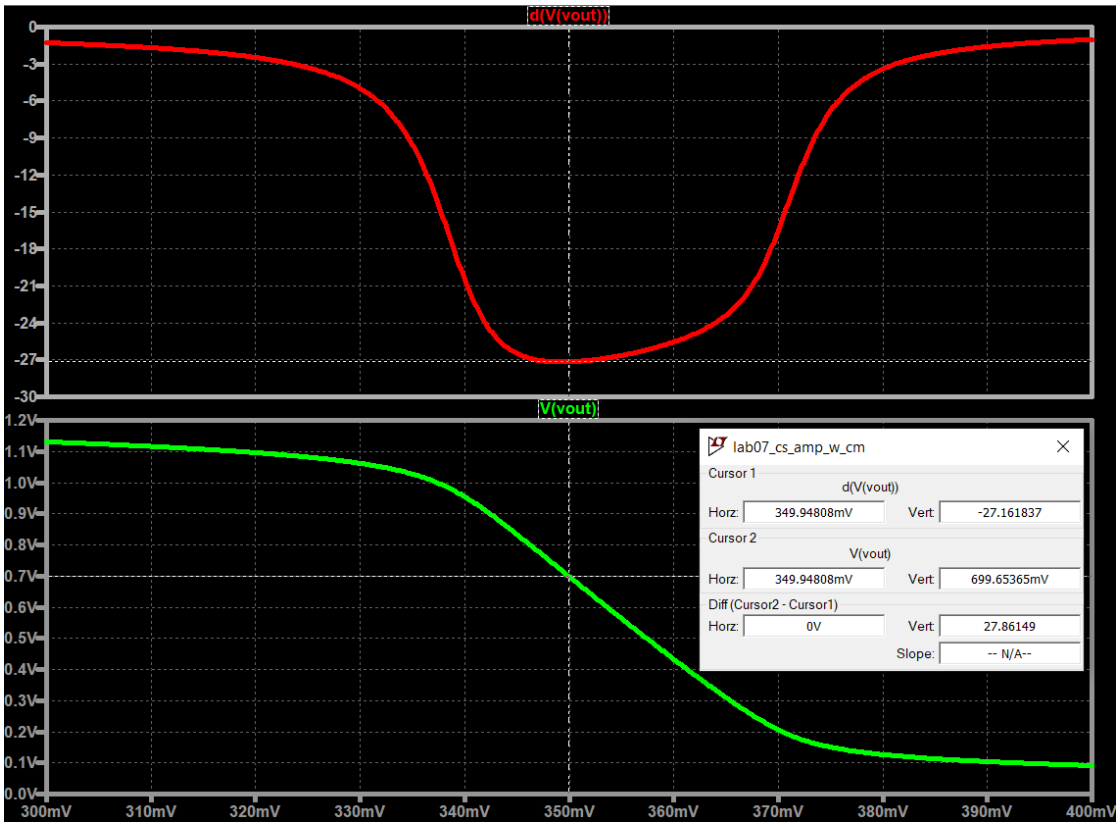

Figure 2.12 A_v and V_{OUT} simulation for the setup in Figure 2.11

Great! Now let's observe our results:

- For one, at $V_{GS} = 0.35\ V$ we have $A_v = -27$ which is actually still pretty close in our previous lab.
- The slight change; however, is that $V_{OUT} = 0.6\ V$ only when $V_{GS} = 0.353\ V$.
- The errors in this scenario are most likely due to the channel length modulation that we have not considered in our assumptions. Nevertheless, our circuit works!

Here's an important realization in our design: Did we even need to check the V_{SG} of the PMOS? No! Heck, we didn't even need to characterize and match the required V_{SG} of the PMOS load. The only thing we tried to match is the sizing given the bias current and the target current that the PMOS should deliver. Therefore, this leads to a very powerful design consideration: *we don't need to go through the tedious process of finding the correct bias for the PMOS load. All we had to do was match the current by sizing the biasing circuits appropriately.* This saves us the trouble of having to characterize over and over again.

Part III: Exercise

Don't You Hate Ladder Problems? ☹

Suppose you were tasked to design a CS amplifier with the following specs:

- It needs to drive a transistor load as a current source
- The gain must be $A_V \geq 25$
- The speed of your amplifier must be $g_{mn,} \geq 1\ mS$
- For simplicity, let's choose $V_{GSN} = 0.35\ V$, $V_{SGP} = 0.35\ V$, and $V_{OUT} = 0.6\ V$
- Start with $W = 500\ nm$ and $L = 500\ nm$ and use multiples of $100\ nm$ for widths and $500\ nm$ for lengths.
- For simplicity, we let $L = 5\ um$ be the maximum length for both NMOS and PMOS.

Do the steps that was taught to you. Show your solution for each step. If you need to provide plots for clarity, feel free to do so.

1. Calculate the r_{op} and r_{on} that gives the minimum $(r_{on}||r_{op})$.

- Show your solution here.

2. Determine the L_N that gives the minimum $g_{mn}r_{on}$.

- *In the event that we can't reach the minimum $g_{mn}r_{on}$ due to device limitations of the NMOS transistor, we need to re-calculate the desired r_{op} for the chosen $g_{mn}r_{on}$.*
- In the event that $g_{mn}r_{on}$ can't be met. Use the maximum specified length $L = 5\ um$.
- Show your solution and thought process here.

3. Using the chosen L_N in step 3, size W_N such that we get the minimum g_{mn}. Also, determine the operating I_{DN}.

- Show your solution and thought process here.

4. Size the PMOS such that we get the desired r_{op} and I_{DP}.

- Show your solution and thought process here.

5. Verify your design!

- Re-use "lab07_cs_amp.asc"
- Show a plot similar to Figure 2.12. Make sure to show via cursors what A_v is when $V_{GS} = 0.35\ V$ and what V_{GS} is when $V_{OUT} = 0.6\ V$.

6. Suppose we want to replace the PMOS current source with a PMOS current mirror that is biased by $I_{BIAS} = 10\ uA$. The case is similar to Figure 2.20.

- How would you size the biasing transistor? Show a plot of the new A_v and V_{OUT}.
- Make sure to show via cursors what A_v is when $V_{GS} = 0.35\ V$ and what V_{GS} is when $V_{OUT} = 0.6\ V$.
- Feel free to re-use "lab07_cs_amp_w_cm.asc"

Part IV: Supplementary Reading / Exercises

Loadline Analysis

There's another method for analyzing and observing how V_{OUT} moves when we vary V_{IN}. For the CS amplifier that uses a resistive load R_L, we have $V_{OUT} = V_{DD} - I_{DS} \cdot R_L$. This equation consists of two components: (1) the KVL $V_{OUT} = V_{DD} - I_L \cdot R_L$ where I_L is the current that goes through the resistor, and (2) the current $I_L = I_{DS}$ where I_{DS} is the transistor current. From our previous math courses, a solution exists if there is an intersection between two lines. For the CS amplifier with resistive load, the corresponding V_{OUT} is simply the intersection where both the KVL equation and the transistor current equation. We can analyze this using the *load line analysis* method where we plot I_{DS} and I_L separately. Consider Figure 4.1 which shows our CS amplifier but with the transistor and resistor components separated from each other. You can open the schematic "lab06_loadline_res.asc" and run the simulation. Simply plot the drain current and the resistor current. You should be able to obtain Figure 4.2. Take note that the simulation runs on a 50 nm NMOS transistor with $W = 10\ um$ and $L = 1\ um$.

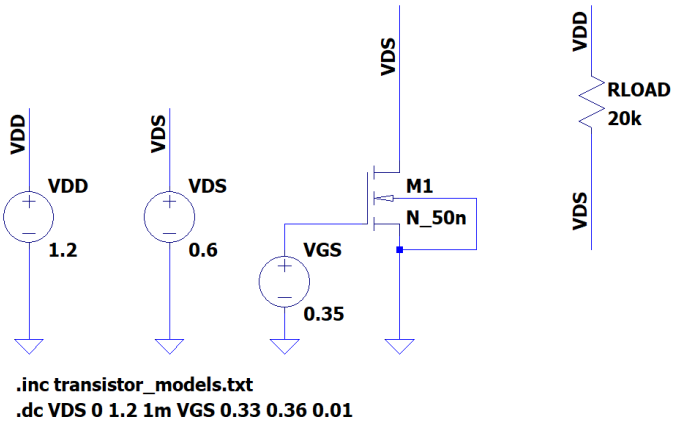

Figure 4.1 Schematic for Plotting Load Line Analysis for CS Amplifier with Resistive Load

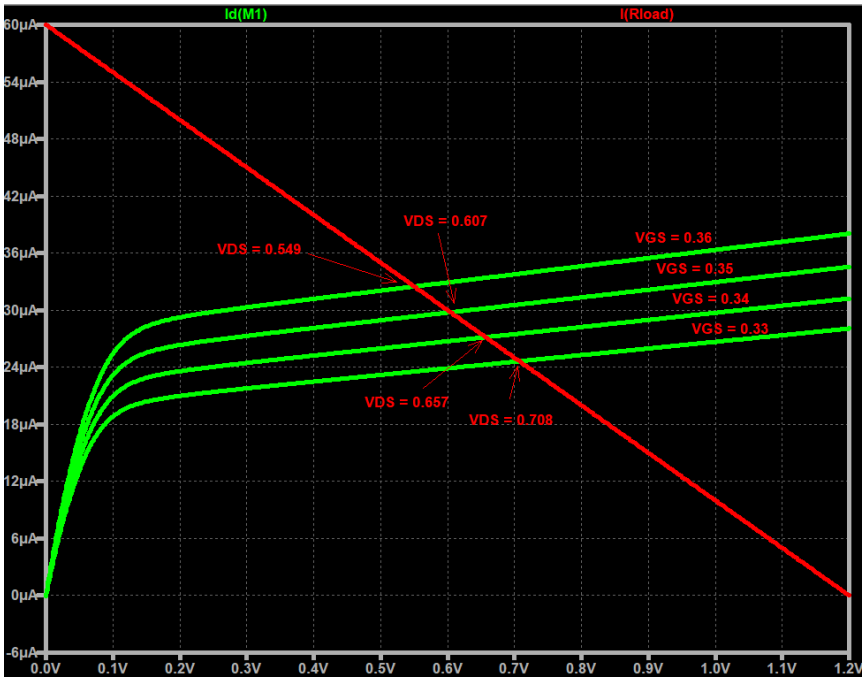

Figure 4.2 Load Line Analysis for Figure 2.9

The intersections where the current of the resistor and the transistor meet is where a $V_{OUT} = V_{DS}$ solution exists. If you plot this using the V_{OUT} vs. V_{IN} curve, you'll get the same $V_{OUT} = V_{DS}$ values (recall the V_{OUT} curves from lab 05). Observe how our NMOS curves slide along the R_L current line as we increase V_{GS}. When V_{GS} is swept from 0.33 V to 0.36 V, the V_{DS} changes from 0.55 V to 0.70 V. If we want to have greater change in V_{OUT} for even small changes in V_{GS} it is desirable that the load line is close to flat. If that happens, we should be seeing how the intersection points change from one end to the other. This only happens when the resistance is as high as possible. Hence, leading to the idea that it's better to have a current source as a load!

We can do the same load line analysis even for a transistor load. Consider Figure 4.3 which shows how to separate the NMOS and PMOS transistors. Feel free to open the schematic "lab06_loadline_tran.asc" and plot both the drain current of the NMOS and the source current of the PMOS.

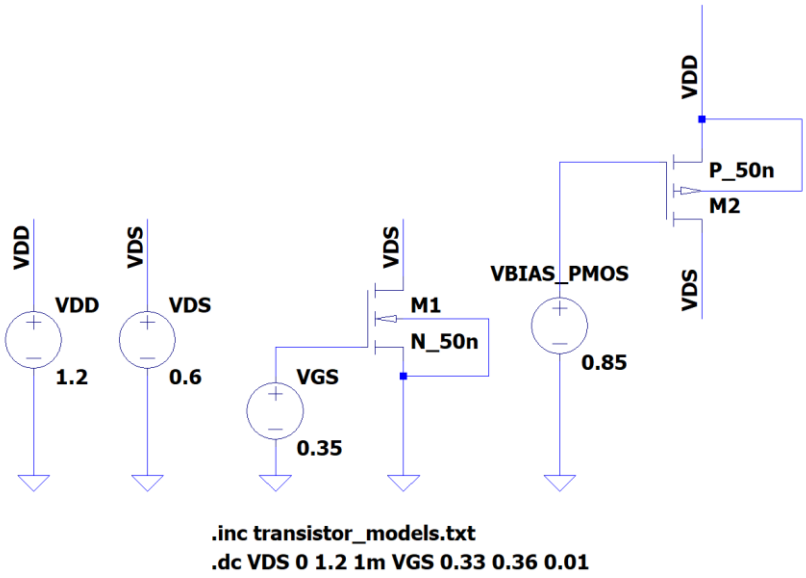

Figure 4.3 Schematic for Plotting Load Line Analysis for CS Amplifier with Current Source Load

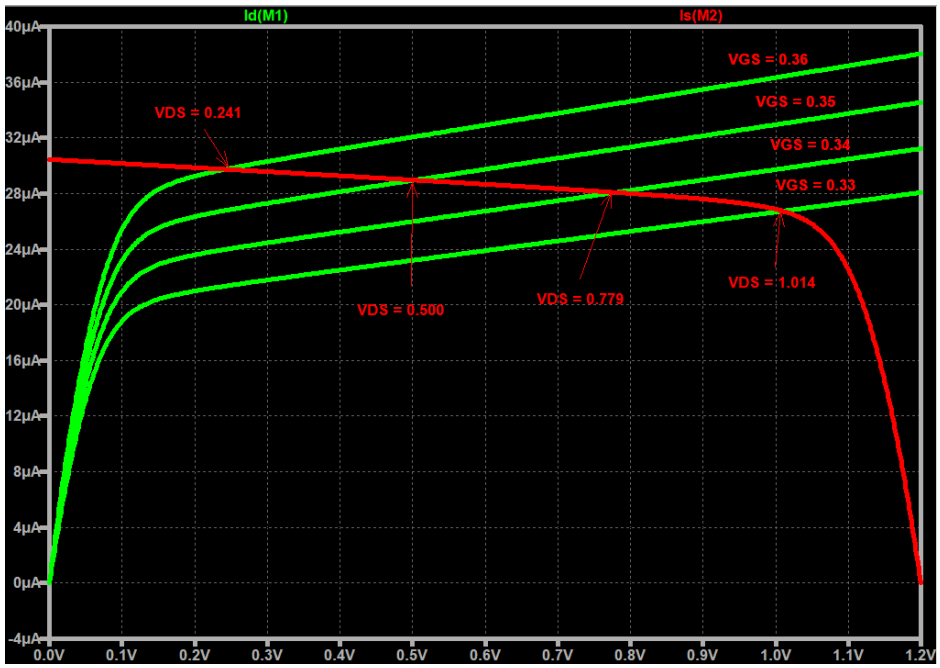

Figure 4.4 Load Line Analysis for Figure 2.11

Viola! Because the PMOS current source load line (the red one) is a lot flatter, then we have a very high change in $V_{OUT} = V_{DS}$ for very small change in V_{GS}. Always remember, if you are given an I-V curve, the flatter it is, the higher the impedance. Here's another important observation: When V_{GS} is low, the intersection point is close to the saturation point ($V_{SD,sat}$) of the PMOS device. When V_{GS} is high, the intersection point is close to the saturation point ($V_{DS,sat}$) of the NMOS device. Take time to internalize these simulations. It would be very nice if you could picture these on the fly.