University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 05 – Intro to Analog Design, Small-signal Parameters, and The Common Source Amplifier

What will you learn from this lab?

- Introduction to analog design.
- Extracting small-signal parameters.

A few reminders for any lab:

Each lab will always be broken down in 3 main sections

- Prelab/Review – this section can be treated like a "pre-lab" where you need to recall some of the previous concepts in your earlier courses or those that were discussed in the lecture.
- Training – this section guides you through a skill that you must learn. This could be a method in using the tool or a concept that is new to you.
- Postlab/Exercises – are some problems that you need to solve. Sometimes you need LTspice for it, and some don't. It's there for you to test what you have learned.
- Supplementary reading – these is an optional content but for the interested students, you can read and answer some of its questions. It's to further help you appreciate what IC design is.

There will be special boxes that you need to watch out for.

BLUE BOXES: Are used for useful notes and discussions. They can help you understand and appreciate the current topic at hand.

RED BOXES: Are notes that you need to watch out for. Some of these may be warnings that pertain to some limitations of our simulator. Or possibly some warnings on how to use particular circuit models.

GREEN BOXES: Are questions for that particular training task. They are also in the answer sheet so they'll be hard to miss.

Part I: Review

Answer the following questions in your answer sheet.

1. What are the small-signal parameters g_m, r_o, and $g_m r_o$? Mathematically, how do we get these? Use long-channel equations.

Part II: Training

Analog circuit design is challenging because of the number of specifications (specs) required for each design. Analog circuits trade-off several parameters: speed, gain, power, noise, voltage swing, area, and so much more. In this lab, we will focus more on further appreciating the behavior of a single transistor. It is loosely expected that you should be familiar with the mathematics of transistors (i.e. current equations and small-signal analysis) and basic circuit analysis (i.e. node-mesh, KVL, KCL, Thevenin-Norton transformations … etc). Our approach would start with a qualitative analysis, then support our understanding through simulations.

The minimum goal at the end of this course is to understand how a Miller Amplifier works. This involves building your knowledge base on the basic components for analog design, and learning how to build these in a step-by-step process. If you recall the Lego analogy, we need to know how to build the Lego pieces first before putting them all together.

A. Large-signal vs. Small-signal Behavior

Every analog designer should know by heart how our transistors behave in both large-signal (DC) perspective. It is in the DC view where we start to build an intuitive understanding of how our transistors work. However, the DC behavior of our transistors is non-linear. This means the current and voltage relationship does not follow Ohm's Law (i.e. $V = IR$ or $I = V/R$) because the current is a complicated function of V_{GS} and V_{DS}. The small-signal (AC) analysis linearizes our transistor by operating our device at a certain bias and applying a small-signal input only. This means we are only interested in a very small region where our devices look linear. *This is equivalent to taking the derivative of our current equation with respect to one voltage input (i.e. V_{GS} or V_{DS}). Which by now, you should know as our small-signal parameters*. Let's prove this concept through an example. Consider our basic characterization circuit in Figure 2.1. This is schematic "lab05_nmos_char.asc". You may open it if you like a side-by-side comparison with this discussion. Let's also assume that this NMOS has $W = 10\ um$ and $L = 1\ um$. We know that the output current I_{DS} is a function of both V_{GS} and V_{DS}. This is evident from the current equation shown in Equation 1.

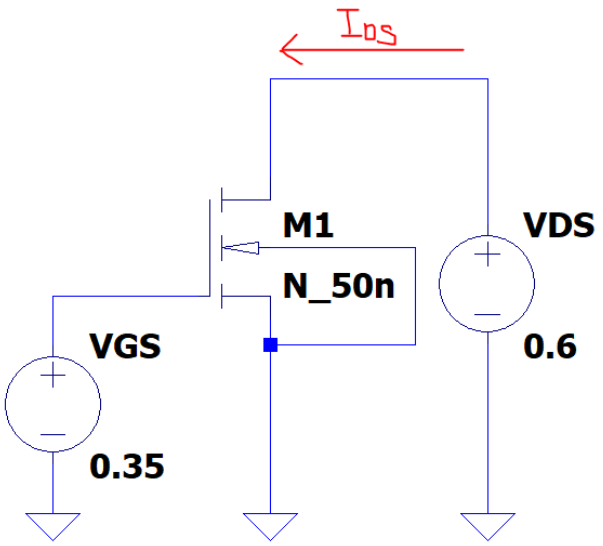


Figure 2.1 Simple characterization schematic for DC analysis

$$I_{DS} = \begin{cases} 0, & V_{GS} < V_{TH} \\ \mu_n C_{ox} \cdot \frac{W}{L} \cdot [(V_{GS} - V_{TH})V_{DS} - V_{DS}^2], & V_{GS} \geq V_{TH} \text{ and } V_{DS} < V_{GS} - V_{TH} \\ \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}), & V_{GS} \geq V_{TH} \text{ and } V_{DS} \geq V_{GS} - V_{TH} \end{cases}$$

Equation 1: Current equation for long-channel MOSFETs

In our previous labs, we were interested on how the output current changes when we fix V_{DS} and sweep V_{GS} (and also the scenario when we fix V_{GS} and sweep V_{DS}). Figure 2.2 is a simulation where V_{GS} is swept from 0 V to 1.2 V while $V_{DS} = 0.6\,V$. You can simulate this in the schematic. Make sure the width, length, and voltages are set appropriately.

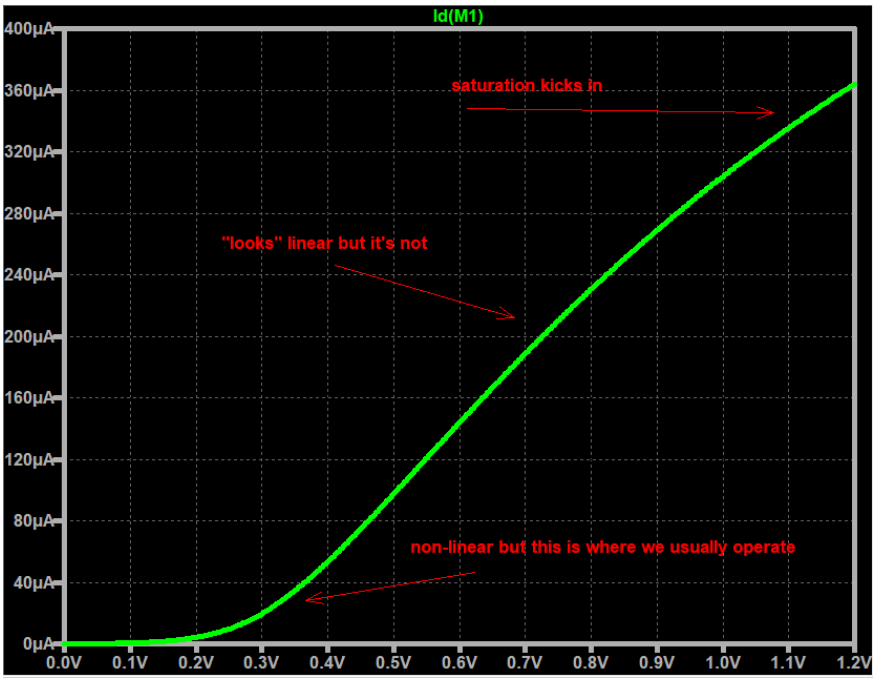


Figure 2.2 I_{DS} vs V_{GS} simulation of Figure 2.1

At a glance, it is clear that *transistors are non-linear devices*. I_{DS} vs V_{GS} does not follow the $y = mx + b$ equation. The lower-left region is highly non-linear. The middle "looks" linear. Finally, when V_{GS} is close to 1.2 V you can see that velocity saturation kicks in. As mentioned earlier, Ohm's law will be difficult to use for this device. KCL, KVL, node, and mesh techniques will be tedious. Remember: *KCL, KVL, node, and mesh techniques were originally taught to us only when voltages and currents are directly proportional to each other. A.K.A Ohm's Law ($V = IR$).* What do we have to do then? We need to "linearize" this behavior by using a small-signal analysis.

Small-signal analysis tells us that "small-signal" inputs to our transistors make our transistors look linear by looking in a very small region only. Mathematically, we are taking the derivative. If they become linear, then we can apply Ohm's law! To see this in action, let's say we want to zoom into the current region in between 0.34V and 0.36V. Figure 2.3 points to the region where we want to zoom into. If we zoom in and take a closer look, we have Figure 2.4.

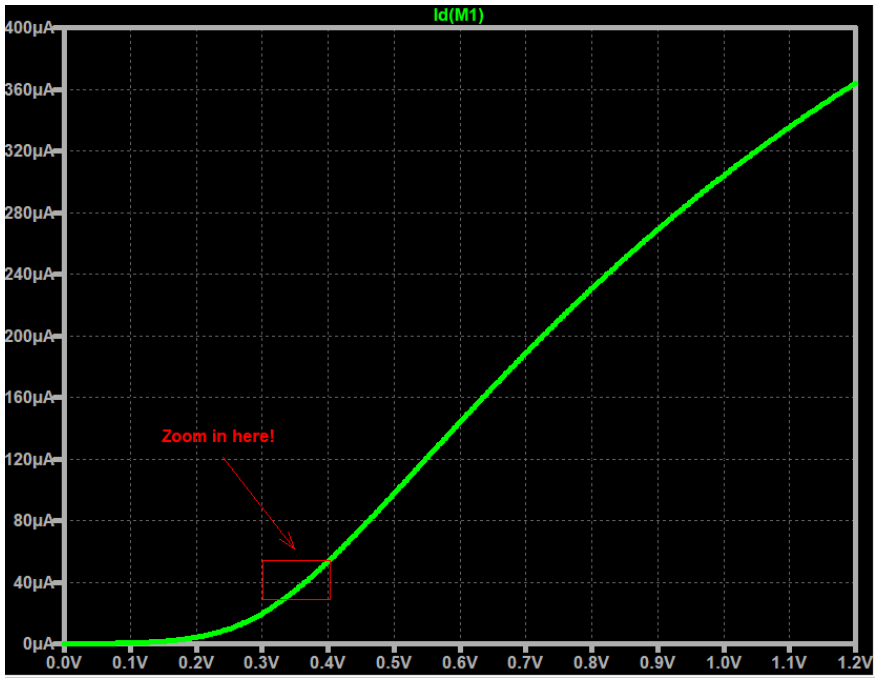


Figure 2.3 Zoom in indicator

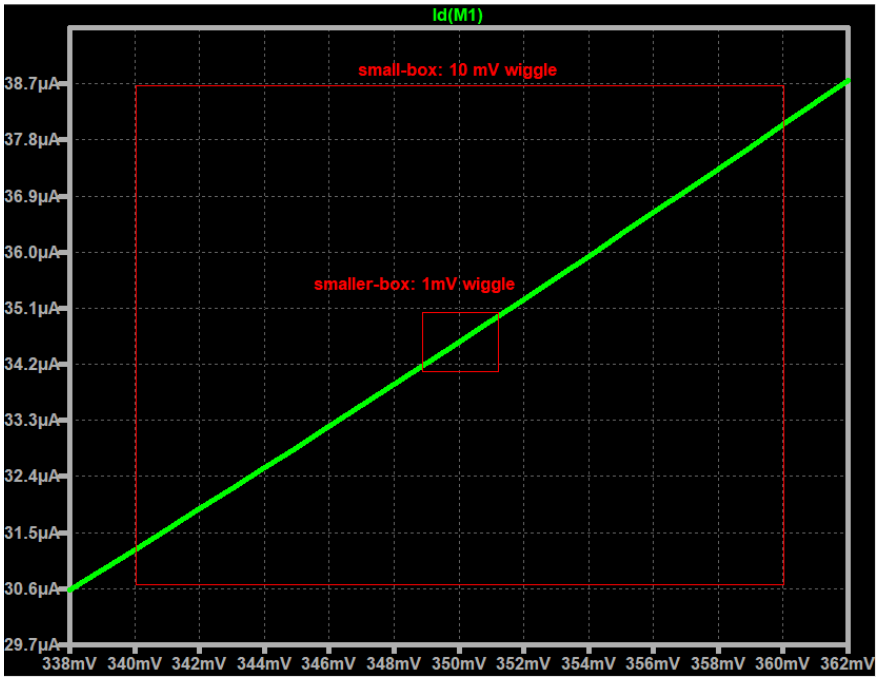


Figure 2.4 Zoomed-in scope. I_{DS} and V_{GS} become linear!

Figure 2.4 makes our transistor look linear only at the very small region (i.e. $< 10\,mV$). Therefore, we can conveniently apply Ohm's Law. Make sure to always remember: *(1) transistors are non-linear devices, (2) small-signal makes them "look" linear.* This is the most intuitive visualization on why small-signal analysis is important.

Alternatively, *small-signal analysis describes how our output currents and voltages change at a given bias*. Figure 2.5 shows that small-signal inputs and outputs are superimposed (added) to the main biasing sources. Small-signal characteristics change whenever our *biasing point* changes. For example, Figure 2.4 shows the linear region in the region close to $V_{GS} = 0.35\,V$ (in the range $0.34\,V \leq V_{GS} \leq 0.36\,V$). If we take a different region, say $1\,V \leq V_{GS} \leq 1.1\,V$ we are most likely going to get a slope of our linear region in Figure 2.4.

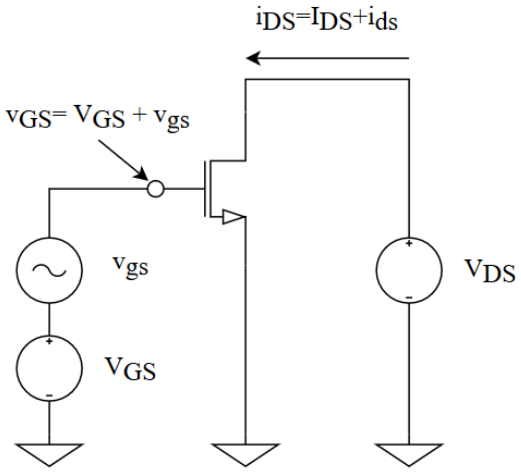


Figure 2.5 Depiction of what small-signal input v_{gs} influencing the output current i_{DS}

Figure 2.5 shows that the small-signal v_{gs} is superimposed (added) to the DC source V_{GS}. Most of the time, we consider v_{gs} to be small-signal when $v_{gs} \leq 10\,mV$. Go beyond 10 mV and the linear region won't look so linear anymore. The larger box in Figure 2.4 shows the 10 mV boxed-region that looks linear but you can still see some artifacts at the far end corners where I_{DS} starts to curve a bit. The 1 mV boxed region shows the greatest linearity. *The smaller the signal, the more linear we can get*. In most cases any input $\leq 10\,mV$ is enough. Ideally, if these small-signal inputs are small enough, they DO NOT change the INPUT DC operating points but it can change the output DC (i.e. $V_{OUT} = V_{DS}$). For example, if $V_{GS} = 350\,mV$ and $v_{gs} = 1\,mV$ sinusoid, then $v_{GS} = 350\,mV \pm 1\,mV \approx 350\,mV$. *If DC sources don't change so much, then in perspective of small-signal circuit models we short all DC voltage sources and open all DC current sources.* Moreover, when we apply a small-signal input, there is a corresponding small-signal change at the output. For example, applying some v_{gs} input produces an output current change i_{ds} that is super-imposed on I_{DS} (hence $i_{DS} = I_{DS} + i_{ds}$). Sometimes, the output *can* change the output DC operating point too as we will see later on. Spoiler alert: you should recognize by now that the resulting i_{ds} for a given input v_{gs} is the transconductance: $i_{ds} = g_m v_{gs}$.

DISCUSSION:
Note that we will use lower-case to indicate small-signal components (i.e. v_{gs}), upper-case for DC components (i.e. V_{GS}), and we use a small-case for the base and upper-case for the subscript to indicate the super-imposition of both DC and small-signal components (i.e. $v_{GS} = v_{gs} + V_{GS}$).

DISCUSSION:
Additionally, it's important to understand that when we do small-signal analysis, we analyze how a small-signal change at the inputs produces a small-signal change at the output. In Figure 2.5, observe how the v_{gs} is added to V_{GS}. Again, when the small-signal input v_{gs} is applied, it produces a small-signal output current i_{ds} and this also sits on top of I_{DS}. For example, let's say our input DC operating point is $V_{GS} = 0.35\ V$ and this produces some $I_{DS} = 30\ uA$. Let's say we want to add $v_{gs} = \pm 10\ mV$ and say $g_m = 300\ uS$ then $i_{ds} = (\pm 10\ mV) \times (300\ uS) = \pm 3\ uA$. This means that $v_{GS} = 340\ mV$ and $v_{GS} = 360\ mV$ ($v_{GS} = V_{GS} + v_{gs}$), produces the total output currents $i_{DS} = 27\ uA$ and $i_{DS} = 33\ uA$, respectively ($i_{DS} = I_{DS} + i_{ds}$). Make sure this concept is clear. DC and small-signal analysis are analyzed separately but the effects are combined into one.

Finally, here are a few things to remember (these were already introduced to you in the lecture and in previous courses):

- Engineers often inter-change AC analysis and small-signal analysis. *The complete definition of AC analysis is that it is the small-signal frequency response*. This is because reactive elements (i.e. capacitors and inductors) start to matter too. However, our lessons usually begin with the DC small-signal. At low frequencies (i.e. DC where $f \to 0$), capacitors are opened and inductors are shorted. This allows us to focus only on g_m and r_o components only which are DC small-signal parameters.
- For every small-signal analysis we always do the following steps:
  1. Calculate the DC operating point (sometimes known as bias point) using our current equations.
  2. Using the DC values computed in step 1, we determine the small-signal parameters.
  3. We replace the MOSFETs in our circuit with their small-signal models.
  4. We short all DC voltage sources and open all DC current sources.
  5. Redraw the small-signal circuit model

B. Quick Review of Small-signal Parameters

Figure 2.6 shows the small-signal two-port circuit model of an NMOS. Let's try to build intuition as to why the small-signal circuit is built in such a way. Try to internalize the following:

1. The input impedance seen at the gate is infinite (an open circuit) because the gate consists of the gate-oxide which acts like an insulator. Therefore, no current can flow through the gate.
2. *Transconductance g_m is defined as how much small signal output current i_{ds} is produced for every unit of small-signal input voltage v_{gs} while V_{DS} is fixed.* Mathematically, $g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{i_{ds}}{v_{gs}}$. Looking at Figure 2.6, observe how $g_m v_{gs}$ contributes to the total i_{ds} current.
3. *The output impedance r_o (or r_{ds}) is defined as how much small-signal output voltage v_{ds} is produced for every unit of small-signal output current i_{ds} while V_{GS} is fixed.* Mathematically, $r_o = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{v_{ds}}{i_{ds}}$.
4. Because the output (from drain to source) is an open circuit, then all of the i_{ds} current goes through the output impedance r_o. Every change in i_{ds} produced by $g_m v_{gs}$, influences the output voltage v_{ds} via the output impedance r_o. *Collectively, we know this as the small-signal gain $g_m r_o$ which tells us how much output voltage v_{ds} changes for every unit of small-signal input voltage v_{gs}*. Mathematically, $g_m r_o = \frac{\partial V_{DS}}{\partial V_{GS}} = \frac{v_{ds}}{v_{gs}} = \frac{v_{out}}{v_{in}}$. Take note that the gain has a negative factor in it because the polarity of the current is opposite of the designated v_{ds} direction (i.e. the direction of the i_{ds} current going through r_o is in the opposite direction).

When in doubt, make sure to remember the 4 important intuitive concepts in mind. This will make it easier for you to go back to in case you forget.

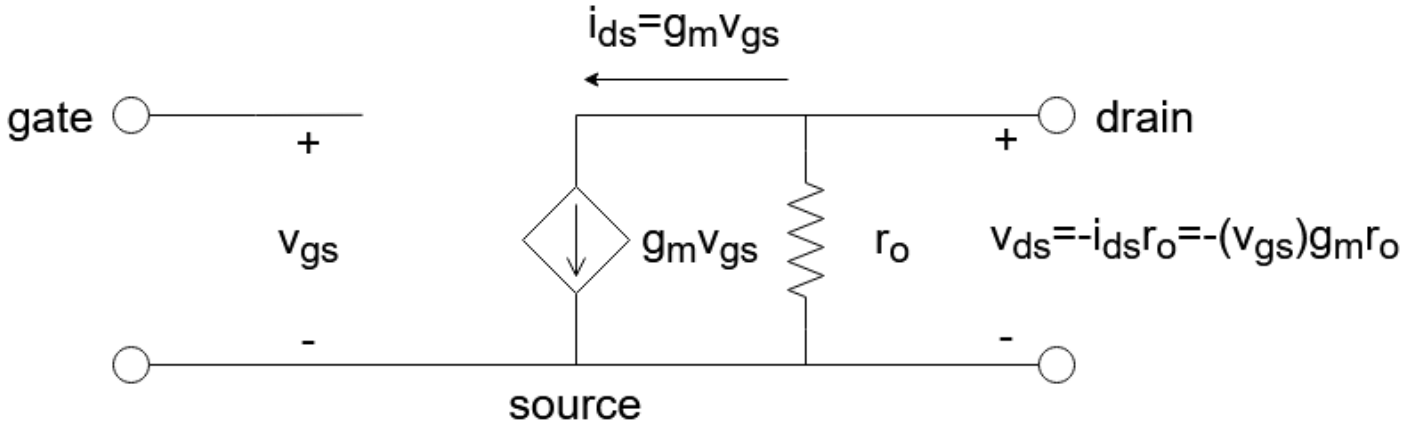


Figure 2.6 Small-signal two-port network circuit model for NMOS transistor

C. Extracting Transconductance

Just to re-iterate, transconductance g_m tells us how much small-signal current changes for every change at the input v_{gs} and we can describe the output small-signal current relationship to the input as: $i_{ds} = g_m v_{gs}$. Because of this "small change" it implies that we can take the derivative of the current in Equation 1. Using the saturation current, we have:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \cdot \frac{W}{L} I_{DS}} = \frac{i_{ds}}{v_{gs}}$$

Let's get a plot for g_m. Do the following steps.

1. Open "lab05_nmos_char.asc".
   - Take note of this schematic as this will be our characterization schematic. Any analog designer always starts with this so he/she can extract small-signal parameters of interest.
   - Use a 50 nm transistor with $W = 10\ um$ and $L = 1\ um$. We'll be using 1 um initial length so we can "simulate" a long-channel but using a short-channel device.
   - Don't forget to set $V_{DS} = 0.6\ V$

.inc transistor_models.txt
.dc VGS 0 1.2 1m

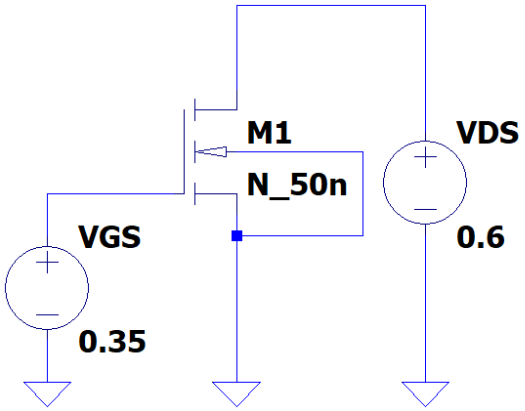


Figure 2.7 Characterization circuit for NMOS transistor

2. Create a DC analysis where V_{GS} is swept from 0 to 1.2 V
3. Simulate and plot I_{DS}. You should get a figure similar to Figure 2.2.
4. Click on Id(M1) in your plotting plane and change it to d(Id(M1)), the d() function computes the derivative of the given plot. If done correctly you should get Figure 2.10.
5. Congratulations! You now have the transconductance of your circuit.

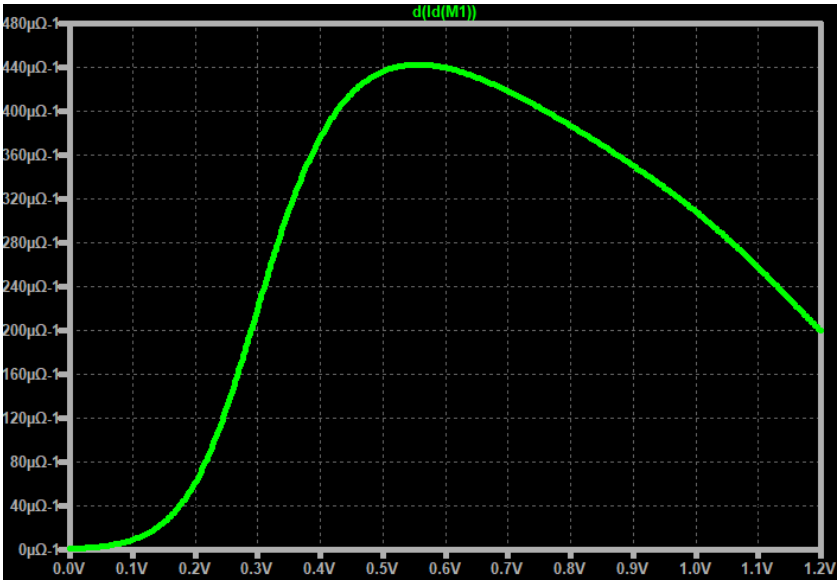


Figure 2.8 g_m vs V_{GS}

QUESTION (Q2.1):
Just to make sure you know how to read plots.

1. What V_{GS} would give us $g_m \approx 250\ uS$?
2. What about $g_m \approx 300\ uS$?
3. What's g_m at 0.35 V?

QUESTION (Q2.2):
Complete the statements with increase, decrease, no change, or makes no sense and be sure to indicate why?

1. As W increases, g_m _____.
2. As L increases, g_m _____.
3. As W and L increases, g_m _____.
4. As V_{GS} increases, g_m _____.

BONUS QUESTION (Q2.3):
Give an intelligent guess as to why the transconductance starts to decrease as we approach $V_{GS} = 1.2\ V$?

D. Extracting Output Impedance

Similar to transconductance, the output impedance r_o describes how the small-signal v_{ds} changes for a change in small-signal i_{ds}. In mathematical terms this is the reciprocal of the $\frac{\partial I_{DS}}{\partial V_{DS}}$:

$$r_o = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{\lambda\left(\frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS})\right)} = \frac{1}{\lambda I_{DS}} = \frac{v_{ds}}{i_{ds}}$$

Extracting the output impedance uses the same characterization schematic in Figure 2.9. The only difference is that we fix V_{GS} and sweep V_{DS}. Do the following steps.

1. Using the same schematic in Figure 2.9 but this time sweep V_{DS} from 0 to 1.2 V in 1mV increments.
   - $V_{GS} = 0.35\ V$ was chosen as such so that we have a low "$V_{DS,sat}$". Increasing V_{GS} will make the range of our saturation region smaller.
   - Make sure to revert $W = 10um$ and $L = 1um$ back. Without the k factor from the questions.
2. Plot I_{DS} once and you should get Figure 2.11.
   - Take note that this this time, the x-axis is V_{DS} and not V_{GS}

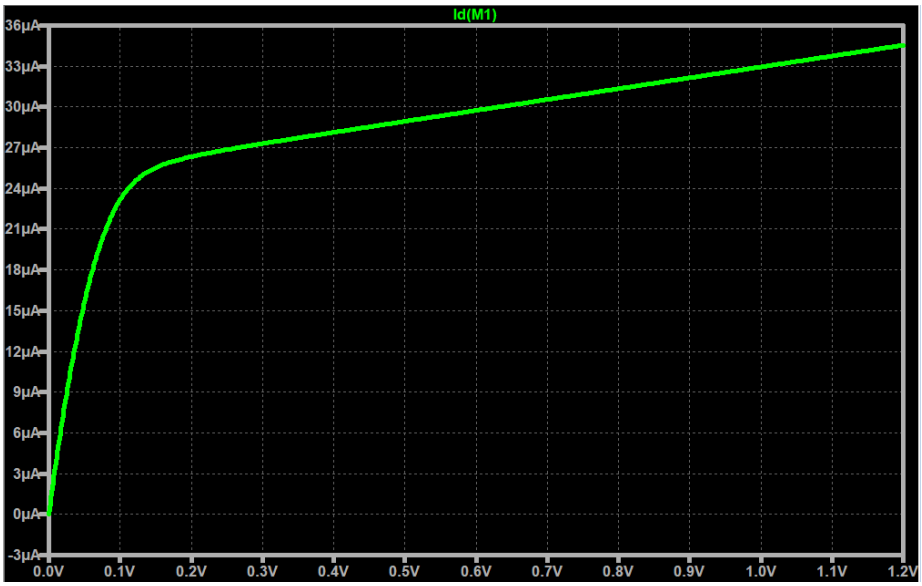


Figure 2.9 I_{DS} vs V_{DS} curve

3. r_o is the reciprocal of the derivative of I_{DS} with respect to V_{DS}. This can be done by modifying Id(M1) into 1/d(Id(M1)). The result should look like Figure 2.12.

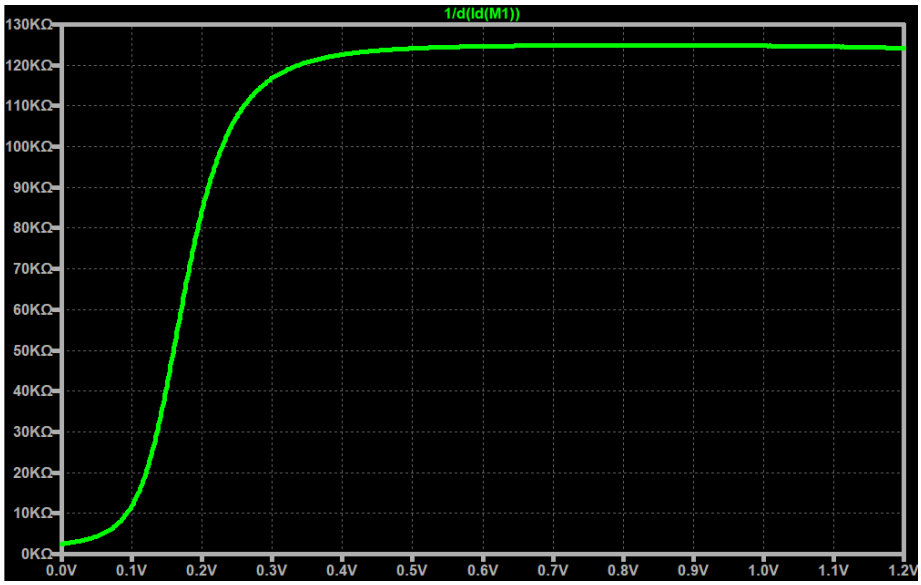


Figure 2.10 r_o vs V_{DS}

4. Congratulations! You now know how to extract r_o.

QUESTION (Q2.4):
Roughly what is r_o for the entire saturation region?

QUESTION (Q2.5):
Complete the statements with increase, decrease, no change, or makes no sense and be sure to indicate why?

1. As W increases, r_o _____.
2. As L increases, r_o _____.
3. As W and L increases, r_o _____.
4. As V_{DS} increases, r_o _____.

QUESTION (Q2.6):
Fill the blanks with increase, decrease, or no change. When we increase the width, g_m _____ and/but r_o _____. When we increase the length, g_m _____ and/but r_o _____. What kind of engineering problem do we have?

E. Extracting Intrinsic Gain ($g_m r_o$)

In this section (and in the next), we might go a bit too fast especially when we're discussing AC analysis. It is recommended that you should review concepts about AC analysis especially on how to read bode-plots. In the interest of time, we'll be omitting some details about these since it is expected that they were taught to you in your earlier courses. However, we'll make sure to emphasize the important interpretations. Should you have any questions, feel free to email your professors/instructors or ask in our Piazza group.

Intrinsic $g_m r_o$ is the inherent gain of the transistor while it's not connected to any load. Practically, it's a measure of how our V_{OUT} changes with V_{IN}. There are several methods for extracting $g_m r_o$ but the characterization circuit in Figure 2.7 would not work because the drain node is tied to an ideal voltage source. Remember, DC sources in small-signal analysis are shorted. Therefore, the v_{out} node in Figure 2.6 will be shorted to ground and it makes it impossible to correctly measure $g_m r_o$ because no output can be produced (i.e. $v_{out} = 0$). AC analysis is the most convenient way of measuring $g_m r_o$ but this requires finding a way on how to correctly bias the transistor while shaking the drain node free in the AC perspective. Consider Figure 2.11 which shows the schematic for extracting $g_m r_o$.

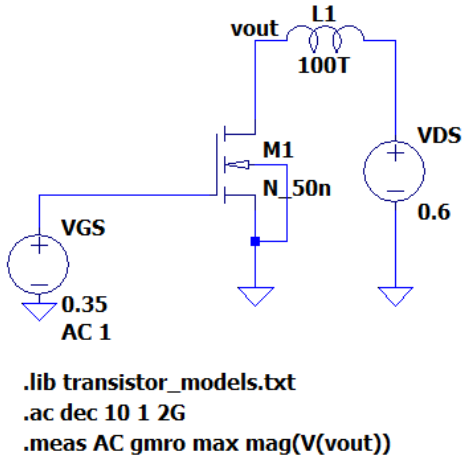


Figure 2.11 Schematic for Extracting $g_m r_o$

The clever trick here is to *use a very large inductor to bias the circuit*. Take note, we're only interested in the frequencies near the DC level ($f \to 0\ Hz$). Recall that inductors are shorted during DC; hence, the 100T H inductor is nothing but a wire and the V_{DS} supply can correctly bias the transistor. During AC analysis, the impedance of the inductor is "infinitely" large due to the 100T H value. Therefore, at $f \geq 0$, the inductor is at "infinite" impedance creating an open circuit. Recall that the impedance of an inductor is $Z_{inductor} = j\omega L$. The small-signal circuit model of Figure 2.11 is equivalent to the ideal small-signal model in Figure 2.6. Figure 2.12 visualizes this scenario.

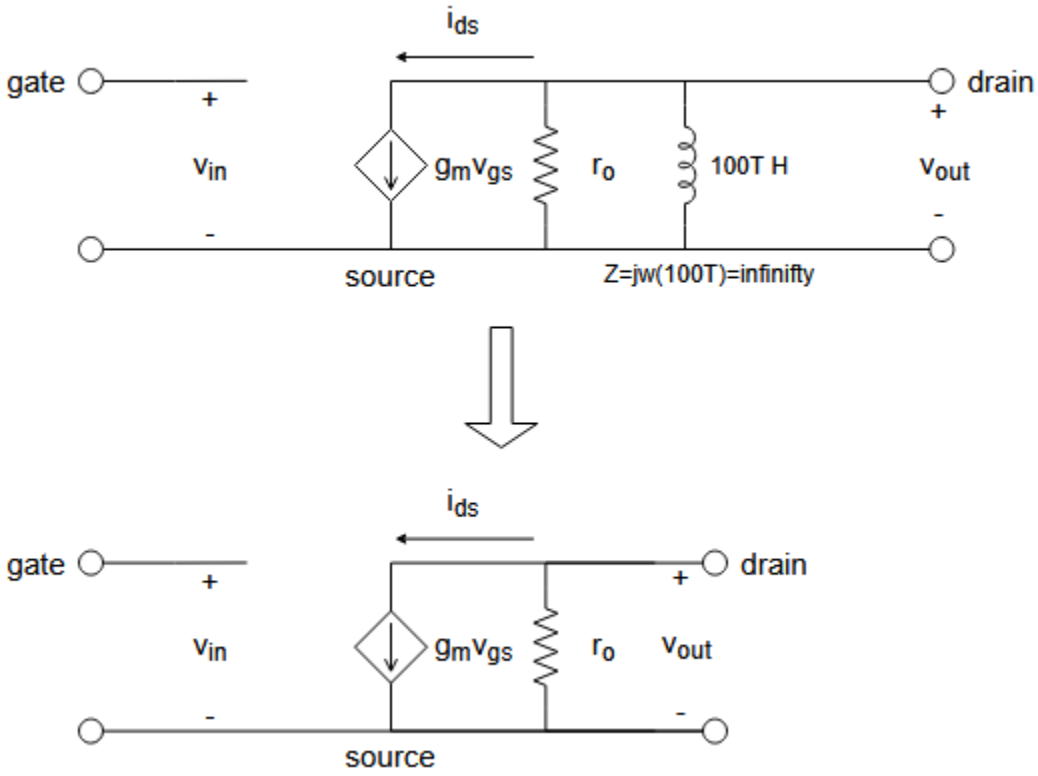


Figure 2.12 Visualization showing that a 100T H inductor becomes an open-circuit in small-signal

Let's simulate something for appreciation. Do the following:

1. Open the schematic "lab05_gmro_extract.asc". This is the same setup as Figure 2.11.
2. Check out the following:
   - The size of the transistor is $W = 10\ um$ and $L = 1\ um$
   - $V_{GS} = 0.35\ V$ and $V_{DS} = 0.6\ V$
   - The V_{GS} supply also has an AC input of 1 V. Right-click V_{GS} supply and you should see it on the right side under the AC amplitude box. This means we are telling the simulator to use $v_{in} = 1\ V$.
   - The .ac SPICE directive tells the simulator to do an AC analysis by sweeping the frequency from 1Hz to 2G Hz with 10 points per decade. The first number indicates how many points per decade, while the 2nd and 3rd arguments indicate the minimum to the maximum frequency range.
   - The .meas SPICE directive tells the simulator to measure the maximum magnitude of the node vout, obtained from the circuit, then store it into the variable gmro.
   - For now, accept what is presented to you first and the explanations will come later.

DISCUSSION:
It is important to know that whenever we invoke AC analysis, the simulator transforms our circuit into it's small-signal model. The transformation in Figure 2.12 depicts this scenario. Using the small-signal model, the simulator takes in an AC input (in this case that's $V_{GS,AC} = 1\ V$ from Figure 2.11) and apply it to the small-signal model in Figure 2.12. Take note, *whenever we set an AC input, this is equivalent to applying a voltage source in the small-signal model*. This is depicted in Figure 2.13.

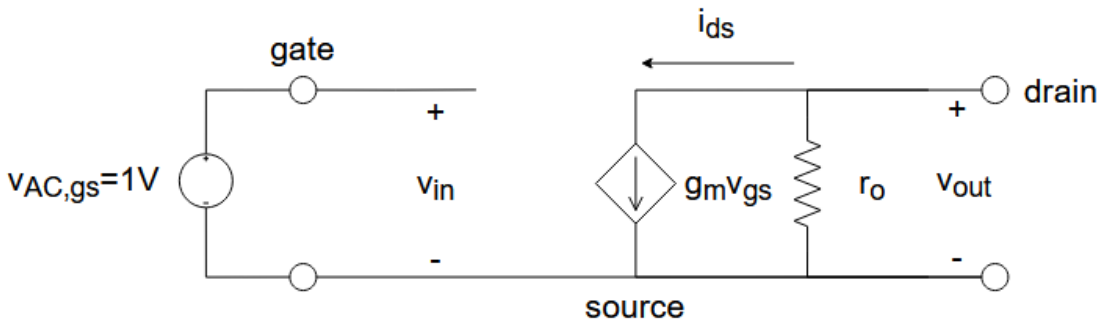


Figure 2.13 Small-signal model with a small-signal AC input = 1V

AC sources do not appear in the DC simulations, and DC sources do not appear in AC simulations. They are exclusive to each other. Keep this in mind!

3. For now, we'll simulate the entire frequency spectrum from $f = 1\ Hz$ up to $f = 2\ GHz$.
4. Run the simulation then plot the vout node. You should get Figure 2.14.

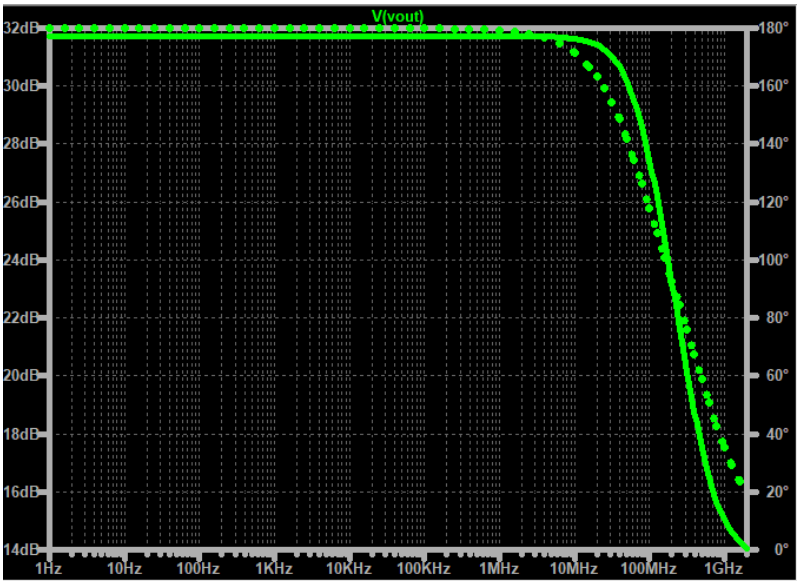


Figure 2.14 Bode plot for Figure 2.11

5. Right-click on the right y-axis (that's depicting the phase) and select don't plot phase to just have the magnitude present. We'll ignore the phase for now.
6. Set a cursor to get the magnitude of vout the range of 1Hz to 100 Hz. You should get around: 31.72 dB.
   - If you view the spice error log, you should also see the measured $g_m r_o = 31.72\ dB$.

- Getting the magnitude of the v_{out} node is equivalent to getting $g_m r_o$ already. Because $v_{out} = g_m r_o \cdot v_{in}$ but since our AC input $v_{in} = 1$, then it follows that $\frac{v_{out}}{v_{in}} = \frac{v_{out}}{1} = g_m r_o$. Keep this in mind!
- The reason why the .meas SPICE directive takes the maximum of the magnitude, is because at DC, we get the maximum gain. The gain goes down at higher frequencies due to the parasitic capacitances.
- Moreover, you should know that $A_{v,dB} = 31.72\ dB \rightarrow A_v = 38.54$.
- Recall that $A_{v,dB} = 20\log(A_v) \rightarrow A_v = 10^{\frac{A_{v,dB}}{20}}$.

7. From sections C and D:
   - $g_m \approx 300\ uS$ when $V_{GS} = 0.35\ V$ and $V_{DS} = 0.6\ V$
   - $r_o \approx 125\ k\Omega$ when $V_{GS} = 0.35\ V$ and $V_{DS} = 0.6\ V$
   - Therefore, $g_m r_o \approx 37.5$ which is close to the simulated small-signal gain of $A_v = 38.54$
   - Fantastic! You now know how to extract $g_m r_o$!

We're also interested on how to extract $g_m r_o$ when V_{GS} changes. Do the following:

1. Close your plotting window from the previous activity.
2. Modify your circuit with the following. The changes are depicted in Figure 2.15.
   - Change the DC bias of the V_{GS} source with the variable vgs. We'll be doing a parametric sweep.
   - Add the spice directive: ".step param vgs 0 1.2 0.01". This means we'll parametrize the vgs variable from 0 V to 1.2 V in 0.01 V increments.

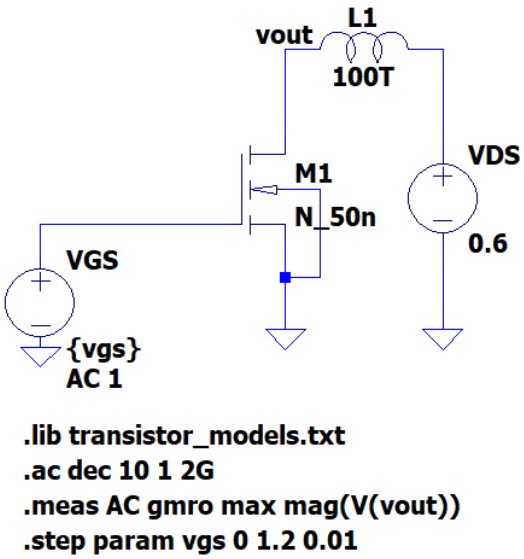


Figure 2.15 Modified $g_m r_o$ extraction circuit

2. Run your simulation.
3. Open the SPICE error log, then look for "measurement: gmro". Right-click that and select "Plot .step'ed .meas data". You should get Figure 2.15.
4. Congratulations! You now know how to plot $g_m r_o$ vs V_{GS}.

In summary, we can obtain $g_m r_o$ by extracting the maximum gain in the AC simulations. We were able to measure $g_m r_o$ without disrupting the biasing of our circuit by the use of a very large inductor. This inductor is a short in DC and an open circuit in AC. Remember, $g_m r_o$ is the DC voltage gain and we're only interested in the value when $f \rightarrow 0\ Hz$.

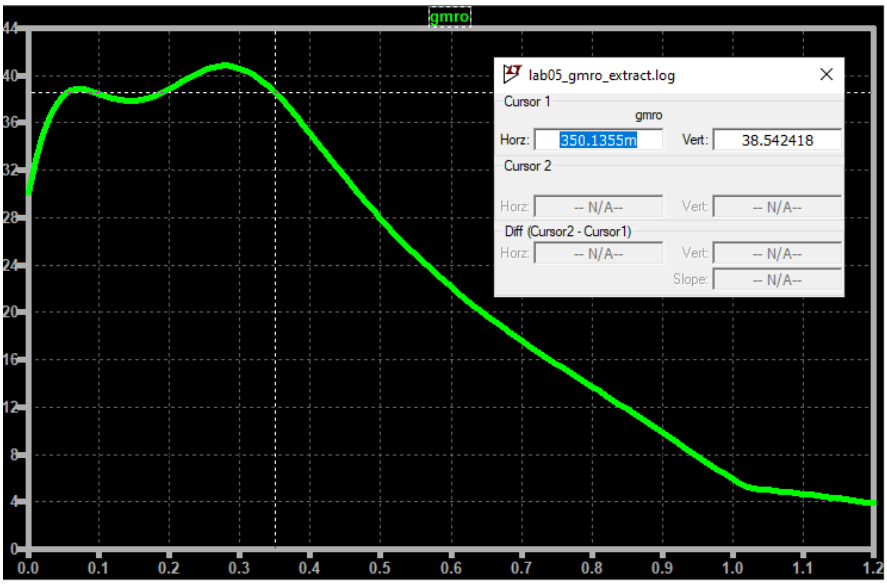


Figure 2.15 $g_m r_o$ vs V_{GS}

F. Extracting Transit Frequency (f_T)

The last important small-signal metric is the transit frequency f_T. *f_T is practically the measurement of the intrinsic speed of the transistor while it's not driving a load*. Higher f_T means it can support and deliver fast moving signals. From the lecture, a transistor has its own parasitic capacitances. In fact, the two most notorious parasitic capacitances are C_{gs} and C_{gd}. Figure 2.16 shows where C_{gs} and C_{gd} can be found in a transistor.

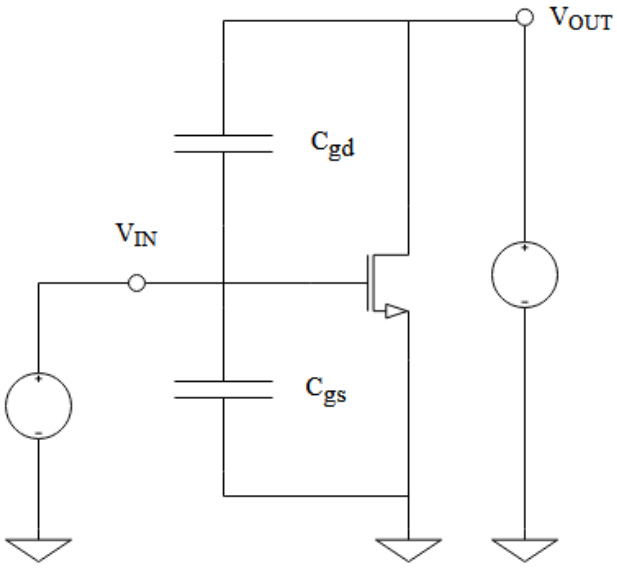
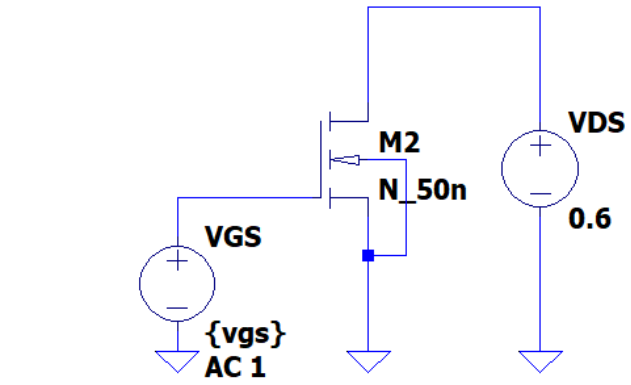


Figure 2.16 Depiction of C_{gs} and C_{gd}

Recall that the impedance of a capacitor is $Z_C = \frac{1}{j\omega C}$, then at frequencies $f \to \infty$ (or $\omega = 2\pi f \to \infty$) the impedances become short circuits: $Z_C \to 0$! If that happens then, it's as if V_{OUT}, V_{IN}, and ground are all shorted together! Imagine that C_{gd} and C_{gs} are short circuit wires. When this happens, we won't be amplifying anything at all. This becomes a motivation for defining the transit frequency f_T metric as the inherent maximum speed of our transistor because going faster would not work as an amplifier anymore.

There is a conventional definition for f_T and it might be difficult to appreciate or understand at first. For now, you'll have to accept this definition and it will become clear to you with further practice. *The standard definition of f_T is that it is the frequency in which the short-circuit AC current gain reaches unity*. Short-circuit AC current gain means the drain node is connected to ground in small-signal analysis. It is important that we are able to bias the transistor correctly while ensuring that the output node is connected to ground in the AC perspective. Figure 2.17 shows the circuit schematic that we will be using for measuring f_T. At a glance, it's the same as the characterization circuit in Figure 2.7 except Figure 2.17 is configured to run an AC analysis and measure f_T. We'll get back to Figure 2.17 in a bit but for now, let's appreciate what happens in AC.




```
.lib transistor_models.txt
.ac dec 10 1 10T
.step param vgs 0 1.2 0.01
.meas AC ft when mag(Id(M2)/Ig(M2))=1
```

Figure 2.17 Schematic for extracting f_T

Figure 2.18 shows the small-signal model of Figure 2.17. The drain is shorted to the source (let's treat the source as ground) because it is biased by an ideal voltage source V_{DS}. Moreover, r_o here can be ignored because it is in "parallel" to a short which has zero resistance (i.e. $r_o||0 = 0\Omega$). Stated in another way, current produced by $i_{out} = g_m v_{gs}$ favors the path of least resistance. Take note, i_{out} is defined as the current produced by $g_m v_{gs}$. This is consistent with the definition of our transistor, because any changes in the input produces some change in the output current I_{DS}. Lastly, current gain is defined as $\frac{i_{out}}{i_{in}}$ and the small-signal i_{in} comes from the AC input v_{in}.

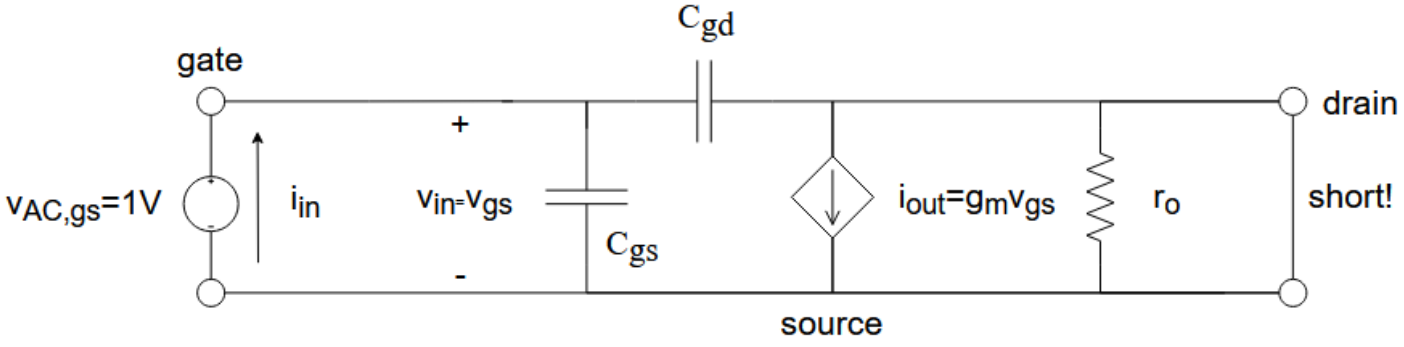


Figure 2.18 Small-signal circuit for Figure 2.17

We can derive $\frac{i_{out}}{i_{in}}$ from Figure 2.18. First, take the KCL at the gate node:

$$i_{in} = \frac{v_{gs}}{\frac{1}{sC_{gs}}} + \frac{v_{gs}}{\frac{1}{sC_{gd}}}$$

Recall that, $Z_C = \frac{1}{sC}$ so the $\frac{v_{gs}}{Z_C}$ terms are simply current. Re-arranging and collecting terms yields:

$$i_{in} = v_{gs} \cdot s\left(C_{gs} + C_{gd}\right)$$

Finally, take note that $i_{out} = g_m v_{gs} \rightarrow v_{gs} = \frac{i_{out}}{g_m}$. Substituting this and getting $\frac{i_{out}}{i_{in}}$ yields:

$$\frac{i_{out}}{i_{in}} = \frac{g_m}{s\left(C_{gs} + C_{gd}\right)}$$

The current gain $\frac{i_{out}}{i_{in}}$ is a function of frequency where $s = j\omega = j2\pi f$. Now, f_T is defined as the frequency in which the current gain is unity: $\frac{i_{out}}{i_{in}} = 1$. Taking the magnitude (the imaginary j term just disappears), yields:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}$$

Terrific! Now, we know that f_T is deterministic and we know what controls its value. Basically, the higher the g_m the faster our transistors are. However, increasing g_m usually involves setting the appropriate V_{GS}, and increasing the sizes. Doing so may affect the parasitic capacitance (i.e. increasing width and length increases C_{gs} and C_{gd}). This is where a trade-off comes in.

Let's simulate how f_T changes with changing V_{GS}. Do the following:

1. Open the schematic "lab05_ft_extract.asc".
2. Observe the following:
   - The input source is still using $v_{in,AC} = 1\ V$ same as what we had in the $g_m r_o$ extraction.
   - We're sweeping frequencies from 1Hz to 10 THz.
   - We're also parametrizing the DC V_{GS} values from 0 to 1.2 V. Same as the one in the $g_m r_o$ extraction.
   - We are measuring f_T with the .meas SPICE directive. Take note, this is $\frac{i_{out}}{i_{in}} = \frac{i_d}{i_g}$ because i_{out} is the small-signal drain current and i_{in} is the small-signal gate current.
3. Run the simulation.
4. Open the Error SPICE Log then plot f_T, you should get Figure 2.19.

Congratulations! You now know how to extract f_T! In the succeeding labs, we will just provide you with the circuit. Just be sure you know what needs to be fixed. For example, setting the appropriate widths, lengths, and the biasing inputs.

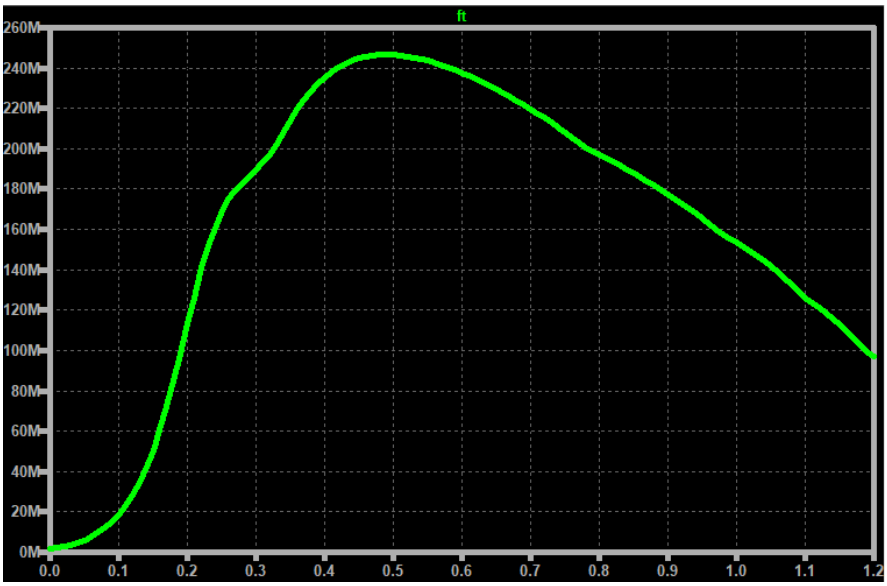


Figure 2.19 f_T vs. V_{GS} of Figure 2.17

This might be too much to take for such a short discussion; however, if you get let you need to accept these concepts first. They will become clear to you as you experience more of these in your future design. In this discussion, the key concepts are:

1. The parasitic capacitances limit the intrinsic speed of our transistor.
2. This is measured by f_T which is the frequency in which the short-circuit AC current gain reaches unity.
3. The mathematical definition of f_T is:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Part III: Exercise

A. Reinforcement Learning

Let's make sure you understood this lab module.

1. How would you differentiate large-signal (DC) vs. small-signal (AC) analysis?
2. How would you define transconductance g_m?
3. How would you define output impedance r_o?
4. How would you define small-signal gain $g_m r_o$?
5. Why is the input impedance infinite?
6. What is the importance of the inductor in Figure 2.11?
7. Why do we need to set AC = 1V for our AC analysis?
8. In Figure 2.11, how is v_{out} indicative of $g_m r_o$? In other words, why is measuring v_{out} equal to $g_m r_o$?
9. How would you define f_T?
10. How do we increase f_T?

B. PMOS Characterization Circuit

Let's see if you know how to use the pre-made schematics for you. You are given the following schematics:

- "lab05_pmos_char"
- "lab05_pmos_gmro_extract"
- "lab05_pmos_ft_extract"

With $W = 10\ um$ and $L = 1$um, Extract the following:

1. Reproduce the PMOS equivalent of Figure 2.8. Use $V_{SD} = 0.6\ V$. Show your plot and place a cursor showing g_m at $V_{SG} = 0.35\ V$.
2. Reproduce the PMOS equivalent of Figure 2.10. Use $V_{SG} = 0.35\ V$. Show your plot and place a cursor showing r_o at $V_{SD} = 0.6\ V$.
3. Reproduce the PMOS equivalent of Figure 2.15. Use $V_{SD} = 0.6\ V$. Show your plot and place a cursor showing $g_m r_o$ at $V_{SG} = 0.35\ V$.
4. Reproduce the PMOS equivalent of Figure 2.19. Use $V_{SD} = 0.6\ V$. Show your plot and place a cursor showing f_T at $V_{SG} = 0.35\ V$.

Part IV: Supplementary Reading / Exercises

Analog Circuit Design: The Black Magic

It is no doubt that analog design may be the most challenging task in integrated circuit design. It's not because the physics and math are heavy, but the number of trade-offs is unimaginable. In the discussion from Part II, we only had to discuss the trade-off between g_m and r_o. Though it was loosely discussed in Section F of part II, the V_{ov} plays an important role in indicating the maximum output swing. Ideally, we desire V_{ov} to be as small as possible so we can avoid having very small output swings. Remember, when $V_{DS} < V_{ov}$ or $V_{DS,sat}$ we start to operate at the linear region. The linear region has very small r_o compared to the r_o in saturation. This in turn reduces our output gain by a tremendous amount. The other problem is that if V_{ov} is chosen to be very small, this reduces the g_m as well. In order to compensate the loss, we tend to increase the width. Essentially, in our training we have three trade-offs: g_m, r_o, and V_{ov}. g_m is usually an indicate of the speed of our transistors. r_o is usually an indicator for gain. Finally, V_{ov} is usually an indicator for output swing. We can make a simple triangle trade-off as shown in Figure 4.1.

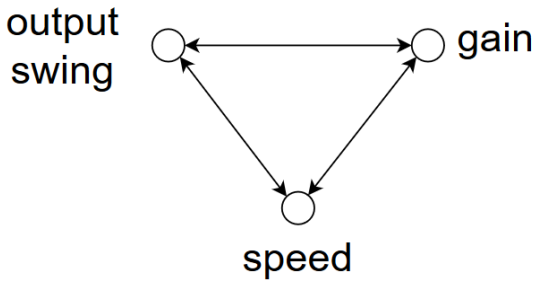


Figure 4.1 Simple trade-off

Figure 4.1 just shows 3 specs that we need to carefully decide. For example, it is desirable to have high gain and high output swing but this results in less speed. Wait! There's more. In practice, the true analog circuit design trade-off star is shown in Figure 4.2. This was taken from Razavi's book "Design of Analog CMOS Integrated Circuits", 2017. The star looks like it wants to summon black magic from an unknown dimension. Just kidding, but it's good to take time and appreciate this figure. In higher education courses (Master's or Ph.D.) you will get a chance to explore this. In this class, we'll mostly deal with power, output swing, gain, and speed only.

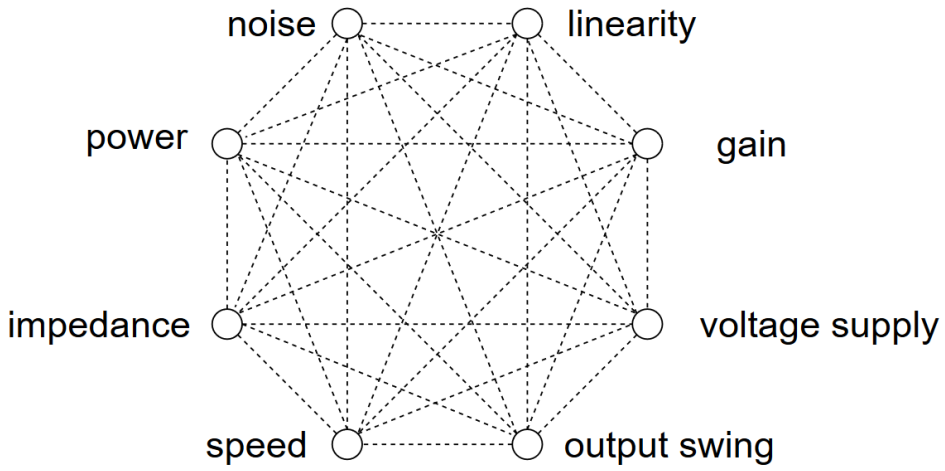


Figure 4.2 True analog circuit design trade-off star. From Razavi's "Design of Analog CMOS I.C."