University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 06 – Common Source with Current Source Loads, Common Drain, Transfer Impedance Concept

What will you learn from this lab?

- Analysis and design of CS amplifiers with current source loads
- Analysis and design of common drain (CD) amplifiers
- Appreciating the transfer impedance concept

A few reminders for any lab:

Each lab will always be broken down in 3 main sections

- Prelab/Review – this section can be treated like a "pre-lab" where you need to recall some of the previous concepts in your earlier courses or those that were discussed in the lecture.
- Training – this section guides you through a skill that you must learn. This could be a method in using the tool or a concept that is new to you.
- Postlab/Exercises – are some problems that you need to solve. Sometimes you need LTspice for it, and some don't. It's there for you to test what you have learned.
- Supplementary reading – these is an optional content but for the interested students, you can read and answer some of its questions. It's to further help you appreciate what IC design is.

There will be special boxes that you need to watch out for.

BLUE BOXES: Are used for useful notes and discussions. They can help you understand and appreciate the current topic at hand.

RED BOXES: Are notes that you need to watch out for. Some of these may be warnings that pertain to some limitations of our simulator. Or possibly some warnings on how to use particular circuit models.

GREEN BOXES: Are questions for that particular training task. They are also in the answer sheet so they'll be hard to miss.

Part I: Review

1. What is a common source amplifier?

Part II: Training

A. Intuitive Analysis of a Common Source Amplifier

Analog design always begins with the simple common source (CS) amplifier. Learning the tricks on how to conveniently analyze CS amplifiers can carry over to other types of amplifiers. Sometimes, we need to accept and appreciate how it works first, then the intuition becomes second nature to us. Consider Figure 2.1 which shows a simple common source amplifier with a resistive load.

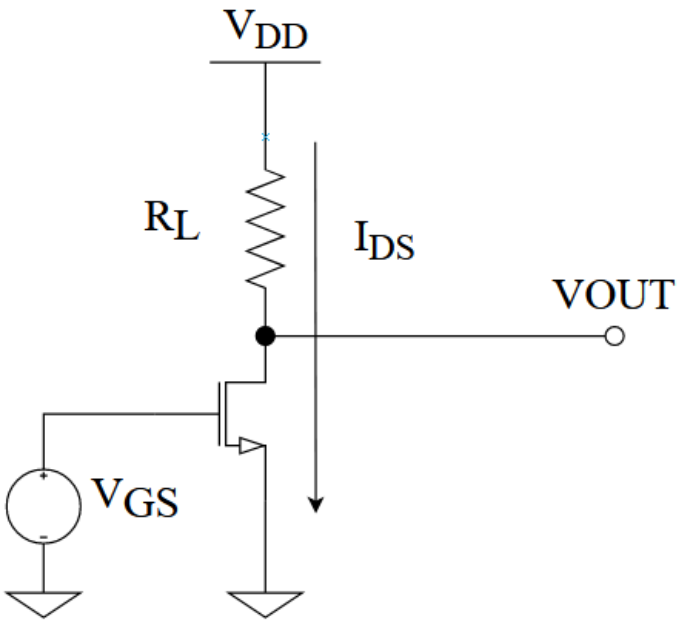


Figure 2.1 Common-source amplifier with drain node KCL

R_L is a resistive load because the task of the NMOS transistor is to drive a current on that load. Regardless of how the transistor is configured, we always ask ourselves *"Where does the current of the transistor go?"*. Alternatively, we can also ask *"What is the critical KCL node?"*. We'll see this kind of analysis in the succeeding labs. In Figure 2.1, the critical node would be the drain node. The KCL on the drain node is trivial:

$$I_L = I_{DS}$$

Where I_L, is the current that goes through the resistor. Therefore, a common source amplifier controls how much current can be delivered to its load. Since the NMOS controls how much current goes through R_L, then this also controls how our V_{OUT} moves. By KVL at the transistor's output, we can get:

$$V_{OUT} = V_{DD} - I_{DS}R_L$$

From the above equation, it is evident that as I_{DS} increases, the output decreases. This should be clear even when we look at Figure 2.1. When I_{DS} increases, then the voltage drop across the resistor increases. Therefore, by KVL, V_{OUT} decreases. Recall from the previous lab that the gain is defined as $\frac{\partial V_{OUT}}{\partial V_{IN}}$ and if we apply this to the above equation, we get:

$$A_v = \frac{\partial V_{OUT}}{\partial V_{IN}} = -\frac{\partial I_{DS}}{\partial V_{IN}} \cdot R_L$$

Remember, V_{DD} is a constant and therefore disappears after taking the derivative. We also know that $V_{IN} = V_{GS}$ leading to $\frac{\partial I_{DS}}{\partial V_{IN}} = \frac{\partial I_{DS}}{\partial V_{GS}}$. We also know that $\frac{\partial I_{DS}}{\partial V_{GS}} = g_m$ for a transistor. Hence, the gain:

$$A_v = \frac{\partial V_{OUT}}{\partial V_{IN}} = -g_m R_L$$

From the lecture, this is the ideal gain of a common source amplifier driving a resistive load. This is an ideal case because this holds true only if $r_o \gg R_L$. The $-g_m R_L$ gain is actually descriptive of how V_{OUT} changes with changing input. Recall that g_m is the rate of how much current our transistor produces for every small-signal increment of V_{GS} (or V_{IN}). Since the current across the resistor is $I_L = I_{DS}$, then the rate at which the voltage drops across R_L increases is $g_m R_L$ with increasing V_{IN}. Finally, since $V_{OUT} = V_{DD} - V_{RL}$ then it makes sense that V_{OUT} *decreases* at the rate of $g_m R_L$. This should lead us to a conclusion that $\frac{\partial V_{OUT}}{\partial V_{IN}} = -g_m R_L$. Make sure you got this descriptive definition of A_{Vv}. In summary, *the voltage gain of a common source amplifier is the product of the rate of how much current we are delivering to the load and the effective impedance (resistance) of the load itself.*

Since $g_m R_L$ is an ideal gain, the more accurate gain would be:

$$A_v = -g_m(r_o || R_L)$$

You might be wondering, where does the r_o factor kick in? From the previous lab, we know that the reciprocal of the output impedance describes the rate of change in the output current I_{DS} when V_{DS} is changing: $\frac{1}{r_o} = \frac{\partial I_{DS}}{\partial V_{DS}}$. This is known as the *output transconductance* ($g_{ds} = \frac{1}{r_o}$). Looking at Figure 2.1, we know that $V_{DS} = V_{OUT}$ and since V_{OUT} changes (becomes more negative but not decreasing) with increasing I_{DS} (increasing V_{IN}), then the effects of changing V_{DS} (because of changing V_{OUT}) affects the current. Observe: increasing V_{IN}, increases I_{DS}, and therefore manipulates $V_{DS} = V_{OUT}$. This change in V_{DS} also affects I_{DS} caused by the output transconductance and in turn limits how much of the real change in current affects the load R_L. *To put it simply, the change in I_{DS} is being shared between r_o and R_L.* Take time to internalize this paragraph.

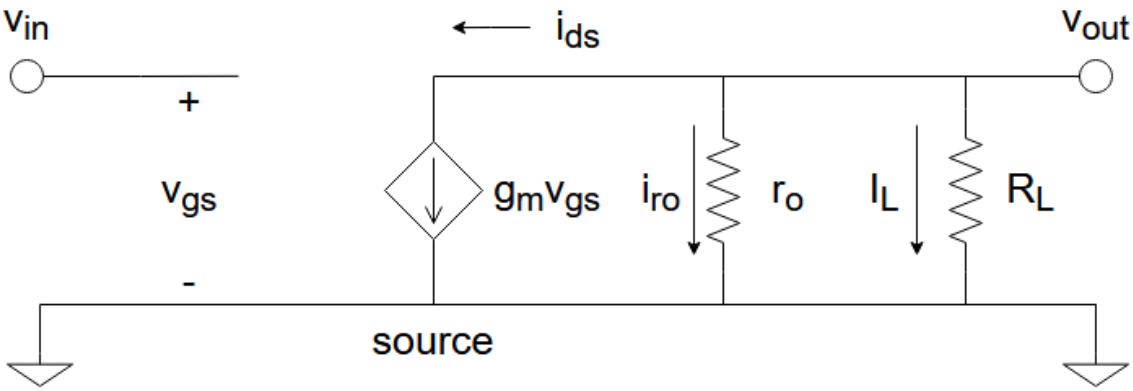


Figure 2.2 Small-signal model for the CS amplifier in Figure 2.1

Another perspective is to look at Figure 2.2 which shows the small-signal model for the CS amplifier in Figure 2.1. You should know how to recreate this circuit model from your lecture. Deriving the gain A_v is straight forward, first do a KCL on the drain node (v_{out} node):

$$i_{ds} + i_{ro} + i_L = 0$$

We can transform these currents into their voltage dependencies and get:

$$g_m v_{in} + \frac{v_{out}}{r_o} + \frac{v_{out}}{R_L} = 0$$

Combining terms and re-arranging yields:

$$g_m v_{in} = -\left(\frac{v_{out}}{r_o} + \frac{v_{out}}{R_L}\right) = -v_{out} \cdot \left(\frac{1}{r_o} + \frac{1}{R_L}\right)$$

Finally, knowing that $\frac{1}{r_o} + \frac{1}{R_L} = \frac{1}{(r_o||R_L)}$ and getting $A_V = \frac{v_{out}}{v_{in}}$ results in:

$$A_V = \frac{v_{out}}{v_{in}} = -g_m(r_o||R_L)$$

By now, you should be over-familiarized with the derivation of the gain. Let's step back a bit and re-analyze each equation. The KCL $i_{ds} = -i_{ro} + -i_L$ tells us that the current i_{ds} drives both i_{ro} and i_L. Essentially, i_{ds} is shared between i_{ro} and i_L making effective resistance that i_{ds} is driving to be: $(r_o||R_L)$. Therefore, the effective change in output voltage $v_{out} = -i_{ds} \cdot (r_o||R_L) = -g_m(r_o||R_L)$. $A_v = -g_m(r_o||R_L)$ tells us that as the current increases at the rate of g_m (because of increasing input v_{in}) the output v_{out} decreases at the rate of $-(r_o||R_L)$ (because of increasing i_{ds}). *Ultimately, gain is simply the rate of how the v_{out} changes for every unit of v_{in} which is the product of the rate of producing i_{ds} (that's g_m) for every unit of v_{in}, and the rate of producing v_{out} for every unit of i_{ds} $(that's\ (r_o||R_L))$.*

QUESTION (Q2.1):
Given some transistor configuration, what's the first thing we always ask?

QUESTION (Q2.2):
Using Figure 2.2 can you visually describe what happens when $r_o \gg R_L$, where does i_{ds} go and how does this translate to $A_v = -g_m R_L$? Explain thoroughly.

B. Simulating A CS Amplifier

Before we get into designing, let's first appreciate how a simple CS amplifier works. *You can't design anything without studying what needs to be designed*. Figure 2.3 shows a pre-built CS amplifier with $W = 10\ um$ and $L = 1\ um$. Let's also assume that we've pre-determined that $V_{GS} = V_{IN} = 0.35\ V$ and $V_{DS} = V_{OUT} = 0.6\ V$. First, let's extract our small-signal parameters g_m and r_o from our characterization circuit. Then we'll prove the consistency of our small-signal models and the analysis we've done earlier. Do the following:

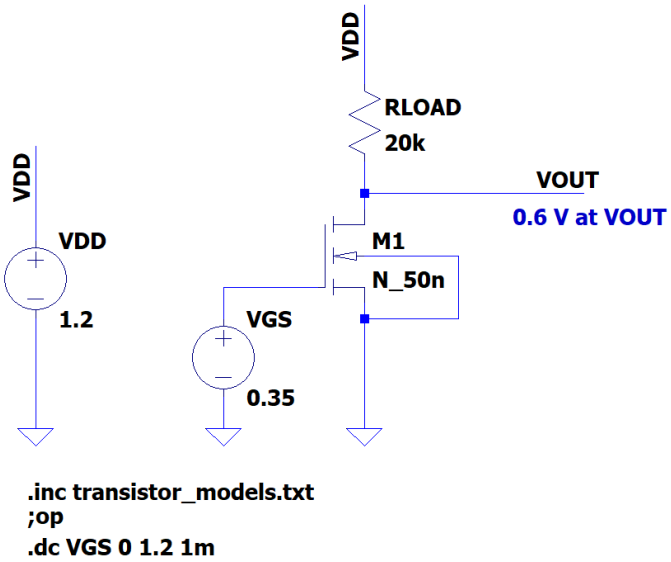


Figure 2.3 Simple CS amplifier schematic

1. Open your characterization circuit "lab06_nmos_char". This is the same schematic from the previous lab.
2. Make sure $W = 10\ um$ and $L = 1\ um$.
3. First extract I_{DS} when $V_{GS} = 0.35\ V$ and $V_{DS} = 0.6\ V$. You should get $I_{DS} \approx 30\ uA$.
   - You should know how to get this. Either sweep I_{DS} for changing V_{GS} or do a .op analysis.
4. Extract the g_m:
   - Set $V_{DS} = 0.6\ V$ because out $V_{OUT} = 0.6\ V$ (as seen in Figure 2.3)
   - Make a DC sweep for V_{GS} from 0 to 0.5 V. (It could've been up to 1.2V but we only needed $V_{IN} = 0.35\ V$)
   - Plot g_m and get the value when $V_{IN} = 0.35\ V$.
   - You should get a $g_m \approx 310\ uS$. This is shown in Figure 2.4.

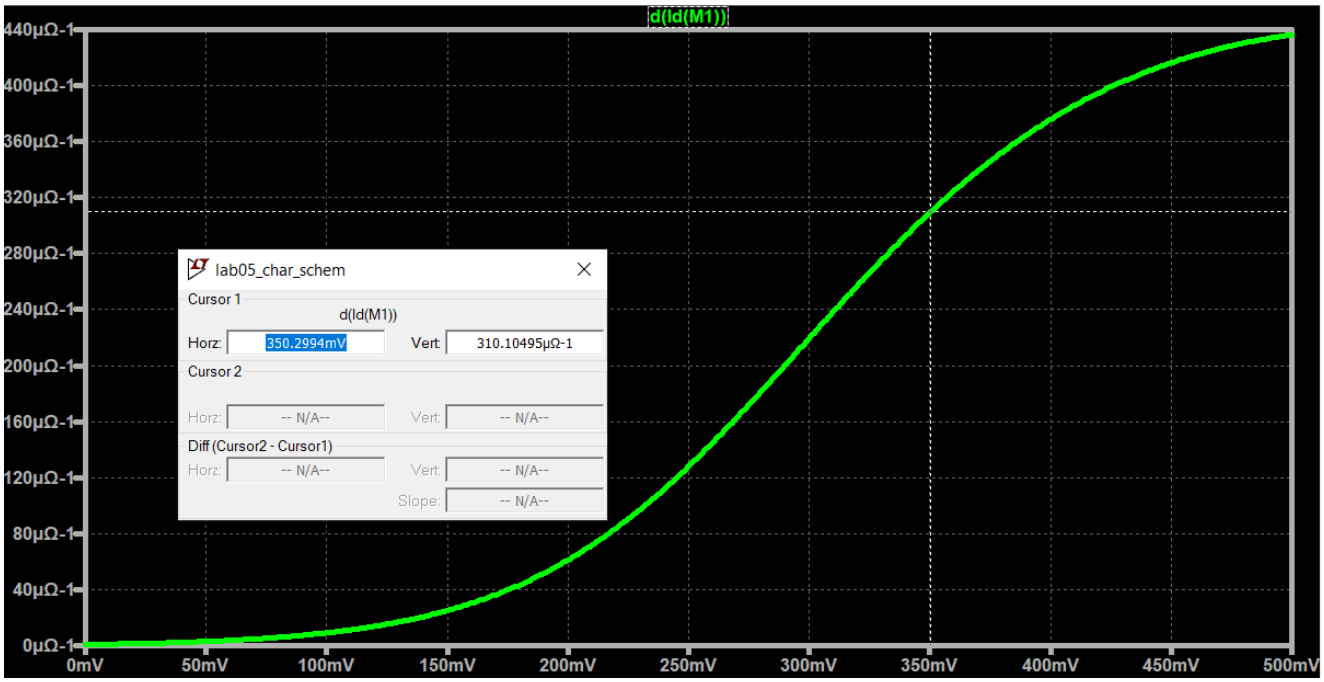


Figure 2.4 Extracting g_m when $V_{GS} = 0.35\ V$ and $V_{DS} = 0.6\ V$

5. Extract r_o:

- Fix $V_{GS} = 0.35\ V$ (this is our operating input) and sweep V_{DS} from 0 V to 1.2 V
- Plot r_o and get the value when $V_{DS} = 0.6\ V$.
- The r_o at $V_{DS} = 0.6\ V$ should be $\approx 125\ k\Omega$
- Figure 2.5 shows this.

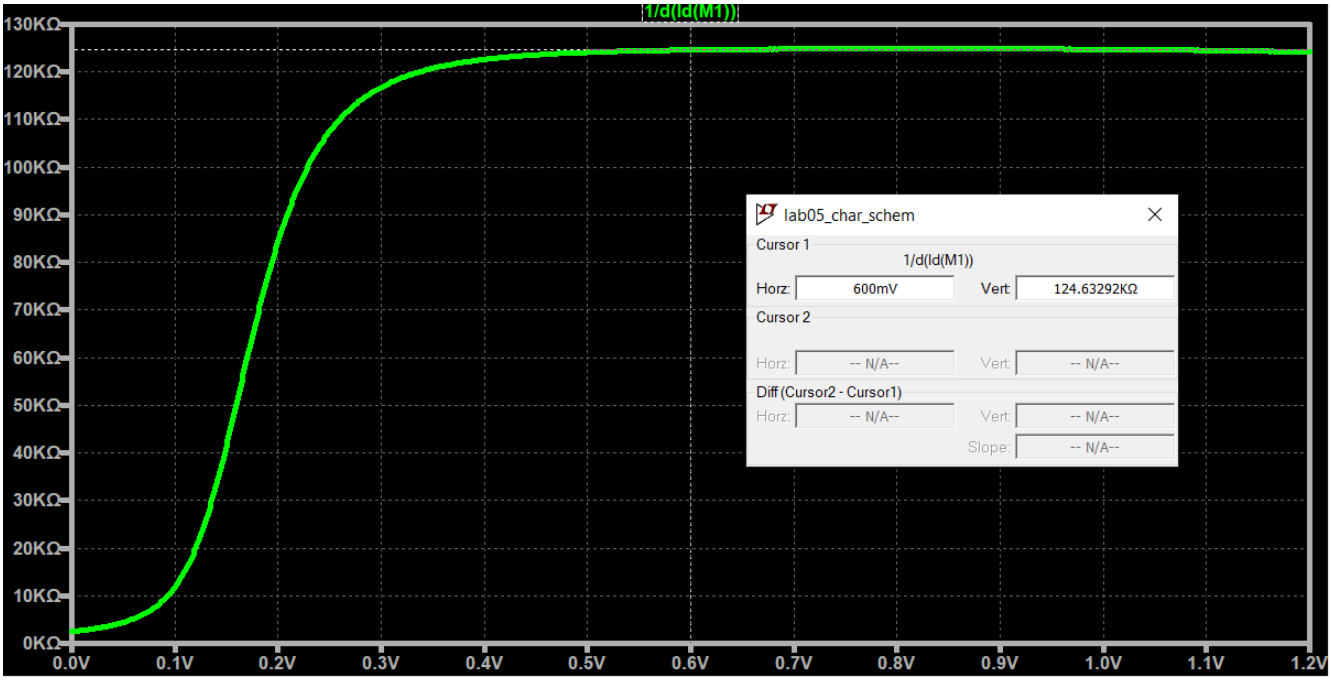


Figure 2.5 Extracting r_o when $V_{GS} = 0.35\ V$ and $V_{DS} = 0.6\ V$

Great! We now have $g_m = 310\ uS$ and $r_o = 125\ k\Omega$. Take note that we rounded the values to "nice" number for convenience. Now using the small-signal model in Figure 2.14, we can immediately calculate the gain. Such that:

$$A_v = -g_m \cdot (r_o || R_L)$$

Take note that r_o is not that high compared to R_L. In fact, $r_o || R_L \approx 17.24\ k\Omega$. That's significantly far from $R_L = 20\ k\Omega$. Therefore, $r_o || R_L \neq R_L$. Calculating the small-signal gain gives us $A_v = -310\ uS \cdot 17{,}240\ \Omega = -5.344$. Let's try to show this from the actual simulation. Do the following:

1. Open the schematic named "lab06_cs_amp.asc". This is the same schematic in Figure 2.3.
2. The circuit is already prepared for you so go ahead and run the simulation.
3. Plot V_{OUT} and I_{DS} on the same plotting plane. You should get Figure 2.6.

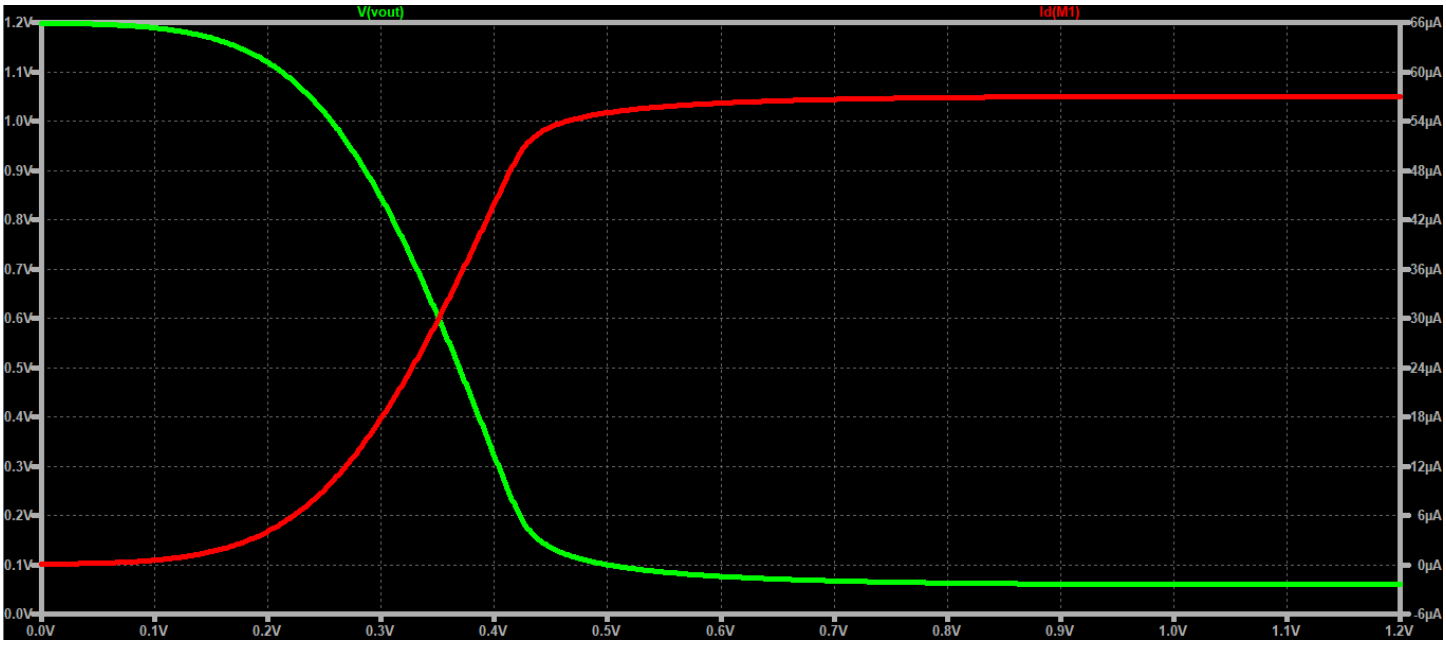


Figure 2.6 V_{OUT} and I_{DS} vs $V_{IN} = V_{GS}$

4. Let's do a quick analysis:
   - The curves are consistent with what we discussed in section A.
   - As $V_{IN} = V_{GS}$ increases, I_{DS} increases and V_{OUT} decreases. Easy!
   - Remember, the V_{OUT} curve follows the $V_{OUT} = V_{DD} - I_{DS}R_L$ equation.
   - Of course, I_{DS} follows the current equation:

$$I_{DS} = \begin{cases} 0, & V_{GS} < V_{TH} \\ \mu_n C_{ox} \cdot \frac{W}{L} \cdot [(V_{GS} - V_{TH})V_{DS} - V_{DS}^2], & V_{GS} \geq V_{TH} \text{ and } V_{DS} < V_{GS} - V_{TH} \\ \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}), & V_{GS} \geq V_{TH} \text{ and } V_{DS} \geq V_{GS} - V_{TH} \end{cases}$$

   - When the transistor is in the region (roughly): $0.28\ V \leq V_{GS} \leq 0.45\ V$, I_{DS} changes because both V_{GS} and V_{DS} are changing at the same time.

5. Let's plot the gain:
   - Remember, gain (A_v) is the change in V_{OUT} over the change in V_{IN}.
   - Add a plotting plane and plot the derivative of V_{OUT}: $d(V(vout))$
   - Place a cursor on both A_v and V_{OUT} when $V_{IN} = 0.35\ V$
   - You should get Figure 2.7.

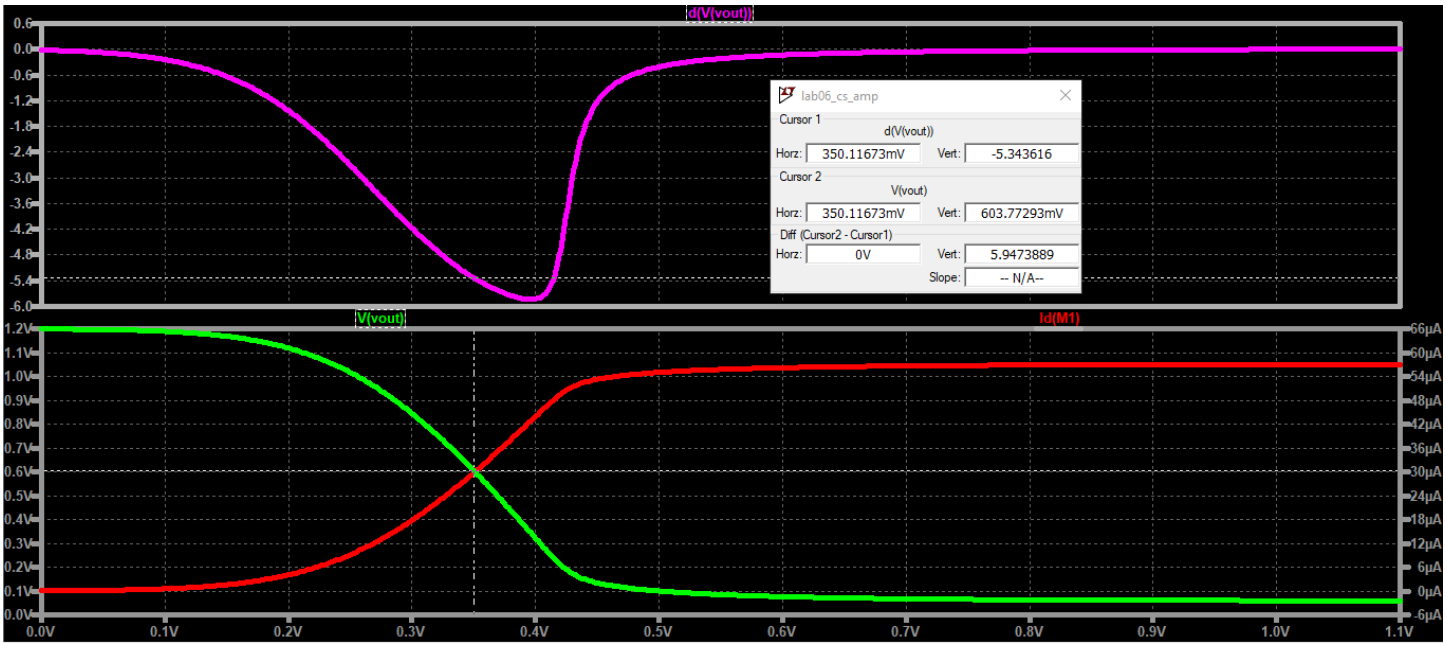


Figure 2.7 Gain (A_v) plot vs V_{GS}. When $V_{GS} = 0.35$ we have $A_v = -5.334$

Great! We have interesting results. First the gain we calculated is consistent with our simulation:

$$A_{v,calculated} = -5.344 \ V/V$$
$$A_{v,simulated} = -5.344 \, V/V$$

Next, the expected V_{OUT} and I_{DS} is accurate (you can change for I_{DS}):

$$V_{OUT} = 0.603 \, V$$
$$I_{DS} = 30 \, uA$$

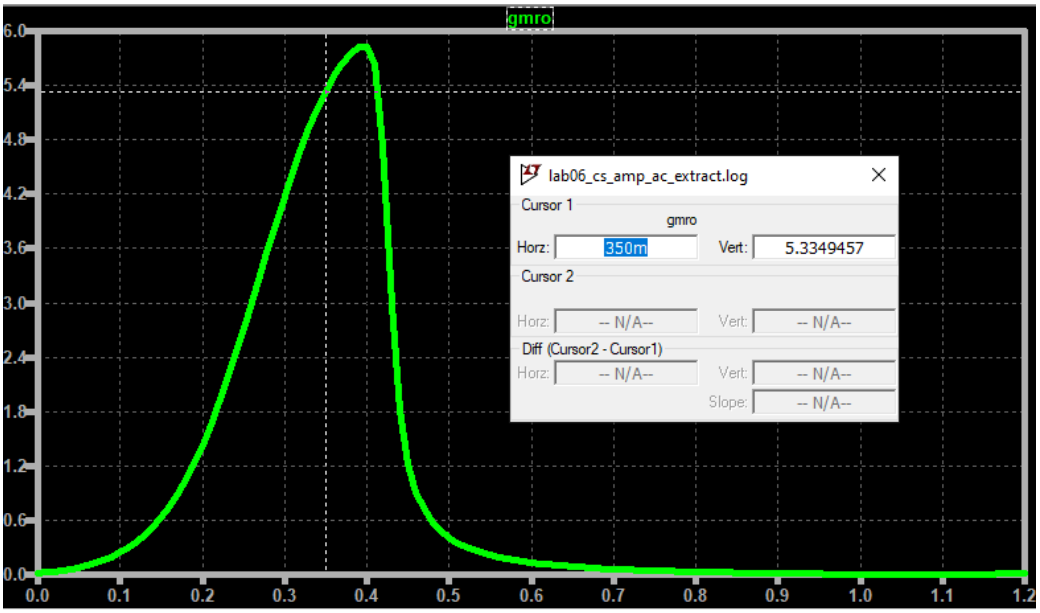
QUESTION (Q2.3):
What operating region is the transistor in when:

1. $V_{GS} < 0.28 \, V$?
2. $0.28 \, V \leq V_{GS} \leq 0.45 \, V$?
3. $V_{GS} > 0.45 \, V$?

Hint: Recall that $V_{THN} \approx 0.28 \, V$

DISCUSSION:
In the previous lab, we used an AC method of extracting the gain of the amplifier. We can actually do the same for the normal CS amplifier. Go ahead and open "lab06_cs_amp_ac_extract.asc" schematic. The setup is the same as the one we have in the previous lab. Observe the following:
1. The V_{GS} source's DC is set to a vgs variable and the AC voltage is set to 1.
2. We did a sweep of frequency from 1 – 100 Hz only, since we only need the DC range ($f \rightarrow 0$).
3. The .meas SPICE directive measure the output gain.

DISCUSSION (continued):
Run the simulation and plot the gain. You should get the same figure below and $A_v = 5.33$ when $V_{GS} = 0.35\,V$. Observe that the figure below is just the magnitude (hence absolute value) of the gain and it is the same curve in Figure 2.7 (top plot).



C. Alternative Analysis of the CS Amplifier

An alternative analysis of the CS amplifier can be derived by carefully dissecting the $A_v = -g_m R_L$ equation. Remember, $A_v = -g_m R_L$ *is an ideal case* because it only applies if and only if $r_o \gg R_L$. In reality, r_o may be comparable to R_L such that $r_o || R_L \neq R_L$. For now, let's assume $A_v = -g_m R_L$ for the sake of simplicity but do keep in mind this is an ideal gain. Let's also assume that we are maintaining our transistor in saturation. That means it satisfies $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$. Recall that:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) = \frac{2I_{DS}}{V_{GS} - V_{TH}}$$

$$V_{OUT} = V_{DD} - I_{DS} R_L \rightarrow R_L = \frac{V_{DD} - V_{OUT}}{I_{DS}}$$

Substituting these to $|A_v| = g_m R_L$ (let's ignore the negative sign for now):

$$A_v = \frac{2 \cdot (V_{DD} - V_{OUT})}{V_{GS} - V_{TH}}$$

Interestingly, this equation tells us that the gain improves when V_{OUT} and V_{GS} (or V_{IN}) decreases. Pretty cool right? Let's investigate this further.

Case 1: decreasing V_{GS}
Decreasing V_{GS} improves the gain based on the equation above. In fact, the math tells us that we can achieve $A_v = \infty$ if $V_{GS} = V_{TH}$ because $A_v = \frac{2\cdot(V_{DD}-V_{OUT})}{0} \rightarrow \infty$. However, this is does not really happen because as V_{GS} approaches V_{TH}, the square law equations become inaccurate and our original g_m equation won't hold true anymore. Moreover, setting V_{GS} to low sets V_{OUT} to high and it would defeat eventually bring A_v down.

Case 2: decreasing V_{OUT}
Decreasing V_{OUT} increases the $V_{DD} - V_{OUT}$ factor and thus making the gain larger. Though unlike the decreasing V_{GS} case, we can never reach an infinite value. Additionally, because $V_{DS} = V_{OUT}$ we can only set V_{OUT} to as low as $V_{DS,sat}$. Go any lower, and our transistor will operate in the linear region instead of the saturation region. That's a big no-no for this case. In some cases, there is a desired V_{OUT} voltage in case this CS amplifier is an input to another amplifier. If that happens, we have no choice but to set V_{GS} only. Controlling V_{OUT} is only possible by biasing the appropriate V_{GS}. Increasing V_{GS} decreases V_{OUT} but the derived gain equation tells us that this reduces the gain as well.

Ultimately, there is a sweet spot where an appropriate V_{GS} can produce the maximum gain. Looking at Figure 2.7 tells us that the highest gain for the CS amplifier occurs when $V_{GS} \approx 0.4\,V$. This leads to roughly around $A_v \approx 6$. This also results in a $V_{OUT} \approx 0.3\,V$. Small V_{GS} and small V_{DS} yields an optimally high again. There's another caveat to this analysis, the g_m and R_L terms were not really specified. In actual practice, there is a desirable g_m and R_L value. For example, some amplifiers require a minimum g_m to support the desired speed. Others need to drive a fixed R_L load. If a specific R_L is needed, then the current can be calculated from the voltages, and this current can be used to compute for the effective g_m (i.e. $g_m = \frac{2I_{DS}}{V_{GS}-V_{TH}}$). On the other hand, if a certain g_m is given (or required), the current can be computed from the desired V_{GS}, then compute the needed R_L to achieve the target V_{OUT} (i.e. $R_L = \frac{V_{DD}-V_{OUT}}{I_{DS}}$).

QUESTION (Q2.4):
Put on your thinking hat and try this out. A resistor-loaded NMOS common-source amplifier has a supply voltage of 1.2V. The nmos transistor was biased to achieve a $\frac{g_m}{I_{DS}} = 10\,V^{-1}$. Don't panic the V^{-1} is just the units for $\frac{g_m}{I_{DS}}$. What is $V_{GS} - V_{TH}$ assuming the transistor is a square-law device? What is the ideal gain that can be achieved if the output DC voltage is set at half of the supply? (Hint: use the equations! $\frac{g_m}{I_{DS}} = ???$).

The question above introduces the $\frac{g_m}{I_D}$ (Gee-ehm-ai-dee) metric which is a very useful spec for every analog designer. Take note, we'll interchange I_D and I_{DS} for now because the general term I_D also applies for PMOS transistors. From the fraction itself, it tells us how much g_m can we get for every unit of I_D. We can simulate this. Do the following:

1. Open the characterization schematic "lab06_nmos_char".
2. Maintain the input sweep of $0 \leq V_{GS} \leq 1.2$. Also, maintain $W = 10\,um$ and $L = 1\,um$.
2. Plot $\frac{g_m}{I_D}$ by plotting d(Id(M1))/Id(M1).
3. You should get Figure 2.8.

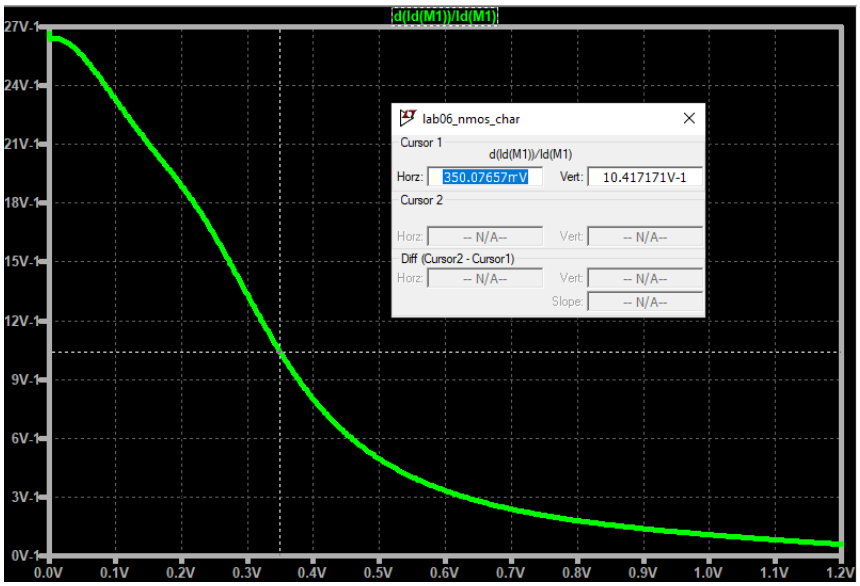


Figure 2.8 g_m/I_D plot

Analog designers use this metric to characterize power. The higher the $\frac{g_m}{I_D}$ the lower the power consumption because it only requires a few units of current to produce higher g_m! What's interesting is that at lower V_{GS} we actually gain higher g_m for every unit of I_D. Operating at $V_{GS} < V_{TH}$ is possible, and we call this the *sub-threshold region*. Even though our ideal square-law equations tell us that at $V_{GS} < V_{TH}$ we should have $I_D = 0$, technically it's just $I_D \approx 0$ but this small current is widely used for ultra-low power applications. One common example are watches. Keep this in mind!

Finally, $V_{GS} - V_{TH}$ can be computed from $\frac{g_m}{I_D}$ because $g_m = \frac{2I_D}{V_{GS}-V_{TH}}$ then $V_{GS} - V_{TH} = \frac{2I_D}{g_m}$. We also know that $V_{GS} - V_{TH} = V_{DS,sat}$ from the lecture slides. However, $V_{GS} - V_{TH}$ is generally known as the *over drive voltage* (V_{ov}) because it describes how much V_{GS} "over drives" V_{TH}. From here on, $V_{DS,sat} = V_{ov} = V_{GS} - V_{TH}$ will be interchangeable.

One more note, $\frac{g_m}{I_D}$ is independent of W and slightly dependent on L. *The slight dependence on L may cause some problems later on, but fret not,* $\frac{g_m}{I_D}$ *is just a measure of (1) efficiency and (2)* $V_{GS} - V_{TH}$.You can experiment on this by parametrizing width and length sweeps. We'll leave the experimentation to you to save up on time.

For the following questions, assuming $W = 10\,um$ and $L = 1um$ while $V_{DS} = 0.6\,V$

QUESTION (Q2.5):
What is $\frac{g_m}{I_D}$ when $V_{GS} = 0.3$? What about when $V_{GS} = 0.4$?

QUESTION (Q2.6):
What V_{GS} gives us $\frac{g_m}{I_D} = 20$? What about $\frac{g_m}{I_D} = 5$?

QUESTION (Q2.7):
What is the V_{ov} that gives us $\frac{g_m}{I_D} = 20$? What about $\frac{g_m}{I_D} = 5$?

DISCUSSION:

The $\frac{g_m}{I_D}$ concept may sometimes be misleading. It is true that higher $\frac{g_m}{I_D}$ implies we have a more efficient device because we get more g_m for every unit of I_D. However, higher $\frac{g_m}{I_D}$ is in the region when V_{GS} is really low. A low V_{GS} implies very low I_D and even though $\frac{g_m}{I_D}$ is 10, but because the I_D is extremely low, then we have very low g_m as well! Take for example, (using the characterization circuit) when $V_{GS} = 0.2\,V$ we have $\frac{g_m}{I_D} \approx 19\,V^{-1}$ and $I_D \approx 3.24\,uA$, this means we have $g_m \approx 61.56\,uS$. As opposed to the case when $V_{GS} = 0.35\,V$ we have $\frac{g_m}{I_D} \approx 10\,V^{-1}$ and $I_D \approx 16.45\,uA$ then, this results in $g_m \approx 164.5\,uS$. The g_m when $V_{GS} = 0.35\,V$ is still higher even though its $\frac{g_m}{I_D}$ is nearly half. *Analog designers often compensate the lack of current by increasing the widths*. Remember, $\frac{g_m}{I_D}$ is independent of W but $I_D \propto W$; therefore, if we up-scale the width to be $10\times$ more, then we would have (for the $V_{GS} = 0.2\,V$ case) $I_D \approx 32.4\,uA$ and $g_m \approx 615.6\,uS$. You can experiment on this using the "lab06_nmos_char.asc" schematic.

Using very low V_{GS} is an attractive biasing point because of its high $\frac{g_m}{I_D}$ ratio efficiency. However, *nothing comes for free*. A lower V_{GS} value translates to a very low transit frequency f_T. Remember, f_T is the measurement of the inherent speed of a transistor with $R_L = 0$. We can re-use the same schematic for extracting f_T in the previous lab. Feel free to run the schematic "lab06_ft_extract.asc". V_{GS} was swept from 0 to 0.6 V only because we're only really interested in $V_{GS} \leq 0.6\,V$. Go ahead and run the simulation then plot f_T. You should get Figure 2.9.

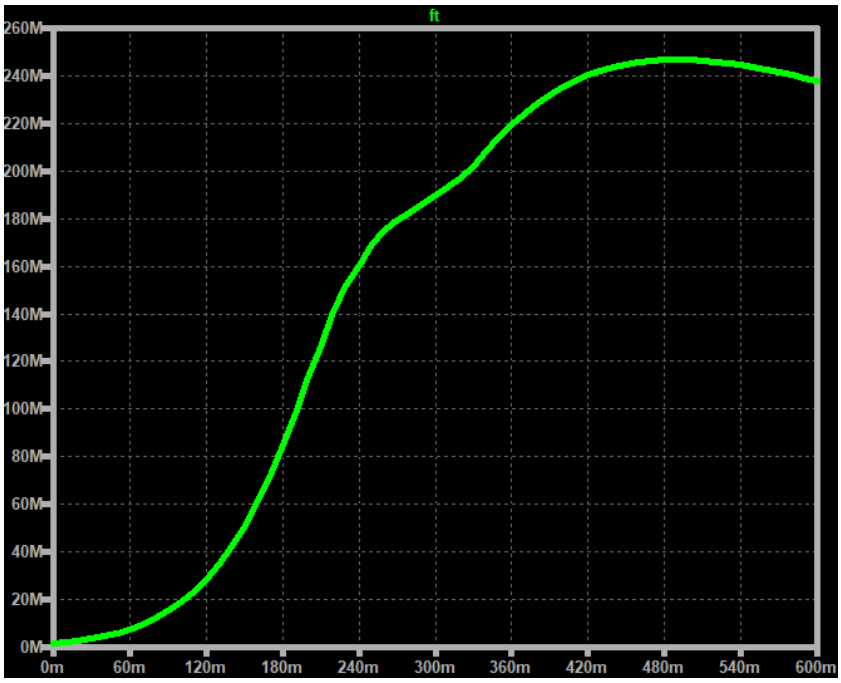


Figure 2.9 f_T vs V_{GS}

Figure 2.9 and Figure 2.8 evidently shows that $\frac{g_m}{I_D}$ and f_T are tradeoffs. Higher $\frac{g_m}{I_D}$ results in lower f_T and vice versa. At a glance, the best V_{GS} range would be in $0.3 \leq V_{GS} \leq 0.4$. Because of this, our succeeding labs will use a biasing point within the desired range. The most important lesson is that $\frac{g_m}{I_D}$ and f_T tradeoff each other.

WARNING:
For the sake of simplicity and learning, we'll use the designated range but in your succeeding courses, you might come across a different scenario. In fact, the *optimal* range is a few milli-volts short of the threshold voltage. We just need to peg into your design philosophies that $\frac{g_m}{I_D}$ and f_T tradeoff each other.

D. Sample Design of a CS Amplifier with a Resistor Load

Let's try to simulate how we would design a simple CS amplifier with a resistor load. Our design example will differ from what was simulated in Section B. Moreover, it may not be the optimal methodology but the process presented should be helpful for beginners. There may be concepts that might come as a surprise to you, but you will have to learn and accept them first. The reasons behind such design decisions will become clear to you with enough practice. Our goal is to emphasize on the design strategies and some things to watch out for.

Consider the following specs for a simple common source amplifier with a resistive load:

- Operating $V_{DD} = 1.2\ V$
- $V_{OUT} = 0.6\ V$ because we want the output to be half-way of V_{DD}.
- Use $V_{GS} = 0.32\ V$.
- The target A_v should be at least 84% of the ideal gain ($g_m R_L$)
- $g_m \geq 500\ uS$ we want our transistor to be at least this fast
- Begin with $W = 500\ nm$ and $L = 500\ nm$ and use multiples of $100\ nm$ if we need a larger size.

1. *Determine* $\frac{g_m}{I_D}$ *and* $V_{GS} - V_{TH}$

We usually begin by determining what $\frac{g_m}{I_D}$ we are using because it gives context on what type of amplifier we will be designing. Moreover, $V_{GS} - V_{TH}$ is easy to extract from $\frac{g_m}{I_D}$:

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{TH}} \rightarrow V_{GS} - V_{TH} = \frac{2}{\frac{g_m}{I_D}}$$

Using "lab06_nmos_char.asc", we can plot the $\frac{g_m}{I_D}$ when $V_{GS} = 0.32\ V$. Figure 2.10 shows that $\frac{g_m}{I_D} \approx 13\ V^{-1}$ while $W = L = 500\ nm$. Using the equation above tells us that $V_{GS} - V_{TH} = \frac{2}{13} \approx 0.1538$. Our effective $V_{GS} - V_{TH}$ is operating relative above the threshold region. Therefore, we're most likely designing a standard CS amplifier (i.e. not so power efficient and not too fast either).

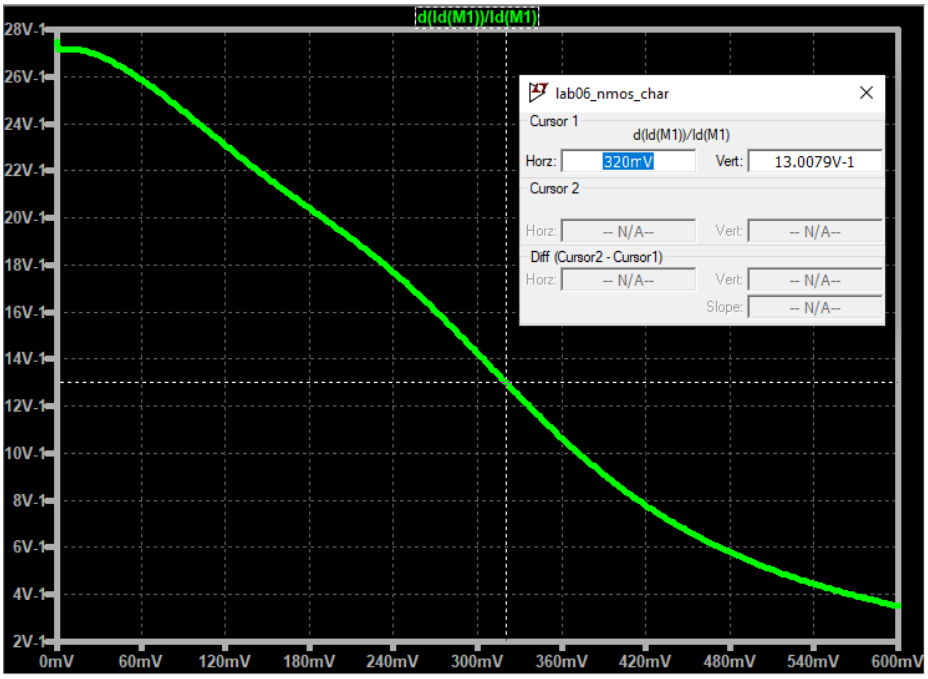


Figure 2.10 $\frac{g_m}{I_D}$ curve. When $\frac{g_m}{I_D} = 13\ V^{-1}$ we have $V_{GS} = 0.320\ V$

2. *Estimate the expected ideal A_v and compute the target minimum gain.*

It is useful to know the expected ideal results because it gives us insight of the limitations of our circuit. Again, the ideal gain ($g_m R_L$) is the "maximum" A_v that we can get if $r_o \gg R_L$. This will not be the case; however, the ideal A_v will be a stepping stone in determining how to size our transistor. From the specs, we know that $V_{OUT} = 0.6\ V$, $V_{DD} = 1.2\ V$, and the extract $V_{GS} - V_{TH} = 0.1538$. The ideal gain is then:

$$|A_{v,ideal}| = g_m R_L = \frac{2 \cdot (V_{DD} - V_{OUT})}{V_{GS} - V_{TH}} = \frac{2 \cdot (1.2 - 0.6)}{0.1538\ldots} = \frac{1.2}{0.1538\ldots} \approx 7.8$$

$A_v = 7.8$ if and only if $r_o \gg R_L$. Since we know that this may be difficult to achieve, the desired minimum gain should be at least 84% of the ideal gain. In other words, at the minimum: $g_m(r_o||R_L) \geq |A_{v,target}|$:

$$\left|A_{v,target}\right| \geq 0.84\left(A_{v,ideal}\right) \approx 6.552$$

3. *Calculate the target intrinsic gain $g_m r_o$*

Making sure we meet the minimum intrinsic gain $g_m r_o$ spec, guarantees us that we can get close to the minimum $|A_{v,target}|$. We can extract $g_m r_o$ from $g_m(r_o||R_L)$ because the math tells us that:

$$\left|A_{v,target}\right| = g_m(r_o||R_L) = g_m \cdot \left(\frac{1}{\frac{1}{r_o} + \frac{1}{R_L}}\right) = \frac{1}{\frac{1}{g_m r_o} + \frac{1}{g_m R_L}}$$

Since we have $\left|A_{v,target}\right| = g_m(r_o||R_L)$ and $g_m R_L$, we can easily compute the target $g_m r_o$:

$$g_m r_o \geq \frac{1}{\frac{1}{|A_{v,target}|} - \frac{1}{g_m R_L}} = \frac{1}{\frac{1}{6.552} - \frac{1}{7.8}} \approx 40.95$$

Let's set the minimum intrinsic gain to $g_m r_o \geq 41$. We'll use 41 for a nice number.

4. Size the length so that your transistor achieves the desired $g_m r_o$.
In general, we choose L to get the desired intrinsic gain $g_m r_o$. We can do this by re-using the $g_m r_o$ extraction schematic from the previous lab. Go ahead and open "lab06_gmro_extract.asc" then observe the following:

- Review the previous lab on how this circuit was setup.
- The AC sweep was only in the range of 1 Hz to 100 Hz because we're only interested in the DC gain.
- There's a .step SPICE directive for sweeping V_{GS}. Take note, that we're only interested in the range close to the desired V_{GS}. (i.e. $0.3 \leq V_{GS} \leq 0.4$)
- There's a .step SPICE directive for sweeping the length of the transistor. Observe that $W = 500\,nm$ and $L = \{500nm * k\}$.
- The .meas SPICE directive simply measures and saves the $g_m r_o$ data.

Go ahead and run the simulation and plot $g_m r_o$. Use the cursor and arrow keys to navigate and get $V_{GS} = 0.32\,V$ (use left and right arrow keys) and to a point where $g_m r_o \geq 41$ (use up and down arrow keys). If done correctly, you should get Figure 2.11 showing that at $V_{GS} = 0.32\,V$ and $L = 1.5\,um = 1{,}500\,nm$ we get $g_m r_o \approx 41.21$.

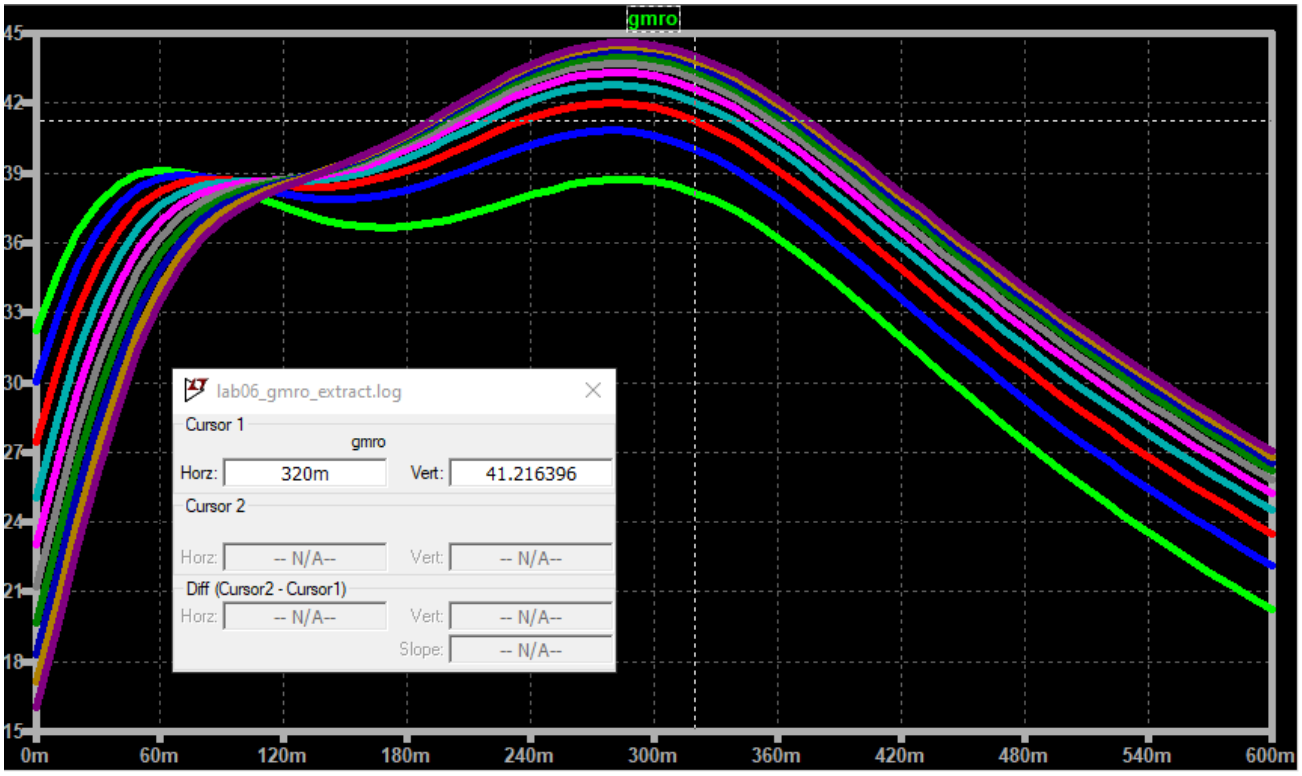


Figure 2.11 $g_m r_o$ vs V_{GS} curve while parametrizing L. $g_m r_o = 41.21$ when $L = 1.5\,um$ and $V_{GS} = 0.32\,V$.

DISCUSSION:

Here's an interesting trend, *the $g_m r_o$ does not change with W* or rather $g_m r_o$ has an insignificant change with changing W. Recall that:

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

$$r_o = \frac{1}{\lambda I_D}$$

Therefore:

$$g_m r_o = \frac{2}{(V_{GS} - V_{TH}) \cdot \lambda}$$

From here, there is no dependency on W. However, $\lambda \propto \frac{1}{L}$. We'll leave it up to you to look for the specific details why, but λ indicates the steepness of the channel length modulation. As L increases, λ decreases because the effects of channel length modulation diminish increasing the effective output impedance. Review your semiconductor physics if you need a refresher. This is why $g_m r_o$ is dependent on L but not on W. Moreover, you can experiment on this using the schematic "lab06_gmro_extract.asc". Simply fix $L = 500\ nm$ and set $W = \{500nm * k\}$. Run the simulations again and you should get Figure 2.12. Evidently, $g_m r_o$ does not change with W. *In summry, L is used to control the gain!*

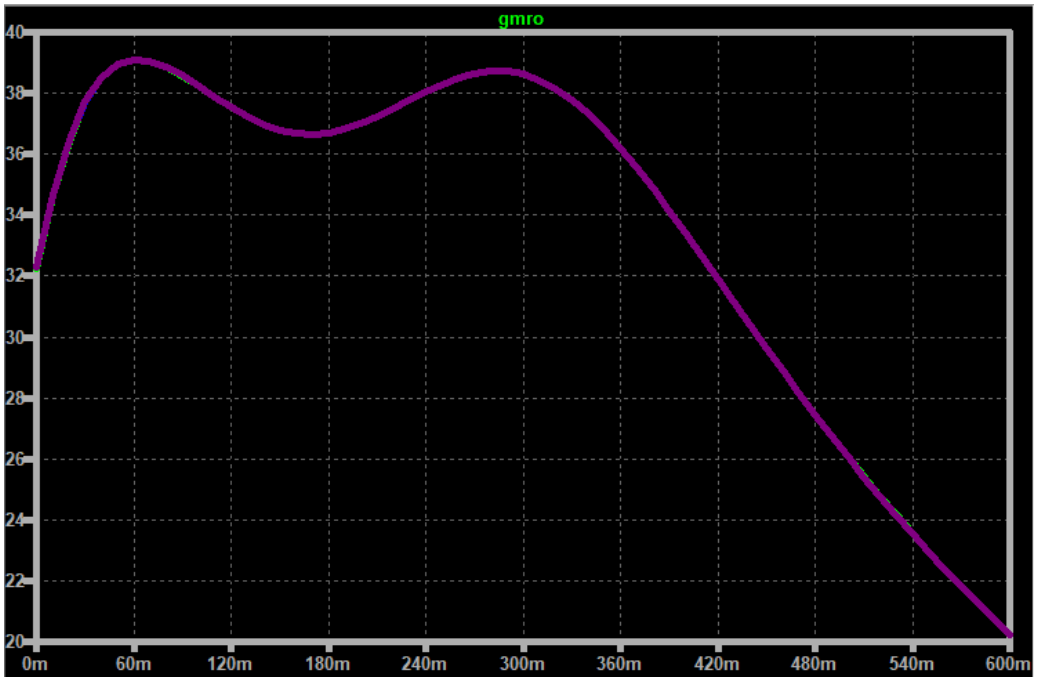


Figure 2.12 $g_m r_o$ vs. V_{GS} with W parameterized and $L = 500\ nm$. $g_m r_o$ does not change with W.

5. *Size the width to get the desired g_m.*

We choose W to get the desired g_m. First, we know that our starting size would be $W = 500\ nm$ and $L = 1.5\ um$ based on the characterization of $g_m r_o$. We can use "lab06_nmos_char.asc" to extract g_m and I_{DS} for this size and when $V_{GS} = 0.32\ V$. If done correctly (make sure the size is the same), you should get Figure 2.13.

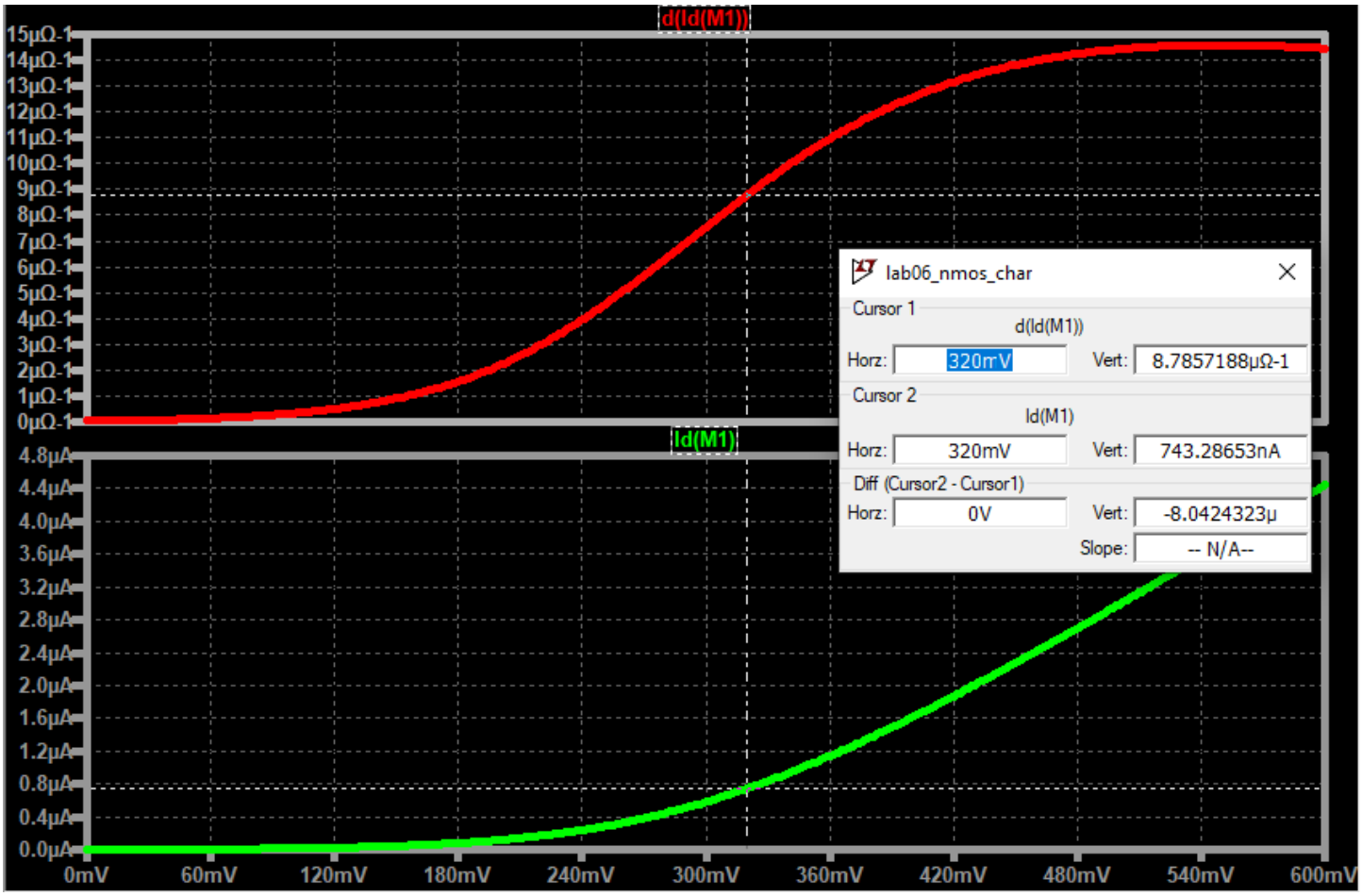


Figure 2.13 g_m and I_{DS} vs. V_{GS} curve. $g_m \approx 8.79\ uS$ and $I_{DS} \approx 743\ nA$ when $W = 500\ nm$ and $L = 1.5\ um$

Since, $g_m \approx 8.79\ uS$, we need to increase the W in order to achieve our minimum $g_m \geq 500\ uS$. Because $g_m \propto W$ then it's a matter of scaling, such that:

$$k_{W,multiplier} = \frac{g_{m,target}}{g_{m,have}} = \frac{500\ uS}{8.79\ uS} \approx 56.88$$

This means that our W needs to be 56.88 larger than the current $W = 500\ nm$ to get the minimum g_m. Therefore:

$$W_{new} = 500\ nm \cdot 56.88 = 28.44\ um \rightarrow 28.5\ um$$

We'll use $28.5\ um$ (round up) to maintain the "multiples of 100 nm" requirement and to have nice numbers. Plugging this into the "lab06_nmos_char.asc" results in Figure 2.14. $g_m \approx 510\ uS$ and $I_D \approx 43.22\ uA$. Great!

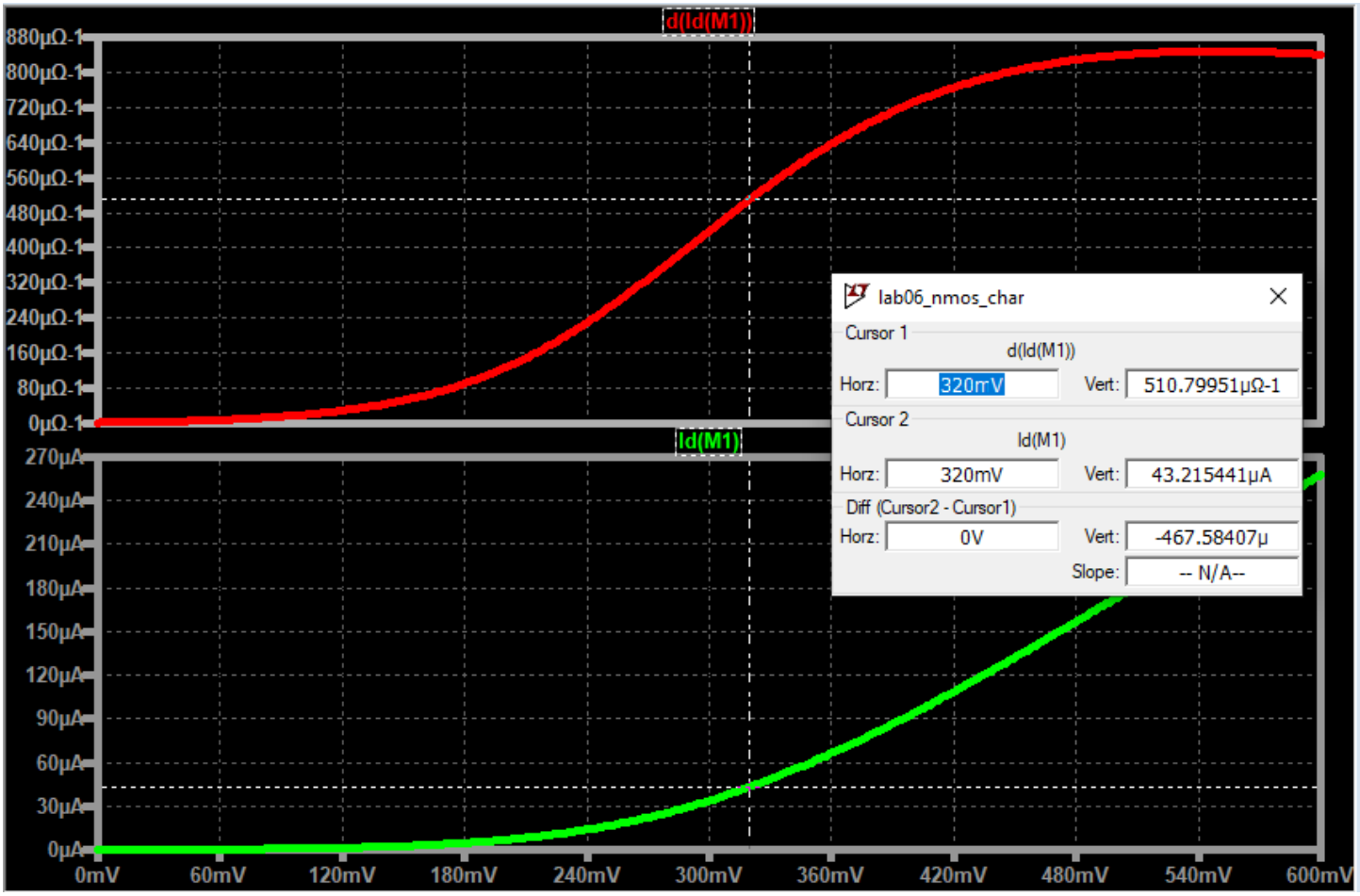


Figure 2.14 g_m and I_{DS} vs. V_{GS} curve. $g_m \approx 510\ uS$ and $I_{DS} \approx 43.22\ uA$ when $W = 28.5\ um$ and $L = 1.5\ um$

6. *Calculate the load resistance to support the desired V_{OUT}*

The load resistance is chosen to support the desired V_{OUT}. Recall that the R_L is computed by doing a KVL at the output:

$$V_{OUT} = V_{DD} - I_{DS}R_L \rightarrow R_L = \frac{V_{DD} - V_{OUT}}{I_{DS}}$$

Since we know from step #5 that $I_{DS} \approx 43.22\ uA$, then we have:

$$R_L = \frac{1.2 - 0.6}{43.22\ uA} = 13.883\ k\Omega$$

7. *Verify your design!*

Great we're, done! In summary our design needs to have:

- $V_{DD} = 1.2\ V$, $V_{OUT} = 0.6\ V$, and $V_{GS} = 0.32\ V$
- $W = 28.5\ um$ and $L = 1.5\ um$
- $g_m \geq 500\ uS$ and $I_{DS} = 43.22\ uA$
- $R_L = 13.882\ k\Omega$

Plug the W, L, V_{GS}, and R_L into the "lab06_cs_amp.asc" schematic and re-extract the output gain. Run the simulation and you should get Figure 2.15. Great!

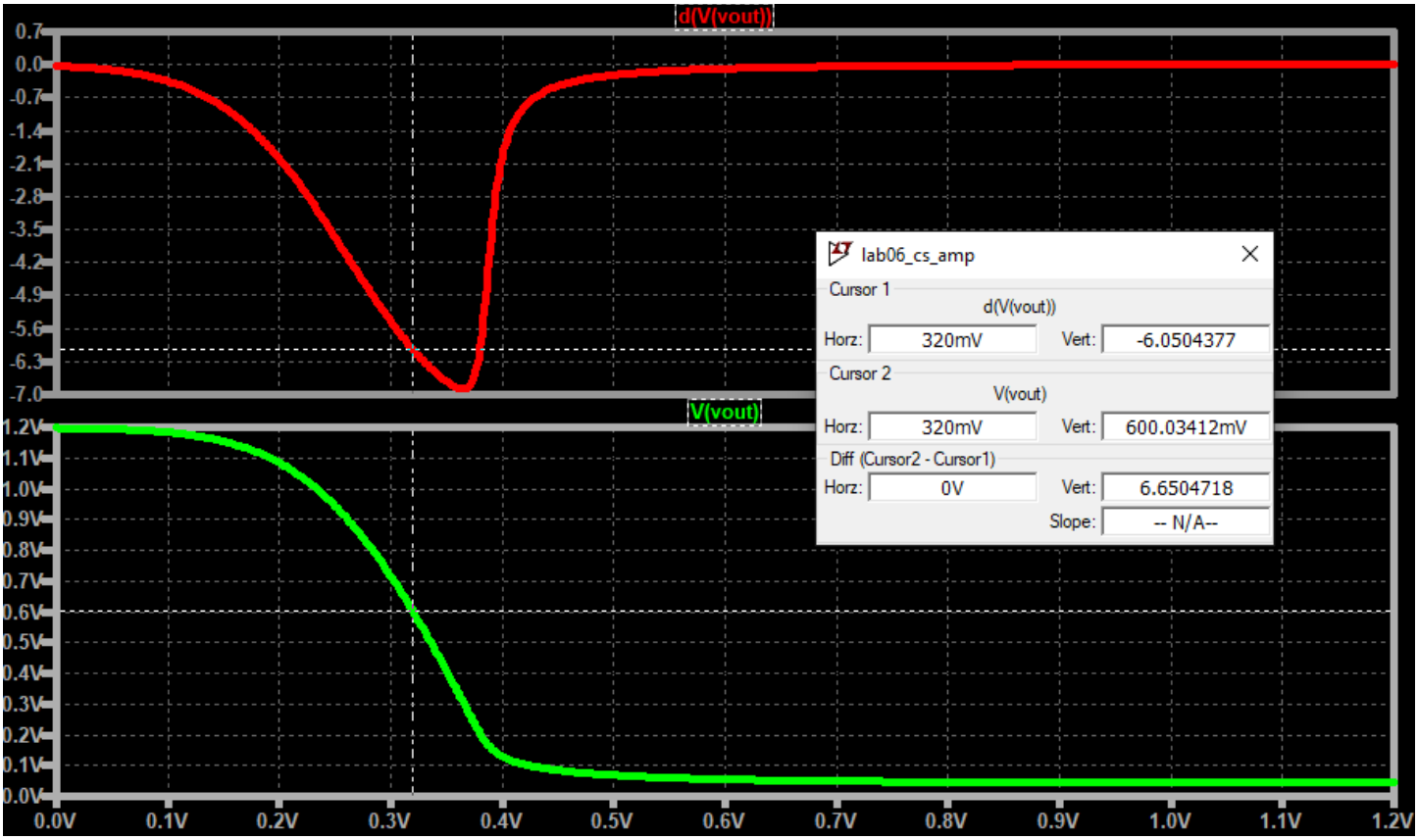


Figure 2.15 CS amplifier simulation with $W = 28.5\ um$, $L = 1.5\ um$, and $R_L = 13.882\ k\Omega$

First, the V_{OUT} is expected at $0.6\ V$. Obviously, this is trivial due to the chosen R_L. However, the actual $A_v = 6.05$ is less than the expected $A_{v,target} = 6.552$. We're a bit short of 0.5 extra gain. Don't panic, this is expected as well! The reason behind this is due to the $\frac{g_m}{I_D}$ and $V_{GS} - V_{TH}$ changing when we increased the lengths. If you re-extract $\frac{g_m}{I_D}$ with the current transistor size $W = 28.5\ um$ and $L = 1.5\ um$ (we'll leave it up to you how to do this), you should get: $\frac{g_m}{I_D} \approx 11.82$ which translates to $V_{GS} - V_{TH} = 0.1692$. Re-computing the $A_{v,target}$ using this $V_{GS} - V_{TH}$ results in:

$$|A_{v,ideal}| = \frac{2 \cdot (V_{DD} - V_{OUT})}{V_{GS} - V_{TH}} = \frac{2 \cdot (1.2 - 0.6)}{0.1692} = \frac{1.2}{0.1692} \approx 7.092$$

$$|A_{v,target}| \geq 0.84(A_{v,ideal}) \approx 5.957$$

Which proves that we did get the target gain if we use the actual $V_{GS} - V_{TH}$ we are using (i.e. $A_{v,actual} \geq A_{v,target} \rightarrow 6.05 \geq 5.957$). Hooray! Next time, just watch out for the $V_{GS} - V_{TH}$ parameter and expect it to change in the design process.

E. Recap Time!

Phew! That's a lot to take in but here's the summary of steps:

1. *Determine $\frac{g_m}{I_D}$ and $V_{GS} - V_{TH}$.*
   - We can infer the context of what kind of amplifier we are designing. (i.e. power efficient or fast).
   - The $V_{GS} - V_{TH}$ tells us how close and how far we are from sub-threshold.
2. *Estimate the expected ideal A_v and compute the target minimum gain.*
   - Getting the ideal A_v gives us a perspective of the maximum gain $g_m R_L$ that we can get for an ideal CS amplifier with a resistive load case.
   - The minimum gain is dictated by a fraction of how close do we want to achieve $g_m R_L$. The closer we are to the ideal, the more difficult it us.
3. *Calculate the target intrinsic gain $g_m r_o$.*
   - The intrinsic gain is a setup for us to characterize and size a single transistor. If we get this right, we're most likely to meet the overall spec.
4. *Size the length so that your transistor achieves the desired $g_m r_o$.*
   - Always remember that $g_m r_o$ is dependent on L but not on W. Or rather, effects are negligible when we change W.
5. *Size the width to get the desired g_m.*
   - Always remember that g_m is compensated by increasing W.
   - In the event that we need to increase L because we need to increase gain, the g_m decreases but we can re-increase it again by scaling W without disturbing the $g_m r_o$.
6. *Calculate the load resistance to support the desired V_{OUT}*
   - After getting the desired W to support the desired g_m we can use the transistor current to determine how much current goes to the load resistance.
   - The choice of the load resistance is for setting V_{OUT}.
7. *Verify your design!*
   - Always verify your design as a sanity check.
   - If your design does not meet the initial calculations, take a step back and review.
   - Watch out for cases like the changing $\frac{g_m}{I_D}$ whenever L changes.

Great! Consider this methodology as a starting point in your adventure to analog design. In the near future, there may be variations to this. It may be a good idea to experiment on your own, and look for limitations for this methodology. For example, if you've noticed, increasing L saturates the increase in $g_m r_o$. This is why we need to support it with auxiliary circuits that help boost our gain (to be discussed in the next labs). What we've presented is the CS amplifier only, but the concepts should still hold true for a common-gate (CG) and common-drain (CD). Lastly, practice makes perfect! Have fun!

Part III: Exercise

DIY: CS Amplifier with Resistive Load

Design your own CS amplifier with a resistive load for the following specs:

- $V_{DD} = 1V$
- $V_{OUT} = 0.5\ V$
- $V_{IN} = 0.36\ V$
- $g_m \geq 1\ mS$
- $A_{v,target}$ should be at least 87.5% of the ideal.
- Begin with $W = L = 500\ nm$ and final size should be in multiples of $100\ nm$ only.

Here are the steps as a guide:

1. Determine $\frac{g_m}{I_D}$ and $V_{GS} - V_{TH}$.
2. Estimate the expected ideal A_v and compute the target minimum gain.
3. Calculate the target intrinsic gain $g_m r_o$.
4. Size the length so that your transistor achieves the desired $g_m r_o$.
5. Size the width to get the desired g_m.
6. Calculate the load resistance to support the desired V_{OUT}
7. Verify your design!

Provide the following:

- Your thinking process for every step.
- Please provide sufficient plots and calculations that explains your design process.
- Highlight (bold, color, put in a table) your final transistor size, intrinsic gain $g_m r_o$, g_m, and actual gain.
- Be sure to provide your final gain plot similar to Figure 2.15.

Part IV: Supplementary Reading / Exercises

Real Engineers Read… A Lot!

Fundamentals are essential to us engineers. Read this article about how important fundamentals are especially when it comes to being a good engineer.