University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 07 – Answer Sheet

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Class: SATURDAY AM
SCORE: XX/40

Instructions:

This is answer sheet is a format only. You may answer using any word processor (i.e. Microsoft Word, Libre Office, Latek, Google docs … etc.) but you need to submit either a pdf or docx file so we can comment on it. Make sure to put your name, student number, and indicate what lab class you are in. This is given in the format above. Name your file "coe197_class_lastname_studentnumber". For the class write "satam" or "satpm" if you're in the morning or afternoon class, respectively. For example: "coe197_satam_antonio_201101474".

When you make your document please maintain the order of the main sections (PART I, PART II, PART III, and PART IV) and stick to the numbering provided in this answer sheet. You may use this word document if you like.

Answer with clear and concise solutions. Indicate your final answer (box it, bold it, change its color but please do not use red font color). For problems that require explanations, elaborate your thoughts. Any unclear answers will be marked wrong. There will be partial points.

Have fun and learn by heart!

Part I: Review (5 pts)

1. Draw a rough sketch of the $I - V$ curves of a resistor, a current source, a non-ideal current source, and a transistor. (4 pts.)

2. In simple terms, what does a current mirror do? (1 pt.)

- A current mirror takes a current, and then copies a fraction of the same current. Depending on the size of the transistor, we can "copy" fractions or multiples of a given current.

Part II: Training (10 pts)

Question Q2.1: (1 pt.)

Briefly explain why a current source load is better than a resistive load.

- An ideal current source load generally has infinite resistance. A non – ideal current source load has a very high resistance. Either way, since it provides a higher resistance, it can provide a higher gain.

Question Q2.2: (1 pt.)

When is the transistor "acting" like a good current source?

- A transistor acts as a good current source whenever it is in the saturation region.

Question Q2.3: (1 pt.)

How would we size a transistor such that it becomes a better current source?

- In the case of an NMOS common source amplifier with an active PMOS load, we size the PMOS transistor in a way that the current is ideally, equally distributed between the PMOS and NMOS r_o.

Question Q2.4: (2 pts.)

Theoretically, we could just have sized the PMOS to get $r_{op} \gg r_{on}$ (does not need to be infinite, just really large) and not worry about what r_{op} should be. In reality, analog designers don't go too far from r_{op} being just a few magnitudes higher ($2\times - 5\times$). Why do you think this is so?

- I think a PMOS with an r_{op} that is far higher than r_{on} has a very big size. This size usually does not give much of a difference compared to those with lower sized ones. It just takes up space.
- As we further increase r_o (by increasing L or decreasing W), the effective V_{out} changes. This way, the currents will also not be matched, and the gain will significantly decrease.
- For example, if we increase the length of the PMOS by just 0.1u, the required NMOS V_{GS} to obtain a 600mV output will just be approximately 338mV instead of 346mV.

Question Q2.5: (3 pts)

Let's see if you're paying attention. Consider Figure 2.16 showing a set of PMOS current mirrors. Similar to Figure 2.14, fill in the table below with the correct sizes such that we can achieve the desired output currents per PMOS device. The width and lengths are in multiples of 1 um. Answer in multiples of the base width and length.

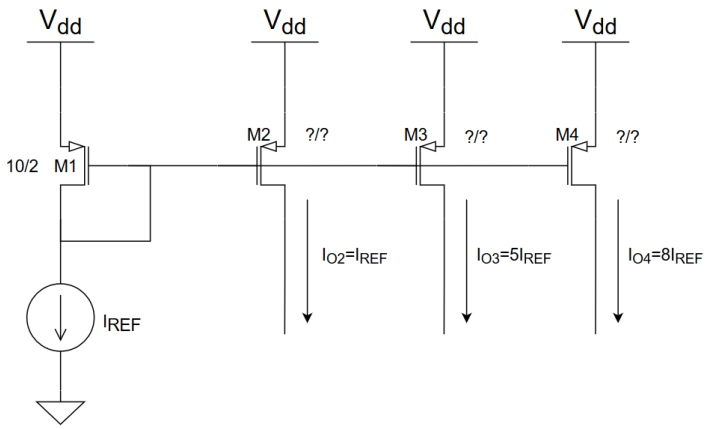


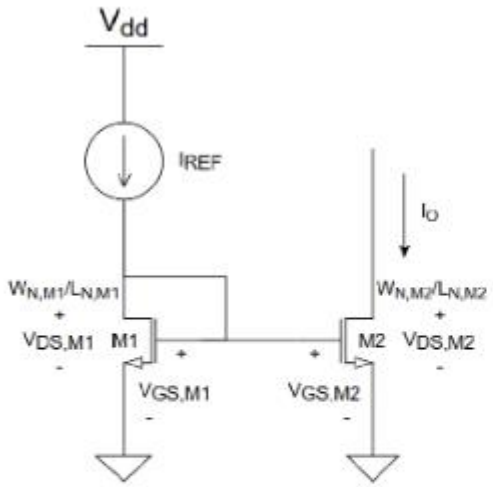
Figure 2.16 Set of PMOS current mirrors

Transistor	Width	Length
M1	10	2
M2	50	2
M3	80	2

Question Q2.6: (2 pts)

Re-derive equation (5) again but this time, include the effects of channel length modulation. In other words, include the $(1 + \lambda V_{DS})$ terms. Be sure to add the current subscripts for each transistor.

Consider the current mirror shown below.



For any long - channel NMOS,

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Solving for V_{GS} in terms of I_{DS},

$$V_{GS} = \left(\frac{I_{DS}}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(1 + \lambda V_{DS})}\right)^{\frac{1}{2}} + V_{TH}$$

Notice that $V_{GS,M1} = V_{GS,M2}$. If the transistors have the same mobility μ_n, gate-oxide capacitance C_{ox} and threshold voltage V_{TH},

Since $I_{DS,M1} = I_{REF}$ and $I_{DS,M2} = I_O$,

$$\frac{I_{REF}}{\frac{W_1}{L_1}(1 + \lambda_1 V_{DS,1})} = \frac{I_O}{\frac{W_2}{L_2}(1 + \lambda_2 V_{DS,2})}$$

Finally,

$$I_O = I_{REF} \cdot \frac{\frac{W_2}{L_2}(1 + \lambda_2 V_{DS,2})}{\frac{W_1}{L_1}(1 + \lambda_1 V_{DS,1})}$$

If both transistors are sized in a way that they have the same lengths, then,

$$I_O = I_{REF} \cdot \frac{W_2(1 + \lambda V_{DS,2})}{W_1(1 + \lambda V_{DS,1})}$$

Part III: Exercise (15 pts)

Don't You Hate Ladder Problems? ☹

Suppose you were tasked to design a CS amplifier with the following specs:

- It needs to drive a transistor load as a current source
- The gain must be $A_V \geq 25$
- The speed of your amplifier must be $g_{mn,} \geq 1\ mS$
- For simplicity, let's choose $V_{GSN} = 0.35\ V$, $V_{SGP} = 0.35\ V$, and $V_{OUT} = 0.6\ V$
- Start with $W = 500\ nm$ and $L = 500\ nm$ and use multiples of $100\ nm$ for widths and $500\ nm$ for lengths.
- For simplicity, we let $L = 5\ um$ be the maximum length for both NMOS and PMOS.

Do the steps that was taught to you. Show your solution for each step. If you need to provide plots for clarity, feel free to do so.

1. Calculate the r_{op} and r_{on} that gives the minimum ($r_{on}||r_{op}$). (2 pts)

$A_v \geq 25,\ g_{mn} \geq 1mS.$

We can start with $r_{on} = r_{op}$ so that $r_{on}\|r_{op} = \frac{1}{2}r_{on}$.

Thus, $A_v = \frac{1}{2}g_{mn}r_{on}$

Obtaining r_{on}, we get $r_{on} = \frac{2A_v}{g_{mn}} = 50k\Omega = r_{op}$.

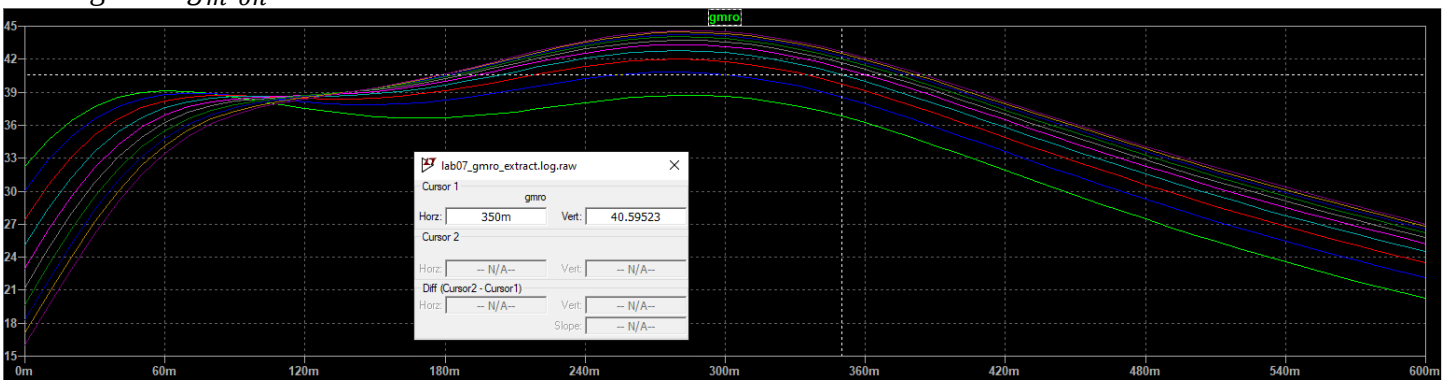
2. Determine the L_N that gives the minimum $g_{mn}r_{on}$.

- *In the event that we can't reach the minimum $g_{mn}r_{on}$ due to device limitations of the NMOS transistor, we need to re-calculate the desired r_{op} for the chosen $g_{mn}r_{on}$.* (3 pts)

Since $r_{on} = 50k\Omega$ and $g_{mn} \geq 1mS$,

$g_{mn}r_{on} \geq 50$, and the minimum $g_{mn}r_{on} = 50$

From the plot, we can see that $g_m r_{on}$ saturates at 45 as we further increase the lengths. We then choose L = 2nm which gives a $g_m r_{on} = 40.6$.

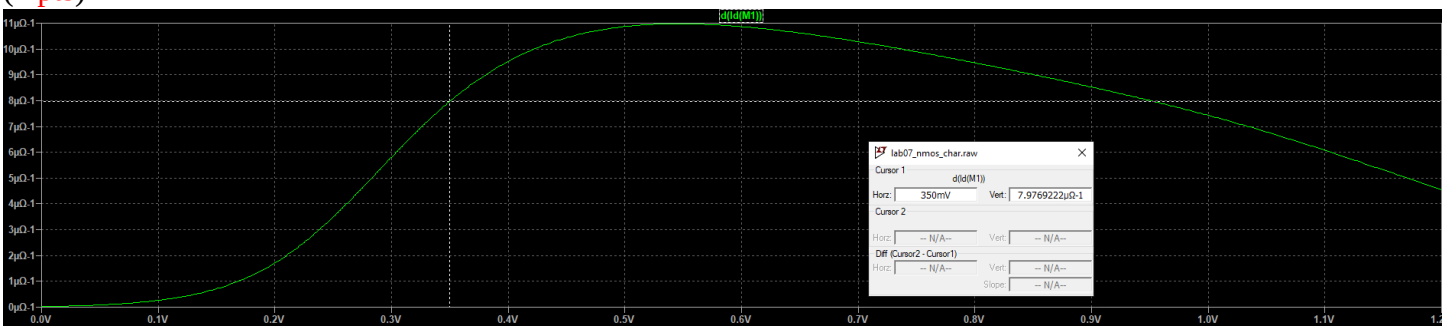


We know that $A_v = g_{mn}(r_{on} \| r_{op})$

Thus, $\frac{1}{g_{mn} r_{op}} = \frac{1}{A_v} - \frac{1}{g_{mn} r_{on}}$

Solving for r_{op} we get $r_{op} = 65.064k\Omega \approx 65k\Omega$

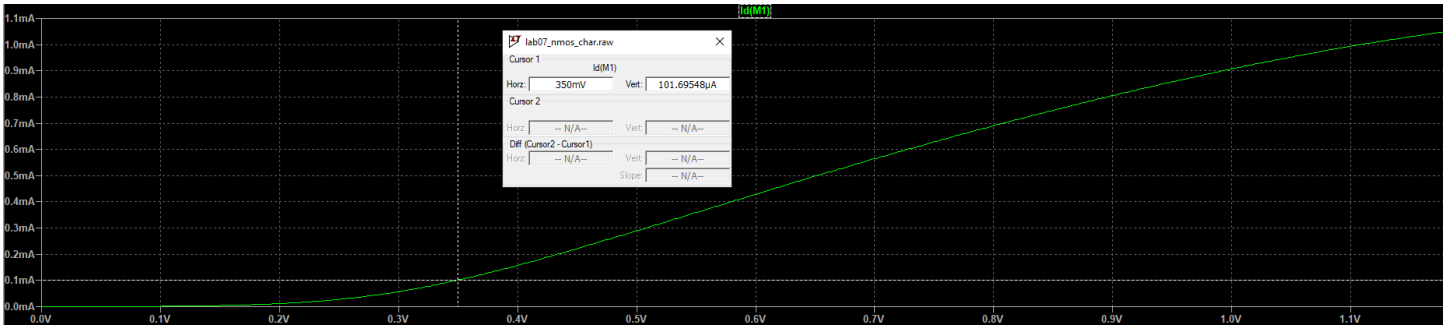
3. Using the chosen L_N in step 3, size W_N such that we get the minimum g_{mn}. Also, determine the operating I_{DN}. (2 pts)



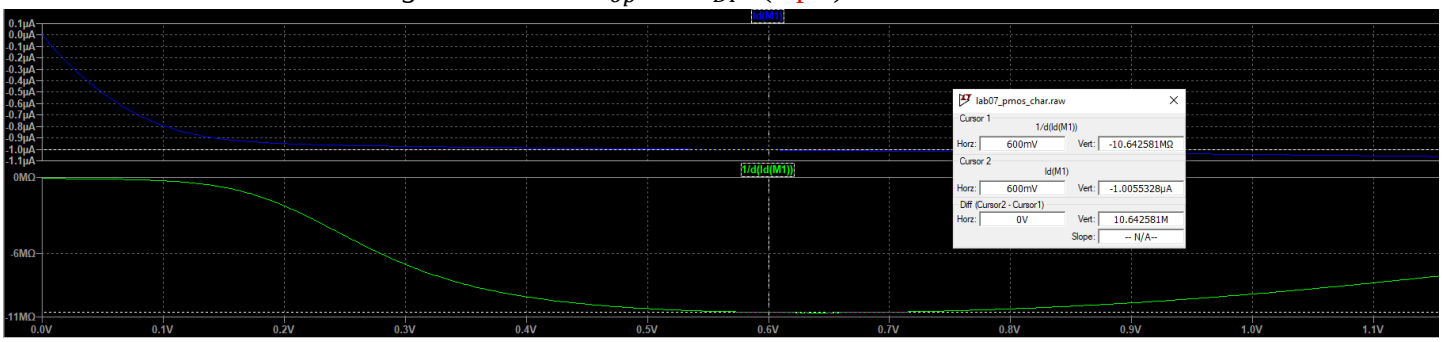
At L = 2um and W=500nm, $g_{mn} \approx 8uS$.

$$k_{multiplier} = \frac{1mS}{8uS} = 125$$

$$W_N = 62.5um,\ I_{DN} = 101.7uA$$



4. Size the PMOS such that we get the desired r_{op} and I_{DP}. (3 pts)

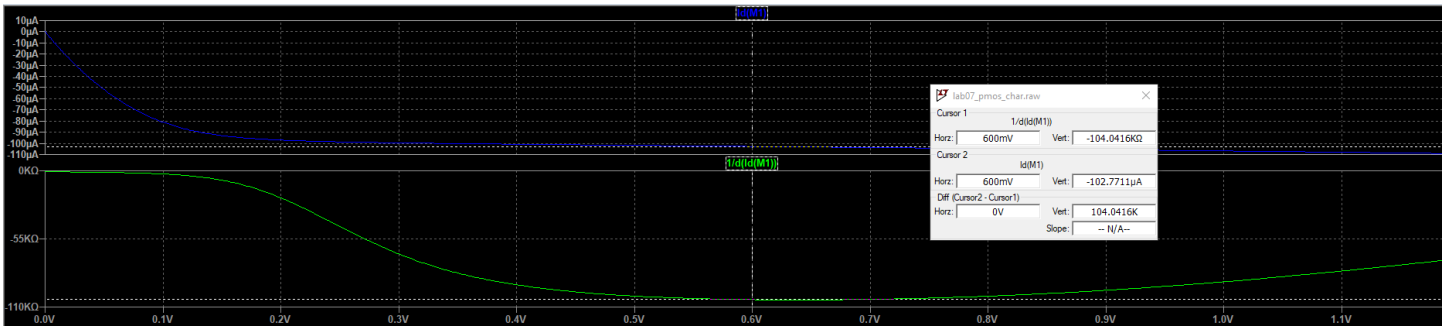


We want $I_{DN} = I_{DP} = 101.7uA$

$$k_{multiplier} = \frac{101.7uA}{1uA} = 101.7$$

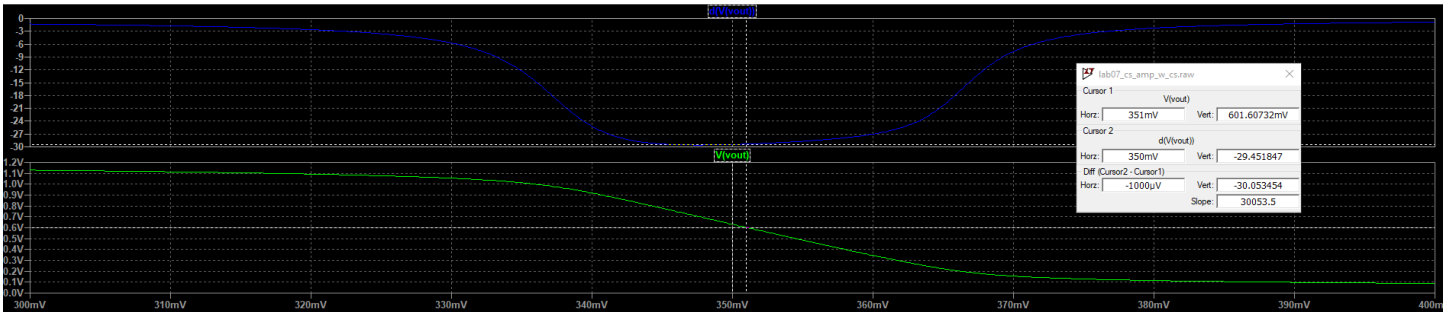
$$W_P = 101.7 \cdot 2um = 203.4um$$

Recalculating r_{op} with W = 203.4um and L = 2um gives, $r_{op} = 104k\Omega \geq 65k$.
Which is what we wanted.



5. Verify your design! (3 pts)

- Re-use "lab07_cs_amp.asc"
- Show a plot similar to Figure 2.12. Make sure to show via cursors what A_v is when $V_{GS} = 0.35\,V$ and what V_{GS} is when $V_{OUT} = 0.6\,V$.



As we can see, $V_{out} = 0.6V$ when $V_{GS} = 351mV$. This is close to what we simulated. $|A_v| \approx 29$ at $V_{GS} = 350mV$.

6. Suppose we want to replace the PMOS current source with a PMOS current mirror that is biased by $I_{BIAS} = 10\ uA$. The case is similar to Figure 2.20. (2 pts)

- How would you size the biasing transistor? Show a plot of the new A_v and V_{OUT}.
- Make sure to show via cursors what A_v is when $V_{GS} = 0.35\ V$ and what V_{GS} is when $V_{OUT} = 0.6\ V$.
- Feel free to re-use "lab07_cs_amp_w_cm.asc"

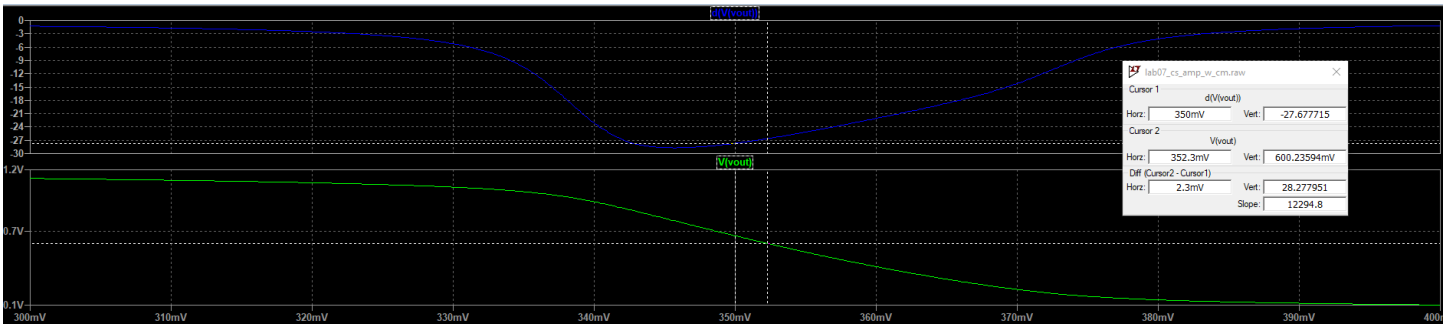
We design the biasing transistor such that they have the same lengths but their widths follow the ratio

$$\frac{W_P}{W_{REF}} = \frac{101.7\mu}{10\mu} = 10.17$$

The biasing transistor should have a width that is 10.17 times smaller than the width of the active PMOS load.

$$W_{REF} = \frac{203.4\mu m}{10.17} = 20\mu m$$

Note that the biasing transistor is the same as the reference transistor.



At $V_{out} = 600mV, V_{GS} = 352.3mV$ this is higher than what we used to simulate.

The gain A_v at $V_{GS} = 0.35$ is ≈ 28. This is still desirable.

The values computed here are different from what we calculated because we did not account that much for channel length modulation. Overall, the output of the circuit is still what we desired.