University of the Philippines
Microelectronics and Microprocessors Laboratory

Lab Module 06 – Answer Sheet

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Class: SATURDAY AM
SCORE: XX/40

Instructions:

This is answer sheet is a format only. You may answer using any word processor (i.e. Microsoft Word, Libre Office, Latek, Google docs … etc.) but you need to submit either a pdf or docx file so we can comment on it. Make sure to put your name, student number, and indicate what lab class you are in. This is given in the format above. Name your file "coe197_class_lastname_studentnumber". For the class write "satam" or "satpm" if you're in the morning or afternoon class, respectively. For example: "coe197_satam_antonio_201101474".

When you make your document please maintain the order of the main sections (PART I, PART II, PART III, and PART IV) and stick to the numbering provided in this answer sheet. You may use this word document if you like.

Answer with clear and concise solutions. Indicate your final answer (box it, bold it, change its color but please do not use red font color). For problems that require explanations, elaborate your thoughts. Any unclear answers will be marked wrong. There will be partial points.

Have fun and learn by heart!

Part I: Review (1pt.)

1. What is a common source amplifier?

- A MOS configuration where you place the input at the gate and probe the output at the drain. In a sense, the source acts as the "common" between the gate and the drain.

Part II: Training (11 pts)

Question Q2.1: (1pt.)

Given some transistor configuration, what's the first thing we always ask?

-Where does the current go?

Question Q2.2: (2pts.)

Using Figure 2.2 can you visually describe what happens when $r_o \gg R_L$, where does i_{ds} go and how does this translate to $A_v = -g_m R_L$? Explain thoroughly.

-When $r_o$becomes significantly greater than R_L, i_{ds} tends to go to R_L. Current always goes to the path of least resistance. If r_o becomes infinitely large, it acts as an open circuit. Current will flow through R_L.

Question Q2.3: (3pts.) 1pt. each

What operating region is the transistor in when:

1. $V_{GS} < 0.28\,V$?
   - Cut-off region because it is lower than the threshold voltage
2. $0.28\,V \leq V_{GS} \leq 0.45\,V$?
   - Saturation region because operating in this range affects V_{out} greatly.
3. $V_{GS} > 0.45\,V$? *Hint: Recall that* $V_{THN} \approx 0.28\,V$
   - Linear region because there is not much effect on V_{out} when operating in this range.

Question Q2.4: (2 pts)

Put on your thinking hat and try this out. A resistor-loaded NMOS common-source amplifier has a supply voltage of 1.2V. The NMOS transistor was biased to achieve a $\frac{g_m}{I_{DS}} = 10\,V^{-1}$. Don't panic the V^{-1} is just the units for $\frac{g_m}{I_{DS}}$. What is $V_{GS} - V_{TH}$ assuming the transistor is a square-law device? What is the gain that can be achieved if the output DC voltage is set at half of the supply? (Hint: use the equations! $\frac{g_m}{I_{DS}} = ???$).

- $g_m = \frac{2 \cdot I_{DS}}{V_{GS} - V_{th}}$. Thus, $\frac{g_m}{I_{DS}} = \frac{2}{V_{GS} - V_{th}}$. Substituting, we get $10 = \frac{2}{V_{GS} - V_{th}} \rightarrow V_{GS} - V_{th} = 0.2$
- $A_v = \frac{2 \cdot (V_{DD} - V_{OUT})}{V_{GS} - V_{th}}$. Since we know $V_{GS} - V_{th}$, $A_v = \frac{2 \cdot (1.2 - 0.6)}{0.2} = 6$

Question Q2.5: (1 pt) 0.5 pts each

What is $\frac{g_m}{I_D}$ when $V_{GS} = 0.3$? What about when $V_{GS} = 0.4$?

- When $V_{GS} = 0.3, \frac{g_m}{I_D} = 13.27V^{-1}$
- When $V_{GS} = 0.4, \frac{g_m}{I_D} = 7.98V^{-1}$

Question Q2.6: (1 pt) 0.5 pts each

What V_{GS} gives us $\frac{g_m}{I_D} = 20$? What about $\frac{g_m}{I_D} = 5$?

- To obtain $\frac{g_m}{I_D} = 20, V_{GS} = 174.13mV$
- To obtain $\frac{g_m}{I_D} = 5, V_{GS} = 496.96mV$

Question Q2.7: (1 pt) 0.5 pts each

What is the V_{ov} that gives us $\frac{g_m}{I_D} = 20$? What about $\frac{g_m}{I_D} = 5$?

- $\frac{g_m}{I_D} = \frac{2}{V_{GS}-V_{th}}, 20 = \frac{2}{V_{GS}-V_{th}} \rightarrow V_{GS} - V_{th} = 0.1 = V_{ov}$
- $\frac{g_m}{I_D} = \frac{2}{V_{GS}-V_{th}}, 5 = \frac{2}{V_{GS}-V_{th}} \rightarrow V_{GS} - V_{th} = 0.4 = V_{ov}$

Part III: Exercise (16 pts)

DIY: CS Amplifier with Resistive Load

Design your own CS amplifier with a resistive load for the following specs:

- $V_{DD} = 1V$
- $V_{OUT} = 0.5\,V$
- $V_{IN} = 0.36\,V$
- $g_m \geq 1\,mS$
- $A_{v,target}$ should be at least 87.5% of the ideal.
- Begin with $W = L = 500\,nm$ and final size should be in multiples of $100\,nm$ only.

Here are the steps as a guide:

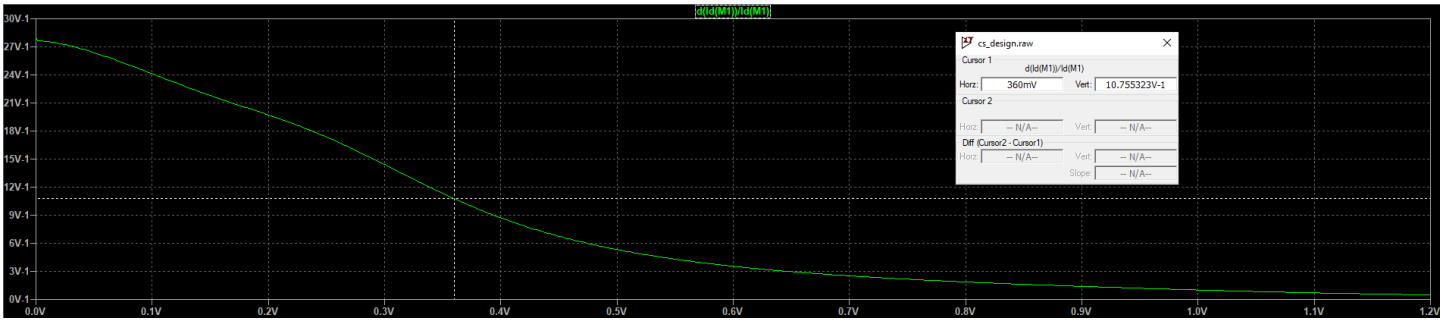
1. Determine $\frac{g_m}{I_D}$ and $V_{GS} - V_{TH}$. (2pts.)
2. Estimate the expected ideal A_v and compute the target minimum gain. (2pts.)
3. Calculate the target intrinsic gain $g_m r_o$. (2pts.)
4. Size the length so that your transistor achieves the desired $g_m r_o$. (2pts.)
5. Size the width to get the desired g_m. (2pts.)
6. Calculate the load resistance to support the desired V_{OUT}(2pts.)
7. Verify your design! (4pts.)

Provide the following:

- Your thinking process for every step.
- Please provide sufficient plots and calculations that explains your design process.
- Highlight (bold, color, put in a table) your final transistor size, intrinsic gain $g_m r_o$, g_m, and actual gain.
- Be sure to provide your final gain plot similar to Figure 2.15.

First, compute for $\frac{g_m}{I_D}$ and $V_{GS} - V_{TH}$.

With $L = W = 500nm$, extracting the $\frac{g_m}{I_D}$ at $V_{GS} = 0.36V$ gives $\frac{g_m}{I_D} = 10.755V^{-1}$.



This means that $10.755 = \frac{2}{V_{GS}-V_{TH}} \rightarrow V_{GS} - V_{TH} = \frac{2}{10.755} \approx 0.186V$. Our system is operating above the threshold region.

After obtaining $V_{GS} - V_{TH}$, I can now compute for the expected ideal gain.

The ideal gain is $|A_{v,ideal}| = g_m R_L = \frac{2 \cdot (V_{DD} - V_{out})}{V_{GS} - V_{TH}}$. Thus, $|A_{v,ideal}| = \frac{1}{0.186} \approx 5.38$ with $V_{DD} = 1V$ and $V_{out} = 0.5V$.

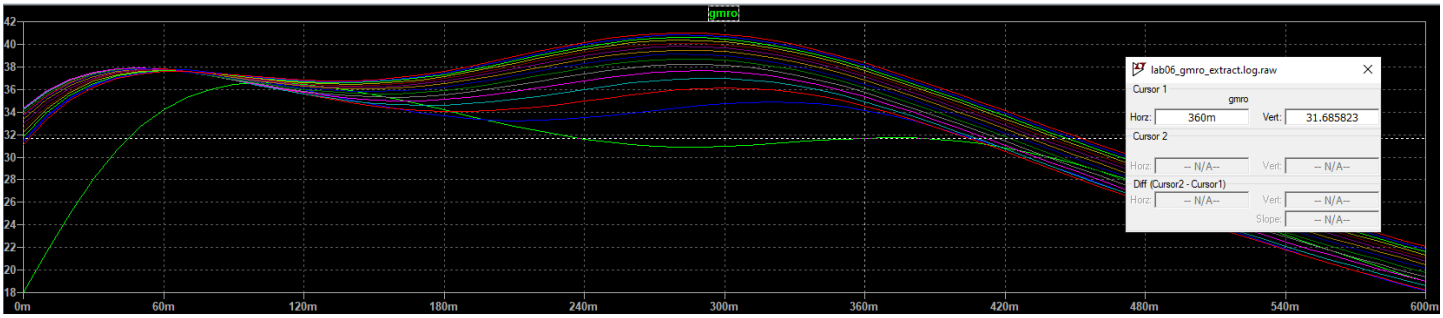
We want $|A_{v,target}| = 0.875 \cdot |A_{v,ideal}|$. Thus, $|A_{v,target}| \approx 4.6$.

The ideal gain only happens when $r_o \approx \infty \gg R_L$ so we need a certain "realistic" target gain.

Now, we need to extract the intrinsic gain of the device.

We know that $\frac{1}{g_m r_o} + \frac{1}{g_m R_L} = \frac{1}{g_m (r_o || R_L)}$. Substituting the values, we get $g_m r_o = 31.728$.

At $W = 500nm, L = 100nm$, $g_m r_o = 31.68$. This is close to our desired $g_m r_o$.



The desired $g_m = 1\text{m}s$. What we have is 41.42. The new width should be $500nm \cdot \frac{1000}{41.42} = 12.07um \approx 12\text{u}m$.

We get $I_{DS} = 58.72uA$ with W = 12um and L = 100nm. Now we compute for the resistance of the load.

$R_L = \frac{0.5V}{58.72uA} = 8515\Omega \approx 8.5k\Omega$.

Finally,

- W = 12um, L = 100nm
- VDD = 1V, VGS = 0.36V, VDS = 0.5V
- g_m = 1.013mS, $g_m r_o$ = 31.68

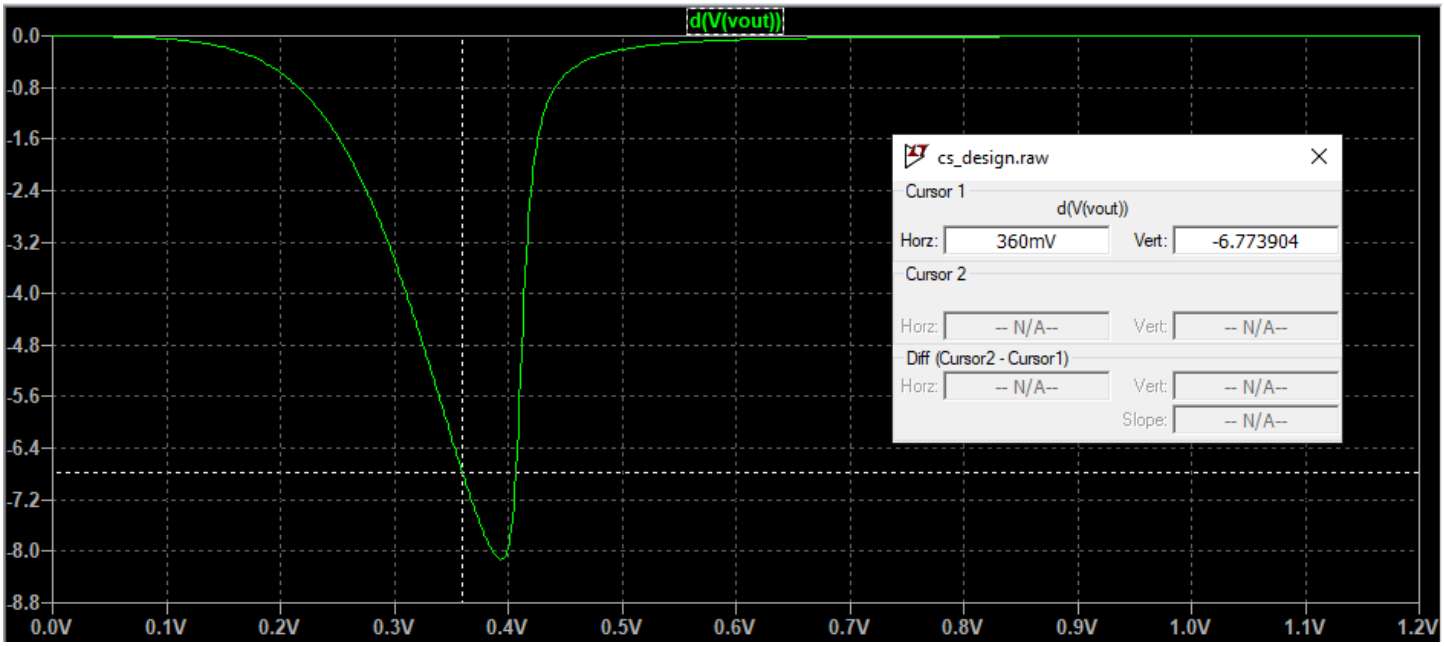
Thought process:

Initially, I started at W = L = 500nm. $g_m r_o$ is high at those values so I decided to make L smaller. Eventually, I got L = 100nm. I then computed for the new width and got $12um$.

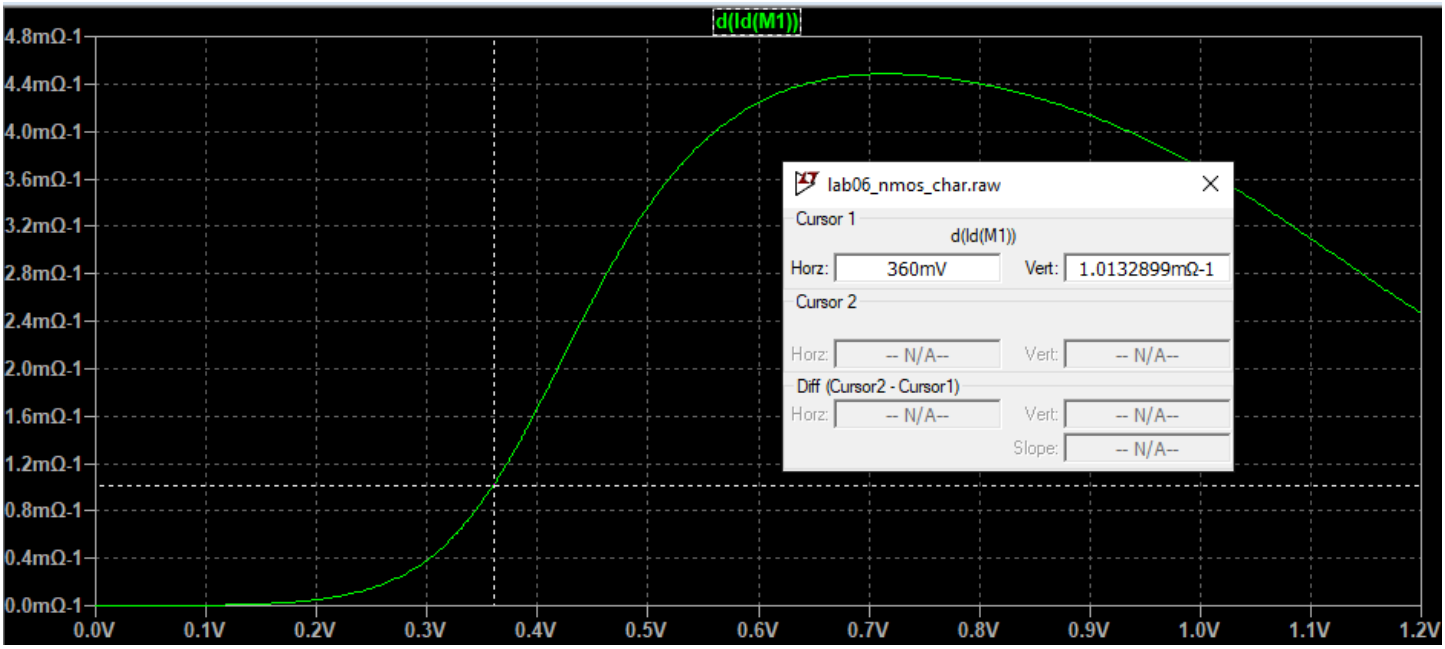
After testing, I got some problems. When I computed for the resistance value, the gain was higher than the target gain, so I figured that it was due to the changes from W and L during the design process.

To get the desired target gain, I need to replace the resistance with $5k\Omega$ but this changes V_{out} to 678mV.

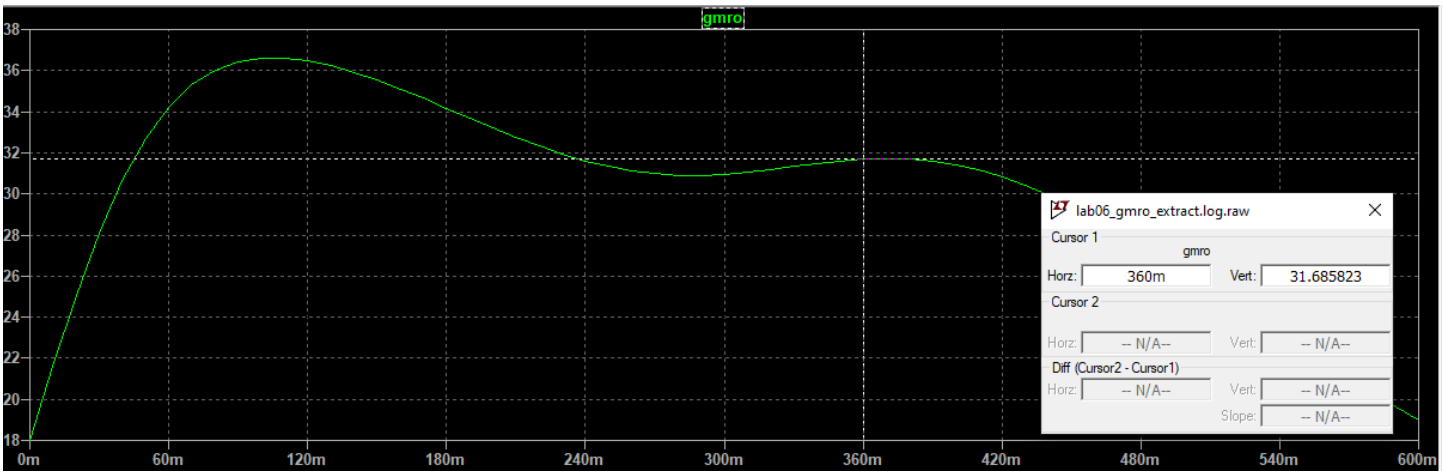
The plot below shows the actual gain I got.



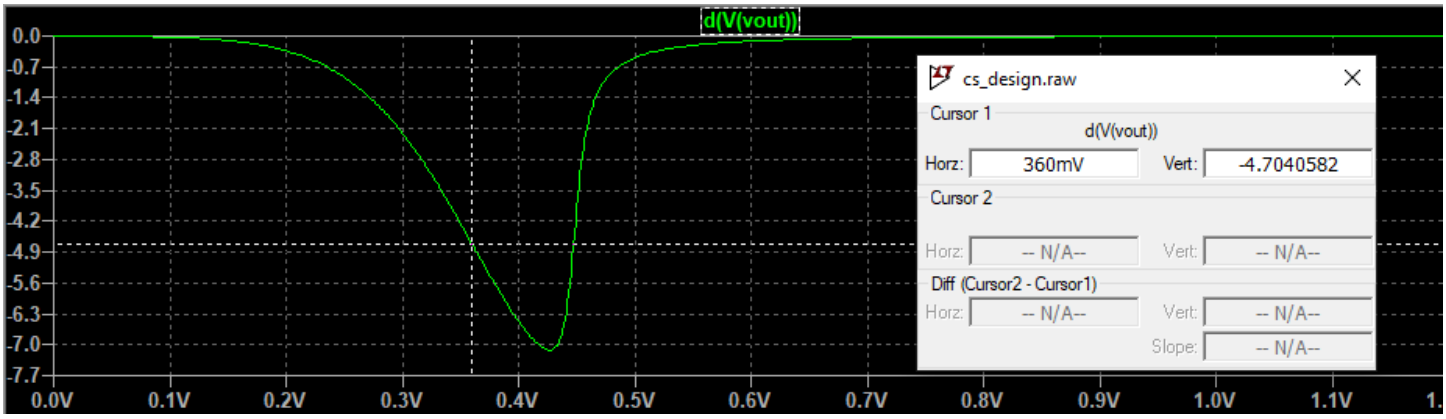
The plot below shows the transconductance of the transistor.



The plot below shows the designed $g_m r_o$.



If I replace the resistor with a 5kΩ resistor. This is what I get.



It has a gain that is close to the targeted gain, but the $V_{out} = 0.678V$.