 University of the Philippines

 Microelectronics and Microprocessors Laboratory

Lab Module 06 – Common Source with Current Source Loads, Common Drain, Transfer Impedance Concept

What will you learn from this lab?

* Analysis and design of CS amplifiers with current source loads
* Analysis and design of common drain (CD) amplifiers
* Appreciating the transfer impedance concept

A few reminders for any lab:

Each lab will always be broken down in 3 main sections

* Prelab/Review – this section can be treated like a “pre-lab” where you need to recall some of the previous concepts in your earlier courses or those that were discussed in the lecture.
* Training – this section guides you through a skill that you must learn. This could be a method in using the tool or a concept that is new to you.
* Postlab/Exercises – are some problems that you need to solve. Sometimes you need LTspice for it, and some don’t. It’s there for you to test what you have learned.
* Supplementary reading – these is an optional content but for the interested students, you can read and answer some of its questions. It’s to further help you appreciate what IC design is.

There will be special boxes that you need to watch out for.

**BLUE BOXES**: Are used for useful notes and discussions. They can help you understand and appreciate the current topic at hand.

**RED BOXES**: Are notes that you need to watch out for. Some of these may be warnings that pertain to some limitations of our simulator. Or possibly some warnings on how to use particular circuit models.

**GREEN BOXES**: Are questions for that particular training task. They are also in the answer sheet so they’ll be hard to miss.

Part I: Review

1. What is a common source amplifier?

Part II: Training

## A. Intuitive Analysis of a Common Source Amplifier

Analog design always begins with the simple common source (CS) amplifier. Learning the tricks on how to conveniently analyze CS amplifiers can carry over to other types of amplifiers. Sometimes, we need to accept and appreciate how it works first, then the intuition becomes second nature to us. Consider Figure 2.1 which shows a simple common source amplifier with a resistive load.

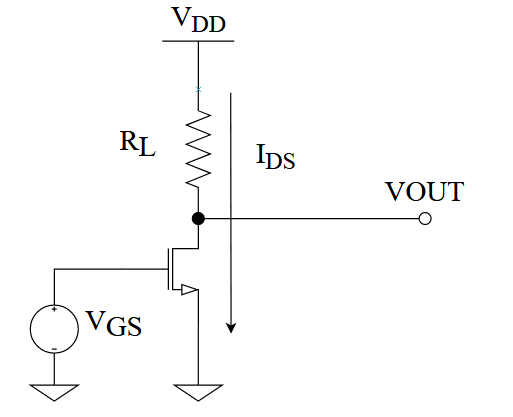


Figure 2.1 Common-source amplifier with drain node KCL

is a resistive load because the task of the NMOS transistor is to drive a current on that load. Regardless of how the transistor is configured, we always ask ourselves *“Where does the current of the transistor go?”*. Alternatively, we can also ask *“What is the critical KCL node?”*. We’ll see this kind of analysis in the succeeding labs. In Figure 2.1, the critical node would be the drain node. The KCL on the drain node is trivial:

Where , is the current that goes through the resistor. Therefore, a common source amplifier controls how much current can be delivered to its load. Since the NMOS controls how much current goes through , then this also controls how our moves. By KVL at the transistor’s output, we can get:

From the above equation, it is evident that as increases, the output decreases. This should be clear even when we look at Figure 2.1. When increases, then the voltage drop across the resistor increases. Therefore, by KVL, decreases. Recall from the previous lab that the gain is defined as and if we apply this to the above equation, we get:

Remember, is a constant and therefore disappears after taking the derivative. We also know that leading to . We also know that for a transistor. Hence, the gain:

From the lecture, this is the ideal gain of a common source amplifier driving a resistive load. This is an ideal case because this holds true only if . The gain is actually descriptive of how changes with changing input. Recall that is the rate of how much current our transistor produces for every small-signal increment of (or ). Since the current across the resistor is , then the rate at which the voltage drops across increases is with increasing . Finally, since then it makes sense that *decreases* at the rate of . This should lead us to a conclusion that . Make sure you got this descriptive definition of . In summary, *the voltage gain of a common source amplifier is the product of the rate of how much current we are delivering to the load and the effective impedance (resistance) of the load itself*.

Since is an ideal gain, the more accurate gain would be:

You might be wondering, where does the factor kick in? From the previous lab, we know that the reciprocal of the output impedance describes the rate of change in the output current when is changing: . This is known as the *output transconductance* (. Looking at Figure 2.1, we know that and since changes (becomes more negative but not decreasing) with increasing (increasing ), then the effects of changing (because of changing ) affects the current. Observe: increasing , increases , and therefore manipulates . This change in also affects caused by the output transconductance and in turn limits how much of the real change in current affects the load . *To put it simply, the change in is being shared between and .* Take time to internalize this paragraph.

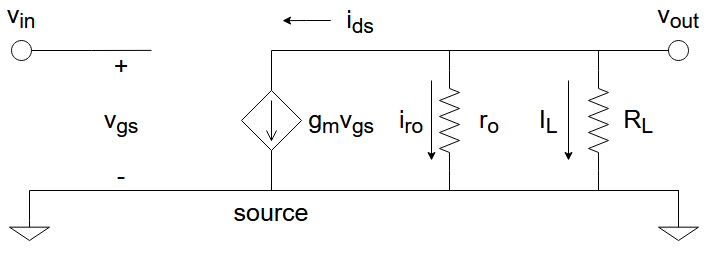


Figure 2.2 Small-signal model for the CS amplifier in Figure 2.1

Another perspective is to look at Figure 2.2 which shows the small-signal model for the CS amplifier in Figure 2.1. You should know how to recreate this circuit model from your lecture. Deriving the gain is straight forward, first do a KCL on the drain node ( node):

We can transform these currents into their voltage dependencies and get:

Combining terms and re-arranging yields:

Finally, knowing that and getting results in:

By now, you should be over-familiarized with the derivation of the gain. Let’s step back a bit and re-analyze each equation. The KCL tells us that the current drives both and . Essentially, is shared between and making effective resistance that is driving to be: . Therefore, the effective change in output voltage . tells us that as the current increases at the rate of (because of increasing input ) the output decreases at the rate of (because of increasing ). *Ultimately, gain is simply the rate of how the changes for every unit of which is the product of the rate of producing (that’s for every unit of , and the rate of producing for every unit of* .

**QUESTION (Q2.1)**:

Given some transistor configuration, what’s the first thing we always ask?

**QUESTION (Q2.2)**:

Using Figure 2.2 can you visually describe what happens when , where does go and how does this translate to ? Explain thoroughly.

## B. Simulating A CS Amplifier

Before we get into designing, let’s first appreciate how a simple CS amplifier works. *You can’t design anything without studying what needs to be designed*. Figure 2.3 shows a pre-built CS amplifier with and . Let’s also assume that we’ve pre-determined that and . First, let’s extract our small-signal parameters and from our characterization circuit. Then we’ll prove the consistency of our small-signal models and the analysis we’ve done earlier. Do the following:

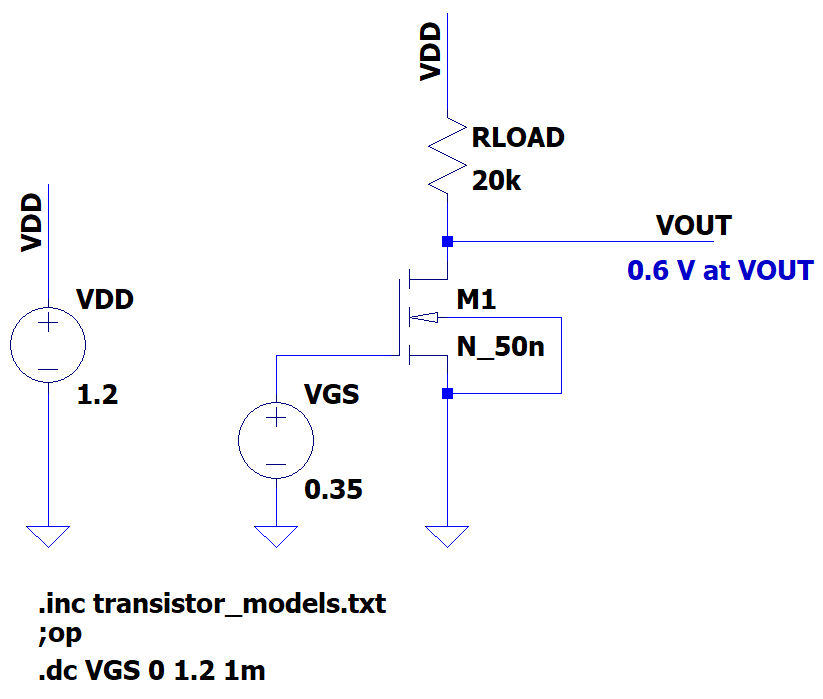


Figure 2.3 Simple CS amplifier schematic

1. Open your characterization circuit “lab06\_nmos\_char”. This is the same schematic from the previous lab.

2. Make sure and .

3. First extract when and You should get .

* You should know how to get this. Either sweep for changing or do a .op analysis.

4. Extract the :

* Set because out (as seen in Figure 2.3)
* Make a DC sweep for from 0 to 0.5 V. (It could’ve been up to 1.2V but we only needed )
* Plot and get the value when .
* You should get a . This is shown in Figure 2.4.

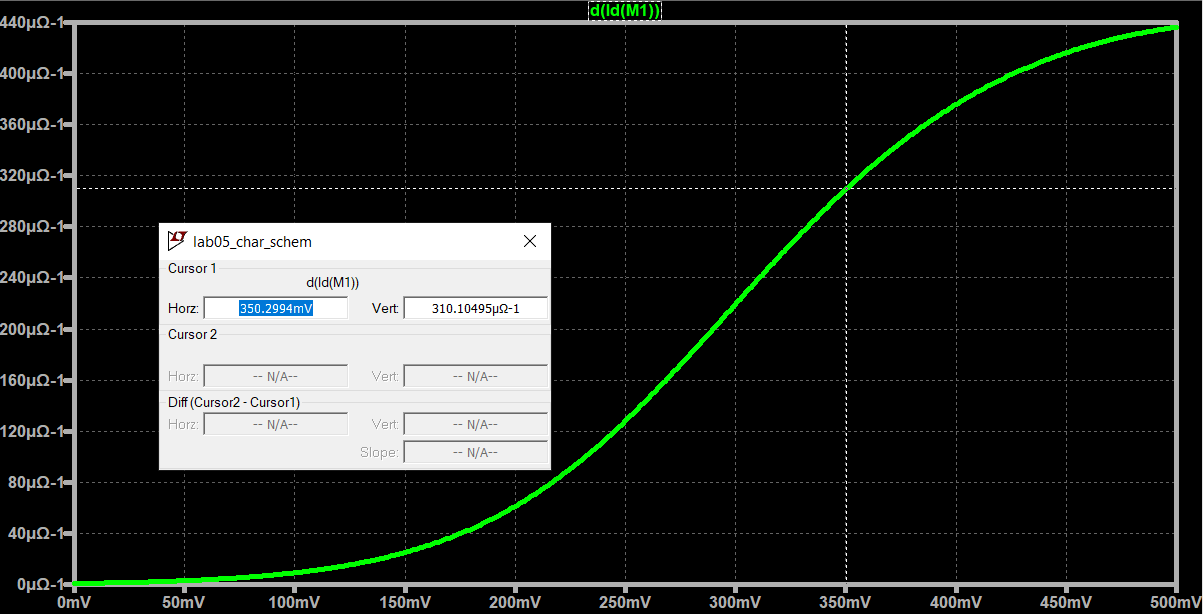


Figure 2.4 Extracting when and

5. Extract :

* Fix (this is our operating input) and sweep from 0 V to 1.2 V
* Plot and get the value when .
* The at should be
* Figure 2.5 shows this.

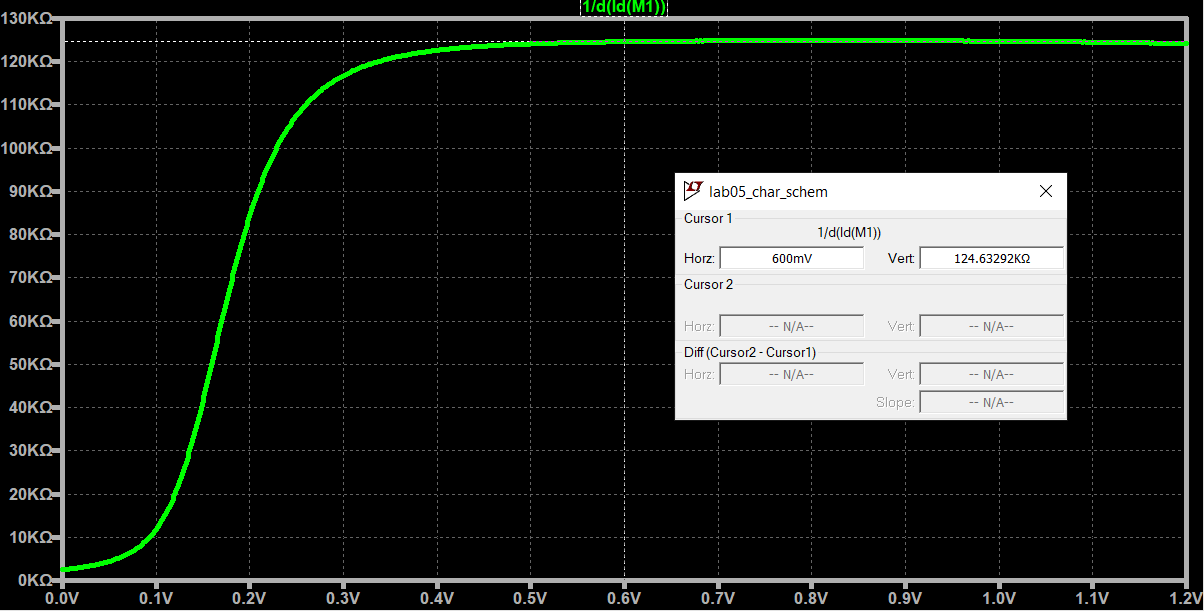


Figure 2.5 Extracting when and

Great! We now have and . Take note that we rounded the values to “nice” number for convenience. Now using the small-signal model in Figure 2.14, we can immediately calculate the gain. Such that:

Take note that is not that high compared to . In fact, . That’s significantly far from . Therefore, . Calculating the small-signal gain gives us . Let’s try to show this from the actual simulation. Do the following:

1. Open the schematic named “lab06\_cs\_amp.asc”. This is the same schematic in Figure 2.3.

2. The circuit is already prepared for you so go ahead and run the simulation.

3. Plot and on the same plotting plane. You should get Figure 2.6.

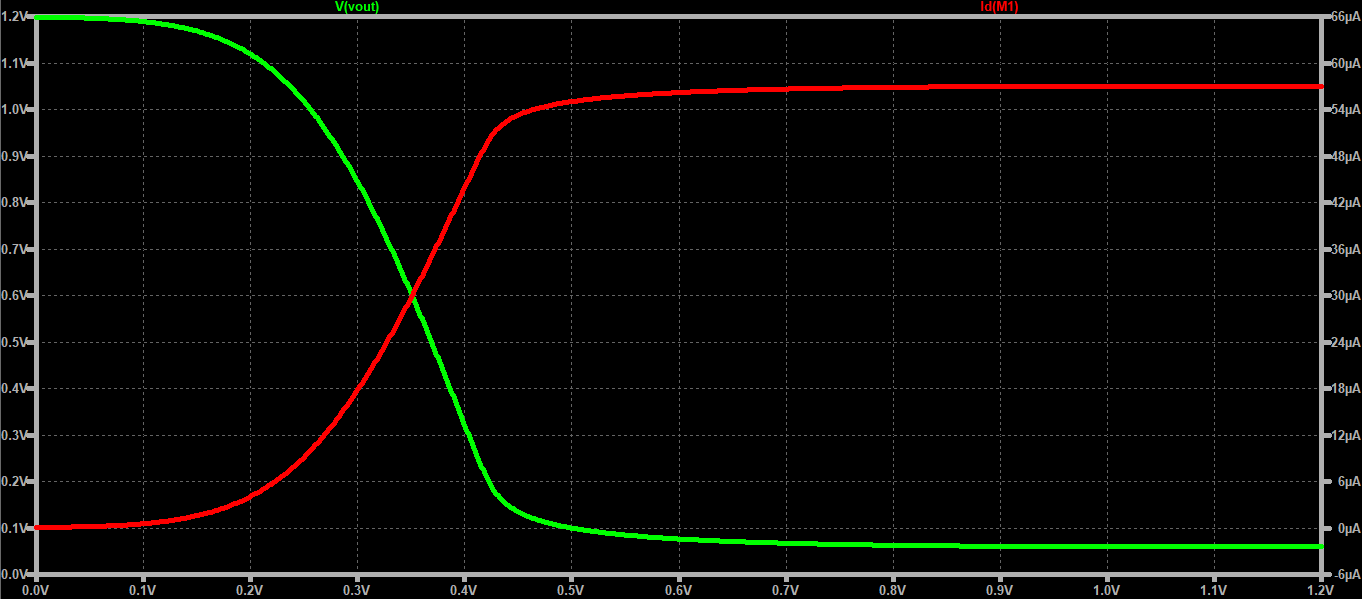


Figure 2.6 and vs

4. Let’s do a quick analysis:

* The curves are consistent with what we discussed in section A.
* As increases, increases and decreases. Easy!
* Remember, the curve follows the equation.
* Of course, follows the current equation:
* When the transistor is in the region (roughly): , changes because both and are changing at the same time.

5. Let’s plot the gain:

* Remember, gain () is the change in over the change in .
* Add a plotting plane and plot the derivative of :
* Place a cursor on both and when
* You should get Figure 2.7.

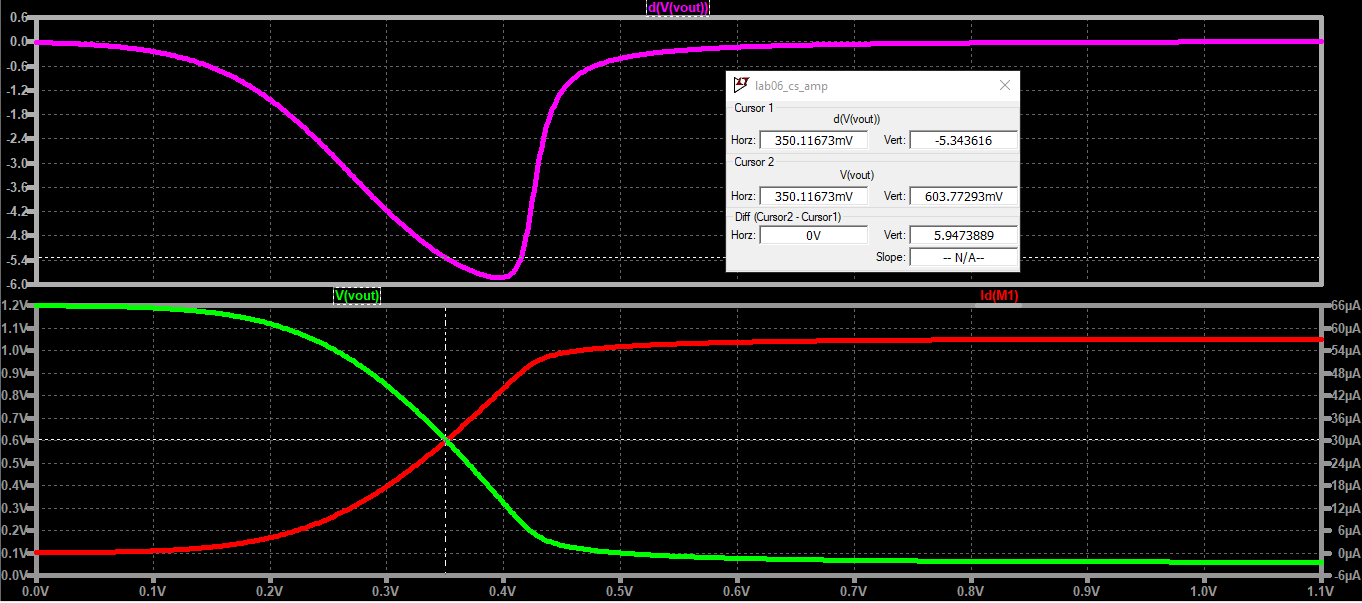


Figure 2.7 Gain () plot vs . When we have

Great! We have interesting results. First the gain we calculated is consistent with our simulation:

Next, the expected and is accurate (you can change for :

**QUESTION (Q2.3)**:

What operating region is the transistor in when:

1. ?
2. ?

*Hint: Recall that*

**QUESTION (Q2.2)**:

Using Figure 2.2 how can you show that when , becomes ? Explain thoroughly.

**DISCUSSION**:

In the previous lab, we used an AC method of extracting the gain of the amplifier. We can actually do the same for the normal CS amplifier. Go ahead and open “lab06\_cs\_amp\_ac\_extract.asc” schematic. The setup is the same as the one we have in the previous lab. Observe the following:

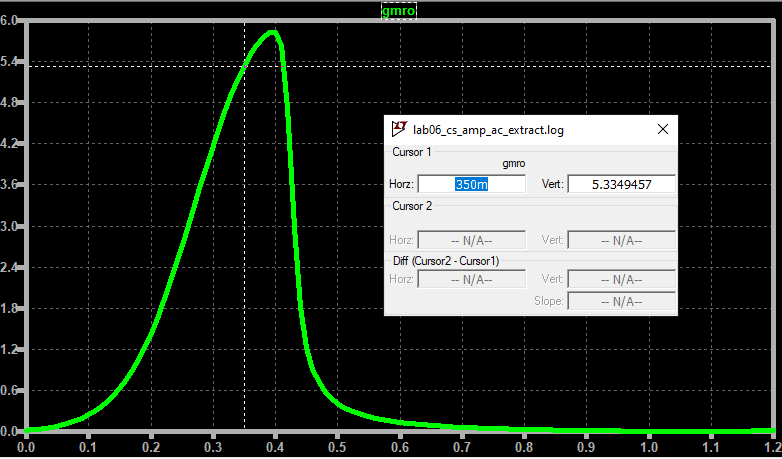
1. The source’s DC is set to a vgs variable and the AC voltage is set to 1.

2. We did a sweep of frequency from 1 – 100 Hz only, since we only need the DC range ().

3. The .meas SPICE directive measure the output gain.

**DISCUSSION (continued)**:

Run the simulation and plot the gain. You should get the same figure below and when . Observe that the figure below is just the magnitude (hence absolute value) of the gain and it is the same curve in Figure 2.7 (top plot).



## C. Alternative Analysis of the CS Amplifier

An alternative analysis of the CS amplifier can be derived by carefully dissecting the equation. Remember,  *is an ideal case* because it only applies if and only if . In reality, may be comparable to such that . For now, let’s assume for the sake of simplicity but do keep in mind this is an ideal gain. Let’s also assume that we are maintaining our transistor in saturation. That means it satisfies and . Recall that:

Substituting these to (let’s ignore the negative sign for now):

Interestingly, this equation tells us that the gain improves when and (or ) decreases. Pretty cool right? Let’s investigate this further.

*Case 1: decreasing*

Decreasing improves the gain based on the equation above. In fact, the math tells us that we can achieve if because . However, this is does not really happen because as approaches , the square law equations become inaccurate and our original equation won’t hold true anymore. Moreover, setting to low sets to high and it would defeat eventually bring down.

*Case 2: decreasing*

Decreasing increases the factor and thus making the gain larger. Though unlike the decreasing case, we can never reach an infinite value. Additionally, because we can only set to as low as . Go any lower, and our transistor will operate in the linear region instead of the saturation region. That’s a big no-no for this case. In some cases, there is a desired voltage in case this CS amplifier is an input to another amplifier. If that happens, we have no choice but to set only. Controlling is only possible by biasing the appropriate . Increasing decreases but the derived gain equation tells us that this reduces the gain as well.

Ultimately, there is a sweet spot where an appropriate can produce the maximum gain. Looking at Figure 2.7 tells us that the highest gain for the CS amplifier occurs when . This leads to roughly around . This also results in a . Small and small yields an optimally high again. There’s another caveat to this analysis, the and terms were not really specified. In actual practice, there is a desirable and value. For example, some amplifiers require a minimum to support the desired speed. Others need to drive a fixed load. If a specific is needed, then the current can be calculated from the voltages, and this current can be used to compute for the effective (i.e. . On the other hand, if a certain is given (or required), the current can be computed from the desired , then compute the needed to achieve the target (i.e. ).

**QUESTION (Q2.4)**:

Put on your thinking hat and try this out. A resistor-loaded NMOS common-source amplifier has a supply

voltage of 1.2V. The nmos transistor was biased to achieve a . Don’t panic the is just the units for . What is assuming the transistor is a square-law device? What is the ideal gain that can be achieved if the output DC voltage is set at half of the supply? (Hint: use the equations! ).

The question above introduces the (Gee-ehm-ai-dee) metric which is a very useful spec for every analog designer. Take note, we’ll interchange and for now because the general term also applies for PMOS transistors. From the fraction itself, it tells us how much can we get for every unit of . We can simulate this. Do the following:

1. Open the characterization schematic “lab06\_nmos\_char”.

2. Maintain the input sweep of . Also, maintain and .

2. Plot by plotting d(Id(M1))/Id(M1).

3. You should get Figure 2.8.

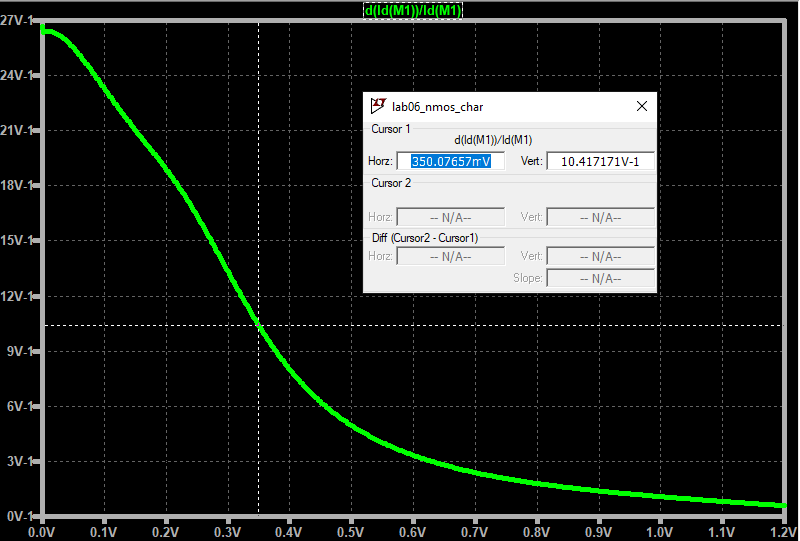


Figure 2.8 plot

Analog designers use this metric to characterize power. The higher the the lower the power consumption because it only requires a few units of current to produce higher ! What’s interesting is that at lower we actually gain higher for every unit of Operating at is possible, and we call this the *sub-threshold region*. Even though our ideal square-law equations tell us that at we should have , technically it’s just but this small current is widely used for ultra-low power applications. One common example are watches. Keep this in mind!

Finally, can be computed from because then . We also know that from the lecture slides. However, is generally known as the *over drive voltage* () because it describes how much “over drives” . From here on, will be interchangeable.

One more note, is independent of and slightly dependent on . *The slight dependence on L may cause some problems later on, but fret not, is just a measure of (1) efficiency and (2) .*You can experiment on this by parametrizing width and length sweeps. We’ll leave the experimentation to you to save up on time.

For the following questions, assuming and while

**QUESTION (Q2.5)**:

What is when What about when ?

**QUESTION (Q2.6)**:

What gives us What about ?

**QUESTION (Q2.7)**:

What is the that gives us What about ?

**DISCUSSION**:

The concept may sometimes be misleading. It is true that higher implies we have a more efficient device because we get more for every unit of . However, higher is in the region when is really low. A low implies very low and even though is 10, but because the is extremely low, then we have very low as well! Take for example, (using the characterization circuit) when we have and , this means we have . As opposed to the case when we have and then, this results in . The when is still higher even though its is nearly half. *Analog designers often compensate the lack of current by increasing the widths*. Remember, is independent of but ; therefore, if we up-scale the width to be more, then we would have (for the case) and . You can experiment on this using the “lab06\_nmos\_char.asc” schematic.

Using very low is an attractive biasing point because of its high ratio efficiency. However, *nothing comes for free*. A lower value translates to a very low transit frequency . Remember, is the measurement of the inherent speed of a transistor with . We can re-use the same schematic for extracting in the previous lab. Feel free to run the schematic “lab06\_ft\_extract.asc”. was swept from 0 to 0.6 V only because we’re only really interested in . Go ahead and run the simulation then plot . You should get Figure 2.9.

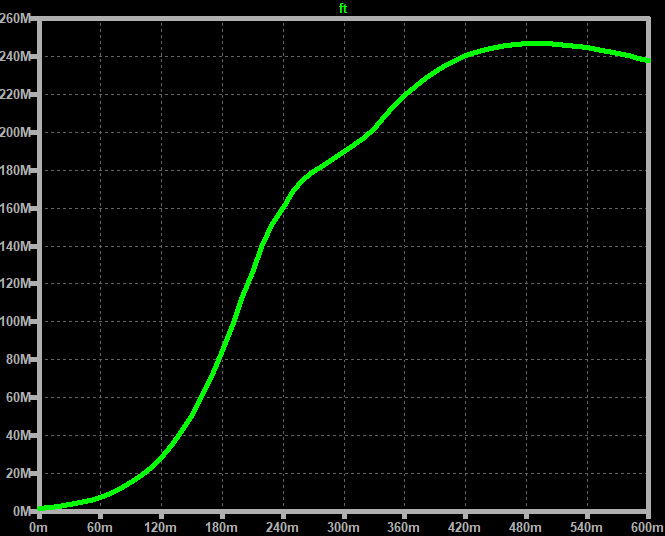


Figure 2.9 vs

Figure 2.9 and Figure 2.8 evidently shows that and are tradeoffs. Higher results in lower and vice versa. At a glance, the best range would be in . Because of this, our succeeding labs will use a biasing point within the desired range. The most important lesson is that and tradeoff each other.

**WARNING**:

For the sake of simplicity and learning, we’ll use the designated range but in your succeeding courses, you might come across a different scenario. In fact, the *optimal* range is a few milli-volts short of the threshold voltage. We just need to peg into your design philosophies that and tradeoff each other.

## D. Sample Design of a CS Amplifier with a Resistor Load

Let’s try to simulate how we would design a simple CS amplifier with a resistor load. Our design example will differ from what was simulated in Section B. Moreover, it may not be the optimal methodology but the process presented should be helpful for beginners. There may be concepts that might come as a surprise to you, but you will have to learn and accept them first. The reasons behind such design decisions will become clear to you with enough practice. Our goal is to emphasize on the design strategies and some things to watch out for.

Consider the following specs for a simple common source amplifier with a resistive load:

* Operating
* because we want the output to be half-way of .
* Use .
* The target should be at least 84% of the ideal gain ()
* we want our transistor to be at least this fast
* Begin with and and use multiples of if we need a larger size.

1. *Determine and*

We usually begin by determining what we are using because it gives context on what type of amplifier we will be designing. Moreover, is easy to extract from :

Using “lab06\_nmos\_char.asc”, we can plot the when . Figure 2.10 shows that while . Using the equation above tells us that . Our effective is operating relative above the threshold region. Therefore, we’re most likely designing a standard CS amplifier (i.e. not so power efficient and not too fast either).

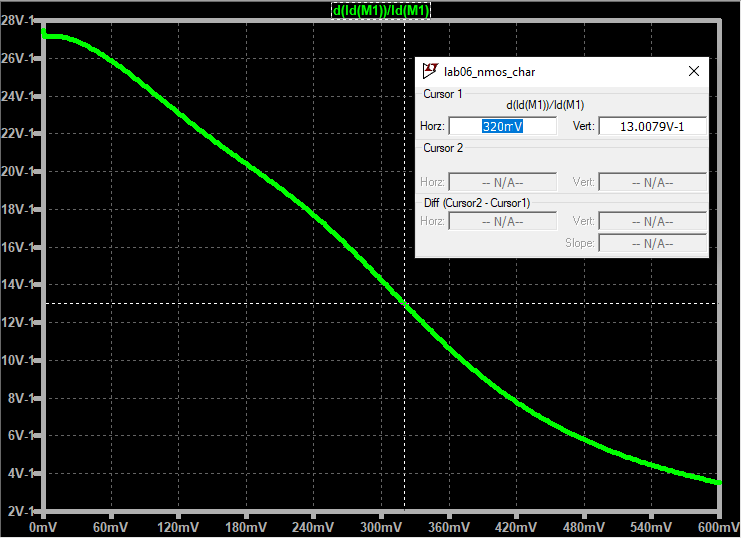


Figure 2.10 curve. When we have

1. *Estimate the expected ideal and compute the target minimum gain.*

It is useful to know the expected ideal results because it gives us insight of the limitations of our circuit. Again, the ideal gain () is the “maximum” that we can get if . This will not be the case; however, the ideal will be a stepping stone in determining how to size our transistor. From the specs, we know that , , and the extract . The ideal gain is then:

if and only if . Since we know that this may be difficult to achieve, the desired minimum gain should be at least 84% of the ideal gain. In other words, at the minimum: :

1. *Calculate the target intrinsic gain*

Making sure we meet the minimum intrinsic gain spec, guarantees us that we can get close to the minimum . We can extract from because the math tells us that:

Since we have and , we can easily compute the target :

Let’s set the minimum intrinsic gain to . We’ll use 41 for a nice number.

1. *Size the length so that your transistor achieves the desired .*

*In general, we choose to get the desired intrinsic gain* . We can do this by re-using the extraction schematic from the previous lab. Go ahead and open “lab06\_gmro\_extract.asc” then observe the following:

* Review the previous lab on how this circuit was setup.
* The AC sweep was only in the range of 1 Hz to 100 Hz because we’re only interested in the DC gain.
* There’s a .step SPICE directive for sweeping . Take note, that we’re only interested in the range close to the desired . (i.e. )
* There’s a .step SPICE directive for sweeping the length of the transistor. Observe that and .
* The .meas SPICE directive simply measures and saves the data.

Go ahead and run the simulation and plot . Use the cursor and arrow keys to navigate and get (use left and right arrow keys) and to a point where (use up and down arrow keys). If done correctly, you should get Figure 2.11 showing that at and we get .

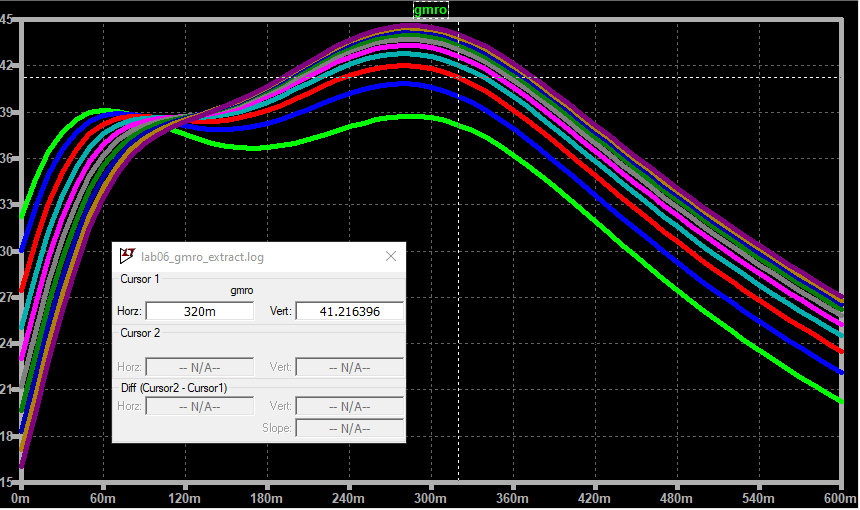


Figure 2.11 vs curve while parametrizing . when and .

**DISCUSSION**:

Here’s an interesting trend, *the does not change with*  or rather has an insignificant change with changing . Recall that:

Therefore:

From here, there is no dependency on . However, . We’ll leave it up to you to look for the specific details why, but indicates the steepness of the channel length modulation. As increases, decreases because the effects of channel length modulation diminish increasing the effective output impedance. Review your semiconductor physics if you need a refresher. This is why is dependent on but not on . Moreover, you can experiment on this using the schematic “lab06\_gmro\_extract.asc”. Simply fix and set . Run the simulations again and you should get Figure 2.12. Evidently, does not change with . *In summry, is used to control the gain!*

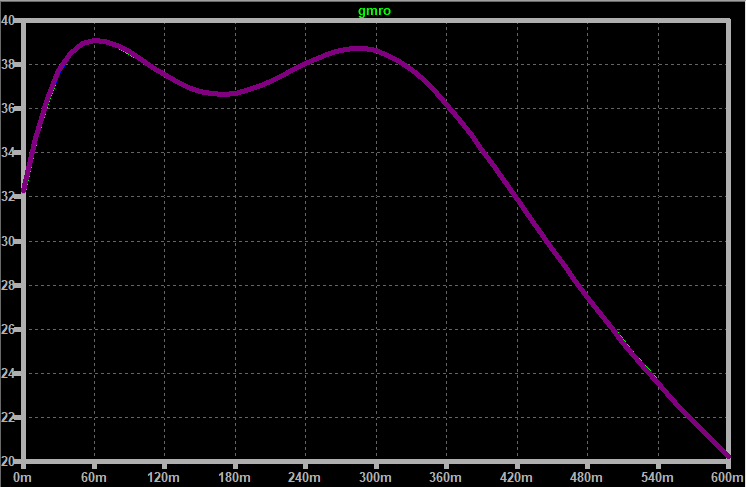


Figure 2.12 vs. with parameterized and . does not change with .

1. *Size the width to get the desired .*

*We choose to get the desired* . First, we know that our starting size would be and based on the characterization of . We can use “lab06\_nmos\_char.asc” to extract and for this size and when If done correctly (make sure the size is the same), you should get Figure 2.13.

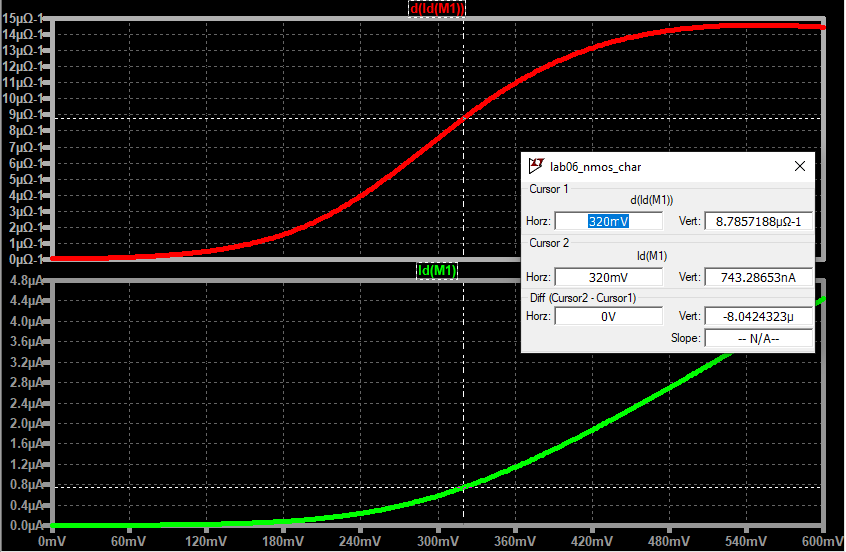


Figure 2.13 and vs. curve. and when and

Since, , we need to increase the in order to achieve our minimum . Because then it’s a matter of scaling, such that:

This means that our needs to be larger than the current to get the minimum . Therefore:

We’ll use (round up) to maintain the “multiples of 100 nm” requirement and to have nice numbers. Plugging this into the “lab06\_nmos\_char.asc” results in Figure 2.14. and . Great!

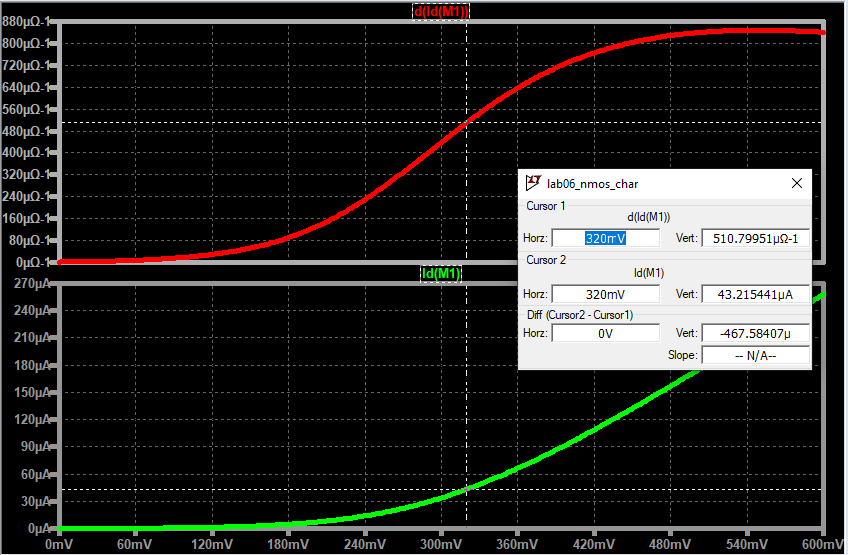


Figure 2.14 and vs. curve. and when and

1. *Calculate the load resistance to support the desired*

The load resistance is chosen to support the desired . Recall that the is computed by doing a KVL at the output:

Since we know from step #5 that , then we have:

1. *Verify your design!*

Great we’re, done! In summary our design needs to have:

* , , and
* and
* and

Plug the , , , and into the “lab06\_cs\_amp.asc” schematic and re-extract the output gain. Run the simulation and you should get Figure 2.15. Great!

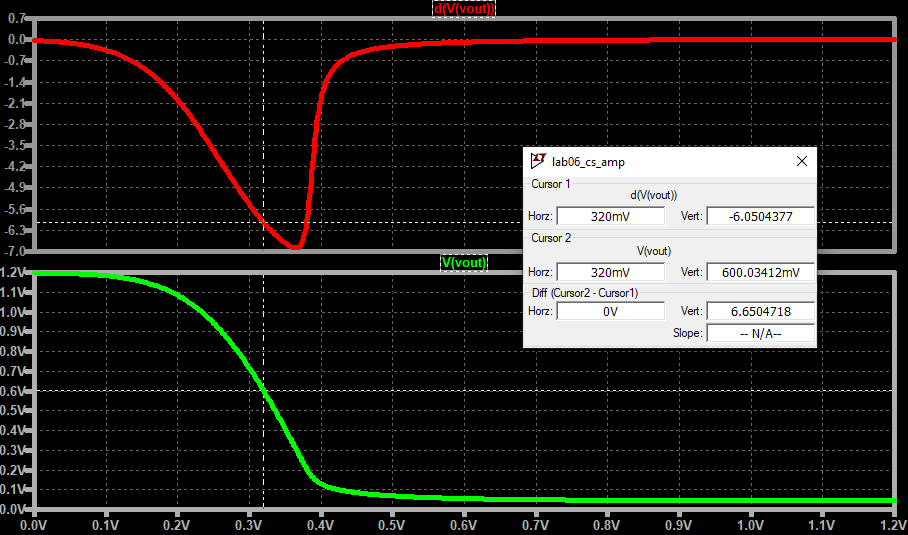


Figure 2.15 CS amplifier simulation with , , and

First, the is expected at . Obviously, this is trivial due to the chosen . However, the actual is less than the expected . We’re a bit short of 0.5 extra gain. Don’t panic, this is expected as well! The reason behind this is due to the and changing when we increased the lengths. If you re-extract with the current transistor size and (we’ll leave it up to you how to do this), you should get: which translates to . Re-computing the using this results in:

Which proves that we did get the target gain if we use the actual we are using (i.e. ). Hooray! Next time, just watch out for the parameter and expect it to change in the design process.

## E. Recap Time!

Phew! That’s a lot to take in but here’s the summary of steps:

1. *Determine and*

* We can infer the context of what kind of amplifier we are designing. (i.e. power efficient or fast).
* The tells us how close and how far we are from sub-threshold.

1. *Estimate the expected ideal and compute the target minimum gain.*

* Getting the ideal gives us a perspective of the maximum gain that we can get for an ideal CS amplifier with a resistive load case.
* The minimum gain is dictated by a fraction of how close do we want to achieve . The closer we are to the ideal, the more difficult it us.

1. *Calculate the target intrinsic gain .*

* The intrinsic gain is a setup for us to characterize and size a single transistor. If we get this right, we’re most likely to meet the overall spec.

1. *Size the length so that your transistor achieves the desired .*

* Always remember that is dependent on but not on . Or rather, effects are negligible when we change .

1. *Size the width to get the desired .*

* Always remember that is compensated by increasing .
* In the event that we need to increase because we need to increase gain, the decreases but we can re-increase it again by scaling without disturbing the .

1. *Calculate the load resistance to support the desired*

* After getting the desired to support the desired we can use the transistor current to determine how much current goes to the load resistance.
* The choice of the load resistance is for setting .

1. *Verify your design!*

* Always verify your design as a sanity check.
* If your design does not meet the initial calculations, take a step back and review.
* Watch out for cases like the changing whenever changes.

Great! Consider this methodology as a starting point in your adventure to analog design. In the near future, there may be variations to this. It may be a good idea to experiment on your own, and look for limitations for this methodology. For example, if you’ve noticed, increasing saturates the increase in . This is why we need to support it with auxiliary circuits that help boost our gain (to be discussed in the next labs). What we’ve presented is the CS amplifier only, but the concepts should still hold true for a common-gate (CG) and common-drain (CD). Lastly, practice makes perfect! Have fun!

Part III: Exercise

## DIY: CS Amplifier with Resistive Load

Design your own CS amplifier with a resistive load for the following specs:

* should be at least 87.5% of the ideal.
* Begin with and final size should be in multiples of only.

Here are the steps as a guide:

1. Determine and

2. Estimate the expected ideal and compute the target minimum gain.

3. Calculate the target intrinsic gain .

4. Size the length so that your transistor achieves the desired .

5. Size the width to get the desired .

6. Calculate the load resistance to support the desired

7. Verify your design!

Provide the following:

* Your thinking process for every step.
* Please provide sufficient plots and calculations that explains your design process.
* Highlight (bold, color, put in a table) your final transistor size, intrinsic gain , , and actual gain.
* Be sure to provide your final gain plot similar to Figure 2.15.

Part IV: Supplementary Reading / Exercises

## Real Engineers Read… A Lot!

Fundamentals are essential to us engineers. Read [this](https://drive.google.com/file/d/1mHWqGbdNQTBVgaI9cJ2QagNY3Q63-4WM/view?usp=sharing) article about how important fundamentals are especially when it comes to being a good engineer.