 University of the Philippines

 Microelectronics and Microprocessors Laboratory

Lab Module 07 – Answer Sheet

Name: Lastname, Firstname

Student #: 20XX-XXXXX

Class: SATURDAY AM / SATURDAY PM

SCORE: XX/40

Instructions:

This is answer sheet is a format only. You may answer using any word processor (i.e. Microsoft Word, Libre Office, Latek, Google docs … etc.) but you need to submit either a pdf or docx file so we can comment on it. Make sure to put your name, student number, and indicate what lab class you are in. This is given in the format above. Name your file “coe197\_class\_lastname\_studentnumber”. For the class write “satam” or “satpm” if you’re in the morning or afternoon class, respectively. For example: “coe197\_satam\_antonio\_201101474”.

When you make your document please maintain the order of the main sections (PART I, PART II, PART III, and PART IV) and stick to the numbering provided in this answer sheet. You may use this word document if you like.

Answer with clear and concise solutions. Indicate your final answer (box it, bold it, change its color but please do not use red font color). For problems that require explanations, elaborate your thoughts. Any unclear answers will be marked wrong. There will be partial points.

**Have fun and learn by heart!**

Part I: Review (5 pts)

1. Draw a rough sketch of the curves of a resistor, a current source, a non-ideal current source, and a transistor. (4 pts.)

2. In simple terms, what does a current mirror do? (1 pt.)

Part II: Training (10 pts)

## Question Q2.1: (1 pt.)

Briefly explain why a current source load is better than a resistive load.

## Question Q2.2: (1 pt.)

When is the transistor “acting” like a good current source?

## Question Q2.3: (1 pt.)

How would we size a transistor such that it becomes a better current source?

## Question Q2.4: (2 pts.)

Theoretically, we could just have sized the PMOS to get (does not need to be infinite, just really large) and not worry about what should be. In reality, analog designers don’t go too far from being just a few magnitudes higher (). Why do you think this is so?

## Question Q2.5: (3 pts)

Let’s see if you’re paying attention. Consider Figure 2.16 showing a set of PMOS current mirrors. Similar to Figure 2.14, fill in the table below with the correct sizes such that we can achieve the desired output currents per PMOS device. The width and lengths are in multiples of 1 . Answer in multiples of the base width and length.

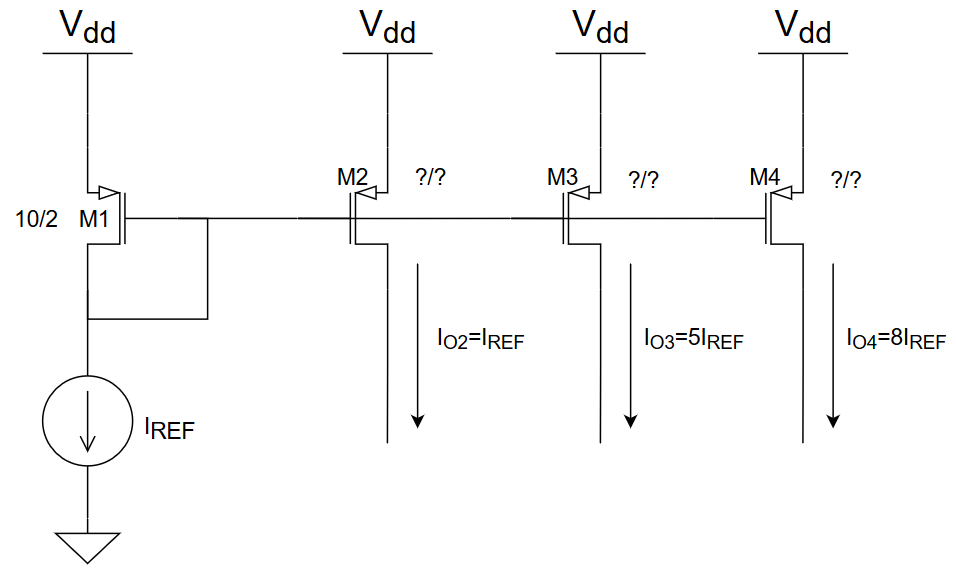


Figure 2.16 Set of PMOS current mirrors

|  |  |  |
| --- | --- | --- |
| Transistor | Width | Length |
| M1 |  |  |
| M2 |  |  |
| M3 |  |  |

## Question Q2.6: (2 pts)

Re-derive equation (5) again but this time, include the effects of channel length modulation. In other words, include the terms. Be sure to add the current subscripts for each transistor.

Part III: Exercise (15 pts)

## Don’t You Hate Ladder Problems? ☹

Suppose you were tasked to design a CS amplifier with the following specs:

* It needs to drive a transistor load as a current source
* The gain must be
* The speed of your amplifier must be
* For simplicity, let’s choose , , and
* Start with and and use multiples of for widths and for lengths.
* For simplicity, we let be the maximum length for both NMOS and PMOS.

Do the steps that was taught to you. Show your solution for each step. If you need to provide plots for clarity, feel free to do so.

*1.* *Calculate the and that gives the minimum .* (2 pts)

*2. Determine the that gives the minimum .*

* *In the event that we can’t reach the minimum due to device limitations of the NMOS transistor, we need to re-calculate the desired for the chosen .* (3 pts)

*3. Using the chosen in step 3, size such that we get the minimum . Also, determine the operating .* (2 pts)

*4. Size the PMOS such that we get the desired and .* (3 pts)

*5. Verify your design!* (3 pts)

* Re-use “lab07\_cs\_amp.asc”
* Show a plot similar to Figure 2.12. Make sure to show via cursors what is when and what is when .

6. Suppose we want to replace the PMOS current source with a PMOS current mirror that is biased by . The case is similar to Figure 2.20. (2 pts)

* How would you size the biasing transistor? Show a plot of the new and .
* Make sure to show via cursors what is when and what is when .
* Feel free to re-use “lab07\_cs\_amp\_w\_cm.asc”