LUTs Median Error	LUTs Mean Error	LUTs 95th Percentile Error
2.3	4.1	12.2

FFs Median Error	FFs Mean Error	FFs 95th Percentile Error
2.6	6	22.5

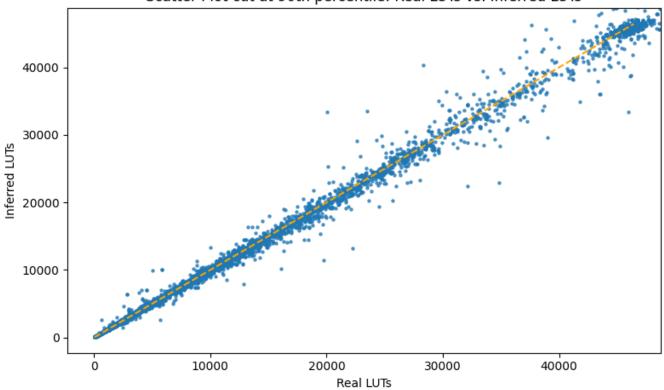
Latency Median Error	Latency Mean Error	Latency 95th Percentile Error
2.5	9.2	36.7

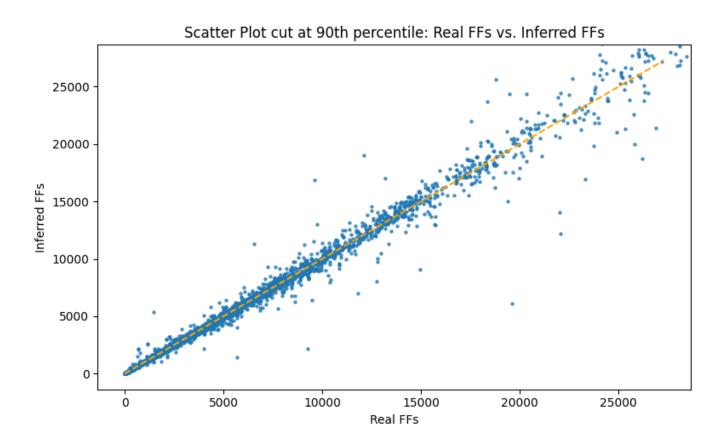
+ Clock Median Error		Clock 95th Percentile Error
0.5	1	3.5

DSPs Median Error	DSPs Mean Error	DSPs 95th Percentile Error
2.7	7.4	20.3

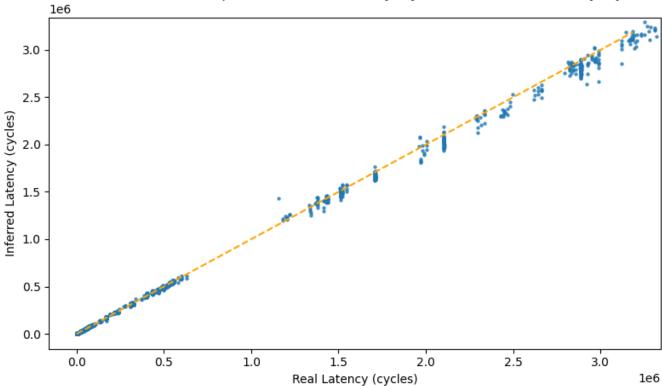
+		+	 		+	 		-+
į	BRAMs Median B	Error		Error		Percentile		_ į
		0.3	 	0.5	:	 	1.2	-+

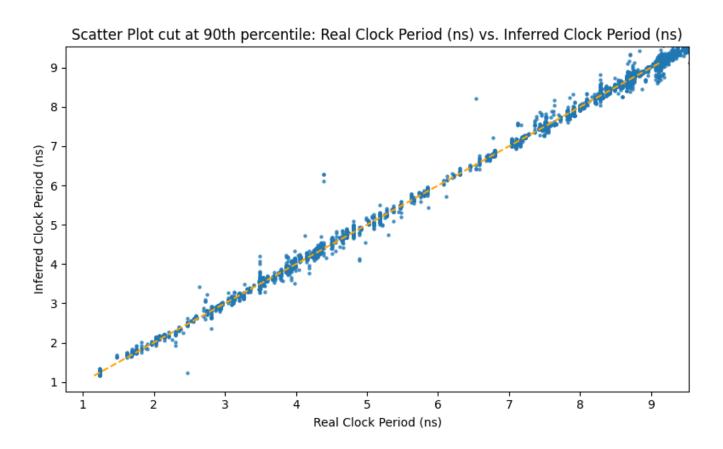
Scatter Plot cut at 90th percentile: Real LUTs vs. Inferred LUTs



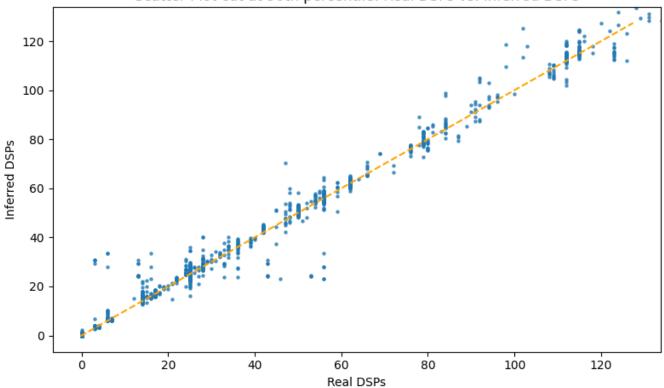


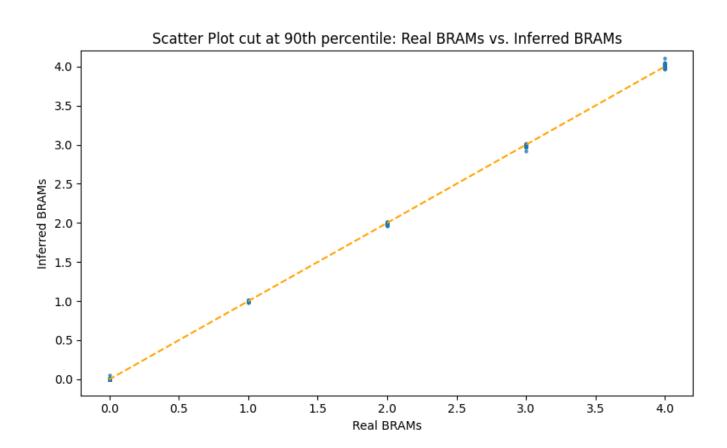
Scatter Plot cut at 90th percentile: Real Latency (cycles) vs. Inferred Latency (cycles)

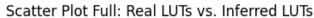


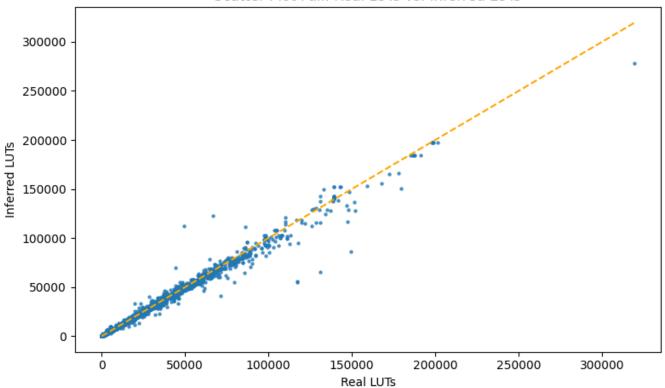


Scatter Plot cut at 90th percentile: Real DSPs vs. Inferred DSPs

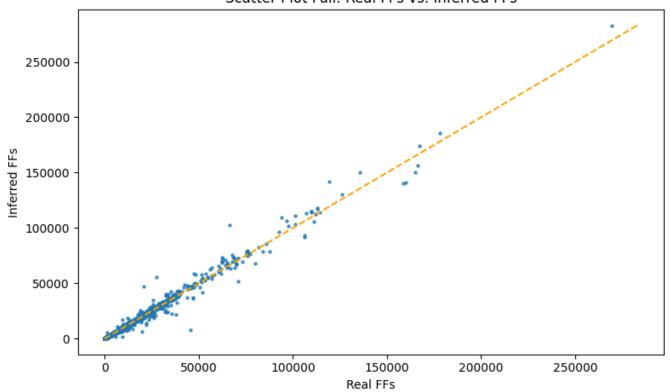


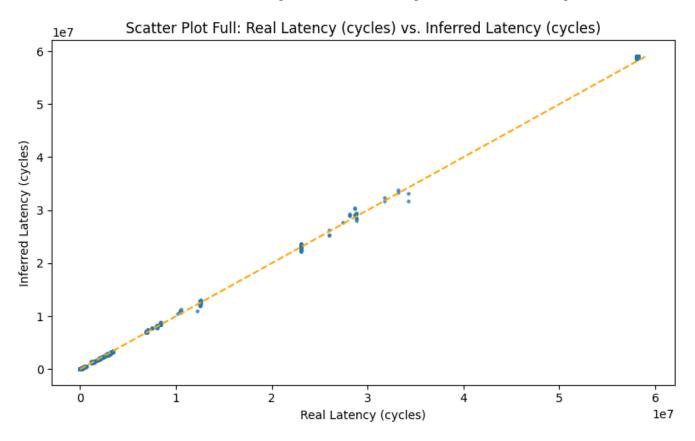


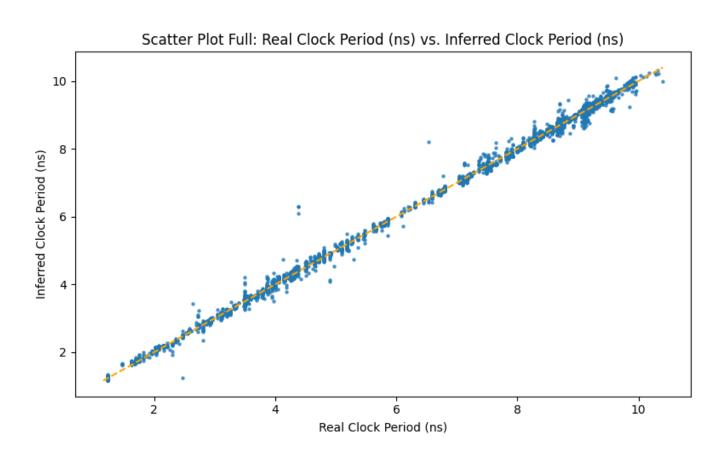




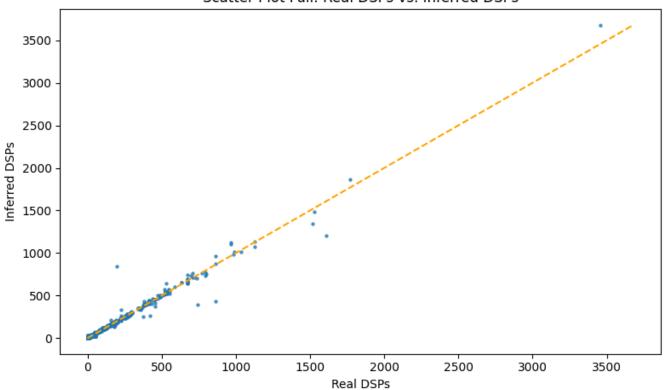
Scatter Plot Full: Real FFs vs. Inferred FFs



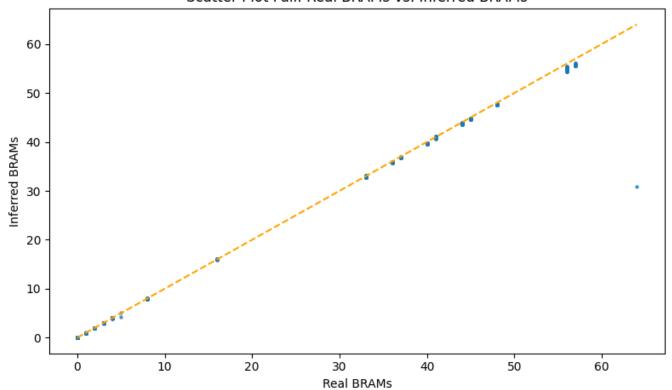




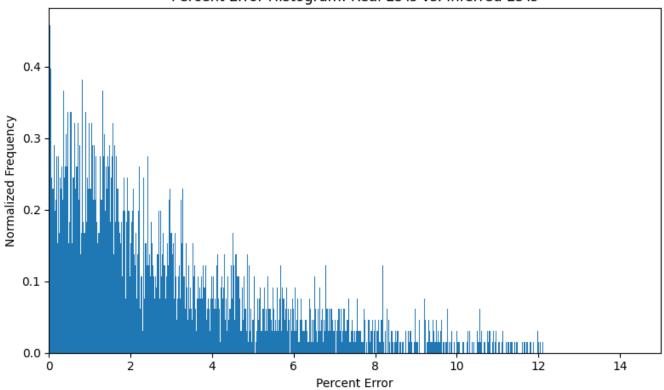


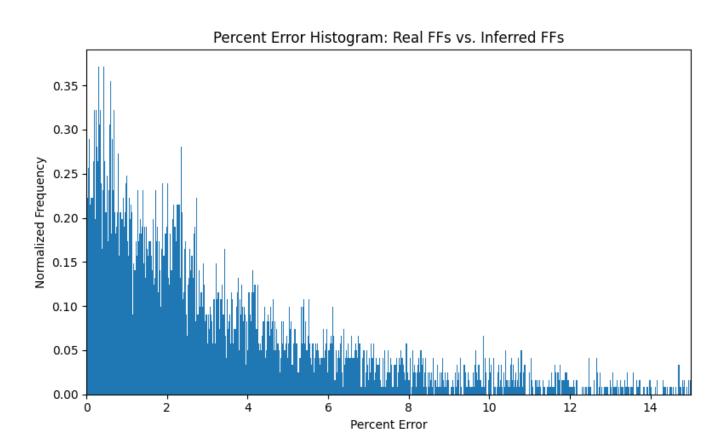




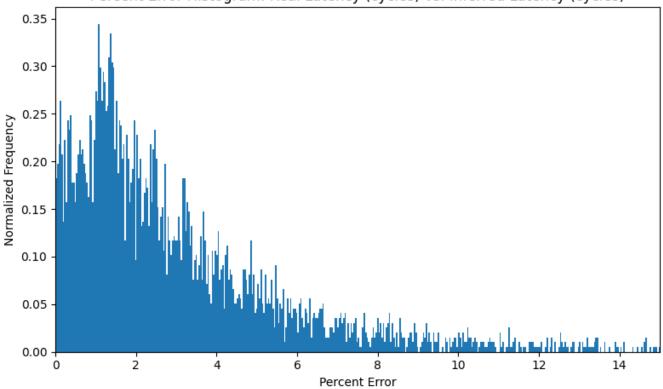


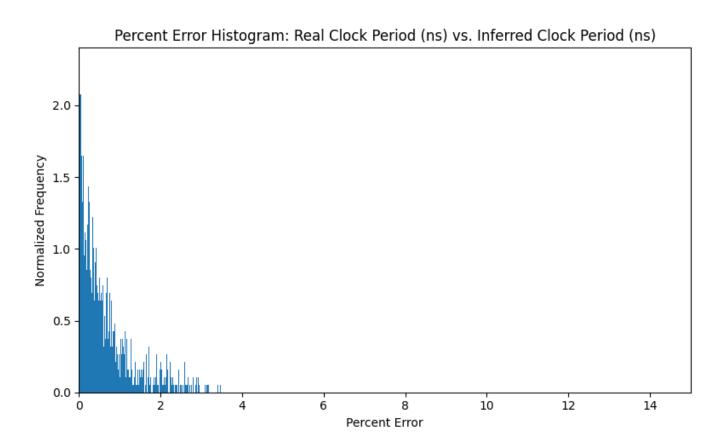
Percent Error Histogram: Real LUTs vs. Inferred LUTs





Percent Error Histogram: Real Latency (cycles) vs. Inferred Latency (cycles)





Percent Error Histogram: Real DSPs vs. Inferred DSPs

