Embedded Systems Engineering, Lab 1, Question 3  
Emmett Fitzharris, R00222357

The pl101\_read function takes three parameters, opaque, offset and size

The opaque parameter is cased to a PL011State Structure type, which is defined in pl011.h. PL011State includes fields which contain the addresses of the various registers of the UART used for control and checking status.

The program runs a switch statement based on the offset address provided in the parameters, which determines which register should be read, then returns the contents of the selected register.

The registers used are the following:

* UARTDR  
  The Data register of the UART device. Which is used to store the data to be sent for write operations or that has been received in read operations.
* UARTRSR  
  Receive Status register. Read to find status information from data received.
* UARTFR  
  Flag Register. Contains data on the state of the UART, including if registers are storing data, or if the UART is busy
* UARTILPR  
  IrDA low-power counter register, stores data required for managing the baud rate, controlling the timing of the UART device.
* UARTIBRD, UARTFBRD  
  Integer and Fractional baud rate registers. Used to calculate baud rate.
* UARTLCR\_H  
  Line control register, manages the configuration of the message format, such as parity error checking methods.
* UARTCR  
  Control Register. Defines settings for the UART, enabling or disabling features such as receiving and transmitting data
* UARTIFLS  
  Interrupt FIFO (First in first out) level select register. Defines the points at which the FIFO buffer emits interrupts, based on how full the register is.
* UARTIMSC

Interrupt mask set/clear register. Determines which interrupt requests are allowed to process.

* UARTRIS  
  Raw interrupt status register. Provides the status of interrupts.
* UARTMIS  
  Masked interrupt status register, similar to the above, but displays the status after masking allows or disallows the interrupt.
* UARTDMACR  
  DMA control register. Enables or disables receiving / transmitting using DMA (Direct memory access)