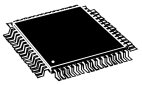
WB32FQ95xC

32-bit ARM® Cortex™-M3 MCU

Up to 256KB Flash / 36KB SRAM, USB OTG FS, 7 TIMs, 12-bit ADC, 11 comm.interfaces



LQFP64 (10 x 10 mm)

LQFP48 (7 x 7 mm)

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 96MHz maximum frequency
  - Dedicated instruction and data caches support 0 wait state memory access
  - Single-cycle multiplication and hardware division
  - AHB, APB1 and APB2 clocks are independent of each other
- Memories
  - 256Kbyte Flash memory
  - 36Kbyte SRAM
- Reset and supply management
  - Dual power supply, main power VDD:2.0V~3.6V, Backup battery power VBAT:1.8V~3.6V
  - Power On Reset(POR),Power Down Reset(PDR), Programmable Voltage Detector (PVD)
- Clock
  - 4 ~ 16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 48 MHz factory-trimmed RC
  - Internal 32 kHz RC for WDG
  - 32.768KHz oscillator for RTC with calibration
- Low power
  - Trickle-Power：Sleep, Stop and Standby modes
  - Dynamic current(Rum mode, disable peripherals)： 140uA/MHz@3.3V
  - Stop mode: ~18.5uA@3.3V
  - Standby mode: ~4.5uA@3.3V
  - VBAT with RTC: ~1.1uA@3.3V
  - VBAT operation is activated when VDD is not present ,supplies the 84-byte backup registers.
- Operation temperature
  - Industrial temperature range: -40°C~+85°C
  - Commercial temperature range: 0°C~85°C
- 12-bit mode ADC
  - Max convert rate: 1Msps
  - Up to 16 A/D channels
  - Flexible sample and converter modes.
  - Temperature sensor
- 2 independent comparators
  - Each with 4 positive and 4 negative input channels
- Up to 57 fast I/O ports
  - 37 or 51 I/Os, all mappable on 16 external interrupt vectors
- Debug mode
  - Serial wire debug (SWD) interface
- Up to 11 communication interfaces
  - Up to 2 I2C interfaces (SMBus),1 I2S interface
  - Up to 3 UART (6 Mbit/s)
  - Up to 3 SPIs, 1 QSPI
  - 1 USB 2.0 full-speed device controller
- Up to 6 timers
  - Up to four 20-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - One 20-bit motor control PWM timers with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
- 2 DMA controller, triggered by Timers, ADC, SPIs, I2Cs, UARTs
- RTC clock counter
- CRC calculation unit, 96-bit unique ID
- ECOPACK® Packages

Contents

List of Figures

List of Tables

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the WB32FQ95xC .

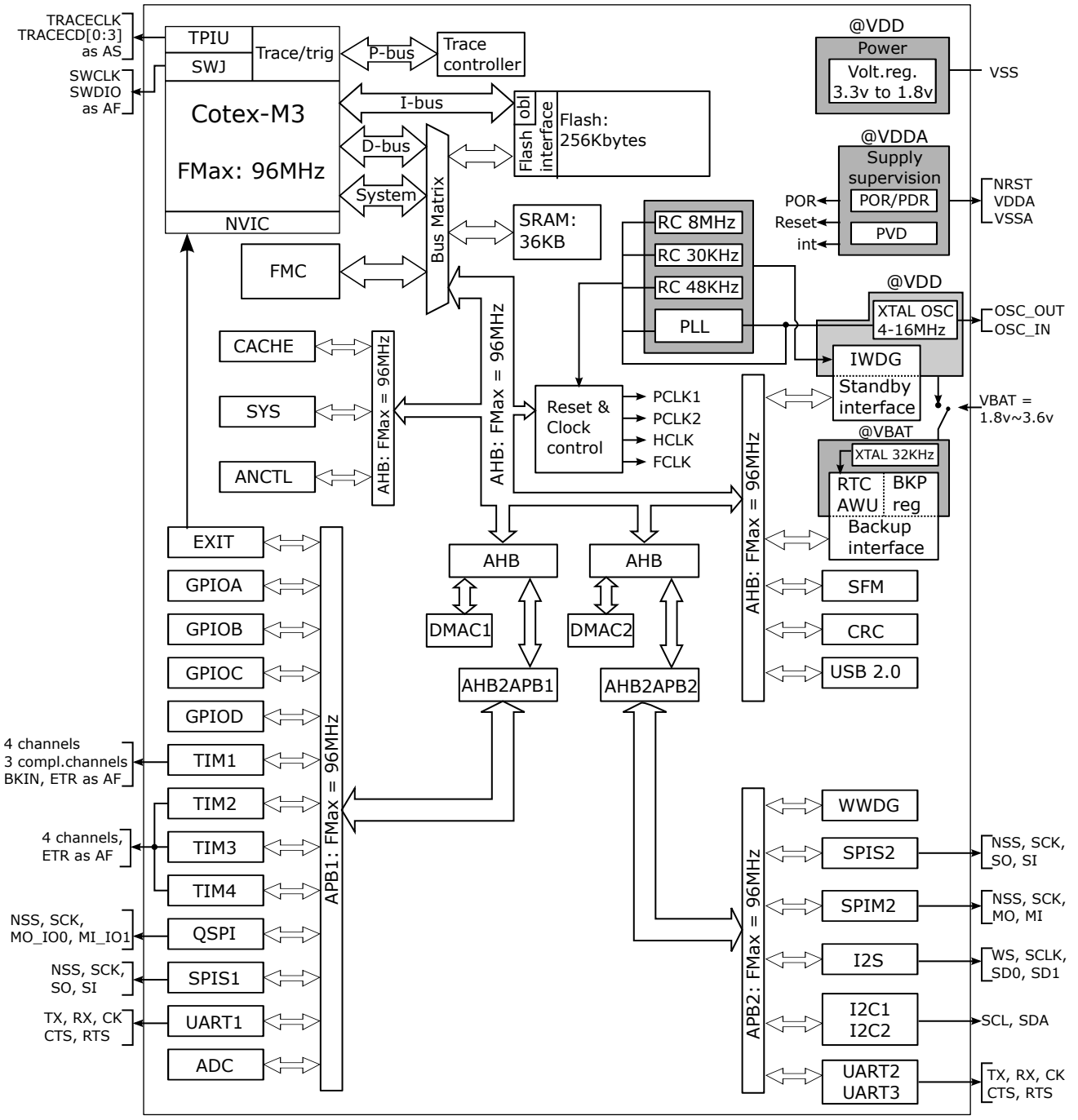
For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website.

2 Overview

The WB32FQ95xC performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 96MHz frequency, high-speed embedded memories (Flash memory up to 256KB Kbytes and SRAM up to 36KB Kbytes), one 20-bit advanced control timer, three general purpose timers, two watchdog timers (Independent and Window), three SPI interfaces, one QSPI interface, two I2C interfaces, three UART interfaces, one USB2.0 Full Speed interface, one SAR ADC converter, two 10-channel comparators, one RTC.

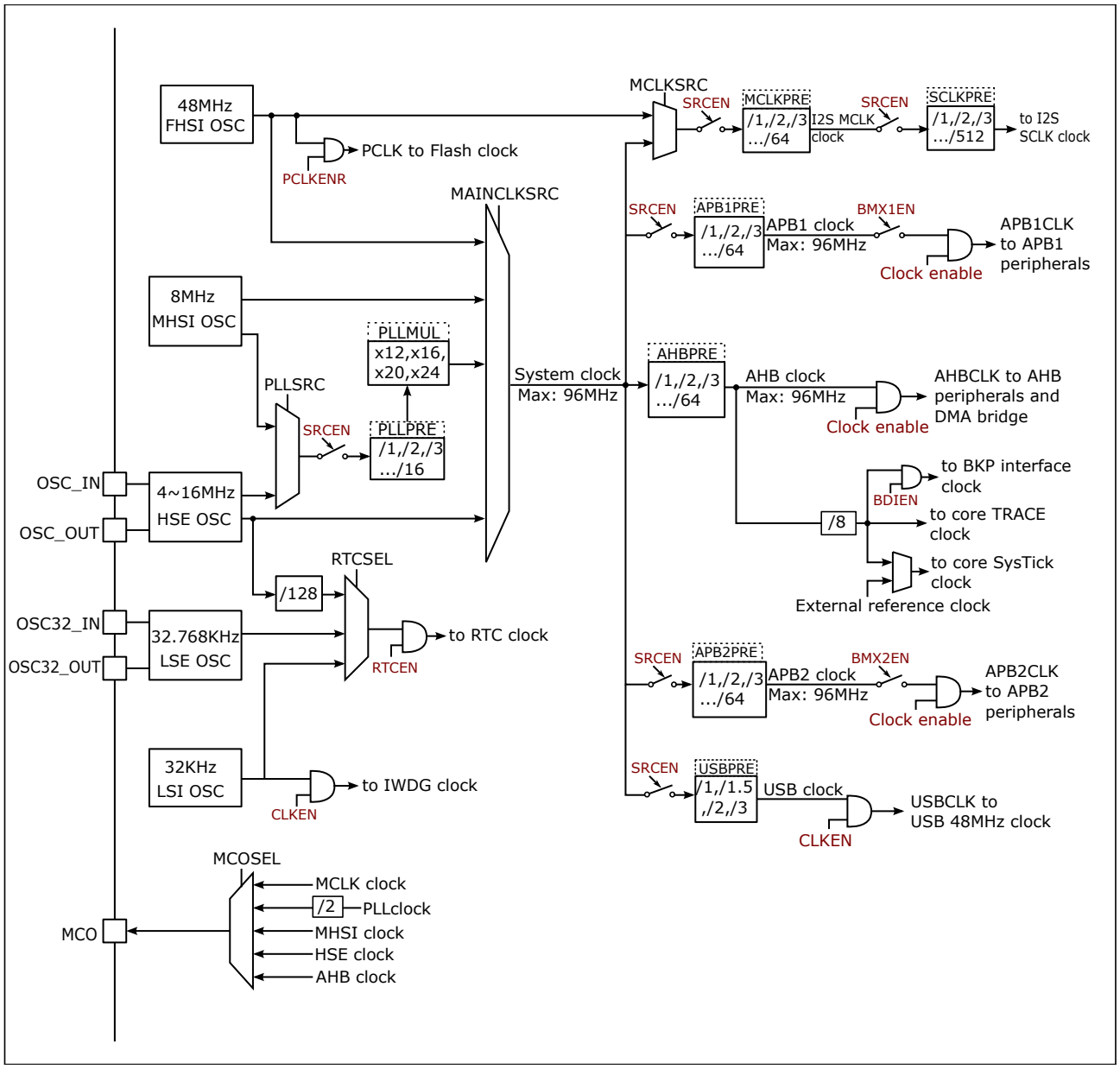
2.1 Block Diagram

Fig 2.1-1 WB32FQ95xC block diagram



2.2 Clock Tree

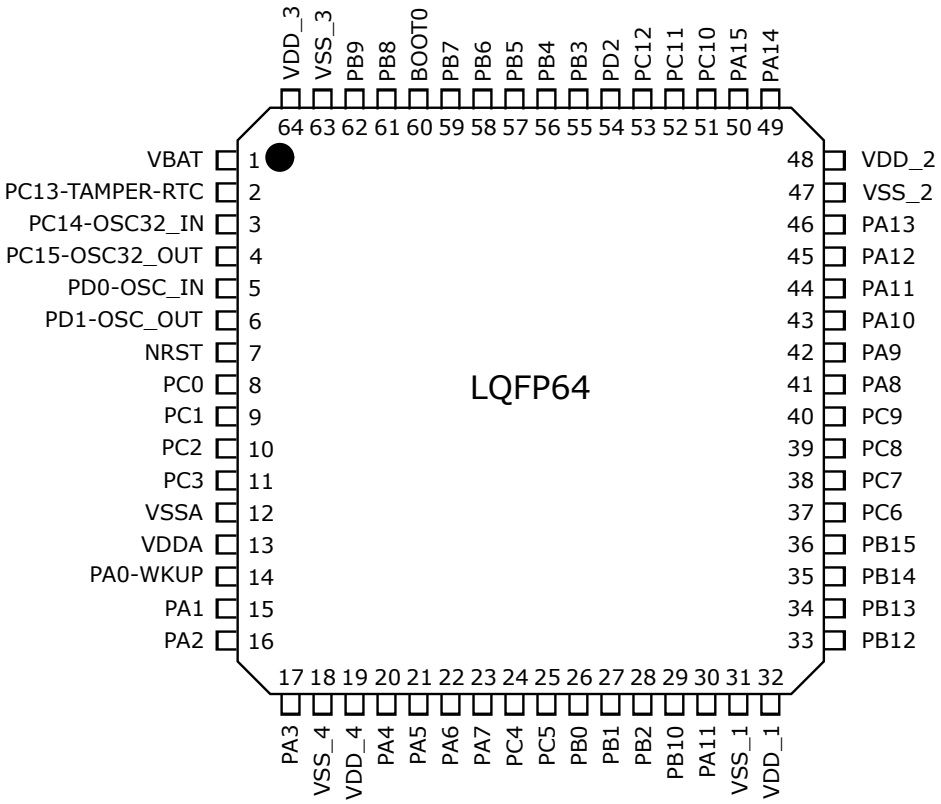
Fig 2.2-1 WB32FQ95xC Clock Tree



3 Pinouts and pin descriptions

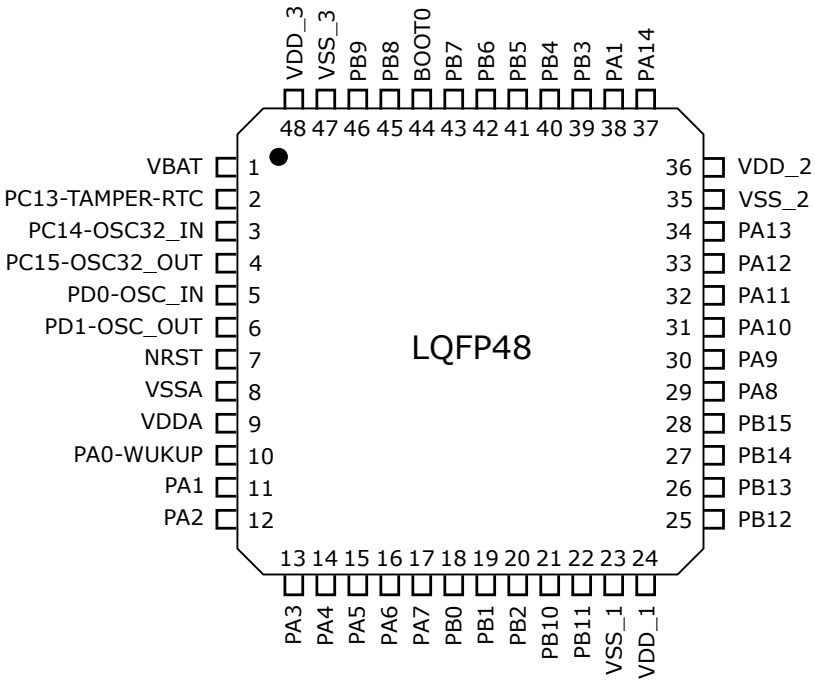
3.1 LQFP64 pinouts

Fig 3.1-1 LQFP64 pinouts



3.2 LQFP48 package

Fig 3.2-1 LQFP48 pinouts



3.3 Pinouts and pin description

Tab 3.3-1 WB32FQ95xC Pinout description

Pin No.		Pin Name	Type	Main Function	Alternate Function	Analog Function
LQFP48	LQFP64					
1	1	VBAT	S	VBAT		
2	2	PC13	I/O	PC13	TAMPER/RTC	
3	3	PC14	I/O	PC14		OSC32_IN
4	4	PC15	I/O	PC15		OSC32_OUT
5	5	PD0	I/O	PD0		OSC_IN
6	6	PD1	I/O	PD1		OSC_OUT
7	7	NRST	I/O	NRST		
-	8	PC0	I/O	PC0	I2S_WS / SPIM2_NSS0 / SPIS2_NSS	ADC_IN10
-	9	PC1	I/O	PC1	I2S_SCLK / SPIM2_SCK / SPIS2_SCK	ADC_IN11
-	10	PC2	I/O	PC2	I2S_SD0 / SPIM2_MI / SPIS2_SO	ADC_IN12
-	11	PC3	I/O	PC3	I2S_SD1 / SPIM2_MO / SPIS2_SI	ADC_IN13
8	12	VSSA	S	VSSA		
9	13	VDDA	S	VDDA		
10	14	PA0	I/O	PA0/WKUP	TIM2_CH1_ETR / UART2_CTS / WKUP	ADC_IN0
11	15	PA1	I/O	PA1	TIM2_CH2 / UART2_RTS	ADC_IN1
12	16	PA2	I/O	PA2	TIM2_CH3 / UART2_TX	ADC_IN2
13	17	PA3	I/O	PA3	TIM2_CH4 / UART2_RX	ADC_IN3
-	18	VSS_4	S	VSS_4		
-	19	VDD_4	S	VDD_4		
14	20	PA4	I/O	PA4	QSPI_NSS0 / SPIS1_NSS / UART2_CK	ADC_IN4
15	21	PA5	I/O	PA5	QSPI_SCK / SPIS1_SCK	ADC_IN5
16	22	PA6	I/O	PA6	TIM1_BKIN / TIM3_CH1 / QSPI_MI_IO1 / SPIS1_SO	ADC_IN6
17	23	PA7	I/O	PA7	TIM1_CH1N / TIM3_CH2 / QSPI_MO_IO0 / SPIS1_SI	ADC_IN7
-	24	PC4	I/O	PC4	TRACECK	ADC_IN14
-	25	PC5	I/O	PC5	SPIM2_NSS2 / TRACED0	ADC_IN15
18	26	PB0	I/O	PB0	TIM1_CH2N / TIM3_CH3 / I2S_MCLK / QSPI_IO2	ADC_IN8
19	27	PB1	I/O	PB1	TIM1_CH3N / TIM3_CH4 / QSPI_IO3	ADC_IN9
20	28	PB2	I/O	PB2/BOOT1		
21	29	PB10	I/O	PB10	TIM2_CH3 / TIM4_CH1 / QSPI_NSS2 / UART3_TX	
22	30	PB11	I/O	PB11	TIM2_CH4 / SPIM2_NSS1 / UART3_RX	
23	31	VSS_1	S	VSS_1		
24	32	VDD_1	S	VDD_1		
25	33	PB12	I/O	PB12	TIM1_BKIN /I2S_WS /SPIM2_NSS0/ SPIS2_NSS/UART3_CK	
26	34	PB13	I/O	PB13	TIM1_CH1N /I2S_SCLK /SPIM2_SCK /SPIS2_SCK /UART3_CTS	
27	35	PB14	I/O	PB14	TIM1_CH2N / SPIM2_MI /SPIS2_SO /UART3_RTS	
28	36	PB15	I/O	PB15	TIM1_CH3N / SPIM2_MO /SPIS2_SI /I2S_SD0	
-	37	PC6	I/O	PC6	TIM3_CH1 / I2S_MCLK	
-	38	PC7	I/O	PC7	TIM3_CH2 / I2S_MCLK	
-	39	PC8	I/O	PC8	TIM3_CH3	
-	40	PC9	I/O	PC9	TIM3_CH4 / TRACED1	
29	41	PA8	I/O	PA8	TIM1_CH1 / UART1_CK / MCO	CMPA_P0
30	42	PA9	I/O	PA9	TIM1_CH2 / UART1_TX	CMPA_N0
31	43	PA10	I/O	PA10	TIM1_CH3 / UART1_RX	
32	44	PA11	I/O	PA11	TIM1_CH4 / UART1_CTS	USBDM
33	45	PA12	I/O	PA12	TIM1_ETR / UART1_RTS	USBDP
34	46	PA13	I/O	SWDIO	QSPI_NSS1	CMPA_P3
35	47	VSS_2	S	VSS_2		
36	48	VDD_2	S	VDD_2		
37	49	PA14	I/O	SWDCLK	QSPI_NSS2	CMPA_N3
38	50	PA15	I/O	PA15	TIM2_CH1_ETR/ I2S_WS/ I2C1_SMBAI/ QSPI_NSS0/ SPIS1_NSS	CMPB_P3
-	51	PC10	I/O	PC10	UART3_TX / TRACED2	CMPB_P1
-	52	PC11	I/O	PC11	UART3_RX / TRACED3	CMPB_P2
-	53	PC12	I/O	PC12	TIM4_ETR / UART3_CK	CMPB_N0
-	54	PD2	I/O	PD2	TIM3_ETR	CMPB_P0
39	55	PB3	I/O	PB3	SWO / TIM2_CH2 / I2S_SCLK / QSPI_SCK / SPIS1_SCK	CMPB_N3
40	56	PB4	I/O	PB4	TIM3_CH1 / QSPI_MI_IO1 / SPIS1_SO	CMPA_P1
41	57	PB5	I/O	PB5	TIM3_CH2 / I2S_SD1 / I2C1_SMBAI / QSPI_MO_IO0 / SPIS1_SI	CMPA_P2

(continued)

Pin No.		Pin Name	Type	Main Function	Alternate Function	Analog Function
LQFP48	LQFP64					
42	58	PB6	I/O	PB6	TIM4_CH1 / I2C1_SCL / QSPI_NSS1 / UART1_TX	CMPA_N1
43	59	PB7	I/O	PB7	TIM4_CH2 / I2C1_SDA / SPIM2_NSS1 / UART1_RX	CMPA_N2
44	60	BOOT0	I	BOOT0		
45	61	PB8	I/O	PB8	TIM4_CH3 / I2C1_SCL / SPIM2_NSS2 / UART1_CTS	CMPB_N1
46	62	PB9	I/O	PB9	TIM4_CH4 / I2C1_SDA / UART1_RTS	CMPB_N2
47	63	VSS_3	S	VSS_3		
48	64	VDD_3	S	VDD_3		

[1] Function availability depends on the chosen device.
[2]symbols: S-supply, I-input, I/O-input/output

Tab 3.3-2 WB32FQ95xC pin definition

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS	TIM1/2	TIM3/4	I2S	I2C	SPI(M)	SPI(S)	UART
PA0	WKUP	TIM2_CH1 TIM2_ETR						UART2_CTS
PA1		TIM2_CH2						UART2_RTS
PA2		TIM2_CH3						UART2_TX
PA3		TIM2_CH4						UART2_RX
PA4						QSPI_NSS0	SPIS1_NSS	UART2_CK
PA5						QSPI_SCK	SPIS1_SCK	
PA6		TIM1_BKIN	TIM3_CH1			QSPI_MI_IO1	SPIS1_SO	
PA7		TIM1_CH1N	TIM3_CH2			QSPI_MO_IO0	SPIS1_SI	
PA8	MCO	TIM1_CH1						UART1_CK
PA9		TIM1_CH2						UART1_TX
PA10		TIM1_CH3						UART1_TX
PA11		TIM1_CH4						UART1_TX
PA12		TIM1_ETR						UART1_RTS
PA13	SWO_DIO					QSPI_NSS1		
PA14	SWO_CLK					QSPI_NSS2		
PA15		TIM2_CH1 TIM2_ETR		I2S_WS	I2C_SMBAI	QSPI_NSS0	SPIS1_NSS	
PB0		TIM1_CH2N	TIM3_CH3	I2S_MCLK		QSPI_IO2		
PB1		TIM1_CH3N	TIM3_CH4			QSPI_IO3		
PB2	BOOT1							
PB3	SWO	TIM2_CH2		I2S_SCLK		QSPI_SCK	SPIS1_SCK	
PB4			TIM3_CH1			QSPI_MI_IO1	SPIS1_SO	
PB5			TIM3_CH2	I2S_SD1	I2C1_SMBAI	QSPI_MO_IO0	SPIS1_SI	
PB6			TIM4_CH1		I2C1_SCL	QSPI_NSS1		UART1_TX
PB7			TIM4_CH2		I2C1_SDA	SPIM2_NSS1		UART1_RX
PB8			TIM4_CH3		I2C1_SCL	SPIM2_NSS2		UART1_CTS
PB9			TIM4_CH4		I2C1_SDA			UART1_RTS
PB10		TIM2_CH3	TIM4_CH1		I2C2_SCL	QSPI_NSS2		UART3_TX
PB11		TIM2_CH4			I2C2_SDA	SPIM2_NSS1		UART3_RX
PB12		TIM1_BKIN		I2S_WS		SPIM2_NSS0	SPIS2_NSS	UART3_CK
PB13		TIM1_CH1N		I2S_SCLK		SPIM2_SCK	SPIS2_SCK	UART3_CTS
PB14		TIM1_CH2N				SPIM2_MI	SPIS2_SO	UART3_RTS
PB15		TIM1_CH3N		I2S_SD0		SPIM2_MO	SPIS2_SI	
PC0				I2S_WS		SPIM2_NSS0	SPIS2_NSS	
PC1				I2S_SCLK		SPIM2_SCK	SPIS2_SCK	
PC2				I2S_SD0		SPIM2_MI	SPIS2_SO	
PC3				I2S_SD1		SPIM2_M0	SPIS2_SI	
PC4	TRACECK							
PC5	TRACED0					SPIM2_NSS2		
PC6			TIM3_CH1	I2S_MCLK				
PC7			TIM3_CH2	I2S_MCLK				

(continue)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SYS	TIM1/2	TIM3/4	I2S	I2C	SPI(M)	SPI(S)	UART
PC8			TIM3_CH3					
PC9	TRACED1		TIM3_CH4					
PC10	TRACED2							UART3_TX
PC11	TRACED3							UART3_RX
PC12			TIM4_ETR					UART3_CK
PC13	TAMPER_RTC							
PC14	OSC32_IN							
PC15	OSC32_OUT							
PD0	OSC_IN							
PD1	OSC_OUT							
PD2			TIM3_ETR					

4 Device Function Description

4.1 ARM Cortex™-M3 core

Cortex™ M3 is a 32-bit RISC processor core with three levels pipeline. It includes the AMBA-Lite interface and is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), which is a low cost but high performance MCU platform. It has optional hardware debugging function, can execute Thumb-2 instruction, and is compatible with other Cortex-M series.

WB32FQ95xC performance line family incorporates the ARM ®Cortex™-M3 processor core, so it is compatible with all ARM tools and software.

4.2 Memory map

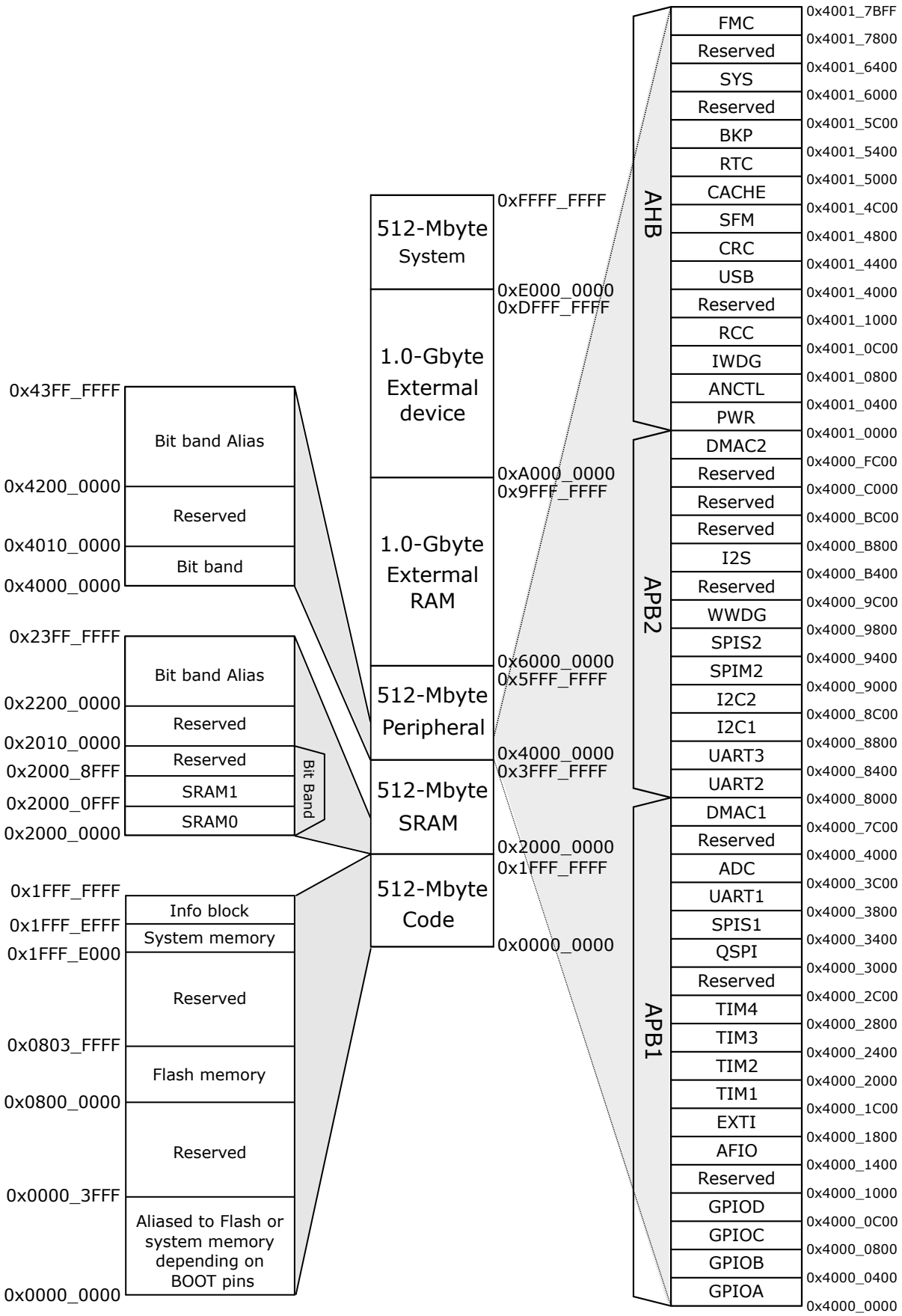
Program memory, data memory, system memory and AHB/APB peripherals are organized within the same linear 4-GB address space. The addressable memory space is divided into 8 main blocks, each of 512 MB.

AHB peripheral address space is 64KB, can support up to 64 peripherals. APB peripheral address space is 64KB, each peripheral can use up to 1KB address space. APB peripheral only support word access, byte and half-word accesses are not supported.

System memory address space is 4KB and reserved for ISP program.

The WB32FQ95xC memory map is organized below:

Fig 4.2-1 WB32FQ95xC memory map



4.3 System reset

System reset can be triggered by the sources below:

- POR reset (POR)
- NRST
- WDG reset (IWDG and WWDG)
- CPU Software reset
- Exiting standby mode

Any source above can trigger the sysrem reset. When the working voltage is proper, the MHSI will be turned on and keep active. When NRST is asserted to high level, the oscillator will start running, and the flash controller will finish the device initilization.

4.4 NVIC

Cortex™-M3 is tightly coupled with the Nested Vectored Interrupt Controller (NVIC). This hardware block provides flexible interrupt management features with minimal interrupt latency.

The main feature includes:

- low latency interrupt processing
- handle the system exceptions/faults and peripheral interrupts/events
- support up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3)
- four programmable levels for the interrupt priority
- generate the software interrupt
- configurable Non Maskable Interrupt (NMI).

4.5 EXTI

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests.

4.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock, internal RC 48 MHz oscillator or clock output from PLL can be selected as system clock. When An external 4-16 MHz clock is used, it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC 8 MHz oscillator. A software interrupt is generated if enabled.

Several prescalers allow the configuration frequency of the AHB, APB1 and APB2 domains. The maximum frequency of the AHB, APB1 and APB2 is 96MHz, and the frequency of them can be configured independently.

4.7 Power supply schemes

- VDD = 2.0∼3.6V: external power supply for I/Os and the internal regulator.
  Provided externally through VDD pins.
- VDDA = 2.4∼3.6V: external analog power supplies for ADC, and the minimum voltage should be 2.4 V when the ADC is used.
- VBAT = 1.8∼3.6V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

Note: *VDDA must be the same potential as VDD. It is recommended to power VDD and VDDA from the same source.*

4.8 DMAC

Two general-purpose DMACs, each have 3 channels and up to 16 hardware DMA requests (16 requests forDMAC0 and 12 requests for DMAC1) are able to manage memory-to-memory, peripheral-to-memory and memoryto-peripheral transfers. The two DMA controllers have internal arbitor to arbitrate the priority of DMA requests.

Each channel can be configured with to hardware DMA requests, or also support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, UART, TIMx and ADC.

4.9 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBAT pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

4.10 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

4.11 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

4.12 System Tick

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter.

It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.

- Clock source is fixed to 1/8 of CPU frequency

4.13 General-purpose timers

There are up to 3 synchronizable general-purpose timers (TIM2, TIM3 and TIM4) embedded in the WB32FQ95xC performance line devices. These timers are based on a 20-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one- pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

4.14 Advanced-control timer

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 20-bit timer, it has the same features as the TIMx timer. If configured as the 20-bit PWM generator, it has full modulation capability (0-100%). In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers which have the same architecture. The advanced-control timer can therefore work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

4.15 I2C bus

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard ($<= 100Kb/s$), fast mode ($<= 400Kb/s$) and high speed mode($<= 3.4Mb/s$).

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). Ahardware CRC generation/verification is embedded.

They can be served by DMA and They support SMBus 2.0/PMBus.

4.16 Inter-integrated sound (I2S)

One standard I2S interface is available, it is operated in master mode. The interface can be configured to operate with 16/32 bit resolution, as input or output channels. The master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

4.17 Universal asynchronous receiver transmitters (UART)

Up to three universal asynchronous receiver transmitters (UART1, UART2 and UART3), These three interfaces provide asynchronous communication, IrDA SIR support.

UART1, UART2 and UART3 interfaces are able to communicate at speeds of up to 6.0 Mbit/s. They also provide hardware management of the CTS and RTS signals.

All interfaces can be served by the DMA controller.

4.18 Serial peripheral interface (SPI)

SPI and QSPI are able to communicate up to 24 Mbits/s in full-duplex and simplex communication modes. The frame can be configurable to 4bits, 8 bits, 16 bits or 32bits.

Both SPIs and QSPI can be served by the DMA controller.

4.19 USB

One USB device peripheral compatible with the USB fullspeed 12 Mbs. The USB interface implements a fullspeed (12 Mbit/s) function interface. It has softwareconfigurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

4.20 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current- capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

4.21 ADC

One 12-bit analog-to-digital converters is embedded into WB32FQ95xC performance line devices and the ADC support up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

VDDA supply power for ADC, range from 2.4V-3.6V, ADC convert input voltage from 0V to VDDA.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

4.22 Comparators

Up to 2 voltage comparators, each of them has 4 positive input channels and 4 negative input channels.

4.23 Random number generator

One Random number generator, used to generte 8/16/32 bit Random number.

4.24 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from an 8/16/32-bit data word and a fixed generator polynomial.

4.25 Embedded SRAM and Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data.

Up to 36 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

4.26 Power supply supervisor

The device has an integrated power-on reset (POR) /power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.0V. The device remains in reset mode when VDD is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD /VDDA power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD /VDDA drops below the V_{PVD} threshold and/or when VDD /VDDA is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

4.27 Low-power modes

WB32FQ95xC supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the MHSI RC, the FHSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm.
- **Standby mode**
  The Standby mode is used to achieve the lowest power consumption. The internalvoltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the MHSI, the FHSI and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on

the WKUP pin, or an RTC alarm occurs.

Note: *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

4.28 SWD Debug Port

The ARM SWJ-DP Interface is embedded, and is a serial wire debug port that enables a serial wire debug to be connected to the target.

5 Electrical Characteristics

5.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 5.1-1: Voltage characteristics, Table 5.1-2: Current characteristics, and Table 5.1-3: Thermal characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5.1.1 Voltage characteristics

Tab 5.1-1 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
VDD - VSS	External main supply voltage (including VDDA, VDD)[1]	-0.5	3.6	V
VIN	Input voltage on pin [2]	VSS - 0.3	VDD + 0.5	
$\|\Delta VDDx\|$	Variations between different VDD power pins	-	50	mV
$\|VSSx$ - VSS$\|$	Variations between all the different ground pins	-	50	

[1] All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power.
[2] VIN maximum value must always be respected.

5.1.2 Current characteristics

Tab 5.1-2 Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into VDD power lines (source)[1]	60	mA
I_{VSS}	Total current out of VSS ground lines (sink)	60	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/Os and control pin	-16	
$I_{INJ(PIN)}$ [2]	Injected current on five-volt tolerant I/O	60	
$\sum I_{INJ(PIN)}$ [3]	Total injected current (sum of all I/O and control pins)	60	

[1] All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
[2] $I_{INJ(PIN)}$ must never be exceeded. A positive injection is induced by VIN>VDD while a negative injection is induced by VIN<VSS.
[3] When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.1.3 Thermal characteristics

Tab 5.1-3 Thermal characteristics

Symbel	Rating	Value	Unit
T_{STG}	Storage temperature range	-40 ~ +150	°C
T_J	Maximum junction temperature	100	

5.2 Operating conditions

5.2.1 General operating conditions

Symbel	Parameter	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	96	
f_{PCLK2}	Internal APB2 clock frequency	0	96	
VDD	Standard operating voltage	2	3.6	V
VDDA	Analog operating voltage(ADC not used)	2	3.6	
	Analog operating voltage(ADC used)	2.4	3.6	
VBAT	Backup operating voltage	1.8	3.6	
T	Ambient temperature	-40	85	°C

[1] It is recommended to power VDD and VDDA from the same source. A maximum difference of 300 mV between VDD and VDDA can be tolerated during power-up and operation

5.2.2 Embedded reset and power control block characteristics

Tab 5.2-2 Power on Reset characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Uint
T_{delay}	RSTN establish time	-	-	40	-	us
$V_{POR/PDR}$	Power on reset threshold	rising edge	-	1.92	-	V
		falling edge	-	1.88	-	V

Tab 5.2-3 PVD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector select (rising edge)	PLS[2:0] = 000	-	2.25	-	V
		PLS[2:0] = 001	-	2.35	-	
		PLS[2:0] = 010	-	2.45	-	
		PLS[2:0] = 011	-	2.55	-	
		PLS[2:0] = 100	-	2.65	-	
		PLS[2:0] = 101	-	2.75	-	
		PLS[2:0] = 110	-	2.85	-	
		PLS[2:0] = 111	-	2.95	-	
	Programmable voltage detector select (falling edge)	PLS[2:0] = 000	-	2.14	-	
		PLS[2:0] = 001	-	2.24	-	
		PLS[2:0] = 010	-	2.34	-	
		PLS[2:0] = 011	-	2.44	-	
		PLS[2:0] = 100	-	2.54	-	
		PLS[2:0] = 101	-	2.64	-	
		PLS[2:0] = 110	-	2.74	-	
		PLS[2:0] = 111	-	2.84	-	

5.2.3 External user clock characteristics

Tab 5.2-4 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	8	16	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage		VSS	-	0.3VDD	
$t_{w(HSE)}$	OSC_IN high or low time		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	5	
$C_{in(HSE)}$	OSC_IN input capacitance		-	5	-	pf
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%

Tab 5.2-5 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	-	MHz
V_{LSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{LSEL}	OSC_IN input pin low level voltage		VSS	-	0.3VDD	
$t_{w(LSE)}$	OSC_IN high or low time		450	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	50	
$C_{in(LSE)}$	OSC_IN input capacitance		-	5	-	pf
$DuCy_{(LSE)}$	Duty cycle		45		70	%
$T_{SU(LSE)}$	startup time	VDD is stabilized	-	2	-	s

5.2.4 Internal clock source characteristics

Tab 5.2-6 High-speed internal (MHSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MHSI}	Frequency	-	-	8	-	MHz
$DuCy_{(MHSI)}$	Duty cycle	-	45	-	55	%
		T_A = -10 to 85°C	-1.5	-	2.2	%
$ACC_{(MHSI)}$	Accuracy of the MHSI oscillator	T_A = 0 to 75°C	-1.3	-	2	%
		T_A = 25°C	-1.1	-	1.8	%
$T_{SU(MHSI)}$	MHSI oscillator startup time	VSS ⩽ Vin ⩽ VDD	1	-	2	us
$I_{DD(MHSI)}$	MHSI oscillator power consumption	-	-	25	-	uA

Tab 5.2-7 High-speed internal (FHSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{FHSI}	Frequency	-	-	48	-	MHz
$DuCy_{(FHSI)}$	Duty cycle	-	45	-	55	%
		T_A = -10 to 85°C	-1.5	-	2.2	%
$ACC_{(FHSI)}$	Accuracy of the FHSI oscillator	T_A = 0 to 75°C	-1.3	-	2	%
		T_A = 25°C	-1.1	-	1.8	%
$T_{SU(FHSI)}$	FHSI oscillator startup time	VSS ⩽ Vin ⩽ VDD	200	-	500	ns
$I_{DD(FHSI)}$	FHSI oscillator power consumption	-	-	55	-	uA

Tab 5.2-8 Low-speed internal (LSI) RC oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	20	-	40	kHz
$T_{SU(LSI)}$	LSI oscillator startup time	-	-	-	85	us
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	250	-	nA

5.2.5 PLL characteristics

Tab 5.2-9 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	1	8	16	MHz
	PLL input clock duty cycle	-	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	-	12	-	96	MHz
T_{LOCK}	PLL lock time	-	-	-	200	us
Jitter	Cycle-to-cycle jitter	-	-	-	300	ps

5.2.6 Memory characteristics

Tab 5.2-10 Memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PROG}	Page program time	-	-	2.1	-	ms
t_{ERASE}	Page erase time	-	-	6.4	-	
t_{ME}	Mass erase time	-	-	25.6	-	
IDD_{PROG}	Page program current	-	-	-	2	mA
IDD_{ERASE}	Page erase current	-	-	-	1.5	
IDD_{READ}	Read current@48MHz	-	-	-	4.7	
	Read current@24MHz	-	-	-	2.5	

Tab 5.2-11 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	-	100	-	-	kcycles
T_{RET}	Data retention	-	10	-	-	year

5.2.7 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size is either 3 parts (cumulative mode) or 3 parts x(n + 1) supply pins (non-cumulative mode). The human body model (HBM) can be simulated. The tests are compliant with JESD22-A114/C101 standard.

Tab 5.2-12 ESD absolute maximum ratings

Symbol	Ratings	Conditions	class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JEDEC JS-001-2017	2	2000	V
$V_{ESD(CMD)}$	Electrostatic discharge voltage (charge device mode)	T_A = +25 °C, conforming to JEDEC JS-002-2018	II	500	

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with ANSI/ESDA/JEDEC IC latch-up standard.

Tab 5.2-13 Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +25 °C, compliant with JEDEC 2016	II level A

5.2.8 EFT Characteristics

Tab 5.2-14 EFT Characteristics

Symbol	Parameter	Standard	Voltage	Class
EFT_{IO}	EFT to IO	(IEC61000-4-4)	2KV	4
EFT_{Power}	EFT to Power	(IEC61000-4-4)	4KV	4

Software suggestion

Software flow must contain code to prevent CPU run away, for example:

- Crashed Program Counter.
- Unpredicted Reset.
- Crashed important data in control register.

Increase driven strength of IOs improve the capability of EFT.

5.2.9 IO characteristics

Tab 5.2-15 IO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	-	0.65VDD	2.1	-	V
V_{IL}	Input low level voltage	-	-0.5	6.4	-	
V_{hys}	Schmitt trigger voltage hysteresis	-	0.05VDD	25.6	-	
I_{lkg}	Input leakage current	VSS ⩽ Vin ⩽ VDD	-	-	±1	uA
R_{pu}	Weak pull-up equivalent resistor	Vin = VSS	30	40	50	KΩ
R_{pd}	Weak pull-down equivalent resistor	Vin = VDD	30	40	50	KΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pf

Tab 5.2-16 Input/output AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/O low-speed						
$f_{max(IO)out}$	Maximum frequency	C_L = 50pf VDD=2V to 3.6V	-	-	10	MHz
$t_{f(IO)out}$	Output high to low level fall time		-	-	125	ns
$t_{r(IO)out}$	Output low to high level rise time		-	-	125	ns
I/O high-speed						
$f_{max(IO)out}$	Maximum frequency	C_L = 50pf VDD=2V to 3.6V	-	-	50	MHz
$t_{f(IO)out}$	Output high to low level fall time		-	-	25	ns
$t_{r(IO)out}$	Output low to high level rise time		-	-	25	ns

5.2.10 TIM characteristics

Tab 5.2-17 TIM characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{res(TIM)}$	Input high level voltage	-	1	-	$t_{TIMxCLK}$
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
Res_{TIM}	Timer resolution	-	-	20	bit
$t_{COUNTER}$	20-bit counter clock period when internal clock is selected	-	1	1048576	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count	-	1	65536 x 1048576	$t_{TIMxCLK}$

5.2.11 USB DC electrical characteristics

Tab 5.2-18 USB DC electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	USB operating voltage	-	3.0	3.6	V
V_{DI}	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
V_{CM}	Differential common mode range	Includes VDI range	0.8	2.5	V
V_{SE}	Single ended receiver threshold	-	1.3	2.0	V
V_{OL}	Static output level low	RL of 1.5 kom to 3.6 V		0.3	V
V_{OH}	Static output level high	RL of 15 kom to VSS V	2.8	3.6	V

[1] To be compliant with the USB 2.0 fullspeed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kom resistor to a 3.0 to 3.6 V voltage range.
[2] Based on simulation and avt test results, not tested in production.
[3] RL is the load connected on the USB drivers.

Tab 5.2-19 USB Fullspeed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time	C_L = 50pf	4	20	ns
t_f	Fall time	C_L = 50pf	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
t_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

[1] Based on simulation and avt test results, not tested in production.

5.2.12 CMP characteristics

Tab 5.2-20 CMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage	-	0.6	-	VDD-0.3	V
V_{HYST}	Hysteresis	-	-	2	5	mV
V_{OFF}	Input Offset voltage	-	-	5	15	mV
T_{PGD}	Propagation Delay	-	-	-	200	ns
I_q	Operation Current	-	-	-	8.5	uA

ADC characteristics

Tab 5.2-21 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Power supply	-	2.4	-	3.6	V
f_s	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14MHz	-	-	823	kHz
V_{AIN}	Conversion voltage range	-	0	-	VDDA	V
R_{AIN}	External input impedance	-	-	-	200	Ω
C_{AIN}	External capacitor	-	-	TBD	-	pf
I_{lkg}	Injection current on Analog input	-	-	-	10	uA
R_{ADC}	Sampling switch resistance	-	-	-	1.4	KΩ
C_{ADC}	Internal sample and hold capacitor/12-bit	-	-	15.5	-	pf

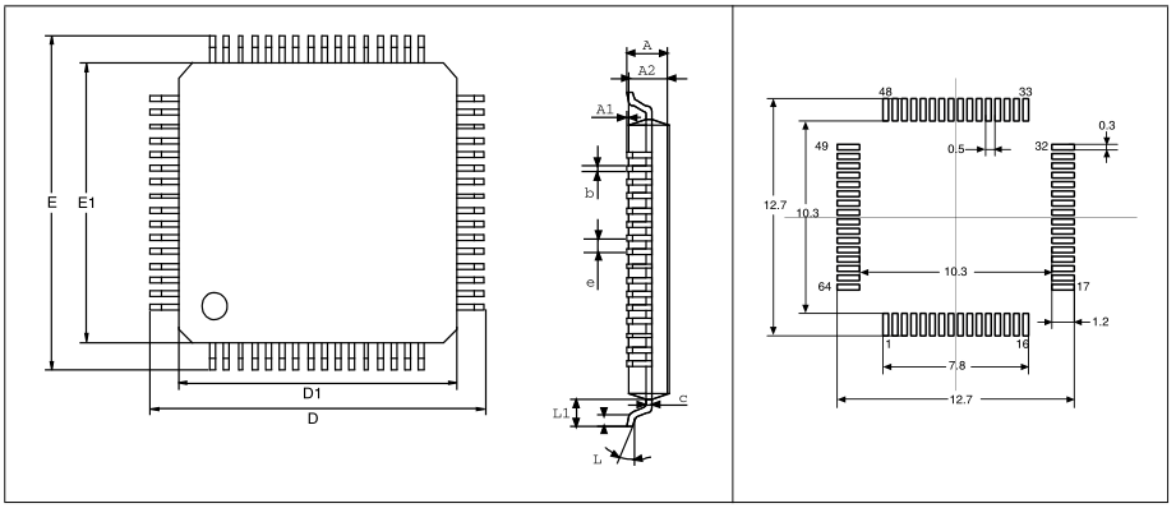
Tab 5.2-22 ADC Conversion time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{AD}	ADC clock cycle	-	62.5	-	-	ns
T_{CONV}	Conversion time	12-bit	-	$13T_{AD}$	-	ns
F_{CONV}	conversion rate	12-bit	-	-	940	KSPS
T_{SAMP}	Sampling time	12-bit	$3T_{AD}$	-	-	ns
t_{DIS}	Dis-charge time	-	-	$0.5T_{AD}$	-	ns
t_{DPU}	Power-up time	-	-	-	10	us

6 Package characteristics

6.1 LQFP64 10x10mm

Fig 6.1-1 LQFP64 10x10mm, 0.5mm pitch and Recommended footprint



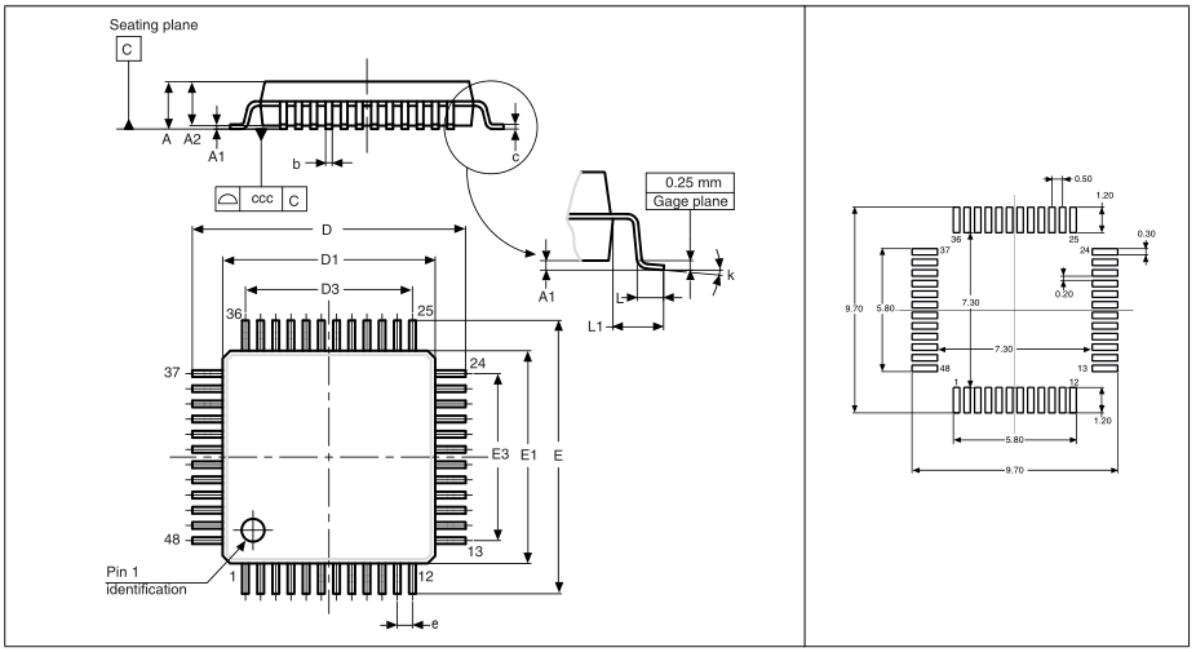
Note1: Drawing is not to scale.
Note2: Dimensions are in millimeters.

Fig 6.1-2 LQFP64 10X10mm, 64 pin package parameters

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

6.2 LQFP48 7X7mm

Fig 6.2-1 LQFP48 7X7mm, 0.5mm pitch and Recommended footprint



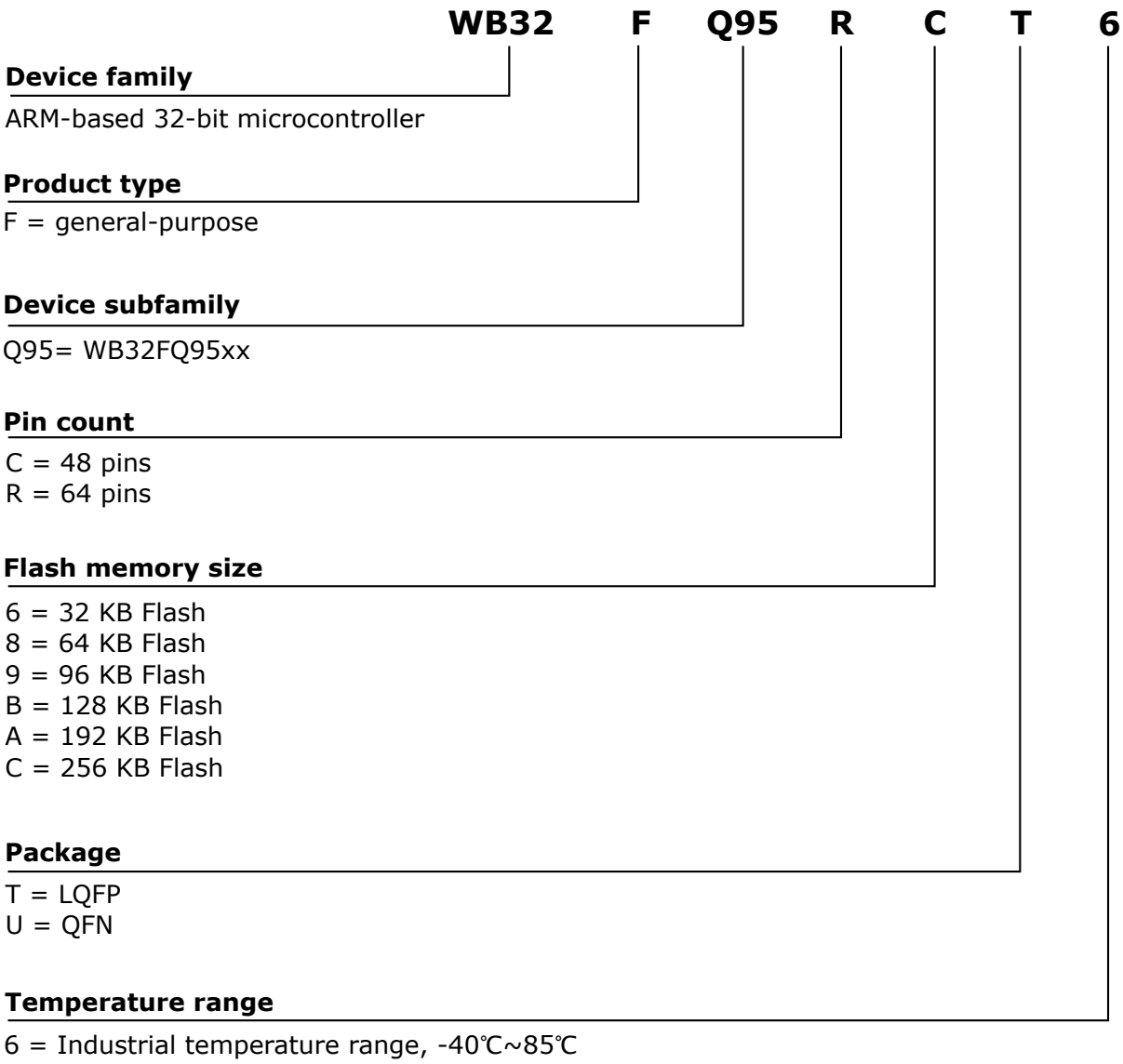
Note1: Drawing is not to scale.
Note2: Dimensions are in millimeters.

Fig 6.2-2 LQFP48 7X7mm, 48 pin package parameters

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

7 Ordering information

Fig 7.0-1 Ordering code information



Tab 7.0-1 MCU selection

USB	1	1
UART	3	3
I2C	2	2
I2S	1	1
SPI (S)	2	2
SPI (M)	1	1
Quad SPI (M)	1	1
Nb COMP Channels	12	16
Nb COMP	2	2
Nb ADC Channels	10	16
Nb ADC 12 bit Cell	1	1
Nb Motor Control Timer	1	1
Nb Timer (20bit)	3	3
Vmax	3.6	3.6
Vmin	2	2
IONb	37	51
Package Name	LQFP48	LQFP64
Ram (Kbytes)	36	36
Flash (Kbytes)	256	256
Core	Cortex-M3	Cortex-M3
Frequency (MHz)	96	96
Commercial Product Code	WB32FQ95CCT6	WB32FQ95RCT6