Computer Architecture
Bus Interconnections

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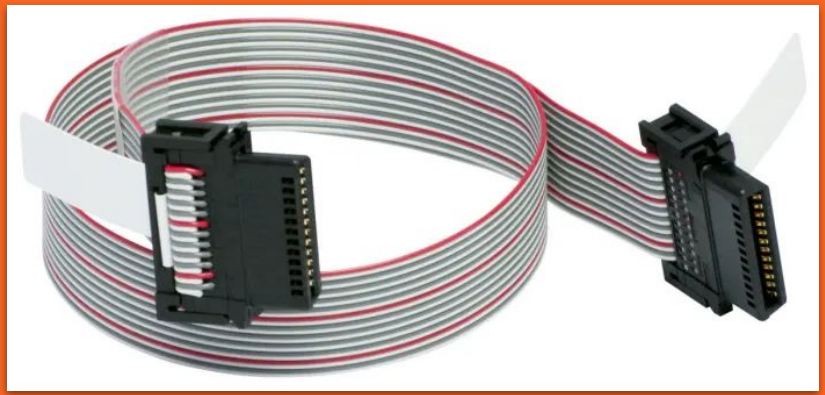
Confession

- Most of the materials have been collected from Internet.
- Images are taken from Internet.
- Various books are used to make these slides.
- Various slides are also used.
- References & credit:
  - Atanu Shome, Assistant Professor, CSE, KU.
  - Computer Organization and Design: the Hardware/Software Interface - Textbook by David A Patterson and John L. Hennessy.
  - Computer Organization and Architecture - Book by William Stallings

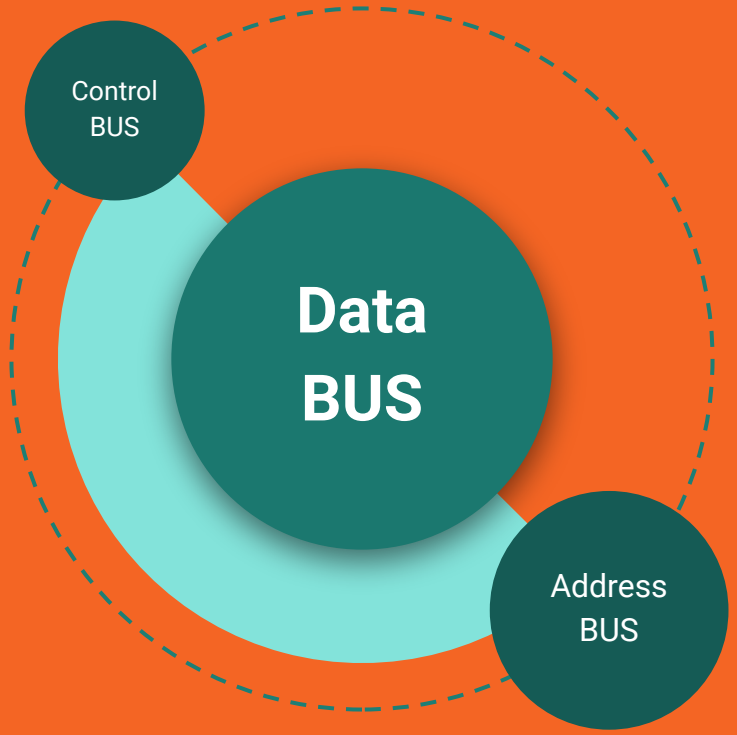
System BUS

A BUS that connects major computer components (processor, memory, I/O) is called a system bus.

The most common computer interconnection structures are based on the use of one or more system buses.



Bus



Data BUS

- Carries data
  - Remember that there is no difference between “data” and “instruction” at this level
- Width is a key determinant of performance
  - 8, 16, 32, 64 bit
- If the data bus is 32 bits wide and each instruction is 64 bits long, then the processor must access the memory module **twice** during each instruction cycle.

Address BUS

- Designate the source or destination of data.
- For example, if the processor wishes to read a word (8, 16, or 32 bits) of data from memory, it puts the address of the desired word on the address lines.
- Clearly, the width of the address bus determines the maximum possible memory capacity of the system.

Control BUS

- Both command and timing information among system modules.

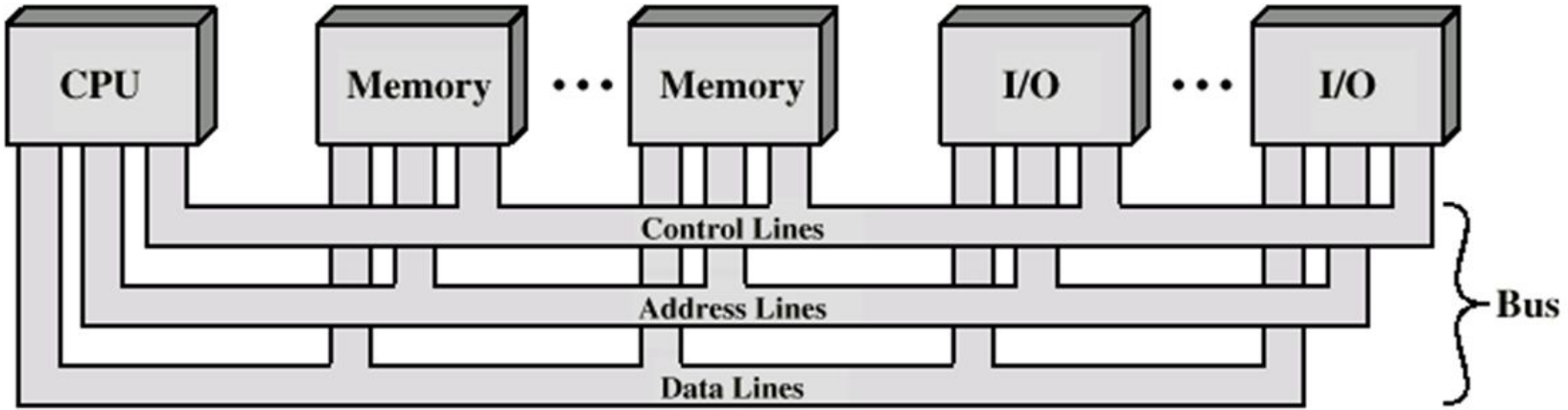
Typical control lines include:

- **Memory write**: causes data on the bus to be written into the addressed location.
- **Memory read**: causes data from the addressed location to be placed on the bus.
- **I/O write**: causes data on the bus to be output to the addressed I/O port.
- **I/O read**: causes data from the addressed I/O port to be placed on the bus.
- **Transfer ACK**: indicates that data have been accepted from or placed on the bus.

Control BUS

- **Bus request**: indicates that a module needs to gain control of the bus.
- **Bus grant**: indicates that a requesting module has been granted control of the bus.
- **Interrupt request**: indicates that an interrupt is pending.
- **Interrupt ACK**: acknowledges that the pending interrupt has been recognized.
- **Clock**: is used to synchronize operations.
- **Reset**: initializes all modules

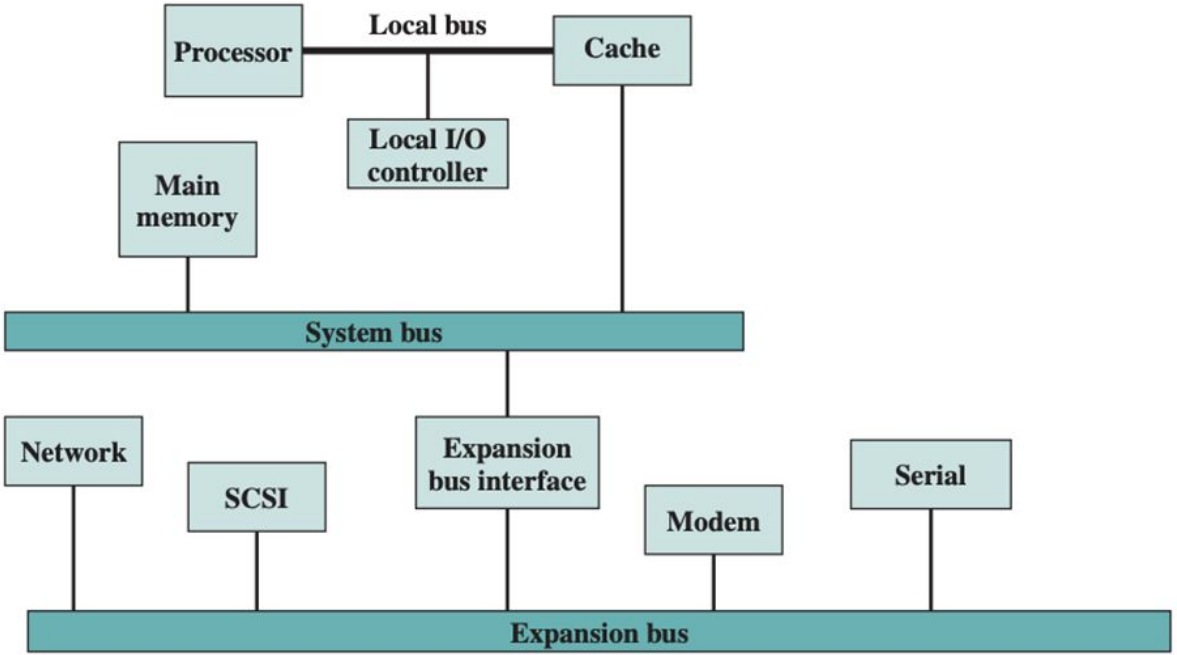
BUS Interconnection Scheme



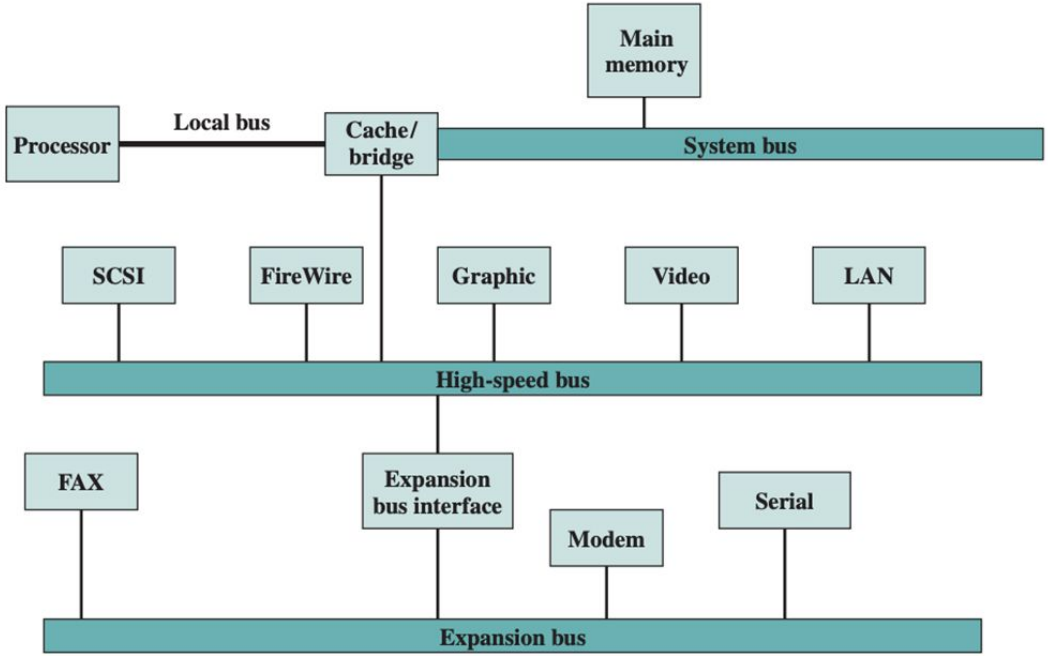
Single BUS Problem

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Traditional (ISA) (with cache)



High Performance BUS



BUS Types

1. **Dedicated**
   - Separate data & address lines
   - assigned to a single function (e.g. address bus) or a physical subset of components
   - (e.g. I/O bus connects all I/O modules).

BUS Types

2. **Multiplexed**
   a bus can be used for both addresses and data. In this case, an address valid control line is needed to determine whether the data is an address or data.

   - Advantage
     - fewer lines
   - Disadvantages
     - More complex control
     - Ultimate performance

BUS Arbitration

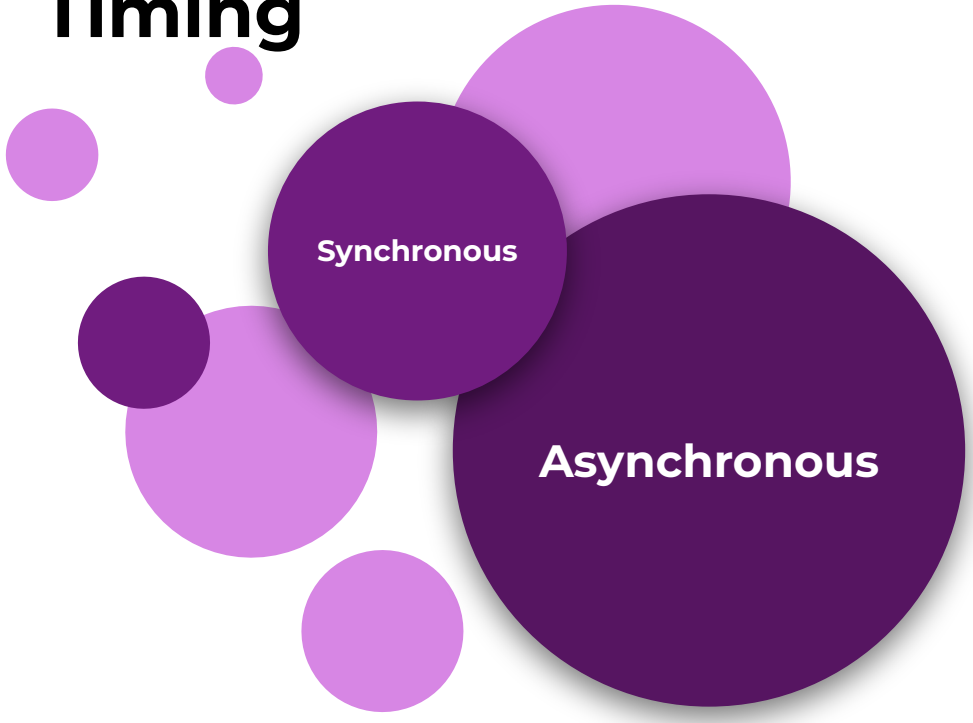
Centralized

a single hardware device known as the bus controller (or arbiter) is responsible for allocating time on the bus.

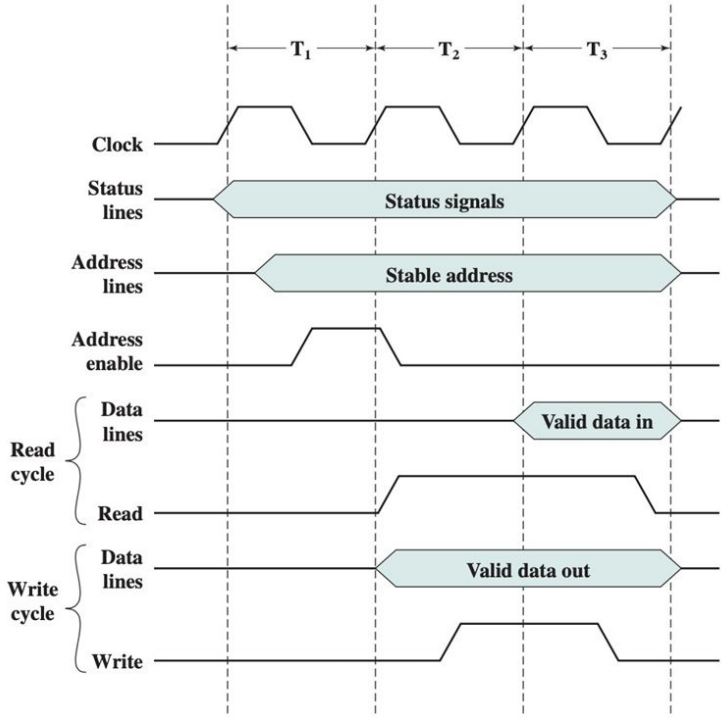
Distributed or Decentralized

with this form of communication there is no central controller. Instead each module has access control logic and the modules act together to share the bus.

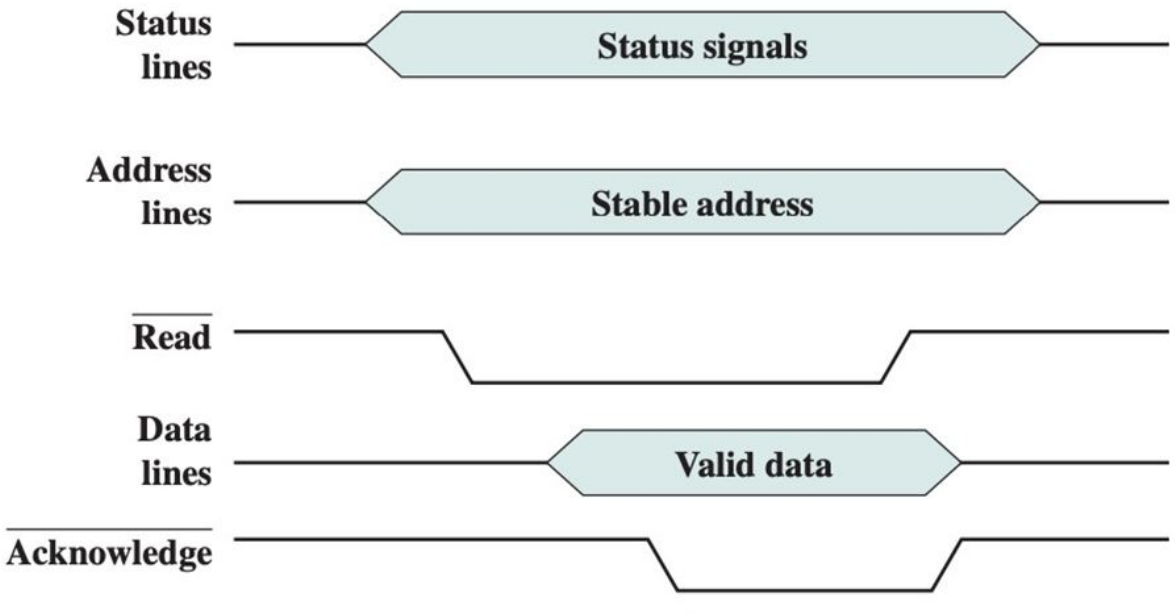
Timing



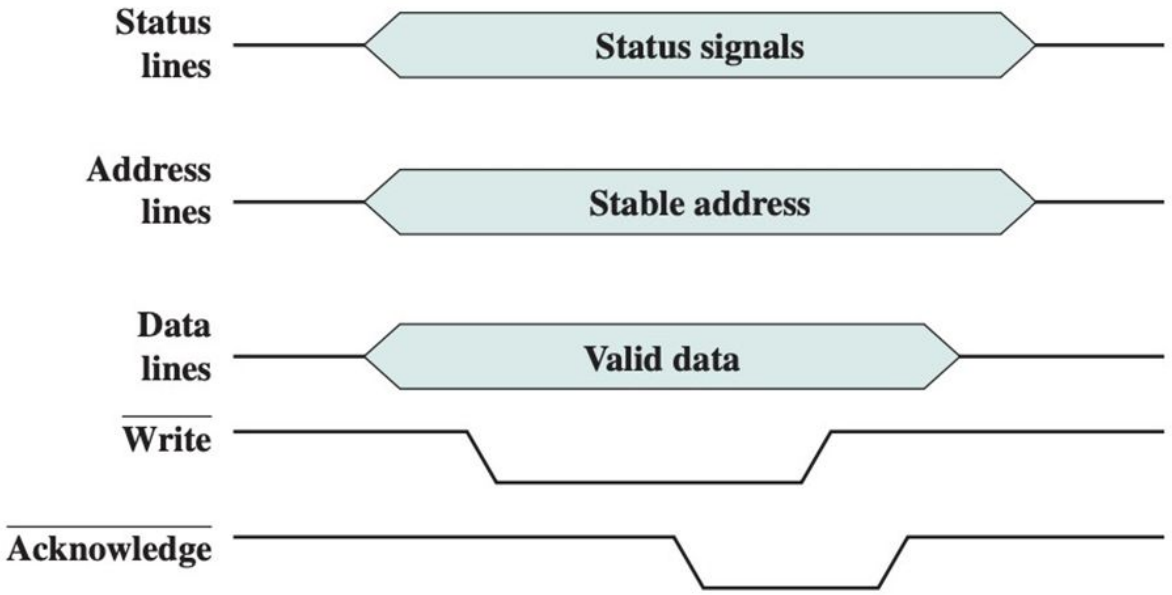
Synchronous Timing Diagram



Asynchronous Timing – Read Diagram



Asynchronous Timing – Write Diagram



(b) System bus write cycle

Thank You