19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

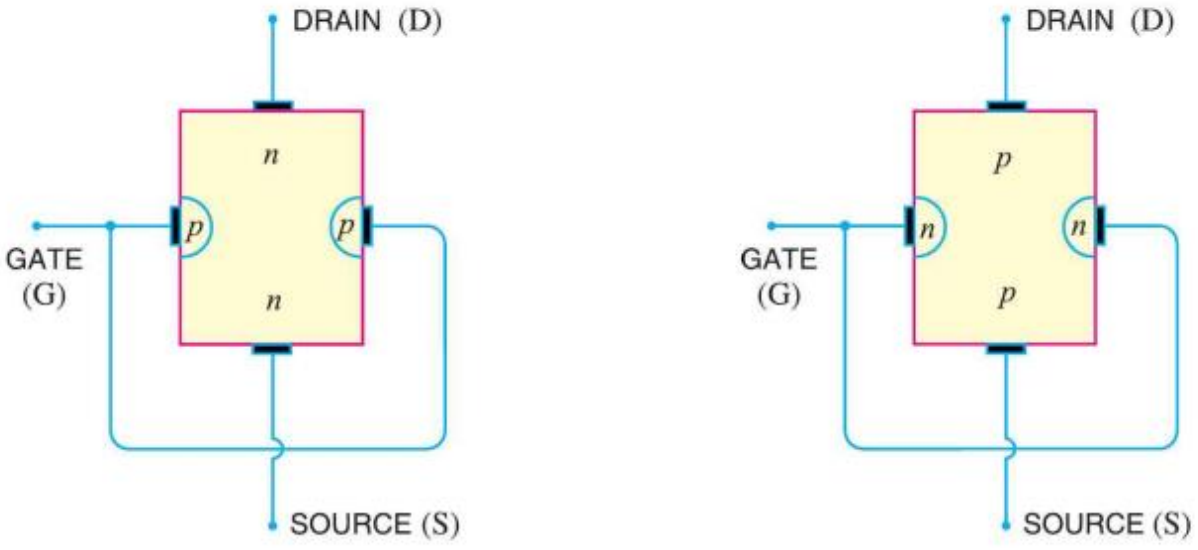
To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET*.

19.2 Junction Field Effect Transistor (JFET)

A **junction field effect transistor** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (*ii*). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).



n-Channel JFET
(*i*)

p-Channel JFET
(*ii*)

Fig. 19.1

JFET polarities. Fig. 19.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 19.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

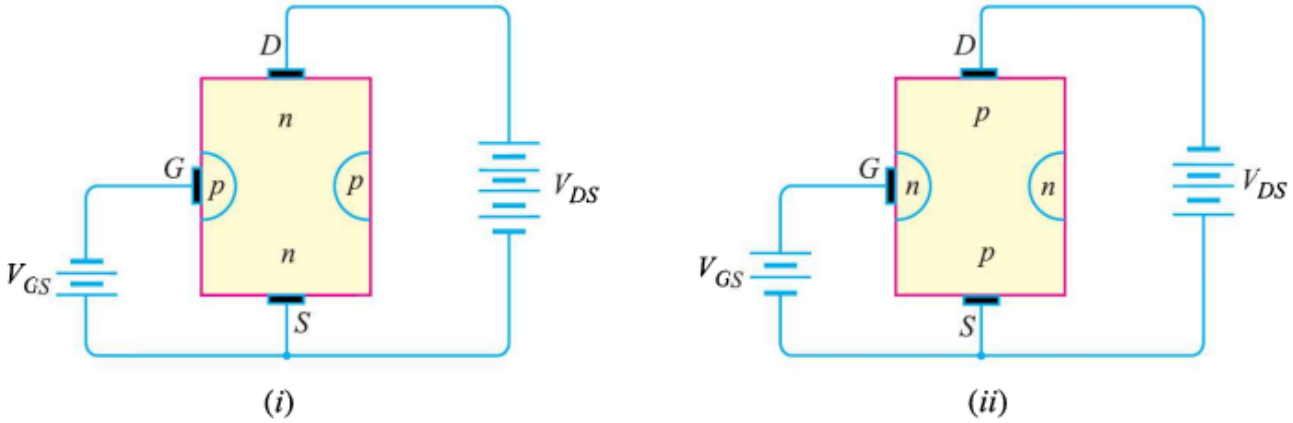


Fig. 19.2

The following points may be noted :

(*i*) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

(*ii*) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

(*iii*) In all *JFETs*, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

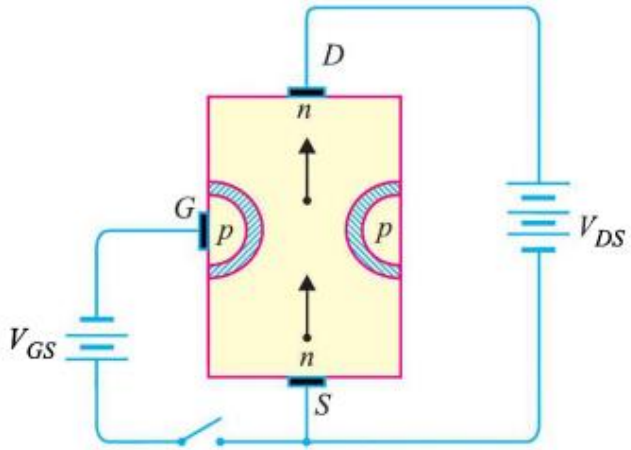
Fig. 19.3 shows the circuit of *n*-channel *JFET* with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence *resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.* In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

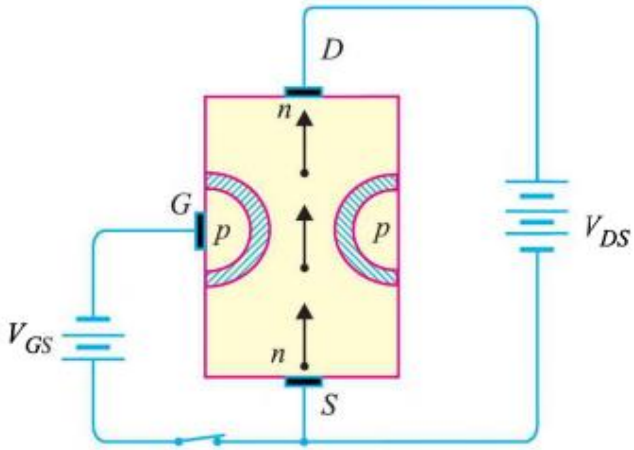
Working. The working of *JFET* is as under :

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.



(*i*)

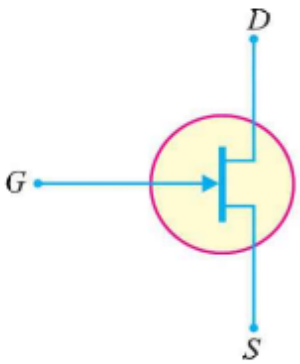


(*ii*)

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

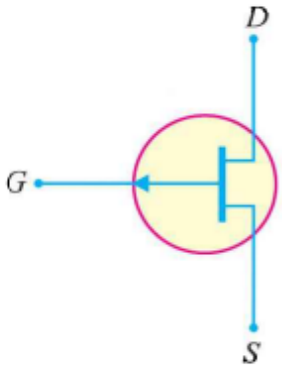
19.4 Schematic Symbol of JFET

Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought



n-Channel *JFET*

(*i*)



p-Channel *JFET*

(*ii*)

Fig. 19.4

as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (*ii*)].

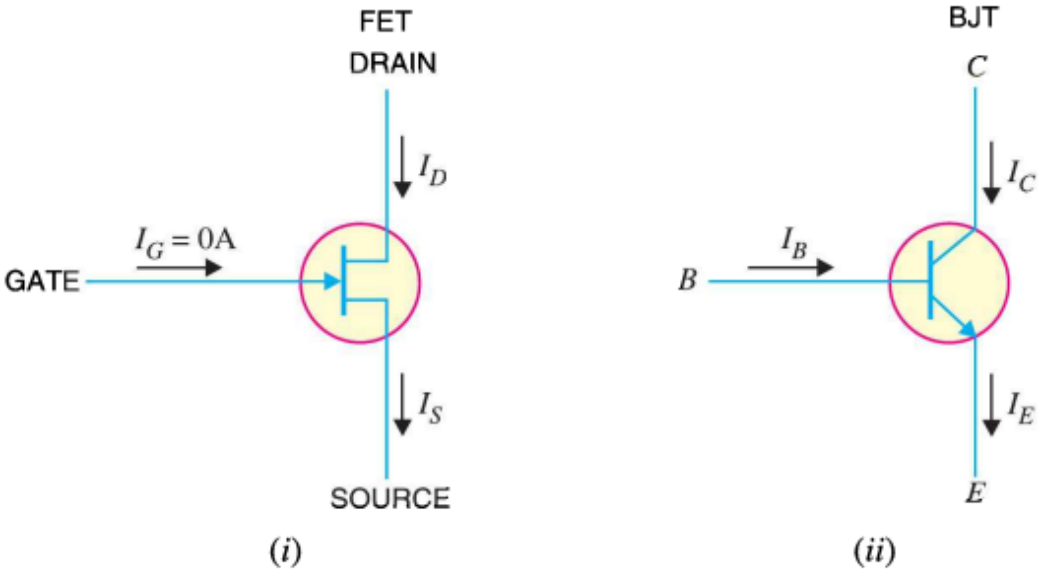
19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0$A). However, typical *BJT* base current might be a few μA while *JFET* gate current a thousand times smaller [See Fig. 19.5].



(*i*) (*ii*)

Fig. 19.5

(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

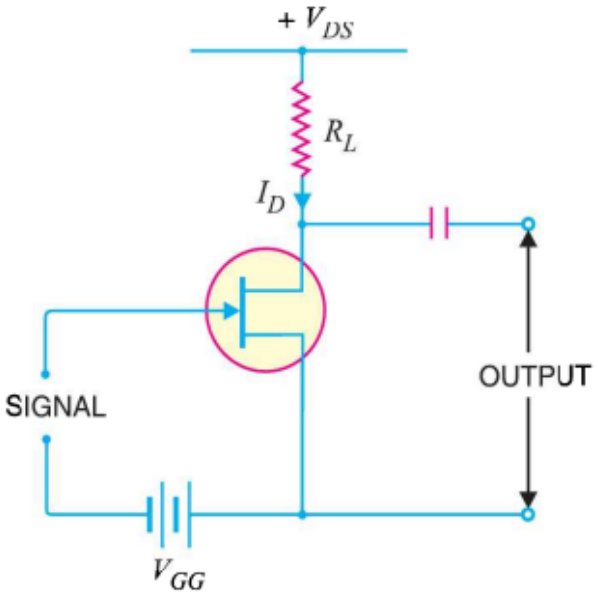


Fig. 19.6

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

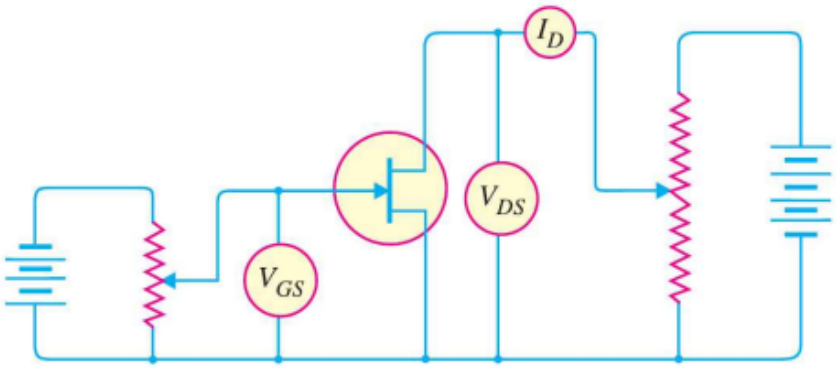


Fig. 19.7

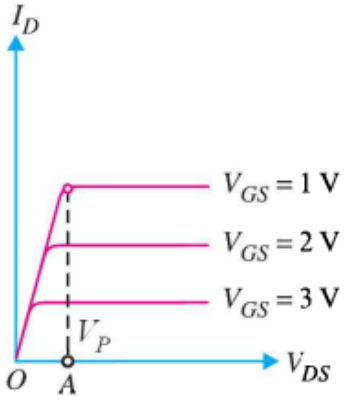


Fig. 19.8

The following points may be noted from the characteristics :

(*i*) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 19.8, *OA* is the *pinch off voltage* V_P.

(*ii*) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(*iii*) The characteristics resemble that of a pentode valve.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. V_{GS} = 0) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current.*

Fig 19.9 shows the *JFET* circuit with V_{GS} = 0 *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

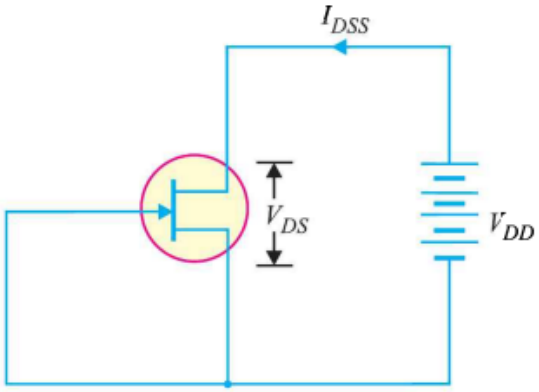


Fig. 19.9

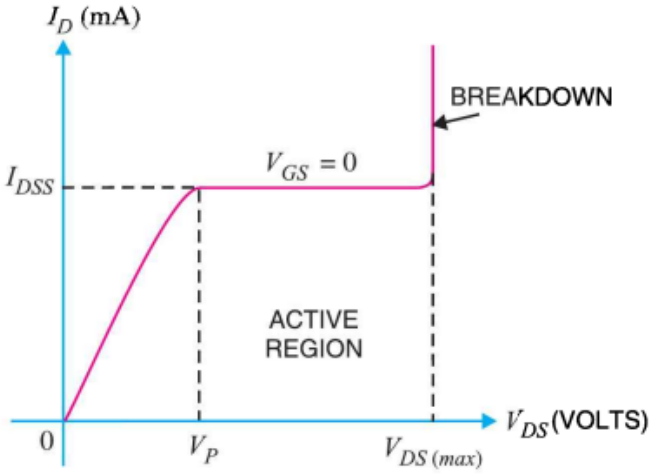


Fig. 19.10

The following points may be noted carefully :

(i) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(ii) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 19.10.

(iii) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or *active region*. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 19.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for $V_{GS} = 0$V, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

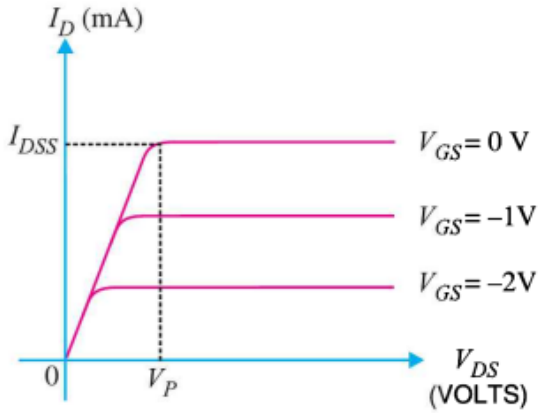


Fig . 19.11

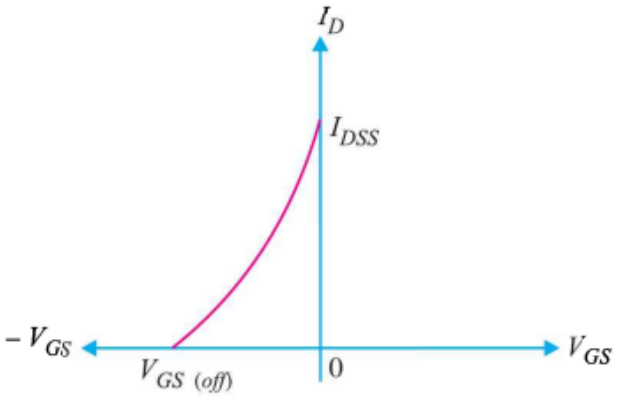


Fig . 19.12

3. Gate-source cut off voltage $V_{GS\,(off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 19.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\,(off)}$.

19.11 Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 19.13. We note that gate-source cut off voltage [*i.e.* $V_{GS\,(off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = |V_{GS\,(off)}|$$

For example, if a *JFET* has $V_{GS\,(off)} = -4\text{V}$, then $V_P = 4\text{V}$.

The transfer characteristic of *JFET* shown in Fig. 19.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where

I_D = drain current at given V_{GS}

I_{DSS} = shorted – gate drain current

V_{GS} = gate–source voltage

$V_{GS\,(off)}$ = gate–source cut off voltage

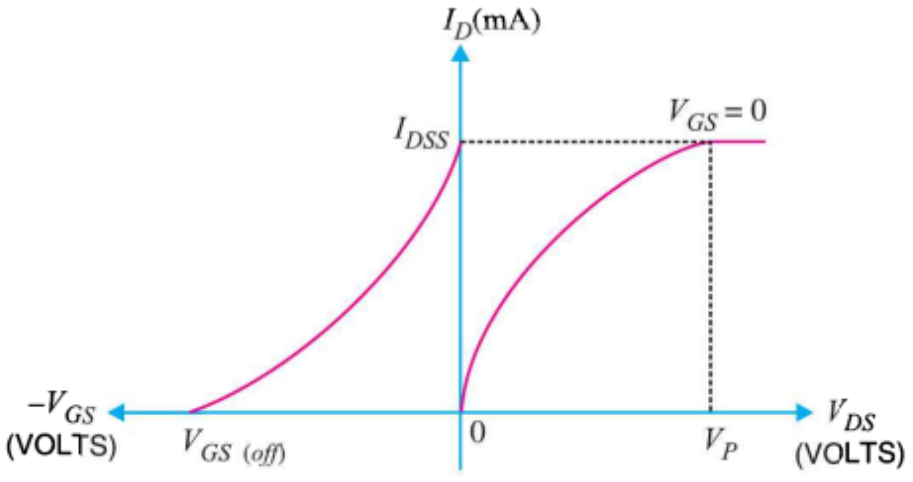


Fig. 19.13

Example 19.1. *Fig. 19.14 shows the transfer characteristic curve of a JFET. Write the equation for drain current.*

Solution. Referring to the transfer characteristic curve in Fig. 19.14, we have,

$$I_{DSS} = 12 \text{ mA}$$
$$V_{GS(off)} = -5 \text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

or
$$I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA} \quad \textbf{Ans.}$$

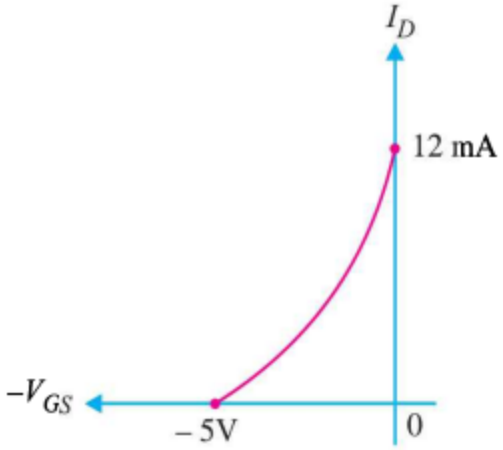


Fig. 19.14

Example 19.4. *For the JFET in Fig. 19.15, $V_{GS(off)} = -4V$ and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

Solution. Since $V_{GS(off)} = -4$V, $V_P = 4$V. The minimum value of V_{DS} for the *JFET* to be in constant-current region is

$$V_{DS} = V_P = 4\text{V}$$

In the constant current region with $V_{GS} = 0$V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$
$$= 4\text{V} + (12 \text{ mA})\,(560\Omega) = 4\text{V} + 6.72\text{V} = \textbf{10.72V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

19.19 JFET with Voltage-Divider Bias

Fig. 19.26 shows potential divider method of biasing a *JFET*. This circuit is identical to that used for a transistor. The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 ($= V_G$) across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$V_{GS} = V_2 - I_D R_S$$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under :

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point. The input impedance Z_i of this circuit is given by ;

$$Z_i = R_1 \| R_2$$

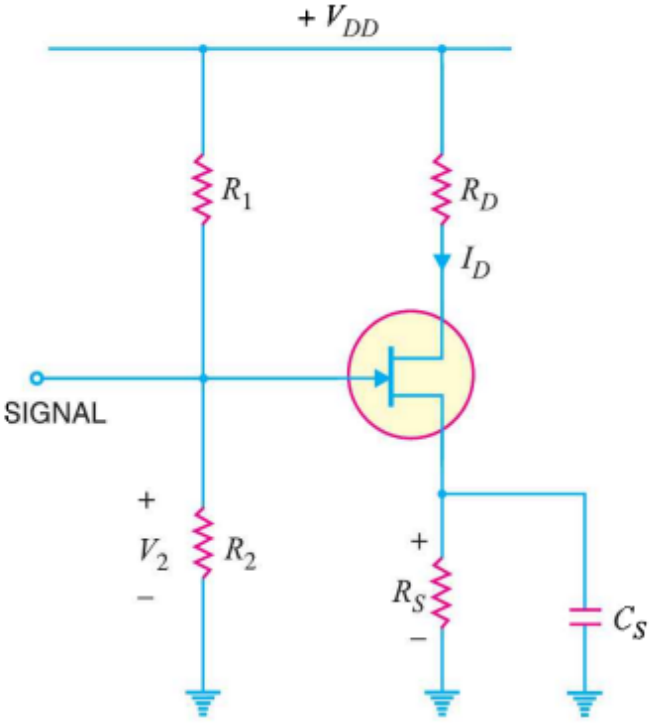


Fig. 19.26

Example 19.21. *In an n-channel JFET biased by potential divider method, it is desired to set the operating point at $I_D = 2.5$ mA and $V_{DS} = 8V$. If $V_{DD} = 30$ V, $R_1 = 1$ MΩ and $R_2 = 500$ kΩ, find the value of R_S. The parameters of JFET are $I_{DSS} = 10$ mA and $V_{GS\,(off)} = -5$ V.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

or $$2.5 = 10\left(1 + \frac{V_{GS}}{5}\right)^2$$

or $$1 + \frac{V_{GS}}{5} = \sqrt{2.5/10} = 0.5$$

or $$V_{GS} = -2.5 \text{ V}$$

Now, $$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{30}{1000 + 500} \times 500$$

$$= 10 \text{ V}$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$10 \text{ V} = -2.5 \text{ V} + 2.5 \text{ mA} \times R_S$$

$$\therefore \quad R_S = \frac{10 \text{ V} + 2.5 \text{ V}}{2.5 \text{ mA}} = \frac{12.5 \text{ V}}{2.5 \text{ mA}}$$

$$= \mathbf{5\ k\Omega}$$

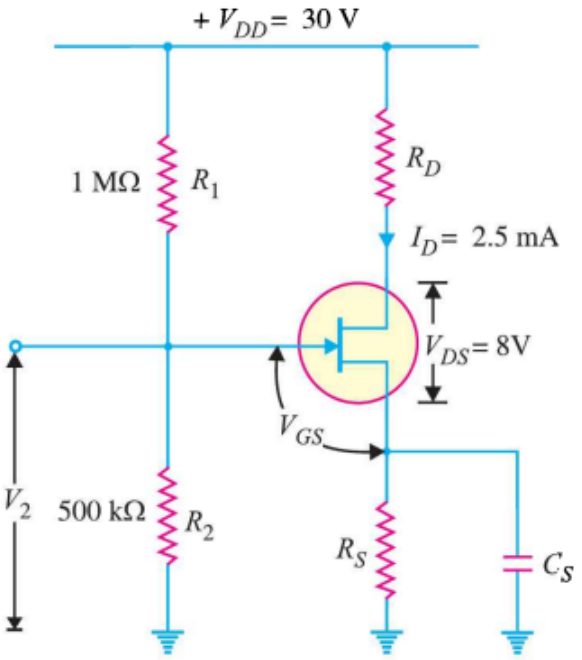


Fig. 19.28

19.28 Types of MOSFETs

There are two basic types of *MOSFETs viz.*

1. Depletion-type *MOSFET* or ***D-MOSFET.*** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET.*
2. Enhancement-type *MOSFET* or ***E-MOSFET.*** The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET.*

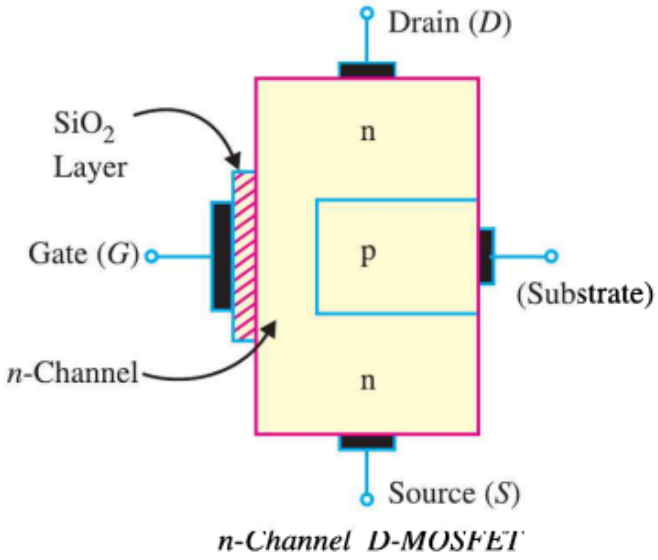
1. D-MOSFET. Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET.* It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(i) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons ($\because$ it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).

(ii) Note carefully the gate construction of *D-MOSFET.* A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET.*

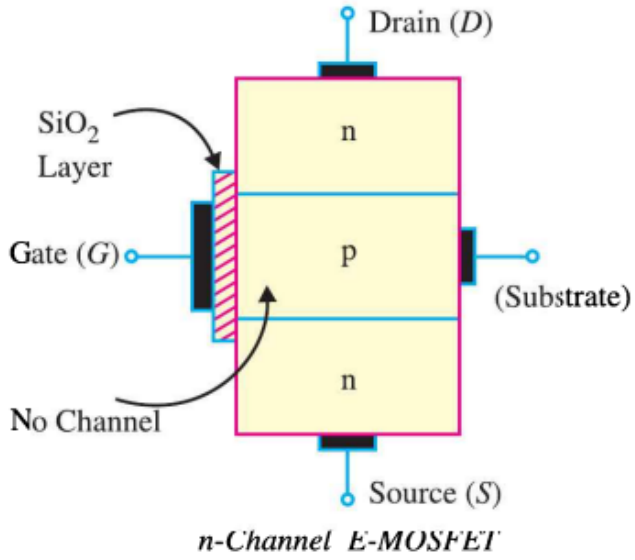
(iii) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals *viz source* (*S*), *gate* (*G*) and *drain* (*D*).

(iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.



n-Channel D-MOSFET

Fig. 19.43

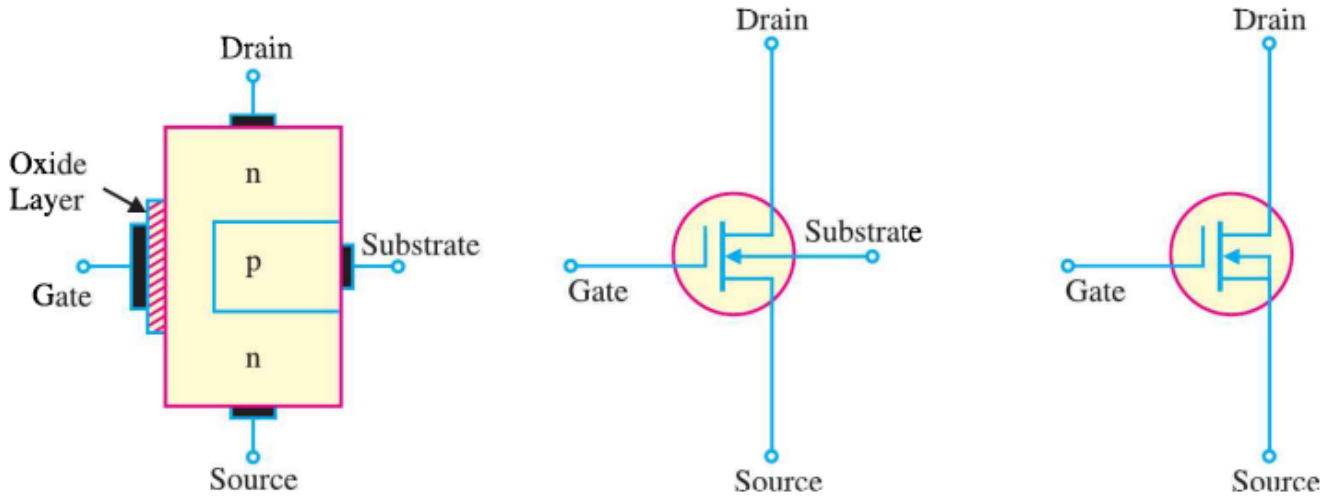


n-Channel E-MOSFET

Fig. 19.44

2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel *E-MOSFET*. Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.

Why the name MOSFET ? The reader may wonder why is the device called *MOSFET?* The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a ***metal oxide semiconductor*** and hence the name *MOSFET*. Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET)*. However, this term is rarely used in place of the term *MOSFET*.



n-Channel D-MOSFET
(*i*)

Symbol
(*ii*)

Symbol
(*iii*)

Fig. 19.45

19.31 D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*. The behaviour of this device can be beautifully explained with the help of this curve as under :

(*i*) The point on the curve where $V_{GS} = 0, I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted *i.e.* $V_{GS} = 0$.

(*ii*) As V_{GS} goes *negative*, I_D decreases below the value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS\,(off)}$ just as with *JFET*.

(*iii*) When V_{GS} is *positive*, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*.

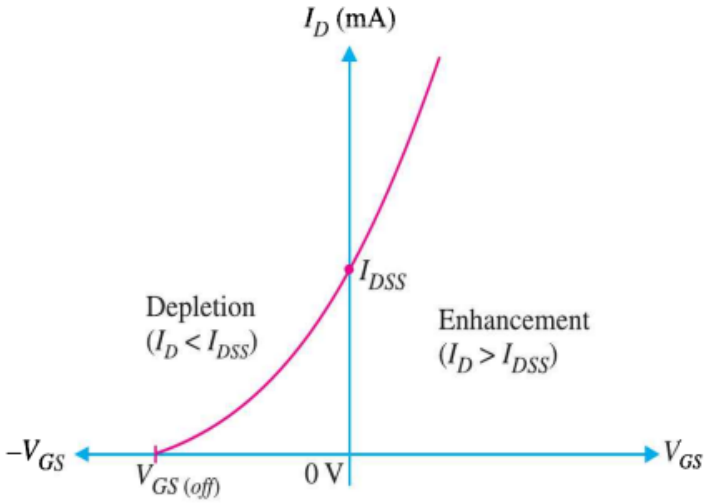


Fig. 19.49

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation *viz.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

20.1 Silicon Controlled Rectifier (SCR)

A silicon *controlled rectifier is a semiconductor **device that acts as a true electronic switch. It can

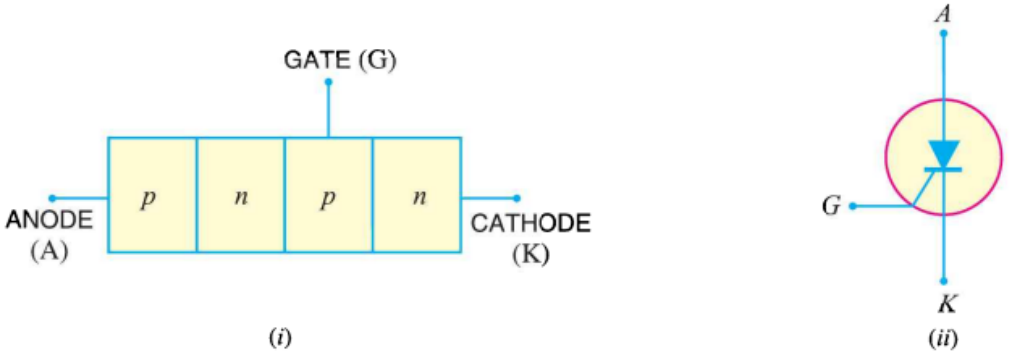


Fig. 20.1

change alternating current into direct current and at the same time can control the amount of powe fed to the load. Thus *SCR* combines the features of a rectifier and a transistor.

20.3 Equivalent Circuit of SCR

The *SCR* shown in Fig. 20.4 (*i*) can be visualised as separated into two transistors as shown in

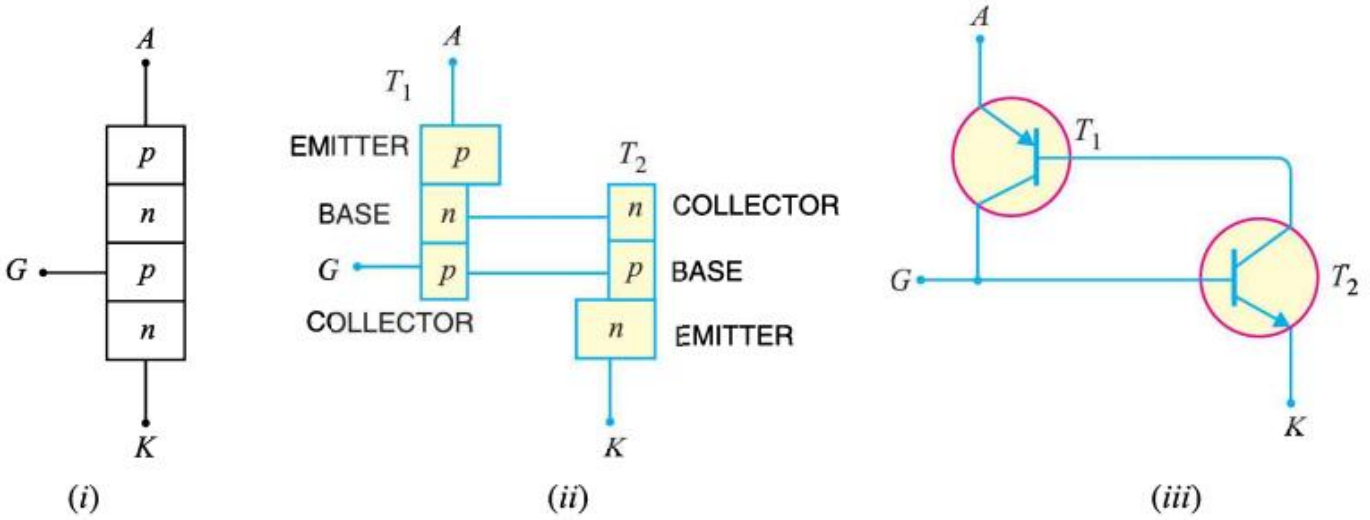


Fig. 20.4

Fig. 20.4 (*ii*). Thus, the equivalent circuit of *SCR* is composed of *pnp* transistor and *npn* transistor connected as shown in Fig. 20.4. (*iii*). It is clear that collector of each transistor is coupled to the base of the other, thereby making a positive feedback loop.

The working of *SCR* can be easily explained from its equivalent circuit. Fig. 20.5. shows the equivalent circuit of *SCR* with supply voltage V and load resistance R_L. Assume the supply voltage V is less than breakover voltage as is usually the case. With gate open (*i.e.* switch S open), there is no base current in transistor T_2. Therefore, no current flows in the collector of T_2 and hence that of T_1. Under such conditions, the *SCR* is open. However, if switch S is closed, a small gate current will flow through the base of T_2 which means its collector current will increase. The collector current of T_2 is the base current of T_1. Therefore, collector current of T_1 increases. But collector current of T_1 is the base current of T_2. This action is accumulative since an increase of current in one transistor causes an increase of current in the other transistor. As a result of this action, both

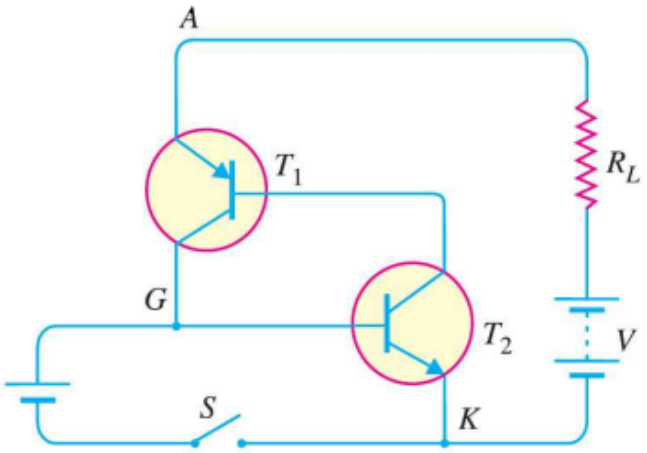


Fig. 20.5

transistors are driven to saturation, and heavy current flows through the load R_L. Under such conditions, the *SCR* closes.

Holding current. *It is the maximum anode current, gate being open, at which SCR is turned off from ON conditions.*

As discussed earlier, when *SCR* is in the conducting state, it cannot be turned *OFF* even if gate voltage is removed. The only way to turn off or open the *SCR* is to reduce the supply voltage to almost zero at which point the internal transistor comes out of saturation and opens the *SCR*. The anode current under this condition is very small (a few mA) and is called *holding current*. Thus, if an *SCR* has a holding current of 5mA, it means that if anode current is made less than 5mA, then *SCR* will be turned off.

(*i*) **Breakover voltage.** *It is the minimum forward voltage, gate being open, at which SCR starts conducting heavily i.e. turned on.*

Thus, if the breakover voltage of an *SCR* is 200 V, it means that it can block a forward voltage (*i.e. SCR* remains open) as long as the supply voltage is less than 200 V. If the supply voltage is more than this value, then *SCR* will be turned on. In practice, the *SCR* is operated with supply voltage less than breakover voltage and it is then turned on by means of a small voltage applied to the gate. Commercially available *SCRs* have breakover voltages from about 50 V to 500 V.

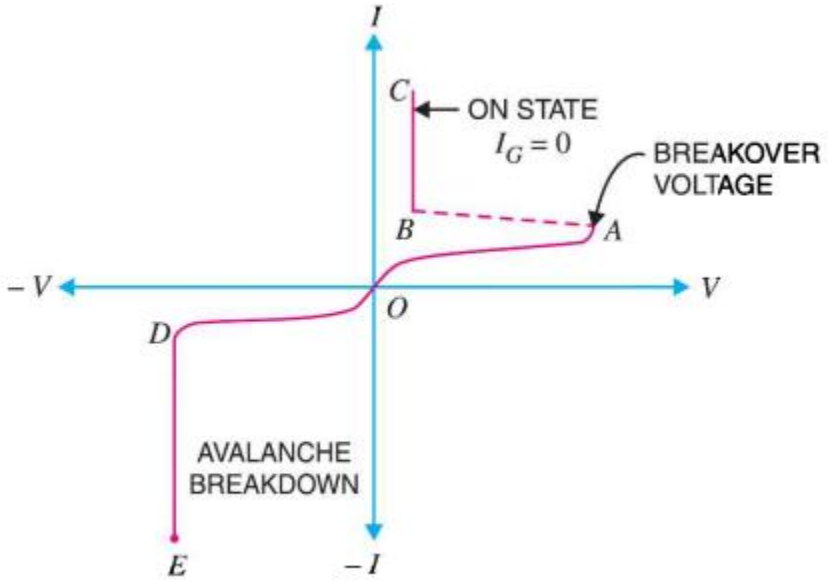


Fig. 20.7

21.3 Triac Construction

***A triac** is a three-terminal, five-layer semiconductor device whose forward and reverse characteristics are indentical to the forward characteristics of the SCR.* The three terminals are designated as main terminal *MT*1, main terminal *MT*2 and gate *G*.

Fig. 21.2 (*i*) shows the basic structure of a triac. As we shall see, a triac is equivalent to two separate *SCR*s connected in inverse parallel (*i.e.* anode of each connected to the cathode of the other) with gates commoned as shown in Fig. 21.2 (*ii*). Therefore, a triac acts like a bidirectional switch *i.e.* it can conduct current in either direction. This is unlike an *SCR* which can conduct current only in one direction. Fig. 21.2 (*iii*) shows the schematic symbol of a triac. The symbol consists of two parallel diodes connected in opposite directions with a single gate lead. It can be seen that even the symbol of triac indicates that it can conduct current for either polarity of the main terminals (*MT*1 and *MT*2) *i.e.* it can act as a bidirectional switch. The gate provides control over conduction in either direction.

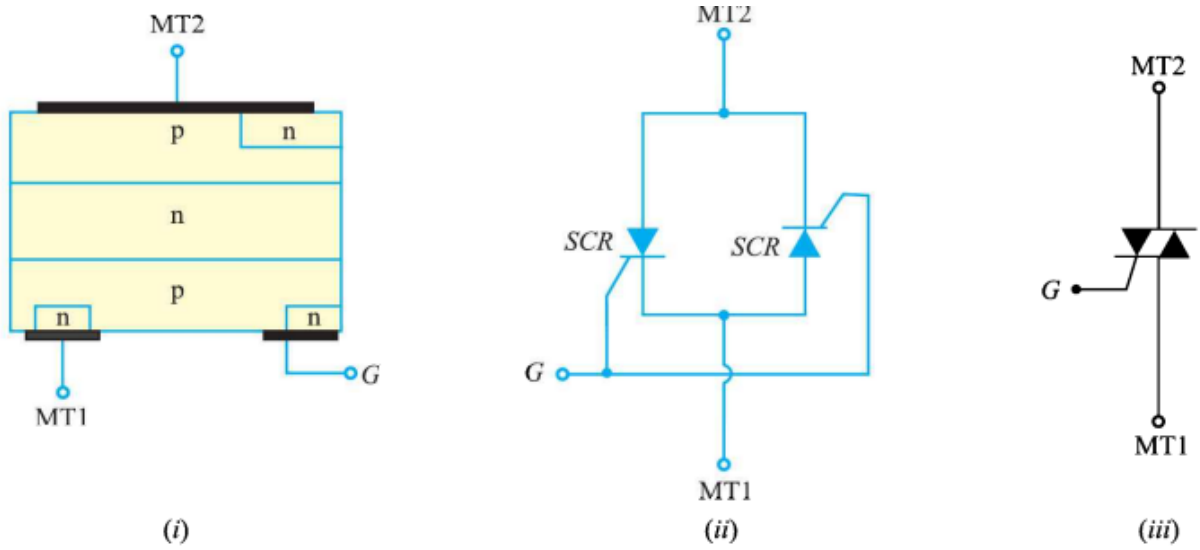


Fig. 21.2

The following points many be noted about the triac :

(*i*) The triac can conduct current (of course with proper gate current) regardless of the polarities of the main terminals *MT*1 and *MT*2. Since there is no longer a specific anode or cathode, the main leads are referred to as *MT*1 and *MT*2.

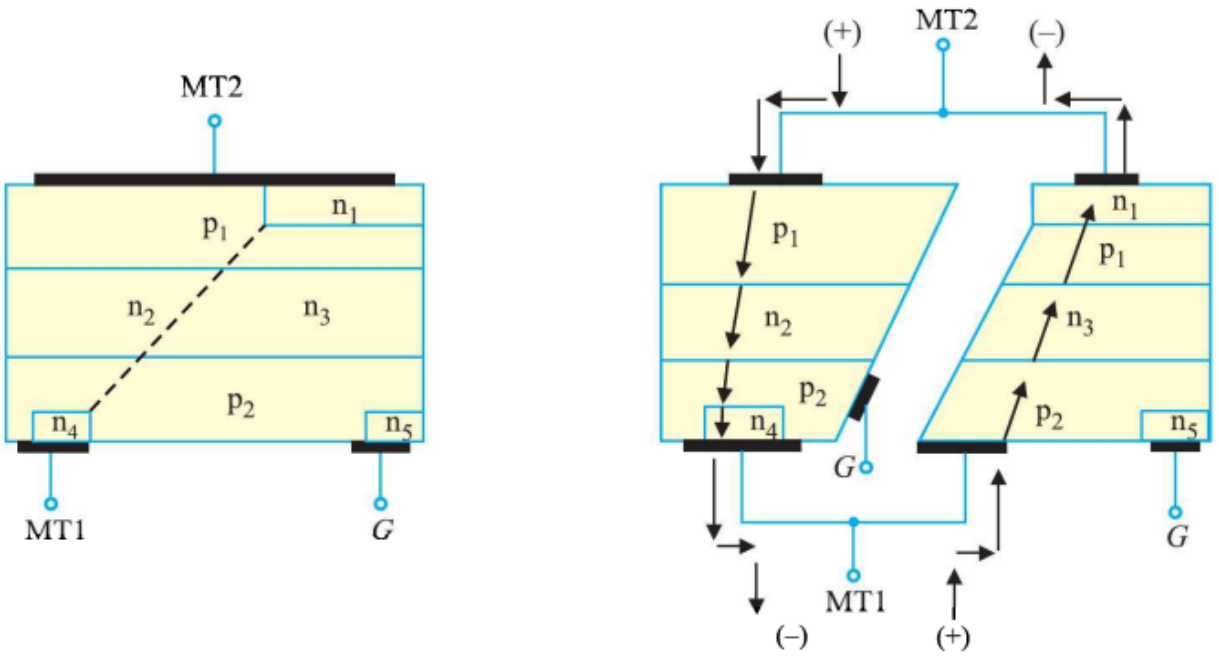
(*ii*) A triac can be turned on either with a positive or negative voltage at the gate of the device.

(*iii*) Like the *SCR*, once the triac is fired into conduction, the gate loses all control. The triac can be turned off by reducing the circuit current to the value of holding current.

(*iv*) The main disadvantage of triacs over *SCR*s is that triacs have considerably lower current-handling capabilities. Most triacs are available in ratings of less than 40A at voltages up to 600V.

21.4 SCR Equivalent Circuit of Triac

We shall now see that a triac is equivalent to two separate *SCRs* connected in inverse parallel (*i.e.* anode of each connected to the cathode of the other) with gates commoned. Fig. 21.3 (*i*) shows the basic structure of a triac. If we split the basic structure of a triac into two halves as shown in Fig. 21.3 (*ii*), it is easy to see that we have two *SCR*s connected in inverse parallel. The left half in Fig. 21.3 (*ii*) consists of a *pnpn* device ($p_1n_2\ p_2n_4$) having three *pn* junctions and constitutes *SCR*1. Similarly, the right half in Fig. 21.3 (*ii*) consists of *pnpn* device ($p_2n_3p_1n_1$) having three *pn* junctions and constitutes *SCR*2. The *SCR* equivalent circuit of the triac is shown in Fig. 21.4.



(*i*) (*ii*)

Fig. 21.3

Suppose the main terminal *MT*2 is positive and main terminal *MT*1 is negative. If the triac is now fired into conduction by proper gate current, the triac will conduct current following the path (left half) shown in Fig. 21.3 (*ii*). In relation to Fig. 21.4, the *SCR*1 is *ON* and the *SCR*2 is *OFF*. Now suppose that *MT*2 is negative and *MT*1 is positive. With proper gate current, the triac will be fired into conduction. The current through the devices follows the path (right half) as shown in Fig. 21.3 (*ii*). In relation to Fig. 21.4, the *SCR*2 is *ON* and the *SCR*1 is *OFF*. Note that the triac will conduct current in the appropriate direction as long as the current through the device is greater than its holding current.

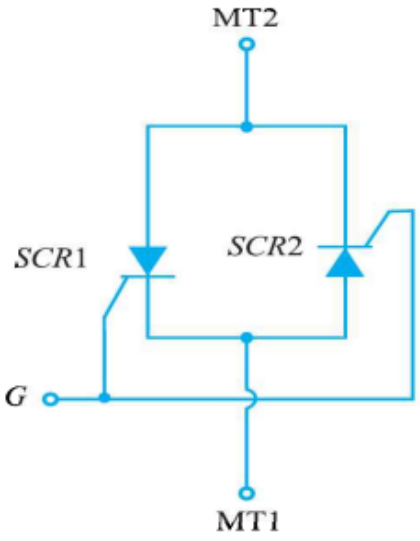


Fig. 21.4

21.9 The Diac

A **diac** *is a two-terminal, three layer bidirectional device which can be switched from its OFF state to ON state for either polarity of applied voltage.*

Fig. 21.17

The diac can be constructed in either *npn* or *pnp* form. Fig. 21.17 (*i*) shows the basic structure of a diac in *pnp* form. The two leads are connected to *p*-regions of silicon separated by an *n*-region. The structure of diac is very much similar to that of a transistor. However, there are several imporant differences:

(*i*) There is no terminal attached to the base layer.

(*ii*) The three regions are nearly identical in size.

(*iii*) The doping concentrations are identical (unlike a bipolar transistor) to give the device symmetrical properties.

Fig. 21.17 (*ii*) shows the symbol of a diac.

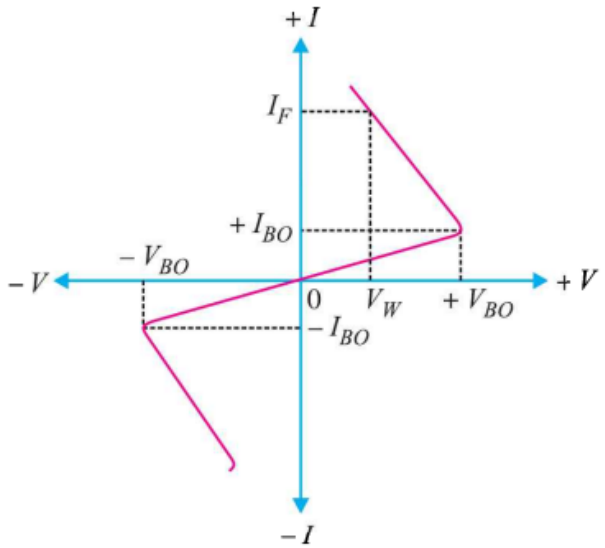
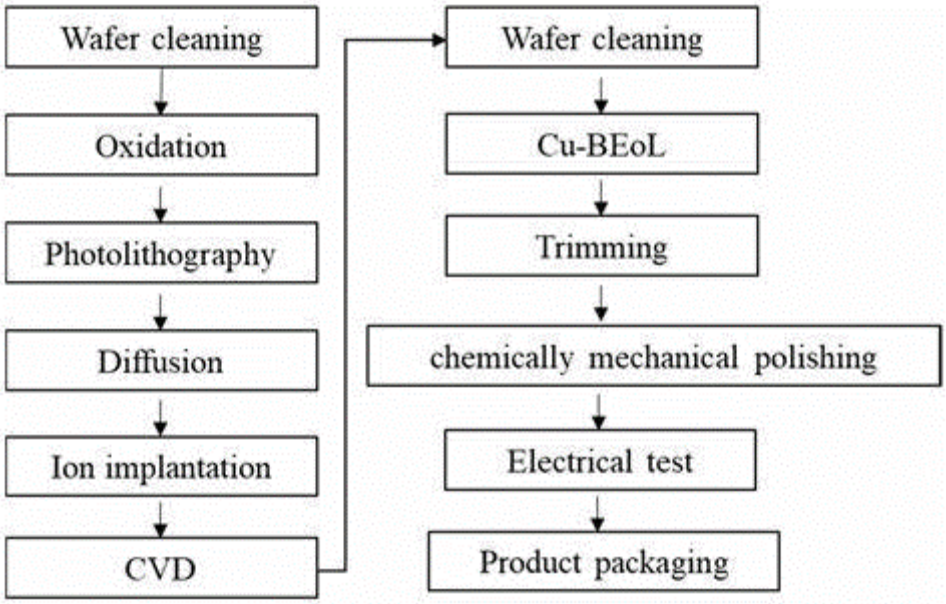


Fig. 21.18

Diacs are used primarily for triggering of triacs in adjustable phase control of a.c. mains power. Some of the circuit applications of diac are (*i*) light dimming (*ii*) heat control and (*iii*) universal motor speed control.


Wafer cleaning
Oxidation
Photolithography
Diffusion
Ion implantation
CVD
Wafer cleaning
Cu-BEoL
Trimming
chemically mechanical polishing
Electrical test
Product packaging