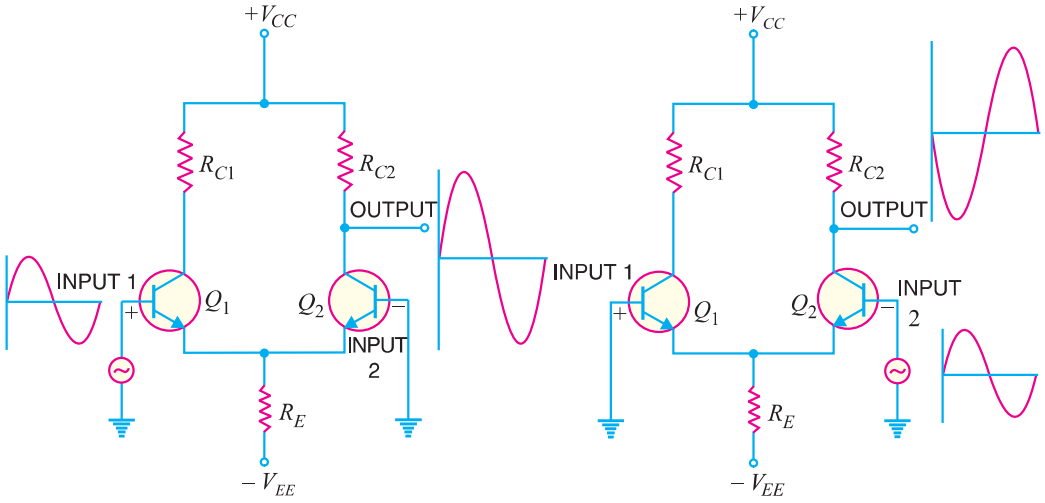
(*b*) When only one output terminal is available, the phase of the output of single-ended input *DA* depends on which input receives the input signal. This is illustrated in Fig. 25.7.



(*i*) Noninverting input (*ii*) Inverting input

Fig. 25.7

When signal applied to the input of *DA* produces no phase shift in the output, it is called *non-inverting input* [See Fig. 25.7 (*i*)]. In other words, for noninverting input, the output signal is in phase with the input signal. When the signal applied to the input of *DA* produces 180° phase shift, it is called *inverting input* [See Fig. 25.7 (*ii*)]. In other words, for inverting input, the output signal is 180° out of phase with the input signal. Since inverting input provides 180° phase shift, it is often identified with –sign. The noninverting input is then represented by +*sign. It may be noted that terms noninverting input and inverting input are meaningful when only one output terminal of *DA* is available.

25.5 Common-mode and Differential-mode Signals

The importance of a differential amplifier lies in the fact that the outputs are proportional to the *difference* between the two input signals. Thus the circuit can be used to amplify the difference between the two input signals or amplify only one input signal simply by grounding the other input. The input signals to a *DA* are defined as :

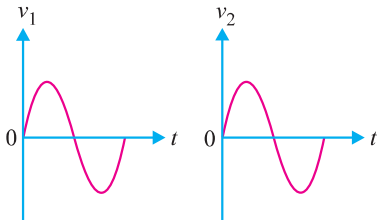
(*i*) Common-mode signals **(*ii*)** Differential-mode signals

(*i*) Common-mode signals : When the input signals to a *DA* are in phase and exactly equal in amplitude, they are called *common-mode signals* as shown in Fig. 25.8. The common-mode signals are rejected (not amplified) by the differential amplifier. It is because a differential amplifier amplifies the difference between the two signals ($v_1 - v_2$) and for common-mode signals, this difference is zero. Note that for common-mode operations, $v_1 = v_2$.

(*ii*) Differential-mode signals. When the input signals to a *DA* are 180° out of phase and exactly equal in amplitude, they are called *differential-mode signals* as shown in Fig. 25.9.

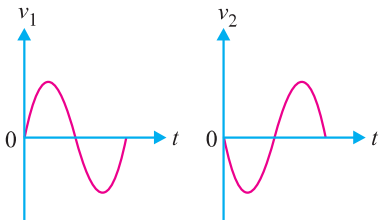
The differential-mode signals are amplified by the differential amplifier. It is because the difference in the signals is twice the value of each signal. For differential-mode signals, $v_1 = -v_2$.

* Note that in Fig. 25.7, the noninverting input terminal is given the +ve sign while the inverting input terminal is given the –ve sign.



Common-mode signals

Fig. 25.8



Differential-mode signals

Fig. 25.9

Thus we arrive at a very important conclusion that a differential amplifier will amplify the differential-mode signals while it will reject the common-mode signals.

25.6 Double-ended Input Operation of DA

A differential amplifier (*DA*) has two inputs so that it can simultaneously receive two signals. The input signals to a *DA* are defined as :

(*i*) Differential-mode signals **(*ii*)** Common-mode signals

The differential-mode signals are equal in amplitude but 180° out of phase. The common-mode signals are equal in magnitude and have the same phase.

(*i*) Differential input. In this mode (arrangement), two opposite-polarity (180° out of phase) signals are applied to the inputs of *DA* as shown in Fig. 25.10 (*i*).

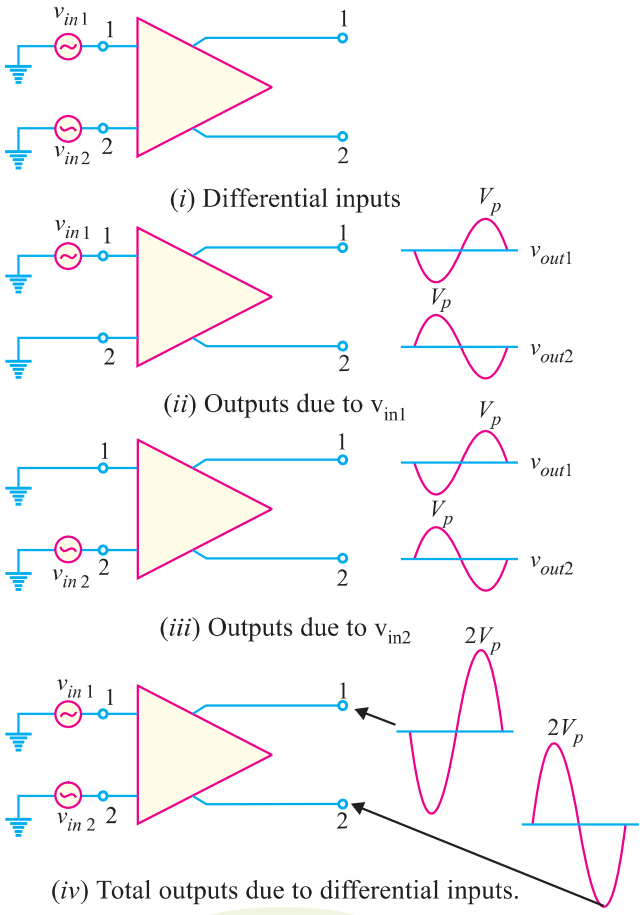
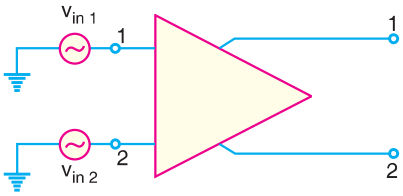


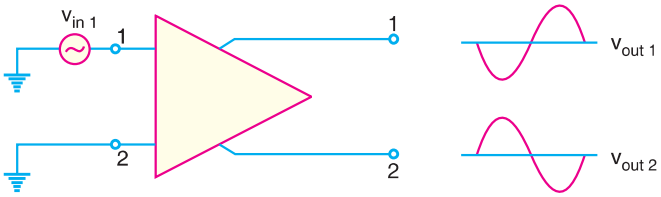
Fig. 25.10

As we shall see, each input affects the *outputs. Fig. 25.10 (*ii*) shows the output signals due to the signal on input 1 acting alone as a single-ended input. Fig. 25.10 (*iii*) shows the output signals due to the signal on **input 2 acting alone as a single-ended input. Note that in Figs. 25.10 (*ii*) and (*iii*), the signals on output 1 are of the same polarity. The same is also true for output 2. By superimposing both output 1 signals and both output 2 signals, we get the total outputs due to differential inputs [See Fig. 25.10(*iv*)].

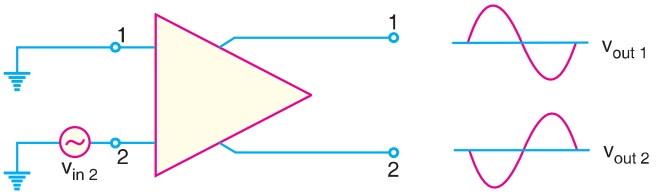
(*ii*) Common-mode input. In this mode, two signals equal in amplitude and having the same phase are applied to the inputs of *DA* as shown in Fig. 25.11(*i*).



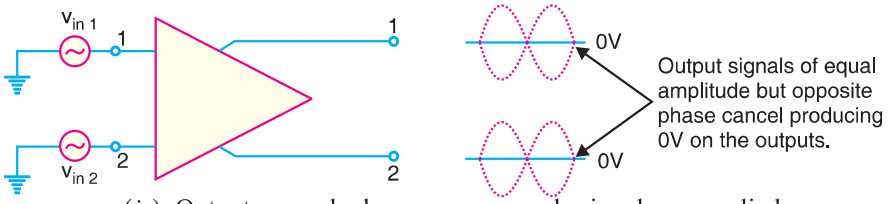
(*i*) Common-mode inputs



(*ii*) Outputs due to v_{in1}



(*iii*) Outputs due to v_{in2}



(*iv*) Outputs cancel when common-mode signals are applied.

Fig. 25.11

* Note that in all the Figures in Fig. 25.10, the phase of the input signal is given in the circle and the phase shift in the output signal is given at the output terminals. Thus in Fig. 25.10 (*ii*), the output signal at terminal 1 is 180° out of phase with the input signal. On the other hand, the output signal at terminal 2 is in phase with the input signal.

** Note that a *DA* amplifies $(v_1 - v_2)$. For Fig. 25.10 (*ii*), $v_{in1} - v_{in2} = v_{in1} - 0 = v_{in1}$. For Fig. 25.10 (*iii*), $v_{in1} - v_{in2} = 0 - v_{in2} = -v_{in2}$.

Again, by considering each input signal acting alone, the basic operation of *DA* in this mode can be explained. Fig. 25.11 (*ii*) shows the output signals due to the signal on only input 1 while Fig. 25.11 (*iii*) shows the output signals due to the signal on only input 2. Note that the corresponding signals on output 1 are of the opposite polarity and so are the ones on output 2. When these are superimposed, they cancel, resulting in zero output voltage as shown in Fig. 25.11 (*iv*).

It is important to note that common-mode signals are rejected by *DA*. This action is called *common-mode rejection.* Most of noises and other unwanted signals are common-mode signals. When these unwanted signals appear on the inputs of a *DA*, they are virtually eliminated on the output.

25.7 Voltage Gains of DA

The voltage gain of a *DA* operating in differential mode is called *differential-mode voltage gain* and is denoted by A_{DM}. The voltage gain of *DA* operating in common-mode is called *common-mode voltage gain* and is denoted by A_{CM}.

Ideally, a *DA* provides a very high voltage gain for differential-mode signals and zero gain for common-mode signals. However, practically, differential amplifiers do exhibit a very small common-mode gain (usually much less than 1) while providing a high differential voltage gain (usually several thousands). The higher the differential gain w.r.t. the common-mode gain, the better the performance of the *DA* in terms of rejection of common-mode signals.

25.8 Common-mode Rejection Ratio (CMRR)

A differential amplifier should have high differential voltage gain (A_{DM}) and very low common-mode voltage gain (A_{CM}). The ratio A_{DM}/A_{CM} is called common-mode rejection ratio (*CMRR*) *i.e.*,

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

Very often, the *CMRR* is expressed in decibels (*dB*). The decibel measure for *CMRR* is given by;

$$CMRR_{dB} = 20\log_{10}\frac{A_{DM}}{A_{CM}} = 20\log_{10} CMRR$$

The following table shows the relation between the two measurements :

$CMRR$	$CMRR_{dB}$
10	20dB
10^3	60dB
10^5	100dB
10^7	140dB

Importance of CMRR. The *CMRR* is the ability of a *DA* to reject the common-mode signals. The larger the *CMRR*, the better the *DA* is at eliminating common-mode signals. Let us illustrate this point. Suppose the differential amplifier in Fig. 25.12 has a differential voltage gain of 1500 (*i.e.*, A_{DM} = 1500) and a common-mode gain of 0.01 (*i.e.*, A_{CM} = 0.01).

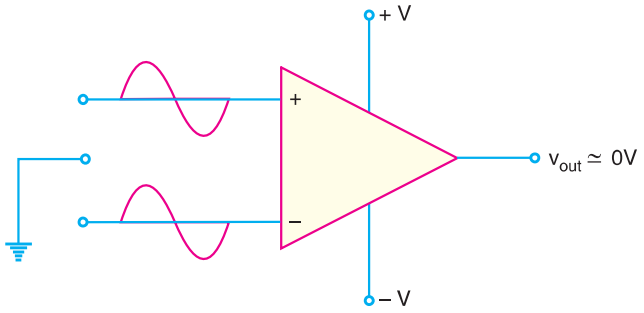


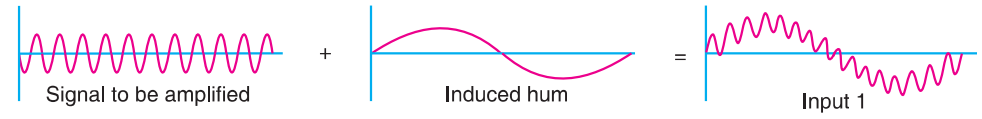
Fig. 25.12

$$\therefore \qquad CMRR = \frac{1500}{0.01} = 150,000$$

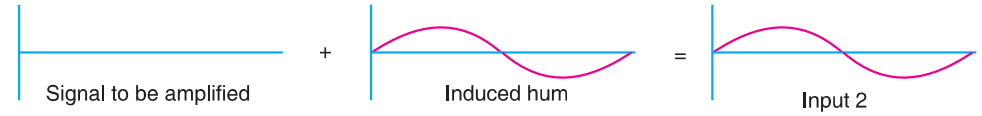
This means that the output produced by a difference between the inputs would be 150,000 times as great as an output produced by a common-mode signal.

The ability of the *DA* to reject common-mode signals is one of its main advantages. Common-mode signals are usually *undesired signals* caused by external interference. For example, any *RF* signals picked up by the *DA* inputs would be considered undesirable. The *CMRR* indicates the *DA*'s ability to reject such unwanted signals.

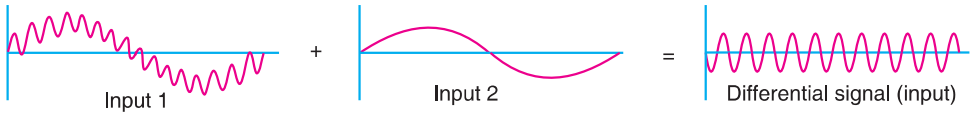
Practical Illustrations. Fig. 25.13 shows how a differential amplifier (*DA*) rejects hum and static voltages induced into its input leads.



(*i*) Signal input to input 1



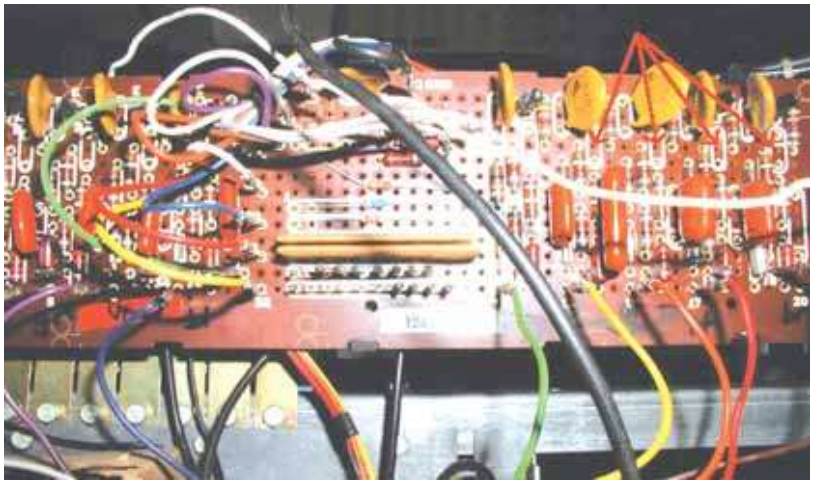
(*ii*) Signal input to input 2



(*iii*) Differential input signal

Fig. 25.13

(*i*) In Fig. 25.13(*i*), the signal is applied to input 1 of the *DA*. However, a low frequency *hum* voltage is also induced into the lead wire. This hum is produced due to building and collapsing magnetic field generated by adjacent conductor carrying 50Hz current. The resultant waveform is shown in Fig. 25.13 (*i*). If this waveform is amplified by a conventional amplifier, the 50 Hz hum in the output will be stronger than the desired signal.



Low voltage differential amplifier for test and measurement applications.

(ii) However, a *DA* also has second input (input 2). Therefore, the lead of second input has the same phase 50 Hz hum induced into it. This is the only voltage (*i.e.*, hum) applied to input 2 as shown in Fig. 25.13(*ii*).

(iii) As shown in Fig. 25.13 (*iii*), the hum components of the two inputs form a common-mode signal which is largely rejected by the *DA*. If the input hum signals are equal at the input, then differential input to *DA* will be devoid of hum. Therefore, the amplified output of *DA* will be free from the hum.

Note : We have considered the ideal case *i.e.* $A_{CM} = 0$. Even in a practical case, the value of A_{CM} is less than 1 while A_{DM} is over 200. This means that the desired signal would be over 200 times larger than the hum at the output terminal.

Example 25.2. *A certain differential amplifier has a differential voltage gain of 2000 and a common mode gain of 0.2. Determine CMRR and express it in dB.*

Solution.
$$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{2000}{0.2} = \mathbf{10{,}000}$$
$$CMRR_{dB} = 20 \log_{10} 10{,}000 = \mathbf{80dB}$$

Example 25.3. *A differential amplifier has an output of 1V with a differential input of 10 mV and an output of 5 mV with a common-mode input of 10 mV. Find the CMRR in dB.*

Solution. Differential gain, $A_{DM} = 1\text{V}/10\text{ mV} = 100$

Common-mode gain, $A_{CM} = 5\text{ mV}/10\text{ mV} = 0.5$

$\therefore$ $CMRR_{dB} = 20 \log_{10} (100/0.5) = \mathbf{46\ dB}$

Example 25.4. *A differential amplifier has a voltage gain of 150 and a CMRR of 90 dB. The input signals are 50 mV and 100 mV with 1 mV of noise on each input. Find (i) the output signal (ii) the noise on the output.*

Solution.

(i) Output signal, $v_{out} = A_{DM}(v_1 - v_2) = 150\ (100\text{ mV} - 50\text{ mV}) = \mathbf{7.5\ V}$

(ii) $CMRR_{dB} = 20 \log_{10} (150/A_{CM})$

or $90 = 20 \log_{10} (150/A_{CM})$

$\therefore$ $A_{CM} = 4.7 \times 10^{-3}$

Noise on output $= A_{CM} \times 1\text{ mV} = 4.7 \times 10^{-3} \times 1\text{mV} = \mathbf{4.7 \times 10^{-6}\ V}$

Example 25.5. *The differential amplifier shown in Fig. 25.14 has a differential voltage gain of 2500 and a CMRR of 30,000. A single-ended input signal of 500 μV r.m.s. is applied. At the same time, 1V, 50 Hz interference signal appears on both inputs as a result of radiated pick-up from the a.c. power system.*

(*i*) *Determine the common-mode gain.*

(*ii*) *Express the CMRR in dB.*

(*iii*) *Determine the r.m.s. output signal.*

(*iv*) *Determine the r.m.s. interference voltage on the output.*

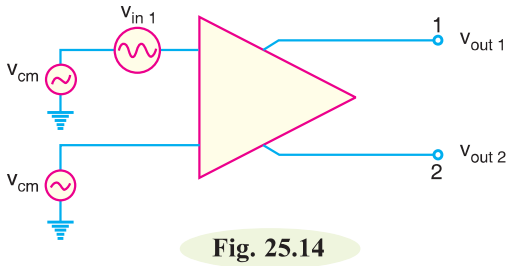


Fig. 25.14

Solution. (*i*) $CMRR = \dfrac{A_{DM}}{A_{CM}}$

$\therefore \quad A_{CM} = \dfrac{A_{DM}}{CMRR} = \dfrac{2500}{30,000} = \mathbf{0.083}$

(*ii*) $CMRR_{dB} = 20 \log_{10} (30{,}000) = \mathbf{89.5\ dB}$

(*iii*) In Fig. 25.14, the differential input voltage is the difference between the voltages on input 1 and that on input 2. Since input 2 is grounded, its voltage is zero.

$\therefore$ Differential input voltage = 500 μV – 0 = 500 μV

The output signal in this case is taken at output 1.

$\therefore \quad v_{out1} = A_{DM} \times (500\ \mu V) = (2500 \times 500)\ \mu V = \mathbf{1.25\ V}$

(*iv*) The common-mode input is 1V r.m.s. and the common-mode gain is $A_{CM} = 0.083$.

$\therefore$ Noise on the output = $A_{CM} \times (1V) = (0.083)\ (1V) = \mathbf{83\ mV}$

25.9 D.C. Analysis of Differential Amplifier (DA)

When no signal is applied to a *DA,* d.c. or quiescent conditions prevail in the circuit. From the transistor circuit theory, we can find *bias voltages and bias currents in the circuit. Fig. 25.15 shows the basic arrangement for an *npn* differential amplifier. Typical circuit values have been assumed to make the treatment illustrative. The circuit is symmetrical *i.e.*, the transistors Q_1 and Q_2 are identical; collector loads are equal ($R_{C1} = R_{C2}$) and base resistors R_B are equal. We assume that base current is very small so that we can ignore the voltage drops across base resistors *i.e.*,

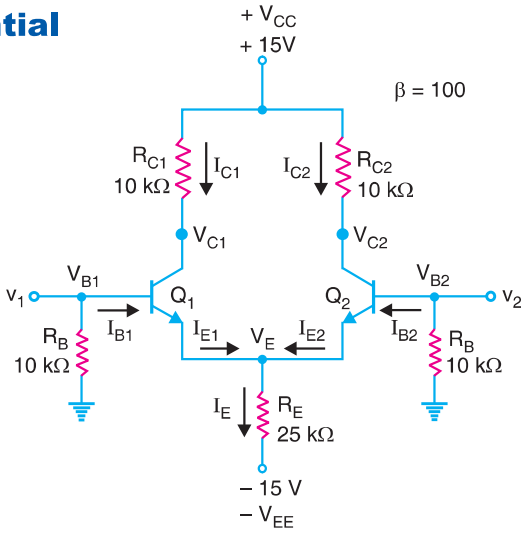


Fig. 25.15

$V_{B1} = V_{B2} \simeq$ **$0V$

Now $V_E = V_{B1} - 0.7 = V_{B2} - 0.7 =$ ***$0 - 0.7 = -0.7$ V

$\therefore \quad V_{E1} = V_{E2} = V_E = \mathbf{-0.7\ V}$

† Voltage across $R_E = V_{EE} - V_{BE}$

Current in R_E, $I_E = \dfrac{V_{EE} - V_{BE}}{R_E}$

---

* Bias voltages and currents mean d.c. values.

** As we shall see, for the considered circuit values, $I_{B1} = I_{B2} = 2.86$ μA.

$\therefore$ Base voltage, $V_B = I_B \times R_B = 2.86\ \mu A \times 10\ k\Omega = 28.6$ mV. Compared to the –15V of V_{EE}, this is a negligible amount of voltage.

*** $V_{BE} = 0.7$ V. There is a plus-to-minus drop in going from the base to emitter. Since base voltage is $0V$, $V_E = -0.7$ V.

† Applying Kirchhoff's voltage law to the loop consisting of V_{EE}, the base-emitter junction of Q_1 and R_B, we have,

$$V_{RE} = V_{EE} - V_{BE} - V_{RB} = V_{EE} - V_{BE} - 0 = V_{EE} - V_{BE}$$

(i) For $A_{CL} = 1$, $BW = \dfrac{1.5 \text{ MHz}}{1} = \mathbf{1.5 \text{ MHz}}$

(ii) For $A_{CL} = 10$, $BW = \dfrac{1.5 \text{ MHz}}{10} = \mathbf{150 \text{ kHz}}$

(iii) For $A_{CL} = 100$, $BW = \dfrac{1.5 \text{ MHz}}{100} = \mathbf{15 \text{ kHz}}$

From this example, we conclude that :

(a) The higher the gain (A_{CL}) of an *OP*-amp, the narrower its bandwidth.

(b) The lower the gain of an *OP*-amp, the wider its bandwidth.

25.20 Slew Rate

The slew rate of an *OP*-amp is a measure of *how fast the output voltage can change* and is measured in volts per microsecond (V/μs). If the slew rate of an *OP*-amp is 0.5V/μs, it means that the output from the amplifier can change by 0.5 V every μs. Since frequency is a function of time, the *slew rate can be used to determine the maximum operating frequency of the OP-amp* as follows:

$$\text{Maximum operating frequency, } f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}}$$

Here V_{pk} is the peak output voltage.

Example 25.23. *Determine the maximum operating frequency for the circuit shown in Fig. 25.44. The slew rate is 0.5 V/μs.*

Solution. The maximum peak output voltage(V_{pk}) is approximately *$8V$. Therefore, maximum operating frequency (f_{max}) is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\,V/\mu s}{2\pi \times 8}$$

$$= \frac{500 \text{ kHz}}{2\pi \times 8} \qquad (\because 0.5 \text{ V/μs} = 500 \text{ kHz})$$

$$= \mathbf{9.95 \text{ kHz}}$$

While 9.95 kHz may not seem to be a very high output frequency, you must realise that the amplifier was assumed to be operating at its maximum output voltage. Let us see what happens when peak output voltage is reduced (See example 25.24).

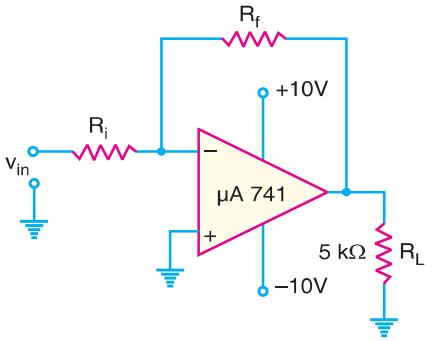


Fig. 25.44

Example 25.24. *The amplifier in Fig. 25.44 is being used to amplify an input signal to a peak output voltage of 100 mV. What is the maximum operating frequency of the amplifier?*

Solution. The maximum operating frequency (f_{max}) of the amplifier is given by;

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_{pk}} = \frac{0.5\,V/\mu s}{2\pi \times 0.1} \qquad (\because 100 \text{ mV} = 0.1\text{V})$$

$$= \frac{500 \text{ kHz}}{2\pi \times 0.1} = \mathbf{796 \text{ kHz}} \qquad (\because 0.5\text{V/μs} = 500 \text{ kHz})$$

The above examples show that an *OP*-amp can be operated at a much higher frequency when being used as a small-signal amplifier than when being used as a large-signal amplifier.

* $+V_{sat} = +V_{supply} - 2 = 10 - 2 = 8V$

where v_{o1} is due to the 6-V voltage source, and v_{o2} is due to the 4-V input. To get v_{o1}, we set the 4-V source equal to zero. Under this condition, the circuit becomes an inverter. Hence Eq. (5.9) gives

$$v_{o1} = -\frac{10}{4}(6) = -15 \text{ V}$$

To get v_{o2}, we set the 6-V source equal to zero. The circuit becomes a noninverting amplifier so that Eq. (5.11) applies.

$$v_{o2} = \left(1 + \frac{10}{4}\right)4 = 14 \text{ V}$$

Thus,

$$v_o = v_{o1} + v_{o2} = -15 + 14 = -1 \text{ V}$$

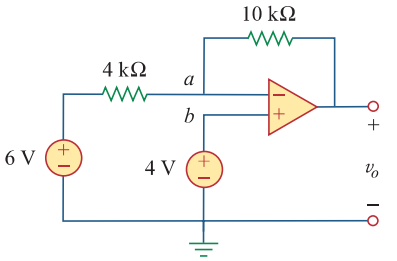


Figure 5.19
For Example 5.5.

METHOD 2 Applying KCL at node a,

$$\frac{6 - v_a}{4} = \frac{v_a - v_o}{10}$$

But $v_a = v_b = 4$, and so

$$\frac{6 - 4}{4} = \frac{4 - v_o}{10} \quad \Rightarrow \quad 5 = 4 - v_o$$

or $v_o = -1$ V, as before.

Practice Problem 5.5

Calculate v_o in the circuit of Fig. 5.20.

Answer: 7 V.

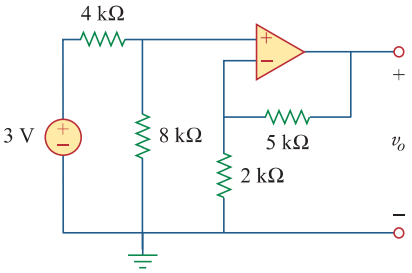


Figure 5.20
For Practice Prob. 5.5.

5.6 Summing Amplifier

Besides amplification, the op amp can perform addition and subtraction. The addition is performed by the summing amplifier covered in this section; the subtraction is performed by the difference amplifier covered in the next section.

A summing amplifier is an op amp circuit that combines several inputs and produces an output that is the weighted sum of the inputs.

The summing amplifier, shown in Fig. 5.21, is a variation of the inverting amplifier. It takes advantage of the fact that the inverting configuration can handle many inputs at the same time. We keep in mind

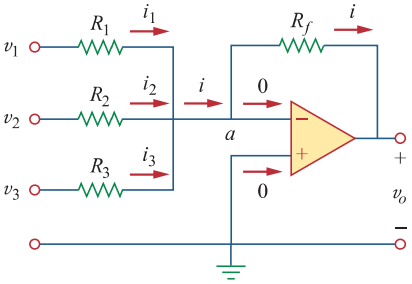


Figure 5.21
The summing amplifier.

that the current entering each op amp input is zero. Applying KCL at node a gives

$$i = i_1 + i_2 + i_3 \tag{5.13}$$

But

$$i_1 = \frac{v_1 - v_a}{R_1}, \quad i_2 = \frac{v_2 - v_a}{R_2}$$
$$i_3 = \frac{v_3 - v_a}{R_3}, \quad i = \frac{v_a - v_o}{R_f} \tag{5.14}$$

We note that $v_a = 0$ and substitute Eq. (5.14) into Eq. (5.13). We get

$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right) \tag{5.15}$$

indicating that the output voltage is a weighted sum of the inputs. For this reason, the circuit in Fig. 5.21 is called a *summer*. Needless to say, the summer can have more than three inputs.

Example 5.6

Calculate v_o and i_o in the op amp circuit in Fig. 5.22.

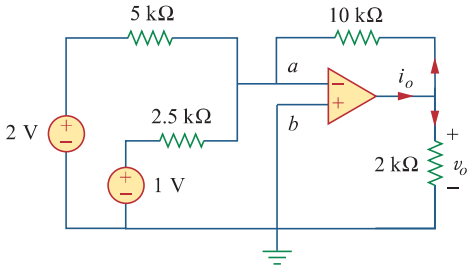


Figure 5.22
For Example 5.6.

Solution:
This is a summer with two inputs. Using Eq. (5.15) gives

$$v_o = -\left[\frac{10}{5}(2) + \frac{10}{2.5}(1)\right] = -(4 + 4) = -8 \text{ V}$$

The current i_o is the sum of the currents through the 10-kΩ and 2-kΩ resistors. Both of these resistors have voltage $v_o = -8$ V across them, since $v_a = v_b = 0$. Hence,

$$i_o = \frac{v_o - 0}{10} + \frac{v_o - 0}{2}\text{mA} = -0.8 - 4 = -4.8 \text{ mA}$$

Practice Problem 5.6

Find v_o and i_o in the op amp circuit shown in Fig. 5.23.

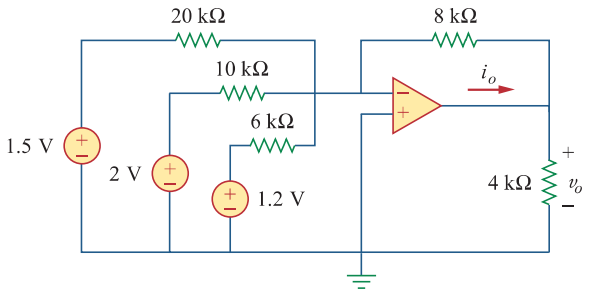


Figure 5.23
For Practice Prob. 5.6.

Answer: −3.8 V, −1.425 mA.

5.7 Difference Amplifier

Difference (or differential) amplifiers are used in various applications where there is need to amplify the difference between two input signals. They are first cousins of the *instrumentation amplifier*, the most useful and popular amplifier, which we will discuss in Section 5.10.

The difference amplifier is also known as the *subtractor*, for reasons to be shown later.

A difference amplifier is a device that amplifies the difference between two inputs but rejects any signals common to the two inputs.

Consider the op amp circuit shown in Fig. 5.24. Keep in mind that zero currents enter the op amp terminals. Applying KCL to node a,

$$\frac{v_1 - v_a}{R_1} = \frac{v_a - v_o}{R_2}$$

or

$$v_o = \left(\frac{R_2}{R_1} + 1\right)v_a - \frac{R_2}{R_1}v_1 \tag{5.16}$$

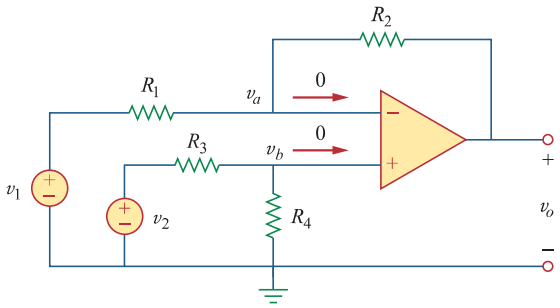


Figure 5.24
Difference amplifier.

Applying KCL to node b,

$$\frac{v_2 - v_b}{R_3} = \frac{v_b - 0}{R_4}$$

or

$$v_b = \frac{R_4}{R_3 + R_4} v_2 \tag{5.17}$$

But $v_a = v_b$. Substituting Eq. (5.17) into Eq. (5.16) yields

$$v_o = \left(\frac{R_2}{R_1} + 1\right)\frac{R_4}{R_3 + R_4} v_2 - \frac{R_2}{R_1} v_1$$

or

$$\boxed{v_o = \frac{R_2(1 + R_1/R_2)}{R_1(1 + R_3/R_4)} v_2 - \frac{R_2}{R_1} v_1} \tag{5.18}$$

Since a difference amplifier must reject a signal common to the two inputs, the amplifier must have the property that $v_o = 0$ when $v_1 = v_2$. This property exists when

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \tag{5.19}$$

Thus, when the op amp circuit is a difference amplifier, Eq. (5.18) becomes

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) \tag{5.20}$$

If $R_2 = R_1$ and $R_3 = R_4$, the difference amplifier becomes a *subtractor*, with the output

$$v_o = v_2 - v_1 \tag{5.21}$$

Example 5.7

Design an op amp circuit with inputs v_1 and v_2 such that $v_o = -5v_1 + 3v_2$.

Solution:
The circuit requires that

$$v_o = 3v_2 - 5v_1 \tag{5.7.1}$$

This circuit can be realized in two ways.

Design 1 If we desire to use only one op amp, we can use the op amp circuit of Fig. 5.24. Comparing Eq. (5.7.1) with Eq. (5.18), we see

$$\frac{R_2}{R_1} = 5 \quad \Rightarrow \quad R_2 = 5R_1 \tag{5.7.2}$$

Also,

$$5\frac{(1 + R_1/R_2)}{(1 + R_3/R_4)} = 3 \quad \Rightarrow \quad \frac{\frac{6}{5}}{1 + R_3/R_4} = \frac{3}{5}$$

or

$$2 = 1 + \frac{R_3}{R_4} \quad \Rightarrow \quad R_3 = R_4 \tag{5.7.3}$$

If we choose $R_1 = 10\ \text{k}\Omega$ and $R_3 = 20\ \text{k}\Omega$, then $R_2 = 50\ \text{k}\Omega$ and $R_4 = 20\ \text{k}\Omega$.

Design 2 If we desire to use more than one op amp, we may cascade an inverting amplifier and a two-input inverting summer, as shown in Fig. 5.25. For the summer,

$$v_o = -v_a - 5v_1 \tag{5.7.4}$$

and for the inverter,

$$v_a = -3v_2 \tag{5.7.5}$$

Combining Eqs. (5.7.4) and (5.7.5) gives

$$v_o = 3v_2 - 5v_1$$

which is the desired result. In Fig. 5.25, we may select $R_1 = 10\ \text{k}\Omega$ and $R_3 = 20\ \text{k}\Omega$ or $R_1 = R_3 = 10\ \text{k}\Omega$.

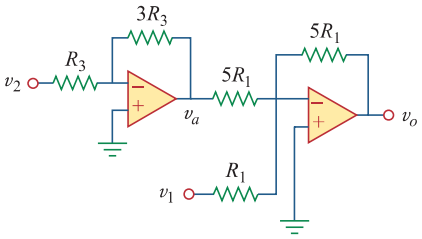


Figure 5.25
For Example 5.7.

Practice Problem 5.7

Design a difference amplifier with gain 5.

Answer: Typical: $R_1 = R_3 = 10\text{k}\Omega$, $R_2 = R_4 = 50\ \text{k}\Omega$.

Example 5.8

An *instrumentation amplifier* shown in Fig. 5.26 is an amplifier of low-level signals used in process control or measurement applications and commercially available in single-package units. Show that

$$v_o = \frac{R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right)(v_2 - v_1)$$

Solution:
We recognize that the amplifier A_3 in Fig. 5.26 is a difference amplifier. Thus, from Eq. (5.20),

$$v_o = \frac{R_2}{R_1}(v_{o2} - v_{o1}) \tag{5.8.1}$$

Since the op amps A_1 and A_2 draw no current, current i flows through the three resistors as though they were in series. Hence,

$$v_{o1} - v_{o2} = i(R_3 + R_4 + R_3) = i(2R_3 + R_4) \tag{5.8.2}$$

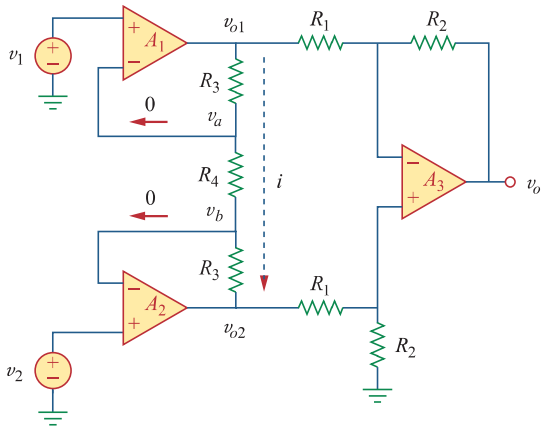


Figure 5.26
Instrumentation amplifier; for Example 5.8.

But

$$i = \frac{v_a - v_b}{R_4}$$

and $v_a = v_1$, $v_b = v_2$. Therefore,

$$i = \frac{v_1 - v_2}{R_4} \tag{5.8.3}$$

Inserting Eqs. (5.8.2) and (5.8.3) into Eq. (5.8.1) gives

$$v_o = \frac{R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right)(v_2 - v_1)$$

as required. We will discuss the instrumentation amplifier in detail in Section 5.10.

Practice Problem 5.8

Obtain i_o in the instrumentation amplifier circuit of Fig. 5.27.

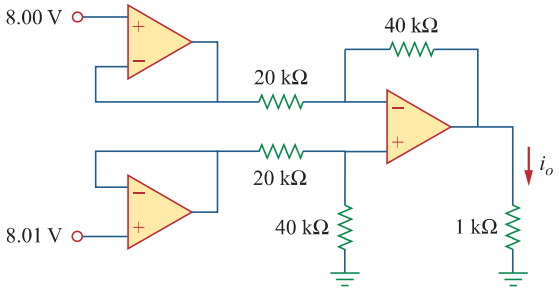


Figure 5.27
Instrumentation amplifier; for Practice Prob. 5.8.

Answer: 20 μA.

5.8 Cascaded Op Amp Circuits

As we know, op amp circuits are modules or building blocks for designing complex circuits. It is often necessary in practical applications to connect op amp circuits in cascade (i.e., head to tail) to achieve a large overall gain. In general, two circuits are cascaded when they are connected in tandem, one behind another in a single file.

A cascade connection is a head-to-tail arrangement of two or more op amp circuits such that the output of one is the input of the next.

When op amp circuits are cascaded, each circuit in the string is called a *stage*; the original input signal is increased by the gain of the individual stage. Op amp circuits have the advantage that they can be cascaded without changing their input-output relationships. This is due to the fact that each (ideal) op amp circuit has infinite input resistance and zero output resistance. Figure 5.28 displays a block diagram representation of three op amp circuits in cascade. Since the output of one stage is the input to the next stage, the overall gain of the cascade connection is the product of the gains of the individual op amp circuits, or

$$A = A_1 A_2 A_3 \tag{5.22}$$

Although the cascade connection does not affect the op amp input-output relationships, care must be exercised in the design of an actual op amp circuit to ensure that the load due to the next stage in the cascade does not saturate the op amp.

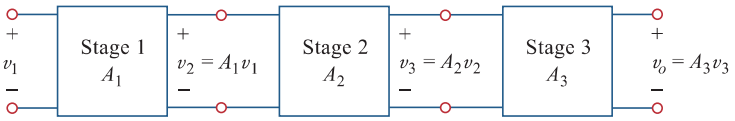


Figure 5.28
A three-stage cascaded connection.

Example 5.9

Find v_o and i_o in the circuit in Fig. 5.29.

Solution:
This circuit consists of two noninverting amplifiers cascaded. At the output of the first op amp,

$$v_a = \left(1 + \frac{12}{3}\right)(20) = 100 \text{ mV}$$

At the output of the second op amp,

$$v_o = \left(1 + \frac{10}{4}\right)v_a = (1 + 2.5)100 = 350 \text{ mV}$$

The required current i_o is the current through the 10-kΩ resistor.

$$i_o = \frac{v_o - v_b}{10} \text{ mA}$$

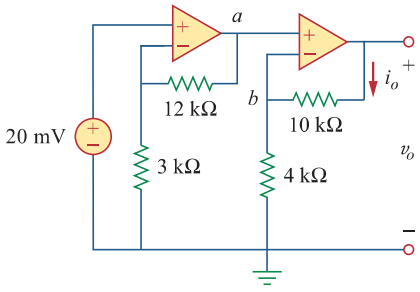


Figure 5.29
For Example 5.9.

But $v_b = v_a = 100$ mV. Hence,

$$i_o = \frac{(350 - 100) \times 10^{-3}}{10 \times 10^3} = 25\ \mu\text{A}$$

Practice Problem 5.9

Determine v_o and i_o in the op amp circuit in Fig. 5.30.

Answer: 24 V, 2 mA.

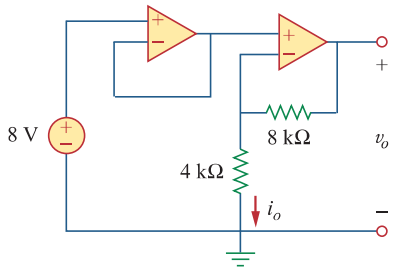


Figure 5.30
For Practice Prob. 5.9.

Example 5.10

If $v_1 = 1$ V and $v_2 = 2$ V, find v_o in the op amp circuit of Fig. 5.31.

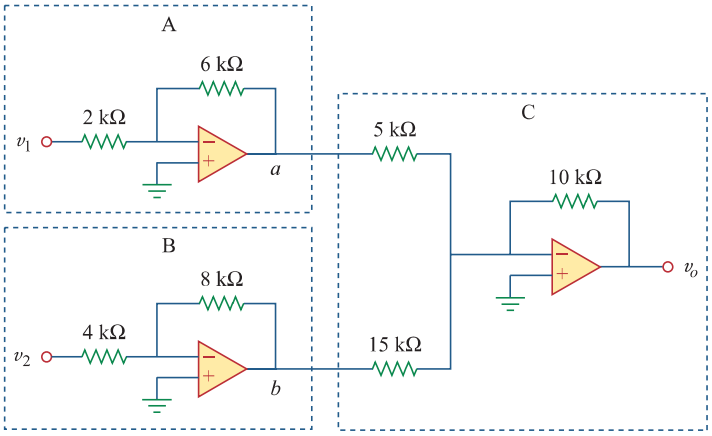


Figure 5.31
For Example 5.10.

Solution:

1. **Define.** The problem is clearly defined.
2. **Present.** With an input of v_1 of 1 V and of v_2 of 2 V, determine the output voltage of the circuit shown in Figure 5.31. The op amp circuit is actually composed of three circuits. The first circuit acts as an amplifier of gain $-3(-6\ \text{k}\Omega/2\ \text{k}\Omega)$ for v_1 and the second functions as an amplifier of gain $-2(-8\ \text{k}\Omega/4\ \text{k}\Omega)$ for v_2. The last circuit serves as a summer of two different gains for the output of the other two circuits.
3. **Alternative.** There are different ways of working with this circuit. Since it involves ideal op amps, then a purely mathematical