North South University

Department of Electrical & Computer Engineering

CSE332

Computer Organization and Architecture

Instruction Set Architecture

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Submitted to

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Number of operands:

There are three operands in this design which will be referred to as rs, rt and rd.

Types of operands:

The operands in this design are mixed.

Number of operations:

There are 11 operations.

- nop (Do nothing)
- beq (Branch if equal)
- sub (Subtraction)
- sll (Shift left)
- and (Applies AND logic)
- sw (Store word)
- slt (Compare less than)
- jmp (Jump)
- add (Addition)
- addi (Addition with immediate)
- lw (Load word)

Types of operations:

There are **six** types of operations (also showing how many of each type):

- 1x Idle state operation
  - nop
- 3x Arithmetic operations
  - sub
  - add
  - addi
- 2x Logical operations
  - sll
  - and
  - slt
- 2x Data Transfer operations
  - sw
  - lw
- 2x Conditional Branch operation
  - beq
- 1x Unconditional Jump operation
  - jmp

Listing the **opcodes** and **binary values:**

Opcode	Binary
nop	0000
beq	0001
sub	0010
sll	0011
and	0100
sw	0101
slt	0110
jmp	0111
add	1000
addi	1001
lw	1010

Number of Instruction Formats:

There are three types of instruction formats:

- R-type Instruction
- I-type Instruction
- J-type Instruction

Description of instruction Formats:

R-type: These instructions use the format: **op rs rt rd**. Where **op** is a 4 bit field that has the operation code; **rs** and **rt** are 4 bit fields which hold address of two source registers; **rd** is a 4 bit field which holds the address of the destination register where the result of an operation is written.

op	rs	rt	rd
(4 bit)	(4 bit)	(4 bit)	(4 bit)

I-type: These instructions use the format: **op rs rd im**. Where **op** is a 4 bit field that has the operation code; **rs** is the 4 bit field which holds address of the source register; **rd** is a 4 bit field which holds the address of the destination register where the result of an operation is written; **im** which stands for immediate, holds the value of the immediate in 4 bits.

op	rs	rd	im
(4 bit)	(4 bit)	(4 bit)	(4 bit)

J-type: These instructions use the format: **op rd**. Where **op** is a 4 bit field that has the operation code; **rd** is a 16 bit field which holds the address of the destination register where the program counter will jump to.

op	Target
(4 bit)	(12 bit)

Overview

Category	Operation	Name	Type	Opcode	Syntax	Comment
Unconditional	Do nothing	nop	X	0000	X	X
Conditional	Check equality	beq	I	0001	beq $s2 $s3 7	If($s3==$s2) then 7
Arithmetic	Subtraction	sub	R	0010	sub $s1 $s2 $s3	$s3 = $s1 - $s2
Logical	Shift left	sll	I	0011	sll $s1 $s2 3	$s2=$s1<<3
Logical	Bit by bit AND	and	R	0100	and $s1 $s2 $s3	$s3 = $s1 AND $s2
Data Transfer	Store word	Sw	I	0101	sw $s1 $s2 2	Mem[$s1+2]=$s2
Conditional	Compare less than	Slt	R	0110	slt $s1 $s2 $s3	If($s1<$s2)then $s3=1 else $s3=0
Unconditional	Jump	Jmp	J	0111	jmp 13	Go to line 13
Arithmetic	Add two numbers	Add	R	1000	add $s1 $s2 $s3	$s3 = $s1 + $s2
Arithmetic	Add numbers with immediate	addi	I	1001	addi $s1 $s2 3	$s2 = $s1 + 3
Data Transfer	Load word	Lw	I	1010	Lw $s1 $s2 $s3	$s2=Mem[$s1+2]