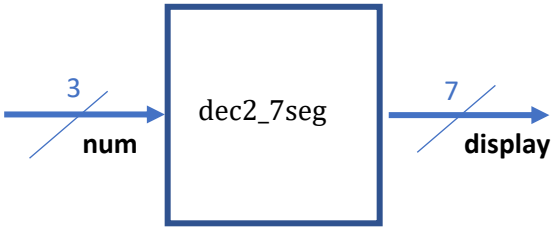
Project 1 Diagrams

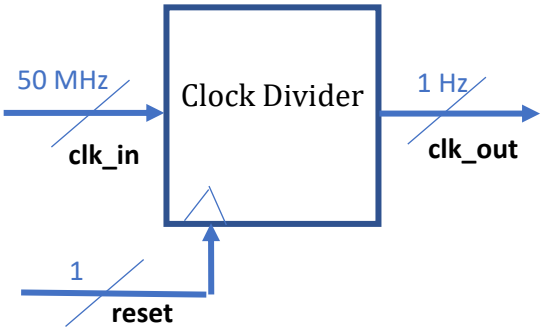
dec2_7seg (7-segment display)

This module takes in a 3 bit input value. It's output is 6 bit value in which each bit corresponds to a region of the 7-bit display that will be turned on.



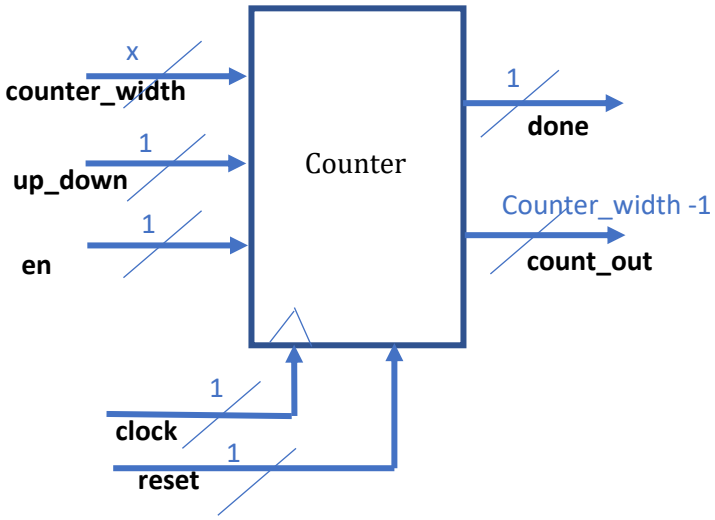
clock_divider

The clock divider has two inputs: the clock and reset values. It takes the clock as input and produces a reduced clock speed as output. The input and output are represented by the rate at which the clock sends the 1 signal.

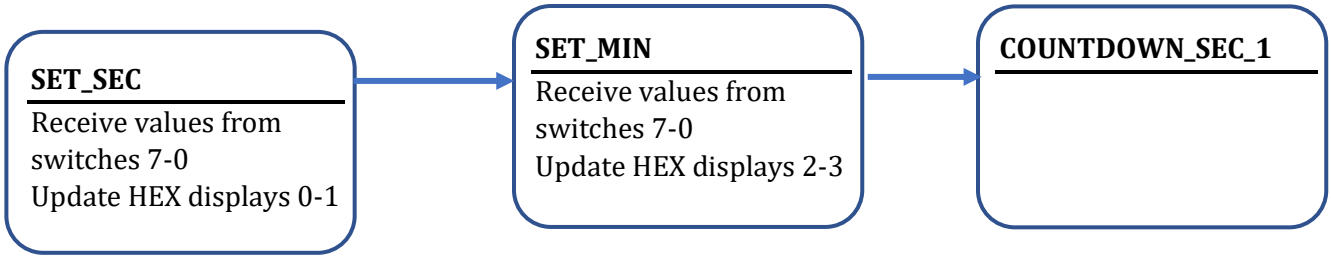


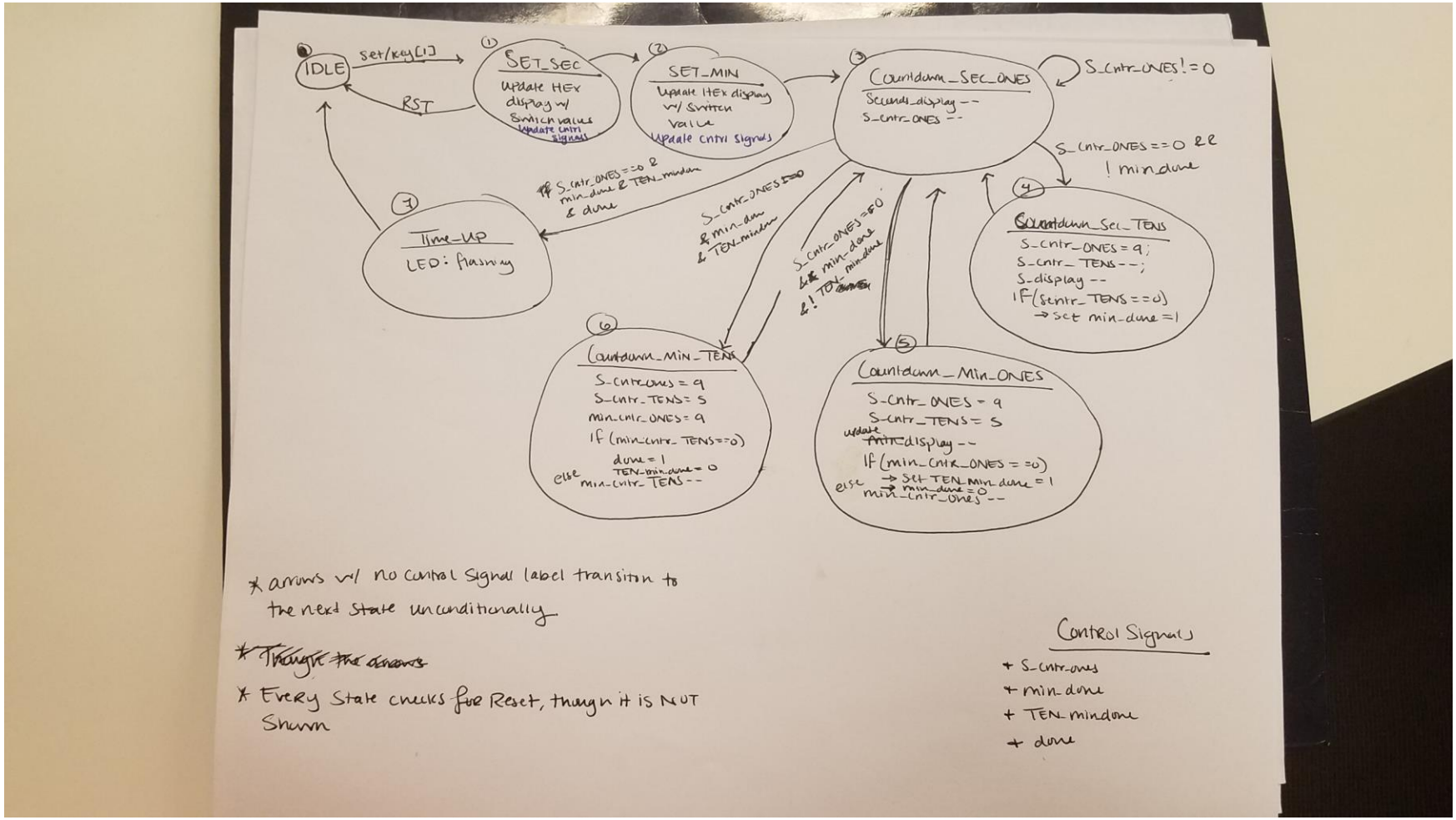
Counter

Increments or decrements by 1 on posedge of clock. Direction of change is determined by up_down value. Counter_width determines the maximum value that the counter can reach.



Timer (I do not expect to receive credit for a complete state diagram in the wrong format , but have included the image below in case it is needed as a reference.**)**




IDLE
set/key[1]
RST
1
SET_SEC
Update HEX display w/ Switch value
Update cntrl signals
2
SET_MIN
Update HEX display w/ Switch value
Update cntrl signals
3
Countdown_SEC_ONES
Seconds_display --
S_cntr_ONES --
S_cntr_ONES != 0
S_cntr_ONES == 0 && ! min_done
4
Countdown_Sec_TENS
S_cntr_ONES = 9;
S_cntr_TENS --;
S_display --
If (scntr_TENS == 0)
→ set min_done = 1
5
Countdown_Min_ONES
S_cntr_ONES = 9
S_cntr_TENS = 5
update display --
If (min_cntr_ONES == 0)
→ Set TEN_min_done = 1
→ min_done = 0
min_cntr_ONES --
else
6
Countdown_MIN_TENS
S_cntr_ONES = 9
S_cntr_TENS = 5
min_cntr_ONES = 9
If (min_cntr_TENS == 0)
done = 1
TEN_min_done = 0
else
min_cntr_TENS --
7
Time_UP
LED: flashing
If S_cntr_ONES == 0 & min_done & TEN_mindone & done
S_cntr_ONES == 0 & min_done & TEN_mindone
S_cntr_ONES == 0 & min_done & ! TEN_mindone
* arrows w/ no control signal label transition to the next state unconditionally
* Every State checks for Reset, though it is NOT Shown
Control Signals
+ S_cntr_ones
+ min_done
+ TEN_mindone
+ done