Oracle SPARC Solaris

HOW IT HANDLES PAGING

Overview

- Oracle Solaris
 - Unix operating system
 - Can run on SPARC or X86
- SPARC Scalable Processor Architecture
 - RISC Reduced Instruction Set Computer
 - Highly scalable using same core instruction sets
- Demand paged virtual memory
 - Pages are brought into memory as needed
 - Paging begins when memory exceeds a threshold

Paging Process Tables

- Multiple levels of tables
- Hashed page tables
 - One for kernel and one for all user processes
- Maps memory addresses from virtual to physical
- Each entry:
 - represents contiguous area of mapped virtual memory
 - Has base address and a span that indicates number of pages that it represents

The Process

- Translation look-aside buffer (TBL) use translation table entries (TTEs)
 from translation storage buffer (TSB)
 - Includes one entry per recently accessed page
- Search the TLB for translation when virtual address reference happens
- TLB Walk
- If match CPU copies entry to TLB
- If not match:
 - kernel interruption
 - Creates TTE from hash table and stores in TSB

General Paging Algorithm

- A memory deficit is noticed
- Page scanner thread runs and walks through memory
- A page is marked as unused
 - If stull unused after an amount of time, the page is viewed for reclaim
 - If modified, a request is made to the pageout thread to schedule the page for I/O
- As memory increases
 - increases the pages it chooses for candidates for reclamation increases
 - increases paging algorithm runs.
- Starts at 4% of one CPU for pageout operations and increases until 80% of one CPU is used

References

<u>Paging-Related Parameters - Oracle Solaris Tunable Parameters Reference Manual</u> <u>https://docs.oracle.com/cd/E23823 01/html/817-0404/chapter2-10.html</u>

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https://www.oracle.com/solaris/solaris11/