

UNIVERSITY OF CALIFORNIA SANTA CRUZ

SENIOR DESIGN FINAL REPORT

Hardware Validation of a Robust Hybrid Power Inverter

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to

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Department of Electrical Engineering



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Declaration of Authorship

We, Ryan Rodriguez and Ben Chainey, declare that this paper titled, 'Hardware Validation of a Robust Hybrid Power Inverter' and the work presented in it are our own. We confirm that:

- This work was done wholly or mainly while in candidature for a bachelors degree at this University.
- Where we have consulted the published work of others, this is always clearly attributed.
- Where we have quoted from the work of others, the source is always given. With the exception of such quotations, this report is entirely our own work.
- We have acknowledged all main sources of help.
- Where the report is based on work done by ourselves jointly with others, we have made clear exactly what was done by others and what We have contributed ourselves.

Signed:

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Date:

*"Don't think, **feel**. It is like a finger pointing out to the moon - don't concentrate on the finger, or you will miss all that heavenly glory."*

Bruce Lee

UNIVERSITY OF CALIFORNIA SANTA CRUZ

Abstract

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Hardware Validation of a Robust Hybrid Power Inverter

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The need for clean and renewable energy sources - coupled with the rapid growth in commercial and residential solar microgrid installations - has driven the development of a new hybrid algorithm for power conversion.

In a departure from traditional pulse-width modulation, or PWM, techniques, the new hybrid controller leverages a reference solution derived from the physical model of our circuit to determine a tracking band, or neighborhood, around the desired output sinusoid. Numerical results have shown that this technique results in a spectral content that is 'cleaner' than its PWM counterpart.[1]

In this design we utilize the canonical power inverter topology consisting of an H-Bridge followed by an RLC low-pass filter. We aim to confirm the computational results of this research with an implementation on a full microinverter system.

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Abbreviations

AC	Alternating Current
DC	Direct Current
DG	Distributed Generator
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
IC	Integrated Circuit
ISR	Interrupt Service Routine
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Squared
ROI	Return On Investment
THD	Total Harmonic Distortion
VER	Variable Energy Resource
μ C	Micro Controller

Symbols

h Planck's Constant $6.6 \times 10^{-34} (Js)$

I Current $A (Cs^{-1})$

P Power $W (Js^{-1})$

V Voltage $V (JC^{-1})$

ω angular frequency $rads^{-1}$

λ wavelength m

To those who came before us...

Chapter 1

The Problems with Solar

1.1 Motivation

Global demand for energy - combined with the surging interest in green technologies - has accelerated the need for a highly reliable, cost-efficient, and self-sustained electric power grid [7]. While scientists and engineers everywhere agree that the global dependence on power derived from heat-engines is a primary cause of the climate change phenomena wreaking havoc on our planet, the integration of renewables into the power grid remains a major engineering endeavor. Future energy distribution systems should be capable of interconnecting diverse power sources including fossil and nuclear-fueled generators, as well as renewable sources such as hydropower, wind turbines, and photovoltaic arrays without adversely affecting the stability of power grids.

While power derived from common thermodynamic cycles can be increased or decreased on-demand, renewable energy sources are dependent on highly variable environmental conditions, and hence, require robust power conversion techniques that can handle unstable and highly varying input power[4]. The focus of this research-oriented senior design project has been to explore the viability of implementing new hybrid control techniques for solar power conversion. This research is of great interest to us, and the public in general, as it may prove to be a valuable addition to the power system designers toolkit for situations necessitating exceptionally clean output with robust stability characteristics in the face of highly variable load and source conditions.

Renewables, sometimes referred to as variable energy resources (VERs), in contrast to traditional power plants are unpredictable and highly dependent on environmental factors. Observations at a solar farm in Arizona showed that output power fluctuated

by as much as 90% over the course of just a few seconds. This reality necessitates feedback controlled electronics to maintain stable power production. This project is focused on delivering a microinverter system as a robust solution for solar power applications.

We seek to understand the reported benefits of hybrid control techniques in the application of solar power converters. In particular, the conversion between the non-linear DC output of solar panels to the steady AC power used in the grid will be studied. In order to test the techniques which have been described analytically in [4], the Hybrid Inverter Team, in partial fulfillment of the requirements for the Bachelors of Science in Electrical Engineering, will develop a small-scale power inverter capable of switching between traditional pulse-width modulation and hybrid techniques. Our development platform will allow for the straightforward comparison between the two. This report is intended to be an exhaustive account of our methodology and research in the pursuit of these goals.

1.2 Background

In order to meet the challenges involved with implementing new hybrid power conversion technologies, we must first understand the current landscape of power inverters, analyze their strengths and weaknesses, and then assess how we might improve upon their implementations. To this end, we will undertake a brief overview of the pulse-width modulation technique, the applicability of hybrid control algorithms to the problem of power conversion, and finally, we will briefly review the additional constraints that photovoltaic (PV) sources place on our design.

1.2.1 Square and Modified Square Inverters

Square wave inverters are the simplest method for generating pseudo-sinusoidal outputs using an H-Bridge. They emulate the positive and negative half cycles of a sine with a simple bipolar scheme where the output is given to be either $+V_{dc}$ or $-V_{dc}$ respectively. After a filtering stage the resulting output can appear quite sinusoidal because primarily low frequency components of the square wave have been allowed to pass; however, closer inspection shows that real-world filters struggle to meet the very low cutoff requirements of the square wave inverter while maintaining a reasonable cost or form factor. As we will demonstrate in Chapter 2, the analog components needed to filter near 60Hz are prohibitively large and expensive. Note that the difference between a pure square wave and a modified square wave is the allowance of the

zero state determined by the quantity α shown in Figure 1.1 - this corresponds to a third state we will call $zero_{vdc}$. Note that the Fourier series of the output is given by

$$v_0(t) = \sum_{n,odd} V_n \sin(n\omega_0 t) \quad (1.1)$$

where

$$V_n = \frac{4V_{dc}}{n\pi} \cos(n\alpha) \quad (1.2)$$

The harmonic content can be controlled by varying the quantity α , and the amplitude can also be controlled by α . With some analysis, it could be shown that the harmonic content or the amplitude of the output can be controlled, but not both simultaneously unless we have a variable V_{dc} input. This variable input would add considerable complexity to existing inverter designs for applications that sought to control both variables independently.

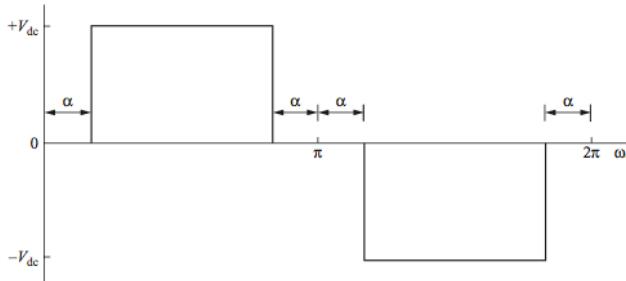


FIGURE 1.1: A modified square wave inverter crudely emulates the positive and negative half-cycles of a sine wave [1]

The ‘deal-breaker’ with the square wave inverter is the fact the the spectral content of the output is particularly rich at all odd harmonics of the fundamental. This means that we are left with a bulk of the harmonic content at the lower registers, which are particularly hard to filter.

1.2.2 Pulse Width Modulation Inverters

Pulse-width modulation (PWM), or bang-bang techniques, are a popular means for taking a fixed input voltage and varying the effective power seen at the output. This is done by rapidly switching the input off and on such that the the output is some fraction of the input including zero and one hundred percent. This fraction corresponds to what is referred to as the duty cycle. If we pair the PWM technique with the ability to drive current bidirectionally, say, through an H-Bridge circuit, we can use this technique to trace out a pseudo-sinusoidal output. PWM inverters are found almost exclusively in one of two flavors: bipolar and unipolar. In bipolar inverters, the H-bridge is allowed

to change state directly from $+V_{dc}$ to $-V_{dc}$, whereas in unipolar designs, the H-bridge is *not* allowed to switch directly from $+V_{dc}$ to $-V_{dc}$. Instead, unipolar inverters switch between from a positive output to zero, or from a negative output to zero.

Compared to square and modified square wave inverters, much of the filtering burden in a traditional PWM inverter is alleviated due to the fact that harmonics are shifted toward the frequency of the modulation index, typically at several tens or hundreds of kHz.

$$m_f = \frac{f_{tri}}{f_{sin}} \quad (1.3)$$

where f_{tri} is the frequency of the triangular carrier frequency, and f_{sin} is the sinusoidal reference signal. In contrast to the square wave inverters discussed above, with PWM it is possible to vary amplitude and frequency independently.

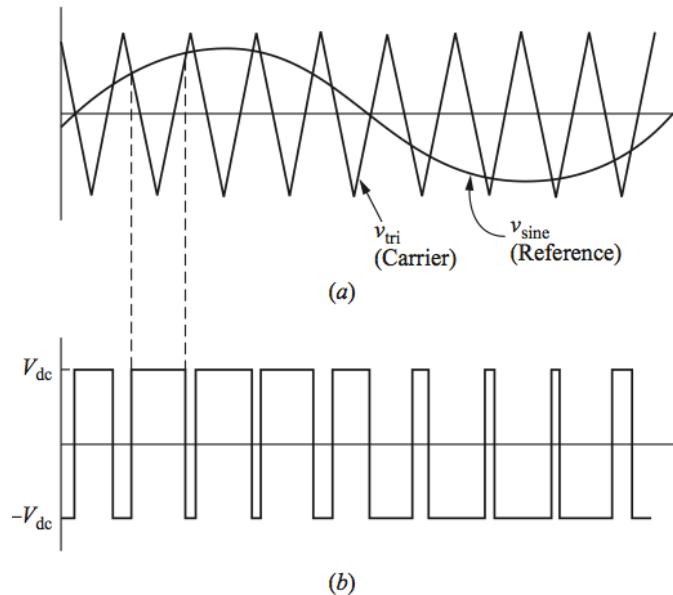


FIGURE 1.2: Bipolar switching uses a triangular carrier and a sinusoidal reference to change states from rail-to-rail. [1]

The effective voltage or current is varied by modulating the duration of on-time of a switch. The switch in this case can take the form of a relay, but more commonly in power applications takes the form of a field-effect transistor (MOSFET) or insulated gate bipolar transistor (IGBT). One can think of this in terms of a common household faucet with only two states, either fully on or off. If we were able to modulate the amount of time that the water flowed from the faucet, clearly we would be able to choose the volumetric flow-rate of the water from the two extrema - on or off - to an arbitrary level of precision depending on how fast we were able to switch the faucet. The scenario put forth in the 'kitchen sink' analogy is analogous to the situation we

face in a modern power inverter. In this case, we are faced with the challenge of taking a nominally fixed input voltage and switching it in such a way that we achieve a close approximation to a sinusoidal output voltage. Given the clear explanation of how PWM techniques can vary from fully on to fully off in the description above, it is easy to see why the PWM approach has become the standard for power inverters. Additionally, today's microcontrollers have extremely sophisticated peripheral modules built specifically for very fast and PWM signal generation, with resolution down to the nanosecond level becoming quite common.

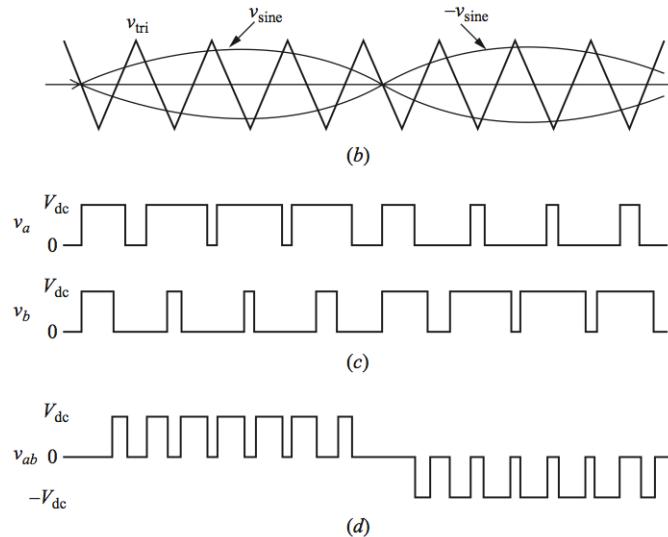


FIGURE 1.3: Unipolar switching uses a triangular carrier and a sinusoidal reference to change states from either rail to zero, but never from rail to rail.[1]

The Fourier analysis for either bipolar or unipolar PWM output signals is not as straightforward as that of the square wave, so a full derivation is saved for Section ???. However, the fact that the harmonic content occurs at multiples of the modulation frequency can be clearly observed in Figure 1.4.

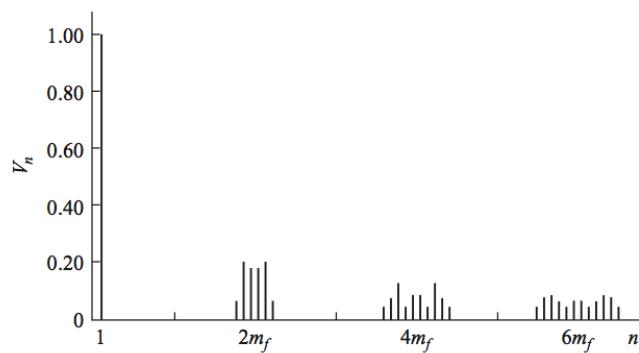


FIGURE 1.4: Fourier spectrum frequency diagram for both bipolar and unipolar pwm inverter control. Note that while the position of harmonics remains unchanged between either, the magnitude will likely differ. [1]

Although the PWM method for signal modulation has the clear advantages of widespread adoption and ease of implementation, we are increasingly faced with the problem of and the high-order noise into the power grid. Further, the typical proportional, integral, derivative, or PID methods for control suffer from a ‘ringing’ phenomena in the presence of the input disturbances. This ringing occurs as the controller attempts to correct for disturbances, and in the process overshoots its target. Because this process is not instantaneous, controllers also suffer from a lag in tracking their reference as the controller takes time to rise or fall to compensate for disturbances. In light of these issues with the traditional PWM techniques, we seek to explore alternate strategies for switching that might alleviate the vulnerability to input disturbances and the problem of an unintentionally rich spectrum at the output of PWM power converters.

1.2.3 Hybrid Systems and Hybrid Control

The study of hybrid systems has emerged in recent years as a response to the increasing entanglement of physical systems and computer control. Hybrid systems are those that exhibit both continuous and discrete-time dynamics. The system in question, namely the canonical power inverter topology, which is the focus of this research, is an excellent candidate for study under the lens of hybrid control due to the continuous evolution of a linear oscillator - our output filter - and the discrete time dynamics of the switch - in our case, a transistor receiving control signals from a micro.

We seek to understand how hybrid control might alleviate some of the challenges associated with PWM techniques, a few of which have been outlined above. While a detailed explanation of the hybrid control algorithm is saved for later on in this paper, in a nutshell, it has been found that with a relatively simple physical model of our system, and the ability to execute discrete state transitions, that we can generate outputs that closely resemble the desired sinusoidal outputs with less switching noise, and with a robust response to highly variable input voltages. For these reasons, we focus this research on the physical realization of such a hybrid system. One of the goals of this paper is to describe the algorithm designed by Jun Chai and Dr. Ricardo Sanfelice in more detail, and outline some of the challenges associated with realizing this implementation on a real world system [4].

1.2.3.1 The Hybrid Pulse Width Modulation Algorithm

A new hybrid systems based feedback control scheme for generating the switching signals of an H-bridge is being utilized in this inverter as an alternative to PWM signals

derived from the comparison of reference sinusoids and triangular carrier waves. Note that we believe it to be a bit of a misnomer to say that this technique is an alternative to PWM; rather, the hybrid controller offers an alternate means for *generating* the pulse-width modulated signal seen at the H-bridge. With the hybrid controller AC output stability is achieved by sampling the state of the system and comparing it to the ideal path of a linearly oscillating RLC filter [4]. The hardware implementation of the microinverter in this project will highlight the advantages and disadvantages of hybrid control versus traditional PWM.

1.2.4 The Problems with Solar

With the cost of photovoltaics rapidly decreasing, we have seen a rush toward the adoption of solar micro-grids which seek to exploit the most abundant source of power known to mankind - the sun. However, our heliocentric conundrum dictates that most places on earth receive time-dependent quantities of solar irradiance over the course of any given day. This high variability in the context of power conversion implies major challenges to our modern power grid which guarantees nearly continuous up-time and rock-solid stability.

Today's renewable power conversion technologies are not robust to highly variable input sources like solar power. Before utilities break ground on large-scale solar farms, complex and costly stability analysis must be done to ensure that the possible energy contribution outweighs the destabilizing effect of megawatts of energy that can be thrown out with an eclipse or fast moving cloud cover. Some other challenges with solar include the problem of shading or partial irradiance of solar arrays, and the non-linear nature of the photovoltaics themselves. This non-linear behavior necessitates the implementation of maximum power point tracking (MPPT) algorithms which comprehend this phenomena and harvest the most power from solar sources and inverters over their finite life spans. This is critical for obtaining the maximum benefit from the non-trivial investment required to operate solar arrays today.

1.3 Approach and Desired Outcomes

Can hybrid techniques for PWM generation handle disturbances more robustly, with less overshoot or rise time than traditional inverters? Can they convert power more efficiently? Can they do it more simply, or for less money? If any combination of these qualities hold for this new process, then we can say definitively that this technique is a viable alternative to the tried and tested PWM techniques prevalent today.

In order to answer these lofty questions satisfactorily, it was first necessary to develop the algorithms needed to run a traditional PWM inverter. This was done using the Solar Explorer by Texas Instruments. To perform a comparative analysis between traditional PWM techniques and the new hybrid algorithm, we deemed it necessary to build our own microinverter system to suit the power requirements requested by the Hybrid Systems Lab. The desired power handling capabilities of the device pointed us toward the microinverter scale. The system level overview for our microinverter is shown in Figure 1.5. This approach has several added benefits.

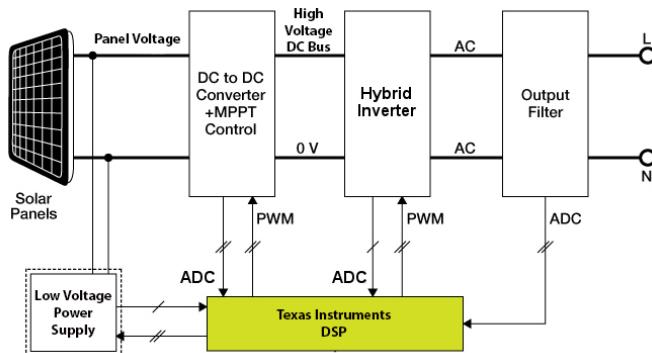


FIGURE 1.5: System level overview of the Hybrid Inverter Team's microinverter

It is widely accepted that distributed generators (DG) and the use of 'smart inverters' have a far less detrimental effect on the stability of the grid than centralized solar production, as in large solar farms. It has been suggested that smart inverters can even have a stabilizing effect on the grid by acting as frequency response reserves, regulating reserves, and ramping reserves that can respond to transient demands on the grid on the minutes to microseconds time-scale [7]. So-called 'microinverter' deployment strategies for solar systems offer improved reliability and potentially reduced installation costs. Widespread integration of microinverters with individual solar panels to form AC power generation units removes single-point failure risks found in common centralized PV inverter arrangements. Microinverters for single panels can have longer mean times between failures since they are often designed for the 200W power range and operate with lower temperatures due to reduced waste heat. The economies of scale for manufacturing many consumer microinverters reduces hardware costs found in building few larger high power PV inverters [8]. Another benefit of the microinverter approach is that the feedback mechanisms at work optimize the power generation of every panel in the system by each unit's particular conditions - this makes them robust in situations like partial shading.

Once the development platform was constructed, it was possible to test and debug the revision one hardware and plan on the second revision. Before, after, and during the hardware design process, we leaned heavily on the Solar Explorer development board

to test our algorithms and to bolster our understanding of inverter systems. With the revision two board, in addition to simulations in Matlab using the Hybrid Equations Toolbox and SimPowerSystems, we gained valuable data on how the hybrid inverter responds under basic load and source conditions. In particular, we performed Fourier analysis, measured efficiency, and analyzed how the systems responded to rapid disturbances.

Chapter 2

Hardware

2.1 Inverter Systems Overview

Power inverters are used for converting the DC power output of photovoltaic (PV) panels, batteries, or other DC sources into the AC power used in power grids worldwide. Our microinverter has three main power conversion stages, namely the DC/DC boost, H-bridge, and output filter. We will refer to the combination of H-Bridge and switching scheme frequently throughout this work simply as ‘the inverter.’ What we refer to as ‘the inverter’ consists of an H-Bridge and transistor driver hardware that creates the pseudo-sinusoidal wave from the high voltage DC output of the boost. The inverter is of central concern in this work, and in particular, the pseudo-sinusoidal waveforms that result from our control scheme - these were mentioned briefly in Sections 1.2.1, 1.2.2, and 1.2.3, but will be discussed in detail in Chapter 5, Section 5.1 - however, an inverter cannot operate in a vacuum. Therefore, we must first offer some background on the complete hardware system supporting the operation of the inverter system as a whole shown in Figure 1.5. The following subsections will provide a detailed account of the role that each component part plays in the system.

2.1.1 Logic Power Supply

Logic power is sourced from the solar panel via a buck converter IC; a buck converter is an efficient means of converting high DC voltages into smaller DC voltages without generating an excess of waste heat, as is typical with LDO regulators. The buck converter steps input voltage down from approximately 35 – 45V to 12V. To combat the relatively high harmonic content of the buck converter and the nefarious effect it would have on our sensitive analog circuitry, we use LDO’s to produce stable, and much

cleaner, 5V and 3.3V rails for the supporting cast of hardware on our inverter - namely, the microcontroller, FET gate drivers, and op-amp sensing circuits.

A logic power supply is required for the inverter board to run the microcontroller, driver circuits, and peripheral sensor network. Three different voltage rails were needed at 12V, 5V and 3.3V. The input from the solar panel was utilized to create these different power rails through a small connection circuit. Efficiency of this type of system is considered crucial, so cascaded switching DC/DC buck converters were used to create the 12V and 5V rails. A fast responding low-dropout linear regulator created the final 3.3V from the 5V rail. The circuit schematic for the logic power supply is shown in Figure B.1.

A variety of features were added to the front input interface for system protection and functionality. There are two options for sourcing power to the inverter board: banana jack connections for solar input and a DC barrel jack plug for testing input. These two circuits are configured so that only the barrel jack will source power if both happened connected and energized at the same time. Two switches are included for toggling the DC jack input and for switching conversion power into the main system. A ten amp blow fuse is included in series with the input to the inverter to prevent damaging short circuit conditions. A green LED on the 3.3V rail turns on to show the system is receiving power.

2.1.2 Boost Converter

The boost converter steps up the relatively low voltage sourced from one or two PV panels while implementing maximum power point tracking (MPPT) to keep the system operating near peak efficiency - this stage is critical for maximizing return on investment (ROI) in the face of the non-linear characteristics of the PV panel. The boost circuit trades current for voltage, much like a transformer, by harvesting the inductive kick of an inductor hooked up to a switch. By the fundamental relationship

$$V = L \frac{\delta i}{\delta t} \quad (2.1)$$

we see that the faster we can change current through the inductor, the larger voltage spike we can capture. This 'capture' is done with a diode and capacitor circuit.

A generic boost converter circuit is shown in Figure 2.1. The operation of a boost converter has two distinct phases depending on the switching mode of the power transistor. In this design, the gate of a MOSFET is sent different logic values at a specific duty cycles through PWM. When the drive circuit outputs logic high in Figure 2.1, the drain

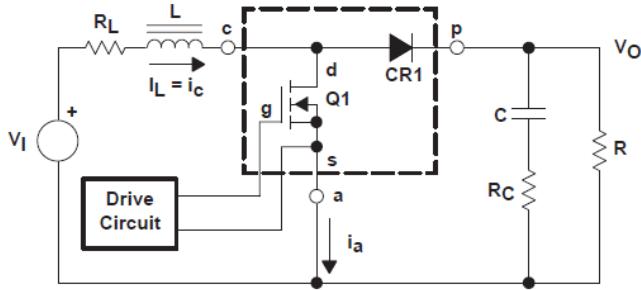


FIGURE 2.1: Traditional Boost Converter Circuit

to source path will conduct since the MOSFET is in the saturation region. This provides a path to ground for the current flowing through the inductor and reverse biases the clamp diode. While the transistor remains on, input current causes energy to be built up in the magnetic field of the inductor coil. Then logic low is sent to the MOSFET to shut it down. Considering the sudden change in current flow, a large voltage kick-back occurs across the inductor and forward biases the diode. Current now can flow to charge the output capacitor and feed the load.

When the MOSFET is conducting, the output capacitor provides power to the load until it receives new charge during the second switching mode. A large ripple current flows through the inductor as the switching takes place. Boost converters can operate in two different ways depending on inductor current values. Continuous conduction mode (CCM) happens when the inductor current remains greater than zero at all times. CCM ensures that the voltage gain function remains in linear relation solely with duty cycle D as shown in Equation 2.2. Discontinuous conduction mode (DCM) occurs when inductor current drops to zero during a switching cycle. The gain function for DCM, shown in Equation 2.3, is more complex since it includes additional circuit parameters like inductance and is dependent on the load.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \quad (2.2)$$

$$\frac{V_{out}}{V_{in}} = 1 + \frac{V_{in}D^2T}{2LI_{out}} \quad (2.3)$$

The Sharp solar panels we are using exhibit the nonlinear output voltage and current relationship typical of PVs. Therefore, power output is highly dependent on lighting conditions and loading, as shown in Figure 2.2. Maximum output power for the 170W panels occurs at $V_{pv,max} = 34.8V$ and $I_{pv,max} = 4.9A$. Boost output voltage is based on the minimum value needed for the $\frac{120V_{rms}}{0.707} = 169.73V$ peak value required for

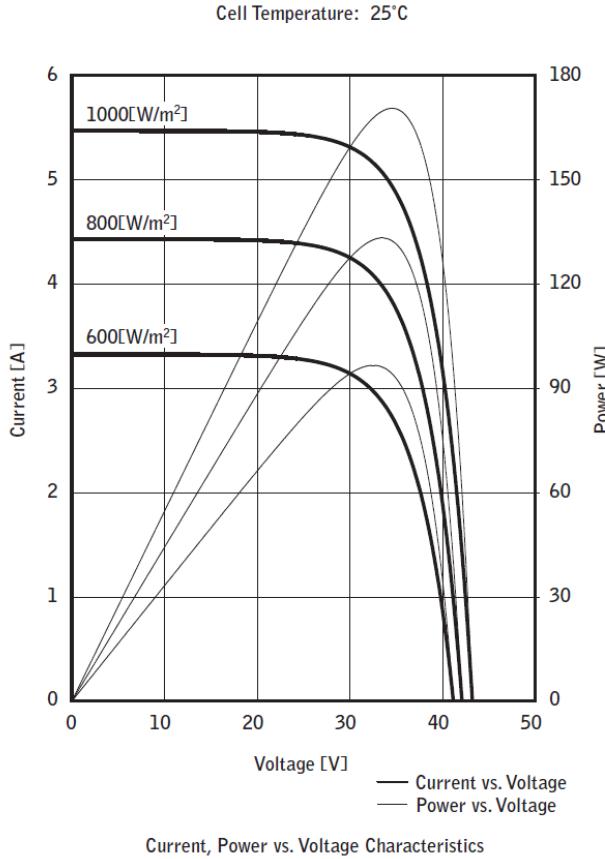


FIGURE 2.2: Solar Panel IV Characteristics[2]

the DC/AC inverter stage input. Maximum rated power of 200W is an upper limit selected for this design considering the solar panel approach with microinverter topology. Switching frequency is set at 50kHz based on recommended ranges and to compare to the TI Solar Explorer Development Board also used in this project.[2]

The process of designing the boost circuit hardware involved a review of application notes and running PSPICE simulations. The voltage at maximum power of the PV panels $V_{pv,max}$ was selected for primary simulation testing. Calculations were performed to best select power components for operation of the boost converter at high power values. Component requirements for SMPS applications also influence the material composition options for parts. An example of this is the need to use electrolytic capacitors to obtain necessary voltage ratings and storage capabilities. The main design steps consider power dissipation, thermal limits, critical inductance, and critical capacitance. The PSPICE circuit encapsulating the entire boost converter design is shown in Figure 2.3. The electrical specifications of this boost converter are listed in Table 2.1.

The operation of the boost converter in PSPICE requires a switching signal to control the power MOSFET. Implementation of the converter will utilize logic signals from a

Parameter	Value
$V_{in} = V_{panel}$	0V to 43.2V DC
I_{in}	5.47A DC max
$V_{out} = V_{load}$	200V DC max
I_{out}	1.18A DC max
P_{rated}	200W
$f_{switching}$	50 kHz
$\bar{\eta}$	83.84 %

TABLE 2.1: Electrical Specifications for Boost Converter

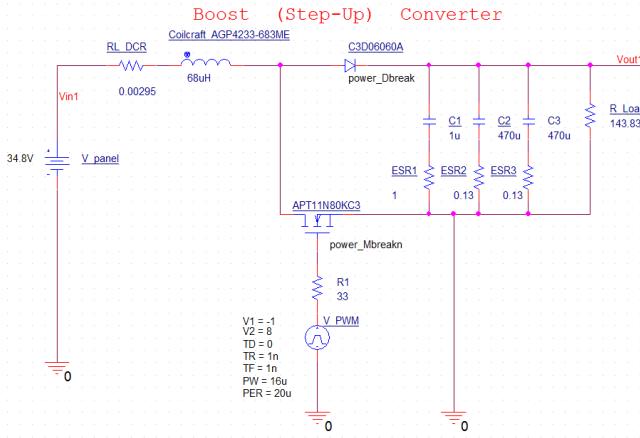


FIGURE 2.3: PSPICE Boost Converter Simulation

function generator fed into a Silicon Labs gate driver circuit used for MOSFET switching. This simulation uses a variable duty cycle for continuous switching at the set frequency. This configuration is currently being run open-loop, but will include a compensation feedback control system to maintain stable output voltage in the final design. The solar panel 34.8V input at max power requires a duty cycle set at 80.13% for the PWM switching signal to achieve 169.73V out. A load of 143.83Ω is connected at the output to simulate max power current draw and realize the 200W capability of the system. Real output power will be less in practice due to additional inefficiencies, panel operating conditions, and sourcing configuration capabilities. The output voltage, current, and power of the boost converter, as it approaches steady-state conditions from start-up, are shown in the simulation results of Figure 2.4.

The simulation and prototype boost circuits have open-loop operation such that manual variation of duty cycle is required to obtain a certain output. Since the solar panel voltage can vary, the simulation circuit runs at a minimum of 20V to check that the needed output voltage can be maintained. The simulation results confirm this with $V_{out} = 169.73V$, $V_{pv,in} = 20V$, and a new duty cycle set at 89.25%.

This boost converter was designed to operate in continuous condition mode (CCM).

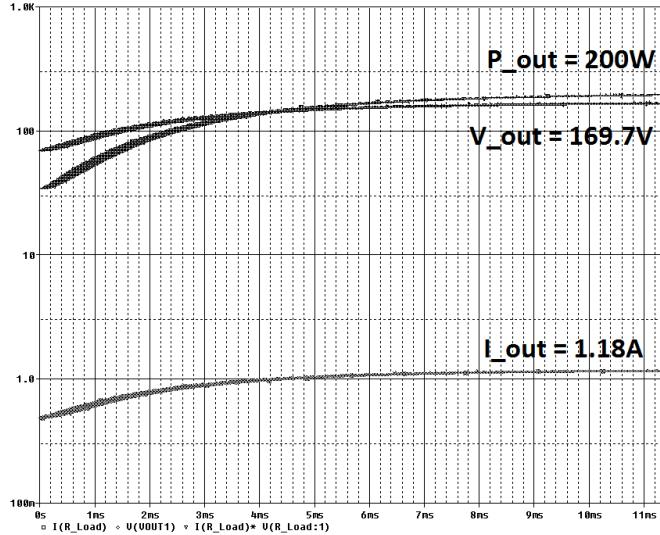


FIGURE 2.4: Boost Converter Approaching Steady State

This was achieved by selecting an inductor value above the calculated critical inductance and by making sure it has appropriate current handling capabilities. CCM requires the average inductor current to be larger than at least half of the load current. This is factored into the inductance calculation of Equation 2.4. Figure 2.5 shows the rippled inductor current during CCM and the MOSFET switching signal that creates these dynamic effects.

$$L_{critical} \geq \frac{R_{load,maxpower} D(1 - D)^2}{2f_{sw}} = 50\mu F \quad (2.4)$$

The series resistance of the inductor does not generate enough heat to justify heatsinking considering its large copper construction but it still dissipates power as estimated in the following equation.

$$P_L = (I_{in,rms})^2 R_L = (5.47A)^2 (0.025\Omega) = 0.75W \quad (2.5)$$

The clamp diode was selected to be a Silicon Carbide (SiC) Schottky since it offers fast recovery times with low reverse recovery charge Q_{rr} for reduced switching losses. Since the diode resides in the power conduction path, energy dissipation was analyzed. The diode was modeled as a series circuit of a temperature dependent voltage source V_{diode} and resistance R_{diode} .[9]

$$V_{diode} = \alpha T_{junction} + V_{diode,0} = 0.95V \quad (2.6)$$

$$R_{diode} = \beta T_{junction} + R_{diode,0} = 0.103\Omega \quad (2.7)$$

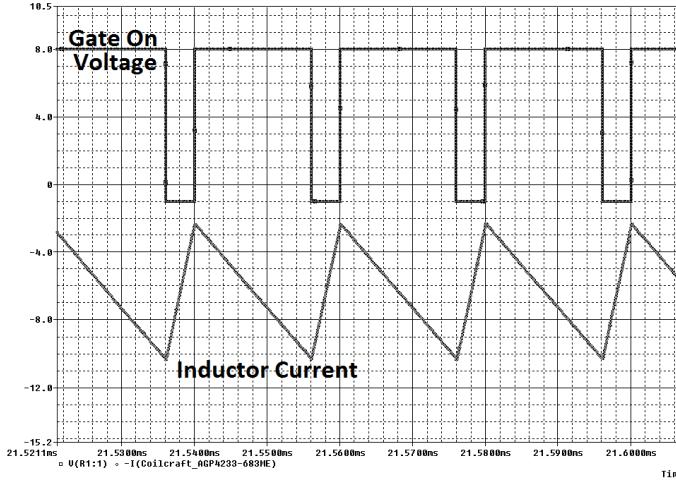


FIGURE 2.5: Switching Signal and Inductor Current

$$P_{cond} = I_{diode,rms}^2 R_{diode} + I_{out,max} V_{diode} = 2.76W \quad (2.8)$$

$$I_{diode,rms} = \frac{I_{out}}{\eta} \sqrt{\frac{16V_{out}}{3\pi V_{in}}} = 3.99A \quad (2.9)$$

$$P_{switching} = Q_{c,diode} V_{out} f_{sw} = 0.14W \quad (2.10)$$

$$P_{dissipation,diode,total} = P_{conduction} + P_{switching} = 2.91W \quad (2.11)$$

The 2.91W that the diode dissipates is significantly lower than the 136.3W rating for the device. Regardless, heat sinking it with a TO-220 bolt-on type sink is still a good practice.

The power MOSFET selected for the boost converter has very adequate voltage and current handling capabilities for the 200W design. The transistor experiences both switching and conduction power consumption which are shown in the following equations along with a thermal analysis for heatsinking.

$$V_{off} = V_{out} + V_{f,diode} = 171.53V \quad (2.12)$$

$$P_{cond} = \frac{1}{2} V_{off} I_D f_{sw} (t_{rise} + t_{fall}) = 0.68W \quad (2.13)$$

$$P_{sw} = C_{oss,FET} V_{off}^2 f_{sw} = 1.11W \quad (2.14)$$

$$P_{dissipation} = P_{cond} + P_{sw} = 1.79W \quad (2.15)$$

$$P_{limit} \leq \frac{T_J - T_A}{R_{\theta JA,max}} = 2.02W > 1.79W \quad (2.16)$$

$$R_{\theta JA,new} = \frac{T_J - T_A}{P_{diss}} = 71.02 \frac{^\circ C}{W} \quad (2.17)$$

$$R_{\theta SA} \leq R_{\theta JA,new} - R_{\theta JC} - R_{\theta CS} = 63.73 \frac{^{\circ}\text{C}}{\text{W}} \quad (2.18)$$

The 2.02W and 1.79W power losses calculated are close and thus heatsinking is required. The standard TO-220 heatsink with a thermal resistance of $25 \frac{^{\circ}\text{C}}{\text{W}}$ meets the criteria calculated in Equation 2.18.

The output capacitance was designed as a parallel arrangement of two values of capacitance for fast and slow transient response. This increases the total capacitance while reducing the equivalent series resistance (ESR) of the combination. This helps reduce the output voltage ripple of the boost converter. Since DC voltage output is required, a maximum ripple of $50\text{mV} = \delta V_{out}$ is selected as the tolerance. To achieve this voltage ripple design, a critical minimum output capacitance was calculated.[10]

$$D = 1 - \frac{V_{out}}{V_{in}} = 79.81\% \quad (2.19)$$

$$C_{critical} \geq \frac{V_{out}D}{F_{sw}\delta V_{out}R_{load,maxpower}} = 370\mu\text{F} \quad (2.20)$$

Voltage and current ratings for components are determined through worst case calculations.[11]

$$I_L = I_{diode} = I_{drain} = \frac{2}{\sqrt{3}}I_{in,rms} \quad (2.21)$$

$$V_{cap} = V_{out} = 1.5V_{out,typ} = 2(169.73\text{V}) = 254.6\text{V} \quad (2.22)$$

$$V_{diode} = V_{DS,FET} = 1.5(169.73\text{V}) = 339.46\text{V} \quad (2.23)$$

$$I_{cap} = I_{out,rms} = 1.18\text{A} \quad (2.24)$$

Figure B.8 contains the complete boost schematic which has many design concepts inspired by the Texas Instruments Solar Explorer Development environment.[12] The circuit schematic shows the conventional boost converter, the associated sensing and signal conditions circuits, and the gate driver circuit. The energy conversion portion of the boost board is shown in Figure B.2 with an additional input filter capacitor bank. The sensing of PV panel voltage and output voltage consisted of basic divider circuits with MCU pin protection diodes as shown in Figure B.3 and Figure B.7. The input PV current is measured with a shunt resistor IC with high common-mode rejection in Figure B.4. The switching transistor current is measured with a differential op-amp configuration as shown in Figure B.6. Lastly, the switched MOSFET has a low-side gate driver IC taking in PWM as depicted in Figure B.5.

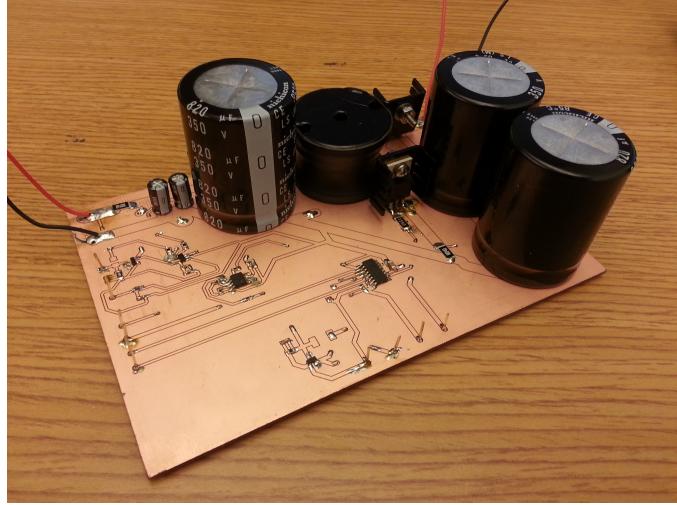


FIGURE 2.6: Assembled Boost Circuit

The top layer of the PCB design is shown in Figure B.9 and the bottom layer is shown in Figure B.10. The first generation prototype boost board PCB was created using an LPKF Protomat M60 router. This machine allows modified PCB gerber files to be milled into two-layer boards from standard copper clad plates. The resulting unpopulated boost board is shown in Figure B.11. The board was then populated with components into a completed circuit as shown in Figure 2.6. Testing of the boost circuit demonstrated its voltage gain capabilities with outputs reaching in excess of 120V during open-loop operation.

2.1.2.1 Boost Converter Efficiency

Energy conversion efficiency is an important factor for determining the effectiveness of the boost converter. Ideally, the circuit will have a 100% power conversion rate but in practice this is not feasible. Losses occur during periods of conduction and switching due to parasitic resistances and capacitances. Rates in the high ninetieth percentile have been achieved in some switching DC/DC converters but efficiencies falling more in the range of 90% to 70% are more common and can be deemed acceptable depending on the application. A first order estimate of the boost's efficiency η_{est} , with the MOSFET, diode and inductor loss considerations, is calculated in the following equation.

$$\eta_{est} = \frac{P_{in} - (P_{sw} + P_L + P_D)}{P_{in}} = 97\% \quad (2.25)$$

This is an optimistic conversion efficiency and does not fully encapsulate an array of other possible factors such as component tolerances and capacitive equivalent series resistances. A deviation of 10% is a fair engineering estimate on how much η_{est} could

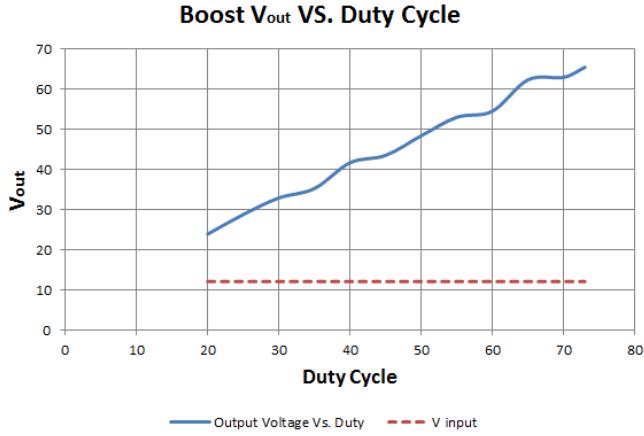


FIGURE 2.7: Boost Converter Output Voltage Vs. Duty Cycle

drift. The boost converter circuit prototype allows efficiency testing under the constraints of a laboratory environment. Experimental efficiency η_{exp} is calculated with the relationship shown in the following equation. The operating parameters of the test are: $V_{in} = 12V$, $R_{load} = 477.66\Omega$, $F_{switching} = 50kHz$.

$$\eta_{exp} = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2 / R_{load}}{V_{in} I_{in}} \quad (2.26)$$

The test uses different PWM duty cycles between 20% and 73% to obtain peak and average efficiencies as shown in the following equation.

$$\eta_{exp,peak} = 85.4\%, \bar{\eta}_{exp} = 83.84\% \quad (2.27)$$

As the testing indicates with $\bar{\eta}_{exp}$, the boost converter operates well within the range of standard energy conversion efficiencies. The boosted output voltage compared to input voltage over different duties is shown in Figure 2.7 and the voltage gain versus duty is shown in Figure 2.8. These results demonstrate how increasing the duty closer to 100% will increase the output voltage.

2.1.3 H-Bridge

Arguably, the lynch-pin of any inverter is the H-Bridge circuit. In order to generate a pseudo-sinusoid from a DC source, we must first have the means to switch this DC voltage on and off, and also to drive current bidirectionally. Thus, careful design of the H-Bridge circuit was a critical step in our development.

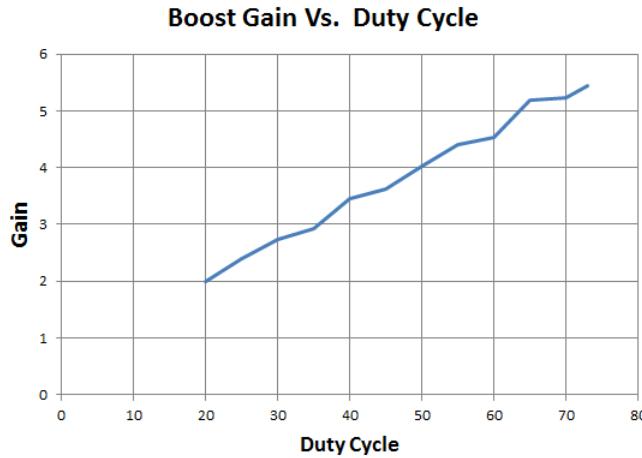


FIGURE 2.8: Boost Converter Gain Vs. Duty Cycle

For a successful H-Bridge design, we needed to consider a number of factors including the speed of switching, deadband, transistor type, transistor gate drivers, thermal analysis, and careful layout due to the speed of the signals involved and the resultant EMI.

After some analysis of the algorithm, further discussed in Chapters 3, and 5, we found that the speed of switching with the hybrid algorithm - unlike the switching speed of PWM algorithms which modulate over a fixed carrier frequency - was highly dependent on the width of the tracking band. Consequently, there is also a dependence on the resolution of the ADC, and the frequency at which our interrupt is serviced. Through simulations in Matlab we were able to determine that the speed at which the algorithm caused the inverter to switch were well under 100kHz for a 'small-enough' tracking band.

Because the switching speed is a function of width of the tracking band, sampling rate, and ADC resolution it is by no means a straightforward calculation to determine the frequency of switching. Contrast this to the PWM approach where this determination is trivial. In any case, because the switching speed was tunable by way of modifications to the width of the tracking band, it was decided that it was not necessary to go with more advanced FET technologies like Gallium Nitride that are more than capable of switching in the MHz range under full load.

Shoot-through is another important consideration with the H-Bridge circuit, as the possibility of a nearly direct path from power to ground can exist as the circuit switches from outputting +Vdc to -Vdc. To prevent this, a mandatory off time is implemented in software along with hardware protection afforded us by the gate drivers. In the configuration of the PWM driver in our micro controller code, a 330ns deadband was

implemented, based off of the 60MHz clock on the Piccolo. The drivers offer a nominal 70nS dead-time giving us robust, multi-tiered protection against shoot-through.

For the transistors in the H-Bridge, we decided on field effect transistors, (FETs), and in particular the CoolMOS™ variety built by Infineon. The IPP60 comes in a standard TO-220 package allowing for the use of standard heatsinks, has a Vds max of 650V - about three times what we would need - and a maximum continuous current of 31 Amps. Additionally, these FETs have a very low gate charge (low capacitance, smaller switching losses), low Rds on, and great slew rate. The fact that the drain to source resistance is low helps with our thermal budget, and also means higher efficiency overall. Because of the bipolar switching that the hybrid algorithm called for, we felt that it was wise to over specify our switches. Finally, the freewheeling diode found on many H-Bridge circuits was not needed here since the diode inherent to the construction of the FET was sufficient to handle any expected back currents in our load.

The heat sinks in our design are connected to the AC ground. Both the low-side and high-side transistors are insulated from the heat sink with thermal pads and insulating shoulder washers. According to the Transform application note we used as reference during our design, "For the high-side transistor, capacitance between the TO220 tab and the heat sink will add to switching loss, and so a thick and/or low permittivity insulator should be used."[\[13\]](#)

Because of the relatively high speeds involved with the H-Bridge, careful layout was especially important here. Parasitic capacitance on gate and drain loops are a main cause of overshoot and ringing in the circuit, and thus the total enclosed area between the gate drive and the FETs was kept to the absolute minimum. In order to minimize inductance in the output current path, high current power and ground planes were utilized. Small ferrite beads were used between the gate drive output and the gates of the FETs to reduce ringing caused by coupling of the drain current to the gate drive loop - these were found to be more useful than small resistances which are sometimes used [\[13\]](#). High voltage SMD ceramic bypass capacitors were placed directly underneath either side of the H-Bridge circuit to minimize the series inductance in the circuit.

2.1.3.1 Gate Drivers, Switching Loss, and Conduction Loss

Because we prefer the high-mobility of N-channel FETs, and because such an arrangement requires a 'bootstrap' circuit to allow the low-side FETs to operate in a half-bridge, we opted to use a gate driver IC by Silicon Labs. The SI823x have under-voltage protection to provide a higher noise margin to our control signal and prevent nuisance trips. They feature breakdown voltages of over 1kV, and can provide up to 4A to the gate's

of the FETs rapidly. We integrated the gate drivers with a bootstrap circuit to allow for operation as both a high-side and low-side driver and use N-type FETs for all four switching transistors.

The two primary modes of power loss in FETs are conduction losses and switching losses. Conduction losses occur because of the finite resistance between the drain and source of the device; the result is continuous power loss by ohmic heating. Unlike conduction loss, switching losses occur during transitions between states. The parasitic intrinsic capacitor at the gate of every FET needs a certain amount of charge in order to change states. This loss of charge to the switching signal is proportional to both the switching speed and capacitance intrinsic to the FET. As device size increases, i.e. as the FETs get larger, capacitance, and therefore switching loss, increases, but conduction loss decreases due to the lower overall resistance between drain and source. The converse is also true, and thus we have a tradeoff between conduction and switching loss in a particular device.

One of the primary factors in the overall efficiency of a modern switching power supply is the switching loss inherent to FET technology, and also the conduction loss associated with $R_{DS\text{ on}}$, the resistance of the FET from drain to source while it is conducting. Switching loss occurs whenever the FET changes state, and can be roughly understood as the net amount of charge it takes to drive the gate of the device. This amount of charge corresponds to a loss of current that could have gone to drive the load in question. This effect can be mitigated in some cases with parallel capacitance at the gate, using ‘faster’ FETs (higher slew-rate), and judiciously selecting the freewheeling diode[14]. Unavoidably, however, there is a trade-off between switching loss related to fast control signals of the H-bridge, or switching more slowly and dealing with bulky analog components and the loss associated with them.

2.1.4 RLC Output Filter

The output filter must attenuate high frequency switching noise while passing the 60Hz fundamental intended for standard loads. In a typical PWM design, the driver factor behind the cutoff frequency of the output filter is the carrier frequency of the PWM signal. In most cases, this carrier frequency is invariant, and therefore allows for a relatively straightforward design parameter during the time where components are selected. Of course, THD is also a primary driver of part selection and valuation of the analog components.

In order to ensure that the vector fields on the power plane are such that the hybrid algorithm can ensure forward invariance, and that the solution of the system converges

to the tracking band in finite time, it is necessary that our design adhere to a set of constraints on the RLC filter described in [4].

Namely, our filter components must meet the following constraints: first, we must satisfy the condition that $LC\omega^2 > 1$ - this property ensures our vector fields are oriented correctly throughout the desired trajectory on the VI plane. Second, we have that the capacitor value must be determined by the output voltage amplitude and current amplitude by the relation: $\frac{I_l\omega}{V_c}$ where I_l is the target output current, and V_c is the target output voltage. From this final condition we observe that the value of the capacitance can be driven up by increasing the target current, decreasing the target voltage, or increasing the frequency of operation.

Let's examine this mathematical condition through the lens of circuit analysis. By inspection, we note the similarity of this condition to the condition for resonance in a series RLC circuit - which is the subject of study in [4]. This condition is given by $\omega_0 = \frac{1}{\sqrt{LC}}$. Taking the square of both sides in the expression, find that $\omega_0^2 LC = 1$, and we see that the condition on the filter components given states that the resonant frequency of the circuit ought to be greater than unity. If we suppress the variable for capacitance in $LC\omega^2 > 1$ given the condition $C = \frac{I_l\omega}{V_c}$, we obtain:

$$L > \frac{V_c}{I_l\omega^2} \quad (2.28)$$

The expression obtained in 2.28 adds a considerable degree of inductance compared to that in a typical PWM inverter. It was considered initially that the quality factor, Q might be at work in the conditions on the filter, but we find that the quality factor for the series RLC filter is given as $Q = \frac{1}{R} \sqrt{\frac{1}{LC}}$, and the analysis in [4] makes no mention of the damping term R .

Subsequent testing on filters that do not adhere to this constraint must be conducted to determine the viability of this algorithm in applications in inverters in the sub-1kW range. Although we have not conducted research on filters for higher power systems, in the regions of interest for this paper this filtering constraint has proved to be quite costly and bulky.

We constructed our filters using 'power reactor' inductors from Triad magnetics. They are values at 35mH each if their coils are wired in series, or around 6mH if their coils are wound in parallel. To be clear, each inductor is constructed of a pair of inductors. Correspondingly, our maximum current decreases at the higher inductance, roughly 5A when wired in series, and maintains the rated inductance in the parallel configuration with a 10A rating. Inductors beyond this current rating were typically found

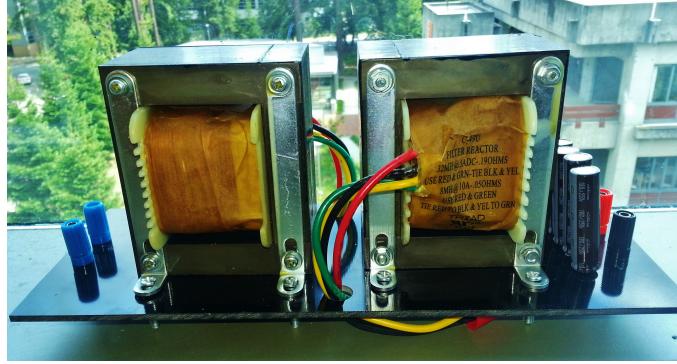


FIGURE 2.9: RLC Resonant Filter

to have lower inductances and prohibitively high prices for our research. This limit on inductance is very much a materials science problem; as the current through the inductors increases, the cores used in their construction saturate and limit the effective inductance.

Using the constraint given above, we sized electrolytic capacitors for our series RLC filter. Because electrolytics are polar devices, we needed to use a special configuration where we used electrolytic pairs to construct non-polar electrolytic capacitors. This was found to be a relatively common trick, but we performed several stress tests to verify the robustness of this solution. Regardless, electrolytics are understood to be the weak-link in the lifespan of inverters with their short mean time to failure at moderate to high temperatures. The final filter design constructed on turret board is shown in Figure 2.9.

2.1.5 Feedback Sense

The sensor network is important for the operation of the inverter since it allows the microcontroller to monitor voltages and currents for feedback control. Voltage dividers are used to measure high potentials around the boost converter and filter outputs. The inverter's AC output voltage is measured by a differential op-amp with a DC offset of 1.65V to allow for the input signal's negative potential swings. A differential comparator IC implements zero cross detection as the biased AC wave oscillates above and below the DC reference.

Inverter output current is measured through the use of two shunt resistors in the low-side legs of the H-bridge. The small voltage drops on these 0.04Ω resistors are conditioned by two differential amplifiers. The difference between the two signals from the legs is calculated by the microcontroller to evaluate the output current. A secondary Hall effect IC is inline with one of the H-bridge outputs so that it can noninvasively

measure a signal linearly proportional to the AC current by using it's changing magnetic field.

2.1.6 The Microcontroller

At the core of our inverter system is the Texas Instruments F28035 'Piccolo' microcontroller. This embedded controller's internal architecture is optimized for the real time control of devices like switching power converters. The Piccolo has a control law co-processor that can operate complex feedback loops without burdening the main processor, freeing the central unit to perform higher level tasks. The device also features versatile pulse width modulation units which are connected to the general purpose outputs for driving the switching power transistors of the boost converter and H-bridge.

With the myriad of choices available to designers of power systems, the task of selecting a microcontroller for a power conversion system is no easy task. The first step was to survey the current landscape and find some examples of the most popular microcontroller choices currently being used in power applications today. The controllers that we found most frequently were the dsPic family by Microchip, and the Piccolo family by Texas Instruments. The reasons that these two families have found dominance in this field became obvious: they were low cost, had detailed documentation and application notes for power conversion, and support for the 'real-time' control loops that our application demands.

With the choice narrowed down to two families of processors, the task of selecting a processor boiled down to a cost/benefit analysis between the two. Both had similar power consumption, but the TI family of Piccolo controllers came with the option of faster clock speeds, and correspondingly, faster ADC sampling times. Additionally, the resolution of the PWM and ADC modules was more precise than those of comparable Microchip controllers. The final check-box in the TI column was the tight integration of the Piccolo family of controllers with two of the power development boards that we were considering - the Solar Explorer by TI, and a competing offering by Transphorm.

With code portability from our development kit to a final implementation being of paramount importance, it was decided that we should go with the Piccolo family. In particular, we chose the F28035 for its mix of speed, low-cost, and wide array of digital control capabilities including a unique co-processor feature known as the CLA which enables offloading of many control implementable in assembly. With the integration of this Control Law Accelerator or CLA, we are able to significantly increase the complexity of our algorithms for a given clock speed, while also running multiple state

machines and servicing interrupts occurring at multiple frequencies - all while doing it *faster* than would be possible on competing microcontrollers.

Our final hardware design includes anti-aliasing filters for all ADC inputs, and is capable of outputting the values measured at the ADC to DAC pins for debugging purposes. The system uses a 20MHz crystal to set the pace for a phase-locked system clock of 60MHz. External hardware in support of the microcontroller includes voltage protection diodes on GPIO and ADC pins, and isolated communication circuits allowing for the use of USB debugging while protecting against ground loops.

2.1.6.1 USB-JTAG interface

The Piccolo microcontroller supports JTAG boundary scanning for device programming and real time debugging. To connect through the JTAG circuit, several integrated circuit solutions are implemented on our inverter. Programming, or ‘flashing’ the micro with code compiled on a workstation necessitates a USB connection to the inverter board. A Future Technology Devices International (FTDI) FT2232D is used to interface a mini USB with the micro by converting the signals to UART. This device also allows the configuration of an EEPROM flash memory array for use with the proprietary Texas Instruments XDS100 debugger use by the Code Composer Studio IDE. The USB connection provides its own power to the JTAG conversion circuit, so galvanic isolation is used between the USB power supply and that of the main inverter board to prevent ground loops. Digital signals are sent between the two subsystems through a series of digital isolator ICs which use capacitive coupling. A Texas Instruments IC MAX3221 is used as an RS-232 driver/receiver for the serial RX and TX connections between the FTDI chip and the microcontroller.

2.2 Photovoltaics

Photovoltaics, more commonly known as solar panels or solar cells, operate by the principle known as the photoelectric effect. The description of this phenomena won Albert Einstein the Nobel prize in 1905. In this work, he described the quantized energy carried by photons. This energy was found to be $E = h\nu$, where h is Planck's constant. If we have a pn junction with a thin, heavily doped n region, then a depletion region exists between the two materials. This region is observed to extend primarily into the p region with an electric field E_0 . While we need electrodes to construct a ‘bulk’ solar cell, these electrodes must also allow light to enter the device. This is typically done by forming

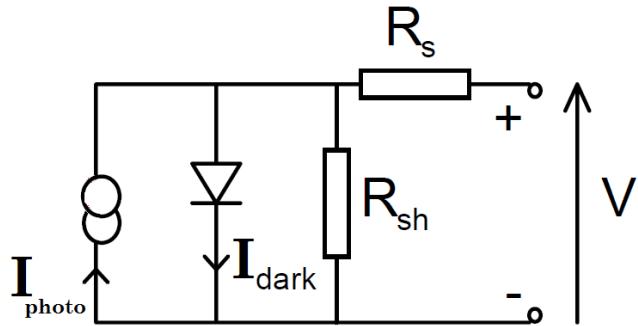


FIGURE 2.10: Circuit Model of Solar Cell[3]

electrodes into thin finger like structures on the surface. Additionally, antireflective coatings are typically applied to maximize light incident upon the device [15].

If we engineer a semiconducting material with a bandgap tuned to the wavelengths of photons emitted from the sun, then the photons strongly interact with the material and are absorbed. The net effect is the emission of electrons which result in an open circuit voltage between the *p* type and *n* type materials. If we complete this circuit, we will obviously obtain an electric current which can be used to drive DC loads - this current is known as a photocurrent.

The engineering of semiconducting materials that can interact with broad ranges of wavelengths is the subject of much research, but is entirely beyond the scope of this report. Rather, we are more concerned with harnessing the direct photocurrents from PV systems readily available today and turning them into alternating currents.

In order to achieve this goal we must understand the non-linear relationship between the power generated by solar panels and their operating conditions. From an electrical standpoint, a solar cell is best represented through an engineering circuit model of a current source in parallel with a diode. Two significant parasitic resistances are included in series and parallel positions in the model to account for the physical factors of a solar cell. The current source is responsible for the photocurrent I_{photo} generation due to incident light and will feed DC loads present on the cell's terminals. The diode contributes to a dark current I_{dark} which counters the positive photocurrent and accounts for cell loading. The circuit model of an individual solar cell is shown in Figure 2.10. [3]

Depending on the load, two important parameters can be determined for a solar cell: open circuit voltage V_{oc} and short circuit current I_{sc} . The short circuit current will be directly proportional to the intensity of a certain light frequency spectrum for the solar cell and I_{sc} will have a finite maximum value based on the efficiency of the panel. The open circuit voltage occurs when there is no load, massive impedance on the cell

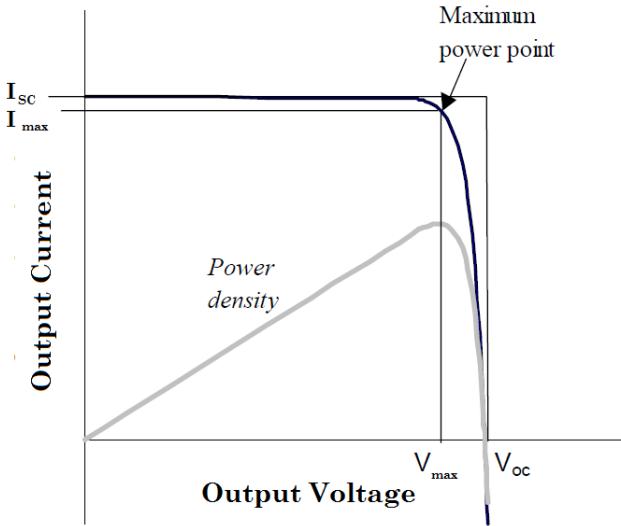


FIGURE 2.11: Output Voltage Vs. Current of a Solar Cell[3]

terminals, and the dark current through the shunt diode derails any photocurrent. The diode potential drop creates the largest effects on the voltage profile of the solar cell and adds to the non-linearity of the I-V plot for the system as shown in Figure 2.11. [3]

Drawing maximum power from the solar unit requires a specific DC load which optimizes the product of photocurrent and output terminal voltage to produce the largest possible value. This sourcing configuration is known as the maximum power point that a solar inverter will ideally operate at by varying its impedance. The I-V curve indicates best performance for energy generation when it closely matches a square since this maximizes the power density of the solar cell. Deviations from this optimal shape occur due to the parasitic elements in the engineering model. Output current can be undesirably leeched through the parasitic shunt resistance R_{sh} which is due to current leaks in the semiconductors. The output current is also hindered by the series resistance R_s which is present due to contact resistances. Larger R_{sh} and smaller R_s values indicate higher quality solar cells. Increased temperatures will also negatively effects the cells by decreasing the maximum possible output voltages.

Solar cells each typically produce under 1V, so multiple cells are be connected in series to create a panel with a useful voltage range. The forward diode in the cell's circuit model has the possibility of drawing current from neighboring cells when they are collected in parallel. Reversed blocking diodes are placed within the panel circuit to mitigate this as the individual cell outputs vary. The complete solar panel features many submodules of solar cells connected to a DC bus network which are then interface with polarized output leads.



FIGURE 2.12: The Hybrid Inverter Team's assembled PCB

2.3 The Hybrid Inverter Team Development Board

The Hybrid Inverter Team's development board will allow power systems researchers to implement and test new control techniques on an extensible piece of hardware. The HIT development board can handle around 250W, and is capable of outputting 120VRMS from typical solar panel input. In effect, our module is a higher power replacement for TI's Solar Explorer development board with several key changes. Several of the auxiliary modules included with the Solar Explorer that were unnecessary for our design were omitted. The omitted modules included the second microcontroller for solar panel emulation, as well as the SEPIC converter used for battery charging. With the already lofty goal of building a full switch-mode boost and inverter, we felt it would be a great deal of added complexity to build, code, and troubleshoot the SEPIC battery charger for our senior design project. The panel emulator was unnecessary since we would either be running the board from an ATX power supply, or a real solar panel.

Our PCB layout utilizes a four layer design with power and ground planes on the two middle layers. Multiple layers allow for components to be placed closer together to achieve a smaller overall form factor. Additionally, there are polygon pours on the central power layers to increase current carrying capacity and aid in the dissipation of heat. Ground plane isolation is used to separate areas with switching power signals and digital logic.

Development of the PCB layout was done with EAGLE to create the top layer as shown in Figure B.14 and the bottom layer shown in Figure B.15. We went through Circuits for PCB fabrication, while components were purchased from Digi-Key. The completed circuit board is displayed in Figure 2.12.



FIGURE 2.13: Solar Panel Stand

Following the microinverter topology, the inverter sits in an enclosure mounted to the back of a solar panel. The output filter and transformer are constructed using turret board, and are also attached on the panel mounting system. For testing in outdoor sunlight environments, a wooden stand for the solar panel and inverter system is used as shown in Figure 2.13.

2.3.1 Revision Two of the Hybrid Inverter Team Board

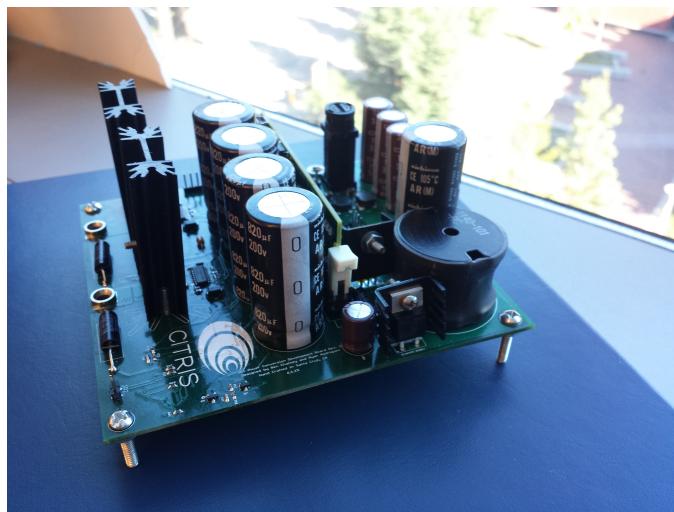


FIGURE 2.14: Completed HIT Board Revision 2

Revision one was found to have a few weak links in the signal chain, namely an undersized trace from the source of the boost FET to the shunt resistor in the path to ground, and a microcontroller layout that was too ambitious given the debugging timeframe. We opted to replace the microcontroller layout with a 100-dimm slot capable of holding a TI ISO-control card. This alleviated the possibility of a small error in the micro layout

derailing our progress, and also had the added benefit of shrinking our board layout slightly. The rearrangement of components necessitated a re-pouring of some power planes to accommodate capacitors that were placed closer to the H-bridge.

The new layout facilitated cutouts in the ground plane that vectored high current injections to the ground plane around both the microcontroller and the sense circuitry. Because banana plugs are relatively expensive and bulky, we omitted a pair dedicated to retrieving feedback signals from the off-board filter with pin headers as these signals are not particularly high current. The completed second generation Hybrid Inverter Team board is shown [2.14](#). PCB layouts of the top and bottom sections can be found in [B.14](#) and [B.15](#). The final schematic designs are shown in the appendix entries: [B.16](#), [B.17](#), [B.18](#), and [B.19](#).

Chapter 3

Software Implementation of the Inverter

3.1 Software System Overview

As with any microcontroller system, it is necessary to first configure the various low level peripherals such as the analog to digital converter (ADC), digital to analog converter (DAC), PWM, phase synchronization of PWM interrupts, PWM safety trips to avoid over-voltage conditions, clock and PLL configurations, and etc. The next step in the development was to design a logical, well organized and most importantly, extensible, software system to work with. The first phase in this development was to build a state framework for the organization of the various tasks associated with our power conversion system, namely the MPPT algorithm, tasks associated with power-up and shutdown, and instances where the power from the solar source is no longer sufficient to meet our output power guarantees. Quite secondarily, we also utilize these state machines to run LED indicators that show the code is operating as expected. The high level overview of the software can be seen in Figure 3.1.

The two primary tasks of the software system are undoubtedly the control of the DC boost circuit, and the control of the inverter hardware. These tasks are pictured in Figure 3.2 and Figure 3.4 respectively. These tasks are performed using interrupt service routines (ISRs) that are cued by the rising edge of a PWM signal. These signals offer a convenient way to trigger the interrupts, as well as the start of conversion (SOC) for the ADC. The SOC begins a sequential sampling of all the control signals on the board, making the most recent data available just in time for the execution of the ISR. Note that the PWM signals used for triggering interrupts are separate from the PWM signals used for switching the transistors. With the execution of rapid-fire service routines, we

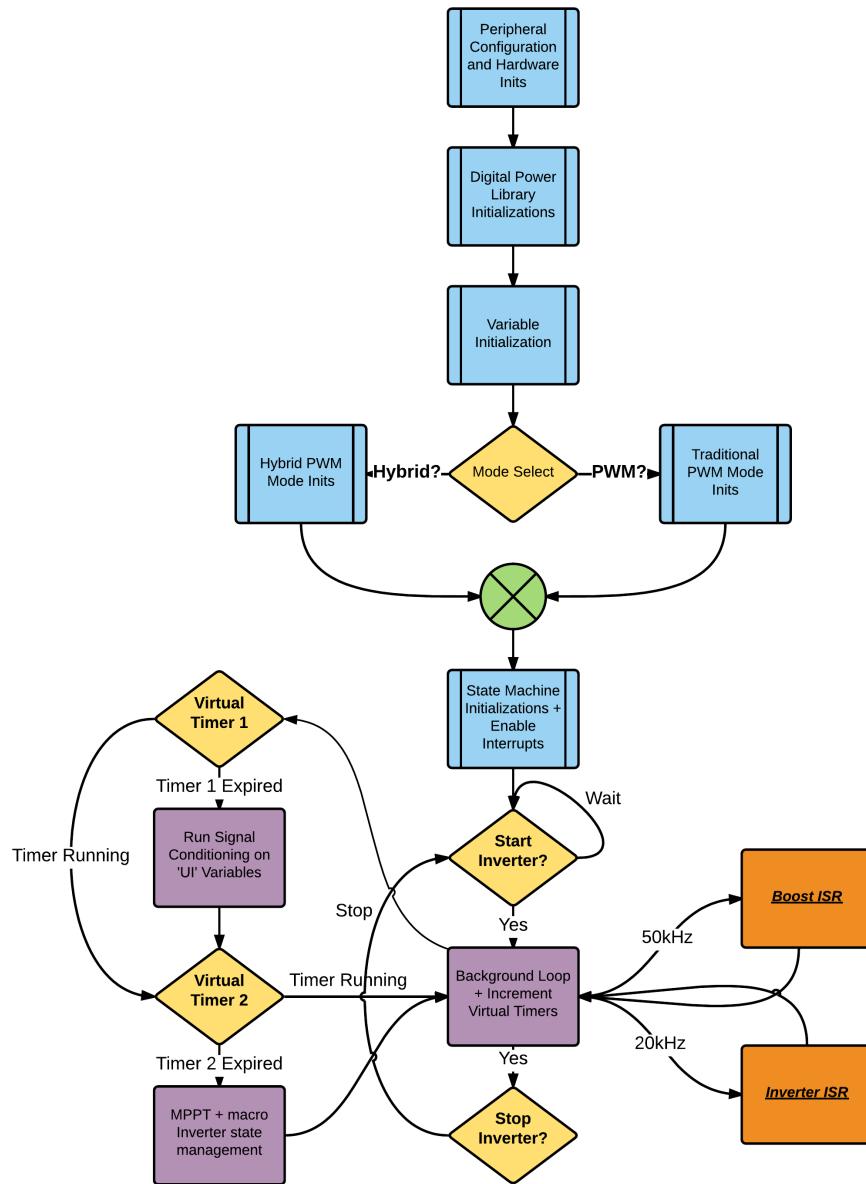


FIGURE 3.1: Software system level overview showing the configuration of the micro, followed by an infinite loop where we run state machines on virtual timers, and service interrupts

may encounter the problematic condition where both ISRs attempt to fire at the same time. Instead of having the service routines fight for processor time with mechanisms like priorities, we opt to implement a phase synchronization scheme wherein the two PWM modules firing off interrupts are separated by a pre-determined phase margin. This phase margin allows us to specify the time between rising edges of both PWM signals in relation to each other, the result being two dependent PWM channels that offer us an assurance that there will be no processor contention as long as we service either interrupt in a reasonable amount of clock cycles.

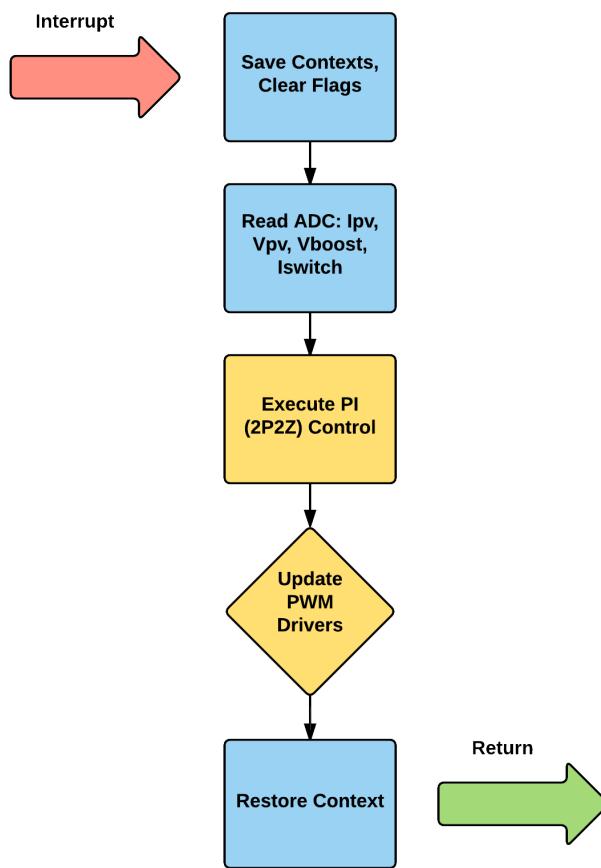


FIGURE 3.2: Software diagram of the ‘fast’ 50kHz boost ISR

3.1.1 State Framework

Although simple state frameworks are possible using functions as a sort of ‘pseudo state,’ these implementations tend to become exceedingly complex and hard to follow for non-trivial state machines. Further, cobbling together new state machines or adding new states can be a daunting task resulting in spaghetti code.

For these reasons, we decided to 'roll our own' state framework using object oriented patterns in C. This involved creating an FSM structure that holds a reference to an FSM object. This FSM object is actually a type defined variable that is, loosely speaking, of the type 'pointer to function'. Additionally, this strategy necessitated the implementation of several helper functions for various tasks like constructing the FSM object, state initialization, state transitions, and event dispatching.

The custom 'pointer to function' type is declared in C as follows:

```
typedef void (*State)(Fsm *, Event const *);
```

The definition above used the C keyword `typedef`. What `typedef` allows us to do is to declare a new data type for our own use. In this case, our type is 'pointer to function.' This is an enabling tool for representing the state of a machine as a function.

The next step is to use structures to organize all of our data in a meaningful way - for our purposes, you can think of these structs as classes, save for the fact that their methods are declared outside of the structure itself. The structure for the FSM itself is defined as follows:

```
struct Fsm
{
    State state__; /* the current state */
};
```

The `Fsm` struct stores the function pointer as its sole attribute. Note that we use the trailing underscores to indicate that the variable is private and should not be tampered with in a nod to the Python style of adding leading underscores to indicate such members of classes.

Students of electrical and computer engineering should be familiar with the concept that state machines respond to what are formally known as 'input alphabets.' These alphabets have strict definitions from a mathematical standpoint, but for our purposes, all we need to understand is that the machine should transition according to a certain mapping if it gets an event, and should - typically - do nothing if we do not send it an event. Accordingly, we should also declare some structure to manage event signals. This is done with

```
struct Event
{
    Signal signal;
};
```

At this point we're ready to implement the functions that will manage this framework and allow for the creation of arbitrary state machines. These functions are inlined for speed - they eliminate a lot of the overhead of normal function calls - and they are well suited to this implementation since we are very concerned with speed and efficiency on our micros.

First up, we need to initialize the current state, i.e. give it something to point to. We will create an Fsm struct and invoke a function pointer for it to use. We will also set this pointer to the initial state of the FSM. We will do this with:

```
#define _FsmCtor_(self_, init_) ((self_)->state__ = (State)(init_))
```

The result is that our FSM's state member now points to a function which serves as our initial state. Next, it is desirable to go about triggering our initial transition. This is to say, our FSM now points to the function we are using as the initialization state where we can do all the prep work we may need for the smooth operation of the FSM, but now we want to get to work and make the machine run. We will trigger the initial transition with the following:

```
#define FsmInit(self_, e_) (*(self_)->state__)((self_), (e_))
```

Now we've got a state machine that is in some state - the FSM 'class' is pointing to some function we are using as a state - and we are ready to respond to events. How do we do it? With this inlined macro:

```
#define FsmDispatch(self_, e_) (*(self_)->state__)((self_), (e_))
```

This will take some member of our particular Event structure that we defined above, and send the event to the function for it to respond to. This response is usually some action or state transition, or both. Finally, to round out our FSM back-bone functions, we need something to actually implement the state transition, i.e. some function that updates the pointer and sets it to the new state when appropriate. This is accomplished with the following macro:

```
#define _FsmTran_(self_, targ_) ((self_)->state__ = (State)(targ_))
```

Note that the function is called within the state functions themselves. Because the implementation of the state framework was, in our collective opinion, a major design hurdle, we feel it is productive to give the user a sense of the simplicity that this implementation imparts on FSM implementations. This is a particularly useful feature for us

since we have several state machines in our systems, and the overall software design goal is extensibility.

```
int main()
{
    int returner = 0;
    hBridge k;
    hBridgeCtor(&k);
    FsmInit((Fsm *)&k, 0);
    for (;;)
    {
        hBridgeEvent ke;
        ke.code = getc(stdin); //replaced by ADC input in uC
        getc(stdin);
        returner = hBridgeTransitionFunction(k, &ke);
        if(returner == -1) return 0;
        FsmDispatch((Fsm *)&k, (Event *)&ke); //dispatch
    }
    return 0;
}
```

While this brief example departs from our actual implementation on the micro, it gives a quick overview of why the time spent developing this state framework was time well-spent, and hopefully provides some insight as to why the research into this area was worthwhile.

3.1.2 The Digital Power Library

One of the key features that made the Piccolo family of micro's an attractive option was the extensive power library that the the micro offered. In particular, the chip has the capability to run digital compensators of the 2P2Z form described in the section on the boost controller, and 3P3Z compensators as well. In addition, we have the ability to implement PID controllers with on-the-fly coefficient tuning via JTAG.

3.2 The PWM Algorithm Implementation Details

In order to assess the performance of the hybrid controller, we first needed to develop and assess the baseline performance of a typical PWM implementation. This was done using the C2000 DSP which has generous functionality for accomplishing power conversion tasks. We decided to implement a unipolar PWM algorithm due to it's relative simplicity, and also because it is the most commonly implemented algorithm found on inverters today. The gist of the unipolar inverter algorithm is covered in Section 1.2.2. Here, we will detail the specifics of the implementation on the micro.

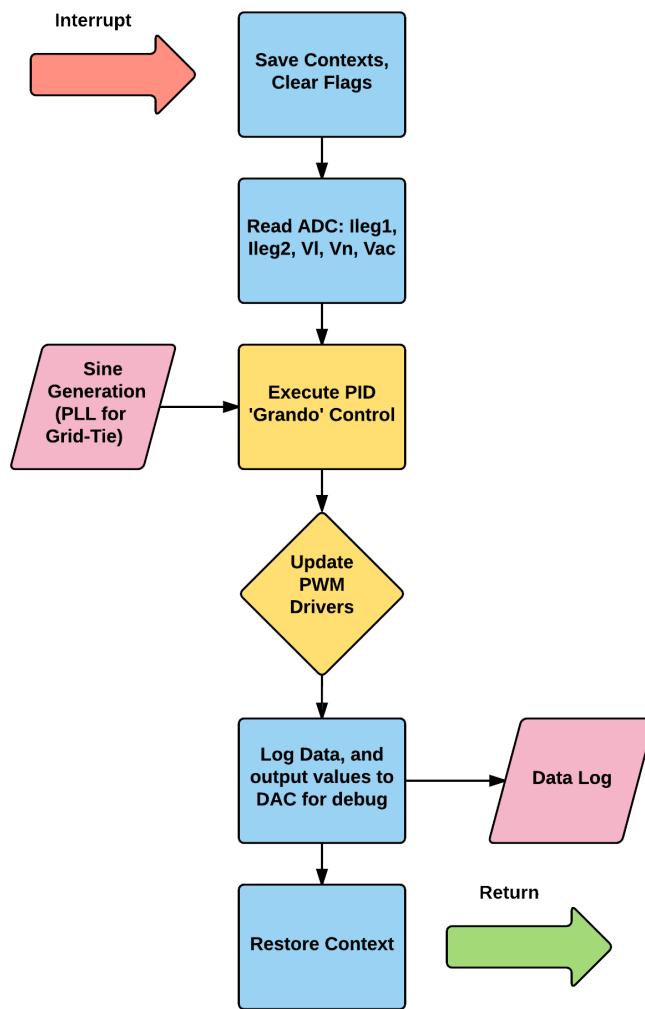


FIGURE 3.3: Software diagram of the 'slow' 20kHZ traditional PWM inverter ISR

Since the DC bus is not regulated by the boost stage feeding the inverter, the inverter itself uses nested control loops; the inner loop is for voltage control, and the outer loop employs current control. The voltage loop is used to provide a reference to the current

loop; as the inverter is loaded and current demand increases, it is natural for the voltage to sag. The current reference at any instant is used with a software PID controller to provide the duty cycle to the inverter. To prevent current distortion, the voltage loop is only updated during zero-crossing events.

A unipolar inverter operates by comparing a triangular carrier wave to a sinusoidal reference signal. The triangular carrier wave generated is not a physical signal in our system, but rather an up-down counter set for a frequency of 20kHz in the case of the inverter's PWM. Using the Texas Instruments digital power library blocks, we then generate the sinusoidal reference. During the positive half cycle, if the sinusoidal reference becomes less than the triangular wave, the output of the PWM goes low. The resulting output waveform is sparse when the phase of the sinusoidal reference is near zero or π radians, and becomes dense around $\frac{\pi}{2}$ radians. Inverse logic is true during the negative half-cycle. These comparisons are done by the PWM driver function, which is fed by the PID controllers of the inverter loop.

3.3 Hybrid Algorithm Implementation Details

In the initial stages of research and development, the hybrid inverter team first sought to recreate the simulations described in [4]. These simulations were best accomplished using the Hybrid Equations Toolbox in Matlab. Although the particulars of this implementation would be quite different than the final implementation in hardware, it was an excellent exercise in understanding the particulars of the algorithm, and also to give us a reference while implementing the hybrid controller on the C2000 micro controller in C.

3.3.1 The Matlab Implementation

The first step in building the algorithm with Matlab was to translate the flow and jump sets into Matlab code. Determining which set the solution of the RLC filter is a member is critical in determining when to switch, and when to allow the differential equation solver to flow.

These sets roughly translate as follows. Note that it can be helpful to refer to Figure 3.5 when deciphering the subsequent expressions. The flow set was translated as shown in A.1.

The translation of the jump set is shown in the following code section. The jump set signals to the framework that it is time to change states. This requires that the solver

change the set of equations that it is operating on. Determining membership of the state variable in the jump set is done by the code given in [A.2](#).

Now that we've determined whether we're in the flow set C , or the jump set D , we can perform the requisite logic for the controller. Here we give priority to jumps; this is to say, if we're in the sets C and D , give priority to the jump set and perform the necessary state transition instead of continuing to flow continuously. If we're in the jump set, this signals to the controller that we ought to execute a transition according to the jump map given in [A.3](#).

In the code, 'qplus' refers to the state that we're going to jump to, and 'pplus' refers to a change of controller. For example, if q is equal to zero, and 'qplus' is found to be one, then the next state of the H-Bridge will be to output $+V_{DC}$. Likewise, if the current controller variable p is equal to two - indicating that the global controller is in the loop - and 'pplus' is found to be one, then the forward controller will take over on the next update.

This is the bulk of the code for the Matlab simulations, though we have omitted the description of the behavior of the system as the solution flows, as this is covered in detail in [\[4\]](#).

3.3.2 The C Implementation on the C2000

We aim to briefly clarify the mechanisms behind how the hybrid inverter works, and discuss the process we undertook in implementing the hybrid algorithm on our custom hardware validation platform.

The derivation of the hybrid control algorithm is roughly as follows: given that the response of a series RLC filter can be thought of as a linear oscillator with a damping term, and given that we have a set of desired output parameters - namely the amplitude of the output voltage, the amplitude of the output current, and the angular frequency ω , then by solving the resultant linear differential equation, we can derive a reference solution for the given system to a perfect sinusoidal driving signal. In reality we will not have a sinusoidal driver, but rather some permutation of a square wave capable of switching between $+V_{dc}$, $-V_{dc}$ and 0, where V_{dc} is the DC bus voltage at the input to the H-Bridge controlled by the state variable q . We consider $q = 1$ to correspond to $+V_{dc}$, $q = -1$ to correspond to $-V_{dc}$, and $q = 0$ to correspond to 0. This process is illustrated clearly in Figure [3.5](#).

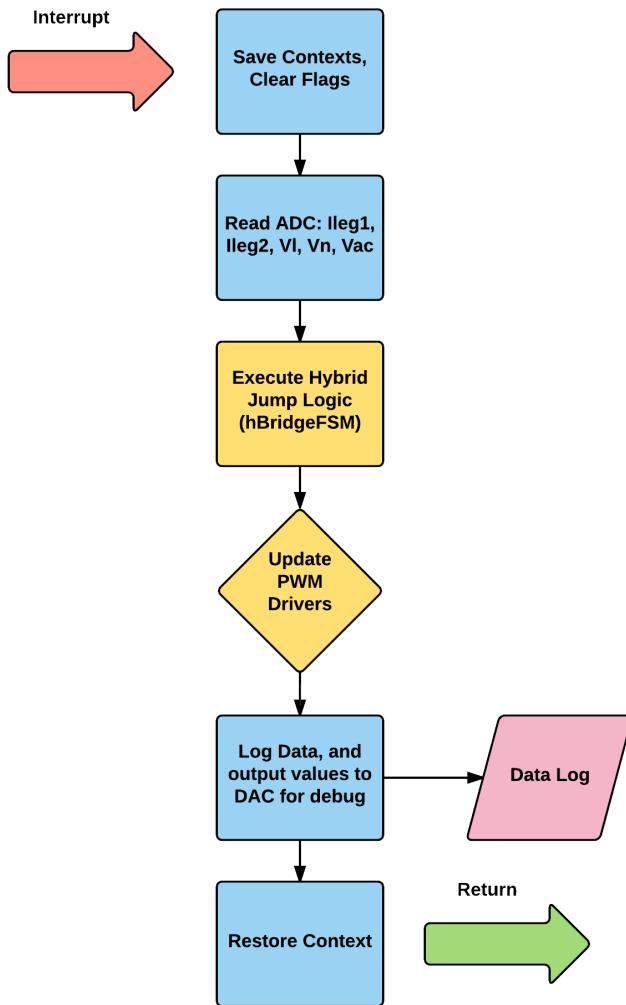


FIGURE 3.4: Software diagram of the ‘slow’ 20kHZ hybrid PWM inverter ISR

We can think of the resultant solution to the sinusoidal driver as the ideal to which our system should strive, and therefore any deviation from this ideal can be considered as an error that needs to be corrected by the controller. These errors are detected by building a tracking band around the reference solution; this is done by choosing a neighborhood around the reference solution. Collectively, this region is known as the tracking band. Now, if we consider the instantaneous state of the system to be a vector made up of the capacitor voltage and the current through the inductor, then we can measure the location of the vector in relation to the tracking band on the VI plane. Since the inductor and capacitor are at all times 90 degrees out of phase without any load or perturbation, the ideal solution takes the shape of an ellipse on the VI plane. By taking the state vector’s position relative to the tracking band, and knowing the trajectory at a given region on the VI plane, it is straightforward to develop a small set of rules

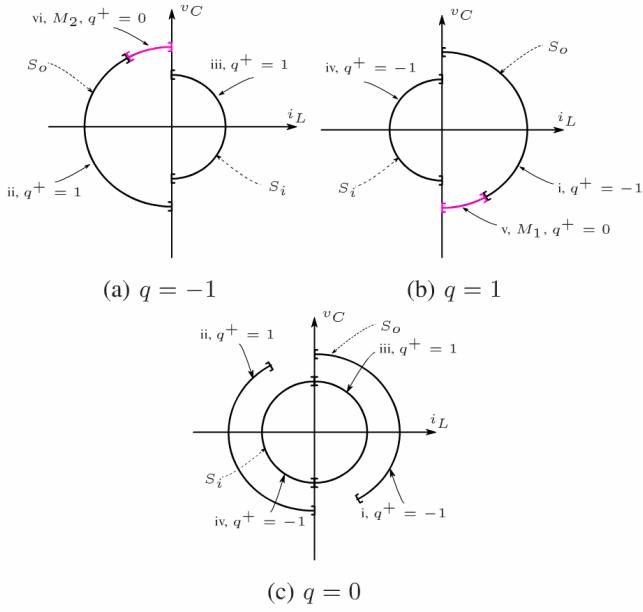


FIGURE 3.5: Jump Map of the Hybrid Algorithm [4]

governing the switching of the inverter, i.e. the jump between the three states of the H-bridge circuit, namely $q = 1$, $q = -1$, and $q = 0$. With this brief foundation, we are able to steer the state of the system around the VI plane, with the resultant output being a pseudo-sinusoid with the desired voltage and current amplitude and frequency.

With the logic for the controller worked out in Matlab, the work of porting the code to embedded C on the Texas Instruments DSP was a matter of fitting this logic within the bounds of the hardware modules onboard. In the sections above, namely Section 3.1, we discussed that the general flow of the software on the C2000 DSP is to first initialize and configure the hardware modules onboard, then to service interrupts for the boost converter and the inverter. Of chief concern in this section is the inverter ISR where we call upon a state machine that determines membership in the jump set, then informs the hardware of the appropriate action to take. The state machine is implemented using the custom state framework described above. The logic used to execute the hybrid PWM algorithm is given in Figure 3.6.

The proper operation of the controller depends on its interface with hardware; therefore, we will briefly cover the initialization of the PWM driver that we use to control the H-bridge. Adjacent PWM modules, namely PWM 1 and PWM 2, are used to operate the half-bridge modules that make up the complete H-Bridge of our inverter. Each PWM module drives two PWM signals that are configured to be duals of one another - this prevent shoot-through in the H-bridge. These two signals are designated by PMWxA or PWMxB, where x is the number of the module, and A and B represent the two PWM

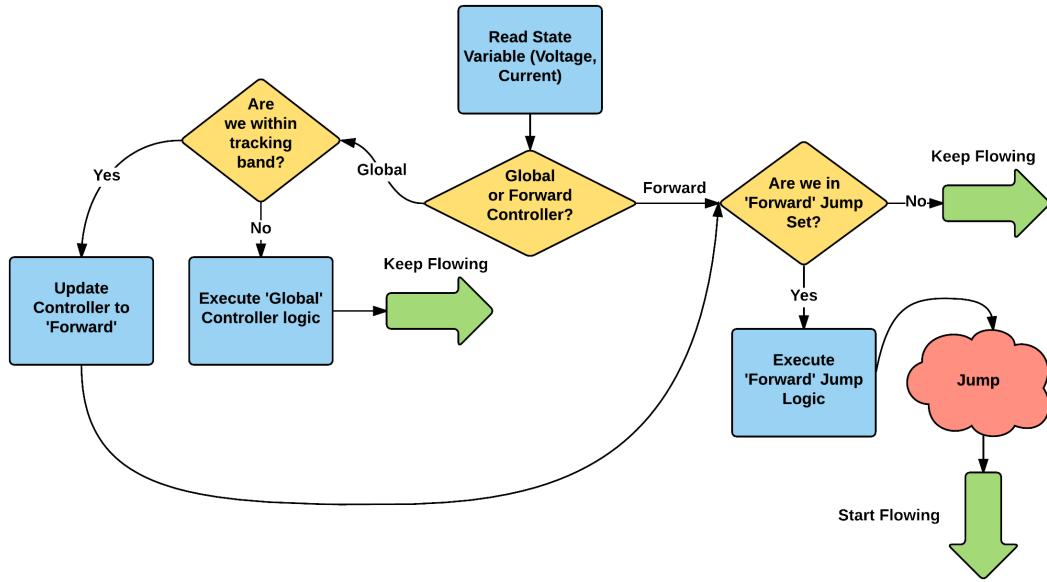


FIGURE 3.6: Flow chart of the logic involved with executing the ‘Hybrid Jump Logic’ within the hybrid PWM inverter ISR

signals of each module. In our implementation, PWMxA of each modules drives the low-side FET of each leg, while PWMxB drives the high side FET.

In our hardware setup, we configure parameters like deadband, counting mode, period and phase synchronization for the adjacent PWM modules driving our H-bridge. The driver function itself - because we are operating the PWM in hybrid mode as simple 0 or 100% duty cycle - utilizes the fact that we can set the trip of the ePWM modules to a period greater or less than the timer can ever reach. In this way, we can operate the PWM modules essentially as GPIO pins that are either logic high or logic low without reconfiguring the hardware to treat these pins as GPIO. This functionality could potentially allow for ‘hot-swapping’ between hybrid and traditional PWM operation, although we do not make use of such a functionality at this time. Secondarily, the use of PWM modules to produce 0 and 100% duty cycles allows for the use of control law accelerator (CLA) functionality in future revisions.

The PWM driver function was written as follows:

```

#define PWMDRV_Hybrid(v)
if ( v == VDC )
{
    (*ePWM[n]).CMPA.half.CMPA = TBPRD + 1;
    (*ePWM[n+1]).CMPA.half.CMPA = 0;
}
  
```

```

else if (v == ZERO_VDC){
    (*ePWM[n]).CMPA.half.CMPA = 0 ;
    (*ePWM[n+1]).CMPA.half.CMPA = 0;
}
else if (v == NEG_VDC)
{
    (*ePWM[n]).CMPA.half.CMPA = 0;
    (*ePWM[n+1]).CMPA.half.CMPA = TBPRD + 1;
}
#endif

```

As shown in code example 3.3.2, putting a zero in the CMPA register of leg 2 (n+1) means that the high side FET on leg 2 is off, and the low side FET is on. Putting TBPRD+1 in the CMPA register of leg 1 means that the low side FET is off, while the high side FET is on. The result is a current path from vdc through the load, and back down to ground (effectively $+V_{dc}$ at the load). Following an inverse logic, we can achieve $-V_{dc}$ at the load, as well as connecting the load to ground - effectively placing zero volts at the load - by driving both low side FETs.

After having properly configured the PWM modules for operation of an H-bridge, we can use the driver function to update the state of the H-Bridge with deadband for shoot-through protection. This driver function is called after the transition logic is executed, and the transition logic is executed only after the current state variable is constructed. Let's examine the update of the state variable on each iteration of the inverter ISR.

```

Vac_in = (long)((long)Vac_FB<<9)-Offset_Volt; // shift to convert to Q21
inv_ref_cur_inst = _IQ24mpy(inv_Iset, (((long) (InvSine)) << 9));

inv_meas_cur_lleg1_inst=(((long) Ileg1_fb) <<12)-_IQ24(0.5);
inv_meas_cur_lleg2_inst=(((long) Ileg2_fb) <<12)-_IQ24(0.5);

inv_meas_cur_diff_inst = (inv_meas_cur_lleg1_inst -
    inv_meas_cur_lleg2_inst)<<1;

inv_meas_vol_inst =((long)((long)Vac_FB<<12)-_IQ24(0.5))<<1; // shift to
    convert to Q24

updateState(&state, inv_ref_cur_inst, inv_meas_vol_inst, phase);

```

update
these be-
fore fi-
nal sub-
mission
to SDP

Once the state variable has been updated for the current iteration of the ISR, the state variable can be passed to the state machine operating the hybrid algorithm. This is done with the following code:

```
char HBridgeTransitionFunction(HBridge self, HBridgeEvent *e, StateVariable
    state)
{
    void    *funptr = self.super_.state__;

    il = state.current;
    vc = state.voltage;
    q = state.bridgeState;
    p = state.controller;

    /**
     * Determine which set the state variable belongs to: C or D
     */

    //Reset set membership status
    inC = false;
    inD = false;

    Vz0 = (il/ALPHA)^2 + (vc/BETA)^2;

    /**
     * Supervisory Controller
     * Determine if we need to switch controllers, depending on where the
     * state variable is
     */
    if(state.controller == GLOBAL){
        if((Vz0 >= CIN) && (Vz0 <= COUT)){      // are we between the two
            tracking bands? -> select forward controller
            state.controller = FORWARD;
            //inD = true;
        }
    }
    else if(state.controller == FORWARD){
        if((Vz0 >= COUT) || (Vz0 <= CIN)){      // are we inside both, or
            outside both tracking bands? -> select global controller
            state.controller = GLOBAL;
        }
    }
}
```

```
/** Forward Controller Check */
if(state.controller == FORWARD)
{
    if((Vz0 >= CIN) && (Vz0 <= COUT)){
        inC = true;
    }
    else{
        inC = false;
    }

}

/** Global Controller Check */
else if(state.controller == GLOBAL)
{
    if((Vz0 <= CIN) && (Vz0 >= COUT)){
        inC = true;
    }
    else{
        inC = false;
    }

}

/** 
 * D:
 * Determining Jump Set membership
 */

/** 
 * Determine if we are in 'fast-switching regions' M1 or M2 so that we
may respond accordingly
*/
M1 = ((_IQabs(Vz0-cout) < ERROR) && ((state.current >= 0) &&
(state.current <= EPSILON)) && (state.voltage <= 0)) ? true:false;
M2 = ((_IQabs(Vz0 - COUT) < ERROR) && ((state.current >= -EPSILON) &&
(state.current <= 0)) && (state.voltage >= 0)) ? true:false;

/** Forward Controller Check */
if(state.controller == FORWARD)
{
    if(q != 0){
        if( (abs(Vz0-cin) <= ERR) && (il*q <= 0)){
            inD = 1;
        }
        else if( (abs(Vz0-cout) <= ERR) && (il*q >= 0)){

```

```
        inD = 1;
    }
}

else if (q == 0){
    if( (abs(Vz0-cin) <= ERR) && (q == 0)){
        inD = 1;
    }
}
}

/** Global Controller Check */
if(state.controller == GLOBAL){
    if((Vz0 >= cin) && (Vz0 <= cout)){
        inD = 1;
    }
}

/** 
 * If we're in the jump set, determine which state transition to make
 * Else, dont waste clock cycles!
 */
if(inD){

    /**
     * For the Hfw Controller
     */
    if(p == FORWARD){
        if(q != NEG_VDC){
            if( ((abs(Vz0-cout) <= ERR) && (il >= 0) && (~M1)) ||
                ((abs(Vz0-cin) <= ERR)) && (il <= 0) ){
                qplus = NEG_VDC;
            }
        }
        else if ( ((M1) && (abs(il - EPSILON) >= ERR) && (q == 1)) ||
                    ((M2) && (abs(il + EPSILON) >= ERR) && (q == -1)) ){
                qplus = ZERO_VDC;
            }
        else if(q != VDC){
            if( ((abs(Vz0 - cout) <= ERR) && (il <= 0) && (~M2)) ||
                ((abs(Vz0 - cin) <= ERR)) && (il >= 0) ){
                qplus = VDC;
            }
        }
    }
}
```

```

        qplus = NO_EVENT;
    }
}

<**
 * For the Hg Controller
 */
else if(p == GLOBAL){
    if(Vz0 <= CIN){
        qplus = VDC;
    }
    else if(Vz0 >= COUT){
        qplus = ZERO_VDC;
    }
    else{
        qplus = NO_EVENT;
    }
}

if(pplus != NO_EVENT){
    e->super_.signal = qplus;
    state.controller = qplus;      //q = qplus
}

return qplus;
}

```

The result of the C code above is identical to that in the Matlab iteration, save for the fact that it is superfluous to know whether or not we are in the flow set because we are not using a numerical solver, but executing on hardware in real-time; therefore, it is sufficient to determine whether or not we are in the jump set. Note that in the above code segment, there is no interface to hardware, only a change in the signal of the event 'e.' After the signal member of the event structure is set, this event gets dispatched to the current state (function), which performs the state transition. The current state of the machine is echoed in hardware via the hybrid PWM driver function. Thus, we have executed the full hybrid controller in C on our DSP.

While PWM algorithms offer a relatively simple means for analyzing the switching waveform since we are modulating a carrier signal of known frequency. This is not quite the case for the hybrid algorithm where the switching occurs in response to where and when the state of the system leaves or enters the tracking band, how often we check

it, and the width of the regions M_1 and M_2 shown in Figure ???. An in-depth comparative analysis of the switching behavior of either algorithm is saved for Chapter 5.

Chapter 4

Linear Control of the Boost Converter

In order to better understand the control mechanisms at play in a typical power inverter, we undertook a course of study to learn about the state-of-the-art in DC boost control. The DC boost circuit is a highly non-linear mechanism, and much of our initial research was into the various mathematical techniques employed to develop linear models of the circuit. Amongst them are the state space averaging technique, circuit linearization via transformation, numerical methods, and small signal analysis.

In the particular case of the DC-DC boost converter circuit shown in Fig. 4.1, the design of a digital or analog controller is complicated by the non-linear nature of the system. From linear control theory, we know that positive gain and phase margins are necessary to ensure the stability of a system in the presence of disturbances. Gain margin can be understood as a safety margin for model uncertainty, while the phase margin provides a safety factor of additional phase lag or lead to ensure system stability. In order to achieve this goal while simultaneously designing for quick response, we set out to study the design of compensators for controlling this class of PWM boost converters.

Subsequent analysis will show that the transfer function for the DC-DC converter displays unstable characteristics in the presence of a RHP pole. A Bode plot of the system reveals negative gain and phase margins. In order to rectify these unstable characteristics, controllers with proportional-integral control are employed. Compensators are specialized filters designed to provide a specific gain and phase shift at a particular frequency. Because the DC boost circuit introduces a phase lag to the system, we must comprehend this in the design and implementation of our feedback loop. If we performed feedback on a lagging signal without compensation, wild oscillations would likely occur as constructive interference would never result in zero error.

The hybrid inverter team is interested in this type of control in order to reliably step up DC voltage from a small set of solar panels, and make it a viable source to the hybrid inverter whose output will be targeted at 120VRMS. Additionally, by changing the voltage reference, we will be able to implement a MPPT algorithm in order to harvest the most energy possible from the panels.

The rest of this paper is structured as follows: in the next section, we will cover the various methods of linearization for the DC boost plant model, as well as the fundamental choice between voltage and current mode operation. Next, we will cover some fundamental topics in control theory, and justify the design of our proportional-integral lag compensator.

Finally, we will discuss the steps needed to implement the compensator digitally, and cover some of the special considerations of implementation on a micro controller.

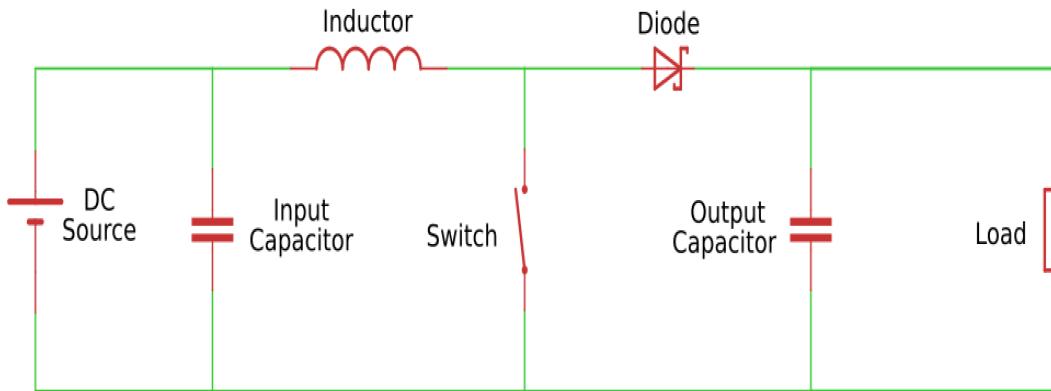


FIGURE 4.1: The Canonical DC-DC Boost Circuit

4.1 Towards a Linear Model of the DC Boost

The DC boost circuit in Fig. 4.1 has been the subject of countless dissertations dating back to the nineteen seventies. Accordingly, the landscape is a dense one. Fortunately, most researchers agree on a small signal model developed by Dr. Raymond Ridley in the nineties. Ridley's innovation was his synergistic approach, applying both numerical, sampled-data techniques with his current control model. This model employed a linear model of PWM which allowed for the simplified analysis of all SWMPS topologies. This is the model that we've used to develop our controller (see Equation 4.17). See Equation. For the sake of being thorough, we will cover some alternative methods

of analysis and circle-back to a discussion on Dr. Ridley's small signal and modeling approach.

4.1.1 Dynamic Averaging

In [16], a method for modeling the DC boost circuit with an ideal switch, an ideal transformer, and ideal current sources allows for a straightforward analysis using basic circuit analysis. After linearizing the circuit model, perturbation theory is applied to allow for the treatment of the non-linear variables as a sum of DC and AC components. For example, the function $x(t)$ would be represented as $x(t) = X + \tilde{x}$, where X is the DC components, and \tilde{x} is the AC component of the small signal representation.

The resulting linear equations for \tilde{v} and \tilde{i} , the voltage on the output loop and the current through the input loop respectively are given by:

$$\begin{aligned}\tilde{v}_{cp}(t) &= D\tilde{v}_{vp} + V_{vp}\tilde{d} \\ \tilde{i}_{vp}(t) &= D\tilde{i}_{cp} + I_{cp}\tilde{d}\end{aligned}\tag{4.1}$$

where the subscripts vp or cp indicate the voltage and current paths respectively. In Mohan's analysis, the boost circuit is split into two loops, the input loop being the current path, the output loop being modeled as the voltage path.

Finally, the transfer function resulting from this analysis is given by:

$$\frac{\tilde{v}}{\tilde{d}} = (1 - \frac{sL_e}{R}) \frac{1 + sRC}{L_eC(s^2 + s(\frac{1}{RC} + \frac{R}{L_eC}) + \frac{1}{L_eC})}\tag{4.2}$$

For a duty cycle D , effective inductance L_e , capacitance C . Note that the effective inductance goes as the inverse square of the prime duty cycle, where the prime duty cycle refers to one minus the duty.

Mohan's analysis was a useful stepping stone for understanding the basis for circuit linearization and analysis; his concise coverage of the modes of operation seen on DC boost converters, namely, the two DC steady states either off or fully on, and his explanation of discontinuous and continuous conduction regimes were invaluable.

4.1.2 State Space Averaging

Because the DC boost circuit can be viewed as occupying one of two states - off or on - we can view a linearized model of the circuit as being the average of the two states, based on the duty cycle of the PWM.

For state one where the switch is closed,

$$\begin{aligned} V_s &= V_L \\ V_s &= L \frac{di}{dt} \\ \frac{di}{dt} &= \frac{V_s}{L} \end{aligned} \tag{4.3}$$

And state two where the switch is open:

$$\begin{aligned} V_s &= V_L + V_o \\ V_s &= L \frac{di}{dt} + V_O \\ \frac{di}{dt} &= \frac{V_s}{L} - \frac{V_o}{L} \end{aligned} \tag{4.4}$$

Because the variable duty cycle gives rise to a weighted average, we define the time that the switch is closed as δT_s and the time that the switch is open as $(1 - \delta)T_s$

So the averaged equations become:

$$\begin{aligned} \dot{i}_L &= \frac{1}{T_s} [\delta T_s \frac{V_s}{L} + (1 - \delta)T_s (\frac{V_s}{L} - \frac{V_o}{L})] \\ \dot{i}_L &= \frac{V_s}{L} - \frac{(1 - \delta)v_o}{L} \end{aligned} \tag{4.5}$$

$$\begin{aligned} v_o &= \frac{-\delta T_s v_o}{RC} + (1 - \delta)T_s (\frac{i_L}{C} - \frac{v_o}{RC}) \\ \dot{v}_o &= \frac{(1 - \delta)i_L}{C} - \frac{v_o}{RC} \end{aligned} \tag{4.6}$$

With the averaged equations defined, we are free to apply the laplace transform with perturbation terms as above.

$$\begin{aligned}\delta(I_L + \hat{i}_L) &= \frac{V_s}{L} - \frac{(1-D-\tilde{d})(V_o + \hat{v}_o)}{L} \\ \delta(V_o + \hat{v}_o) &= \frac{(1-D-\tilde{d})(I_L \hat{i}_L)}{\delta t} - \frac{(V_o + \hat{v}_o)}{RC}\end{aligned}\quad (4.7)$$

After expansion and elimination:

$$\begin{aligned}\hat{i}_L &= \frac{\hat{V}_o}{L} - \frac{\hat{v}_o}{L} + \frac{D\hat{v}_o}{L} \\ \hat{v}_o &= \frac{(1-D)\hat{i}_L}{C} - \frac{\delta I_L}{C} + \frac{\hat{v}_o}{RC}\end{aligned}\quad (4.8)$$

By Laplace transform we arrive at:

$$\begin{aligned}\hat{V}_o &= sL\hat{i}_L - (1-D)\hat{v}_o \\ \hat{i}_L &= \frac{(1-D)\hat{i}_L}{C} - (sC = \frac{1}{R})\hat{v}_o\end{aligned}\quad (4.9)$$

Which leads naturally to the state space representation given below:

$$\begin{bmatrix} V_0 \\ I_L \end{bmatrix} = \begin{bmatrix} sL & (1-D) \\ (1-D) & -(sC + \frac{1}{R}) \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_o \end{bmatrix} \quad (4.10)$$

Since we want $\frac{\hat{v}_o}{\delta}$, we take the inverse of the matrix and get

$$\frac{1}{\delta} \begin{bmatrix} V_0 \\ I_L \end{bmatrix} = \begin{bmatrix} sL & (1-D) \\ (1-D) & -(sC + \frac{1}{R}) \end{bmatrix}^{-1} \begin{bmatrix} \hat{i}_L \\ \hat{v}_o \end{bmatrix} \quad (4.11)$$

with the inverse matrix given as:

$$A^{-1} = \frac{1}{tf} \begin{bmatrix} sRC + 1 & R(1-D) \\ R(1-D) & -(sC + \frac{1}{R}) \end{bmatrix} \quad (4.12)$$

Where

$$tf = s^2RLC + sL + R(1-D)^2 \quad (4.13)$$

So we have that

$$\frac{\hat{V}_o}{\delta} = \frac{V_o}{(1-D)} \left\{ \frac{-sL + R(1-D)^2}{s^2RLC + sL + R(1-D)^2} \right\} \quad (4.14)$$

Note the deviation in this result from the previous one obtained by the average dynamic model. We did not utilize this method for designing the feedback loop, but it was a useful and enlightening exercise nonetheless.

4.1.3 Numerical Methods in Matlab

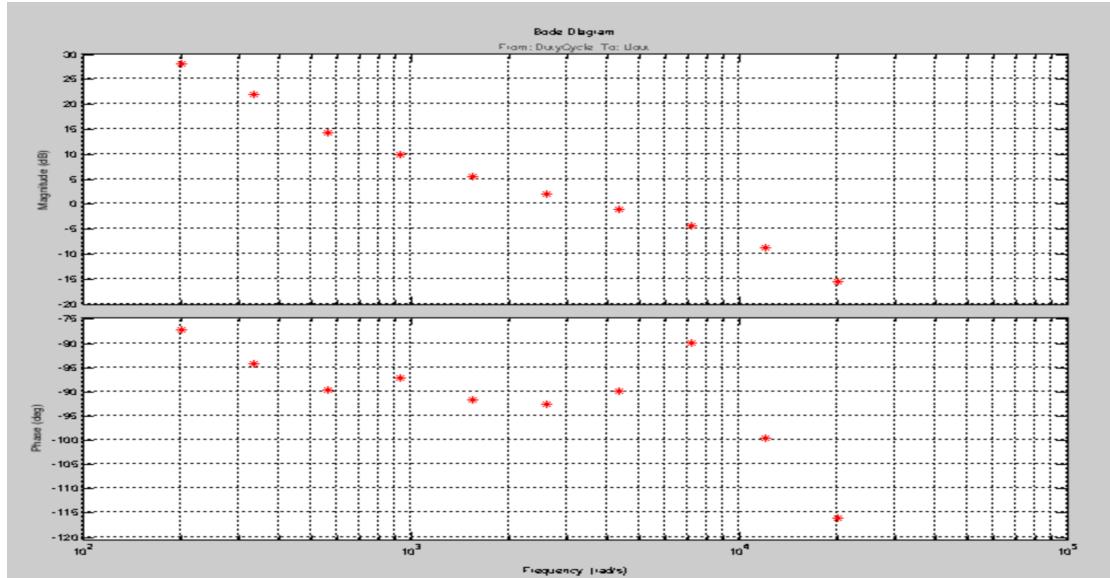


FIGURE 4.2: Sampled Data Before Estimation

One of the first methods that we used was modeling via Simulink. By utilizing an off-the-shelf inverter model, we were able to ascertain the transfer function by following the steps outlined below.

We began by opening the model below. The *mdl* variable is reused, so do not omit it.

```
mdl = 'iddemo_boost_converter';
open_system(mdl);
```

The frequency response input and output points are created using the *linio* command and for this example are the outputs of the DutyCycle and Voltage Measurement blocks.

```
ios = [...
linio([mdl,'/DutyCycle'],1,'input');...
linio([mdl,'/Voltage Measurement'],
1,'output'));
```

Use the *frest.Sinestream* command to define the sinusoids to inject at the input point. We are interested in the frequency range 200 to 20k rad/s, and want to perturb the

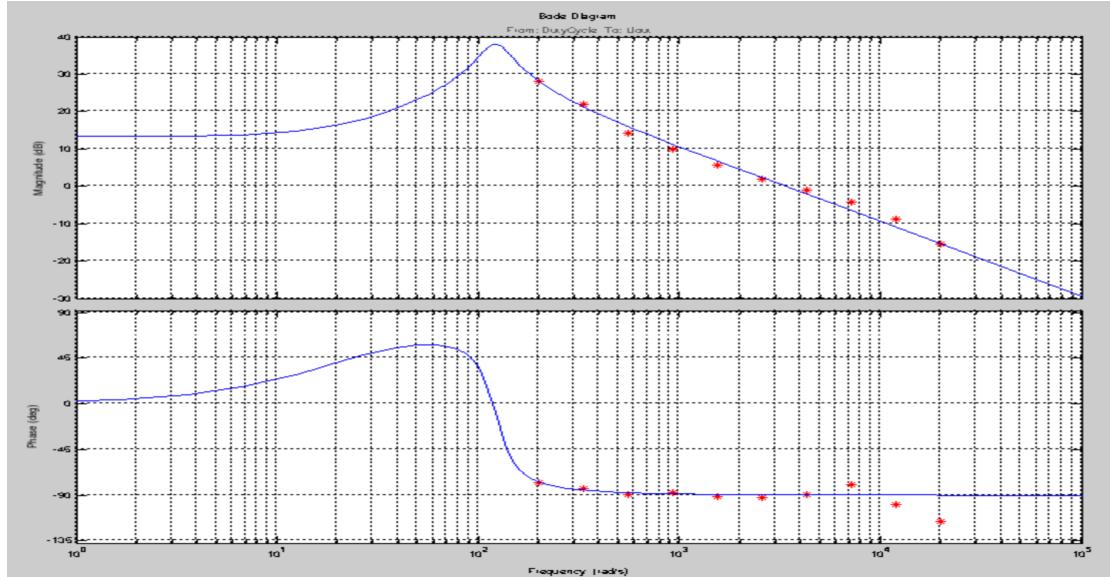


FIGURE 4.3: Sampled Data with Estimation

duty cycle by 0.03. After the following commands are entered, the Bode plot of the estimated transfer function is shown as above in Fig. 4.3. This series of commands is given as follows:

```
f = logspace(log10(200),
              log10(20000),10);
in = frest.Sinestream('Frequency',
                      f,'Amplitude',0.03);

getSimulationTime(in)/0.02

[sysData,simlog] =
    frestimate(mdl,ios,in);
bopt          = bodeoptions;
bopt.Grid      = 'on';
bopt.PhaseMatching = 'on';
figure, bode(sysData,'*r',bopt)
```

4.1.4 Small Signal Analysis

After a bit of derivation, we arrive at our final point of analysis, the small signal model proposed by Dr. Ray Ridley in his PhD dissertation circa 1990. Using a combination of the technique described above, Dr. Ridley was able to come up with a linear model of

the PWM block that could be used alongside numerical methods. The resulting Transfer function has proven to be the most accurate and reliable for designers of SWMPS. Before we jump into his methods, We'd like to touch on the two fundamental methods for controlling the DC boost circuit.

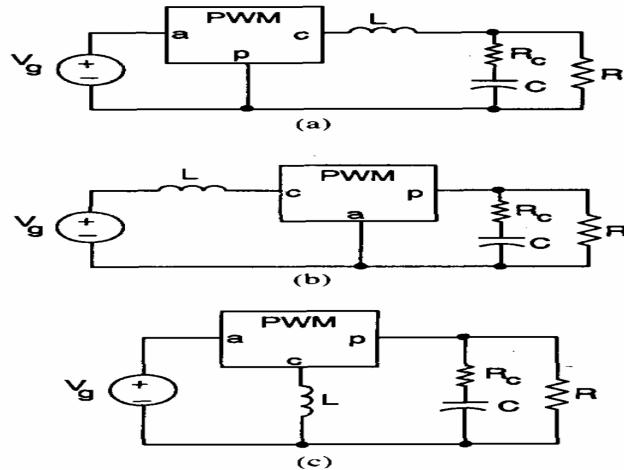


FIGURE 4.4: Linearized Model of the PWM per Ridley[5]

The first method is known as voltage mode control, and as its name implies, relies on voltage feedback from the boost circuits output to regulate itself. This technique is problematic for a few reasons. Changes in the loading condition of the circuit must be sensed as an output change first, then get corrected by the feedback loop. This delay results in slow response. Next, The output filter contributes two poles to the control loop requiring either a dominant pole for low frequency roll-off at the error amplifier, or an added zero in compensation. Lastly, compensation is complicated by the fact that the loop gain varies with the input voltage.

The preferred controller for the DC/DC boost is the so-called current mode controller; it operates by sensing current through the inductor, or through the FET switch. This method has the advantage over voltage mode control, in that as its inductor current rises with a slope determined by $(V_{in} - V_o)$, the waveform will respond immediately to line voltage changes eliminating the delayed response and gain variation with changes to the input voltage. Additionally, since the error amplifier if now used to command an output current rather than an output voltage, the effect of loading is minimized and only a single pole is contributed to the feedback loop. This allows for simpler compensation and higher bandwidth over a comparable voltage mode controller.

Dr. Ridley's model is designed with current mode control in mind. His analysis shows that the transfer function of a boost converter is found to be:

$$f_p(s) = \frac{k[1 + \frac{s}{\omega_z}][1 - \frac{s}{\omega_{z,RHP}}]}{[1 + \frac{s}{\omega_p}]} \quad (4.15)$$

Where $\omega_p = \frac{2}{RC}$, $\omega_z = \frac{1}{R_c C}$, R_c is the ESR of the cap, and $\omega_{z,RHP} = \frac{R(1-D)^2}{L}$.

The difference between the average inductor current and the dc value of the sampled inductor current can cause instability for certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. These oscillations are characteristic of boost circuits using current mode control. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. This term contributes to the total transfer function and is given by:

$$f_h(s) = \frac{1}{\frac{s^2}{w_n^2} + \frac{s}{w_n Q_p} + 1} \quad (4.16)$$

We summarize their constituent expressions here:

$$\begin{aligned} m_c &= 1 + \frac{s_e}{s_n} \\ s_e &= \frac{Vpp}{Ts} \\ s_n &= \frac{Von}{L} \\ \omega_n &= \frac{\pi}{Ts} \\ Q_p &= \frac{1}{\pi(m_c D' - 1/2)} \end{aligned}$$

Where V_{on} is the inductor voltage with the switch on, and R_i is the gain from the inductor current, implying that R_i is the sense resistor.

Therefore, the total transfer function given by Ridley in [5] is found to be:

$$f_p(s)f_h(s) = \frac{k[1 + \frac{s}{\omega_z}][1 - \frac{s}{\omega_{z,RHP}}]}{[1 + \frac{s}{\omega_p}][\frac{s^2}{w_n^2} + \frac{s}{w_n Q_p} + 1]} \quad (4.17)$$

From here, we are ready to analyze the resultant Bode plot to determine what type of compensation will be necessary for this plant model. This plot is shown below in Fig.4.5. The poles and zeros are placed in such a way that the system has enough phase

margin, and to minimize the effect of maximum phase lag due to a Right-Half plane zero.

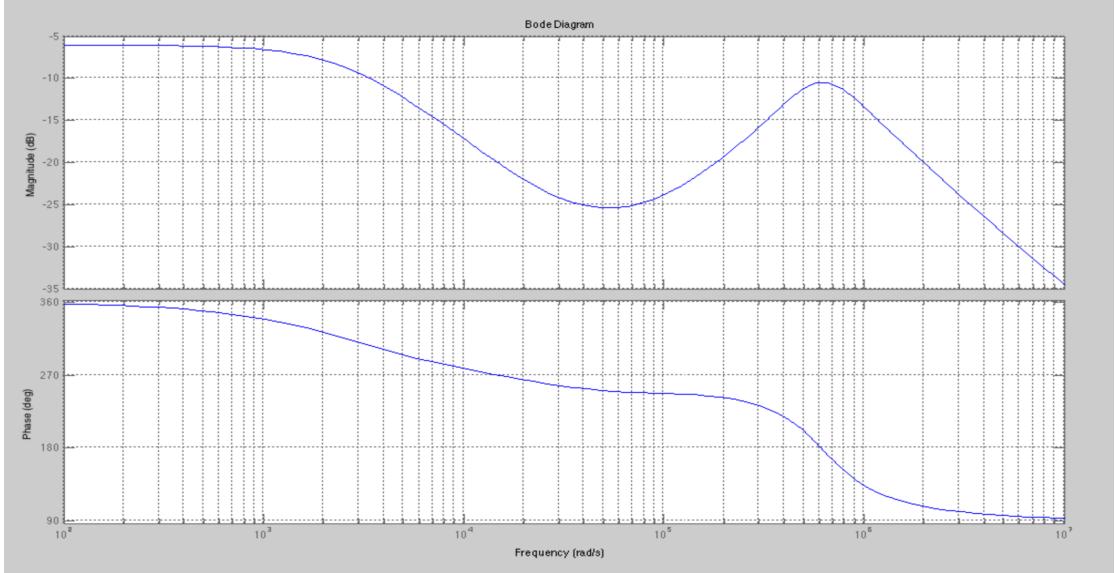


FIGURE 4.5: The total transfer function $f_p(s)f_h(s)$ for the DC boost circuit

From [16], we have that a compensator for this system in current mode control is given by

$$G_c(s) = \frac{k_c(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})} \quad (4.18)$$

Choosing our desired phase margin to be $\phi_{boost} = 60^\circ$, we have that our key parameters are:

$$\begin{aligned} k_{boost} &= \tan(45^\circ + \frac{\phi_{boost}}{2}) \\ f_z &= \frac{f_c}{k_{boost}} \\ f_p &= f_c k_{boost} \\ k_c &= \frac{\omega_z}{|G_{ps}(s)|_{f_c}} \end{aligned}$$

By selecting a reasonable crossover frequency f_c , we can calculate the required parameters of this expression. The resulting compensator is shown in Fig. 4.6. Finally, calculating the closed-loop with compensator, we get the stabilized system shown in the third panel of Fig. 4.7.

For a closer inspection, see Fig. 4.8 which clearly shows the gain and phase margins make for a stable system.

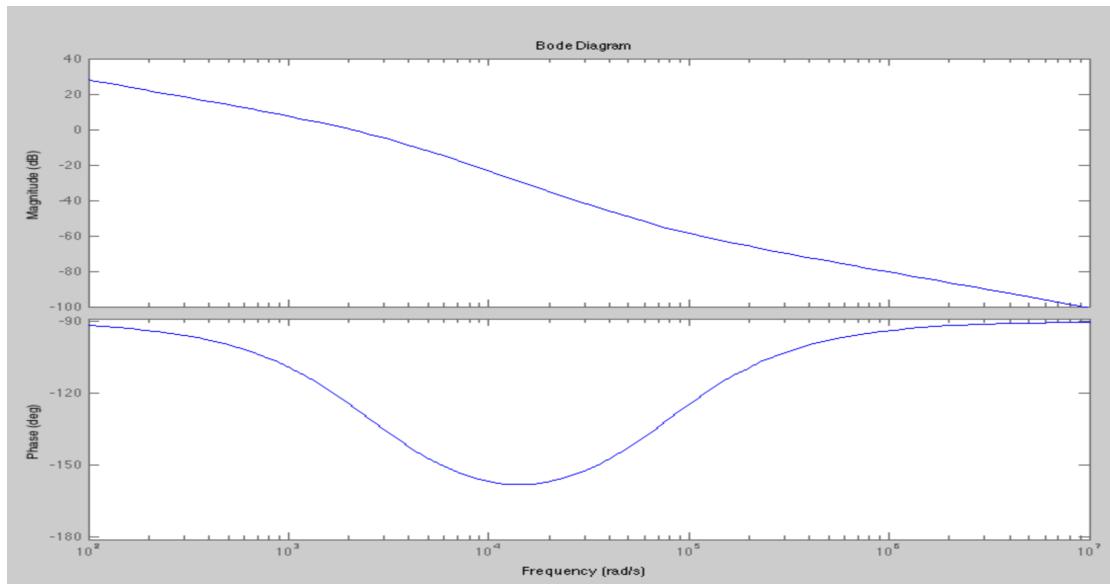


FIGURE 4.6: The lag compensator for the DC boost circuit

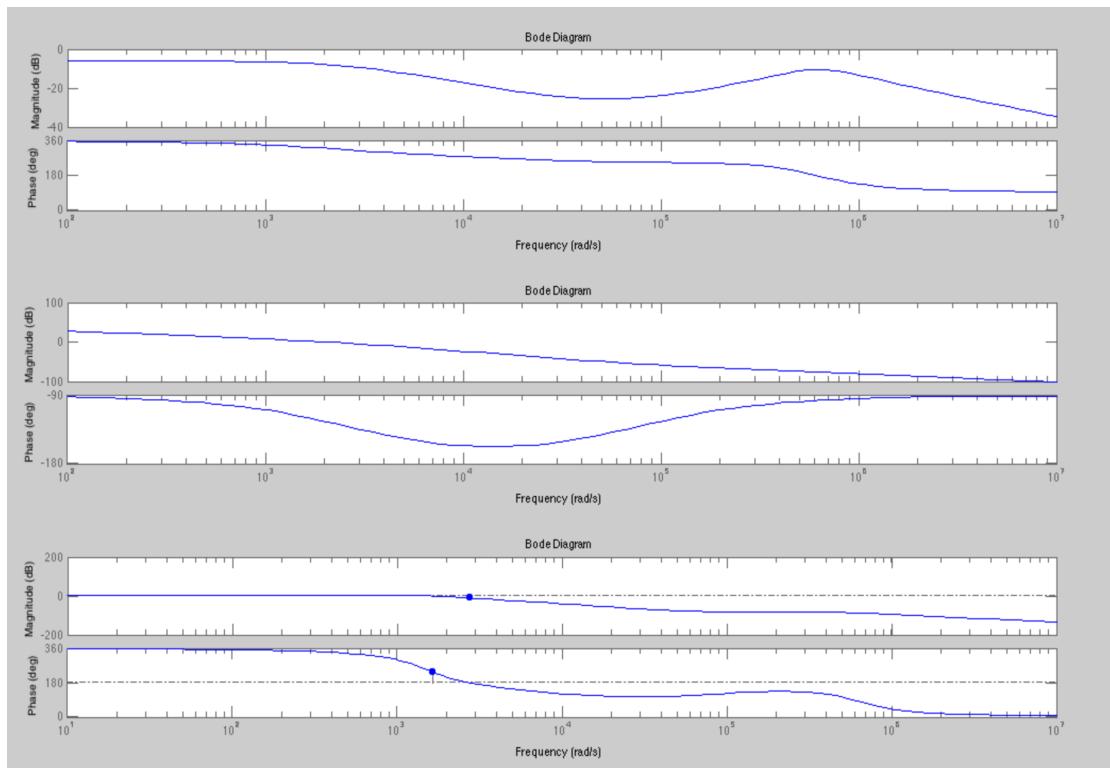


FIGURE 4.7: The Plant, Compensator, and Closed Feedback Loop Bode Plots for the DC boost circuit

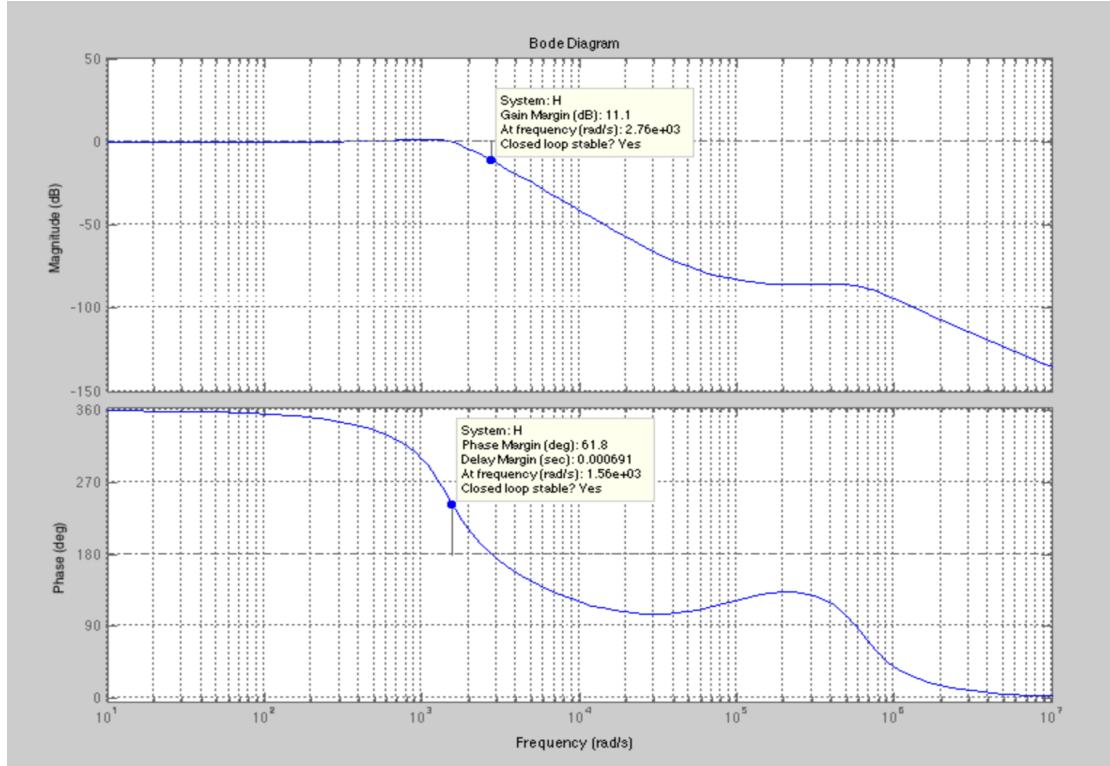


FIGURE 4.8: Bode plot of the closed loop transfer function with gain and phase margin labels

4.2 2P2Z

As we can see, the lag compensator was simply a special case of PI control. A 2P2Z can implement the continuous time version by way of a bilinear or Tustin transformation. The rule for the bilinear transform is that $s \leftarrow \frac{2z-1}{Tz+1}$. Performing this transformation on our controller equation results in an expression of the same form, implementable in assembly on a C2000 Piccolo micro controller by TI. The Biricha tool recommended by TI takes the position of poles and zeroes and converts them to the necessary coefficients for the micro.

4.3 Concluding Remarks on the Boost Controller

After a fairly exhaustive review of the literature regarding the accuracy of the linearized DC boost model, and the control theory behind their employment in SWMPS, We were able to get favorable results in simulation, namely a stable system. While there are multiple methods for linearizing the boost circuit, the most widely accepted models today utilize of Dr. Ridley's due to its highly accurate predictions. This model was

used in the design of a lag compensator. The Final phase involved the conversion of our linear model to a discrete model suitable for implementation on a micro controller.

Chapter 5

Analytical and Experimental Results

5.1 Fourier Analysis

One of the most pressing concerns regarding switching power supplies is the spectral content of the output signal, both before and after filtering. This is of chief concern to power systems designers because the demands that excess spectral content can place on filtering increase size, weight, and cost of the inverter system. These additional frequencies represent energy that must be dissipated by the filter, and hence an inefficiency in our system. A comparative analysis of the dominant PWM techniques is necessary to understand the costs and benefits of each technique, but more importantly for the purpose of this paper, to understand how the hybrid algorithm used to modulate pulse-widths stacks up. In this section we lean heavily on the work of Zhou in [6]. We contribute to this discussion by analyzing the performance of closed loop control, where Zhou strictly examines open loop PWM inverters.

Recall that any signal can be decomposed into a sum of sines and cosines given by the expression:

$$f_N(\omega t) = \frac{a_0}{2} + \sum_{n=1}^N \left(\overbrace{a_n}^{A_n \sin(\phi_n)} \cos(n\omega t) + \overbrace{b_n}^{A_n \cos(\phi_n)} \sin(n\omega t) \right) = \sum_{n=-N}^N c_n \cdot e^{in\omega t} \quad (5.1)$$

Where

$$\begin{aligned}
 a_0 &= \frac{1}{T} \int_0^T f(t) dt \\
 a_n &= \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \cdot \cos(n\omega t) dt \\
 b_n &= \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \cdot \sin(n\omega t) dt \\
 c_n &= \frac{1}{T} \int_{t_0}^{t_0+T} f(t) \cdot e^{-in\omega t} dt \\
 c_n &\stackrel{\text{def}}{=} \begin{cases} \frac{a_n}{2i} e^{i\phi_n} = \frac{1}{2}(a_n - ib_n) & \text{for } n > 0 \\ \frac{1}{2}a_0 & \text{for } n = 0 \\ c_{|n|}^* & \text{for } n < 0. \end{cases} \quad (5.2)
 \end{aligned}$$

The magnitude of every harmonic of the fundamental can be found by:

$$\begin{aligned}
 K_0 &= \frac{a_0}{2} \\
 K_n &= \sqrt{a_n^2 + b_n^2}
 \end{aligned}$$

Note that in all cases it is understood that $n \in \mathbb{Z}$.

Additionally, because direct application of the Fourier analysis can be cumbersome, the analysis of less friendly waveforms can be simplified by the application of the following properties of symmetry.

For **odd symmetry**, that is, functions satisfying the equality $f(t) = -f(-t)$ it is given that:

$$\begin{cases} a_n = 0 \\ b_n = \frac{2}{\pi} \int_0^\pi f(\omega t) \sin(n\omega t) d\omega t \end{cases} \quad (5.3)$$

For **half-wave symmetry**:

$$\begin{cases} C_n = 0 & \text{for even } n \\ a_n = \frac{2}{\pi} \int_0^\pi f(\omega t) \cos(n\omega t) d\omega t & \text{for odd } n \\ b_n = \frac{2}{\pi} \int_0^\pi f(\omega t) \sin(n\omega t) d\omega t & \text{for odd } n \end{cases} \quad (5.4)$$

This condition holds when $f(\omega t) = -f(-\omega t + \frac{T}{2})$.

And for **quarter-wave symmetry**:

$$\begin{cases} a_0 = 0 \\ a_n = 0 & \text{for even } n \\ a_n = \frac{8}{T} \int_0^{\frac{T}{4}} \cos n\omega t & \text{for odd } n \\ b_n = 0 & \text{for all } n \end{cases} \quad (5.5)$$

Quarter-wave symmetry holds for signals possessing half-wave symmetry, and also symmetry about the midpoint of the positive and negative half cycles.

5.1.1 Total Harmonic Distortion and Electromagnetic Interference

One of the most common metrics for assessing the quality of a signal is the total harmonic distortion (THD.) The THD is given by the expression:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} (V_n)^2_{rms}}}{(V_1)_{rms}} = \frac{(V)^2_{rms} - (V_1)^2_{rms}}{(V_1)_{rms}} = \frac{\sqrt{K_0^2 + K_1^2 + \dots + K_n^2}}{K_1} \cdot 100\% \quad (5.6)$$

'Where $V_{n rms}$ is the rms value of the n^{th} harmonic of $V_0(t)$, while $V_{1 rms}$ is the rms value of the fundamental frequency component.' [6] The ideal to which we strive is a zero value for THD; however, this is typically unattainable in a real-world inverter implementation. As one of the primary metrics used to assess the spectral content of a signal, we aim to minimize the THD seen at the output of an inverter. With the Fourier series, we are able to derive the expected THD analytically for

By using Fourier series, the determination of THD of a certain output is easy to obtain because magnitude of each harmonic (C_n) can be calculated.

From Maxwell's equations, we know that quickly varying electric fields cause the propagation of electromagnetic transverse waves. This phenomena is commonly referred to as electromagnetic interference (EMI). This radiated energy can couple into adjacent circuits and interfere with sensitive circuitry. Ostensibly, this noise can also couple into the inverter itself and introduce noise into analog measurements critical for operation of feedback loops. The Federal Communications Commission (FCC) has strict guidelines regarding the level of radiated energy allowable by any particular electronic device. FCC Part 15 B, concerning unintentional radiators, is the section we are most concerned with. The FCC guidelines dictate that power inverters do not generate excessive harmonic content or EMI, that inverters should be immune to other sources of EMI, and that the level of EMI generated by any inverter does not interfere with the normal operation of surrounding devices.

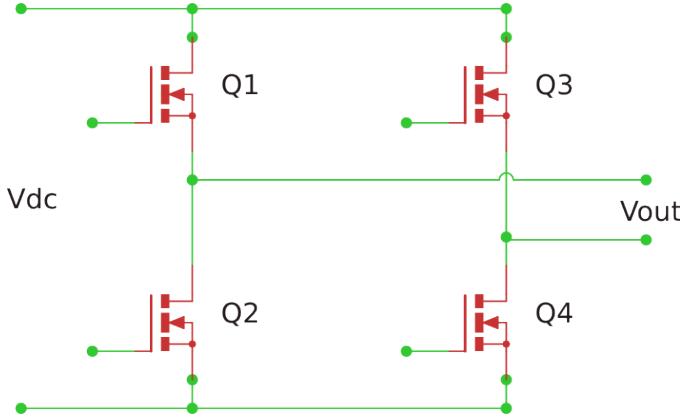


FIGURE 5.1: The H-bridge circuit showing switching-leg pairs (Q1, Q2) and (Q3, Q4), and opposing-leg pairs (Q1, Q4) and (Q2, Q3)

Although these concerns are generally beyond the scope of this research, it is still an area of critical research to evaluate where the hybrid approach stands with respect to other PWM methods for its assessment as a product in the future. Because we have no plans for grid-tie capability at this time, we omit a coverage of common mode ‘series’ filtering in this paper.

For the following subsections, we will refer to the switching pairs (Q1, Q2) and (Q3, Q4) as shown in the H-bridge in Figure 5.1.

5.1.2 Analyzing the Spectrum of Bipolar PWM

The operation of a bipolar switching scheme generally operates as follows:

$$\begin{cases} V_{out} = V_{dc} & \text{if } V_{ref} > V_c \\ V_{out} = -V_{dc} & \text{if } V_{ref} < V_c \end{cases} \quad (5.7)$$

In this inversion scheme, opposing switching pairs are modulated simultaneously. Where V_{ref} is the reference signal, and V_c is the carrier signal. In Figure 5.2 we can see that $V_{out} = V_{AO} - V_{BO}$ resulting in an output that exists only in one of the two states described in equation 5.7. If we select an odd modulation index, the output waveform exhibits odd-symmetry and we can effectively eliminate all even harmonics at the output.

In Simulink we implemented a simple bipolar inverter and performed an FFT using the powerGUI in SimPower Systems. The results are shown in Figure 5.3. The THD of this signal is found to be nearly 147%, and we note that the harmonics at the the frequency of modulation are greater than the fundamentals for this scheme.

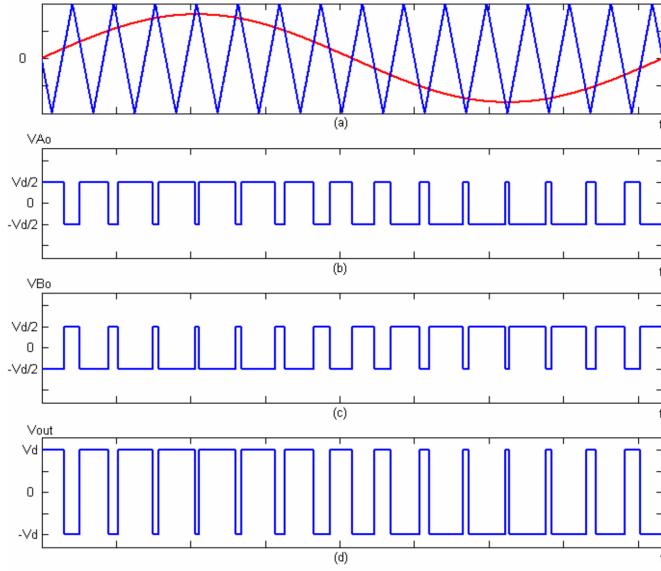


FIGURE 5.2: The operation of a bipolar switching scheme for an inverter.[6]

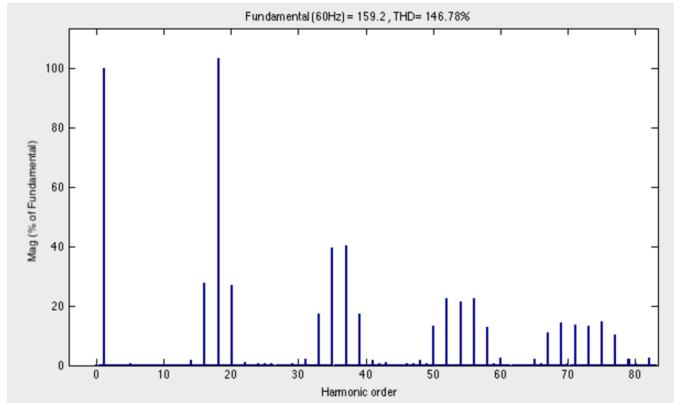


FIGURE 5.3: The spectral content of a bipolar inverter is given by FFT, with harmonics shown as multiples of the fundamental at 60Hz

Analytically, from [?], we get that the Fourier coefficients of the bipolar switching scheme are:

$$a_n = \frac{2}{\pi} \left[\int_{\theta_1}^{\theta_2} \cos(n\omega t) d\omega t + \int_{\theta_2}^{\theta_3} -\cos(n\omega t) d\omega t + \dots + \int_{\theta_{k-1}}^{\theta_k} (-1)^k \cos(n\omega t) d\omega t \right] \quad (5.8)$$

and

$$b_n = \frac{2}{\pi} \left[\int_{\theta_1}^{\theta_2} \sin(n\omega t) d\omega t + \int_{\theta_2}^{\theta_3} -\sin(n\omega t) d\omega t + \dots + \int_{\theta_{k-1}}^{\theta_k} (-1)^k \sin(n\omega t) d\omega t \right] \quad (5.9)$$

Due to time constraints, we were not able to perform analyses on a bipolar inverter in hardware; the focus of this work is on the industry standard unipolar scheme discussed

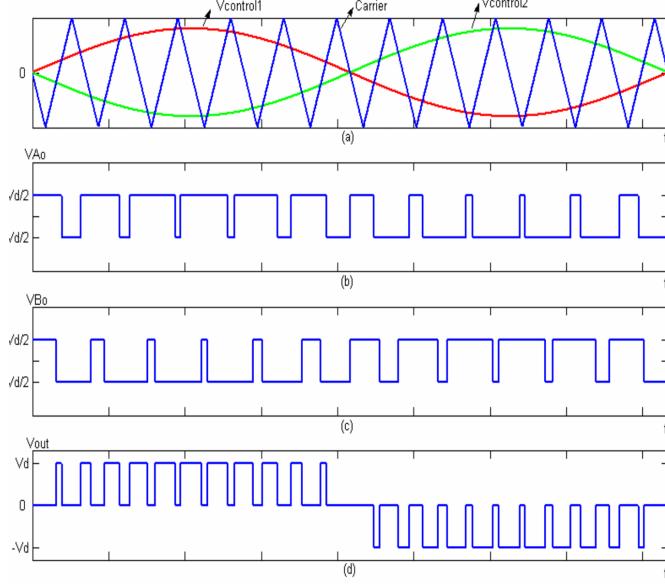


FIGURE 5.4: The operation of a unipolar switching scheme for an inverter. Note that a single control signal is used in our software implementation since each control signal is the other's dual. [6]

in the next subsection.

5.1.3 Analyzing the Spectrum of Unipolar PWM

The operation of the unipolar PWM works under the following rules, given a triangular carrier signal and a sinusoidal reference. Note that in Figure 5.10, $V_{control1}$ is the dual of $V_{control2}$, so we only require a single control signal in software.

$$\begin{cases} V_{out} = V_{dc} & \text{if } V_{ref} > V_c \\ V_{out} = -V_{dc} & \text{if } V_{ref} < V_c \\ V_{out} = 0 & \text{if } V_{ref} < V_c \end{cases} \quad (5.10)$$

From this control law, one obtains the resultant waveforms shown in Figure 5.4.

Again, using Simulink we implemented a unipolar inverter and performed an FFT using the powerGUI in SimPower Systems. The results are shown in Figure 5.5. The THD of this signal is found to be around 77%, or nearly half that of the bipolar scheme. Here, the magnitude of the fundamental is greater than any of the harmonics. These results confirm those of [6], though we found the THD of the bipolar scheme in our simulation to be much higher. Both measurements were taken before any kind of filtering stage.

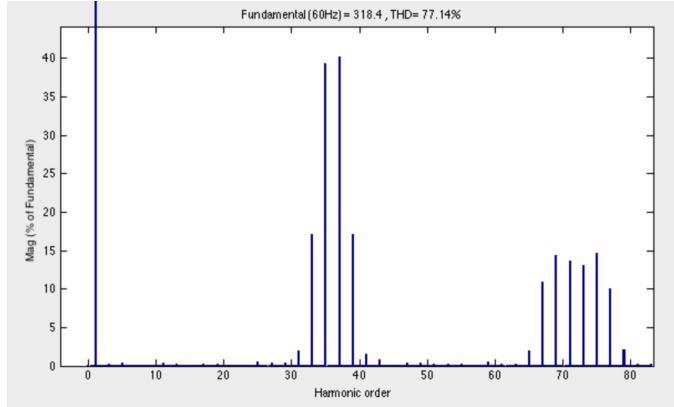


FIGURE 5.5: The spectral content of a unipolar inverter is given by FFT, with harmonics shown as multiples of the fundamental at 60Hz

As for the bipolar case, the Fourier coefficients for the unipolar case are found to be:

$$a_n = \frac{2}{\pi} \left[\int_{\theta_1}^{\theta_2} \cos(n\omega t) d\omega t + \int_{\theta_3}^{\theta_4} \cos(n\omega t) d\omega t + \dots + \int_{\theta_{2k-1}}^{\theta_{2k}} \cos(n\omega t) d\omega t \right] \quad (5.11)$$

and

$$b_n = \frac{2}{\pi} \left[\int_{\theta_1}^{\theta_2} \sin(n\omega t) d\omega t + \int_{\theta_3}^{\theta_4} -\sin(n\omega t) d\omega t + \dots + \int_{\theta_{2k-1}}^{\theta_{2k}} (-1)^k \sin(n\omega t) d\omega t \right] \quad (5.12)$$

5.1.4 Analyzing the Spectrum of the Hybrid PWM

The results obtained for the hybrid PWM are thought to be quite similar to those of the bipolar switching scheme, due to the fact that they both allow switching directly from $+V_{dc}$ to $-V_{dc}$. Therefore, it can be safely assumed that both EMI and THD in the hybrid switching case will be unfavorable in comparison to the unipolar switching scheme.

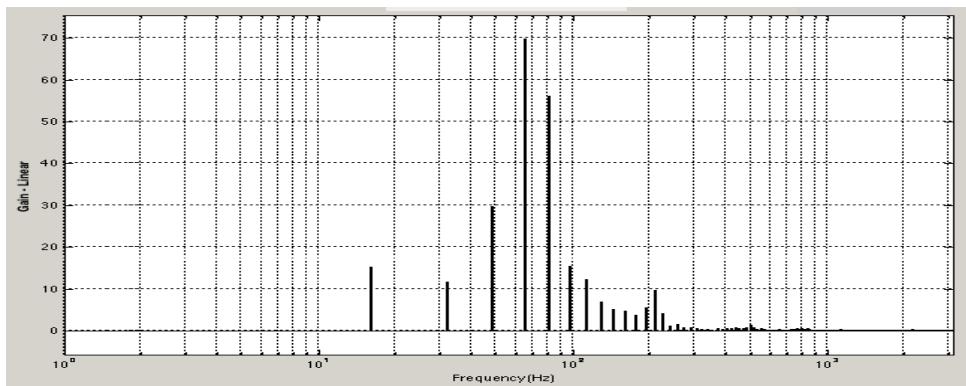


FIGURE 5.6: The spectrum of the hybrid inverter, calculated from the voltage vector generated by the hybrid simulation. The output shows significant low frequency content with harmonics bunched around the fundamental.

The spectrum shown in Figure 5.6 is rich in sub-fundamental content, with a much tighter bunching of harmonics around the fundamental as compared to other switching schemes studied thus far.

From an efficiency standpoint, it appears that the hybrid switching scheme is also at a disadvantage compared to unipolar due to the fact that the sine wave is traced out of a wave rapidly switching between $+V_{dc}$ to $-V_{dc}$ to obtain a sine wave, and hence we are ‘undoing’ some of the peak voltage seen at the output. The result is lower V_{rms} output from the bipolar switching, necessitating a higher voltage input. This voltage differential must be accounted for either by higher duty cycles of the boost converter, or more solar panels. While it would be a stretch to say that the boost converter is inefficient, the DC/DC stage is far from ideal, accounting for a large percentage of loss in inverters that utilize them.

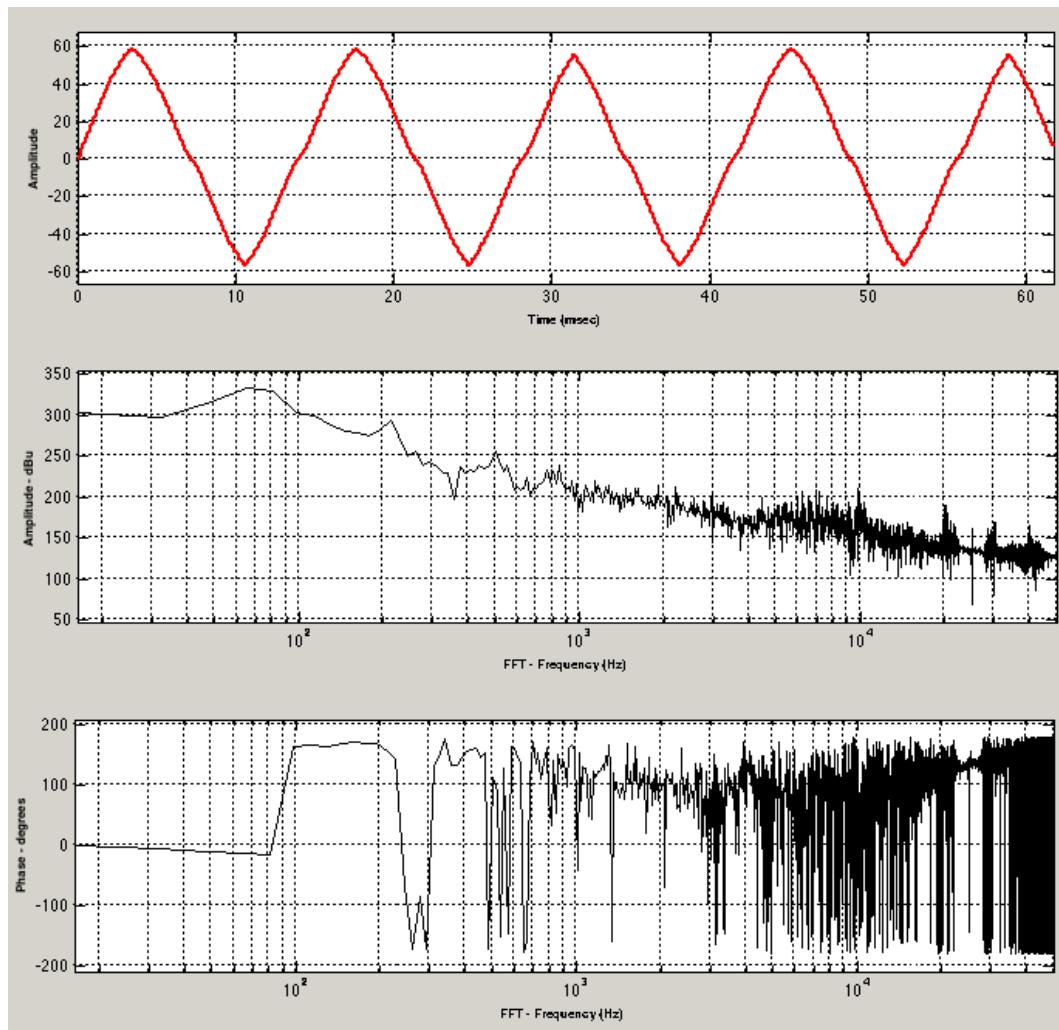


FIGURE 5.7: A plot showing voltage output of the hybrid inverter simulated in Matlab, as well as Fourier data for the magnitude (dB) and phase (degrees) respectively.

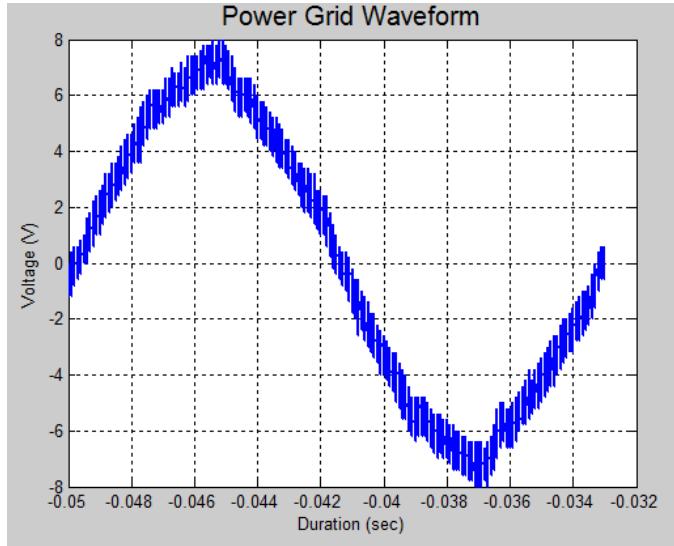


FIGURE 5.8: Power Grid Signal of the UC Santa Cruz Campus

From Figure 5.7, we see that Bode plot of the voltage FFT confirms the presence of low frequencies at the output, with approximately $100dB$ per decade roll-off past the $60Hz$ cutoff.

5.1.5 Distortion in the Power Grid

Power quality for the grid is subject to strict regulations that mandate either $60Hz$ or $50Hz$ operation depending on region. Grid-connected equipment and most consumer loads are designed for a set frequency. Deviation from these frequencies can result in serious system wide consequences including inefficiencies, interference and blackouts in the worst cases. Superimposed effects from variations in generation and loading conditions cause undesirable drift in the fundamental signal across the grid. An example of this is the spectral distortion caused by the nonlinear currents drawn by switching loads found in many consumer electronics and modern lighting ballasts. For comparison purposes, with the inverter discussed in this paper, the quality of the local power grid is analyzed. A time domain graph of a power cycle in our laboratory is shown in 5.8

The ideal waveform for Figure 5.8 is a sinusoid but aspects of distortion are observable in the irregularities of the curve. The mean frequency during the test is $60.04Hz$ with high and low values of $60.20Hz$ and $59.90Hz$ respectively. To better understand the non-ideal underlying signals causing these effects, a fast Fourier transform is taken on the grid wave to reveal its harmonic contents as shown in 5.9.

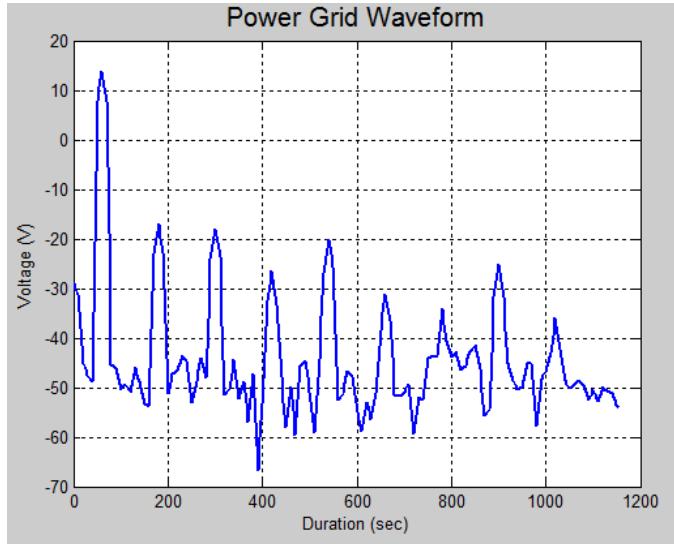


FIGURE 5.9: Fast Fourier Transform Spectrum of UC Santa Cruz's Grid

The strength of the fundamental signal is apparent in Figure 5.9 but the presence of harmonics is also seen. The odd order harmonics (180Hz, 300Hz, ect.) in Figure 5.9 dominate the spectrum while even orders tend to have lesser influence due to their canceling nature. The total harmonic distortion is calculated to be 0.4%. These potentially harmful distortions are why preventative measures such as filtering and financial penalties are used for keeping grid-tied equipment within compliance. As the diversity of the grid grows, including the spread of distributed generation through photovoltaics, we must be aware of the quality of our electricity as it is important for a reliable grid.

5.2 PWM Performance

The reality of being a two-man team has definitely caught up with our lofty research ambitions on this project: to build and control a DC/DC boost circuit at output voltages in excess of 180V; to build an inverter from the ground up and implement previously unimplemented controllers; and lastly, to characterize the THD, efficiency and robustness of the various inverter switching schemes.

If time were on our side, it would have been our wish to have implemented both bipolar and unipolar PWM in addition to hybrid PWM in order to compare their real world performance in terms of THD, efficiency, and robustness to disturbance; however, these analyses are what Masters theses are made of. With our limited time and budget, we were able to bounce back from a problematic Rev 1 board and send out a Rev 2 design in just a few days. Even still, the PCB turn times that were within our budget left

us with all of a day and a half to power up and debug our hardware before our final presentation.

In spite of the setbacks, and the impossible time-frame of a complete PCB overhaul, the Hybrid Inverter Team (HIT) is proud to present the 'HIT Power Conversion Development Board Rev. 2' to CITRIS and the Hybrid Systems Lab. With this tool, we have enabled the study of power conversion algorithms at the micro inverter scale. As an incoming graduate student to the Hybrid Systems Lab at UCSC, Ryan Rodriguez and Jun Chai plan on using this robust and extensible validation tool to perform more in-depth research on power conversion and the 'smart grid.'

Our goal was to undertake a comparative study of the three PWM techniques that have been the focus of much of this work: bipolar or unipolar PWM, and the hybrid PWM. Due to severe time constraints, we have only had the opportunity to successfully demonstrate unipolar PWM operation on our custom hardware. With the successful results given below, we are confident that full operation of the hybrid algorithm is simply a matter of debugging time that we just do not have at the moment.

In the following section we discuss how the unipolar PWM technique fairs in our real-world tests on the HIT development board. These results are obtained using the FFT functionality of a Tektronix DPO 3054 oscilloscope, and are intended to verify the results we have obtained numerically in Section 5.2.1. We also present fundamental results obtained from our outdoor test using the 170W Sharp PV module.

5.2.1 Unipolar PWM

The Hybrid Inverter Team's board is characterized while running unipolar PWM with a focus on spectral output. FFT is implemented on the AC output of the inverter during experimental testing in lab while using a high power DC supply for system input. The test's resulting frequency spectrum is shown in Figure 5.10.

Figure 5.10 depicts a fundamental signal at 60Hz which dominates above the adjacent harmonics as seen by the logarithmic scale. The total harmonic distortion of this inverter output is calculated to be 19.84% which is less than the 77.14% predicted by the SimPower System's simulation. The lower THD value is likely a consequence of our test using a low pass filter on the inverter output to reduce higher frequency distortions. These results still verify the presence of moderately significant distortion which is less than ideal in a power supply.

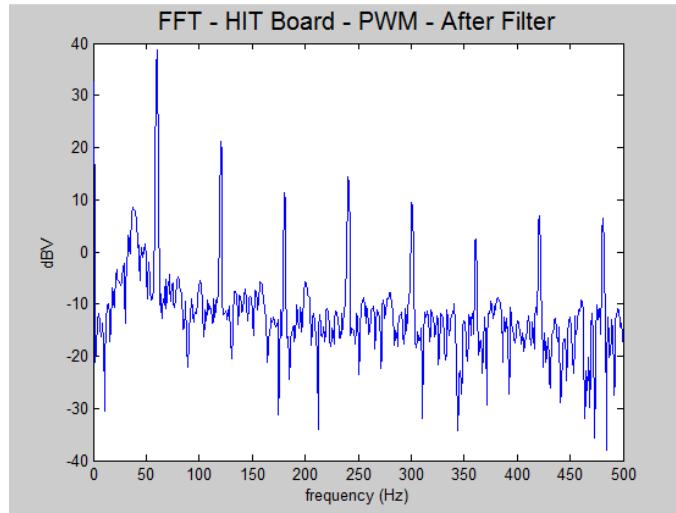


FIGURE 5.10: Frequency Spectrum of HIT Board Using Unipolar PWM

In addition to the laboratory testing, an outdoor field test is conducted with a single PV panel and the HIT board operating with unipolar PWM. The experiment environmental conditions are close to optimal with a clear sky during mid-day in June. These conditions contribute to a high solar irradiance on the solar panel and allow for close to the maximum power draw. A resistive load is varied to alter current draw from the panel while input and output power measurements are taken. With no load, the open circuit voltage for the panel is resting at 40.1V which indicates the net effects of shunt diode currents in the solar cell network. The changing resistive load causes the terminal voltage of the panel to vary as expected from the non-linear IV loading curve. A minimum load of 100Ω is placed on the 120VAC *rms* output of the inverter and a power output of 137W is achieved. Due to some suspected discrepancy in the current transformer clamp measurement tool used in the experiment, inverter board efficiency is approximately estimated to be about 80% which correlates with the testing done on



FIGURE 5.11: Scope trace of the AC output of the HIT board running unipolar PWM



FIGURE 5.12: Outdoor HIT Board Solar Test Setup

the boost converter. This indicates that upwards of 164W is sourced from the panel out of its capability of 170W. The outdoor test setup at the Baskin School of Engineering is displayed in Figure 5.12.

5.3 Conclusion

Power conversion is far and above the most difficult task that a power systems designer working in the field of renewables can undertake due to the breadth that these engineers must possess; they need to have superior circuit analysis skills, a knack for using industry standard simulations tools, and a deft way with modern programming languages and digital signal controllers. Lacking any one of the above, it is nearly impossible to innovate, or even survive, in this space. The problems found in ‘standard’ power converters are compounded in renewable energy systems where loading and sourcing conditions can fluctuate wildly throughout the course of any given day. With the demand for clean energy more dire than ever, engineers must push their understanding to squeeze every last Joule that their system can provide.

This study, motivated by the need for new and innovative conversion techniques, has sought to assess the viability of a new hybrid technique for PWM generation. We have attempted to cover many of the challenges encountered by power systems designers while planning the architecture of their power converters while addressing the most

pressing concerns: harmonic content, efficiency, robustness, and ease of implementation.

Over the course of our 20+ week senior design project, we have come to understand the pulse-width modulation techniques that drive today's power converters, namely the single-phase inverter. The contender? A new hybrid technique for generating PWM signals. The reigning champion? The unipolar PWM technique. Initial numerical results have shown that the new hybrid PWM technique is capable of producing a spectrum largely free from the low frequency content in the traditional PWM technique, it was later found that these simulations were taken from a simulation with a step disturbance at the input. Further Fourier analysis has again shown a favorable THD for hybrid control vs PWM.

Although some of the initial research into the spectral content of the hybrid inverter proved to be somewhat misleading results, further analysis has so far confirmed at least a comparably 'clean' output from hybrid as from PWM.

Although we have yet to settle the hybrid vs. PWM debate, it is clear that the Hybrid Inverter Team's development platform will enable this research to move beyond just numerical results. IN a short amount of time, we have demonstrated a development platform capable of driving standard loads at grid voltages. Future work on this system include porting the controllers to Matlab, continuing research on efficiency and THD, as well as analyzing robustness to disturbances.

Appendix A

The Matlab Implementation

A.1 Flow Set

```
%=====
%Hs Controller - Hfw in the loop
%=====

if(p == 1)      % if were between the tracking bands, flow
    if((Vz0 >= cin) && (Vz0 <= cout))
        inC = 1;
    else    % not in the tracking bands, report not-flowing
        inC = 0;
    end
%=====

%Hs Controller - Hg in the loop
%=====

else
    if(Vz0 >= cout)          %if were beyond Co
        inC = 1;
    elseif(Vz0 <= cin);      %if were within Ci
        inC = 1;
    else
        inC = 0;
    end
end
```

```
%=====
%For the Hfw Controller
%=====

if(p == 1)
    if((Vz0 >= cin) && (Vz0 <= cout))
        inC = 1;
    else
        inC = 0;
    end
else
    inC = 0;
end

%=====
%For the Hg Controller
%=====

if(p == 2)
    if((Vz0 <= cin) || (Vz0 >= cout))
        inC = 1;
    else
        inC = 0;
    end
else
    inC = 0;
end
```

A.2 Jump Set

```
%=====
%Determine if Solution is in M1 or M2
%=====

mEpsilon = .5; %dependant on the current and voltage targets
if ((abs(Vz0 - cout) < err) && ((il >= 0) && (il <= mEpsilon)) && (vc
<= 0))
    M1 = 1;
else
```

```

M1 = 0;
end
if ((abs(Vz0 - cout) < err) && ((il >= -mEpsilon) && (il <= 0)) &&
(vc >= 0))
    M2 = 1;
else
    M2 = 0;
end

%=====
%For the Hs Controller
%=====

%p == 1 -> Hfw in the loop
%p == 2 -> Hg in the loop

if(p == 2)
    if((Vz0 >= cin) && (Vz0 <= cout))
        inD = 1;
    end
else
    inD = 0;
end

%=====
%For the Hfw Controller
%=====

if(p == 1)
    if(q == 0)
        if( (abs(Vz0-cin) <= err) && (il*q <= 0))
            inD = 1;
        elseif( (abs(Vz0-cout) <= err) && (il*q >= 0))
            inD = 1;
        end
    elseif (q == 0)
        if( (abs(Vz0-cin) <= err) && (q == 0))
            inD = 1;
        end
    end
end

```

```

end

%=====
%For the Hg Controller
%=====

if(p == 2)
    if((Vz0 >= cin) && (Vz0 <= cout))
        inD = 1;
    else
        inD = 0;
    end
end

```

A.3 Jump Map

```

%=====
%For the Hs Controller
%=====

if(p == 2)
    if((Vz0 >= cin) && (Vz0 <= cout))
        pplus = 1;
    end
else
    pplus = p;
end

%=====
%For the Hfw Controller
%=====

if(p == 1)
    if(q == -1)
        if( ((abs(Vz0-cout) <= err) && (il >= 0) && (~M1)) ||
            ((abs(Vz0-cin) <= err) && (il <= 0)) )
            qplus = -1;
        end
    elseif ( ((M1) && (abs(il - mEpsilon) >= err) && (q == 1)) ||
              ((M2) && (abs(il + mEpsilon) >= err) && (q == -1)) )

```

```
qplus = 0;
elseif(q ~= 1)
    if( ((abs(Vz0 - cout) <= err) && (il <= 0) && (~M2)) ||
((abs(Vz0 - cin) <= err)) && (il >= 0)) )
        qplus = 1;
    end
else
    qplus = q;
end
end

%=====
%For the Hg Controller
%=====

if(p == 2)
    if((Vz0 >= cin) && (Vz0 < cout))
        pplus = 1;
    else
        pplus = p;
    end
end
```

Appendix B

Circuits

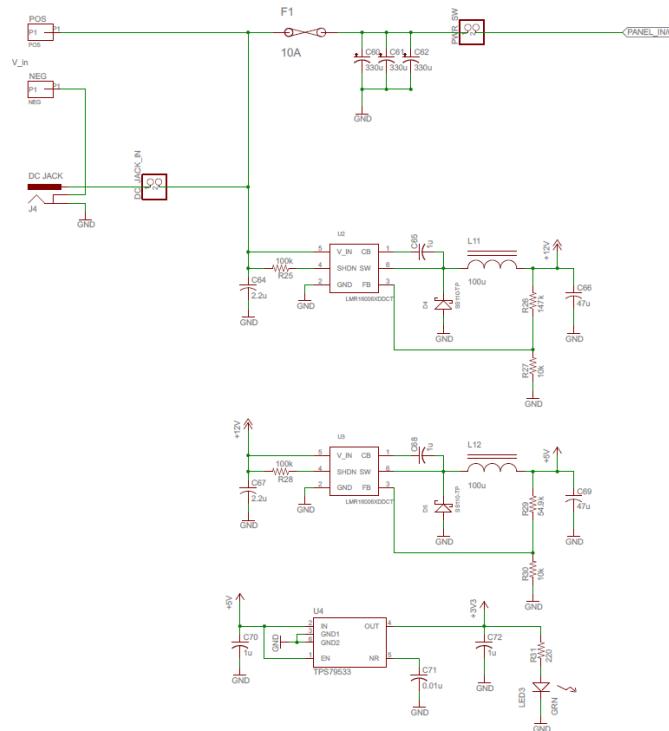


FIGURE B.1: Logic Power Supply Circuit

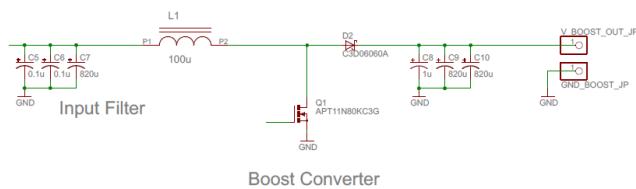
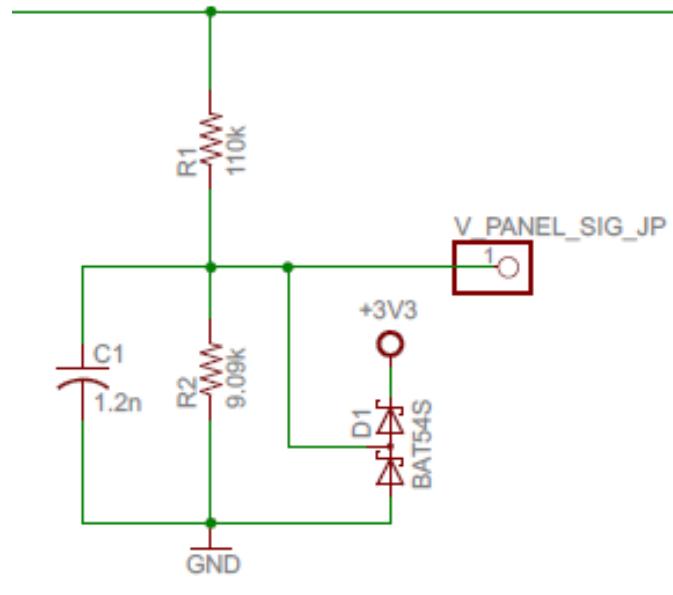
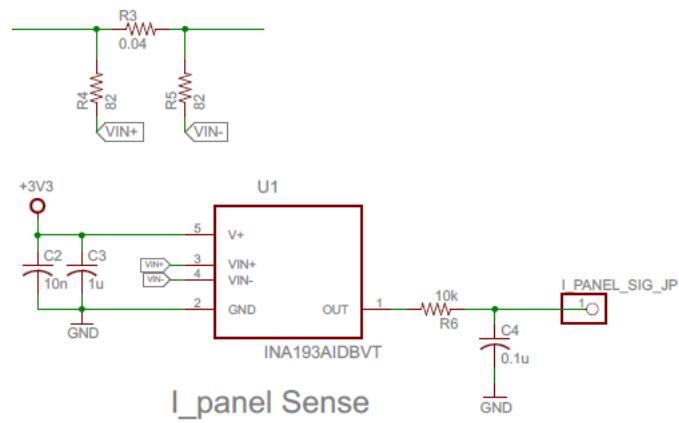


FIGURE B.2: Boost Converter Circuit



V_panel Sense

FIGURE B.3: PV Voltage Sense Circuit



I_panel Sense

FIGURE B.4: PV Current Sense Circuit

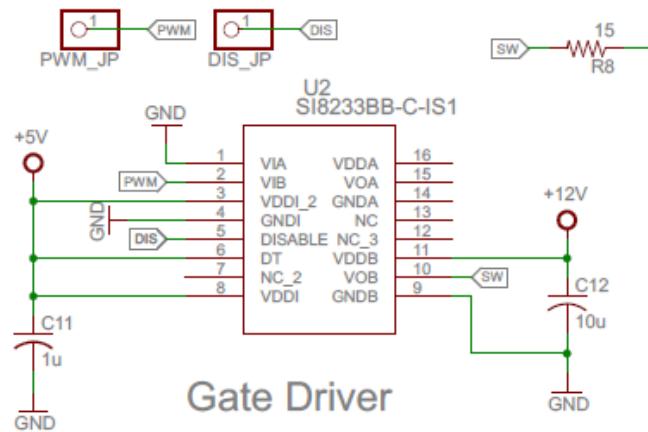


FIGURE B.5: Gate Driver Circuit

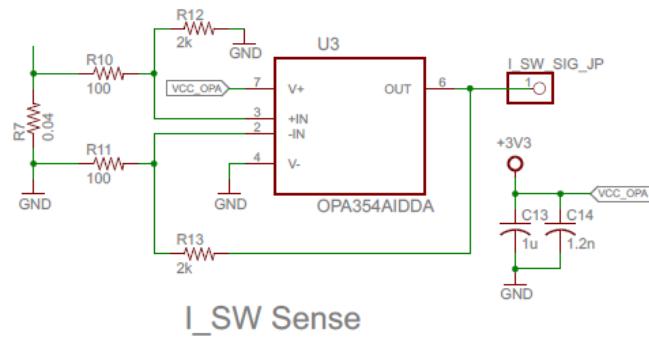


FIGURE B.6: Switch Current Sense Circuit

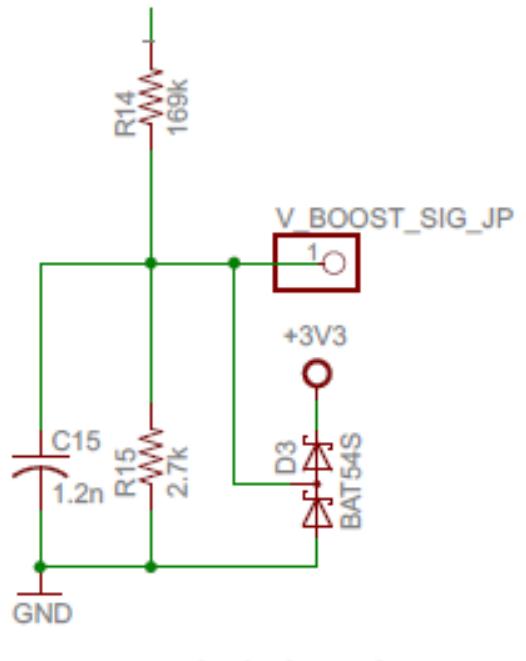


FIGURE B.7: Boosted Voltage Sense Circuit

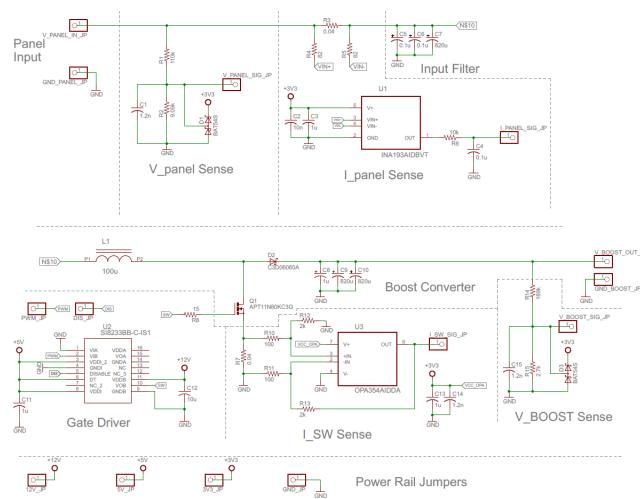


FIGURE B.8: Boost Converter Schematic

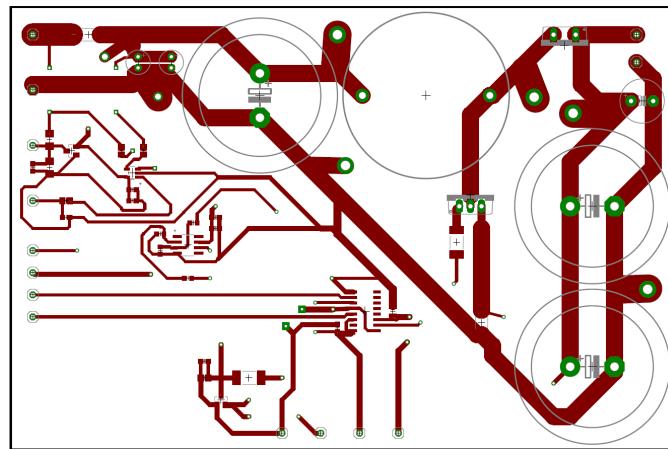


FIGURE B.9: Boost Board PCB Top

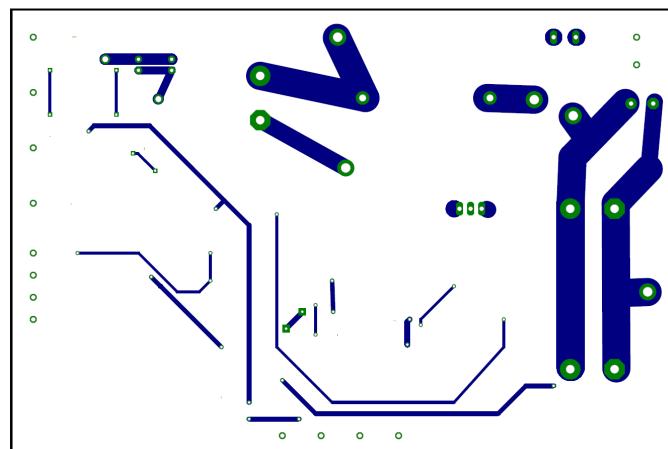


FIGURE B.10: Boost Board PCB Bottom

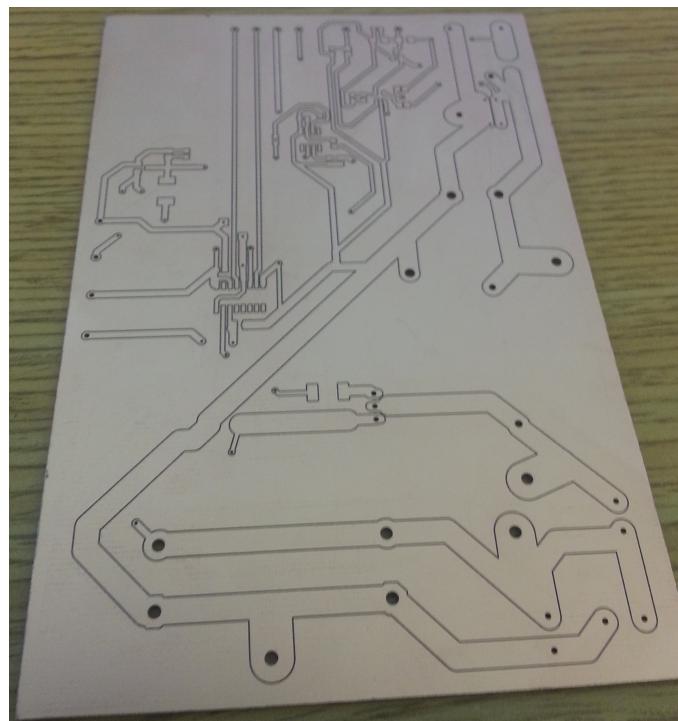


FIGURE B.11: Board Board PCB

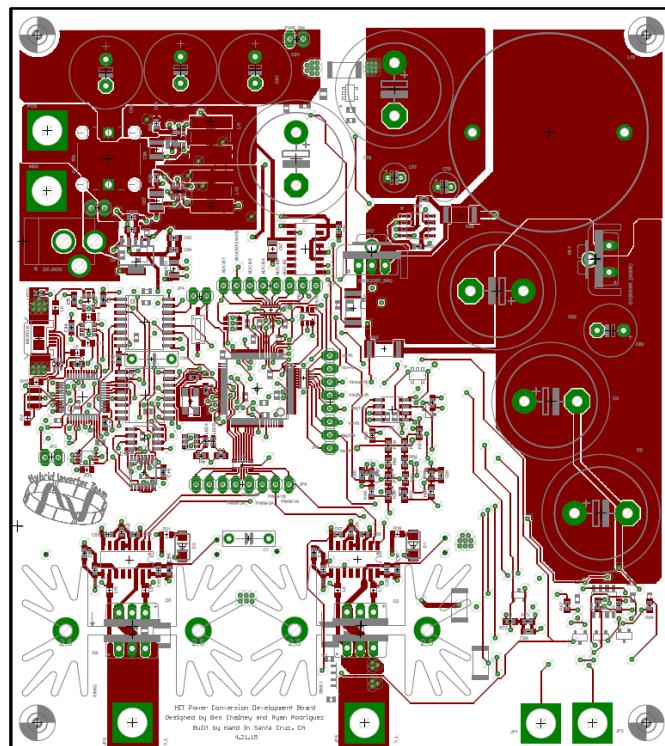


FIGURE B.12: Hit Board Rev 1, Top

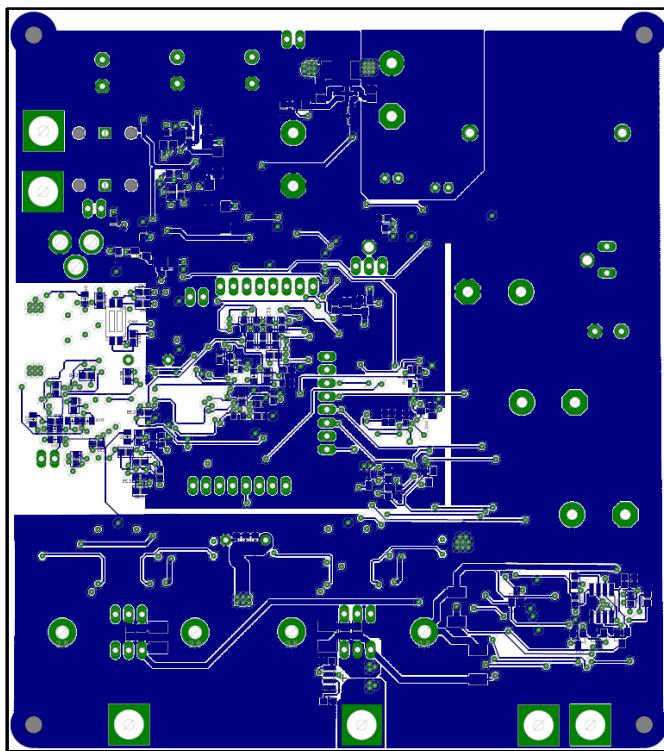


FIGURE B.13: Hit Board Rev 1, Bottom

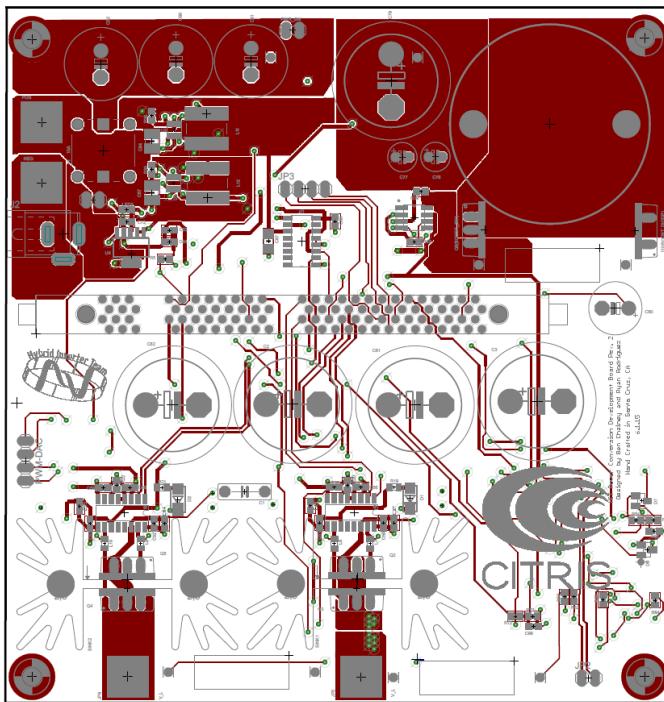


FIGURE B.14: HIT Board Gen.2 Layout Top

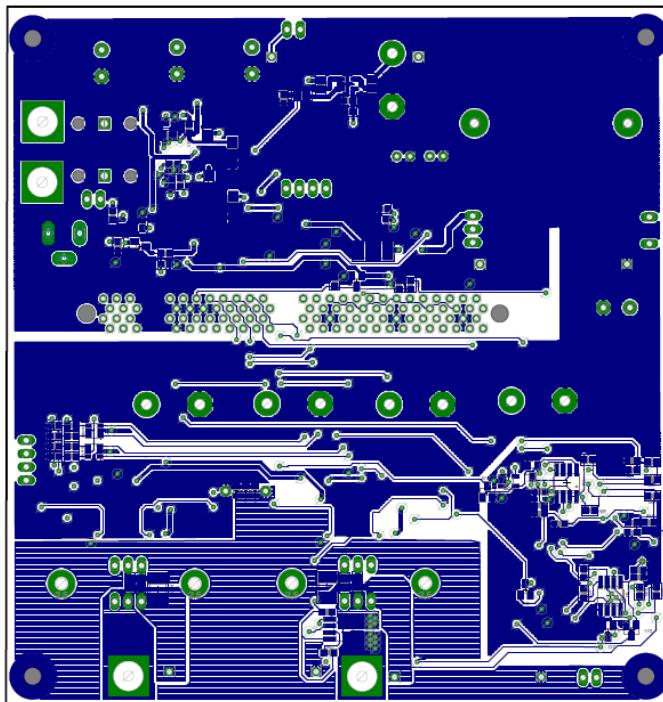


FIGURE B.15: HIT Board Gen.2 Layout Bottom

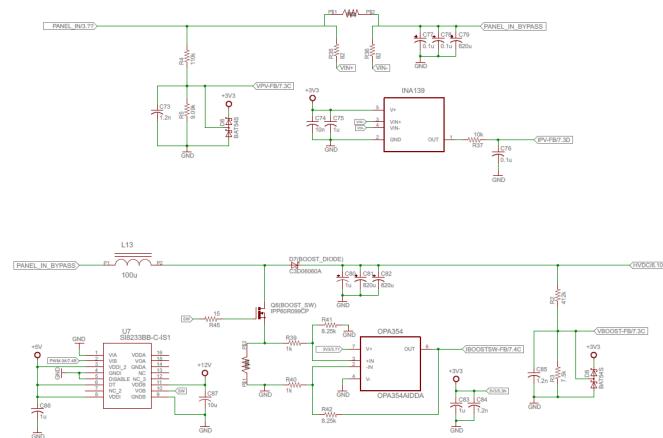


FIGURE B.16: HIT Board Rev.2 Boost Schematic

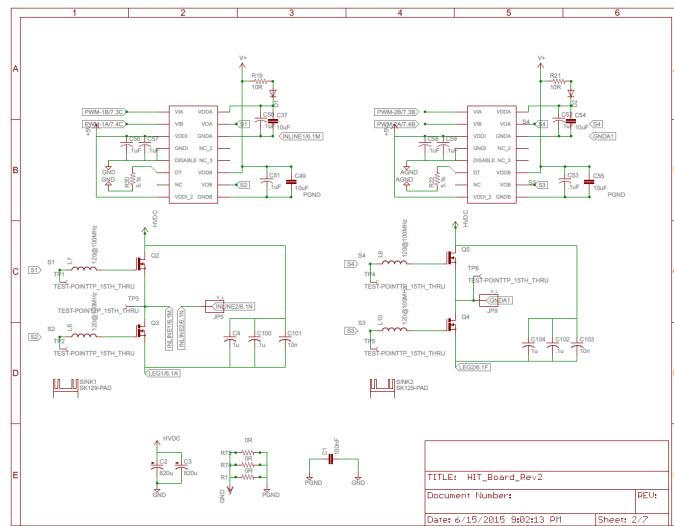


FIGURE B.17: HIT Board Rev.2 H-Bridge Schematic

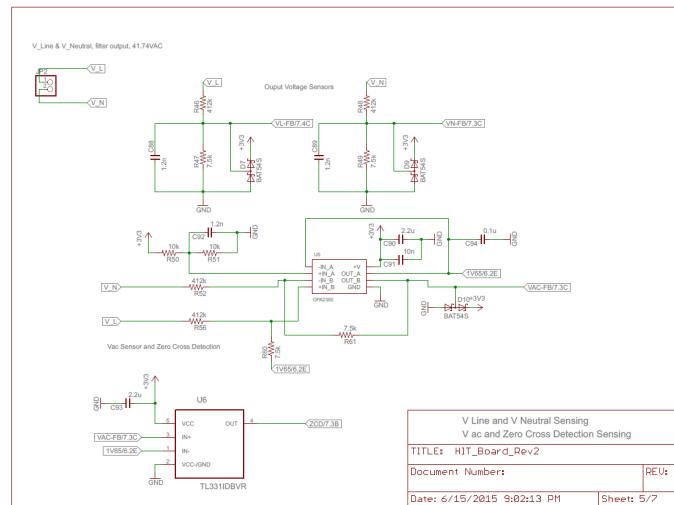


FIGURE B.18: HIT Board Rev.2 Output Sensors 1 Schematic

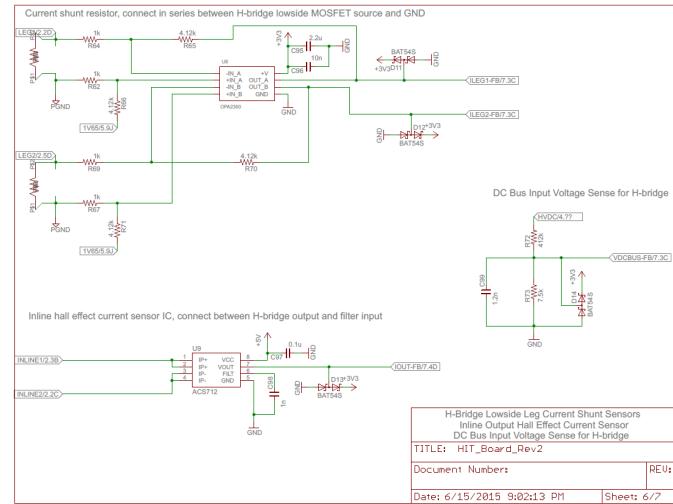


FIGURE B.19: HIT Board Rev.2 Output Sensors 2 Schematic

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