EE 463

Hardware Project - Complete Simulation Report

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Contents

1 Introduction

The objective of this project is to design, simulate, build, and test a DC motor driver that converts AC power into an adjustable DC output up to 180 V and is able to run a DC motor starting from standstill. Through this project, the aim is to learn how to choose a suitable power circuit topology, perform basic calculations and simulations, select proper real-life components, and safely implement and test a working hardware system.

This report includes the selection process of a suitable power converter topology and components for a DC motor driver system, analytical calculations and simulation results.

2 System Specifications

This section outlines the electrical specifications and performance requirements for the DC motor drive system designed in this project. The system is designed to convert a three-phase AC grid voltage into a controlled DC output to drive a separately excited DC motor under varying load conditions.

2.1 Input Specifications

- **Source:** Three-phase AC grid
- **Voltage:** 380 V_{LL} (line-to-line)
- **Frequency:** 50 Hz
- **Input Protection:** Safety fuses are implemented on the input side to protect the rectifier stage and the grid connection against short-circuit currents or excessive inrush.

2.2 Output Specifications

- **Output Voltage:** Adjustable DC voltage ranging from 0 V to 180 V.
- **Output Power:** The system is rated for a continuous output power of 1.6 kW.
- **Output Protection:** Safety fuses are implemented on the output side to protect the DC Motor.

2.3 Load Specifications

The drive is specifically tuned to operate the following motor–generator set:

- **Motor Type:** Separately excited DC motor.
- **Coupling:** Mechanically coupled to a separately excited AC generator.
- **Armature Winding Parameters:**
  - Resistance $R_a = 0.8\ \Omega$
  - Inductance $L_a = 12.5$ mH

- **Shunt Winding Parameters:**
  - Resistance $R_a = 210\ \Omega$
  - Inductance $L_a = 23$ H
- **Interpoles Winding Parameters:**
  - Resistance $R_a = 0.27\ \Omega$
  - Inductance $L_a = 12$ mH
- **Load Characteristic:** The system is tested with a 1.6 kW resistive load connected to the output of the coupled AC generator, simulating the mechanical torque load on the DC motor.

2.4 Performance Requirements

The design stick to the following performance criteria:

- **Switching Frequency ($f_{\mathbf{sw}}$):** Selected to be smaller than 100 kHz in order to balance switching losses and passive component sizing.
- **Current Ripple Target (ΔI_L):** Designed to be smaller than 30% of the rated average current. This minimizes torque ripple and reduces heating in the motor windings.
- **Voltage Ripple Target ($\Delta V_{\mathbf{out}}$):** Designed to be smaller than 5% of the output voltage to ensure a stable DC voltage applied to the armature.

3 Topology Selection & Design Decisions

3.1 Selected Topology

The selected topology consists of a three-phase rectifier followed by a DC–DC buck converter.

A three-phase input is chosen because it provides a better quality DC voltage and can handle higher power levels. In a single-phase full-wave rectifier, the ripple frequency is 100 Hz, while in a three-phase rectifier it is 300 Hz. This higher ripple frequency is easier to filter, which allows the use of smaller and cheaper DC capacitors. Also, three-phase rectification produces a higher average DC voltage for the same line voltage, giving enough margin for the buck converter to regulate the output down to 180 V. In addition, the load is shared between three phases, which means the input current is more balanced and this is better for motor drive applications.

The buck converter is selected because it is highly efficient and well suited for step-down voltage applications. Since the DC voltage after the rectifier is much higher than the required motor voltage (180 V), a step-down converter is necessary. The buck converter has a simple and nearly linear control characteristic, where the output voltage is directly proportional to the duty cycle. This makes its control simple and reliable.

3.2 Theoretical Analysis

3.2.1 Rectifier Stage

For a three-phase rectifier, the average DC link voltage is approximated by

$$V_{\mathrm{dc}} = 1.35\, V_{\mathrm{LL}}, \tag{1}$$

where V_{LL} is the line-to-line RMS grid voltage. This DC-link voltage is sufficiently higher than 180 V, which provides sufficient margin for regulation via the buck converter.

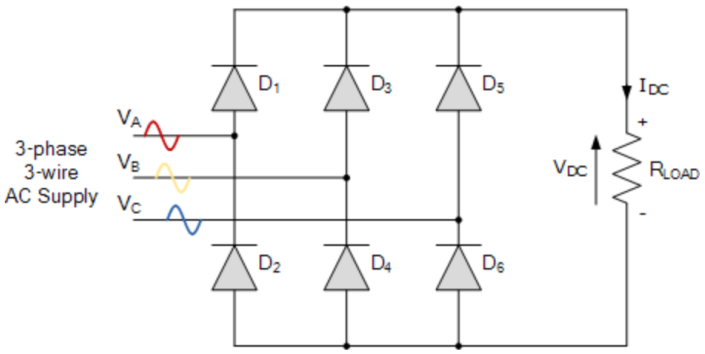

Figure 1: Three Phase Rectifier Topology.

3.2.2 Buck Stage

For an ideal buck converter, the duty cycle needed to obtain the desired output voltage is given by

$$D = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}, \tag{2}$$

where V_{in} is the rectified DC-link voltage and V_{out} is the desired output (up to 180 V). This relation is used in the design and verification of the control loop.

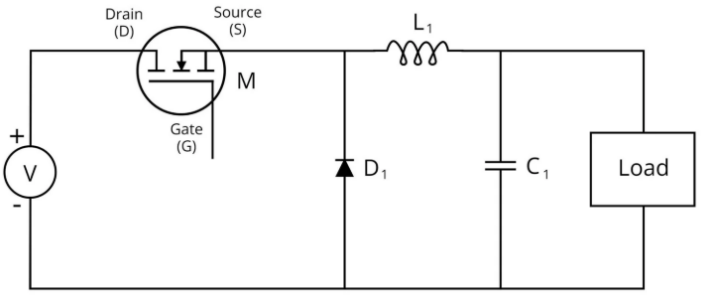

Figure 2: Buck Converter Topology.

3.3 Control Method Decision

In DC motor drives, the output voltage must stay stable even when conditions change. With open-loop control, the duty cycle D is fixed, so it assumes that the input voltage

and load are constant. In reality, the rectified 3-phase grid voltage has ripple, and the motor load changes with mechanical torque, causing the output voltage to vary and the armature current to rise, which can damage the motor. For this reason, a closed-loop system is required: it measures the output voltage, compares it with the reference, and adjusts the duty cycle in real time to keep the voltage regulated under changing input and load conditions.

For the buck converter stage, two main control methods are considered: voltage mode control (VMC) and current mode control (CMC).

Voltage Mode Control (VMC) In VMC, a single feedback loop compares the output voltage with a reference. The error signal is processed by a compensator and then converted to a PWM duty cycle.

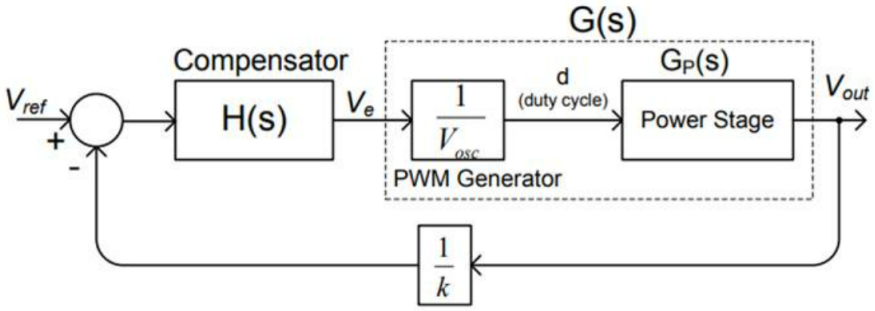

Figure 3: Block diagram for voltage mode control.

This method is simple, but it has important disadvantages in this application:

- The LC filter of the buck converter makes the system behave like a second-order system. This complicates the compensator design and limits how fast the loop can respond.
- The controller only measures the output voltage. Changes in the input voltage or load are seen indirectly and relatively slowly, which leads to a slower dynamic response.
- The switch current is not directly monitored, so there is no inherent cycle-by-cycle over-current protection. This is risky for a DC motor drive, especially during start-up or stall conditions.

Current Mode Control (CMC)

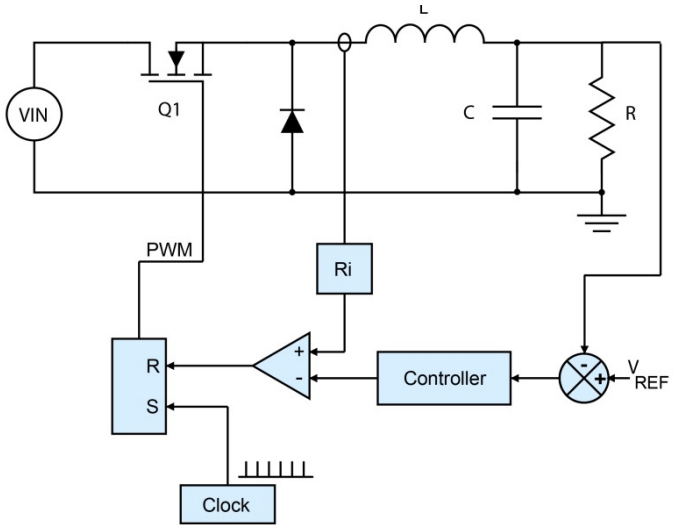

Figure 4: CMC schematics.

In CMC, the inductor current is measured in every switching cycle and compared with a reference signal.

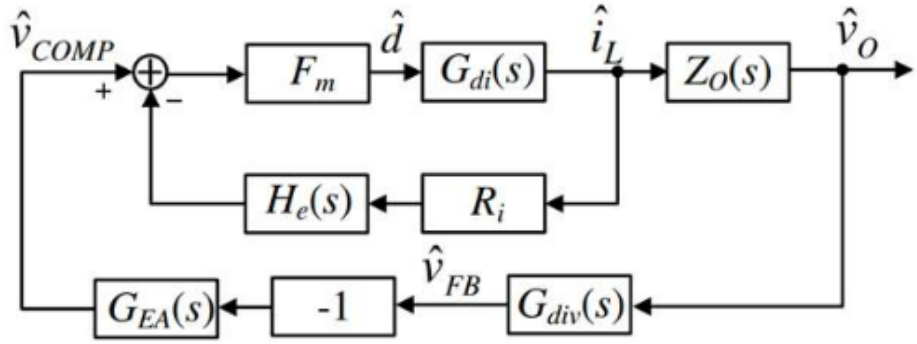

Figure 5: Block diagram for current mode control.

The control structure has two loops:

- Inner current loop: directly controls the inductor current by comparing the sensed current with a current reference every switching cycle.
- Outer voltage loop: regulates the output voltage and generates the current reference for the inner loop.

This approach offers several advantages. First, because the inductor current is directly controlled, the power stage behaves more like a first-order system, which simplifies the design of the voltage loop and helps achieve a stable and fast response. Second, since the inductor current is sensed in every switching cycle, the converter can react quickly to changes in input voltage or load without waiting for large deviations in the output voltage. Finally, the peak current in each switching cycle is limited by the current-sense threshold, providing natural cycle-by-cycle over-current protection and increasing the safety of both the motor and the power stage.

Due to these advantages in dynamic performance, stability and protection, peak current mode control is chosen as the control method for this project.

4 Component Selection

4.1 Three-Phase Full Bridge Rectifier

For the three-phase rectifier stage, the SKBPC5016 bridge module is selected. It is a three-phase bridge rectifier rated for an average output current of 50 A and a repetitive peak reverse voltage of 1600 V. The SKBPC5016 also has a high surge current capability , which is important to handle the inrush current when the large DC-link capacitor is first charged. SKBPC5016 can be seen in Figure 6

Figure 6: Selected three-phase full bridge rectifier.

4.2 Power Semiconductor Switch

The STW20NM60 MOSFET is selected because its voltage and current ratings are suitable for this project. It has a 600 V drain-to-source voltage rating, which is appropriate for the approximately 560 V DC-link voltage obtained from the three-phase rectifier. Its 20 A current capability is sufficient to safely handle both the normal motor current and the high starting current.

The MOSFET has a low on-state resistance, which reduces power losses and increases efficiency. Its TO-247 package allows effective heat dissipation using a heatsink. In addition, the selected switching frequency of 50 kHz is suitable for the STW20NM60, as it allows efficient operation with acceptable switching losses. Finally, this MOSFET is widely available in Turkey, making it a practical and reliable choice for this project.

4.3 Power Diodes

For freewheeling diode, the MUR3060PT diode is selected because its 600 V voltage rating matches the DC voltagelevel of the system, and its 30 A current rating is acceptable for the expected operating conditions. It is a fast recovery diode, which makes it suitable for the 50 kHz switching frequency of the buck converter.

4.4 Passive Components

In this section, the passive component values used in the simulation and design are verified through theoretical calculations. The input voltage is assumed to be the output of a three-phase full-wave rectifier, approximately 550 V. The output voltage is 180 V with a load of 21.7 Ω and 12.5 mH (armature included), resulting in 9 A output current.

4.4.1 Inductor L

The inductor value is selected based on the switching frequency and the target current ripple. For a buck converter operating in continuous conduction mode (CCM), the inductor current ripple can be approximated by

$$\Delta I_L = \frac{(V_{\text{in}} - V_{\text{out}})\, D}{L f_{\text{sw}}}, \tag{3}$$

so that the required inductance is

$$L = \frac{(V_{\text{in}} - V_{\text{out}})\, D}{\Delta I_L f_{\text{sw}}}. \tag{4}$$

Using $V_{\text{in}} \approx 550$ V, $V_{\text{out}} = 180$ V, $f_{\text{sw}} \approx 50$ kHz and a target ripple of about $\Delta I_L \approx 0.24\, I_{\text{avg}}$, the inductor value is found to be approximately $L \approx 1.08$ mH. The resulting current ripple is 23.8%, which satisfies the desired condition ($\Delta I_L < 30\%\, I_{\text{avg}}$).

4.4.2 Output Capacitor C

The output capacitor is selected to minimize the output voltage ripple. For a buck converter in CCM, the capacitive component of the output voltage ripple can be approximated by

$$\Delta V_C \approx \frac{\Delta I_L}{8 C f_{\text{sw}}}, \tag{5}$$

while the ESR-related ripple is

$$\Delta V_{\text{ESR}} \approx \Delta I_L R_{\text{ESR}}. \tag{6}$$

The total peak-to-peak output voltage ripple can be written as

$$\Delta V_{\text{out}} \approx \Delta V_C + \Delta V_{\text{ESR}}. \tag{7}$$

In practice, for high switching frequencies, the ripple is primarily determined by the equivalent series resistance (ESR) rather than the capacitance value itself. With $C = 470$ μF and a typical ESR value, the calculated output voltage ripple is about 1.2%, which satisfies the desired condition ($\Delta V_{\text{out}} < 5\%\, V_{\text{out}}$). The ESR value is critical at this point; however, this is not a concern since 470 μF capacitors generally have about 0.2 Ω maximum ESR.

4.4.3 Input Capacitor

The input capacitor must attenuate the 300 Hz ripple from the three-phase rectifier and handle the high-frequency pulsed RMS current drawn by the buck converter. For a

three-phase diode bridge feeding a capacitive DC link, the low-frequency DC-link voltage ripple can be approximated as

$$\Delta V_{\mathrm{dc}} \approx \frac{I_{\mathrm{out}}}{6 f_{\mathrm{line}} C_{\mathrm{dc}}}, \tag{8}$$

where f_{line} is the grid frequency (50 Hz) and C_{dc} is the DC-link capacitor.

In addition, the high-frequency RMS current drawn by the buck stage is approximately

$$I_{C,\mathrm{rms}} \approx I_{\mathrm{out}} \sqrt{D(1-D)}, \tag{9}$$

which is used to check the current rating of the input capacitor.

A value of $C_{\mathrm{dc}} = 10$ mF is selected, which provides sufficient attenuation of the 300 Hz ripple and can safely handle the worst-case RMS input current for the buck converter.

4.5 Controller IC (UC3842)

The UC3842 high-performance current mode controller is selected as the core control IC for this project. It is a peak current mode PWM controller and its native architecture is designed for current mode control, which aligns with the control strategy decided in Section 3.3. Unlike voltage-mode controllers (e.g. SG3525, TL494), the UC3842 includes a dedicated current sense comparator and internal logic that provide cycle-by-cycle current limiting and fast transient response.

4.5.1 Internal Operation

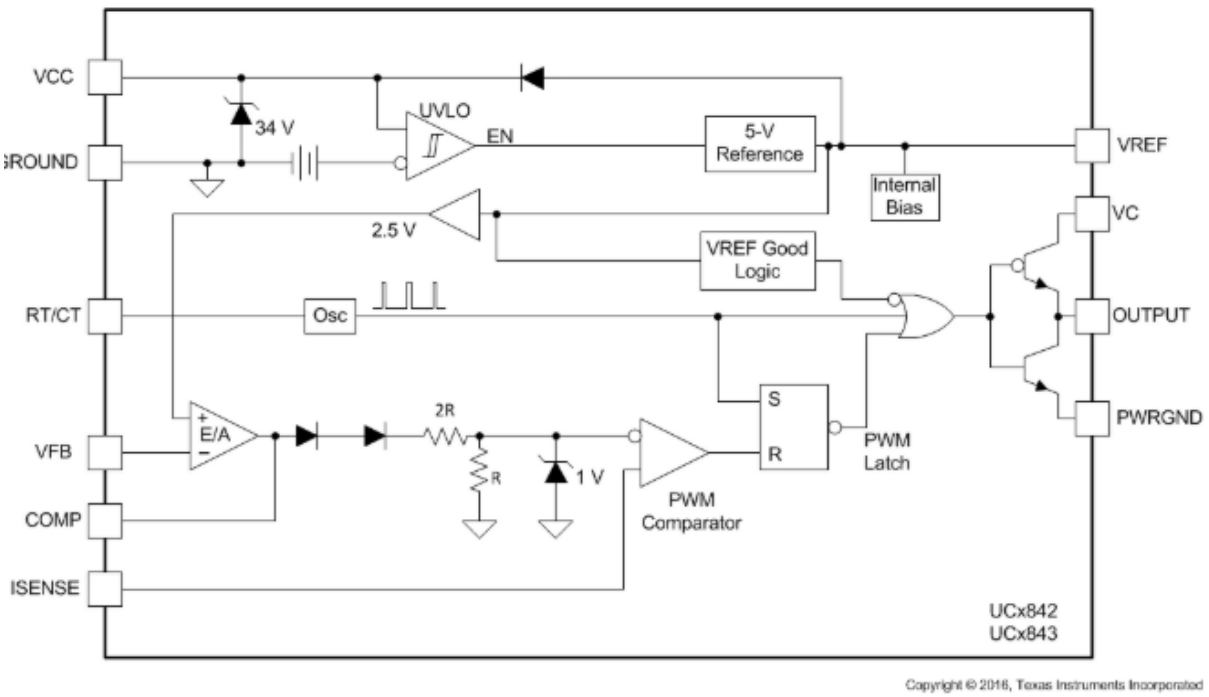

Figure 7: Internal logic of UC3842.

The main internal building blocks of the UC3842 used in this design are:

Error Amplifier The error amplifier compares the output feedback voltage (from the voltage divider) with the internal reference. The difference between these two signals creates an error signal, which determines the required peak inductor current for regulation. A higher error signal increases the allowed peak current and therefore the duty cycle; a lower error signal decreases it.

Current Sense Comparator The inductor (switch) current is measured using the shunt resistor in the return path. The resulting sense voltage is applied to the current sense pin and compared with the error amplifier output. When the sensed current reaches the level set by the error signal, the comparator turns the switch off. In this way, the peak inductor current is directly controlled in every switching cycle.

PWM Latch and Oscillator The internal oscillator defines the switching period. At the beginning of each cycle, the PWM latch turns the MOSFET on. When the current sense comparator detects that the peak current limit has been reached, the latch is reset and the MOSFET is turned off. This process repeats every period and generates the PWM signal at the UC3842 output. For the selected operating conditions, additional slope compensation is not required.

In the overall closed loop in Figure 8, the buck converter and DC motor form the plant, the current shunt and voltage divider provide the feedback signals, the UC3842 acts as the controller that generates the PWM signal, and the FOD3120 gate driver functions as the actuator that isolates and drives the MOSFET gate.

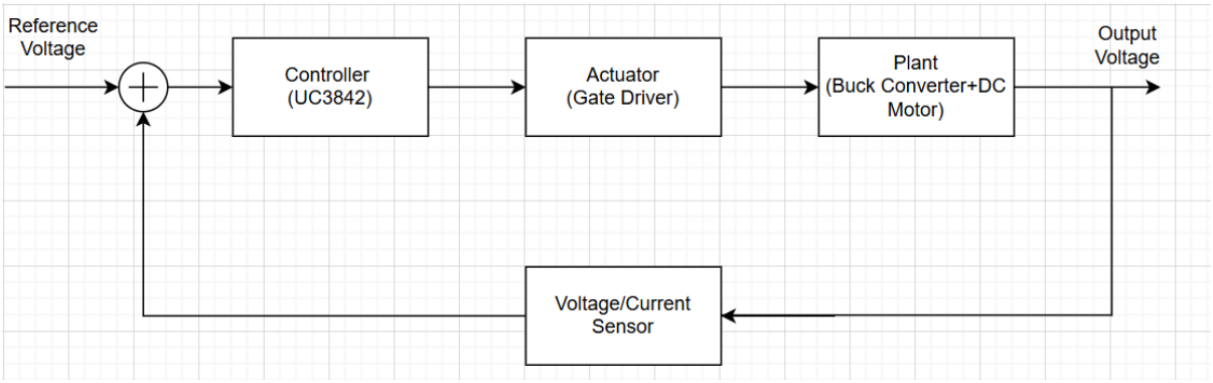

Figure 8: Block diagram of closed loop control.

4.5.2 Peripheral Design

The switching frequency of the converter is determined by the internal oscillator of the UC3842, which is programmed via an external resistor R_T and capacitor C_T. According to the datasheet, the oscillator frequency can be approximated by

$$f_{\text{osc}} \approx \frac{1.72}{R_T C_T}. \tag{10}$$

To achieve a switching frequency of about 50 kHz, the following component values are selected within the allowable ranges (5 kΩ $< R_T <$ 100 kΩ and $C_T >$ 1 nF):

- timing resistor $R_T = 10$ kΩ

- timing capacitor $C_T = 3.3$ nF

Substituting these values into the equation gives $f_{\text{osc}} \approx 52.1$ kHz, which satisfies the design target.

4.5.3 Powering the IC

The UC3842 requires a stable DC supply voltage V_{CC} to operate. The device has a start-up threshold of about 16 V and a maximum rating of 30 V.

In this design, a separate supply strategy is used. According to the project specifications, a second power source for the driver circuitry is allowed, so an independent 18 V DC source is used to feed the VCC pin. Using a separate, isolated low-voltage supply ensures that the controller is active and stable regardless of the main power stage status, and allows safer testing of the gate drive signals before high voltage is applied.

A bypass capacitor $C_{\text{bypass}} = 0.1$ μF is placed close to the VCC pin to filter noise and supply the high current spikes required during the charging of the MOSFET gate capacitance.

4.6 Gate Driver

In the buck converter, the NMOS is used as a high-side switch, so its source is not at ground and its voltage changes during switching. To turn the MOSFET on, a gate-to-source voltage of about 12–15 V is required, which means the gate voltage must follow the source. Since the UC3842 is referenced to ground, it cannot drive the high-side MOSFET directly. To solve this, the FOD3120 optically isolated gate driver is used. The PWM signal from the UC3842 drives the FOD3120, and the switching signal is transferred optically, providing galvanic isolation and protecting the control circuit from high-voltage noise. The output side of the FOD3120 is powered by an isolated 15 V supply referenced to the MOSFET source, allowing it to maintain a proper gate-to-source voltage even as the source node potential fluctuates. The FOD3120 can supply high peak output current (up to 2.5 A) to charge and discharge the MOSFET gate capacitance rapidly, ensuring fast switching speeds suitable for 50 kHz operation. On the primary side, the UC3842 output is connected to the FOD3120 input anode through a current-limiting resistor; on the secondary side, the FOD3120 VCC pin is tied to the floating +15 V, GND is tied to the MOSFET source, and the output pin is connected to the MOSFET gate.

4.7 Sensing & Feedback

4.7.1 Current Sensing Method

In this design, the inductor (output) current is measured with a shunt resistor placed in the return path of the load. Since the resistor is located between the load and ground, it carries the current both when the MOSFET is on and when the freewheeling diode conducts. Thus, the voltage across the resistor directly represents the instantaneous inductor current I_L:

$$V_{\text{sense}} = I_L R_{\text{sense}}. \tag{11}$$

The UC3842 current sense pin has a threshold of approximately 1.0 V. To limit the maximum inductor current to 20 A, the sense resistor value is chosen as

$$R_{\text{sense}} = \frac{1.0 \text{ V}}{20 \text{ A}} = 0.05 \ \Omega, \tag{12}$$

which provides a safe operating margin for the 2 kW motor drive.

To avoid false triggering of the UC3842 current comparator due to switching noise and leading-edge spikes, an RC low-pass filter is added between the sense resistor and Pin 3:

- $R_f = 1$ kΩ
- $C_f = 470$ pF

This filter attenuates high-frequency noise so that the controller responds to the true current ramp.

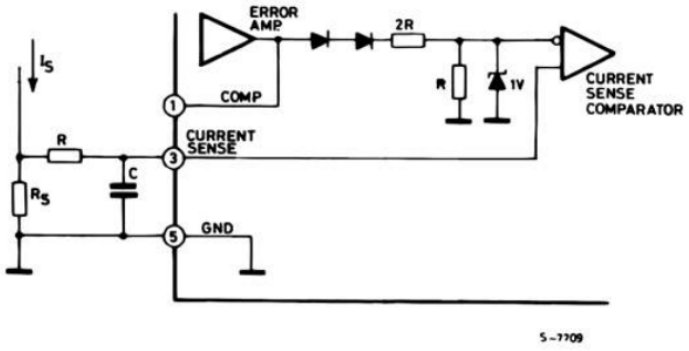

Figure 9: Current sensing schematic from datasheet.

4.7.2 Voltage Feedback Divider Calculations

The output voltage is regulated by feeding a scaled version of V_{out} to the VFB pin (Pin 2) of the UC3842. The internal error amplifier compares this feedback signal with the 2.5 V internal reference.

A resistive divider is used to generate the feedback voltage:

- Top resistor: $R_{\text{top}} = 390$ kΩ
- Bottom branch: $R_{\text{bot}} = 4.7$ kΩ in series with a 50 kΩ potentiometer

The relationship between the output voltage and the feedback voltage is

$$V_{\text{FB}} = V_{\text{out}} \frac{R_{\text{bot}}}{R_{\text{top}} + R_{\text{bot}}}, \tag{13}$$

so

$$V_{\text{out}} = V_{\text{ref}} \left(1 + \frac{R_{\text{top}}}{R_{\text{bot}}}\right), \tag{14}$$

where $V_{\text{ref}} = 2.5$ V.

When the potentiometer is at minimum, $R_{\text{bot}} \approx 4.7$ kΩ and the maximum output voltage is higher than 180 V, so the 180 V target can be reached easily. When the potentiometer is at maximum, $R_{\text{bot}} \approx 54.7$ kΩ and the minimum output voltage is around 20 V. Thus, the divider provides an adjustable output range of approximately 20–180 V, which is suitable for controlling the DC motor speed

4.8 Fuses

For input side protection, the Bussmann FWC-32A10F fast-acting fuse (10×38 mm, 32 A, 600 V) is selected. The 600 V voltage rating provides a safe margin over both the 380 V line-to-line AC input and the ≈ 560 V DC link voltage after rectification.

5 Simulations

This section presents the verification of the design using two different simulation environments: PSIM for system-level control verification and LTspice for detailed circuit/component behavior.

5.1 PSIM Simulations

This section presents the verification of the design using PSIM simulation software. The simulation process is divided into two stages. Firstly, we implement an Open-Loop simulation with ideal components to verify the topology decisions, passive component sizing, and rectifier operation. Secondly, a Closed-Loop simulation using the UC3842 controller model to verify the feedback regulation and system stability.

5.1.1 Open Loop Testing

The primary objective of this stage is to validate the DC link generation and the filtering performance of the Buck converter stage without the complexities of the feedback loop. The schematic for this simulation is shown in Figure 10. The circuit consists of a Three-Phase Diode Bridge Rectifier fed by a 3-phase grid, a 10mF DC link capacitor, and the Buck converter stage. The switch is operated with a fixed duty cycle calculated to yield 180V output.

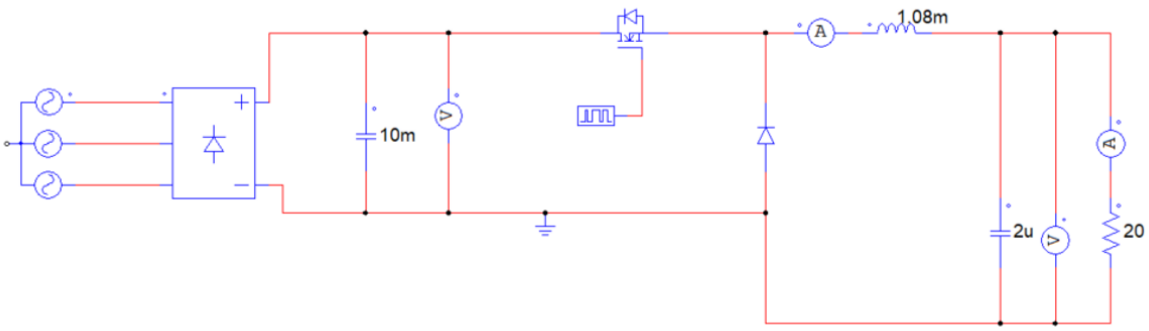

Figure 10: Psim schematic for open loop testing.

As we can observe in the simulation results shown in Figure 11, the rectified 3-phase voltage is smoothed by the input capacitor. The DC link voltage settles at approximately 565 V. This confirms the peak rectification of the line to line voltage and shows that the capacitor is sufficient to hold the voltage stable with minimal ripple.

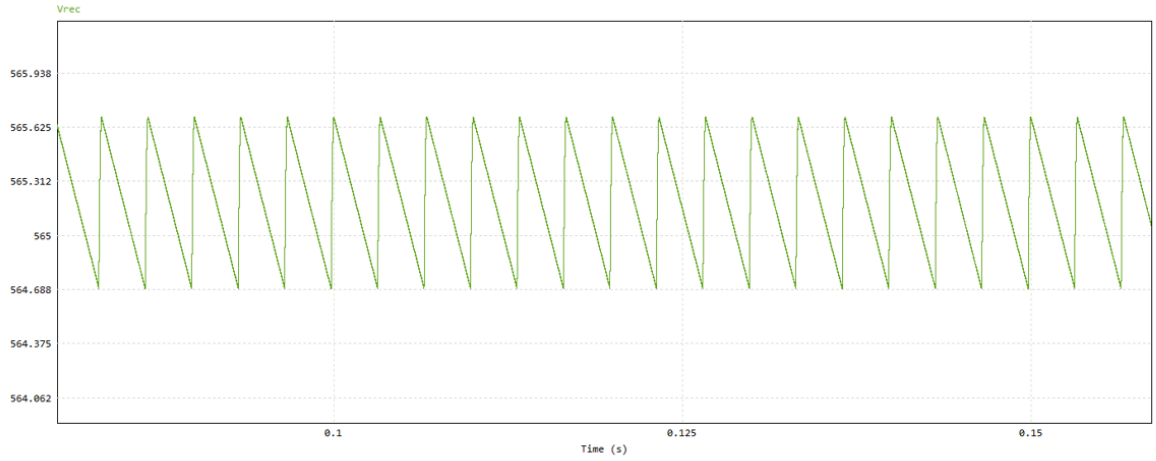

Figure 11: Rectified voltage.

Output voltage reaches the desired value and the steady-state output voltage oscillates between approximately 186.5 V and 188.5 V. This corresponds to a peak-to-peak ripple of about 1.1% of the output voltage, which is well within the 5% target specification.

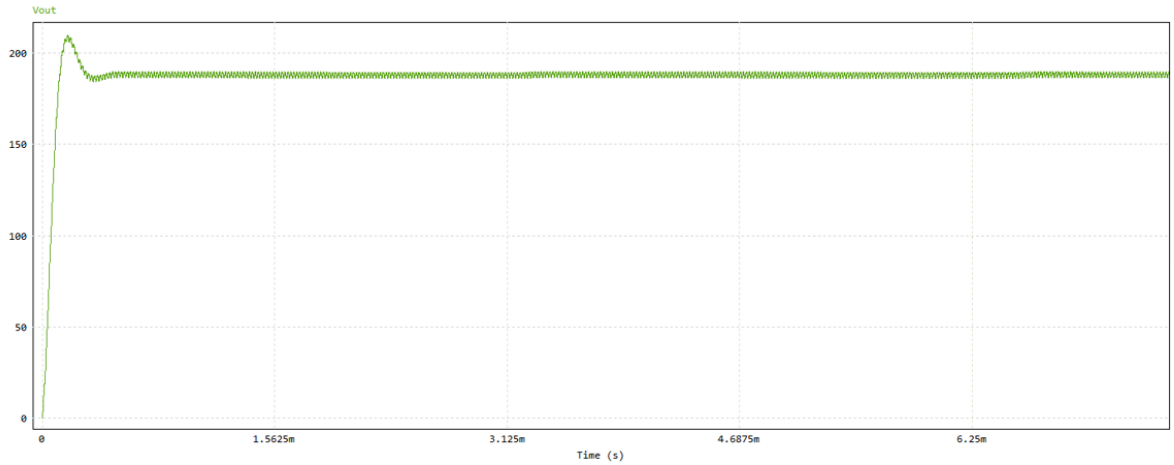

Figure 12: Open loop output voltage.

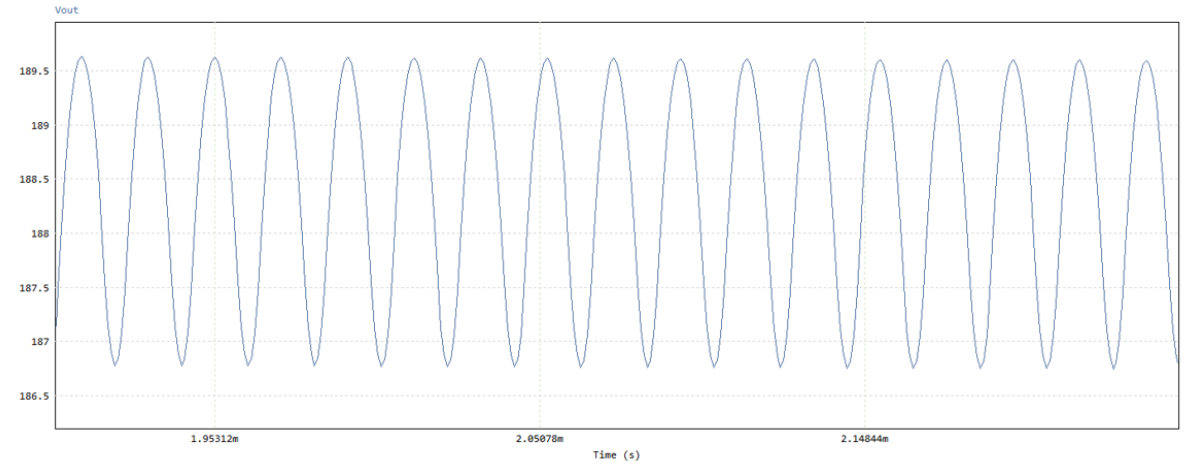

Figure 13: Output voltage ripple.

The inductor current demonstrates continuous conduction mode (CCM) operation, oscillating between 8.3 A and 10.5 A. The ripple magnitude is roughly 23% of the average current, satisfying the design goal of $< 30\%$.

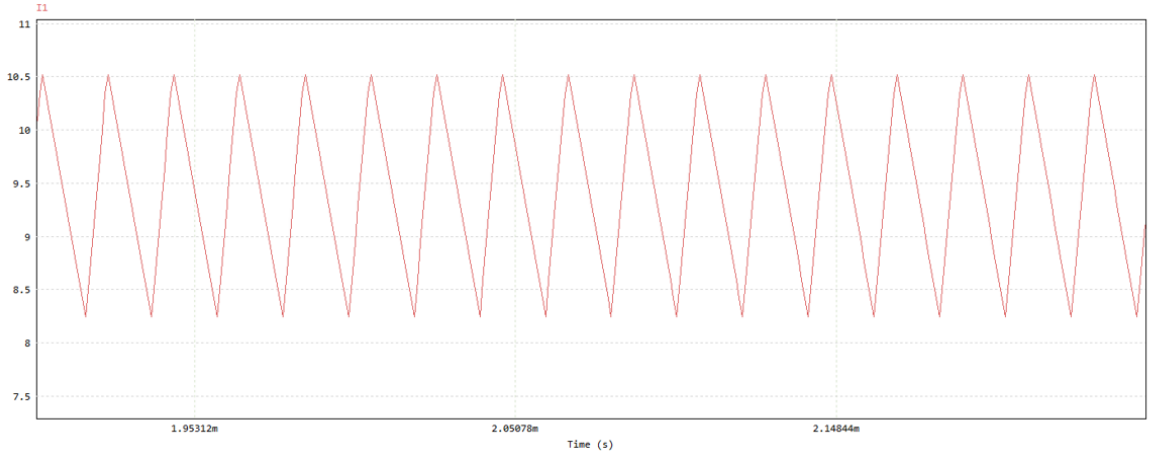

Figure 14: Open loop inductor current.

5.1.2 Closed Loop Testing

After the open loop verifications, we integrated the UC3842 to the circuit to make a closed loop system and control the output. This setup validates the Current Mode Control logic, including the voltage divider network and current sensing. Figure 15 shows the circuit schematic.

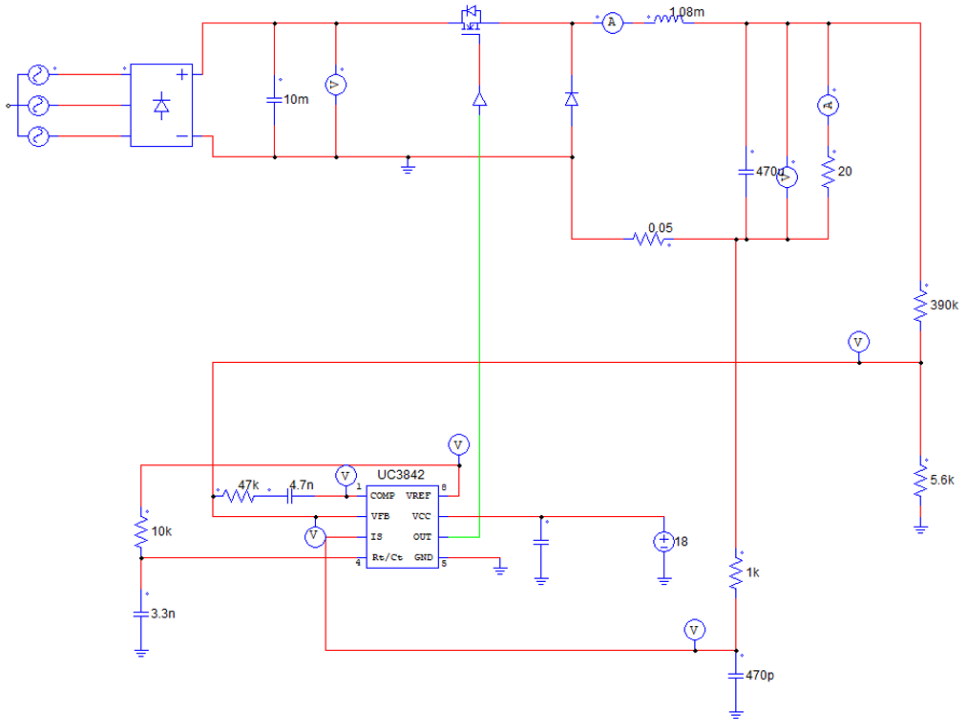

Figure 15: Closed loop schematic.

The system start-up behavior is shown in the following plots. The output voltage ramps up smoothly from 0 to the target 180V within approximately 15ms.

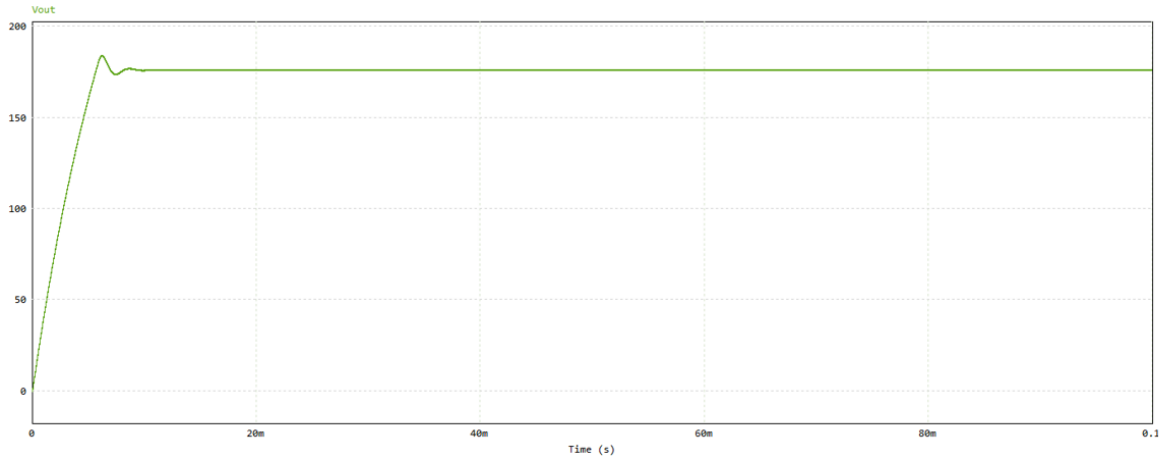

Figure 16: Closed loop simulation output voltage.

In Figure 17, inductor current is shown. These results verify our design.

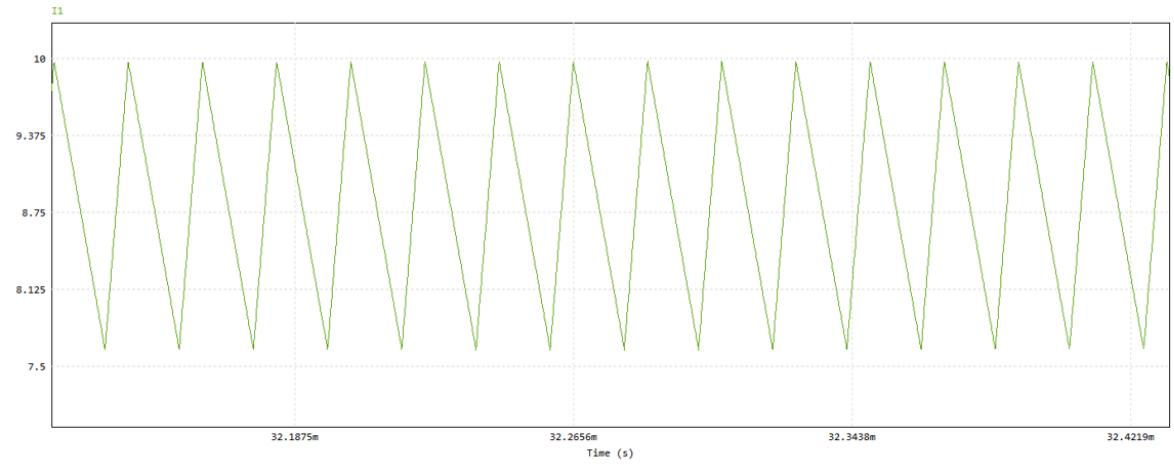

Figure 17: Closed loop simulation inductor current.

5.1.3 Simulation With DC Machine

Following the closed-loop verification with a static resistive load, the system was tested with a dynamic DC Machine model to validate the drive's performance under realistic load characteristics. This step is crucial to observe the effects of the motor's back-EMF (Eb), armature inductance (La), and mechanical inertia (J) on the converter's startup transient and steady-state operation. The resistive load was replaced in PSIM with DC Machine block. The motor parameters were configured to match the physical motor available in the laboratory. The parameters given to this block are shown in the Figure 18. And schematic of the circuit is given in Figure 19. We connected constant torque load to the motor.

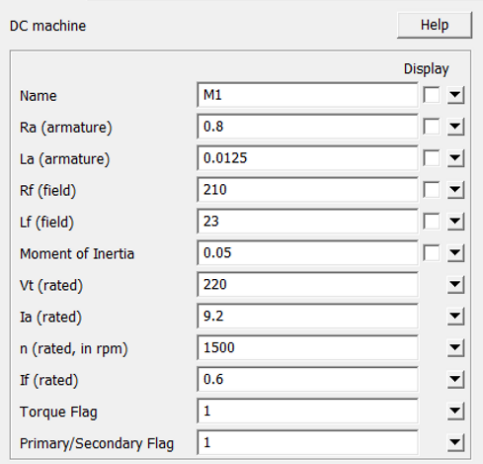

Figure 18: Motor parameters in PSIM.

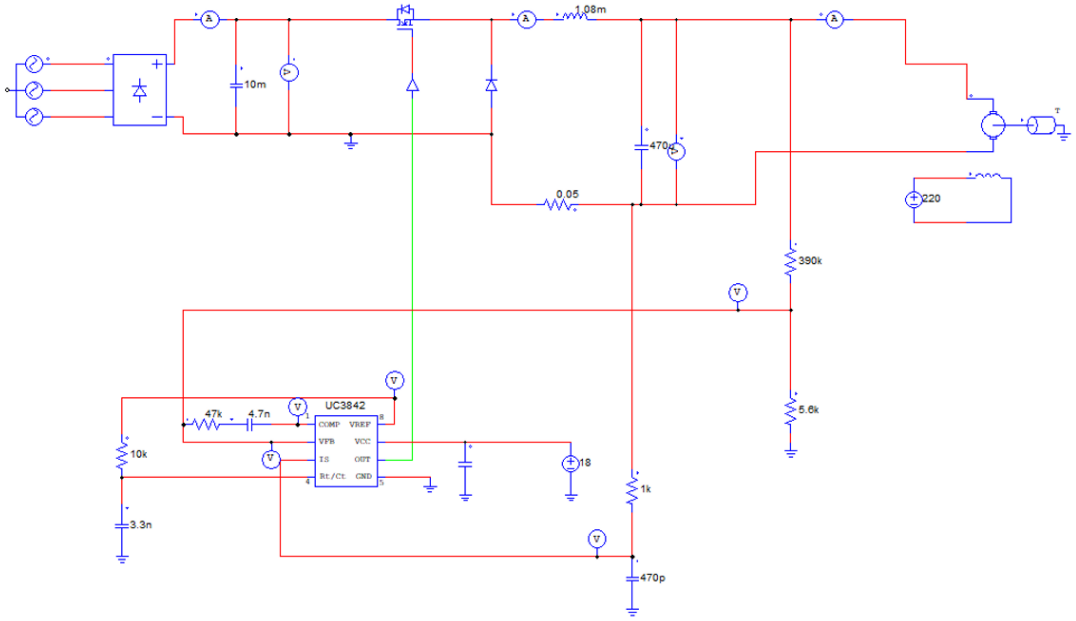

Figure 19: Circuit schematic with DC machine.

The output voltage and output current waveforms are shown in Figure 20 and Figure 21. The DC link voltage applied to the motor terminals ramps up from 0V to the target 180V over a period of approximately 300ms. This controlled ramp-up is significantly slower than the resistive load case, which is expected due to the "Soft Start" effect created by the large mechanical inertia of the motor. The current waveform reveals a significant inrush current spike at the beginning of the operation. This high transient current occurs because the motor is at a standstill where the back-EMF is zero, leaving only the small armature resistance to limit the current flow. To protect the power semiconductor switches and the motor windings from potentially damaging electrical and thermal stresses during the physical implementation, a Soft Start strategy is strictly required. This should be implemented by gradually increasing the output voltage reference to allow the motor to build up back-EMF slowly, thereby keeping the startup current within safe operating limits.

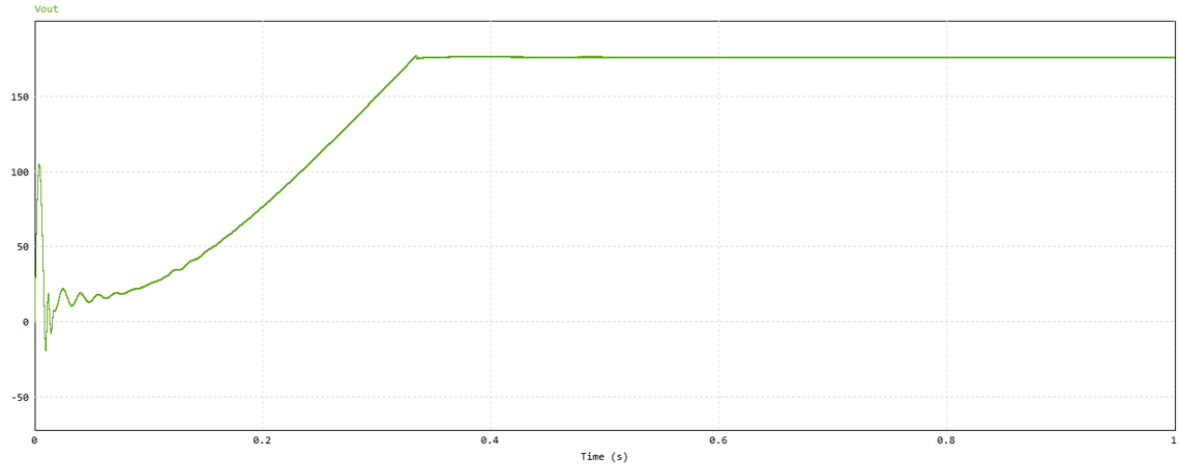

Figure 20: Output voltage when dc machine connected.

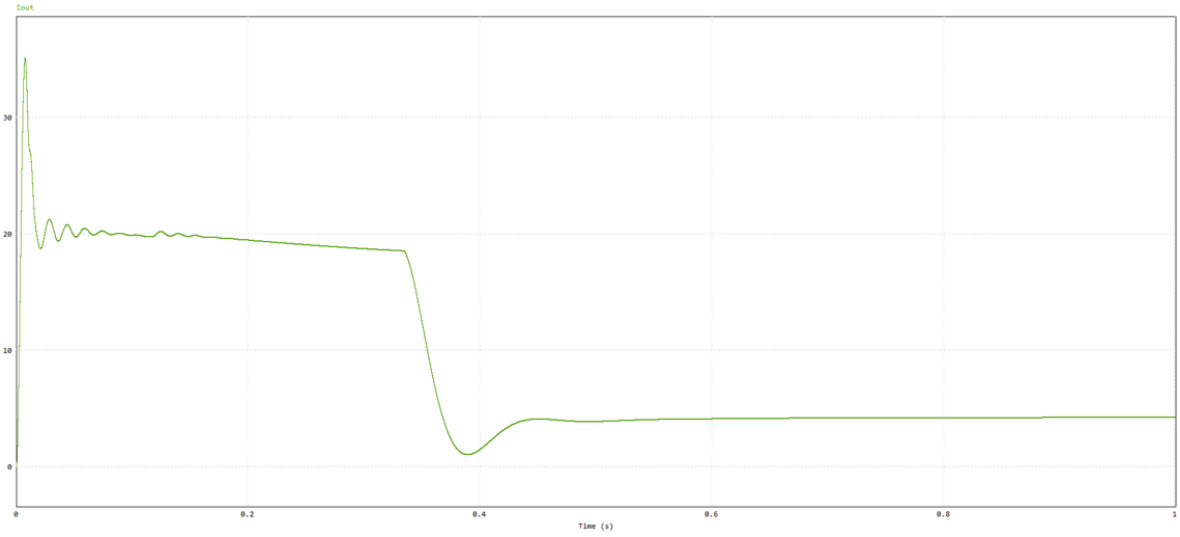

Figure 21: Output current when dc machine connected.

5.2 LTspice Simulations

5.2.1 Simulation Setup

The LTspice schematic in Figure 22 uses the SPICE model of the UC3842 (modeled here with LT1246 as an equivalent), as well as realistic models for the MOSFET and diodes. The FOD3120 is modeled as an operational amplifier with the same input and output configuration. The component values and parameters are selected to match the practical design as closely as possible.

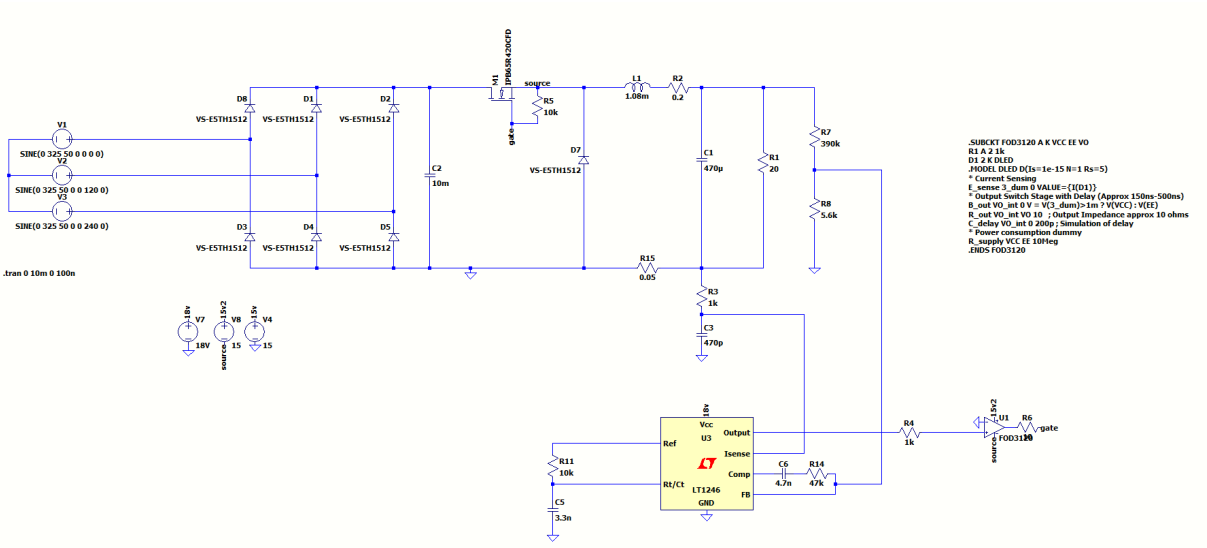

Figure 22: Schematic of the design.

5.2.2 Voltage and Current Waveforms

Output Voltage of the Rectifier We are supplying 325 V peak to peak voltage to 3-phase diode rectifier. Rectifier output has the following voltage waveform:

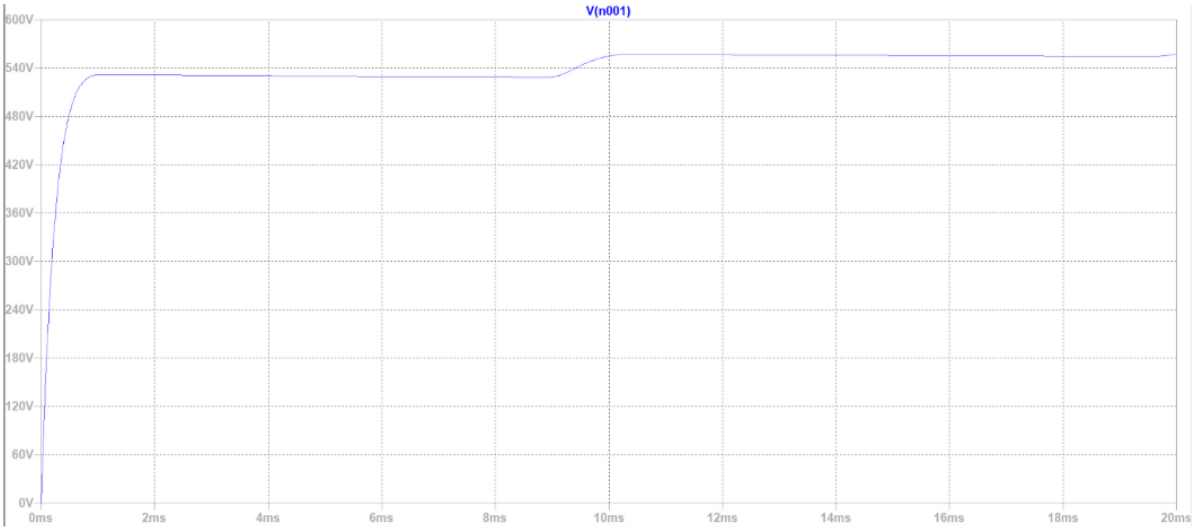

Figure 23: Output voltage of the rectifier.

During the first 10 ms, the DC link voltage rises because the large input capacitor (10 mF) is charging. Since the buck converter starts with a low duty cycle due to soft-start, the DC link voltage increases toward the peak line-to-line voltage $\sqrt{2}\,V_{\mathrm{LL}}$, and there may be a small overshoot because of the source impedance.

Gate to Source Voltage $V_{\mathbf{GS}}$ FOD3120 gate driver controls the on-off of the MOSFET, i.e. arranging the duty cycle. This configuration can be observed from the Vgs waveform of the MOSFET.

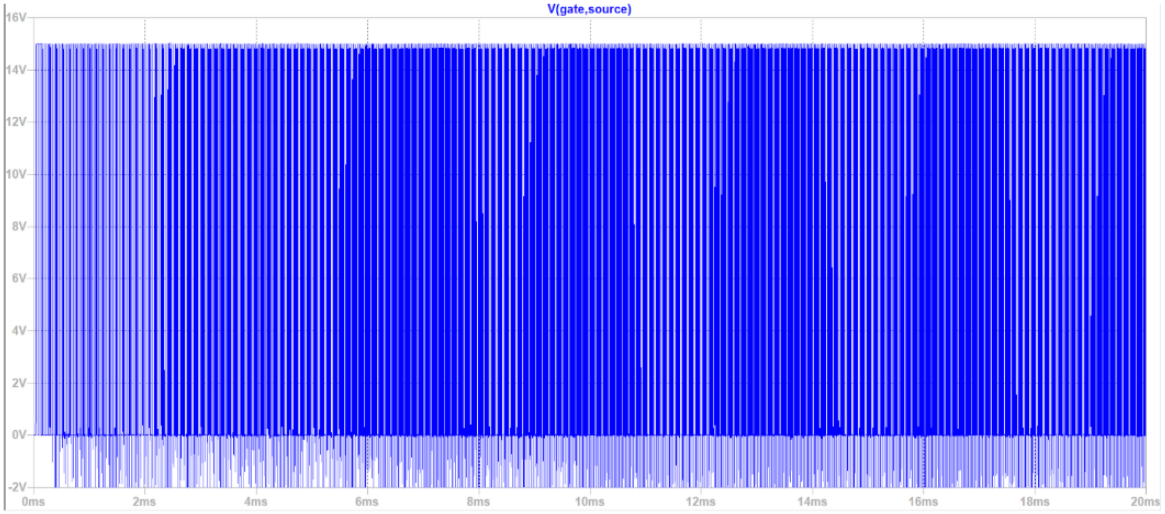

Figure 24: (V_{GS}).

Since frequency is high, we can't observe a clear behavior. However, if you take a closed look at this waveform you can observe that during soft start (beginning of the simulation), duty cycle is small and keep increasing slowly until output voltage reaches 180V. After that point, we have constant output voltage, therefore constant duty cycle. Observe the initial and final state down below.

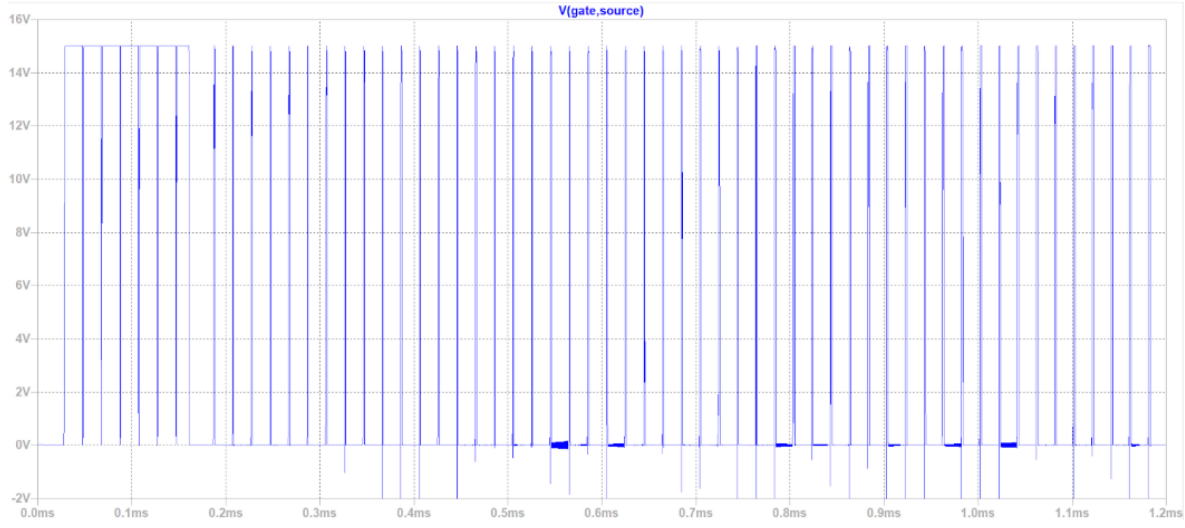

Figure 25: Initial duty cycle.

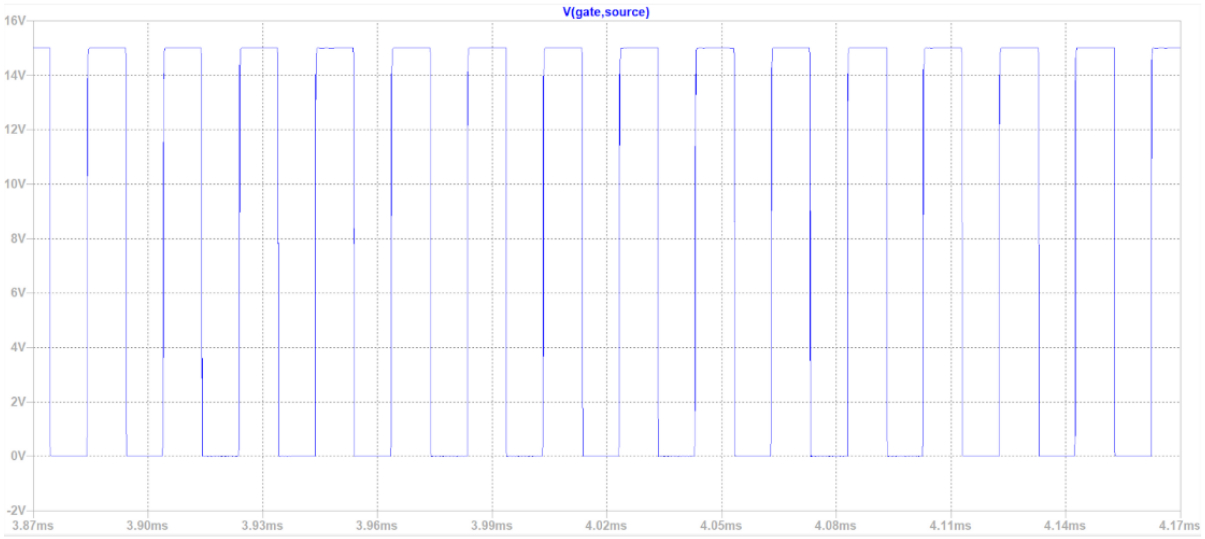

Figure 26: Duty cycle increased since output voltage increased.

Switching Characteristics By zooming in on the MOSFET turn-on and turn-off transitions, the drain-source voltage V_{DS} waveform is examined and can be seen in Figure 27

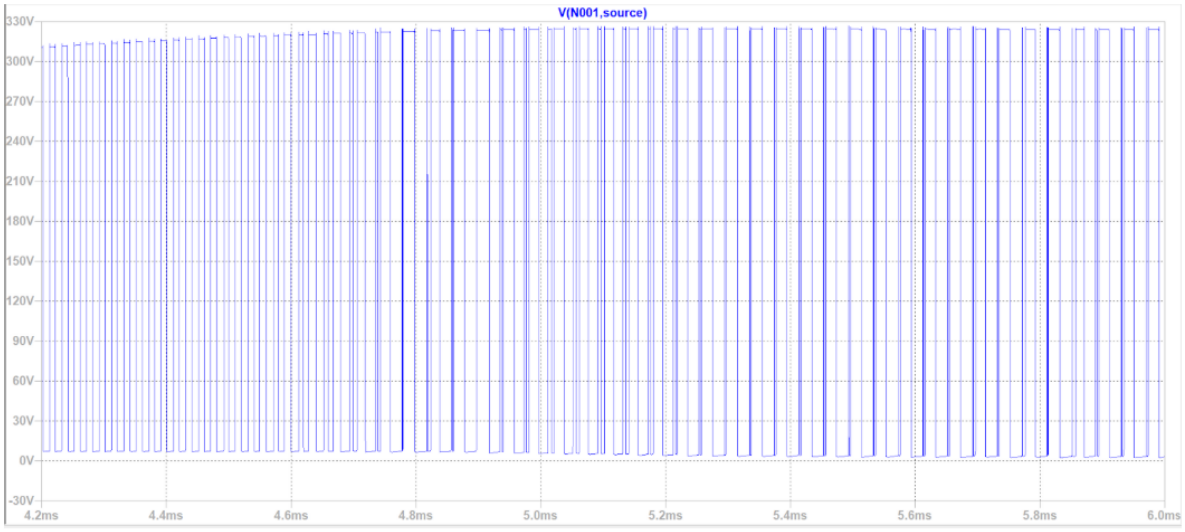

Figure 27: V_{DS}.

Drain-Source voltage Vds waveform across the STW20NM60 MOSFET. The plot demonstrates switching transitions and confirms that the peak voltage stress (approximately 560V) remains within the safe operating limits of the device (600V breakdown rating).

Output Waveforms Resulted output voltage is in Figure 28

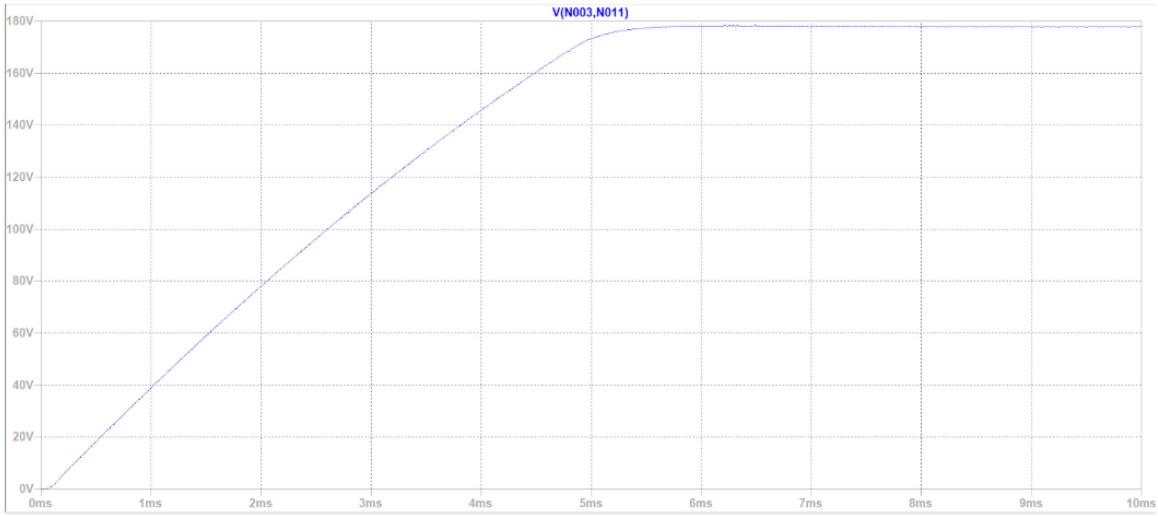

Figure 28: V_{O}.

Output voltage, slow increase due to soft start. Voltage safely reaches the desired 180V without overshoot.

Resulted output current is in Figure 29.

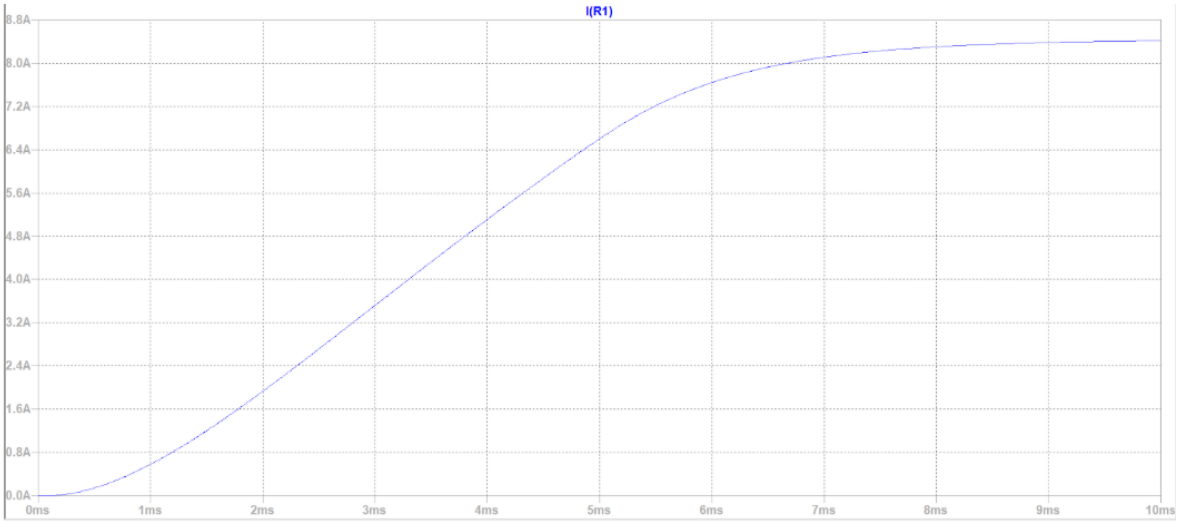

Figure 29: I_{O}.

Output current slowly reaches to 8.5A, supplying 1550W to the load side.

Resulted inductor current is in Figure 31

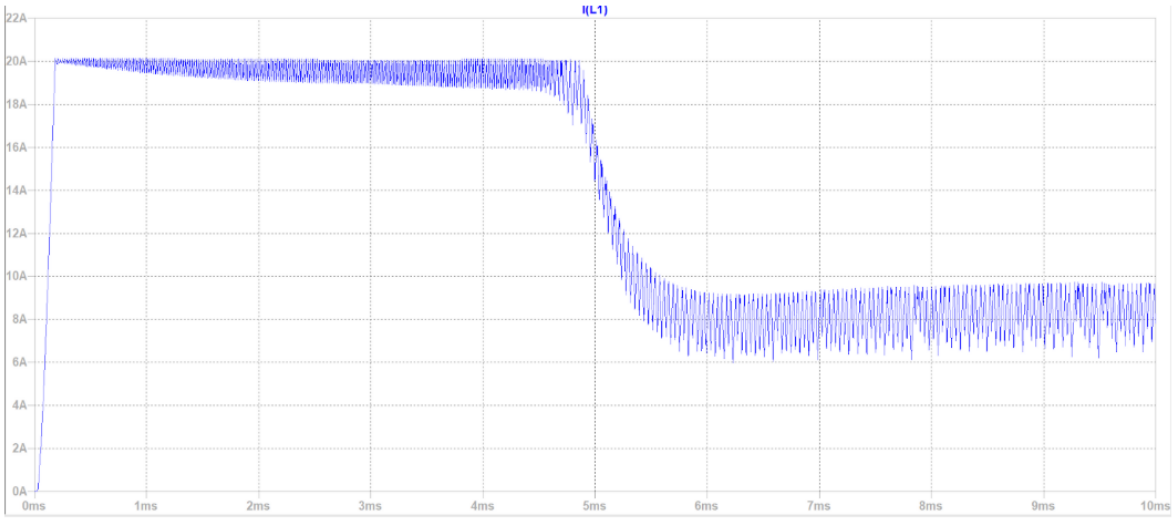

Figure 30: I_{L}.

Inductor (1.08mH) current starts with 20A, which is the reason we selected 30A free-wheeling diode, and drops to approximately 8.5A. This inductor selection of 1.08 mH satisfies our current ripple expectation. Down below, you can take a close look to the waveform and observe the ripple when system reaches steady state.

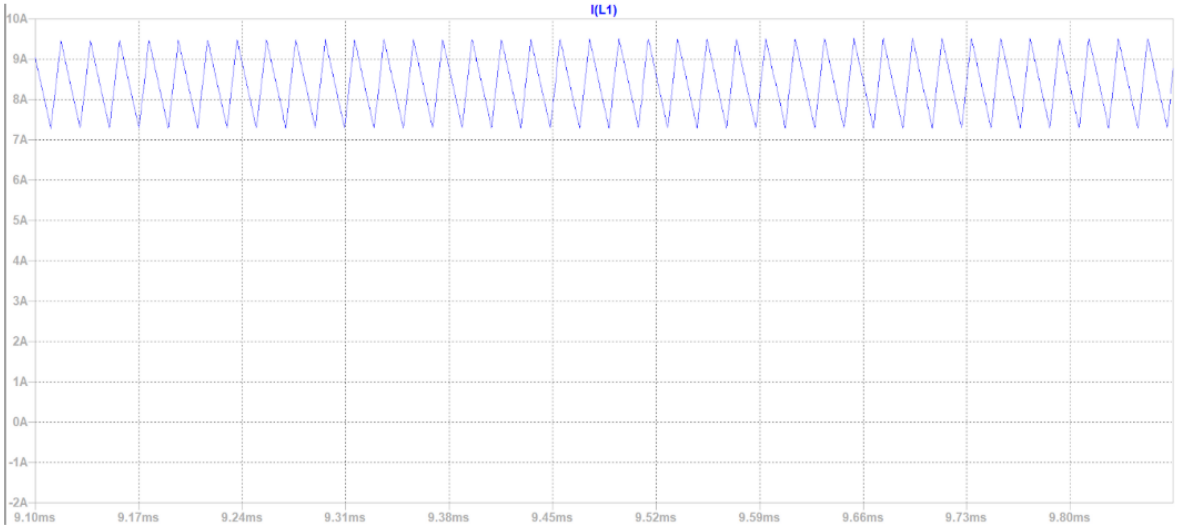

Figure 31: I_{L} ripple.

UC3842 Operation The current sense pin (Pin 3) waveform is observed to show the ramp signal across the sense resistor and the effect of the RC filter. The VCC voltage is monitored to verify that the IC supply is stable during start-up and normal operation.

Figure 32 shows the output voltage of the DC3842.

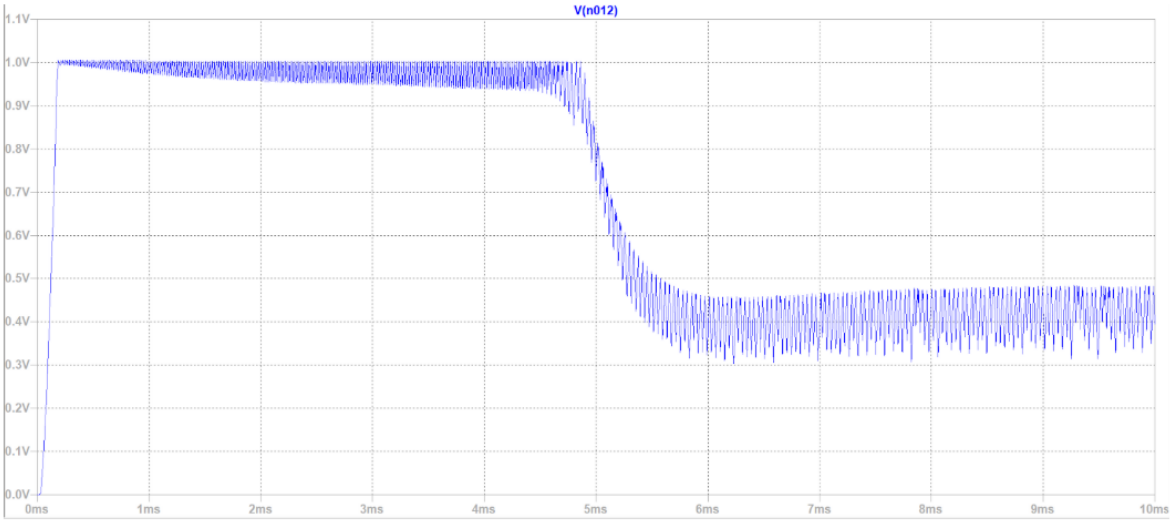

Figure 32: Output voltage of the DC3842.

This waveform at the Current Sense pin (Pin 3) shows the instantaneous current flowing through the sense resistor. It tells us how much current is passing through the power switch and reflects the Peak Current Mode operation of the UC3842. A smooth, clean ramp means the RC filter is working well, preventing false triggering from spikes and ensuring stable control. To ensure this, observe for a small time interval after output voltage reaches 180V, corresponding to 5 - 6ms.

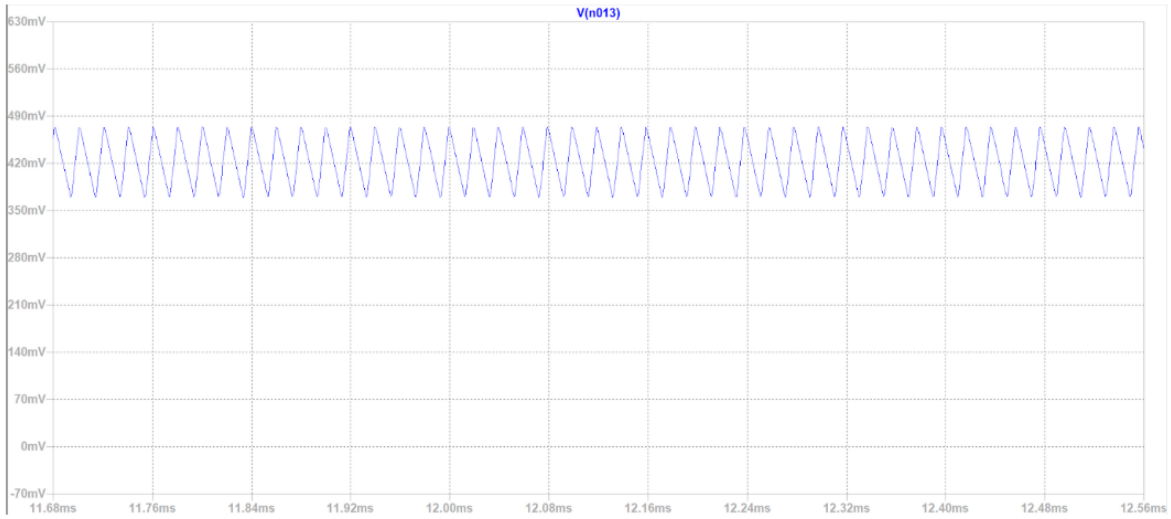

Figure 33: Output voltage of the DC3842 for a small time interval.

6 Conclusion

In this project, we designed, simulated, and analyzed a high-power DC motor driver system that converts a three-phase 380 V AC grid input into an adjustable 0–180 V DC output. The main goal was to safely and accurately drive a 1.6 kW separately excited DC motor, with good voltage regulation and reliable current protection. To achieve this, we chose a buck converter supplied by a three-phase rectifier. This setup provides a high DC link voltage of about 560 V, giving enough margin for the buck converter to regulate the output down to 180 V while also keeping the current draw from the three-phase grid balanced.

We used peak current mode control with a UC3842 controller instead of voltage mode control. Both theory and simulations showed that this approach simplifies the control structure, makes loop compensation easier, and naturally limits current cycle by cycle. As a result, the system responds quickly and stably to sudden changes in input voltage or load conditions.

Simulation results from LTspice and PSIM confirmed the design's validity. The inductor current ripple was 23.8%, staying under our 30% target, and the output voltage ripple was limited to 1.2%, well below the 5% requirement. We set the switching frequency at around 52.1 kHz, balancing switching losses and the size of passive components. The high-side N-channel MOSFET was successfully driven with a FOD3120 optically isolated gate driver and a floating power supply, ensuring safe and reliable operation. The feedback network allowed the output voltage to be adjusted from roughly 20 V to 180 V, fully covering the motor's operating range.

While simulations confirm the design works in theory, moving to a real hardware prototype introduces practical challenges. In a real circuit, the freewheeling diode's reverse recovery can produce sharp current spikes each time the MOSFET switches on. An RC filter helps reduce these spikes, but proper grounding is crucial to avoid unstable operation.

Parasitic inductance and the resulting voltage spikes are another concern. Even though our MOSFET is rated for 600 V, these spikes can still exceed safe limits or cause ringing and electromagnetic noise. If large spikes occur during testing, adding a snubber circuit may be necessary.

Inrush current is also significant. The large DC link capacitor helps reduce low-frequency ripple, but when first connected to the rectified grid, it draws a very large current almost like a short circuit, which can damage diodes or blow fuses. To prevent this, a soft-start method such as a pre-charge resistor with a bypass relay can be used in the prototype.

Finally, thermal management is critical. Even with good simulated efficiency, switching and conduction losses generate heat in the MOSFET and diode at 52.1 kHz. While the TO-247 package can dissipate heat, proper mounting, thermal paste, and insulation are essential for both effective heat transfer and electrical safety, since the MOSFET drain is connected to the metal tab. Heat sinks will be used to mitigate this problem. Since the system operates with relatively high voltage and current, fuses will be placed on both the rectifier side and the load side.

In conclusion, the system meets the main design goals for power capability, ripple performance, and control stability. It provides a solid foundation for moving from simulation to a real hardware prototype, while highlighting the practical considerations that need careful attention for reliable operation.

In conclusion, the design meets the main requirements: the rectifier and load outputs

are as desired, the control system operates as intended (as observed from the simulations), and the system gives the necessary response when the output voltage reaches 180 V. Our gate driver and controller work in correlation. We preferred an analog design to gain insight into the topics covered throughout the course, without any digital control. This makes our design more sensitive and required detailed research. However, a real-life implementation will probably have unexpected problems due to environmental effects, and we may need to reconsider some of our design decisions.

7 References

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