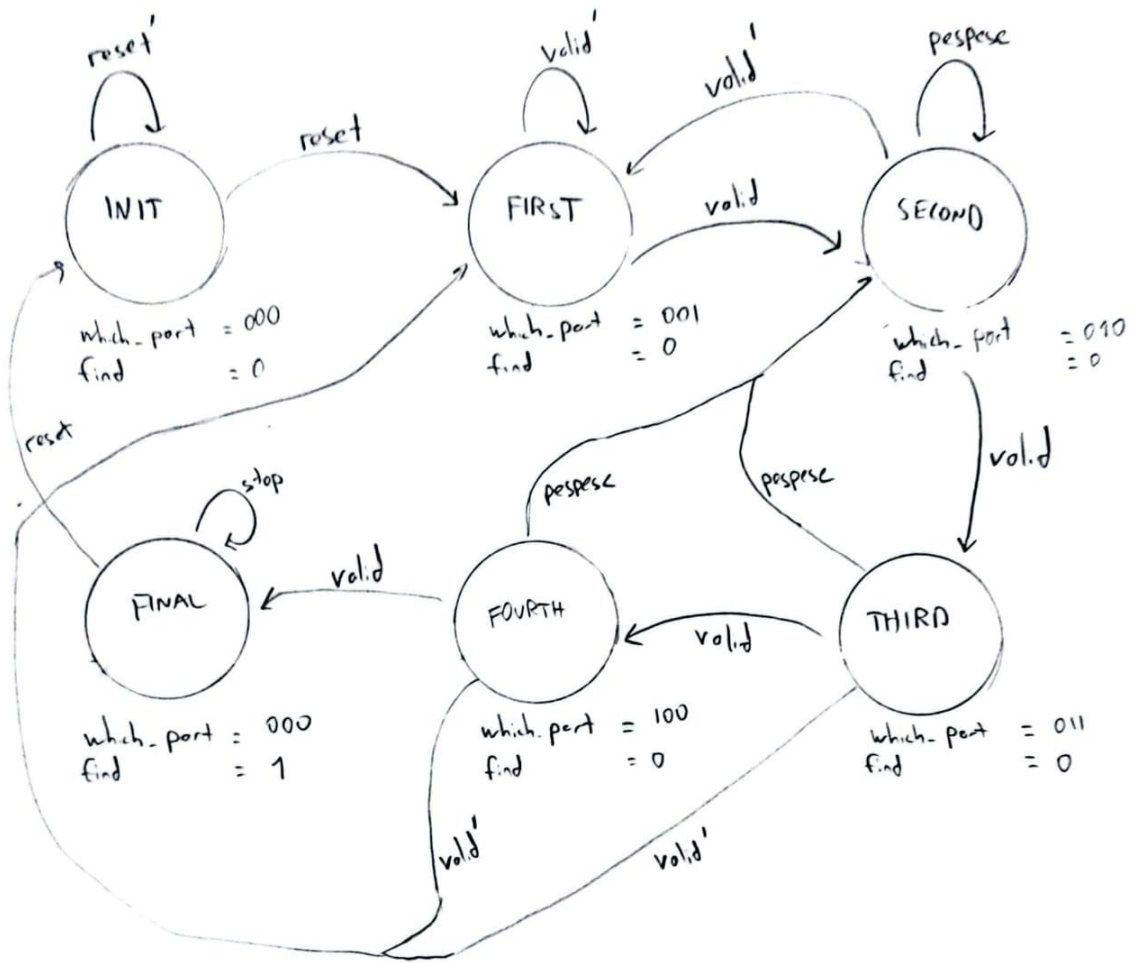
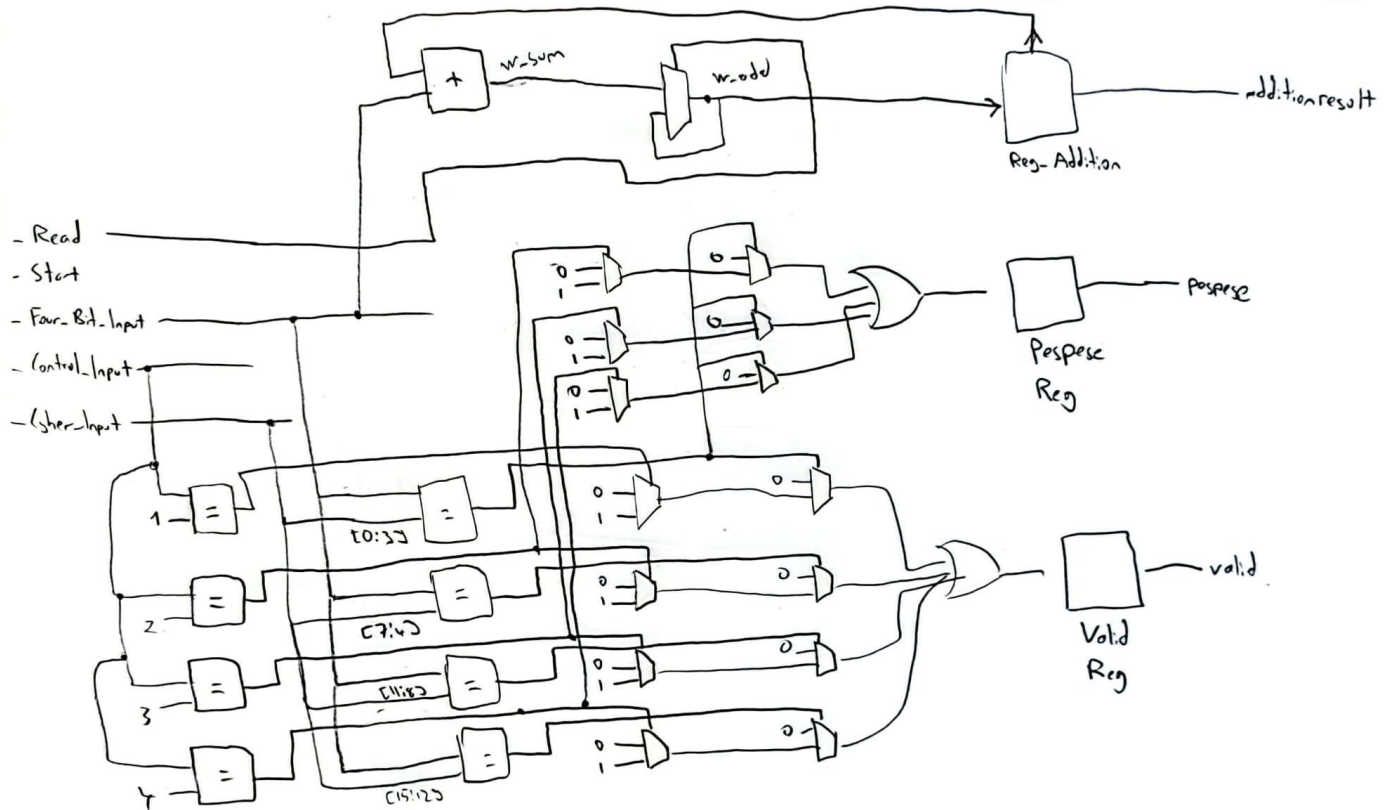


FSM:



Datapath:

Note: Datapath looks a little bit complex since I change it while coding. Sorry for complex structure. On the other hand, code is clear. You can get it from the code easily. There may be unused wires and registers in code. Ignore them.



Test and Results:

Firstly, the both test codes is in the tb.v and tb2.v files. You can test them your own.

1.)

Tb.v

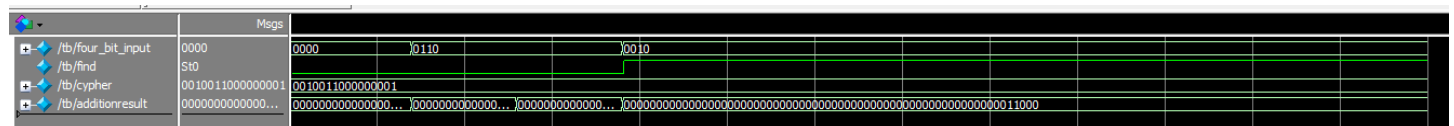
I tested your example in PDF.

Cypher was: 0010 0110 0000 0001 (Cypher is 2-6-0-1)

Give inputs respectively: 0000-0001-0011-0000-0011-0100-0001-0000-0010-0001-0001-0000-0110-0010

I expect 24 and 1 as output. One of them is sum, one of them represents whether we find the key or not.

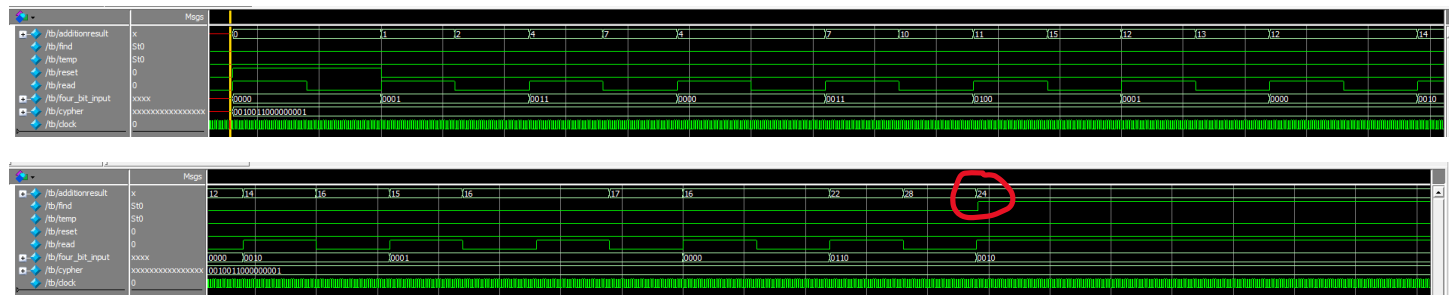
You can see those inputs in testbench file (tb.v)



As you see, at the end addition result is $11000 = 24$, and find output is 1 (True)

Code is verified.

All waves from beginning to end:



I draw a circle the critical point that *find* output is being 1.

2.)

Tb.v

I tested my own example.

Give inputs respectively: 0000 0010 1111 0010 0011 0101 1001 0000 0010 0001 0001 0010 0011 0100

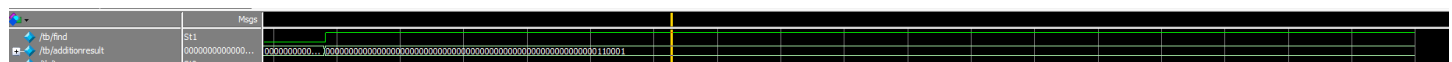
In decimal, inputs are: 0, 2, 15, 2, 3, 5, 9, 0, 2, 1, 1, 2, 3, 4

Sum of them is = 49

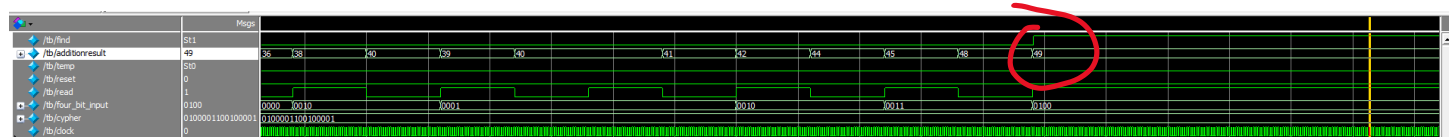
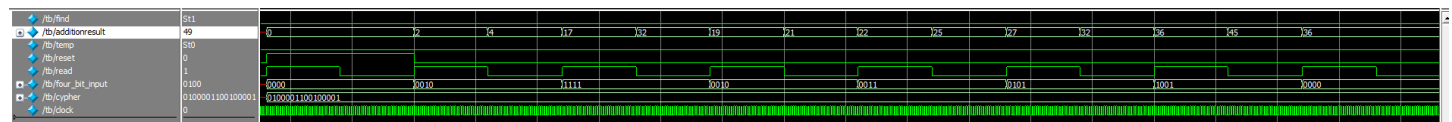
As you see the addition result in wave form, it is 110001 = 49

Also, find variable is 1 after the last input.

Code is verified.



All waves from the beginning to end:



I draw a circle the critical point that *find* output is being 1.

Notes:

- Code runs correctly as you see. It gives expected outputs. Testbenches are in the tb.v and tb2.v. You can test them on your own.
- I checked the code many times. When I update the code, updated the datapath drawing too. But still may be small differences between datapath drawing and Verilog code. I did my best. If you do not understand a point in the code or in drawings, please, contact me.
- I send all Verilog files and project files

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Best Regards.