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EE102-02

EE-102 LAB 7 REPORT: FINITE STATE MACHINE

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Purpose

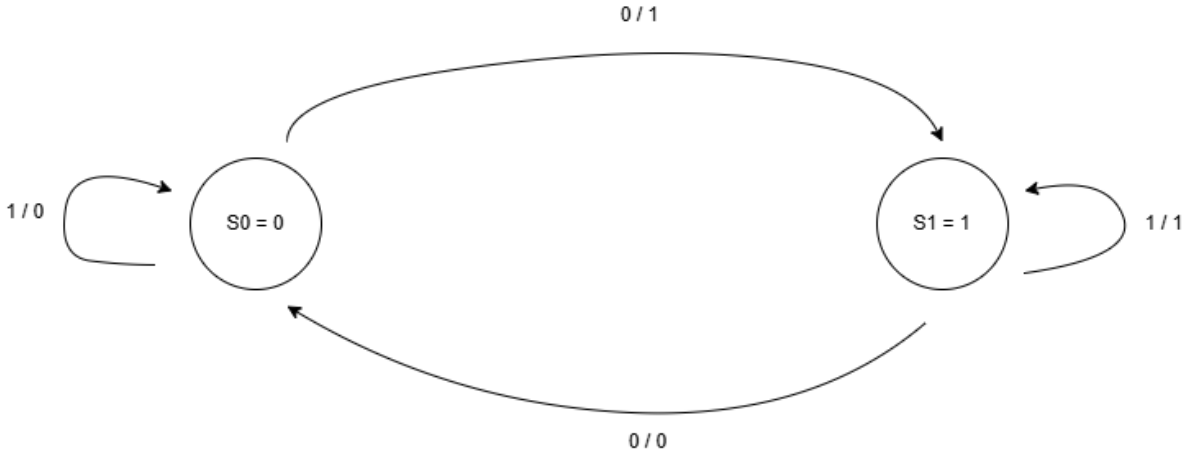
The purpose of this lab was to design an arbitrary finite state machine and implement it on the breadboard using some logic gates and D-Flipflop.

Methodology

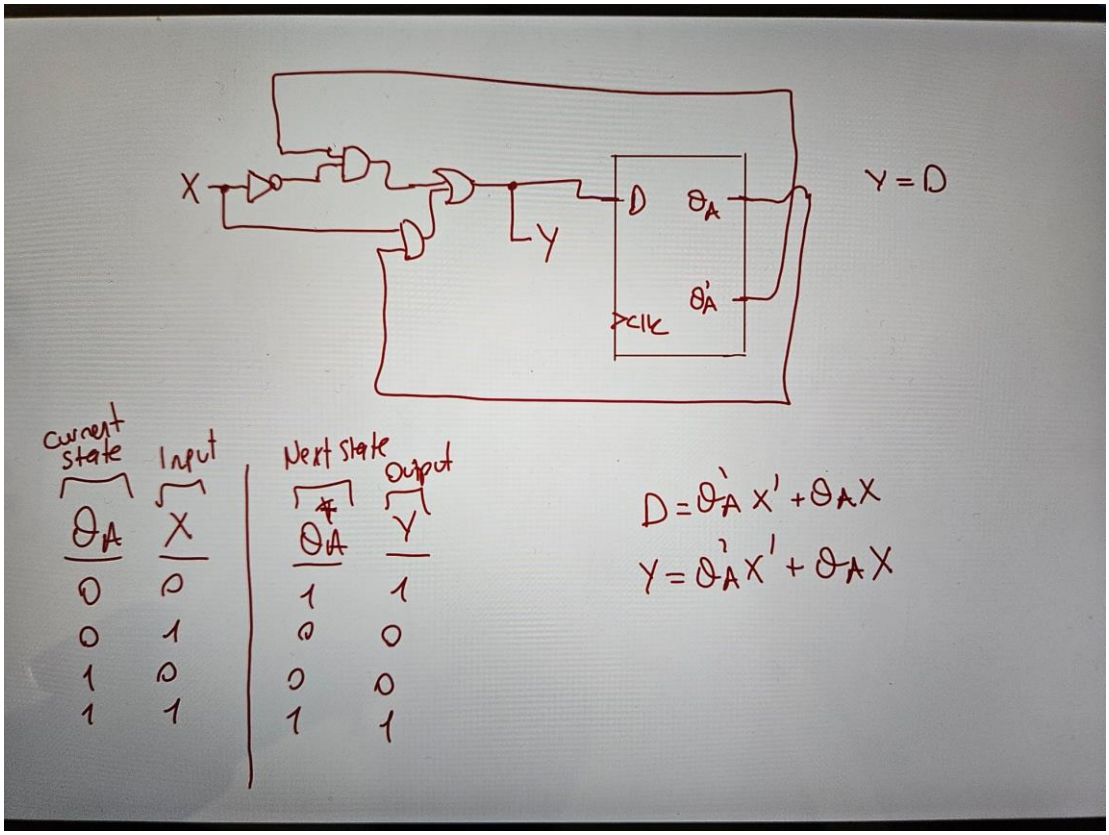
In order to create a finite state machine, first, a design was supposed to be made. To decrease complexity, a D-Flipflop and two states are used. To observe the transition between states and the output, a blue LED for the states and a red LED for the output are used. For the logic gates, a hex inverter (74 LS/HC 04), a Quad 2-input AND gate (74 LS/HC 08), and a Quad 2-input OR gate are used. For the clock of the D-Flipflop, signal function generator is connected to the clock of the D-Flipflop. 5V is provided for the power terminals and 1K ohm resistors are used for the LEDs.

Design Specifications

The system under consideration has one input, denoted by X, and one output, denoted by Y. The D input of the flip-flop is directly connected to the output Y, meaning the output of the system also determines the next state. The flip-flop's output is referred to as Qa, which represents the current state of the system. This finite state machine (FSM) operates with two distinct states: s0, corresponding to Qa = 0, and s1, corresponding to Qa = 1. The transitions between these states depend on the value of the input X, and the output Y reflects both the next state and the system's output response. The behavior of the FSM is defined by the accompanying state diagram and output table.

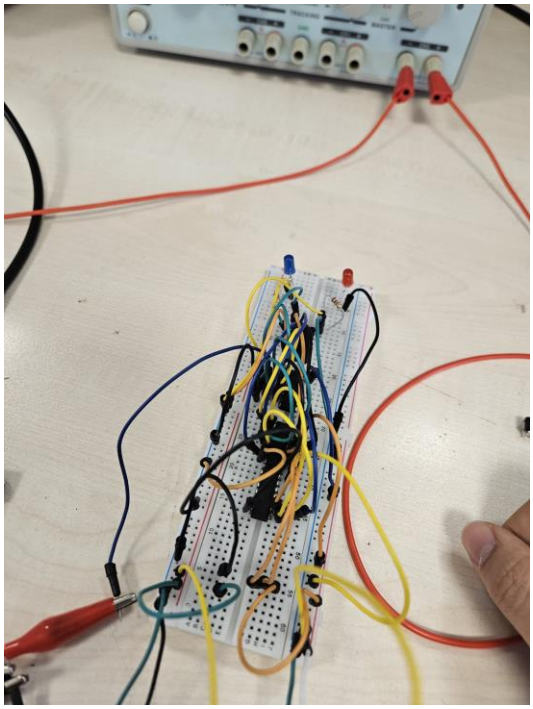


State Diagram

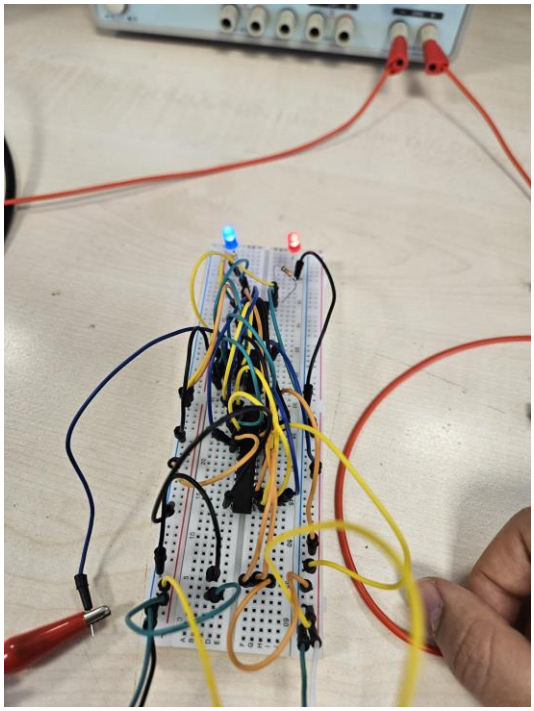


Output Table

Results



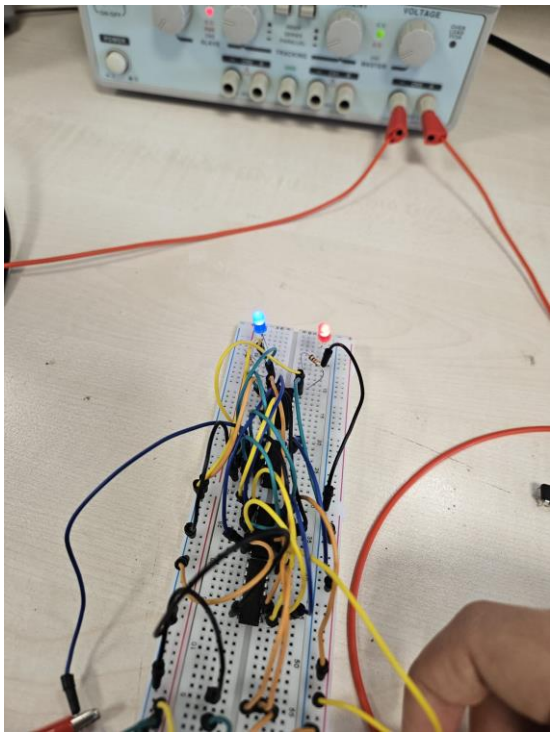
State 0, Input = 1, Output = 0



State 1, Input = 0, Output = 1

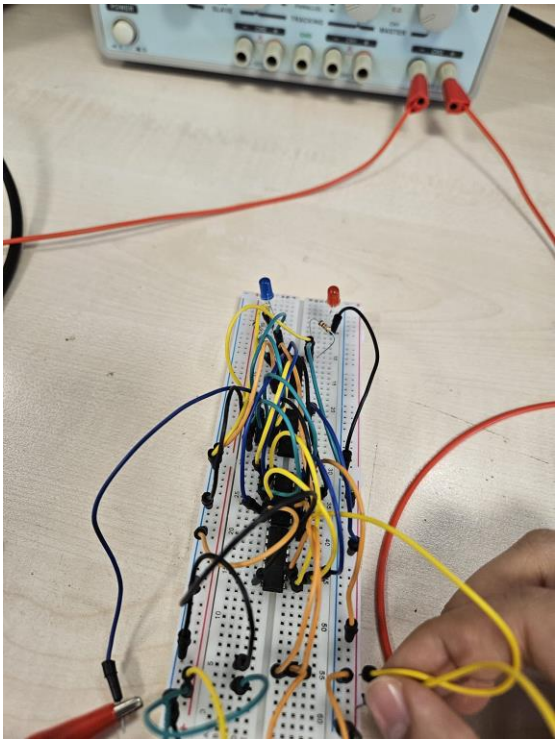
(Transition from State 0 to State 1)

Note: The blue LED indicates the current state of Qa (the output of the flip-flop), while the red LED represents the system's output Y. The input X is manually controlled by connecting it to the appropriate pins on the power terminal.



State 1, Input = 1, Output = 1

(Transition from State 0 to State 1)



State 0, Input = 0, Output = 0

Conclusion

The objective of this lab was to implement a basic FSM on breadboard to comprehend the basics of FSMs. Although I had many troubles with the not working properly flipflops, I've managed to implement the design, having a good command of the state and output diagrams of the FSMs. As a result, the lab was successful and played a critical role in understanding the basics of FSMs.

Reference

LogicGates.pdf