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EE447 – PRELIMINARY WORK 5

Video to demonstration of Q1: VIDEO1
Video to demonstration of Q3: VIDEO3

BOTH GPIO AND ADC INITIALIZATIONS ARE THE SAME FOR ALL THE THREE QUESTIONS. HOWEVER, I ADDED ALL OF THEM IN ANY CASE.

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;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;                   MAIN OF Q1                    ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;


ADC0_RIS            EQU 0x40038004  ; Interrupt status
ADC0_PSSI           EQU 0x40038028  ; Initiate sample
ADC0_SSFIFO3        EQU 0x400380A8  ; Channel 3 results ADC0_PC EQU 0x40038FC4 ; Sample rate
ADC0_ISC            EQU 0X4003800C  ;INTERRUPT STATUS AND CLEAR REGISTER

;LABEL          DIRECTIVE   VALUE               COMMENT
                AREA main,  CODE,   READONLY,   ALIGN=2
                THUMB

                IMPORT      GPIOE_Init
                IMPORT      ADC0_Init
                EXPORT      __main

;R0 STORES THE VOLTAGE VALUE BETWEEN 0X000-0XFFF

__main          PROC
                BL          GPIOE_Init
                BL          ADC0_Init

                ; start sampling routine
                LDR         R3, =ADC0_RIS       ; interrupt address
                LDR         R4, =ADC0_SSFIFO3   ; result address
                LDR         R2, =ADC0_PSSI      ; sample sequence initiate address
                LDR         R6,= ADC0_ISC
                ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
Smpl            LDR         R0, [R2]
                ORR         R0, R0, #0x08       ; set bit 3 for SS3
                STR         R0, [R2]
                ; check for sample complete (bit 3 of ADC0_RIS set)
Cont            LDR         R0, [R3]
                ANDS        R0, R0, #8
                BEQ         Cont
                ;branch fails if the flag is set so data can be read and flag is cleared
                LDR         R0,[R4]
                ;STR        R0,[R5],#4          ;store the data

                MOV         R0, #8
                STR         R0, [R6]            ; clear flag
                B           Smpl



                ENDP
                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;                    MAIN OF Q2                   ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

ADC0_RIS            EQU 0x40038004  ; Interrupt status
ADC0_PSSI           EQU 0x40038028  ; Initiate sample
ADC0_SSFIFO3        EQU 0x400380A8  ; Channel 3 results ADC0_PC EQU 0x40038FC4 ; Sample rate
ADC0_ISC            EQU 0X4003800C  ;INTERRUPT STATUS AND CLEAR REGISTER

;LABEL          DIRECTIVE   VALUE               COMMENT
                AREA main,  CODE,   READONLY,   ALIGN=2
                THUMB

                IMPORT      GPIOE_Init
                IMPORT      ADC0_Init
                EXPORT      __main

;R0 STORES THE VOLTAGE VALUES BETWEEN 0-330

__main          PROC
                BL          GPIOE_Init
                BL          ADC0_Init

                ; start sampling routine
                LDR         R3, =ADC0_RIS       ; interrupt address
                LDR         R4, =ADC0_SSFIFO3   ; result address
                LDR         R2, =ADC0_PSSI      ; sample sequence initiate address
                LDR         R6,= ADC0_ISC
                ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
Smpl            LDR         R0, [R2]
                ORR         R0, R0, #0x08       ; set bit 3 for SS3
                STR         R0, [R2]
                ; check for sample complete (bit 3 of ADC0_RIS set)
Cont            LDR         R0, [R3]
                ANDS        R0, R0, #8
                BEQ         Cont
                ;branch fails if the flag is set so data can be read and flag is cleared
                LDR         R0,[R4]
                ;STR        R0,[R5],#4          ;store the data
                LDR         R1,=0X13ACA         ;80586
                MUL         R0,R1
                LDR         R1,=0XF4240         ;1000000
                UDIV        R0,R1

                MOV         R0, #8
                STR         R0, [R6]            ; clear flag
                B           Smpl



                ENDP
                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;                    MAIN OF Q3                            ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

ADC0_RIS            EQU 0x40038004  ; Interrupt status
ADC0_PSSI           EQU 0x40038028  ; Initiate sample
ADC0_SSFIFO3        EQU 0x400380A8  ; Channel 3 results ADC0_PC EQU 0x40038FC4 ; Sample rate
ADC0_ISC            EQU 0X4003800C  ;INTERRUPT STATUS AND CLEAR REGISTER

;LABEL          DIRECTIVE   VALUE               COMMENT
                AREA main,  CODE,    READONLY,    ALIGN=2
                THUMB

                IMPORT      GPIOE_Init
                IMPORT      ADC0_Init
                IMPORT      OutChar
                EXPORT      __main

;R7 STORES THE VOLTAGE VALUES BETWEEN 0-330

__main          PROC
                BL          GPIOE_Init
                BL          ADC0_Init
                ; start sampling routine
                MOV         R7,#0               ;R7 STORES THE VOLTAGE VALUES
                ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
Smpl            LDR         R1,=ADC0_PSSI
                LDR         R0, [R1]
                ORR         R0, R0, #0x08       ; set bit 3 for SS3
                STR         R0, [R1]
                ; check for sample complete (bit 3 of ADC0_RIS set)
                LDR         R1, =ADC0_RIS
Cont            LDR         R0, [R1]
                ANDS        R0, R0, #8
                BEQ         Cont
                ;branch fails if the flag is set so data can be read and flag is cleared
                LDR         R1, =ADC0_SSFIFO3
                LDR         R0,[R1]
                ;STR        R0,[R5],#4          ;store the data
                LDR         R1, =0X13ACA            ;80586
                MUL         R0, R1
                LDR         R1, =0XF4240            ;1000000
                UDIV        R0, R1
                CMP         R0, R7
                BEQ         EXIT
                SUBHI       R2, R0,R7
                SUBLO       R2, R7,R0
                CMP         R2, #0X14           ;IF THE CHANGE IS HIGHER THAN 0.2V PRINT
                BLO         EXIT

PRINT           CPY         R7, R0              ;UPDATE R7
                MOV         R10,#100
                UDIV        R5, R0, R10
                MUL         R1, R5,R10
                SUB         R0, R1
                ADD         R5, #48
                BL          OutChar
                LDR         R5, =0X2E
                BL          OutChar
                MOV         R10,#10
                UDIV        R5, R0, R10
                MUL         R1,R5,R10
                SUB         R0,R1
                ADD         R5, #48
                BL          OutChar
                CPY         R5,R0
                ADD         R5, #48
                BL          OutChar
                MOV         R5, #0X0A
                BL          OutChar

EXIT            MOV         R0, #8
                LDR         R1, =ADC0_ISC
                STR         R0, [R1]            ; clear flag
                B           Smpl
```

```
78
79                      ENDP
80                      END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;           GPIO PORTE INITIALIZATION OF Q1        ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

PE_INP              EQU     0X40024020 ;0000_0010_0000
GPIO_PORTE_DIR_R    EQU     0X40024400
GPIO_PORTE_AFSEL_R  EQU     0X40024420
GPIO_PORTE_DEN_R    EQU     0X4002451C
GPIO_PORTE_AMSEL_R  EQU     0X40024528
GPIO_PORTE_PDR      EQU     0X40024514 ;514
SYSCTL_RCGC2_R      EQU     0X400FE608
GPIO_PORTE_IS       EQU     0X40024404
GPIO_PORTE_IBE      EQU     0X40024408
GPIO_PORTE_IEV      EQU     0X4002440C
GPIO_PORTE_IM       EQU     0X40024410
GPIO_PORTE_ICR      EQU     0X4002441C
GPIO_PORTE_RIS      EQU     0X40024414
RCGCADC             EQU 0x400FE638 ; ADC clock register



;LABEL          DIRECTIVE   VALUE               COMMENT
                AREA init_gpio, CODE,    READONLY,    ALIGN=2
                THUMB

                EXPORT      GPIOE_Init

;ADC CLOCK IS THE FIRST THING INITIALIZED. OTHERWISE IT GIVES ERROR.

GPIOE_Init  PROC
    ;ACTIVATE ADC CLOCK
            LDR         R1, =RCGCADC     ; Turn on ADC clock
            LDR         R0, [R1]
            ORR         R0, R0, #0x01    ; set bit 0 to enable ADC0 clock
            STR         R0, [R1]
            NOP
            NOP
            NOP
    ;ACTIVATE PORTE CLOCK
            LDR     R1,=SYSCTL_RCGC2_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X10 ;only port E
            STR     R0,[R1]
            NOP
            NOP
            NOP
    ;SET DIRECTION REGISTER
            LDR     R1,=GPIO_PORTE_DIR_R
            LDR     R0,[R1]
            BIC     R0,R0,#0X08         ;PE3 IS INPUT
            STR     R0,[R1]
    ;REGULAR PORT FUNCTION
            LDR     R1,=GPIO_PORTE_AFSEL_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X08         ;PE3 IS ALTERNATE
            STR     R0,[R1]
    ;PULLDOWN RESISTORS ON SWITCH PINS
            ;LDR        R1,=GPIO_PORTE_PDR
            ;MOV        R0,#0X0F
            ;STR        R0,[R1]
    ;DISABLE DIGITAL PORT
            LDR     R1,=GPIO_PORTE_DEN_R
            LDR     R0,[R1]
            BIC     R0,R0,#0X08
            STR     R0,[R1]
    ;ENABLE ANALOG PORT
            LDR     R1,=GPIO_PORTE_AMSEL_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X08
            STR     R0,[R1]
    ;CONFIGURE INTERRUPT FOR PORTE PINS 0-3=INPUT
            ;LDR        R1,=GPIO_PORTE_IS
            ;LDR        R2,=GPIO_PORTE_IBE
            ;LDR        R3,=GPIO_PORTE_IEV
            ;LDR        R4,=GPIO_PORTE_IM
            ;LDR        R5,=GPIO_PORTE_ICR

```

```
78                ;MOV         R0,#0X00
79                ;STR         R0,[R1]
80                ;STR         R0,[R2]
81                ;MOV         R0,#0X0F
82                ;STR         R0,[R3]
83                ;STR         R0,[R4]
84                ;STR         R0,[R5]
85
86        ;CONFIGURE NVIC
87                ;LDR         R1,=NVIC_ISER0
88                ;LDR         R0,[R1]
89                ;ORR         R0,R0,#02
90                ;STR         R0,[R1]
91                ;CPSIE  I
92
93
94                BX      LR
95                ENDP
96                ALIGN
97                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;          ADC0 INITIALIZATION OF Q1              ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

RCGCADC             EQU 0x400FE638 ; ADC clock register
; ADC0 base address EQU 0x40038000
ADC0_ACTSS          EQU 0x40038000 ; Sample sequencer (ADC0 base address)
ADC0_RIS            EQU 0x40038004 ; Interrupt status
ADC0_IM             EQU 0x40038008 ; Interrupt select
ADC0_EMUX           EQU 0x40038014 ; Trigger select
ADC0_PSSI           EQU 0x40038028 ; Initiate sample
ADC0_SSMUX3         EQU 0x400380A0 ; Input channel select
ADC0_SSCTL3         EQU 0x400380A4 ; Sample sequence control
ADC0_SSFIFO3        EQU 0x400380A8 ; Channel 3 results
ADC0_PC             EQU 0x40038FC4 ; Sample rate


;LABEL          DIRECTIVE   VALUE           COMMENT
                AREA init_adc,  CODE,   READONLY,   ALIGN=2
                THUMB

                EXPORT      ADC0_Init

ADC0_Init       PROC
                ;ADC CLOCK IS INITIALIZED IN PORTE INITIALIZATION.
                ;LDR        R1, =RCGCADC    ; Turn on ADC clock
                ;LDR        R0, [R1]
                ;ORR        R0, R0, #0x01   ; set bit 0 to enable ADC0 clock
                ;STR        R0, [R1]
                ;NOP
                ;NOP
                ;NOP
                        ; Let clock stabilize
                ; Disable sequencer while ADC setup
                LDR         R1, =ADC0_ACTSS
                LDR         R0, [R1]
                BIC         R0, R0, #0x08   ; clear bit 3 to disable seq 3
                STR         R0, [R1]
                ; Select trigger source
                LDR         R1, =ADC0_EMUX
                LDR         R0, [R1]
                BIC         R0, R0, #0xF000 ; clear bits 15:12 to select SOFTWARE
                STR         R0, [R1] ; trigger
                ; Select input channel
                LDR         R1, =ADC0_SSMUX3
                LDR         R0, [R1]
                BIC         R0, R0, #0x000F ; clear bits 3:0 to select AIN0
                STR         R0, [R1]
                ; Config sample sequence
                LDR         R1, =ADC0_SSCTL3
                LDR         R0, [R1]
                ORR         R0, R0, #0x06   ; set bits 2:1 (IE0, END0)
                STR         R0, [R1]
                ; Set sample rate
                LDR         R1, =ADC0_PC
                LDR         R0, [R1]
                ORR         R0, R0, #0x01   ; set bits 3:0 to 1 for 125k sps
                STR         R0, [R1]
                ; Done with setup, enable sequencer
                LDR         R1, =ADC0_ACTSS
                LDR         R0, [R1]
                ORR         R0, R0, #0x08   ; set bit 3 to enable seq 3
                STR         R0, [R1]        ; sampling enabled but not initiated yet

                BX          LR
                ENDP
                ALIGN
                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;           GPIO PORTE INITIALIZATION OF Q2        ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

PE_INP              EQU     0X40024020 ;0000_0010_0000
GPIO_PORTE_DIR_R    EQU     0X40024400
GPIO_PORTE_AFSEL_R  EQU     0X40024420
GPIO_PORTE_DEN_R    EQU     0X4002451C
GPIO_PORTE_AMSEL_R  EQU     0X40024528
GPIO_PORTE_PDR      EQU     0X40024514 ;514
SYSCTL_RCGC2_R      EQU     0X400FE608
GPIO_PORTE_IS       EQU     0X40024404
GPIO_PORTE_IBE      EQU     0X40024408
GPIO_PORTE_IEV      EQU     0X4002440C
GPIO_PORTE_IM       EQU     0X40024410
GPIO_PORTE_ICR      EQU     0X4002441C
GPIO_PORTE_RIS      EQU     0X40024414
RCGCADC             EQU 0x400FE638 ; ADC clock register



;LABEL          DIRECTIVE   VALUE               COMMENT
                AREA init_gpio, CODE,    READONLY,    ALIGN=2
                THUMB

                EXPORT      GPIOE_Init

;ADC CLOCK IS THE FIRST THING INITIALIZED. OTHERWISE IT GIVES ERROR.

GPIOE_Init  PROC
    ;ACTIVATE ADC CLOCK
            LDR         R1, =RCGCADC     ; Turn on ADC clock
            LDR         R0, [R1]
            ORR         R0, R0, #0x01    ; set bit 0 to enable ADC0 clock
            STR         R0, [R1]
            NOP
            NOP
            NOP
    ;ACTIVATE PORTE CLOCK
            LDR     R1,=SYSCTL_RCGC2_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X10 ;only port E
            STR     R0,[R1]
            NOP
            NOP
            NOP
    ;SET DIRECTION REGISTER
            LDR     R1,=GPIO_PORTE_DIR_R
            LDR     R0,[R1]
            BIC     R0,R0,#0X08         ;PE3 IS INPUT
            STR     R0,[R1]
    ;REGULAR PORT FUNCTION
            LDR     R1,=GPIO_PORTE_AFSEL_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X08         ;PE3 IS ALTERNATE
            STR     R0,[R1]
    ;PULLDOWN RESISTORS ON SWITCH PINS
            ;LDR        R1,=GPIO_PORTE_PDR
            ;MOV        R0,#0X0F
            ;STR        R0,[R1]
    ;DISABLE DIGITAL PORT
            LDR     R1,=GPIO_PORTE_DEN_R
            LDR     R0,[R1]
            BIC     R0,R0,#0X08
            STR     R0,[R1]
    ;ENABLE ANALOG PORT
            LDR     R1,=GPIO_PORTE_AMSEL_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X08
            STR     R0,[R1]
    ;CONFIGURE INTERRUPT FOR PORTE PINS 0-3=INPUT
            ;LDR        R1,=GPIO_PORTE_IS
            ;LDR        R2,=GPIO_PORTE_IBE
            ;LDR        R3,=GPIO_PORTE_IEV
            ;LDR        R4,=GPIO_PORTE_IM
            ;LDR        R5,=GPIO_PORTE_ICR

```

```
78                ;MOV         R0,#0X00
79                ;STR         R0,[R1]
80                ;STR         R0,[R2]
81                ;MOV         R0,#0X0F
82                ;STR         R0,[R3]
83                ;STR         R0,[R4]
84                ;STR         R0,[R5]
85
86        ;CONFIGURE NVIC
87                ;LDR         R1,=NVIC_ISER0
88                ;LDR         R0,[R1]
89                ;ORR         R0,R0,#02
90                ;STR         R0,[R1]
91                ;CPSIE  I
92
93
94                BX      LR
95                ENDP
96                ALIGN
97                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;          ADC0 INITIALIZATION OF Q2                ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

RCGCADC             EQU 0x400FE638 ; ADC clock register
; ADC0 base address EQU 0x40038000
ADC0_ACTSS          EQU 0x40038000 ; Sample sequencer (ADC0 base address)
ADC0_RIS            EQU 0x40038004 ; Interrupt status
ADC0_IM             EQU 0x40038008 ; Interrupt select
ADC0_EMUX           EQU 0x40038014 ; Trigger select
ADC0_PSSI           EQU 0x40038028 ; Initiate sample
ADC0_SSMUX3         EQU 0x400380A0 ; Input channel select
ADC0_SSCTL3         EQU 0x400380A4 ; Sample sequence control
ADC0_SSFIFO3        EQU 0x400380A8 ; Channel 3 results
ADC0_PC             EQU 0x40038FC4 ; Sample rate


;LABEL          DIRECTIVE   VALUE              COMMENT
                AREA init_adc,  CODE,   READONLY,   ALIGN=2
                THUMB

                EXPORT      ADC0_Init

ADC0_Init       PROC
                ;ADC CLOCK IS INITIALIZED IN PORTE INITIALIZATION.
                ;LDR        R1, =RCGCADC    ; Turn on ADC clock
                ;LDR        R0, [R1]
                ;ORR        R0, R0, #0x01   ; set bit 0 to enable ADC0 clock
                ;STR        R0, [R1]
                ;NOP
                ;NOP
                ;NOP
                        ; Let clock stabilize
                ; Disable sequencer while ADC setup
                LDR         R1, =ADC0_ACTSS
                LDR         R0, [R1]
                BIC         R0, R0, #0x08   ; clear bit 3 to disable seq 3
                STR         R0, [R1]
                ; Select trigger source
                LDR         R1, =ADC0_EMUX
                LDR         R0, [R1]
                BIC         R0, R0, #0xF000 ; clear bits 15:12 to select SOFTWARE
                STR         R0, [R1] ; trigger
                ; Select input channel
                LDR         R1, =ADC0_SSMUX3
                LDR         R0, [R1]
                BIC         R0, R0, #0x000F ; clear bits 3:0 to select AIN0
                STR         R0, [R1]
                ; Config sample sequence
                LDR         R1, =ADC0_SSCTL3
                LDR         R0, [R1]
                ORR         R0, R0, #0x06   ; set bits 2:1 (IE0, END0)
                STR         R0, [R1]
                ; Set sample rate
                LDR         R1, =ADC0_PC
                LDR         R0, [R1]
                ORR         R0, R0, #0x01   ; set bits 3:0 to 1 for 125k sps
                STR         R0, [R1]
                ; Done with setup, enable sequencer
                LDR         R1, =ADC0_ACTSS
                LDR         R0, [R1]
                ORR         R0, R0, #0x08   ; set bit 3 to enable seq 3
                STR         R0, [R1]        ; sampling enabled but not initiated yet

                BX          LR
                ENDP
                ALIGN
                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;          GPIO PORTE INITIALIZATION OF Q3       ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

PE_INP             EQU     0X40024020 ;0000_0010_0000
GPIO_PORTE_DIR_R   EQU     0X40024400
GPIO_PORTE_AFSEL_R EQU     0X40024420
GPIO_PORTE_DEN_R   EQU     0X4002451C
GPIO_PORTE_AMSEL_R EQU     0X40024528
GPIO_PORTE_PDR     EQU     0X40024514 ;514
SYSCTL_RCGC2_R     EQU     0X400FE608
GPIO_PORTE_IS      EQU     0X40024404
GPIO_PORTE_IBE     EQU     0X40024408
GPIO_PORTE_IEV     EQU     0X4002440C
GPIO_PORTE_IM      EQU     0X40024410
GPIO_PORTE_ICR     EQU     0X4002441C
GPIO_PORTE_RIS     EQU     0X40024414
RCGCADC            EQU 0x400FE638 ; ADC clock register



;LABEL           DIRECTIVE    VALUE              COMMENT
                 AREA init_gpio, CODE,    READONLY,    ALIGN=2
                 THUMB

                 EXPORT       GPIOE_Init

;ADC CLOCK IS THE FIRST THING INITIALIZED. OTHERWISE IT GIVES ERROR.

GPIOE_Init   PROC
    ;ACTIVATE ADC CLOCK
            LDR         R1, =RCGCADC     ; Turn on ADC clock
            LDR         R0, [R1]
            ORR         R0, R0, #0x01    ; set bit 0 to enable ADC0 clock
            STR         R0, [R1]
            NOP
            NOP
            NOP
    ;ACTIVATE PORTE CLOCK
            LDR     R1,=SYSCTL_RCGC2_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X10 ;only port E
            STR     R0,[R1]
            NOP
            NOP
            NOP
    ;SET DIRECTION REGISTER
            LDR     R1,=GPIO_PORTE_DIR_R
            LDR     R0,[R1]
            BIC     R0,R0,#0X08          ;PE3 IS INPUT
            STR     R0,[R1]
    ;REGULAR PORT FUNCTION
            LDR     R1,=GPIO_PORTE_AFSEL_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X08          ;PE3 IS ALTERNATE
            STR     R0,[R1]
    ;PULLDOWN RESISTORS ON SWITCH PINS
            ;LDR        R1,=GPIO_PORTE_PDR
            ;MOV        R0,#0X0F
            ;STR        R0,[R1]
    ;DISABLE DIGITAL PORT
            LDR     R1,=GPIO_PORTE_DEN_R
            LDR     R0,[R1]
            BIC     R0,R0,#0X08
            STR     R0,[R1]
    ;ENABLE ANALOG PORT
            LDR     R1,=GPIO_PORTE_AMSEL_R
            LDR     R0,[R1]
            ORR     R0,R0,#0X08
            STR     R0,[R1]
    ;CONFIGURE INTERRUPT FOR PORTE PINS 0-3=INPUT
            ;LDR        R1,=GPIO_PORTE_IS
            ;LDR        R2,=GPIO_PORTE_IBE
            ;LDR        R3,=GPIO_PORTE_IEV
            ;LDR        R4,=GPIO_PORTE_IM
            ;LDR        R5,=GPIO_PORTE_ICR

```

```
78                ;MOV         R0,#0X00
79                ;STR         R0,[R1]
80                ;STR         R0,[R2]
81                ;MOV         R0,#0X0F
82                ;STR         R0,[R3]
83                ;STR         R0,[R4]
84                ;STR         R0,[R5]
85
86        ;CONFIGURE NVIC
87                ;LDR         R1,=NVIC_ISER0
88                ;LDR         R0,[R1]
89                ;ORR         R0,R0,#02
90                ;STR         R0,[R1]
91                ;CPSIE  I
92
93
94                BX      LR
95                ENDP
96                ALIGN
97                END
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;          ADC0 INITIALIZATION OF Q3               ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

RCGCADC             EQU 0x400FE638 ; ADC clock register
; ADC0 base address EQU 0x40038000
ADC0_ACTSS          EQU 0x40038000 ; Sample sequencer (ADC0 base address)
ADC0_RIS            EQU 0x40038004 ; Interrupt status
ADC0_IM             EQU 0x40038008 ; Interrupt select
ADC0_EMUX           EQU 0x40038014 ; Trigger select
ADC0_PSSI           EQU 0x40038028 ; Initiate sample
ADC0_SSMUX3         EQU 0x400380A0 ; Input channel select
ADC0_SSCTL3         EQU 0x400380A4 ; Sample sequence control
ADC0_SSFIFO3        EQU 0x400380A8 ; Channel 3 results
ADC0_PC             EQU 0x40038FC4 ; Sample rate


;LABEL          DIRECTIVE   VALUE               COMMENT
                AREA init_adc,  CODE,    READONLY,    ALIGN=2
                THUMB

                EXPORT      ADC0_Init

ADC0_Init       PROC
                ;ADC CLOCK IS INITIALIZED IN PORTE INITIALIZATION.
                ;LDR        R1, =RCGCADC    ; Turn on ADC clock
                ;LDR        R0, [R1]
                ;ORR        R0, R0, #0x01   ; set bit 0 to enable ADC0 clock
                ;STR        R0, [R1]
                ;NOP
                ;NOP
                ;NOP
                        ; Let clock stabilize
                ; Disable sequencer while ADC setup
                LDR         R1, =ADC0_ACTSS
                LDR         R0, [R1]
                BIC         R0, R0, #0x08   ; clear bit 3 to disable seq 3
                STR         R0, [R1]
                ; Select trigger source
                LDR         R1, =ADC0_EMUX
                LDR         R0, [R1]
                BIC         R0, R0, #0xF000 ; clear bits 15:12 to select SOFTWARE
                STR         R0, [R1] ; trigger
                ; Select input channel
                LDR         R1, =ADC0_SSMUX3
                LDR         R0, [R1]
                BIC         R0, R0, #0x000F ; clear bits 3:0 to select AIN0
                STR         R0, [R1]
                ; Config sample sequence
                LDR         R1, =ADC0_SSCTL3
                LDR         R0, [R1]
                ORR         R0, R0, #0x06   ; set bits 2:1 (IE0, END0)
                STR         R0, [R1]
                ; Set sample rate
                LDR         R1, =ADC0_PC
                LDR         R0, [R1]
                ORR         R0, R0, #0x01   ; set bits 3:0 to 1 for 125k sps
                STR         R0, [R1]
                ; Done with setup, enable sequencer
                LDR         R1, =ADC0_ACTSS
                LDR         R0, [R1]
                ORR         R0, R0, #0x08   ; set bit 3 to enable seq 3
                STR         R0, [R1]        ; sampling enabled but not initiated yet

                BX          LR
                ENDP
                ALIGN
                END
```