

EE447 – PRELIMINARY WORK 5

Video to demonstration of Q1: [VIDEO1](#)

Video to demonstration of Q3: [VIDEO3](#)

BOTH GPIO AND ADC INITIALIZATIONS ARE THE SAME FOR ALL THE THREE QUESTIONS. HOWEVER, I ADDED ALL OF THEM IN ANY CASE.

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1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;                      MAIN OF Q1                      ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5
6  ADC0_RIS            EQU 0x40038004 ; Interrupt status
7  ADC0_PSSI          EQU 0x40038028 ; Initiate sample
8  ADC0_SSIFO3        EQU 0x400380A8 ; Channel 3 results ADC0_PC EQU 0x40038FC4 ; Sample rate
9  ADC0_ISC           EQU 0x4003800C ; INTERRUPT STATUS AND CLEAR REGISTER
10
11 ;LABEL              DIRECTIVE  VALUE                      COMMENT
12 AREA main, CODE, READONLY, ALIGN=2
13 THUMB
14
15 IMPORT              GPIOE_Init
16 IMPORT              ADC0_Init
17 EXPORT              __main
18
19 ;R0 STORES THE VOLTAGE VALUE BETWEEN 0X000-0XFFF
20
21 __main              PROC
22 BL                  GPIOE_Init
23 BL                  ADC0_Init
24
25 ; start sampling routine
26 LDR                 R3, =ADC0_RIS ; interrupt address
27 LDR                 R4, =ADC0_SSIFO3 ; result address
28 LDR                 R2, =ADC0_PSSI ; sample sequence initiate address
29 LDR                 R6, =ADC0_ISC
30 ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
31 Smp1                LDR                 R0, [R2]
32 ORR                 R0, R0, #0x08 ; set bit 3 for SS3
33 STR                 R0, [R2]
34 ; check for sample complete (bit 3 of ADC0_RIS set)
35 Cont                LDR                 R0, [R3]
36 ANDS                R0, R0, #8
37 BEQ                 Cont
38 ;branch fails if the flag is set so data can be read and flag is cleared
39 LDR                 R0, [R4]
40 ;STR                 R0, [R5], #4 ;store the data
41
42 MOV                 R0, #8
43 STR                 R0, [R6] ; clear flag
44 B                   Smp1
45
46
47
48 ENDP
49 END

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1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;                      MAIN OF Q2                      ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  ADC0_RIS                EQU 0x40038004 ; Interrupt status
6  ADC0_PSSI               EQU 0x40038028 ; Initiate sample
7  ADC0_SSFI03             EQU 0x400380A8 ; Channel 3 results ADC0_PC EQU 0x40038FC4 ; Sample rate
8  ADC0_ISC                EQU 0x4003800C ; INTERRUPT STATUS AND CLEAR REGISTER
9
10 ; LABEL                DIRECTIVE  VALUE                COMMENT
11 ;                      AREA main, CODE, READONLY, ALIGN=2
12 ;                      THUMB
13
14 ;                      IMPORT      GPIOE_Init
15 ;                      IMPORT      ADC0_Init
16 ;                      EXPORT      __main
17
18 ;R0 STORES THE VOLTAGE VALUES BETWEEN 0-330
19
20 __main                  PROC
21 ;                      BL          GPIOE_Init
22 ;                      BL          ADC0_Init
23
24 ; start sampling routine
25 LDR                     R3, =ADC0_RIS ; interrupt address
26 LDR                     R4, =ADC0_SSFI03 ; result address
27 LDR                     R2, =ADC0_PSSI ; sample sequence initiate address
28 LDR                     R6, =ADC0_ISC
29 ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
30 Smpl LDR                 R0, [R2]
31 ORR                     R0, R0, #0x08 ; set bit 3 for SS3
32 STR                     R0, [R2]
33 ; check for sample complete (bit 3 of ADC0_RIS set)
34 Cont LDR                 R0, [R3]
35 ANDS                    R0, R0, #8
36 BEQ                     Cont
37 ;branch fails if the flag is set so data can be read and flag is cleared
38 LDR                     R0, [R4]
39 ;STR                     R0, [R5], #4 ;store the data
40 LDR                     R1, =0X13ACA ;80586
41 MUL                     R0, R1
42 LDR                     R1, =0XF4240 ;1000000
43 UDIV                    R0, R1
44
45 MOV                     R0, #8
46 STR                     R0, [R6] ; clear flag
47 B                       Smpl
48
49
50
51 ENDP
52 END

```

```

1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;                      MAIN OF Q3                      ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  ADC0_RIS                EQU 0x40038004  ; Interrupt status
6  ADC0_PSSI               EQU 0x40038028  ; Initiate sample
7  ADC0_SSFIFO3            EQU 0x400380A8  ; Channel 3 results ADC0_PC EQU 0x40038FC4 ; Sample rate
8  ADC0_ISC                EQU 0x4003800C  ; INTERRUPT STATUS AND CLEAR REGISTER
9
10 ;LABEL                  DIRECTIVE    VALUE                      COMMENT
11                          AREA main,  CODE,      READONLY,      ALIGN=2
12                          THUMB
13
14                          IMPORT        GPIOE_Init
15                          IMPORT        ADC0_Init
16                          IMPORT        OutChar
17                          EXPORT        __main
18
19 ;R7 STORES THE VOLTAGE VALUES BETWEEN 0-330
20
21 __main                   PROC
22                          BL            GPIOE_Init
23                          BL            ADC0_Init
24                          ; start sampling routine
25                          MOV          R7, #0                      ;R7 STORES THE VOLTAGE VALUES
26                          ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
27 Smpl                     LDR          R1, =ADC0_PSSI
28                          LDR          R0, [R1]
29                          ORR          R0, R0, #0x08              ; set bit 3 for SS3
30                          STR          R0, [R1]
31                          ; check for sample complete (bit 3 of ADC0_RIS set)
32                          LDR          R1, =ADC0_RIS
33 Cont                     LDR          R0, [R1]
34                          ANDS         R0, R0, #8
35                          BEQ          Cont
36                          ;branch fails if the flag is set so data can be read and flag is cleared
37                          LDR          R1, =ADC0_SSFIFO3
38                          LDR          R0, [R1]
39                          ;STR        R0, [R5], #4                ;store the data
40                          LDR          R1, =0x13ACA                ;80586
41                          MUL          R0, R1
42                          LDR          R1, =0xF4240                ;1000000
43                          UDIV         R0, R1
44                          CMP          R0, R7
45                          BEQ          EXIT
46                          SUBHI        R2, R0, R7
47                          SUBLO        R2, R7, R0
48                          CMP          R2, #0x14                  ;IF THE CHANGE IS HIGHER THAN 0.2V PRINT
49                          BLO          EXIT
50
51 PRINT                    CPY          R7, R0                      ;UPDATE R7
52                          MOV          R10, #100
53                          UDIV         R5, R0, R10
54                          MUL          R1, R5, R10
55                          SUB          R0, R1
56                          ADD          R5, #48
57                          BL            OutChar
58                          LDR          R5, =0x2E
59                          BL            OutChar
60                          MOV          R10, #10
61                          UDIV         R5, R0, R10
62                          MUL          R1, R5, R10
63                          SUB          R0, R1
64                          ADD          R5, #48
65                          BL            OutChar
66                          CPY          R5, R0
67                          ADD          R5, #48
68                          BL            OutChar
69                          MOV          R5, #0x0A
70                          BL            OutChar
71
72 EXIT                     MOV          R0, #8
73                          LDR          R1, =ADC0_ISC
74                          STR          R0, [R1]                    ; clear flag
75                          B            Smpl
76
77

```

```
78  
79         ENDP  
80     END
```

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1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;          GPIO PORTE INITIALIZATION OF Q1          ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  PE_INP          EQU      0X40024020 ;0000_0010_0000
6  GPIO_PORTE_DIR_R    EQU      0X40024400
7  GPIO_PORTE_AFSEL_R  EQU      0X40024420
8  GPIO_PORTE_DEN_R    EQU      0X4002451C
9  GPIO_PORTE_AMSEL_R  EQU      0X40024528
10 GPIO_PORTE_PDR      EQU      0X40024514 ;514
11 SYSCTL_RCGC2_R      EQU      0X400FE608
12 GPIO_PORTE_IS       EQU      0X40024404
13 GPIO_PORTE_IBE       EQU      0X40024408
14 GPIO_PORTE_IEV       EQU      0X4002440C
15 GPIO_PORTE_IM        EQU      0X40024410
16 GPIO_PORTE_ICR       EQU      0X4002441C
17 GPIO_PORTE_RIS       EQU      0X40024414
18 RCGCADC            EQU 0x400FE638 ; ADC clock register
19
20
21
22 ;LABEL            DIRECTIVE    VALUE                COMMENT
23                 AREA init_gpio, CODE,    READONLY,    ALIGN=2
24                 THUMB
25
26                 EXPORT          GPIOE_Init
27
28 ;ADC CLOCK IS THE FIRST THING INITIALIZED. OTHERWISE IT GIVES ERROR.
29
30 GPIOE_Init  PROC
31     ;ACTIVATE ADC CLOCK
32     LDR      R1, =RCGCADC      ; Turn on ADC clock
33     LDR      R0, [R1]
34     ORR      R0, R0, #0x01     ; set bit 0 to enable ADC0 clock
35     STR      R0, [R1]
36     NOP
37     NOP
38     NOP
39     ;ACTIVATE PORTE CLOCK
40     LDR      R1,=SYSCTL_RCGC2_R
41     LDR      R0, [R1]
42     ORR      R0,R0,#0x10 ;only port E
43     STR      R0, [R1]
44     NOP
45     NOP
46     NOP
47     ;SET DIRECTION REGISTER
48     LDR      R1,=GPIO_PORTE_DIR_R
49     LDR      R0, [R1]
50     BIC      R0,R0,#0x08      ;PE3 IS INPUT
51     STR      R0, [R1]
52     ;REGULAR PORT FUNCTION
53     LDR      R1,=GPIO_PORTE_AFSEL_R
54     LDR      R0, [R1]
55     ORR      R0,R0,#0x08      ;PE3 IS ALTERNATE
56     STR      R0, [R1]
57     ;PULLDOWN RESISTORS ON SWITCH PINS
58     ;LDR      R1,=GPIO_PORTE_PDR
59     ;MOV      R0,#0X0F
60     ;STR      R0, [R1]
61     ;DISABLE DIGITAL PORT
62     LDR      R1,=GPIO_PORTE_DEN_R
63     LDR      R0, [R1]
64     BIC      R0,R0,#0x08
65     STR      R0, [R1]
66     ;ENABLE ANALOG PORT
67     LDR      R1,=GPIO_PORTE_AMSEL_R
68     LDR      R0, [R1]
69     ORR      R0,R0,#0x08
70     STR      R0, [R1]
71     ;CONFIGURE INTERRUPT FOR PORTE PINS 0-3=INPUT
72     ;LDR      R1,=GPIO_PORTE_IS
73     ;LDR      R2,=GPIO_PORTE_IBE
74     ;LDR      R3,=GPIO_PORTE_IEV
75     ;LDR      R4,=GPIO_PORTE_IM
76     ;LDR      R5,=GPIO_PORTE_ICR
77

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```
78             ;MOV      R0,#0X00
79             ;STR      R0,[R1]
80             ;STR      R0,[R2]
81             ;MOV      R0,#0X0F
82             ;STR      R0,[R3]
83             ;STR      R0,[R4]
84             ;STR      R0,[R5]
85
86             ;CONFIGURE NVIC
87             ;LDR      R1,=NVIC_ISERO
88             ;LDR      R0,[R1]
89             ;ORR      R0,R0,#02
90             ;STR      R0,[R1]
91             ;CPSIE    I
92
93
94             BX        LR
95
96             ENDP
97             ALIGN
98             END
```

```

1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;          ADC0 INITIALIZATION OF Q1          ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  RCGCADC          EQU 0x400FE638 ; ADC clock register
6  ; ADC0 base address EQU 0x40038000
7  ADC0_ACTSS       EQU 0x40038000 ; Sample sequencer (ADC0 base address)
8  ADC0_RIS         EQU 0x40038004 ; Interrupt status
9  ADC0_IM          EQU 0x40038008 ; Interrupt select
10 ADC0_EMUX        EQU 0x40038014 ; Trigger select
11 ADC0_PSSI        EQU 0x40038028 ; Initiate sample
12 ADC0_SSMUX3      EQU 0x400380A0 ; Input channel select
13 ADC0_SSCTL3      EQU 0x400380A4 ; Sample sequence control
14 ADC0_SSFIFO3     EQU 0x400380A8 ; Channel 3 results
15 ADC0_PC          EQU 0x40038FC4 ; Sample rate
16
17
18 ;LABEL          DIRECTIVE    VALUE          COMMENT
19 AREA init_adc, CODE, READONLY, ALIGN=2
20 THUMB
21
22 EXPORT          ADC0_Init
23
24 ADC0_Init       PROC
25 ;ADC CLOCK IS INITIALIZED IN PORTE INITIALIZATION.
26 ;LDR            R1, =RCGCADC      ; Turn on ADC clock
27 ;LDR            R0, [R1]
28 ;ORR            R0, R0, #0x01    ; set bit 0 to enable ADC0 clock
29 ;STR            R0, [R1]
30 ;NOP
31 ;NOP
32 ;NOP
33             ; Let clock stabilize
34             ; Disable sequencer while ADC setup
35 LDR            R1, =ADC0_ACTSS
36 LDR            R0, [R1]
37 BIC            R0, R0, #0x08    ; clear bit 3 to disable seq 3
38 STR            R0, [R1]
39             ; Select trigger source
40 LDR            R1, =ADC0_EMUX
41 LDR            R0, [R1]
42 BIC            R0, R0, #0xF000 ; clear bits 15:12 to select SOFTWARE
43 STR            R0, [R1] ; trigger
44             ; Select input channel
45 LDR            R1, =ADC0_SSMUX3
46 LDR            R0, [R1]
47 BIC            R0, R0, #0x000F ; clear bits 3:0 to select AIN0
48 STR            R0, [R1]
49             ; Config sample sequence
50 LDR            R1, =ADC0_SSCTL3
51 LDR            R0, [R1]
52 ORR            R0, R0, #0x06    ; set bits 2:1 (IE0, END0)
53 STR            R0, [R1]
54             ; Set sample rate
55 LDR            R1, =ADC0_PC
56 LDR            R0, [R1]
57 ORR            R0, R0, #0x01    ; set bits 3:0 to 1 for 125k sps
58 STR            R0, [R1]
59             ; Done with setup, enable sequencer
60 LDR            R1, =ADC0_ACTSS
61 LDR            R0, [R1]
62 ORR            R0, R0, #0x08    ; set bit 3 to enable seq 3
63 STR            R0, [R1] ; sampling enabled but not initiated yet
64
65 BX            LR
66 ENDP
67 ALIGN
68 END

```



```

1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;          GPIO PORTE INITIALIZATION OF Q2          ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  PE_INP          EQU      0X40024020 ;0000_0010_0000
6  GPIO_PORTE_DIR_R    EQU      0X40024400
7  GPIO_PORTE_AFSEL_R  EQU      0X40024420
8  GPIO_PORTE_DEN_R    EQU      0X4002451C
9  GPIO_PORTE_AMSEL_R  EQU      0X40024528
10 GPIO_PORTE_PDR      EQU      0X40024514 ;514
11 SYSCTL_RCGC2_R      EQU      0X400FE608
12 GPIO_PORTE_IS       EQU      0X40024404
13 GPIO_PORTE_IBE       EQU      0X40024408
14 GPIO_PORTE_IEV       EQU      0X4002440C
15 GPIO_PORTE_IM        EQU      0X40024410
16 GPIO_PORTE_ICR       EQU      0X4002441C
17 GPIO_PORTE_RIS       EQU      0X40024414
18 RCGCADC            EQU 0x400FE638 ; ADC clock register
19
20
21
22 ;LABEL            DIRECTIVE    VALUE                COMMENT
23                 AREA init_gpio, CODE,    READONLY,    ALIGN=2
24                 THUMB
25
26                 EXPORT          GPIOE_Init
27
28 ;ADC CLOCK IS THE FIRST THING INITIALIZED. OTHERWISE IT GIVES ERROR.
29
30 GPIOE_Init  PROC
31     ;ACTIVATE ADC CLOCK
32     LDR      R1, =RCGCADC      ; Turn on ADC clock
33     LDR      R0, [R1]
34     ORR      R0, R0, #0x01     ; set bit 0 to enable ADC0 clock
35     STR      R0, [R1]
36     NOP
37     NOP
38     NOP
39     ;ACTIVATE PORTE CLOCK
40     LDR      R1,=SYSCTL_RCGC2_R
41     LDR      R0, [R1]
42     ORR      R0,R0,#0x10 ;only port E
43     STR      R0, [R1]
44     NOP
45     NOP
46     NOP
47     ;SET DIRECTION REGISTER
48     LDR      R1,=GPIO_PORTE_DIR_R
49     LDR      R0, [R1]
50     BIC      R0,R0,#0x08      ;PE3 IS INPUT
51     STR      R0, [R1]
52     ;REGULAR PORT FUNCTION
53     LDR      R1,=GPIO_PORTE_AFSEL_R
54     LDR      R0, [R1]
55     ORR      R0,R0,#0x08      ;PE3 IS ALTERNATE
56     STR      R0, [R1]
57     ;PULLDOWN RESISTORS ON SWITCH PINS
58     ;LDR      R1,=GPIO_PORTE_PDR
59     ;MOV      R0,#0X0F
60     ;STR      R0, [R1]
61     ;DISABLE DIGITAL PORT
62     LDR      R1,=GPIO_PORTE_DEN_R
63     LDR      R0, [R1]
64     BIC      R0,R0,#0x08
65     STR      R0, [R1]
66     ;ENABLE ANALOG PORT
67     LDR      R1,=GPIO_PORTE_AMSEL_R
68     LDR      R0, [R1]
69     ORR      R0,R0,#0x08
70     STR      R0, [R1]
71     ;CONFIGURE INTERRUPT FOR PORTE PINS 0-3=INPUT
72     ;LDR      R1,=GPIO_PORTE_IS
73     ;LDR      R2,=GPIO_PORTE_IBE
74     ;LDR      R3,=GPIO_PORTE_IEV
75     ;LDR      R4,=GPIO_PORTE_IM
76     ;LDR      R5,=GPIO_PORTE_ICR
77

```

```
78             ;MOV      R0,#0X00
79             ;STR      R0,[R1]
80             ;STR      R0,[R2]
81             ;MOV      R0,#0X0F
82             ;STR      R0,[R3]
83             ;STR      R0,[R4]
84             ;STR      R0,[R5]
85
86             ;CONFIGURE NVIC
87             ;LDR      R1,=NVIC_ISER0
88             ;LDR      R0,[R1]
89             ;ORR      R0,R0,#02
90             ;STR      R0,[R1]
91             ;CPSIE    I
92
93
94             BX        LR
95
96             ENDP
97             ALIGN
98             END
```

```

1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;          ADC0 INITIALIZATION OF Q2          ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  RCGCADC          EQU 0x400FE638 ; ADC clock register
6  ; ADC0 base address EQU 0x40038000
7  ADC0_ACTSS       EQU 0x40038000 ; Sample sequencer (ADC0 base address)
8  ADC0_RIS         EQU 0x40038004 ; Interrupt status
9  ADC0_IM          EQU 0x40038008 ; Interrupt select
10 ADC0_EMUX        EQU 0x40038014 ; Trigger select
11 ADC0_PSSI        EQU 0x40038028 ; Initiate sample
12 ADC0_SSMUX3      EQU 0x400380A0 ; Input channel select
13 ADC0_SSCTL3      EQU 0x400380A4 ; Sample sequence control
14 ADC0_SSFIFO3     EQU 0x400380A8 ; Channel 3 results
15 ADC0_PC          EQU 0x40038FC4 ; Sample rate
16
17
18 ;LABEL          DIRECTIVE  VALUE          COMMENT
19 AREA init_adc, CODE, READONLY, ALIGN=2
20 THUMB
21
22 EXPORT          ADC0_Init
23
24 ADC0_Init       PROC
25 ;ADC CLOCK IS INITIALIZED IN PORTE INITIALIZATION.
26 ;LDR            R1, =RCGCADC      ; Turn on ADC clock
27 ;LDR            R0, [R1]
28 ;ORR            R0, R0, #0x01     ; set bit 0 to enable ADC0 clock
29 ;STR            R0, [R1]
30 ;NOP
31 ;NOP
32 ;NOP
33             ; Let clock stabilize
34             ; Disable sequencer while ADC setup
35 LDR            R1, =ADC0_ACTSS
36 LDR            R0, [R1]
37 BIC            R0, R0, #0x08      ; clear bit 3 to disable seq 3
38 STR            R0, [R1]
39             ; Select trigger source
40 LDR            R1, =ADC0_EMUX
41 LDR            R0, [R1]
42 BIC            R0, R0, #0xF000    ; clear bits 15:12 to select SOFTWARE
43 STR            R0, [R1] ; trigger
44             ; Select input channel
45 LDR            R1, =ADC0_SSMUX3
46 LDR            R0, [R1]
47 BIC            R0, R0, #0x000F    ; clear bits 3:0 to select AIN0
48 STR            R0, [R1]
49             ; Config sample sequence
50 LDR            R1, =ADC0_SSCTL3
51 LDR            R0, [R1]
52 ORR            R0, R0, #0x06      ; set bits 2:1 (IE0, END0)
53 STR            R0, [R1]
54             ; Set sample rate
55 LDR            R1, =ADC0_PC
56 LDR            R0, [R1]
57 ORR            R0, R0, #0x01      ; set bits 3:0 to 1 for 125k sps
58 STR            R0, [R1]
59             ; Done with setup, enable sequencer
60 LDR            R1, =ADC0_ACTSS
61 LDR            R0, [R1]
62 ORR            R0, R0, #0x08      ; set bit 3 to enable seq 3
63 STR            R0, [R1]          ; sampling enabled but not initiated yet
64
65 BX             LR
66 ENDP
67 ALIGN
68 END

```

```

1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;          GPIO PORTE INITIALIZATION OF Q3          ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  PE_INP          EQU      0X40024020 ;0000_0010_0000
6  GPIO_PORTE_DIR_R    EQU      0X40024400
7  GPIO_PORTE_AFSEL_R  EQU      0X40024420
8  GPIO_PORTE_DEN_R    EQU      0X4002451C
9  GPIO_PORTE_AMSEL_R  EQU      0X40024528
10 GPIO_PORTE_PDR      EQU      0X40024514 ;514
11 SYSCTL_RCGC2_R      EQU      0X400FE608
12 GPIO_PORTE_IS       EQU      0X40024404
13 GPIO_PORTE_IBE       EQU      0X40024408
14 GPIO_PORTE_IEV       EQU      0X4002440C
15 GPIO_PORTE_IM        EQU      0X40024410
16 GPIO_PORTE_ICR       EQU      0X4002441C
17 GPIO_PORTE_RIS       EQU      0X40024414
18 RCGCADC            EQU 0x400FE638 ; ADC clock register
19
20
21
22 ;LABEL            DIRECTIVE    VALUE                COMMENT
23                 AREA init_gpio, CODE,    READONLY,    ALIGN=2
24                 THUMB
25
26                 EXPORT          GPIOE_Init
27
28 ;ADC CLOCK IS THE FIRST THING INITIALIZED. OTHERWISE IT GIVES ERROR.
29
30 GPIOE_Init  PROC
31     ;ACTIVATE ADC CLOCK
32     LDR      R1, =RCGCADC      ; Turn on ADC clock
33     LDR      R0, [R1]
34     ORR      R0, R0, #0x01     ; set bit 0 to enable ADC0 clock
35     STR      R0, [R1]
36     NOP
37     NOP
38     NOP
39     ;ACTIVATE PORTE CLOCK
40     LDR      R1,=SYSCTL_RCGC2_R
41     LDR      R0, [R1]
42     ORR      R0,R0,#0x10 ;only port E
43     STR      R0, [R1]
44     NOP
45     NOP
46     NOP
47     ;SET DIRECTION REGISTER
48     LDR      R1,=GPIO_PORTE_DIR_R
49     LDR      R0, [R1]
50     BIC      R0,R0,#0x08      ;PE3 IS INPUT
51     STR      R0, [R1]
52     ;REGULAR PORT FUNCTION
53     LDR      R1,=GPIO_PORTE_AFSEL_R
54     LDR      R0, [R1]
55     ORR      R0,R0,#0x08      ;PE3 IS ALTERNATE
56     STR      R0, [R1]
57     ;PULLDOWN RESISTORS ON SWITCH PINS
58     ;LDR      R1,=GPIO_PORTE_PDR
59     ;MOV      R0,#0X0F
60     ;STR      R0, [R1]
61     ;DISABLE DIGITAL PORT
62     LDR      R1,=GPIO_PORTE_DEN_R
63     LDR      R0, [R1]
64     BIC      R0,R0,#0x08
65     STR      R0, [R1]
66     ;ENABLE ANALOG PORT
67     LDR      R1,=GPIO_PORTE_AMSEL_R
68     LDR      R0, [R1]
69     ORR      R0,R0,#0x08
70     STR      R0, [R1]
71     ;CONFIGURE INTERRUPT FOR PORTE PINS 0-3=INPUT
72     ;LDR      R1,=GPIO_PORTE_IS
73     ;LDR      R2,=GPIO_PORTE_IBE
74     ;LDR      R3,=GPIO_PORTE_IEV
75     ;LDR      R4,=GPIO_PORTE_IM
76     ;LDR      R5,=GPIO_PORTE_ICR
77

```

```
78             ;MOV      R0,#0X00
79             ;STR      R0,[R1]
80             ;STR      R0,[R2]
81             ;MOV      R0,#0X0F
82             ;STR      R0,[R3]
83             ;STR      R0,[R4]
84             ;STR      R0,[R5]
85
86             ;CONFIGURE NVIC
87             ;LDR      R1,=NVIC_ISER0
88             ;LDR      R0,[R1]
89             ;ORR      R0,R0,#02
90             ;STR      R0,[R1]
91             ;CPSIE    I
92
93
94             BX        LR
95
96             ENDP
97             ALIGN
98             END
```

```

1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;          ADC0 INITIALIZATION OF Q3                      ;
3  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
4
5  RCGCADC          EQU 0x400FE638 ; ADC clock register
6  ; ADC0 base address EQU 0x40038000
7  ADC0_ACTSS       EQU 0x40038000 ; Sample sequencer (ADC0 base address)
8  ADC0_RIS         EQU 0x40038004 ; Interrupt status
9  ADC0_IM          EQU 0x40038008 ; Interrupt select
10 ADC0_EMUX        EQU 0x40038014 ; Trigger select
11 ADC0_PSSI        EQU 0x40038028 ; Initiate sample
12 ADC0_SSMUX3      EQU 0x400380A0 ; Input channel select
13 ADC0_SSCTL3      EQU 0x400380A4 ; Sample sequence control
14 ADC0_SSFIFO3     EQU 0x400380A8 ; Channel 3 results
15 ADC0_PC          EQU 0x40038FC4 ; Sample rate
16
17
18 ;LABEL           DIRECTIVE   VALUE                               COMMENT
19 AREA init_adc,   CODE,      READONLY,   ALIGN=2
20 THUMB
21
22 EXPORT          ADC0_Init
23
24 ADC0_Init       PROC
25 ;ADC CLOCK IS INITIALIZED IN PORTE INITIALIZATION.
26 ;LDR            R1, =RCGCADC    ; Turn on ADC clock
27 ;LDR            R0, [R1]
28 ;ORR            R0, R0, #0x01   ; set bit 0 to enable ADC0 clock
29 ;STR            R0, [R1]
30 ;NOP
31 ;NOP
32 ;NOP
33             ; Let clock stabilize
34             ; Disable sequencer while ADC setup
35 LDR          R1, =ADC0_ACTSS
36 LDR          R0, [R1]
37 BIC          R0, R0, #0x08      ; clear bit 3 to disable seq 3
38 STR          R0, [R1]
39             ; Select trigger source
40 LDR          R1, =ADC0_EMUX
41 LDR          R0, [R1]
42 BIC          R0, R0, #0xF000    ; clear bits 15:12 to select SOFTWARE
43 STR          R0, [R1] ; trigger
44             ; Select input channel
45 LDR          R1, =ADC0_SSMUX3
46 LDR          R0, [R1]
47 BIC          R0, R0, #0x000F    ; clear bits 3:0 to select AIN0
48 STR          R0, [R1]
49             ; Config sample sequence
50 LDR          R1, =ADC0_SSCTL3
51 LDR          R0, [R1]
52 ORR          R0, R0, #0x06      ; set bits 2:1 (IE0, END0)
53 STR          R0, [R1]
54             ; Set sample rate
55 LDR          R1, =ADC0_PC
56 LDR          R0, [R1]
57 ORR          R0, R0, #0x01      ; set bits 3:0 to 1 for 125k sps
58 STR          R0, [R1]
59             ; Done with setup, enable sequencer
60 LDR          R1, =ADC0_ACTSS
61 LDR          R0, [R1]
62 ORR          R0, R0, #0x08      ; set bit 3 to enable seq 3
63 STR          R0, [R1]          ; sampling enabled but not initiated yet
64
65 BX           LR
66 ENDP
67 ALIGN
68 END

```